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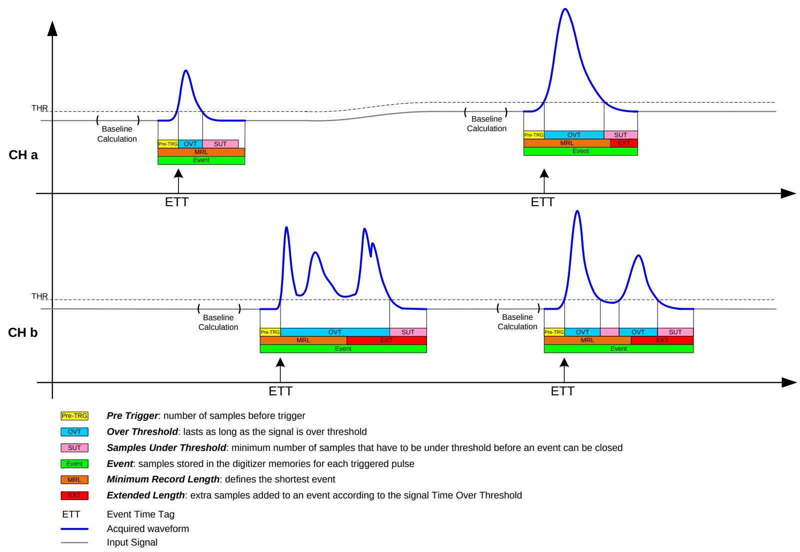
Electronic Instrumentation



User Manual UM5954

DPP-DAW

Digital Pulse Processing for Dynamic Acquisition Window

Rev. 2 - May 7th, 2020

Purpose of this Manual

The User Manual contains the full description of the DPP-DAW firmware for 724, 725 and 730 series. The description is compliant with the DPP-DAW firmware revision **4.17_137.7** for 724 series, **4.17_141.3** for 725 and 730 series and **4.22_141.130** for 725S and 730S series. For future release compatibility, check in the firmware history files.

Change Document Record

Date	Revision	Changes
June 5th, 2019	00	Initial Release
July 12th, 2019	01	Added support to DPP-DAW for 724 series. Added Online Commands for 725 and 730 series.
May 7th, 2020	03	Added support to 725S and 730S series.

Symbols, abbreviated terms and notation

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
DPP	Digital Pulse Processing
DPP-DAW	DPP for Dynamic Acquisition Window
LVDS	Low-Voltage Differential Signal
ROC	ReadOut Controller
USB	Universal Serial Bus

Reference Documents

[RD1] UM1935 – CAENDigitizer User & Reference Manual.

[RD2] UM5913 – 724 DPP-DAW Registers Description.

[RD3] UM6237 – 725-730 DPP-DAW Registers Description.

All CAEN documents can be downloaded at:
`www.caen.it/support-services/documentation-area`

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MADE IN ITALY: We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (while this is true for the boards marked ”MADE IN ITALY”, we cannot guarantee for third-party manufactures).

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1 Introduction

This manual describes the special DPP firmware for Dynamic Acquisition Window (DPP-DAW firmware) designed for 724, 725 and 730 digitizer families. The board configuration and the DAW acquisition can be managed through a demo software, which relies on CAENDigitizer library functions **[RD1]**. Customers can take advantage of the library functions and the C sources of the demo to develop and customize their own acquisition software.

The DPP-DAW firmware allows the user to acquire data from each channel independently and to adapt the acquisition window to the real pulse duration (over-threshold). Samples are identified when their distance from the baseline is larger than a programmable threshold. After the minimum record length is reached, the DPP-DAW firmware acquires the input samples until they return below the threshold level for a programmable number of samples. The acquisition can be vetoed/gated with an external signal on TRG-IN front panel connector.

The DPP-DAW firmware has many advantages with respect to the default firmware for waveform recording, like the possibility to acquire each channel independently (the default firmware acquires with global trigger logic), and the possibility to adjust the record length of each event individually (the default firmware acquires with a fixed record length). This ensures an optimization of the data transfer, since only the ”relevant” samples are transmitted, while channels with no data are not transferred at all.

2 Principle of Operation

The Digital Pulse Processing for Dynamic Acquisition Window (DPP-DAW) is a special firmware developed for 724, 725 and 730 CAEN digitizer families.

The firmware identifies an event when its samples exceed a programmable threshold value relative to the signal baseline (0-Volt level). The user can decide to write a fixed value of baseline level (see register 0x1n64 **[RD2], [RD3]**), or to let the algorithm evaluate it as the mean value of a moving average window (the number of samples to be averaged can be set through bits [22:20] of register 0x8000). The trigger threshold and the polarity can be set through registers 0x1n60 and bit[16] of register 0x1n80 respectively. The polarity defines whether a trigger is issued for the samples under the threshold (negative polarity) or over the threshold (positive polarity).

The relevant samples are identified when the following condition is met:

$$(S_i - BSL) > TRG\_Thr, \text{ for positive polarity}$$

$$(BSL - S_i) > TRG\_Thr, \text{ for negative polarity}$$

where S_i is the i^{th} sample, BSL is the baseline value, and TRG_Thr is the threshold value.

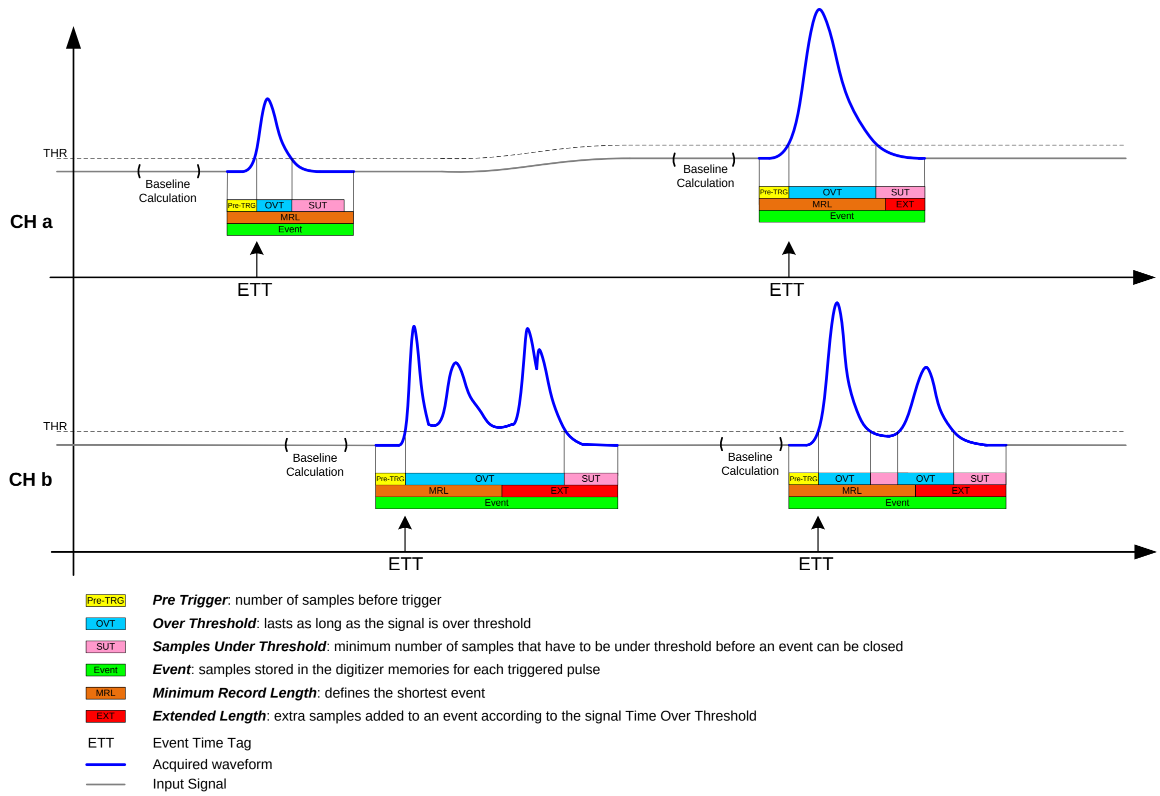

Fig. 2.1: DAW algorithm description

All these functions can be set either through CAENDigitizer library functions, as shown in the demo software, or through direct firmware register writes.

The firmware first acquires the full record length, then it waits for the samples to return below the threshold value (positive polarity) for at least a programmable number of samples (see register 0x1n78). The event is therefore fully acquired and saved into memory. If the memory is full or busy, the event is truncated. It is possible to select whether it is acquired and tagged in the data (see bit[29] of the SIZE word - Fig. **2.3**) or it is rejected. **Da capire per il 724...**

The firmware continues the data acquisition until the under threshold condition is met. It is possible to set a maximum time after which the firmware stops anyway the acquisition and starts a new baseline calculation (see register 0x1n7C). This can be useful in case there is a jump in the baseline and the signal does not return below the threshold.

It is also possible to set an external veto/gate (see bits[13:12] of register 0x8000) on the TRG IN front panel connector. Inputs can also be delayed to be synchronous with the external signal (register 0x1n34). In case of 724 series, if the veto signal ends when the input is still over-threshold,an artificial then trigger is issued and the tail of the signal is acquired. If the veto occurs within the acquisition window, the event is discarded.

Fig. **2.1** shows the parameters of the DAW algorithm for two channels called ”CHa” and ”CHb”.
The signal recording starts N samples before according to the Pre-Trigger value (see register 0x1n38). The full over-threshold signal is acquired until the input reaches the ”SUT” (samples under threshold) region. The record length value is the minimum value of the acquisition window which is acquired even if the signal return below the threshold. Samples outside the ROI (region of interest) are discarded.

Event Structure

An event is structured as:

- **Header** (four 32-bit words)
- **Data** (variable size and format)

Header

The event Header consists of four words including the following information:

- **EVENT SIZE** (bits[27:0] of 1st header word) is the total size of the event, i.e. the number of 32-bit long words to be read.
- **BOARD ID** (bits[31:27] of 2nd header word) is the GEO address, meaningful for VME64X modules.
- **BOARD FAIL FLAG** (bit[26] of 2nd header word) is set to "1" in consequence of a hardware problem (e.g. PLL unlocking). The user can collect more information about the cause by reading register 0x8104 and contacting CAEN Support Service if necessary (see Chap. **Technical Support**).
- **PATTERN** (bits[23:8] of 2nd header word) where PATTERN is the 16-bit PATTERN latched on the LVDS I/Os as the trigger arrives (VME only).
- **CHANNEL MASK[7:0]** (and **CHANNEL MASK[15:8]** in case of 725-730 VME) (bits[7:0] of 2nd header word (and bits[31:24] of the 3rd header word)) is the mask of the channels participating in the event (e.g. CH5 and CH7 participating → Channel Mask = 0xA). This information must be used by the software to associate each data section to the correct channel (the first event contains the samples from the channel with the lowest index).
- **BOARD EVENT COUNTER** (bits[23:0] of 3rd header word) is the number of events created in the board memory.
- **BOARD EVENT TIME TAG** (bits[31:0] of 4th header word) is the time of creation of the event in the board (this does not correspond to any real physical event).

Data (724 series)

The data section in case of 724 series for each enabled channels is made by a channel header for each active channel and by the data of the corresponding channel. The channel header are two 32-bit words reporting the following information:

- **CHANNEL SIZE** (bits[22:0] of the first word) is the size of the channel, i.e. the number of 32-bit long words to be read for the specific channel.
- **TRIGGER TIME STAMP** (bits[29:0] of the second word) is the trigger time stamp of the event in the channel.

The channel header is followed by a sequence of the acquired samples.

An example of data format is reported in Fig. **2.2**

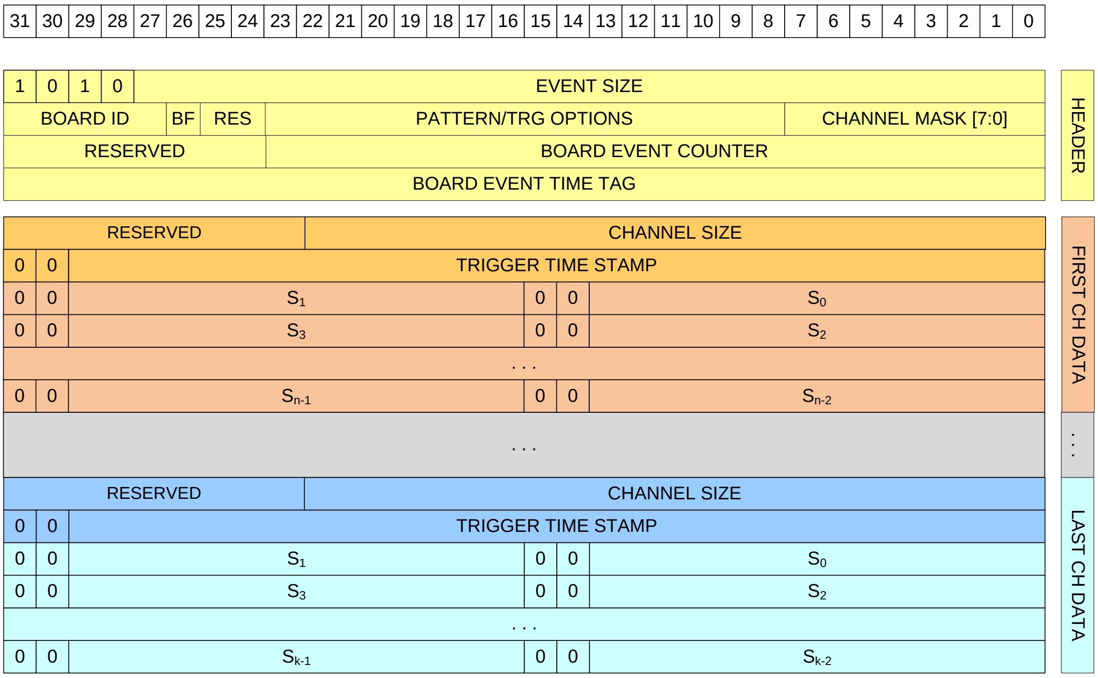

Fig. 2.2: 724 series event format example

Data (725 and 730 series)

The data section in case of 725 and 730 series for each enabled channel is made by a channel header for each active channel and by the data of the corresponding channel. The user must indeed take into account that even if a channel is enabled it will not be present in the events if it has no data. The channel header counts of three 32-bit words reporting the following information:

- **TRUNC** (bit[29] of the first word) is a flag indicating whether the event is truncated.
- **CHANNEL SIZE** (bits[22:0] of the first word) is the size of the channel, i.e. the number of 32-bit long words to be read for the specific channel.
- **TRIGGER TIME STAMP (32 LSBs)** (second word) contains the 32 LSB of the channel trigger time stamp.
- **BASELINE** (bits[29:16] of the third word) is the baseline value of the event in the channel.
- **TRIGGER TIME STAMP (16 MSBs)** (bits[15:0] of the third word) counts the 16 MSB of the channel trigger time stamp.

The channel header is followed by the acquired samples.

The data format is schematically reported in Fig. **2.3**

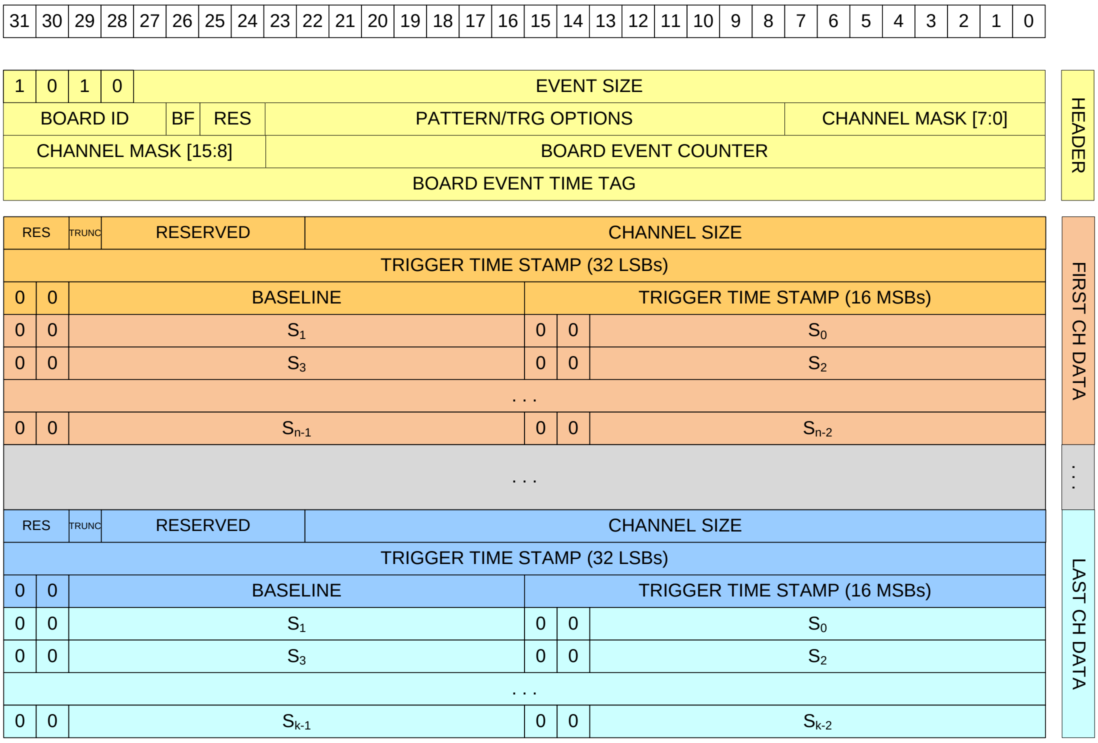

Fig. 2.3: 725 and 730 series event format example

Notes on Firmware and Licensing

The DPP-DAW firmware runs on 724, 725 and 730 digitizer series. The supported digitizer models and the DPP firmware license are listed in the table below.

Desktop Digitizer	Description
DT5724(*)	4 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
DT5724A(*)	2 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
DT5724B	4 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE
DT5724C	2 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE
DT5724D(*)	4 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, SE
DT5724E(*)	2 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, SE
DT5724F	4 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE
DT5724G	2 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE
DT5725	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
DT5725B	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
DT5725S	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
DT5725SB	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
DT5730	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
DT5730B	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
DT5730S	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
DT5730SB	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
NIM Digitizer	**Description**
N6724(*)	4 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
N6724A(*)	2 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
N6724B	4 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch,C20, SE
N6724C	2 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE
N6724F	4 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch,C20, SE
N6724G	2 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE
N6725	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
N6725B	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
N6725S	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
N6725BS	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
N6730	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
N6730B	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
N6730S	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
N6730BS	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
Desktop Digitizer	**Description**
V1724(*)	8 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
V1724B(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, SE
V1724C(*)	8 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, DIFF
V1724D(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, DIFF
V1724E	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE
V1724F(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, DIFF
V1724G	8 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE
V1725	16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
V1725B	16 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1725C	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
V1725D	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1725S	16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
V1725BS	16 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1725CS	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE

V1725DS	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1730	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
V1730B	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1730C	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
V1730D	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1730S	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
V1730BS	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1730CS	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
V1730DS	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1724(*)	8 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
VX1724B(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, SE
VX1724C(*)	8 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, DIFF
VX1724D(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, DIFF
VX1724E	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE
VX1724F(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, DIFF
VX1725	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1725B	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1725C	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1725D	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1725S	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1725BS	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1725CS	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1725DS	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1730	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1730B	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1730C	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1730D	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1730S	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1730BS	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1730CS	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1730DS	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
DPP Firmware	**Description**
DPP-DAW (4/2ch x 724)	Digital Pulse Processing with Dynamic Acquisition Window (4/2ch x 724)
DPP-DAW (8ch x 724)	Digital Pulse Processing with Dynamic Acquisition Window (8ch x 724)
DPP-DAW (8ch x 725)	Digital Pulse Processing with Dynamic Acquisition Window (8ch x 725)
DPP-DAW (16ch x 725)	Digital Pulse Processing with Dynamic Acquisition Window (16ch x 725)
DPP-SUP 16ch x725	DPP-SUP - Super Licence for 16ch x725 Digital Pulse Processing
DPP-SUP 8ch x725	DPP-SUP - Super Licence for 8ch x725 Digital Pulse Processing
DPP-DAW (8ch x 730)	Digital Pulse Processing with Dynamic Acquisition Window (8ch x 730)
DPP-DAW (16ch x 730)	Digital Pulse Processing with Dynamic Acquisition Window (16ch x 730)
DPP-SUP (16ch x730)	DPP-SUP - Super Licence for 16ch x730 Digital Pulse Processing
DPP-SUP (8ch x730)	DPP-SUP - Super Licence for 8ch x730 Digital Pulse Processing

(*) The board is currently obsolete.

Tab. 2.1: Compliance table of the DPP-DAW with CAEN digitizers and DPP firmware.

3 DAW Demo Software Interface

CAEN provides a C demo software for the DPP-DAW readout. The user can either use the software to collect the data or take the source codes as an example to access the CAENDigitizer library functions and develop his/her own customized readout program. The package includes the C source files, the Visual Studio project, and (for the Linux version) the Linux Makefile.

Installation

In order to be able to install the demo software, the host station needs Windows or Linux OS. CAEN provides the full installation package for the DPP-DAW demo software in a standalone version for Windows and Linux OS. This version installs all the binary files and required libraries.

1. Download the DPP-DAW demo software for your OS from CAEN Website under the path:
   `www.caen.it/download/?filter=DPP-DAW`
   which are called ”DAW Demo” and ”CAEN WaveCut” for 725-730 and 724 series respectively.
2. Extract the files

Linux Installation

To install the software type the following commands

```
./configure
make
sudo make install
```

To launch the software type

`DAW_Demo` for 725 and 730 series
`WaveCut` for 724 series

The default configuration file, called `DAW_Config.txt/Wavecut_Config.txt` is located under the path `/etc/DAW_Demo//etc/Wavecut` respectively. Since that location requires administrator rights, it is possible to launch the software in the local installation folder, by typing

`DAW_Demo DAW_Config.txt` for 725 and 730 series
`Wavecut Wavecut_Config.txt` for 724 series

At the first launch the software automatically created a folder for the output files, in the home path, called `DAW_output` (725 and 730 series only).

Windows Installation

Run the executable “CAENDAW_DemoSetup-x.exe” for 725-730 series, and ”CAENWaveCutSetup-x.exe” for 724 series. The Setup Wizard will guide you throughout the installation procedure.

Note: The Windows OS must be up-to-date to correctly install the Visual C++ Redistributable (see Figs. **3.6**, **3.7**, and **3.8**).

Note: The following screenshots are taken with “CAENDAW_DemoSetup-x.exe” for 725-730 series in a Window 10 OS, but they can be generalized for 724 series and Windows 7, Windows 8 OS.

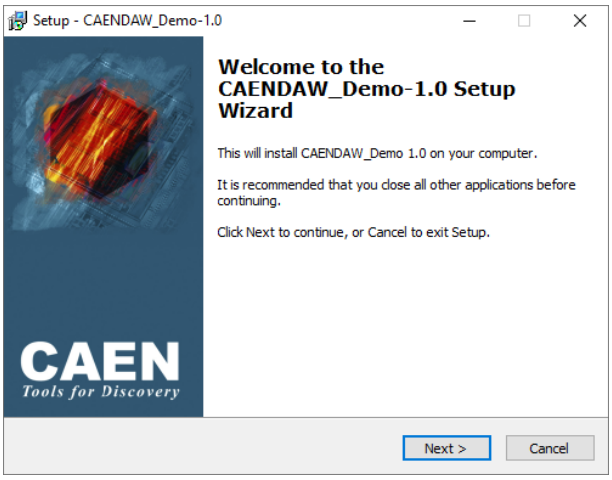

Fig. 3.1: DPP-DAW demo Wizard Dialog Box - Start Installation.

Left click on “**Next**” (or left click on “**Cancel**” any time during the installation process to abort the installation).

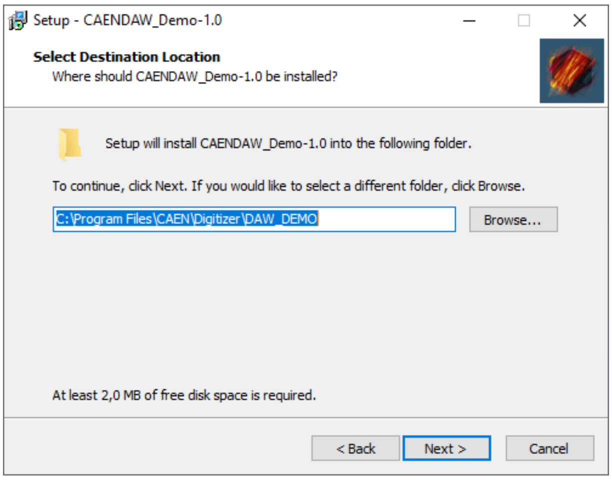

Fig. 3.2: DPP-DAW demo Wizard Dialog Box - Installation Path.

Left click on “**Next**” (or left click on “**Back**” at any time during the installation process to modify the previous settings).

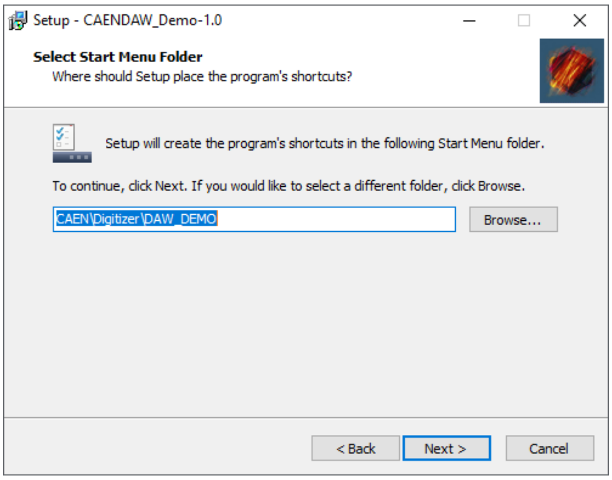

Fig. 3.3: DPP-DAW demo Wizard Dialog Box - Start Menu Folder Path.

Left click on “**Next**” to continue.

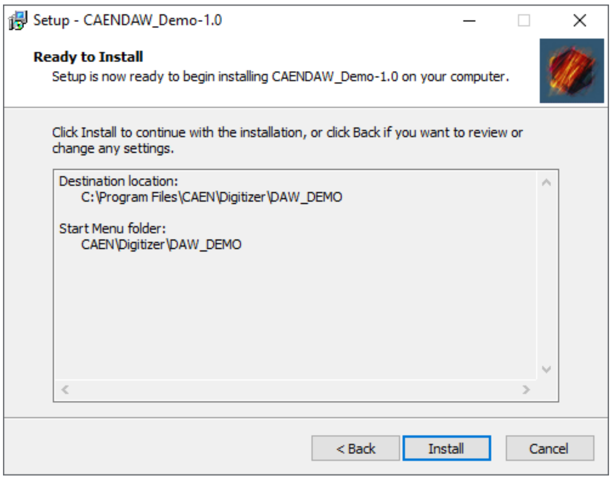

Fig. 3.4: DPP-DAW demo Wizard Dialog Box - Installation Summary.

Left click on “**Install**” to install the CAEN DPP-DAWDemo Software.

The DPP-DAW demo Setup Wizard will extract and install the relevant files.

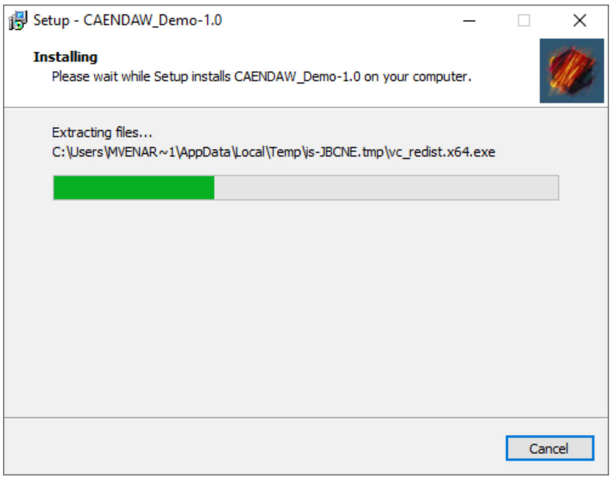

Fig. 3.5: DPP-DAW demo Wizard Dialog Box - Installation progress.

The DPP-DAW demo Setup Wizard will then install Microsoft Visual C++ 2015 Redistributable as needed requirement.

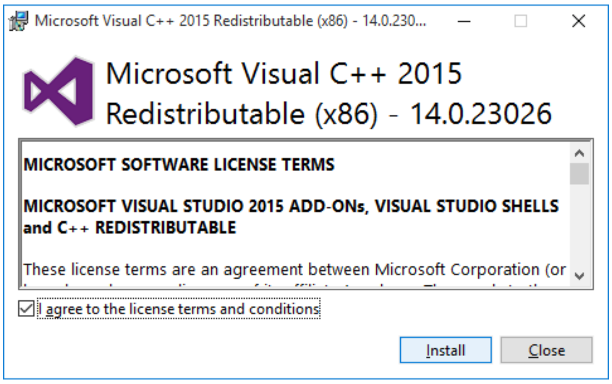

Fig. 3.6: DPP-DAW demo Wizard Dialog Box - Microsoft Visual C++ 2015 Redistributable installation start.

If the Wizard detects an already present installation it will abort the procedure. In case no installation is found the Wizard will proceed.

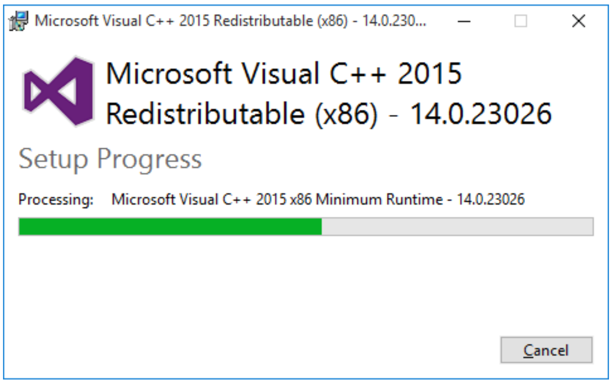

Fig. 3.7: DPP-DAW demo Wizard Dialog Box - Microsoft Visual C++ 2015 Redistributable installation ongoing.

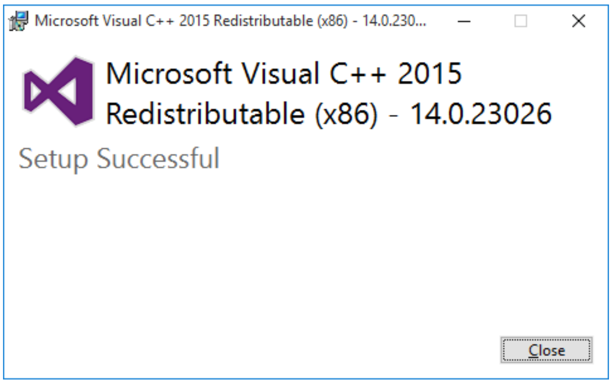

Fig. 3.8: DPP-DAW demo Wizard Dialog Box - Microsoft Visual C++ 2015 Redistributable installation completed.

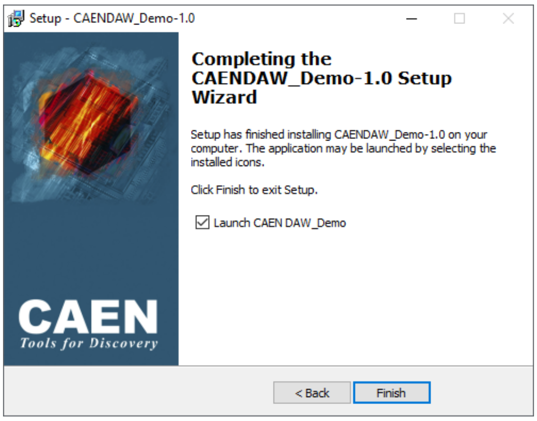

Fig. 3.9: DPP-DAW demo Wizard Dialog Box - Finish Installation.

To complete the DPP-DAW demo Installation left click on "**Finish**".

The DPP-DAW Demo Program is installed under the path

`C:\Program Files\CAEN\Digitizers\DAW_DEMO` for 725-730 series and
`C:\Program Files\CAEN\Digitizers\WaveCut` for 724 series.

Since the folder requires administrator rights, it is created a running folder under the path:

`C:\Users\USER_NAME\DAW_Demo` for 725-730 series and
`C:\Users\USER_NAME\WaveCut` for 724 series.

The software can be launched by double clicking in the `DAW_Demo.exe/WaveCut.exe` icon. The configuration file is called `DAW_Demo.txt/WaveCut_Config.txt` and it can be directly modified with user rights. In addition, a folder for the output files is created, called `DAW_output` (725 and 730 series only).

724 On-line commands

At start-up, the demo software retrieves general information from the digitizer, program it and waits for the start of the acquisition ('s' key). The table below lists the accepted on-line commands associated to specific keys.

Key	Function
s	Start acquisition.
S	Stop acquisition.
t	Single Software Trigger; this command sends a software trigger (single shot), useful especially when the card has no data (no trigger) because it forces the acquisition of an event. In analogy with the oscilloscope, this command corresponds to the "Force trigger" button.
T	Continuous Software Trigger; this command enables / disables the continuous generation of software trigger at a fixed rate. Inside the acquisition loop, the program sends a trigger, reads the corresponding event and executes data analysis. It corresponds to the "Auto trigger" of the oscilloscope.
W	Continuous Event Saving; this command enables / disables the continuous events saving to file. It creates one file per channel and it writes the events consecutively. The file format is selected via configuration file (see command OUTPUT_FILE_FORMAT).
b	In case of multi-board systems, this command selects the board whose channels are plotted.
c	This command selects the channel to be plotted. Write the corresponding channel number after the 'c' command.
0, ..., 7	This command enables / disables channel n (n = 0 .. 7) from the plot (if such channel is enabled).
w	Continuous Plot; this command enables / disables the continuous plot of the enabled channels. When enabled, the input signal trace of channel 0 is plotted by default. Check the 'c' command to enable the other channels.
i	This command enables the dump of all the board firmware registers. This feature can be useful for debug purposes.
q	This command quits the software.
Space	This command displays the online help.

Tab. 3.1: Software on-line commands.

Inside the Gnuplot window, there are active bindkeys and functions associated to the mouse:

Key	Function
a	x and y-axis auto-scale.
r	Enable / Disable ruler.
g	Enable / Disable grid.
p	Return to previous zoom.

Tab. 3.2: Gnuplot on-line commands.

Zoom Area: right click on one corner of the area, release the button, left click on the opposite corner.

Click with the right button on the window bar to open a menu that allows to make the print, copy the screen-shot to the clipboard, change colours, etc.

724 Config File Sintax

The configuration file is located in the main software folder and it is called ”WaveCut_Config.txt”.

The setting modes can be [COMMON] (all boards-related), ”[BOARD] #” (single board-related) or ”[CHANNEL] #” (single channel-related).

If a setting is CHANNEL-related, it can also be BOARD-related or COMMON (i.e. the setting refers to all the channels in all the boards of the system). However not all options that are COMMON can also be BOARD- or CHANNEL-related. The ”[BOARD] #” or ”[CHANNEL] #” directives have no effect on such settings. The ”[BOARD] #” and ”[CHANNEL] #” modes are alternative to [COMMON] but do not exclude each other. This means that one can issue a command to a specific channel of a specific board, to all channels of a specific board or to a specific channel of all boards.

When the ”[BOARD] #” mode is set, the following settings apply to all channels (even if a specific channel was previously selected). The board index follows the board initialization order using the OPEN command (see below). The lines between the commands @OFF and @ON will be skipped. This can be used to exclude parts of the config file.

Board Settings

OPEN `LinkType LinkNumber NodeNumber BaseAddress`

Specifies the path of the physical channel to open communication with the digitizer:

`LinkType`	Identifies the type of communication channel, choosing between USB and PCI. USB corresponds to both the direct connection from PC to digitizer (Desktop models or NIM), and the connection through V1718 and VME bus (VME models). PCI corresponds to both the direct connection from PC A2818 (PCI controller) or A3818 (PCIe controller) to the digitizer through optical fibre (all models), and connection through V2718 and VME bus (VME models).
`LinkNumber`	The number of the connection. It is typically 0 (only one digitizer connection to the PC); in case of many digitizers connected it is necessary to specify which has to be accessed. Remember that the DPP-DAW Control Software demo can handle only one digitizer at a time. LinkNumber identifies which USB or A2818/A3818 is in use. Be aware that it is not known in advance which LinkNumber corresponds to which USB port or PCI slot.
`NodeNumber`	This parameter must be specified only when connected via optical link (PCI) and indicates the node in the daisy chain. It is typically 0 (only one digitizer in the optical chain), it may be different if more than one digitizer (or V2718) is connected in a daisy chain.
`BaseAddress`	Indicates the Base Address (32-bit hexadecimal number) to access the digitizer via the VME bus. This number should be 0 for direct connections from a PC to a digitizer.

Common Settings

START_MODE `option`

This command specifies the source of the start acquisition. The possible `options` are:

`INDEP_SW`: a software command starts the acquisition;

`SYNC_S_IN`: the acquisition is synchronized with the logic level of an external signal feed into the S-IN front panel connector. The connection TRG OUT->S IN must be done from each board of the system (master to first slave, etc) to propagate the RUN.

OUT_FILE_FORMAT `option`

Defines the format of the output file. To enable the output dump press 'W' in the command window. The possible `options` are:

`BINARY`, all the acquired waveform are saved in a .dat file where the format is defined in Sec. **Event Structure**;

`ASCII`, waveform samples are reported in a single column. For each event is also reported the time stamp (Ts) and the number of samples (Ns). The output file is in the .txt format.

FPIO_TYPE `option`

Indicates the electrical level for the front panel LEMO I/Os (TRG IN, TRG OUT and S IN for VME; TRG IN, GPI and GPO for Desktop and NIM). The possible `options` are:

`TTL` if the desired I/O level is TTL,

`NIM` if the desired I/O level is NIM.

TRIGGER_MODE `option`

Selects the trigger source. The possible `options` are:

`SELF_TRIGGER` to use the channel self-trigger;

`EXT_TRIGGER` to use the external trigger from TRG IN front panel connector.

VETO_MODE `option`

Selects the veto mode. The veto signal can be fed into the TRG IN front panel connector. The possible `options` are:

`VETO_DISABLED` to disable the veto;

`VETO_ACTIVE_HIGH` to veto the acquisition when the veto signal is in a logic high state;

`VETO_ACTIVE_LOW` to veto the acquisition when the veto signal is in a logic high state. In this case the veto acts as a gate.

INPUT_DELAY `value`

Defines the number of delay samples (where 1 sample corresponds to 10 ns for 724 series) that are added to the input waveform.

`value` is an integer value ranging from 2 to 511. The number of input delay samples corresponds to `value` · 2.

RECORD_LENGTH `value`

Indicates the minimum number of samples (where 1 sample corresponds to 10 ns for 724 series) to be acquired for each trigger in one acquisition window.

> `value` is an integer value ranging from 4 to 2097150. The number of record length samples corresponds to `value` · 2. `value` must be an even number.

PRE_TRIGGER `value`

Defines the number of samples to be acquired in the acquisition window before the trigger.

> `value` is an integer value ranging from 2 to 511. The number of pre trigger samples corresponds to `value` · 2.

PULSE_POLARITY `value`

Sets the trigger polarity. The possible `values` are:

> `POSITIVE`: trigger condition met for over-threshold samples;
>
> `NEGATIVE`: trigger condition met for under-threshold samples.

Individual Settings

Individual settings are written under the [CHANNEL n] command, where n is the channel index. If they are written in the common settings area, then they are applied to all channels at the same time.

ENABLE_INPUT `option`

This command enables or disables the corresponding channel for the acquisition. Possible `options` are:

> `YES` to enable it;
>
> `NO` to disable it.

DC_OFFSET `value`

The DC_OFFSET allows to shift the input dynamics (-FSR / 2 to +FSR / 2, where FSR is the full scale range, 2 V_{pp} or 0.5 V_{pp} for 730 and 725 series) towards negative or positive values.

> `value` ranges from -50 to 50, where -50 corresponds to a signal dynamics from -FSR to 0 (completely negative signal), and 50 corresponds to a signal dynamics from 0 to FSR (completely positive signal). The default value is 0, corresponding to the signal dynamics of -FSR / 2 to +FSR / 2 (bipolar signal).

Note: the dynamic range of the DAC does not correspond exactly to the ADC range, so there is not an exact correspondence between the 0-level of DC offset and the baseline at mid-scale of the ADC channels.

TRIGGER_THRESHOLD `value`

Sets the trigger threshold relative to the baseline value.

> `value` is an integer value ranging from 0 to 16383.

BASELINE_SAMPLES `option`

Sets the number of samples of a moving windows for the baseline calculation. Possible `options` are:

0 = the baseline is not calculated and the **TRIGGER_THRESHOLD** `value` is an absolute value;

1 = 16 samples;

2 = 32 samples;

3 = 64 samples;

4 = 128 samples;

5 = 256 samples;

6 = 512 samples;

7 = 1024 samples.

N_LFW `value`

Defines the number of samples to be acquired when the pulse exits the over-threshold condition.

`value` is an integer value ranging from 0 to 511. The number of samples corresponds to `value` · 2. When `value` = 0, then the minimum record length is acquired.

725-730 On-line commands

At start-up, the demo software retrieves general information from the digitizer, program it and waits for the start of the acquisition ('s' key). The table below lists the accepted on-line commands associated to specific keys.

Key	Function
s	Start/Stop acquisition.
t	Single Software Trigger; this command sends a software trigger (single shot), useful especially when the card has no data (no trigger) because it forces the acquisition of an event. In analogy with the oscilloscope, this command corresponds to the "Force trigger" button.
p	This command plots a single event.
g	This command select which octet (ch0-ch7 or ch8-ch15) is plotted.
1-8	This command enables / disables channel n (n = 0 .. 7, or n = 8, ..., 15) of the selected octet from the plot.
+/-	In case of multi-board systems, this command plots the next/previous board respectively.
q	This command quits the software.
Space	This command displays the online help.

Tab. 3.3: Software on-line commands.

Inside the Gnuplot window, there are active bindkeys and functions associated to the mouse:

Key	Function
a	x and y-axis auto-scale.
r	Enable / Disable ruler.
g	Enable / Disable grid.
y	Set the scale y at full scale, while x-scale remains unchanged
p	Return to previous zoom.

Tab. 3.4: Gnuplot on-line commands.

Zoom Area: right click on one corner of the area, release the button, left click on the opposite corner.

Click with the right button on the window bar to open a menu that allows to make the print, copy the screen-shot to the clipboard, change colours, etc.

725 and 730 Config File Sintax

The configuration file is located in the main software folder and it is called ”DAW_Config.txt”.

The setting modes can be [COMMON] (all boards-related), ”[BOARD] #” (single board-related) or ”[CHANNEL] #” (single channel-related).

If a setting is CHANNEL-related, it can also be BOARD-related or COMMON (i.e. the setting refers to all the channels in all the boards of the system). However not all options that are COMMON can also be BOARD- or CHANNEL-related. The ”[BOARD] #” or ”[CHANNEL] #” directives have no effect on such settings. The ”[BOARD] #” and ”[CHANNEL] #” modes are alternative to [COMMON] but do not exclude each other. This means that one can issue a command to a specific channel of a specific board, to all channels of a specific board or to a specific channel of all boards.

When the ”[BOARD] #” mode is set, the following settings apply to all channels (even if a specific channel was previously selected). The board index follows the board initialization order using the OPEN command (see below). The lines between the commands @OFF and @ON will be skipped. This can be used to exclude parts of the config file.

Board Settings

OPEN `LinkType LinkNumber NodeNumber BaseAddress`

Specifies the path of the physical channel to open communication with the digitizer:

`LinkType`	Identifies the type of communication channel, choosing between USB and PCI. USB corresponds to both the direct connection from PC to digitizer (Desktop models or NIM), and the connection through V1718 and VME bus (VME models). PCI corresponds to both the direct connection from PC A2818 (PCI controller) or A3818 (PCIe controller) to the digitizer through optical fibre (all models), and connection through V2718 and VME bus (VME models).
`LinkNumber`	The number of the connection. It is typically 0 (only one digitizer connection to the PC); in case of many digitizers connected it is necessary to specify which has to be accessed. Remember that the DPP-DAW Control Software demo can handle only one digitizer at a time. LinkNumber identifies which USB or A2818/A3818 is in use. Be aware that it is not known in advance which LinkNumber corresponds to which USB port or PCI slot.
`NodeNumber`	This parameter must be specified only when connected via optical link (PCI) and indicates the node in the daisy chain. It is typically 0 (only one digitizer in the optical chain), it may be different if more than one digitizer (or V2718) is connected in a daisy chain.
`BaseAddress`	Indicates the Base Address (32-bit hexadecimal number) to access the digitizer via the VME bus. This number should be 0 for direct connections from a PC to a digitizer.

Common Settings

START_ACQ `option`

This command specifies the source of the start acquisition and it is relevant only when `SYNC_ENABLE` is set to `NO` (see next parameter). The possible `options` are:

`SW`: a software command starts the acquisition;

`S_IN`: a level on the S_IN/GPI front panel connector drives the acquisition;

`FIRST_TRG`: first trigger on TRG-IN front panel connector starts the acquisition;

`LVDS`: signal on LVDS connectors starts the acquisition;

SYNC_ENABLE `option`

Sets all the registers required for the synchronization procedure described in Chapter **Board Synchronization**. Board delays might need a further tuning according to the experimental setup used.

Note: The start acquisition is SW-controlled for the master board and propagated through LVDS connectors to the slaves. Command `START_ACQ` is not applied.

The possible `options` are:

`YES` to enable it;

`NO` to disable it.

STAT_REFRESH `value`

Statistics Refresh period (msec), including event plotting if enabled.

PERIODIC_PLOT `option`

If enabled, the waveform will be plotted periodically, the period being set by the `STAT_REFRESH` variable. On slower PCs, disabling this feature might improve the demo software performances. Single events can be plotted by pressing the ”p” key during acquisition. The possible `options` are:

`YES` to enable it;

`NO` to disable it.

GNUPLOT_PATH `path`

Path of the gnuplot executable file, which is the working directory by default. In case of custom gnuplot installation it is recommended to verify the correct path.

OUTFILE_TYPE `option`

In case of `OUTFILE_RAW`, it is possible to dump a file of all the acquired waveform in binary format, where the format is defined in Sec. **Event Structure**. In case of `OUTFILE_WAVE`, the program saves a .txt file with the last acquired waveform for each enabled channel. The possible `options` are:

`OUTFILE_RAW YES/NO` to enable/disable the board dump (.bin);

`OUTFILE_WAVE YES/NO` to enable/disable the dump of the last waveform of each active channel (.txt).

OUTFILE_PATH `path`

This command sets the path for the output file write.
The default output directory in Windows is <UserDir>\DAW_Demo\DAW_output (created by the program).
The default output directory in Linux is ”UserDir”\DAW_output (created by the program)
The default file name is run0, then *b*, *c*, and *seg* identify the board, channel and output segment respectively (segmented according to OUTFILE_MAXSIZE):

`"file_name"_raw_b#_seg#.bin` for the raw

`"file_name"_wave_b#_c#.txt` for the wave

OUTFILE_MAXSIZE `value`

This command defines the maximum size of a file. After this size has been reached, a new file is created with a _seg(#+1) suffix.

> `value` is expressed in MBytes.

CONT_SWTRIGGER `option`

This command enables or disables the continuous software trigger. The possible `options` are:

> `YES` to enable it;
>
> `NO` to disable it.

ENABLE_GRAPH `value`

`value` corresponds to the index of the default channel enabled for plotting. The plotted channel can be chosen by using the '1'-'8' keys, which correspond to ch. 0-7 and ch. 8-15. The groups ch.0-7 and ch.8-15 can be toggled by pressing the 'g' key. In case of multiple boards, it is possible to select the plotted board by pressing the '+'/'-' keys.

EXTERNAL_TRIGGER `option`

This command manages how an external trigger on the TRG IN front panel connector is used. The possible `options` are:

> `ACQUISITION_ONLY`: the arrival of a trigger on the front panel causes the acquisition of one event in all the channels of the board.
>
> `ACQUISITION_AND_TRGOUT`: the same as ACQUISITION_ONLY. In addition, the external trigger is also propagated to the TRG-OUT (or GPO for the Desktop and NIM versions) front panel connector.
>
> `DISABLED`: the external trigger is ignored.

FPIO_LEVEL `option`

Indicates the electrical level for the front panel LEMO I/Os (TRG IN, TRG OUT and S IN for VME; TRG IN, GPI and GPO for Desktop and NIM). The possible `options` are:

> `TTL` if the desired I/O level is TTL,
>
> `NIM` if the desired I/O level is NIM.

RECORD_LENGTH `value`

Indicates the minimum number of samples (where 1 sample corresponds to 2 ns for 730 and 4 ns for 725 series) to be acquired for each trigger in one acquisition window.

> `value` is an integer value ranging from 1 to 2097151. The number of record length samples corresponds to `value` · 10.

MAX_TAIL `value`

Defines the maximum number of over-threshold samples collected after the minimum record length end. One sample corresponds to 2 ns for 730 and 4 ns for 725 series. After the MAX_TAIL time, the baseline calculation starts again from scratch.

`value` is an integer value ranging from 0 to 2097151. The number of samples corresponds to `value` · 4.

GAIN_FACTOR `value`

Sets the input dynamic range of the board. The possible `values` are:

0 = 2 V_{pp};

1 = 0.5 V_{pp}.

PRE_TRIGGER `value`

Defines the number of samples to be acquired in the acquisition window before the trigger.

`value` is an integer value ranging from 0 to 511. The number of pre trigger samples corresponds to `value` · 4.

N_LFW `value`

Defines the number of samples to be acquired when the pulse exits the over-threshold condition.

`value` is an integer value ranging from 0 to 511. The number of samples corresponds to `value` · 4.

BLINE_DEFMODE `option`

This command enables or disables the use of a fixed baseline value. The possible `options` are:

`YES` the algorithm uses the default value written in BLINE_DEFVALUE `value`;

`NO` the algorithm automatically evaluates the baseline.

BLINE_DEFVALUE `value`

Sets the fixed value of the baseline in case of `BLINE_DEFMODE=YES`.

`value` is an integer value ranging from 0 to 16383.

PULSE_POLARITY `value`

Sets the trigger polarity. The possible `values` are:

`POSITIVE`: trigger condition met for over-threshold samples;

`NEGATIVE`: trigger condition met for under-threshold samples.

TEST_PULSE `option`

When enabled, the input channels are replaced by an exponentially decaying or sawtooth pulse, internally generated by the FPGA. The possible `options` are:

`YES` to enable it;

`NO` to disable it.

TP_TYPE `option`

Sets the type of the internal test pulse when enabled. The possible `options` are:

`0` = exponential decay;

`1` = sawtooth;

SELF_TRIGGER `option`

This command enables or disables the channel self-trigger. When disabled, it is enabled the use of software trigger or global trigger. The possible `options` are:

`YES` self-trigger enabled;

`NO` self-trigger disabled.

TRG_THRESHOLD `value`

Sets the trigger threshold relative to the baseline value.

`value` is an integer value ranging from 0 to 16383.

WRITE_REGISTER `address data mask`

This command allows to write register values on the board.

`address` is the hexadecimal address offset of the register (16 bit value);

`data` is the data to be written into the register (16 or 32 bit value);

`mask` is the bit masking for the data writing (16 or 32 bit value).

EXAMPLES:

1. Set only bit [12] of register 1080 to 1, leaving the other bits to their previous value:
   WRITE_REGISTER 1080 1000 1000
2. Set bit [12] = 1 and bit [13] = 0 of register 1080, leaving the other bits to their previous value:
   WRITE_REGISTER 1080 1000 3000
3. Set register 1080 to the value of 0x45:
   WRITE_REGISTER 1080 45 FFFFFFFF

Note: Writes are executed at the end of the digitizer programming, therefore they can overwrite common or individual settings.

Individual Settings

Individual settings are written under the [CHANNEL n] command, where n is the channel index. If they are written in the common settings area, then they are applied to all channels at the same time.

ENABLE_INPUT `option`

This command enables or disables the corresponding channel for the acquisition. Possible `options` are:

`YES` to enable it;

`NO` to disable it.

DC_OFFSET `value`

The DC_OFFSET allows to shift the input dynamics (-FSR / 2 to +FSR / 2, where FSR is the full scale range, 2 V_{pp} or 0.5 V_{pp} for 730 and 725 series) towards negative or positive values.

`value` ranges from -50 to 50, where -50 corresponds to a signal dynamics from -FSR to 0 (completely negative signal), and 50 corresponds to a signal dynamics from 0 to FSR (completely positive signal). The default value is 0, corresponding to the signal dynamics of -FSR / 2 to +FSR / 2 (bipolar signal).

Note: the dynamic range of the DAC does not correspond exactly to the ADC range, so there is not an exact correspondence between the 0-level of DC offset and the baseline at 8192 ADC channels.

4 Board Synchronization

This chapter details the required steps in order to synchronize several boards are reported. Although the guide refers to the DAW package for V1725/30 boards, the described procedure also fits other board models: in what follows you should refer to the DAW package for what concerns the code and to the V1725/30 manuals for the registers and their description. The pictures refer to two synchronized boards, but the procedure applies to any number of boards.

1. **CLOCK**: all the boards should work with the same clock, and all the clock of all the boards should ideally be in phase. In order to do that, one board (the clock master, CM) distributes its clock to all the others (clock slaves, CSs) through the CLK IN / CLK OUT connectors in the upper part of the front panel (see Fig. **4.1**). The connections should be made through the A317 connectors provided by CAEN, as shown in the picture below:

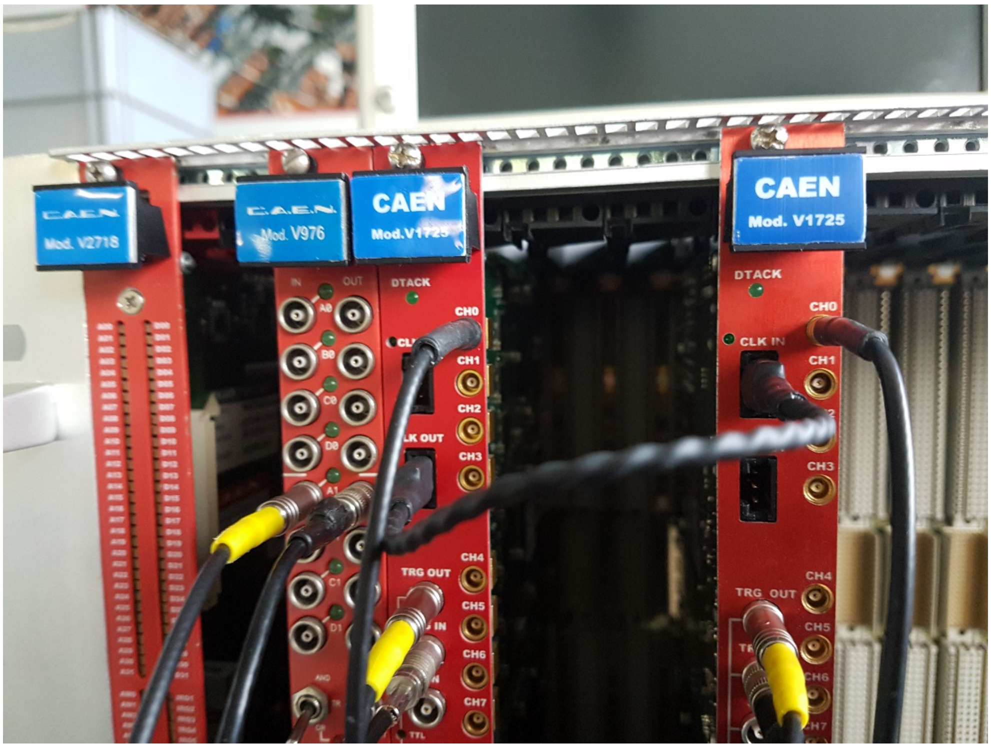

Fig. 4.1: Digitizer clock daisy-chain.

Please remember to set the clock switch on the board PCB (located in the space between the two daughter-boards) to **INT** for the CM only, while it should be set to **EXT** for the CSs.

An update of the internal PLL must also be made. In the DAW packages the required PLL configuration files are provided: the user should use the 50 MHz internal oscillator reference configuration (PLLClockMaster.rbf) for the CM and the 62.5 MHz reference configuration (PLLClockSlave.rbf, the 62.5 MHz clock is received from the previous board in the daisy chain) for the CSs.

In order to upgrade the board PLL the user have to do the following for each board

(a) Open the CAENUpgrader software
(b) Select Upgrade PLL into the "Board Upgrade" tab
(c) Choose the relevant board from the menu
(d) Select the PLL file to upload

(e) Select the connection type

(f) Press ”Upgrade”

Once this operation has been done for all boards, the user must power-cycle the crate.

The clocks can be checked to be synchronous and in phase by setting the register 0x811c to 0x90000 and observing the clocks on an oscilloscope from the TRG OUT connector. As the phase setting might be slightly dependent from the board and the running conditions, in case of relevant phase differences between two or more clocks please refer to the CAEN Technical Support.

2. **SYNCHRONIZATION PROCEDURE**: The synchronization procedure described in this Chapter assumes a fanned-out trigger in input to the TRG IN connector of each board via equal-length LEMO cables.

   Furthermore, the TRG OUT connector must not be used for triggering purposes, as it is used to stop triggering the boards in case one of them is in a BUSY state (i.e. it will soon reach a situation in which received triggers cannot be processed).

   The relevant registers to be configured for this synchronization procedure can be seen directly in the ProgramDigitizers() function included in the demo: if the `SYNC_ENABLE` demo option is set to `YES`, the demo will configure the board according to the described synchronization procedure. Here we only highlight the most relevant points of the procedure:

   (a) The first board of the daisy chain is configured to start the run via software (in the demo, this corresponds to pushing the ‘s’ key), while the other boards are configured to start via LVDS signals;

   (b) The RUN IN signal is propagated from one board to the other in daisy-chain through the LVDS connectors in the lower part of the board front panel, as shown in Fig. **4.2**. In particular, the LVDS pair 7 of each board is configured as a RUN IN output and should be connected to the LVDS pair 3 of the following board in the daisy chain (configured as a RUN IN input), see Fig. **4.2**;

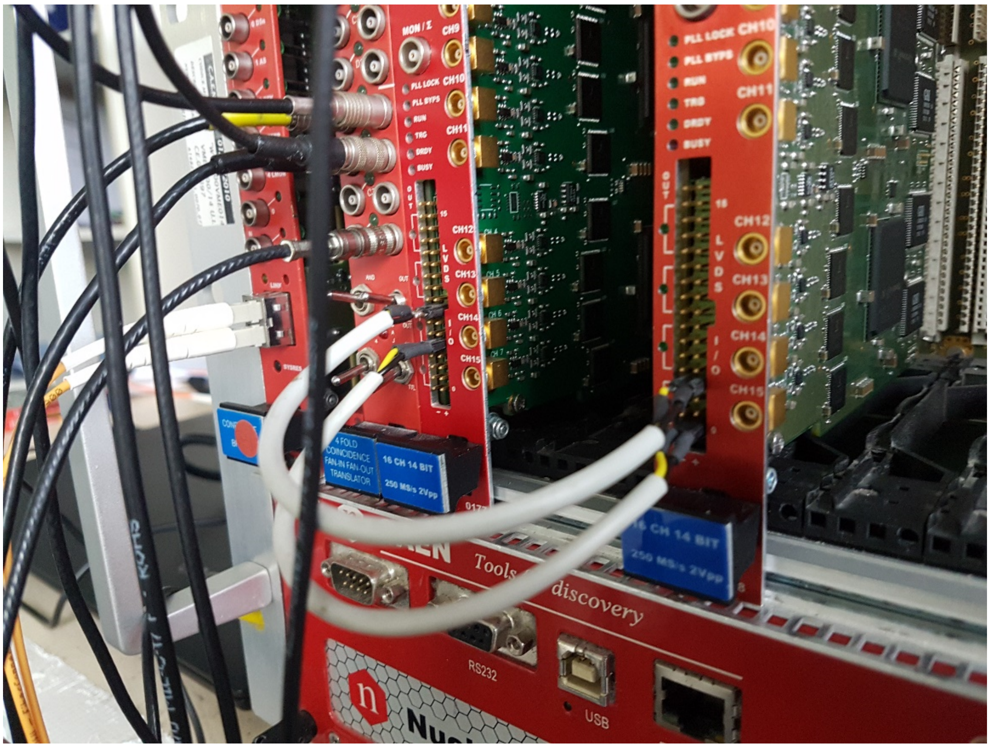

Fig. 4.2: RUN IN and BUSY daisy-chains through the LVDS connectors

   (c) The BUSY signal is propagated from one board to the other in daisy-chain through the LVDS connectors in the lower part of the board front panel, as shown in Fig. **4.2**. In particular, the LVDS pair 4 of each board is configured as a BUSY output and should be connected to the LVDS pair 0 of the following board in the daisy chain (configured as a BUSY input), see Fig. **4.2**. Note that each board adds his own BUSY signal to the daisy-chained BUSY, so that at the end of the daisy chain one has the OR of all the BUSY signals from the boards. This latter signal, that is fanned-out from the TRG OUT connector of the last board in the daisy chain (see Fig. **4.3**) must be used to veto triggers to the boards;

Fig. 4.3: The signal from the TRG OUT connector must be used to veto the global trigger

(d) The timestamp of each board is conveniently delayed (through the register 0x8170), in order to eliminate timestamp shifts given by the daisy-chain delay. NB: This does not eliminate a possible shift of +/- 1 LSB given by the fact that triggers are non-synchronous.

5 Technical Support

CAEN makes available the technical support of its specialists for requests concerning the software and hardware. Use the support form available at the following link:

https://www.caen.it/support-services/support-form

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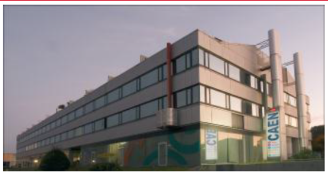

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