

**28 June 2021**

**RAMpiler+ ®**

**06/07nm SP Compiler**

***User Manual***

***Revision 1.0***

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# REVISION HISTORY

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Revision | Date | Description of Changes | Compiler | Author |
| 1.0 | 06/28/2021 | Initial document |  | Viet |

# Introduction

This document explains each option available in the memory compiler. The next sections explain the options and the ranges for Single Port. The user also has the option of selecting two redundant quad-rows, two redundant Columns (IO’s) or both for the Single Port. The compiler is capable of generating the fuse box logic as well if the user wishes to use the redundancy feature. The compiler comes complete with tool tips for ease of use and is capable of providing suggestions for the most optimal configuration based on input criteria specified by the user.

# Compiler Usage

## SRAM Options

### Basic options

DTI supports these following basic options. Customer can see more details in part 2.2

Column mux option

Output drive strength

Write enable

register output (with and without scanning mode)

Asynchronous write through

Clock edge

Test input

XOR

Column redundancy

Row redundancy

Output enable

Decap

Deep Nwell

VT options

Memory cell options

Synchronous write

### Additional options

DTI supports some additional options as well. Additional/extra license is required for them.

Low power

Low leakage

Power gating

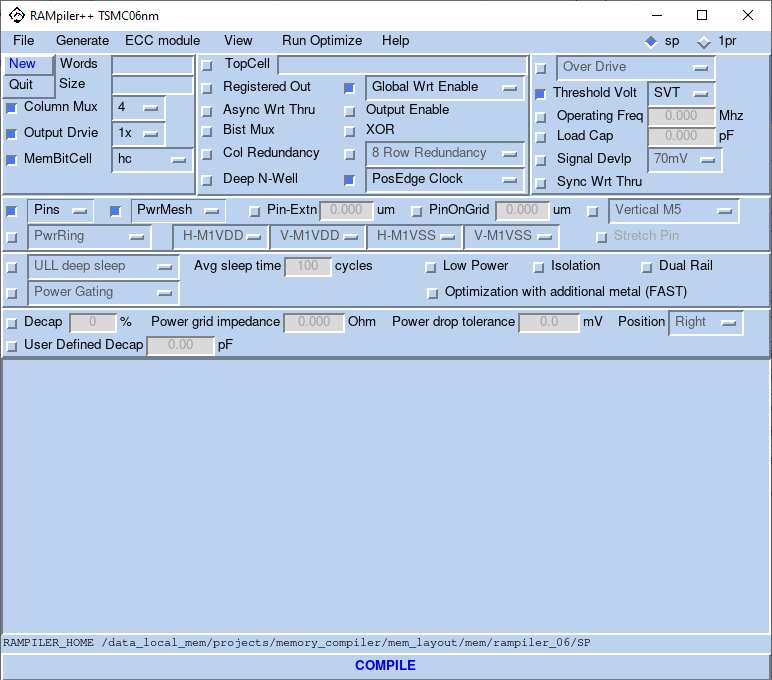
Dual power

Isolation

## Main GUI Pull Down Menus

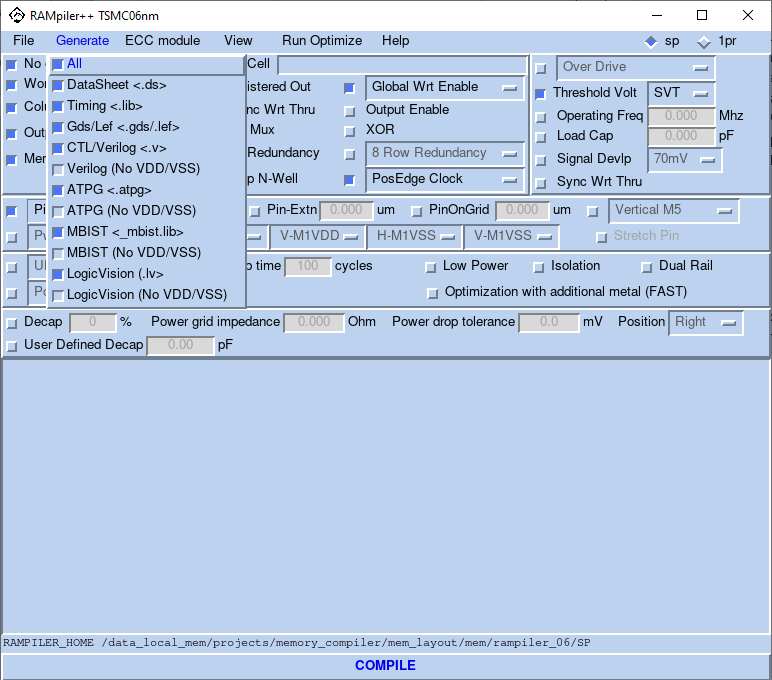
### File

The **“File”** option shown below is a pull down menu. The user **must** select **“New”** to generate a new instance of a memory. After generating the required instances, the user can select **“Quit”** to quit the tool.



### Generate

The **“Generate”** option allows the user to select the different views that can be generated. By default the compiler generates all the views. If the user wants to generate only timing views, he/she can deselect the **“ALL”** button. Timing views are always generated. If the aim is to find out the optimum configuration, the user can generate the timing views only. Based on the access time and the area from the datasheet, the user can decide to generate other views. The different views available in the compiler are **Netlist, Gds, Lef, Verilog, ATPG, MBIST, Logic Vision** and **Timing**. The user can generate all the views for a memory instance in less than a minute. Depending on the requirements, different views are added to the compiler from time to time. The compiler also generates the **“Antenna Lef”**.



## GUI Options

The number of words (Depth) determines the number of rows and can be specified using **“No of Words”** option.

Number of physical rows = No. of words/Column Mux.

**Note:** Column Mux is also a number specified by the user and will be discussed later in this document.

|  |  |
| --- | --- |
| Compiler Type | Maximum Physical Rows |
| SinglePort | 256 |

|  |  |
| --- | --- |
| Compiler Type | Minimum Physical Rows |
| SinglePort | 1 |

# RAMpiler+ Pin Definition and

Table . RAMpiler Single Port Pin Definition

|  |  |
| --- | --- |
| Port Name | Function |
| A[0:M-1]\* | Address Bus (has address of the Access location in Memory) |
| T\_A[0:M-1] | Bist Address |
| DI[0:N-1] | Data In Bus |
| T\_DI[0:N-1] | Bist Data In Bus |
| DO[0:N-1]\*\* | Data Out Bus |
| CLK | Clock |
| GWE\_N | Global Read/Write Enable (low for write) |
| T\_GWE\_N | Bist Global Read/Write Enable (low for write) |
| BWE\_N[0:N-1] / BYWE\_N[0:N-1] | Bit Write Enable (low for write)  Byte Write Enable (low for write) |
| T\_BWE\_N[0:N-1] /  T\_BYWE\_N[0:N-1] | Bist Bit Write Enable (low for write)  Bist Byte Write Enable (low for write) |
| CE\_N | RAM select (active low) |
| T\_CE\_N | Bist RAM select (active low) |
| OE\_N | Output Enable (low for output) |
| T\_OE\_N | Bist Output Enable (low for output) |
| T\_BE\_N | Bist enable(active low) |
| T\_AWT\_N | Asynchronous write through(active low) |
| T\_RWM | Read Write Margin |
| XOR\_OUT | Xor output |
| SE | Scan enable (active high) |
| SI | Scan input |
| SO | Scan output |
| \* M = log2(words) \*\*\*T\_BE\_N is the select signal for built in self-test.\*\* N = Bits per word | |

# RAMpiler+ Naming Convention

dti\_sp(pp)\_(lp)\_(ll/lli)(pg/pgr)(dr)\_tm06(ff)(od)(hvt/lvt/ulvt)\_(nw)x(ws)\_ )(ep/op/sec/secde\*)\_(i)(t)(aw)(1/2/4/8/16/32)(bw/byw/ww)(r)(1/3/9)x(oe)(r)(c) \_(shd/hd/shc/hc)\_(isol)

Table . Naming Convention for Top Level

|  |  |  |
| --- | --- | --- |
| Field Value | Description |  |
| dti | Dolphin Technology |  |
| sp | Single Port SRAM Block without redundancy | Default |
| spp | SinglePort Plus [with Column Redundancy] |  |
| sppp | Single Port Plus Plus [with Row Redundancy] |  |
| shd/hd/shc/hc | Bit cell type |  |
| ll | Low Leak- deep sleep |  |
| lli | Low Leak- light sleep | Optional |
| dr | Dual Power Rail | Optional |
| pg | Power gating | Optional |
| pgr | Power gating with data retention | Optional |
| Tm06/07 | Foundry = TSMC Technology = 06/07nm | Default |
| ffp/ffc | Process |  |
| od | Over Drive |  |
| hvt | Higher Threshold Voltage logic device | Optional |
| lvt | Low Threshold Voltage logic device | Optional |
| ulvt | Ultra low Threshold Voltage logic device | Optional |
| nw | Number of Words |  |
| ws | Word Size |  |
| secded | Single Error Correct Double Error Detect | Optional |
| sec | Single Error Correct | Optional |
| op | Odd Parity | Optional |
| ep | Even Parity | Optional |
| \* | Number of parity bits | Optional |
| i | Clock = Negative Edge. If not present, Clock = Positive Edge | Optional |
| t | BistMux is selected and Test Pins are generated. | Optional |
| x | XOR the outputs of the bist mux | Optional |
| aw | Asynchronous Write through is enabled. | Optional |
| 4 | Column Mux select Option 4 | Default for SP |
| 8 | Column Mux select Option 8 |  |
| 16 | Column Mux select Option 16 |  |
| 32 | Column Mux select Option 32 |  |
| bw | Bit Write |  |
| byw | Byte Write |  |
| ww | Global Write | Default |
| r | Registered Output | Optional |
| 1x | Output Driver Strength 1x | Default |
| 3x | Output Driver Strength 3x |  |
| 9x | Output Driver Strength 9x |  |
| oe | Output enable | Optional |
| r | Redundant Row(s) created | Optional |
| c | Redundant Column(s) created | Optional |
| pn | Power Ring Enabled | Optional |
| po | Power Ring Enabled with Overlap | Optional |
| isol | Isolation | Optional |

# READWRITE Timing Diagram Without Output Register

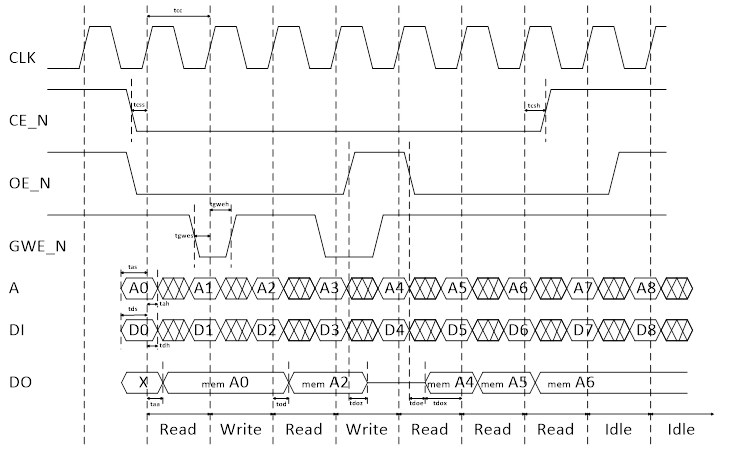


Figure : Read Write Timing Diagram without Registered Output

# Appendix A: Datasheet description

# Appendix B: Optimizing for AREA

# Appendix C: Optimizing for Timing