# CS311-Lab5

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## 1 Data

| TEST CASE | Hash of state | Number of instructions | Number of cycles |
|---|---|---|---|
| descending.out | 255541867 | 277 | 277 |
| evenorodd.out | -224294686 | 6 | 6 |
| fibonacci.out | -1518357572 | 78 | 78 |
| palindrome.out | 155317940 | 49 | 49 |
| prime.out | -1414219998 | 29 | 29 |

Table 1: Before Pipeline

| TEST CASE | Hash of state | OF stalls | Wrong branch instructions in pipeline | Number of cycles |
|---|---|---|---|---|
| descending.out | 255541867 | 126 | 220 | 658 |
| evenorodd.out | -224294686 | 10 | 4 | 19 |
| fibonacci.out | -1518357572 | 44 | 36 | 157 |
| palindrome.out | 155317940 | 51 | 18 | 124 |
| prime.out | -1414219998 | 19 | 28 | 79 |

Table 2: After Pipeline

## 2 Cache

Added cache with following parameters:

| TEST CASE | Hash of state | Control Hazards | Data Hazards | Number of cycles | IPC |
|---|---|---|---|---|---|
| descending.out | 255541867 | 88 | 143 | 11432 | 0.01469559132260322 |
| evenorodd.out | -224294686 | 0 | 3 | 248 | 0.020161290322580645 |
| fibonacci.out | -1518357572 | 16 | 0 | 3156 | 0.019328263624841573 |
| palindrome.out | 155317940 | 7 | 3 | 1982 | 0.020686175580221997 |
| prime.out | -1414219998 | 5 | 0 | 1174 | 0.013628620102214651 |

Table 3: Discrete event simulator

| Cache size | 16B | 128B | 512B | 1kB |
|---|---|---|---|---|
| Latency | 1 | 2 | 3 | 4 |
| Linesize | 4B | | | |
| Associativity | 2 | | | |
| Write Policy | Write Through | | | |

# 3 Vary L1i cache

| Program | IPC without cache | 16B | 128B | 512B | 1024B |
|---|---|---|---|---|---|
| Descending | 0.014695 | 0.0475 | 0.0523 | 0.0531 | 0.0512 |
| Fibonacci | 0.019328 | 0.0349 | 0.0566 | 0.0567 | 0.0565 |

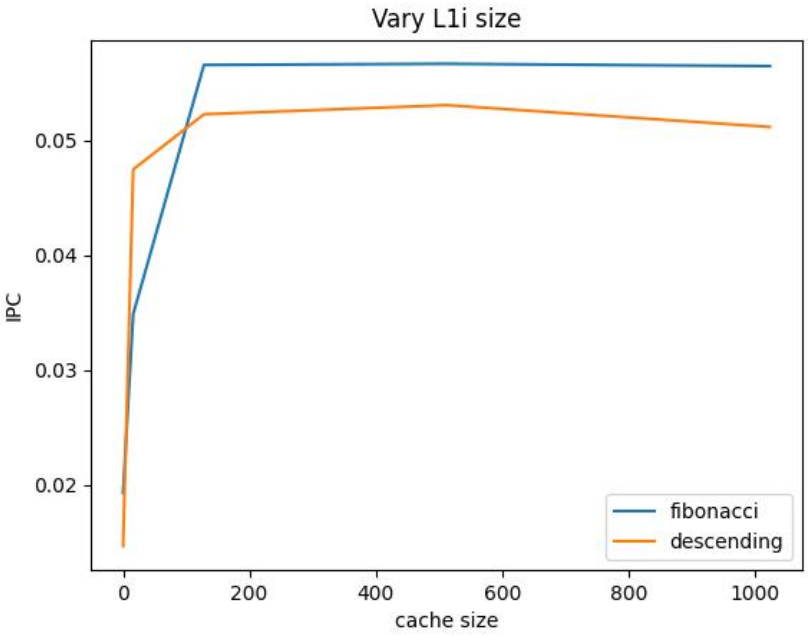


Figure 1: Vary L1i

# 4 Vary L1d cache

| Program | IPC without cache | 16B | 128B | 512B | 1024B |
|---|---|---|---|---|---|
| Descending | 0.014695 | 0.01345 | 0.0523 | 0.07013 | 0.07122 |
| Fibonacci | 0.019328 | 0.01725 | 0.0566 | 0.0631 | 0.0655 |

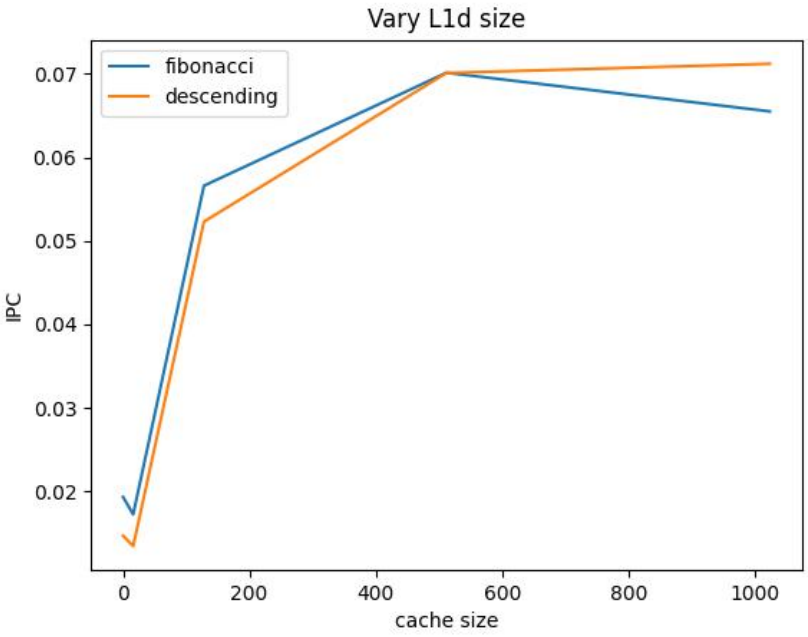


Figure 2: Vary L1d

## 5 Observations from data:

In graph 1 as size of L1i size increases the hit rate also increases, and then it plateaus because more cache does not benefit when instructions do not increase.

In graph 2 as size of L1i size increases the hit rate also increases, and then it plateaus because more cache does not benefit when memory access instructions do not increase.