CS 311, Assignment 6 - Report

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1 Abstract

In this assignment, we essentially had to add caches to the simulated memory system.

- Add one cache between the IF stage and the main memory. Let us call this the level 1 instruction cache or the `L1i-cache`.
- Add one cache between the MA stage and the main memory. Let us call this the level 1 data cache or the `L1d-cache`.

1.1 Configurations of Cache

Table 1 gives the Configurations of Cache.

1.2 Analyses to be Performed

1. First fix the size of the L1d-cache at 1kB. Vary the size of the L1i-cache from 4B to 1kB (remember to change latency accordingly), and study the performance (instructions per cycle). Plot your results for the different benchmarks.
2. Now fix the size of the L1i-cache at 1 kB. Vary the size of the L1d-cache from 4B to 1kB, and plot your results for the different benchmarks.
3. Correlate the nature of the benchmark to the observed plot.

Cache Size	8B	32B	128B	1kB
Latency	1 cycle	2 cycle	4 cycle	8 cycle
Line Size	4B			
Associativity	2			
Write Policy	Write Through			

Table 1: Configurations of Cache

Program	IPC	L1d = 1kB			L1d = L1i = 1KB	L1d = 1kB		
	Without Cache	L1i = 8B	L1i = 32B	L1i = 128B		L1i = 128B	L1i = 32B	L1i = 8B
Evenodd (6)	0.0242	0.0220	0.021	0.02	0.0173	0.017	0.017	0.017
Prime (92)	0.0244	0.0230	0.050	0.04	0.0314	0.031	0.031	0.031
Palindrome (49)	0.0247	0.0231	0.069	0.05	0.038	0.035	0.037	0.038
Fibonacci (78)	0.0249	0.0227	0.030	0.047	0.0353	0.035	0.036	0.036
Descending (277)	0.0248	0.0227	0.028	0.06	0.0455	0.046	0.047	0.043

Table 2: IPC Table

4. Create a toy-benchmark that shows significant performance improvement when the L1i-cache is increased from 32B to 128B. Assume favorable L1d-cache size.

5. Create a toy-benchmark that shows significant performance improvement when the L1d-cache is increased from 32B to 128B. Assume favorable L1i-cache size.

2 IPC Table for different values of Caches

The following table (Table 2) shows the IPC values for different values as mentioned above.

3 Graphs Interpretation and Comments

In Graph-1 (Figure 1) of IPC for various values of L1i cache where L1d Cache size is fixed to 1KB. We can clearly see that when L1i cache size increases, latency also increases, and so does the hit rate. There will be an optimum size of L1i cache when the IPC is at its maximum value.

In Graph-2 (Figure 2) of IPC for various values of L1d cache where L1i cache size is fixed to 1KB. We can clearly see that when L1d cache size increases, latency increases with increment in cache size and hit rate also increases. There will be an optimum size of L1d cache when the IPC is at its maximum value.

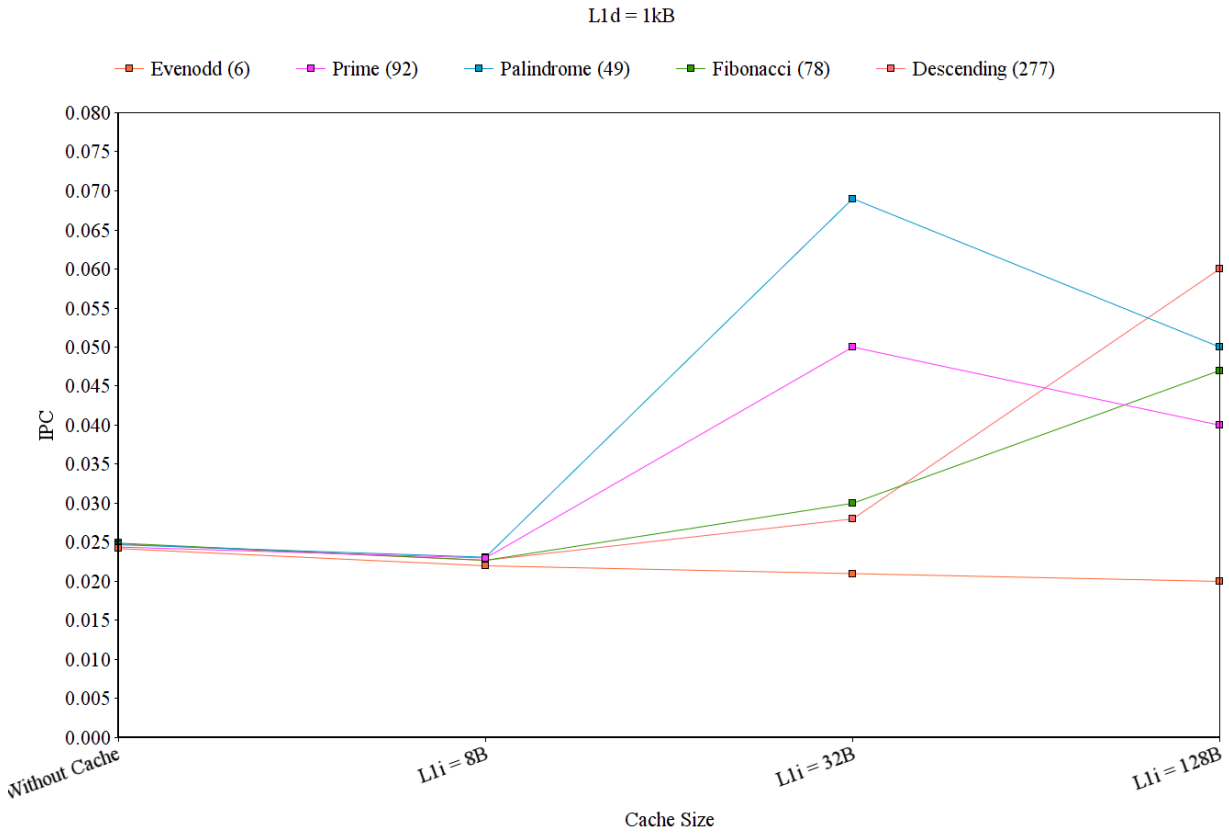

Figure 1: IPC Variation when L1d = 1kB

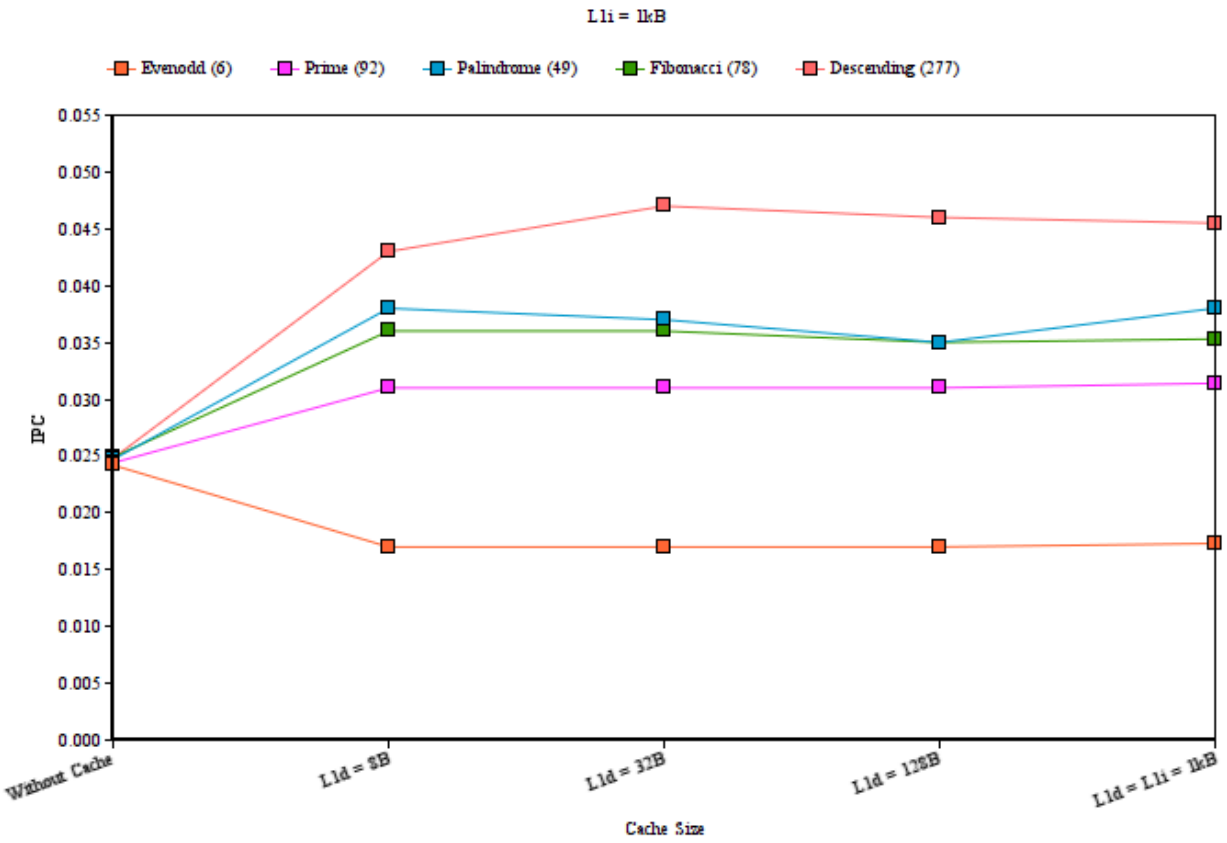

Figure 2: IPC Variation when L1i = 1kB