

CS 311, Assignment 5 - Report

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1 Abstract

In this assignment, we essentially had to upgrade the simulator to a discrete event simulator.

1.1 Discrete Event Simulator Model

An event is a tuple of the form: $\langle \text{event time, event type, requesting element, processing element, payload} \rangle$. The event queue is a list of events ordered by time. An event is said to “fire” when the current clock cycle is equal to the event time. When this happens, the `handleEvent()` function of the processing element is invoked. Handling of an event may in turn lead to more events being generated, for the same clock cycle, or for some future clock cycle.

1.2 Functionalities Implemented

- Modeling the latency of the main memory
This reflects in both instruction fetches and load/store operations.
- Modeling the latencies of different functional units
These units include ALU, multiplier, divider, etc.

2 Statistics Table

The following table (Table 1) touches upon the number of cycles taken by each benchmark program & the throughput in terms of instructions per cycle(IPC).

3 Interpretation and Comments

We observed that IPC of all the benchmark programs is between 0.024 and 0.025. The programs which have a lot of data hazards and control hazards and that take more no. of iterations have lot of cycles.

File Name	No.of Cycles	IPC
descending.asm	14960	0.024398396
evenorodd.asm	248	0.024193548
fibonacci.asm	3808	0.024684874
palindrome.asm	2252	0.024866786
prime.asm	1368	0.024853801

Table 1: Statistics Table