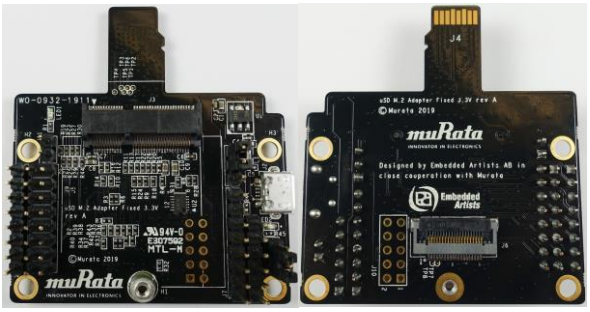
Murata uSD-M.2 Adapter Datasheet



Revision History

Revision	Date	Author	Change Description
1.0	04/15/2019	S. Kerr	Initial release

Table of Contents

List of Figures

List of Tables

Murata uSD-M.2 Adapter Kit

1.1 Introduction

Murata has partnered closely with Embedded Artists AB to provide a flexible Wi-Fi & Bluetooth solution for NXP Semiconductors' i.MX RT and i.MX 6 Evaluation Kits. Murata's uSD-M.2 Adapter Kit with Embedded Artists' Wi-Fi/BT M.2 Modules enable users with a simple plug-in solution. The Embedded Artists' Wi-Fi/BT M.2 Modules are based on Murata modules using Cypress Semiconductor's Wi-Fi/BT chipsets. Current Wi-Fi/BT EVB support include Murata Type 1DX (CYW4343W), Type 1MW (CYW43455), and Type 1LV (CYW43012). Note that all these M.2 EVB's use the WLAN-SDIO interface; this adapter **does not** support interfacing WLAN-PCIe-only modules such as Embedded Artists' Type 1CX M.2 Module.

The uSD-M.2 Adapter provides the following interfaces to host MCU/MPU:

- microSD (uSD) interface for WLAN-SDIO (SD is an option with microSD-SD Adapter).
- Arduino Headers (i.MX RT) or Flat/Flex Connector (i.MX 6) for Bluetooth UART, Bluetooth PCM and WLAN/Bluetooth control signals.
- Optional power, debug, and clocking signals connect through Arduino Header or Micro-AB USB Connector.

Murata's uSD-M.2 Adapter uses a type **2230-xx-E** M.2 Connector: this interface is essentially M.2 Key-E compliant with some enhancements to support additional debug signals and 3.3V VDDIO override[1] for Embedded Artists' Wi-Fi/BT M.2 Modules. Refer to Section 5 uSD-M.2 Adapter: Pinout Definition section for more details.

1.2 Acronyms

Table 1: Acronyms used in Adapter Kit Document

Acronym	Meaning
BT	Bluetooth
CTRL	Control
CTS	Clear to Send
DL	DualLite
EVB	Evaluation Board
EVK	Evaluation Kit
FFC	Flat Flexible Cable
GND	Ground
GPIO	General Purpose Input Output
JTAG	Joint Test Action Group
LED	Light-emitting Diode

[1] Note that 3.3V VDDIO override feature is currently only supported on Embedded Artists' 1DX and 1MW M.2 modules. The 1LV M.2 module is 1.8V VIO only (module/chipset limitation).

M.2	Formerly known as the Next Generation Form Factor (NGFF), is a specification for internally mounted computer expansion cards and associated connectors. The M.2 specification is defined by PCI-SIG (www.pcisig.com).
OOB IRQ	Out of Band Interrupt Request Line
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
Q	Quad
QP	QuadPlus
RTOS	Real-time Operating System
RTS	Request to Send
RX	Receive
SD	Secure Digital
SDIO	Secure Digital Input Output
SL	SoloLite
SX	SoloX
TX	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UL	UltraLite
USB	Universal Serial Bus
uSD	microSD
VBAT	Voltage of Battery
VDDIO	Voltage used by signals on memory bus
VIO	Input Offset Voltage
Wi-Fi	Wireless LAN: “Wi-Fi” is a registered trademark of Wi-Fi Alliance
WLAN	Wireless Local Area Network

1.3 References

1.3.1 Murata Wi-Fi/BT EVK for i.MX RT Hardware User Manual

Murata Wi-Fi/BT EVK for i.MX RT Hardware User Manual 1.0, “Murata Wi-Fi & BT EVK for i.MX RT Hardware User Manual 1.0.pdf”.

This manual describes the Murata Wi-Fi/BT EVK InterConnect Adapter hardware. All interface signals to the NXP i.MX RT (1050/1060/1064) EVK’s are described. Specifics on interfacing each i.MX RT EVK to Murata Wi-Fi/BT EVK are provided. This document is made available on Murata’s NXP i.MX Wireless landing page here.

1.3.2 Murata Wi-Fi/BT EVK for i.MX 6 Hardware User Manual

Murata Wi-Fi/BT EVK for i.MX 6 Hardware User Manual 3.0, “Murata Wi-Fi & BT EVK for i.MX 6 Hardware User Manual 3.0.pdf”.

This manual describes the Murata Wi-Fi/BT EVK InterConnect Adapter hardware. All interface signals to the NXP i.MX 6 (QP/Q/DL/SX/SL/UL/ULL/ULZ) EVK’s are described. Specifics on interfacing each i.MX 6 EVK to Murata Wi-Fi/BT EVK are provided. This document is made available on Murata’s NXP i.MX Wireless landing page here.

1.3.3 Murata Wi-Fi/BT Solution for i.MX Quick Start Guide (RTOS)

Murata Wi-Fi/BT Solution for i.MX Quick Start Guide (RTOS) 1.0, “Murata Wi-Fi & BT Solution for i.MX Quick Start Guide (RTOS) 1.0.pdf”.

This Quick Start Guide details steps to get Murata Wi-Fi/BT solution up and running quickly on i.MX RT EVK’s. This document is made available on Murata’s NXP i.MX Wireless landing page here.

1.3.4 Murata Wi-Fi/BT Solution for i.MX Quick Start Guide (Linux)

Murata Wi-Fi/BT Solution for i.MX Quick Start Guide (Linux) 6.0, “Murata Wi-Fi & BT Solution for i.MX Quick Start Guide (Linux) 6.0.pdf”.

This Quick Start Guide details steps to get Murata Wi-Fi/BT solution up and running quickly on i.MX6/7/8 platforms. This document is made available on Murata’s NXP i.MX Wireless landing page here.

1.3.5 Murata uSD-M.2 Adapter Schematic

Murata uSD-M.2 Adapter Schematic Rev A, “Murata uSD-M.2 Adapter Schematic Rev A.pdf”. This document is made available on Murata’s NXP i.MX Wireless landing page here.

1.3.6 Murata uSD-M.2 Adapter Layout

Murata uSD-M.2 Adapter Layout Rev A, “Murata uSD-M.2 Adapter Layout Rev A.pdf”. This document is made available on Murata’s NXP i.MX Wireless landing page here.

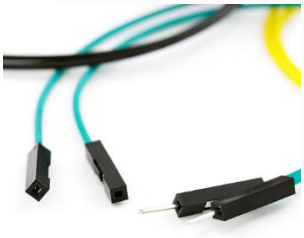
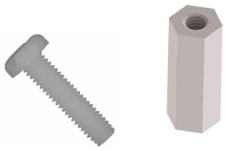
1.3.7 Murata uSD-M.2 Adapter Product Brief

Murata uSD-M.2 Adapter Product Brief 1.0, “Murata uSD-M.2 Adapter Product Brief 1.0.pdf”. This document is made available on Murata’s NXP i.MX Wireless landing page here.

2 Murata Kit Contents

The Murata uSD-M.2 Adapter Kit (Part No: **LBEE0ZZ1WE-TEMP**) contents are shown in Table 2.

Table 2: uSD-M.2 Adapter Kit Contents

Picture of Contents	Description of Contents
	uSD-M.2 Adapter (Revision A)
	M.2 screw for attaching Wi-Fi/Bluetooth M.2 Evaluation Board (EVB)
	75mm 20-pos, 0.5mm pitch flat/flex cable
	13 pieces 200mm long male-to-female jumper cables (compatible with Arduino header)
	4 x 19mm stand-offs in nylon and associated M3 screws
	microSD to SD Card Adapter

3 uSD-M.2 Adapter High-Level Description

Figure 1: uSD-M.2 Adapter Features (Top View), and Figure 2: uSD-M.2 Adapter Features (Bottom View) show the features on the uSD-M.2 Adapter; with text explanation in Table 3: uSD-M.2 Adapter Features.

The uSD-M.2 Adapter supports additional signals to WLAN-SDIO using either Arduino headers (J5, J8, and J9) or 20 pin FFC connector (J6). The 20 pin FFC connector is currently supported by NXP's i.MX 6 Platforms. The Arduino headers' layout matches NXP's i.MX RT 1050/1060/1064 EVK's. For more details on interconnecting with NXP's evaluation platforms, refer to Murata Wi-Fi/BT EVK for i.MX6 Hardware User Manual, Murata Wi-Fi/BT EVK for i.MX RT Hardware User Manual, Murata Wi-Fi/BT Solution for i.MX Quick Start Guide (RTOS), and Murata Wi-Fi/BT Solution for i.MX Quick Start Guide (Linux). Refer to Section 1.3 References for more details.

Table 3: uSD-M.2 Adapter Features

A	microSD connector provides Power (VBAT, GND) and WLAN-SDIO
B	SDIO bus test points (CLK, CMD, DAT0, DAT1, DAT2, DAT3)
C	Power LED Indicator (green): if not illuminated then no power applied to M.2 EVB
D	J11 = Optional BT Disable Jumper for WLAN-Only Mode (close this jumper to drive BT_REG_ON low and disable Bluetooth Core; thereby optimizing power consumption for WLAN-Only Mode)
E	J9 = BT UART TX/RX and WLAN/BT CTRL Arduino Header
F	J5 = Optional BT PCM and WLAN/BT Debug Signals
G	Threaded mount for M.2 screw: 30mm distance from M.2 connector
H	J7 = Optional Arduino Header Power Supply (can connect either 5V or 3.3V VBAT)
I	J8 = BT UART RTS/CTS Arduino Header
J	J12 = VDDIO Override: Short for 3.3V VDDIO; Open for 1.8V (default)
K	LED2 = 3.3V VDDIO Override Indicator (Blue)
L	J2 = Optional 5V USB Power Supply via Micro-AB USB Connector
M	J1 = Power Supply Selector Jumper must be installed to power Adapter (unless J5 Arduino Header Pins #15/16 are connected to external GND/3.3V VBAT). **Position 1-2:** 5V/3.3V VBAT supply from micro-USB (J2) or Arduino (J7); **Position 2-3:** VBAT supply (typical 3.1~3.3V) from microSD connector
N	Regulator to step down optional 5V VBAT from USB or Arduino header to 3.3V
O	M.2 Connector: type 2230-xx-E
P	microSD connector pins: provides Power and WLAN-SDIO
Q	WLAN JTAG header (header pins not populated)
R	20 pin FFC connector (BT UART, BT PCM, WLAN/BT Control signals)
S	Additional test points from 20pin flat/flex connector

Figure 1: uSD-M.2 Adapter Features (Top View)

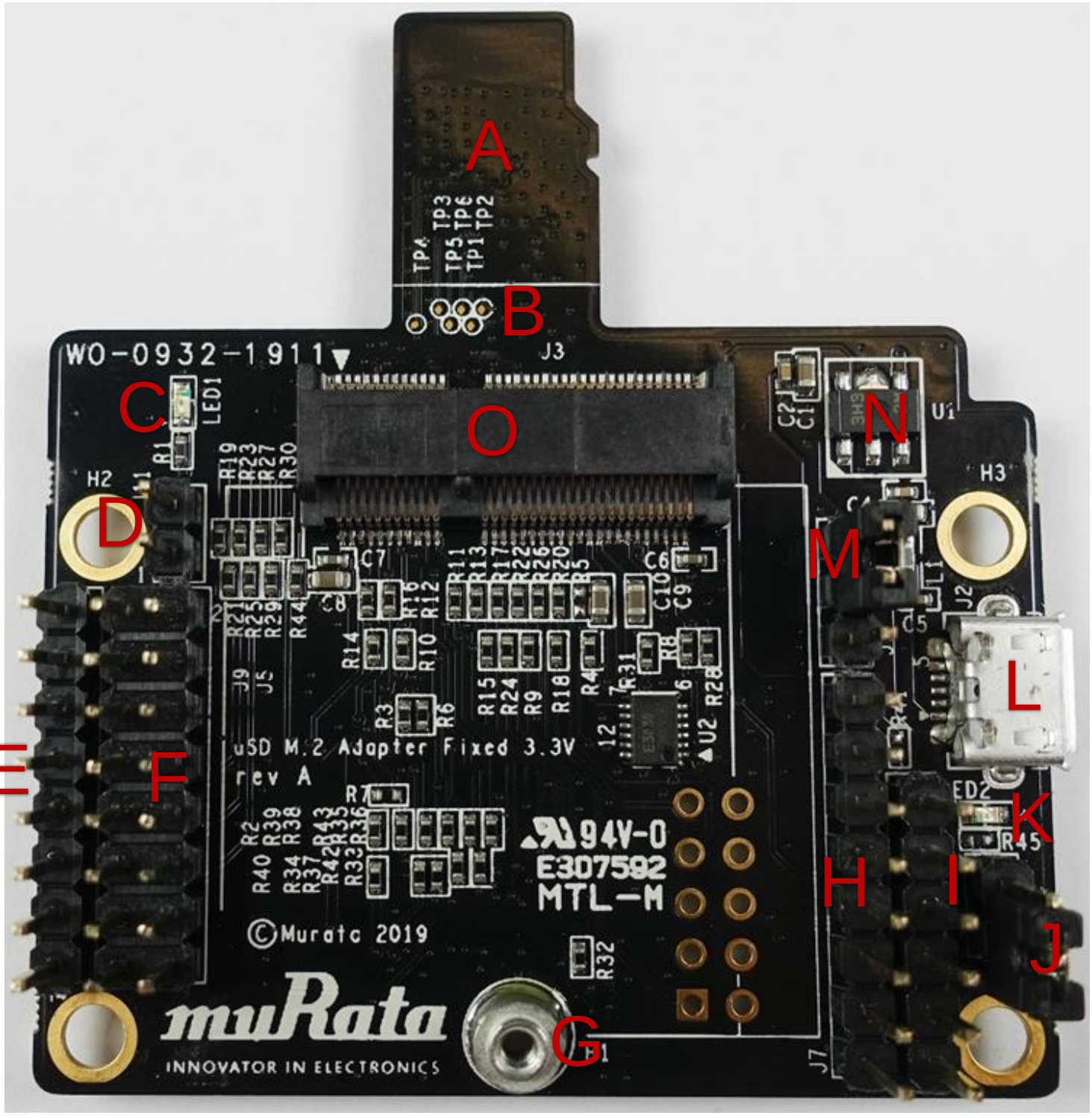
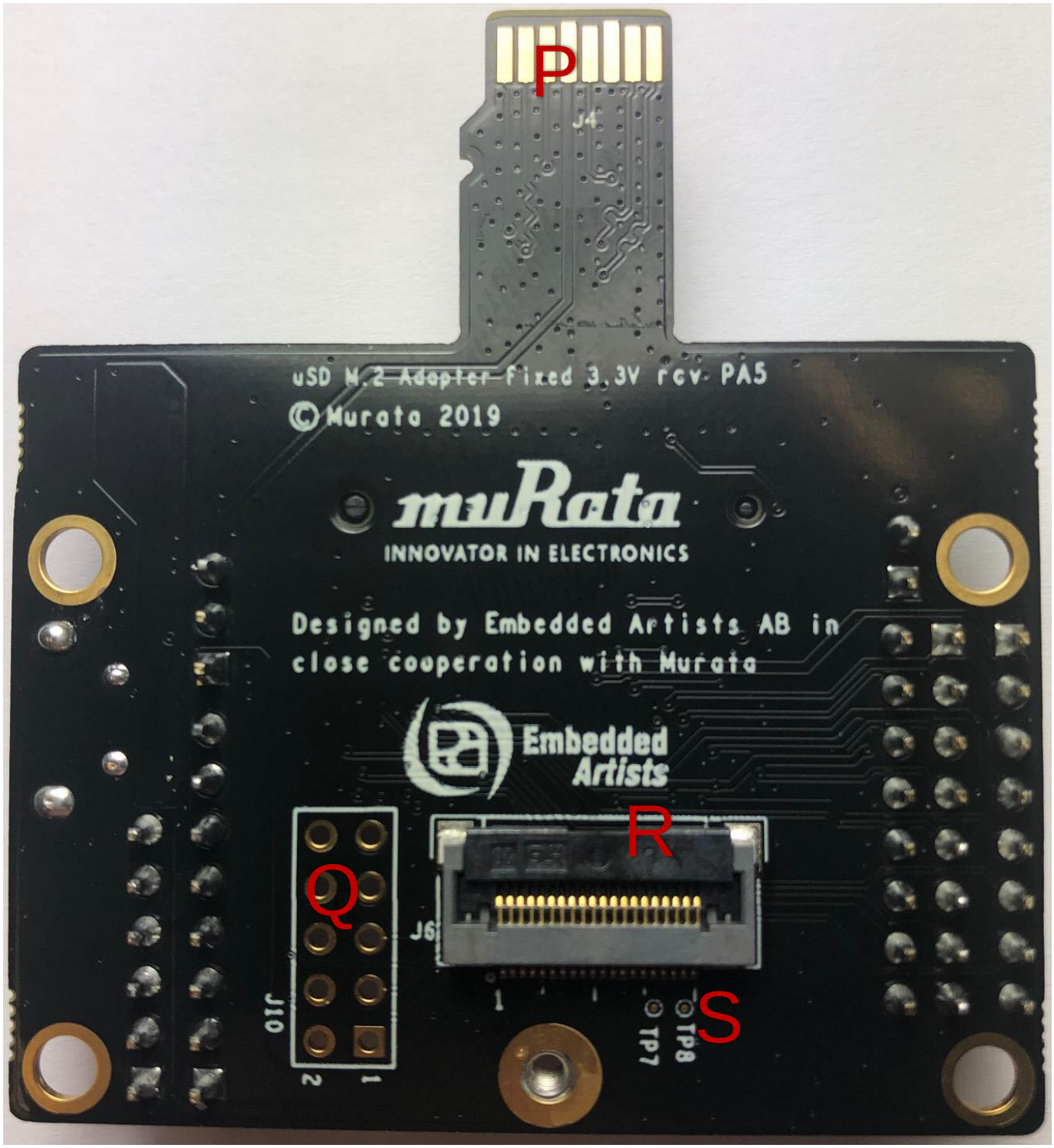


Figure 2: uSD-M.2 Adapter Features (Bottom View)



4 uSD-M.2 Adapter: Headers/Jumpers in Detail

For more details on the headers and jumpers, refer to Figure 3: uSD-M.2 Adapter - Left Headers/Jumpers, and Figure 4: uSD-M.2 Adapter - Right Headers/Jumpers. Pin #1 location on J5 and J9 Arduino Headers are marked clearly on Figure 3. Regarding even/odd pins on J5, pin #2 is to the immediate right of pin #1: also seen referring to Figure 6: uSD-M.2 Adapter Layout (top).

4.1 J11: Optional Jumper to Disable Bluetooth for WLAN-Only Operation

Referring to Figure 3: uSD-M.2 Adapter - Left Headers/Jumpers, J11 (see blue rectangle) is an optional jumper to disable Bluetooth core. This option is provided to minimize current consumption when running WLAN-only mode. When J11 pins are not closed (i.e. jumper not installed), BT_REG_ON is driven active high (VDDIO = 1.8V default or 3.3V when J12 is closed) when power is applied to the adapter. Referring to Figure 5: uSD-M.2 Adapter Schematic, R3 and C10 provide a simple resistor-capacitor power-on-reset signal for BT_REG_ON.

4.2 J9: Bluetooth UART TX/RX and WLAN/Bluetooth Control Arduino Header

Referring to Figure 3: uSD-M.2 Adapter - Left Headers/Jumpers, J9 (see orange rectangle) is a 8-pin Arduino Header that provides connectors to Bluetooth UART TX/RX and WLAN/Bluetooth control signals. All signals are 3.3V VIO. Referring to Figure 5: uSD-M.2 Adapter Schematic, current limiting resistors in lieu of level shifters (R9, R8, R7, R13, and R11) are included when interfacing 3.3V VIO signals to 1.8V VIO signals on Wi-Fi/BT M.2 Module. WL_REG_ON_3V3, BT_REG_ON_3V3, and BT_HOST_WAKE_3V3 interface directly to 3.3V VIO signals on Wi-Fi/BT M.2 Module.

Arduino Header signals connect with 200mm long male-to-female jumper cables (refer to Table 2: uSD-M.2 Adapter Kit Contents).

4.3 J5: Optional BT PCM and WLAN/BT Debug Signals

Referring to Figure 3: uSD-M.2 Adapter - Left Headers/Jumpers and Figure 5: uSD-M.2 Adapter Schematic, J5 (see green rectangle) is a 16-pin header that provides access to the following signals:

- Bluetooth PCM signals.
- WLAN and Bluetooth UART debug signals. This provides debug output from the WLAN/Bluetooth cores on the Cypress chipset.
- Bluetooth GPIO signals.
- Optional slow clock (LPO_IN_3V3) connection. If the user wants to bypass the onboard slow clock provided by U2 (i.e. remove R4), then this pin allows direct injection of the signal to M.2 Module.
- Optional 3.3V VBAT and GND power option: this is the only way to power the uSD-M.2 Adapter with J1 jumper removed.

Note that the signals listed in Figure 3 do not describe the less-used debug signals and optional Bluetooth GPIO's. Only specially-enabled WLAN firmware or Bluetooth patchfiles will enable these optional debug pins.

4.4 J1: Power Supply Selector

Referring to Figure 4: uSD-M.2 Adapter - Right Headers/Jumpers and Figure 5: uSD-M.2 Adapter Schematic, the J1 Jumper is used to select the power source for the adapter. This jumper must be installed to power Adapter (unless J5 Arduino Header Pins #15/16 are connected to external GND/3.3V VBAT). There are only two options/positions:

Position 1-2: 5V/3.3V VBAT supply from micro-USB (J2) or Arduino Header (J7);

Position 2-3: VBAT supply (typical 3.1~3.3V) from microSD connector (default).

NOTE: the kit is shipped with default position of 2-3; thereby configuring the uSD-M.2 Adapter to pull power from the microSD connector.

4.5 J12: VDDIO Override: Short for 3.3V VDDIO; Open for 1.8V (default)

Referring to Figure 4: uSD-M.2 Adapter - Right Headers/Jumpers and Figure 5: uSD-M.2 Adapter Schematic, Jumper J12 is installed to force VDDIO to 3.3V. Per M.2 interface, WLAN SDIO/BT UART/BT PCM interfaces operate at a default 1.8V. With J12 jumper Installed, VDDIO changes to 3.3V using pin #64 on M.2 interface to drive this override voltage setting. LED2 (blue) illuminates when 3.3V VDDIO setting is selected. **NOTE**: this will only work on select M.2 Modules such as Type 1DX and 1MW. Type 1LV M.2 Module **only supports 1.8V VIO**.

When J12 is not installed (default setting), VDDIO is set at 1.8V. This setting works for all M.2 Modules (currently 1DX, 1MW, and 1LV).

4.6 J7: Optional Arduino Header Power Supply (can connect either 5V or 3.3V VBAT)

Referring to Figure 4: uSD-M.2 Adapter - Right Headers/Jumpers and Figure 5: uSD-M.2 Adapter Schematic, J7 Arduino Header is used to provide optional power supply to microSD connector. Jumper J1 must be in 1-2 position (see Section 4.4) to disconnect microSD power and enable J7 header. Powering options include the following (J1 in position 1-2):

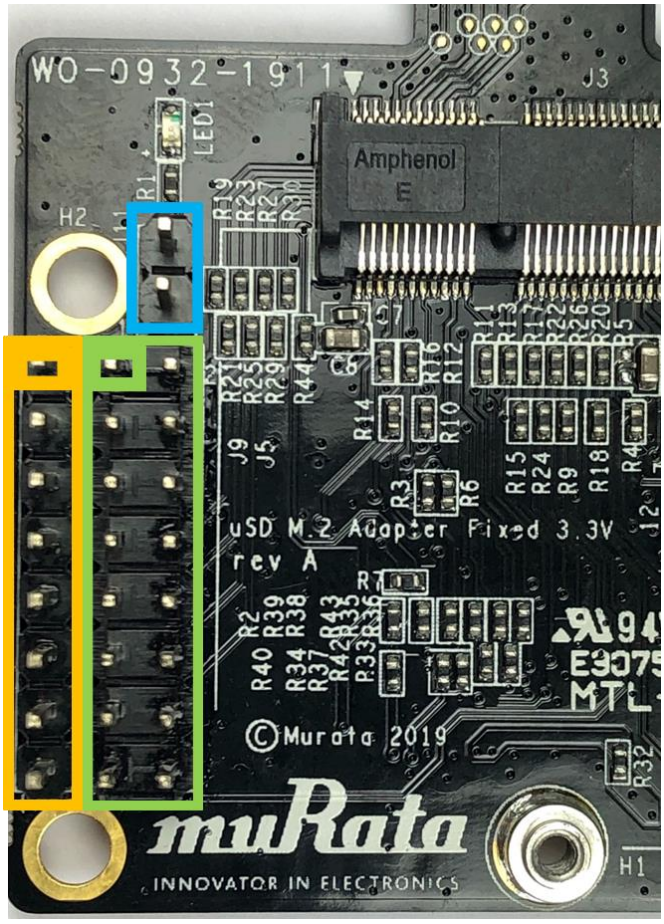
- Connect J7 Pins #2 and/or #3 to 3.3V VBAT; and Pin #6 and/or #7 to GND.
- Connect J7 Pins #5 to 5V VBAT; and Pin #6 and/or #7 to GND.

4.7 J8: BT UART RTS/CTS Arduino Header

Referring to Figure 4: uSD-M.2 Adapter - Right Headers/Jumpers and Figure 5: uSD-M.2 Adapter Schematic, J8 Arduino Header provides Bluetooth RTS and CTS connections. Default configuration for the Murata module (1DX/1MW/1LV) is to require flow control (i.e. not just TX/RX). As such, both RTS/CTS signals **need to be connected** to host MCU/MPU to provide correctly functioning BT UART connection using H4 UART transport.

NOTE: BT_UART_CTS_3V3 (UART CTS) is an input signal, and BT_UART_RTS_3V3 (UART RTS) is an output. For complete details on the pin/signal definitions, refer to Section 5 uSD-M.2 Adapter: Pinout Definition.

Figure 3: uSD-M.2 Adapter - Left Headers/Jumpers



J11 = Optional BT Disable; Jumper for WLAN-Only Mode

- ➔ Jumper Installed = BT_REG_ON is Low (BT Core disabled)
- ➔ Not Installed = BT_REG_ON is driven active high by Adapter on-board circuitry (default); or driven by Host if Arduino cable installed (J9; Pin #4).

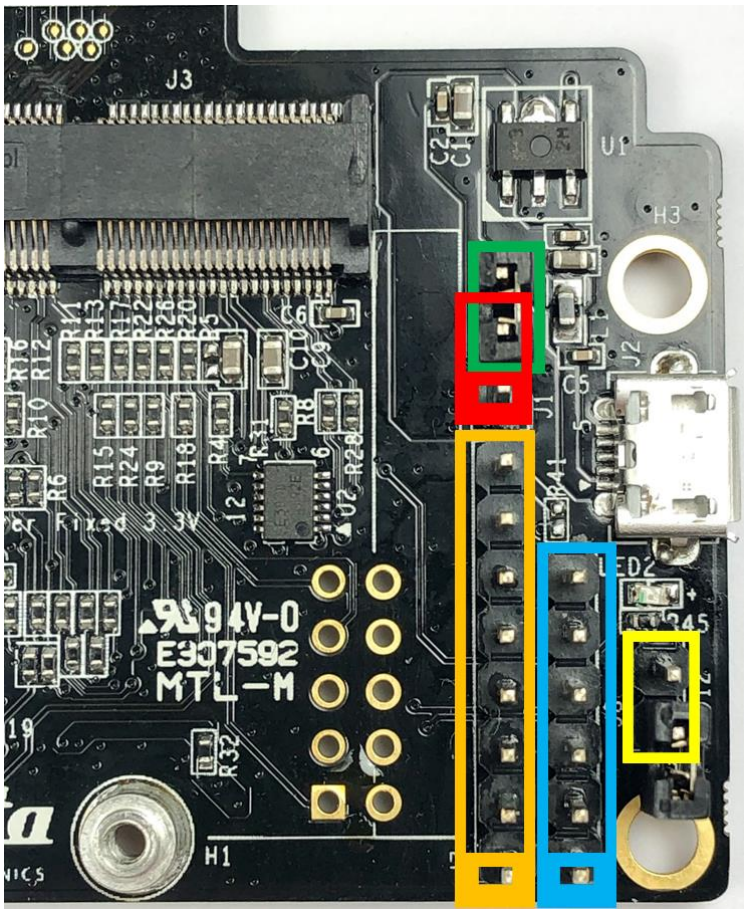
J9 = BT UART TX/RX and WLAN/BT CTRL Arduino Header

Pin#	J9 Signal		Pin#	J9 Signal
1	BT_UART_TXD_3V3		5	WL_HOST_WAKE_3V3
2	BT_UART_RXD_3V3		6	BT_HOST_WAKE_3V3
3	WL_REG_ON_3V3		7	WL_DEV_WAKE_3V3
4	BT_REG_ON_3V3		8	BT_DEV_WAKE_3V3

J5 = Optional BT PCM and WLAN/BT Debug Signals

Pin#	J5 Signal		Pin#	J5 Signal
1	BT_PCM_IN_3V3		14	LPO_IN_3V3
3	BT_PCM_OUT_3V3		15	GND
5	BT_PCM_SYNC_3V3		16	USD_3V3
7	BT_PCM_CLK_3V3			

Figure 4: uSD-M.2 Adapter - Right Headers/Jumpers



J1 = Power Supply Selector

Jumper must be installed to power Adapter

➔ Position 1-2: 5V/3.3V VBAT supply from micro-USB (J2) or Arduino (J7)

➔ Position 2-3: VBAT supply (typical 3.1~3.3V) from microSD connector

J12 = VDDIO Override Short for 3.3V VDDIO (open for 1.8V)

➔ Jumper Installed = VDDIO set to 3.3V; LED2 (Blue) illuminates

➔ Not Installed = VDDIO set to 1.8V (default)

J7 = Optional Arduino Header Power Supply

Pin#	J7 Signal		Pin#	J7 Signal
2	3V3		6	GND
4	3V3		7	GND
5	5V			

J8 = BT UART RTS/CTS Arduino Header

Pin#	J8 Signal		Pin#	J8 Signal
3	BT_UART_RTS_3V3		4	BT_UART_CTS_3V3

5 uSD-M.2 Adapter: Pinout Definition

Table 4: uSD-M.2 Adapter Pinout Definition

J#	Pin#	Name	I/O	V	Description
J1	1-2	SEL-LINK	N/A	3.3	5V/3.3V VBAT supply from micro-USB (J2) or Arduino Header (J7)
J1	2-3	SEL-LINK	N/A	3.0~3.3	VBAT supply (typical 3.1~3.3V) from microSD connector (default)
J2	1-5	USB micro-B	N/A	5.0	Optional 5V USB Power Supply via Micro-AB USB Connector
J3	1,7,18,33, 39,45,51, 57,63,69, 75	GND	N/A	N/A	M.2 Ground connections
J3	2,4,72,74	VBAT	N/A	3.3~3.6	M.2 VBAT supply
J3	8	BT_PCM_CLK_1V8	I/O	1.8	Bluetooth PCM Clock
J3	9	USD_CLK	I	1.8	SDIO Clock
J3	10	BT_PCM_SYNC_1V8	I/O	1.8	Bluetooth PCM Sync
J3	11	USD_CMD	I/O	1.8	SDIO Command
J3	12	BT_PCM_OUT_1V8	O	1.8	Bluetooth PCM Output
J3	13	USD_DATA0	I/O	1.8	SDIO DATA0
J3	14	BT_PCM_IN_1V8	I	1.8	Bluetooth PCM Input
J3	15	USD_DATA1	I/O	1.8	SDIO DATA1
J3	17	USD_DATA2	I/O	1.8	SDIO DATA2
J3	19	USD_DATA3	I/O	1.8	SDIO DATA3
J3	20	BT_HOST_WAKE_3V3	O	3.3	Bluetooth Host Wake: Active Low
J3	21	WL_HOST_WAKE_1V8	O	1.8	WLAN Host Wake: Active Low (OOB IRQ)
J3	22	BT_UART_TXD_1V8	O	1.8	Bluetooth UART Transmit
J3	32	BT_UART_RXD_1V8	I	1.8	Bluetooth UART Receive
J3	34	BT_UART_RTS_1V8	O	1.8	Bluetooth UART Request-To-Send

J#	Pin#	Name	I/O	V	Description
J3	36	BT_UART_CTS_1V8	I	1.8	Bluetooth Clear-To-Send
J3	38	WL_GPIO_5_1V8-JTAG_TDO	I/O	1.8	WLAN GPIO or JTAG Debug signal
J3	40	WL_GPIO_4_1V8-JTAG_TDI	I/O	1.8	WLAN GPIO or JTAG Debug signal
J3	42	BT_DEV_WAKE_1V8	I	1.8	Bluetooth Device Wake
J3	44	WL_GPIO_6_1V8-JTAG_TRST	I/O	1.8	WLAN GPIO or JTAG Debug signal
J3	46	WL_GPIO_2_1V8-JTAG_TCK	I/O	1.8	WLAN GPIO or JTAG Debug signal
J3	48	WL_GPIO_3_1V8-JTAG_TMS	I/O	1.8	WLAN GPIO or JTAG Debug signal
J3	50	LPO_IN_3V3	I	3.3	External Sleep Clock (32.768 kHz) – used in deep sleep mode
J3	54	BT_REG_ON_3V3	I	3.3	Enables/Disables Bluetooth core: Active High
J3	56	WL_REG_ON_3V3	I	3.3	Enables/Disables WLAN core: Active High
J3	59	BT_GPIO_2_1V8	I/O	1.8	Bluetooth GPIO
J3	61	BT_GPIO_3_1V8	I/O	1.8	Bluetooth GPIO
J3	62	GPIO10_WL_UART_CTS	I/O	1.8	WLAN GPIO or WLAN UART CTS Debug
J3	64	VDDIO override	I	1.8~3.3	Overrides default 1.8V VDDIO; used to force 3.3V operation on some supported M.2 Modules
J3	65	BT_GPIO_4_1V8-BT_DBG_RTS	I/O	1.8	Bluetooth GPIO or Bluetooth UART RTS Debug
J3	66	GPIO1_WL_DEV_WAKE	I	1.8	WLAN Device Wake
J3	67	BT_GPIO_5_1V8-BT_DBG_CTS	I/O	1.8	Bluetooth GPIO or Bluetooth UART CTS Debug
J3	68	GPIO9_WL_UART_TXD	I/O	1.8	WLAN GPIO or WLAN UART TX Debug
J3	70	GPIO8_WL_UART_RXD	I/O	1.8	WLAN GPIO or WLAN UART RX Debug
J3	71	BT_GPIO_6_1V8-BT_DBG_TXD	I/O	1.8	Bluetooth GPIO or Bluetooth UART TX Debug
J3	73	BT_GPIO_7_1V8-BT_DBG_RXD	I/O	1.8	Bluetooth GPIO or Bluetooth UART RX Debug
J4	1	USD_DATA2	I/O	1.8	microSD SDIO DATA2
J4	2	USD_DATA3	I/O	1.8	microSD SDIO DATA3

J#	Pin#	Name	I/O	V	Description
J4	3	USD_CMD	I/O	1.8	microSD SDIO Command
J4	4	VCC	N/A	3.0~3.3	VBAT supply from microSD
J4	5	USD_CLK	O	1.8	microSD SDIO Clock
J4	6	GND	N/A	N/A	microSD Ground
J4	7	USD_DATA0	I/O	1.8	microSD DATA0
J4	8	USD_DATA1	I/O	1.8	microSD DATA1
J5	1	BT_PCM_IN_3V3	I	1.8~3.3	Bluetooth PCM Input
J5	2	BT_GPIO_2_3V3	I/O	1.8~3.3	Bluetooth GPIO
J5	3	BT_PCM_OUT_3V3	O	1.8~3.3	Bluetooth PCM Output
J5	4	BT_GPIO_3_3V3	I/O	1.8~3.3	Bluetooth GPIO
J5	5	BT_PCM_SYNC_3V3	I/O	1.8~3.3	Bluetooth PCM Sync
J5	6	BT_GPIO_4_3V3-BT_DBG_RTS	I/O	1.8~3.3	Bluetooth GPIO or Bluetooth UART RTS Debug
J5	7	BT_PCM_CLK_3V3	I/O	1.8~3.3	Bluetooth PCM Clock
J5	8	BT_GPIO_5_3V3-BT_DBG_CTS	I/O	1.8~3.3	Bluetooth GPIO or Bluetooth UART CTS Debug
J5	9	GPIO10_3V3-WL_UART_CTS	I/O	1.8~3.3	WLAN GPIO or WLAN UART CTS Debug
J5	10	BT_GPIO_6_3V3-BT_DBG_TXD	I/O	1.8~3.3	Bluetooth GPIO or Bluetooth UART TX Debug
J5	11	GPIO9_3V3-WL_UART_TXD	I/O	1.8~3.3	WLAN GPIO or WLAN UART TX Debug
J5	12	BT_GPIO_7_3V3-BT_DBG_RXD	I/O	1.8~3.3	Bluetooth GPIO or Bluetooth UART RX Debug
J5	13	GPIO8_3V3-WL_UART_RXD	I/O	1.8~3.3	WLAN GPIO or WLAN UART RX Debug
J5	14	LPO_IN_3V3	I	3.3	External Sleep Clock (32.768 kHz) – used in deep sleep mode. Optional input to drive signal directly on this pin – or can be used to measure/check clock signal. If driving this pin with external clock; remove R4. Another option is to ground the clock input signal (install R5 and remove R4).
J5	15	GND	N/A	N/A	Ground connection; used for external power (i.e. lab bench power supply).

J#	Pin#	Name	I/O	V	Description
J5	16	USD_3V3	N/A	3.3	3.3V VBAT external power supply (i.e. lab bench power supply). Need to disconnect/remove Jumper J1.
J6	1	WL_REG_ON_3V3	I	1.8~3.3	Enables/Disables WLAN core: Active High
J6	2	WL_HOST_WAKE_3V3	O	1.8~3.3	WLAN Host Wake: Active Low (OOB IRQ)
J6	5	WL_DEV_WAKE_3V3	I	1.8~3.3	WLAN Device Wake
J6	6	BT_REG_ON_3V3	I	1.8~3.3	Enables/Disables Bluetooth Core: Active High
J6	7	BT_HOST_WAKE_3V3	O	1.8~3.3	Bluetooth Host Wake: Active Low
J6	8,20	GND	N/A	N/A	Ground
J6	9	BT_PCM_CLK_3V3	I/O	1.8~3.3	Bluetooth PCM Clock
J6	10	BT_PCM_SYNC_3V3	I/O	1.8~3.3	Bluetooth PCM Sync
J6	11	BT_PCM_OUT_3V3	O	1.8~3.3	Bluetooth PCM Output
J6	12	BT_PCM_IN_3V3	I	1.8~3.3	Bluetooth PCM Input
J6	13	BT_DEV_WAKE_3V3	I	1.8~3.3	Bluetooth Device Wake
J6	14,15	3V3	N/A	3.3	Alternative VBAT supply for Adapter
J6	16	BT_UART_RXD_3V3	I	1.8~3.3	Bluetooth UART Receive
J6	17	BT_UART_CTS_3V3	I	1.8~3.3	Bluetooth UART Clear-To-Send
J6	18	BT_UART_TXD_3V3	O	1.8~3.3	Bluetooth UART Transmit
J6	19	BT_UART_RTS_3V3	O	1.8~3.3	Bluetooth UART Request-To-Send
J7	2,4	3V3	N/A	3.3	Alternative VBAT supply for Adapter
J7	5,(8)	5V	N/A	5.0	Alternative VBAT supply for Adapter: to connect Pin #8, populate R41.
J7	6,7	GND	N/A	N/A	Ground
J8	3	BT_UART_RTS_3V3	O	1.8~3.3	Bluetooth UART Request-To-Send
J8	4	BT_UART_CTS_3V3	I	1.8~3.3	Bluetooth UART Clear-To-Send
J9	1	BT_UART_TXD_3V3	O	1.8~3.3	Bluetooth UART Transmit

J#	Pin#	Name	I/O	V	Description
J9	2	BT_UART_RXD_3V3	I	1.8~3.3	Bluetooth UART Receive
J9	3	WL_REG_ON_3V3	I		Enables/Disables WLAN core: Active High
J9	4	BT_REG_ON_3V3	I	1.8~3.3	Enables/Disables Bluetooth Core: Active High
J9	5	WL_HOST_WAKE_3V3	O	1.8~3.3	WLAN Host Wake: Active Low (OOB IRQ)
J9	6	BT_HOST_WAKE_3V3	O	1.8~3.3	Bluetooth Host Wake: Active Low
J9	7	WL_DEV_WAKE_3V3	I	1.8~3.3	WLAN Device Wake
J9	8	BT_DEV_WAKE_3V3	I	1.8~3.3	Bluetooth Device Wake
J10	2,4,6,8,10	GND	N/A	N/A	Ground
J10	1	WL_GPIO_6_1V8-JTAG_TRST	I/O	1.8~3.3	WLAN GPIO or JTAG Debug signal
J10	3	WL_GPIO_4_1V8-JTAG_TDI	I/O	1.8~3.3	WLAN GPIO or JTAG Debug signal
J10	5	WL_GPIO_5_1V8-JTAG_TDO	I/O	1.8~3.3	WLAN GPIO or JTAG Debug signal
J10	7	WL_GPIO_3_1V8-JTAG_TMS	I/O	1.8~3.3	WLAN GPIO or JTAG Debug signal
J10	9	WL_GPIO_2_1V8-JTAG_TCK	I/O	1.8~3.3	WLAN GPIO or JTAG Debug signal
J11	1	BT_REG_ON_3V3	N/A	N /A	Enables/Disables Bluetooth Core: Active High; J11 provides option to disable Bluetooth core
J11	2	GND	N/A	N/A	Ground
J12	1	VDDIO Override Connector	N/A	N/A	Connect J12: Pins 1-2 to force VDDIO = 3.3V
J12	2	VDDIO Override Connector	N/A	N/A	Connect J12: Pins 1-2 to force VDDIO = 3.3V

6 uSD-M.2 Adapter Schematic and Layout

For more specifics on adapter circuit and layout refer to Figure 5: uSD-M.2 Adapter Schematic, Figure 6: uSD-M.2 Adapter Layout (top), and Figure 7: uSD-M.2 Adapter Layout (bottom). Both schematic and layout files are available individually. Refer to Section 1.3 References.

Figure 5: uSD-M.2 Adapter Schematic

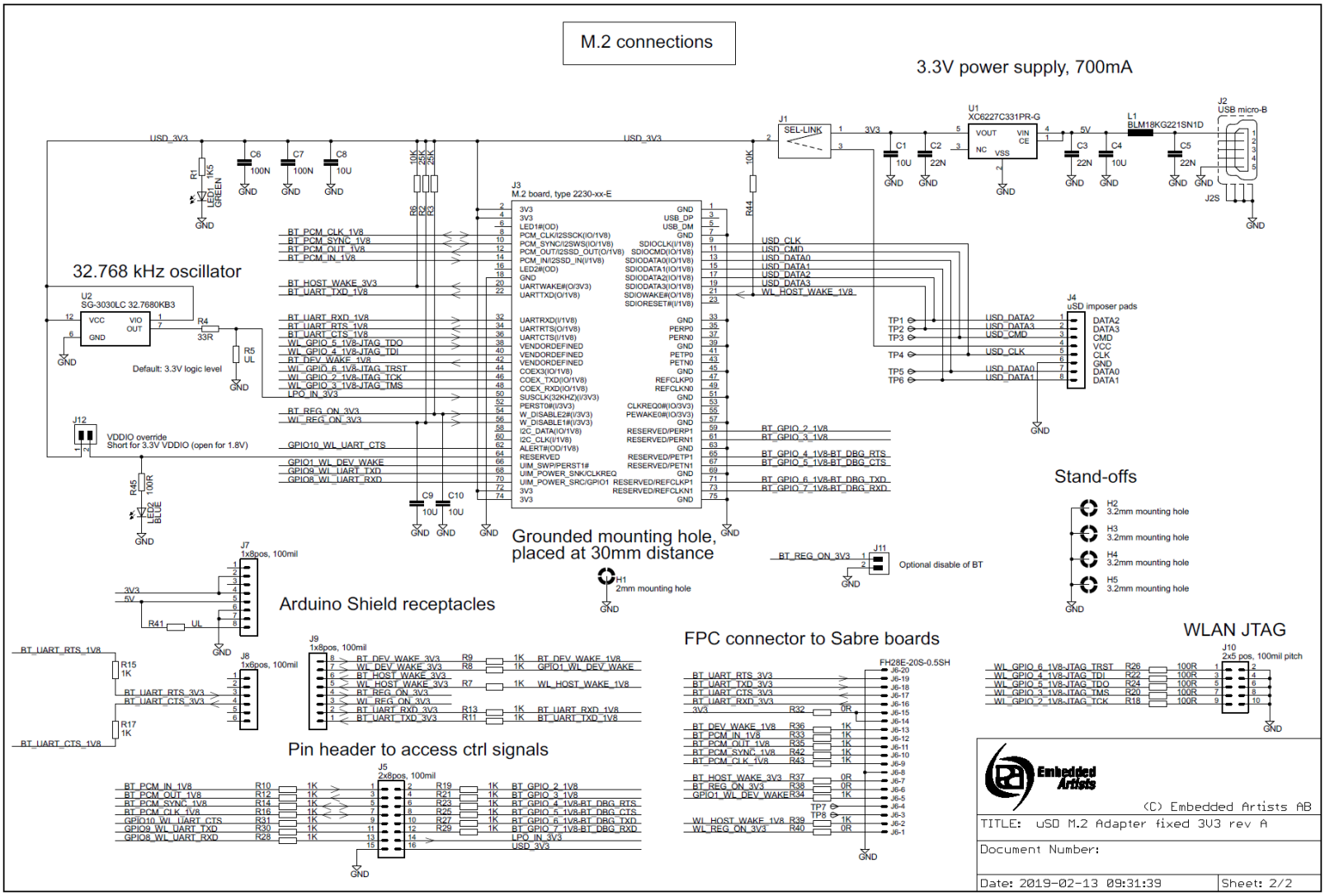


Figure 6: uSD-M.2 Adapter Layout (top)

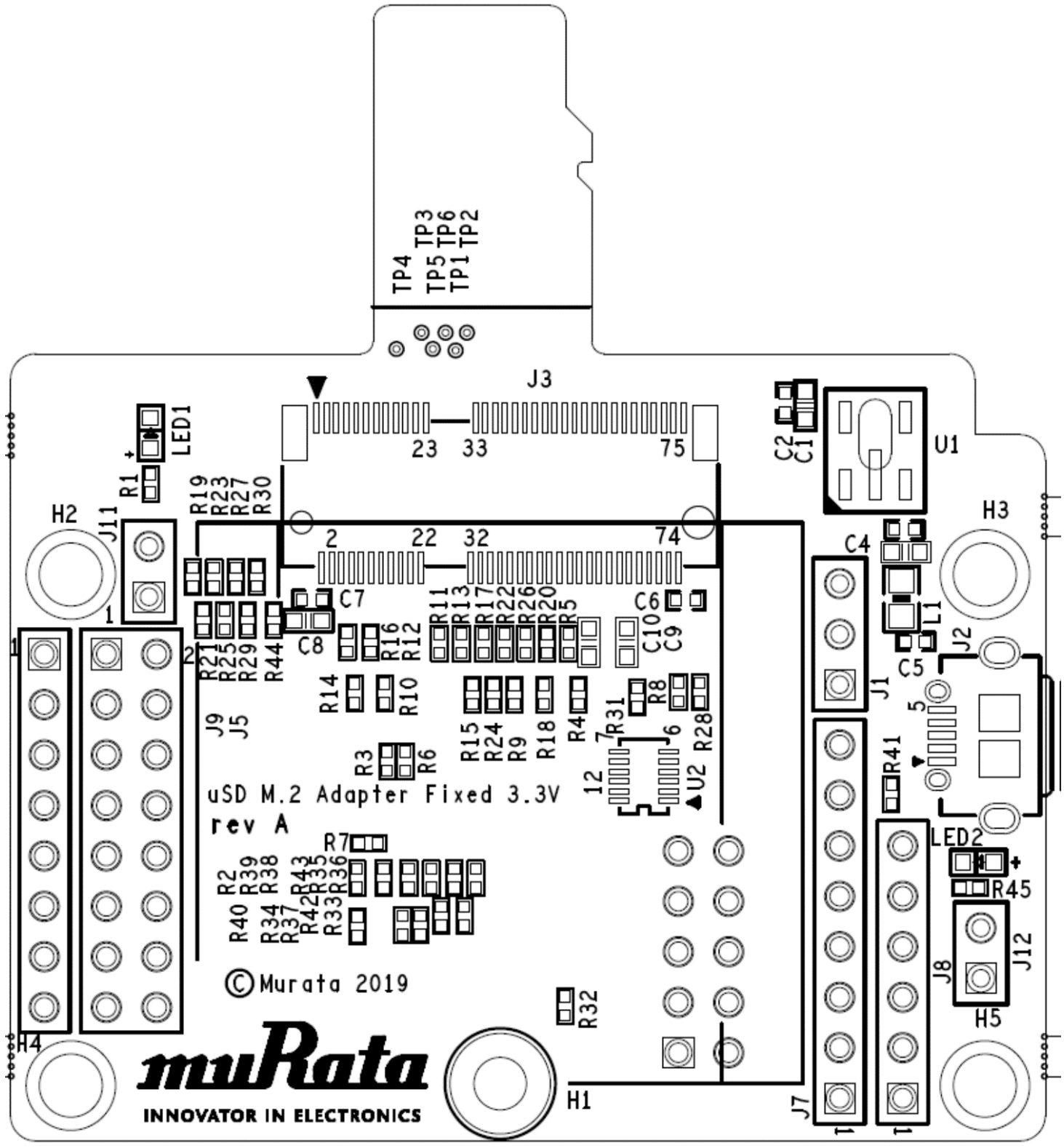


Figure 7: uSD-M.2 Adapter Layout (bottom)