

TLV320AIC3206 Ultra Low-Power Stereo Audio Codec

1 Features

- Stereo Audio DAC with 100-dB SNR
- 5.8-mW Stereo 48-ksps DAC-to-Ground-Centered Headphone Playback
- Stereo Audio ADC with 93-dB SNR
- 5.2-mW Stereo 48-ksps ADC Record
- PowerTune™
- Extensive Signal Processing Options
- Six Single-Ended or 3 Fully-Differential Analog Inputs
- Stereo Analog and Digital Microphone Inputs
- Ground-Centered Stereo Headphone Outputs
- Very Low-Noise PGA
- Low Power Analog Bypass Mode
- Programmable Microphone Bias
- Programmable PLL
- 5-mm x 5-mm 40-pin QFN or 3.5-mm x 3.3-mm 42-ball WCSP (DSBGA) Package

2 Applications

- Portable Navigation Devices (PND)
- Portable Media Player (PMP)
- Mobile Handsets
- Communication
- Portable Computing

3 Description

The TLV320AIC3206 (sometimes referred to as the AIC3206) is a flexible, low-power, low-voltage stereo audio codec with programmable inputs and outputs, PowerTune capabilities, fixed predefined and parameterizable signal processing blocks, integrated PLL and flexible digital interfaces.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---------------|------------|-------------------|
| TLV320AIC3206 | WQFN (40) | 5.00 mm x 5.00 mm |
| | DSBGA (42) | 3.49 mm x 3.29 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Block Diagram

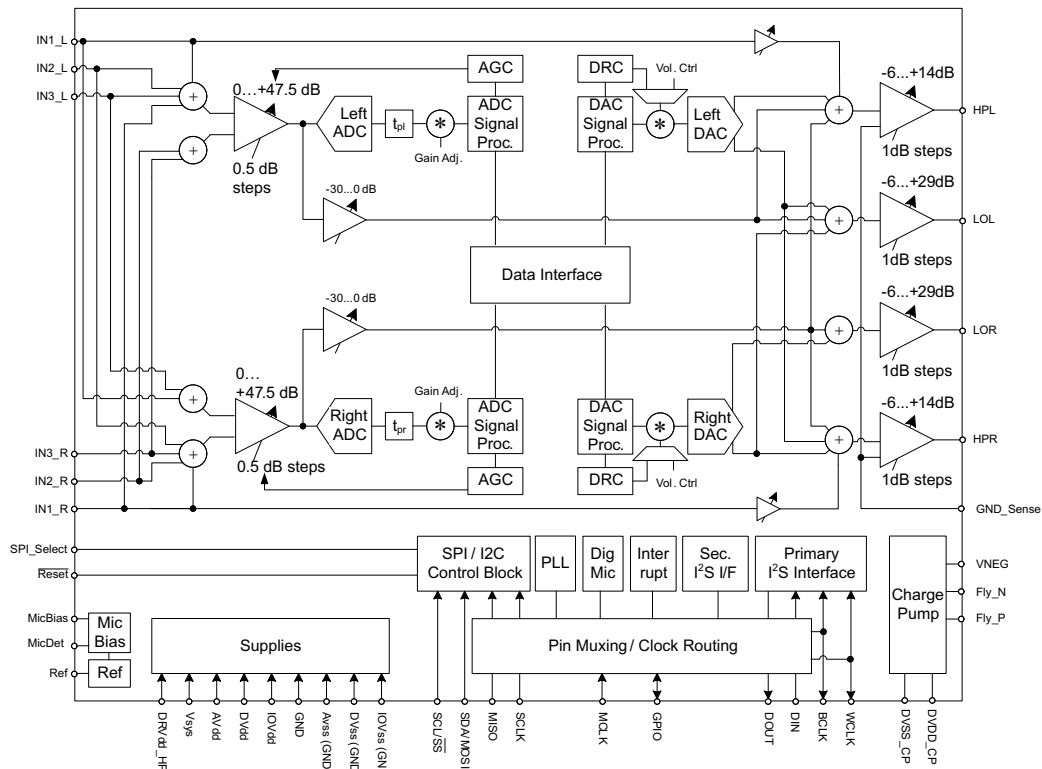


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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

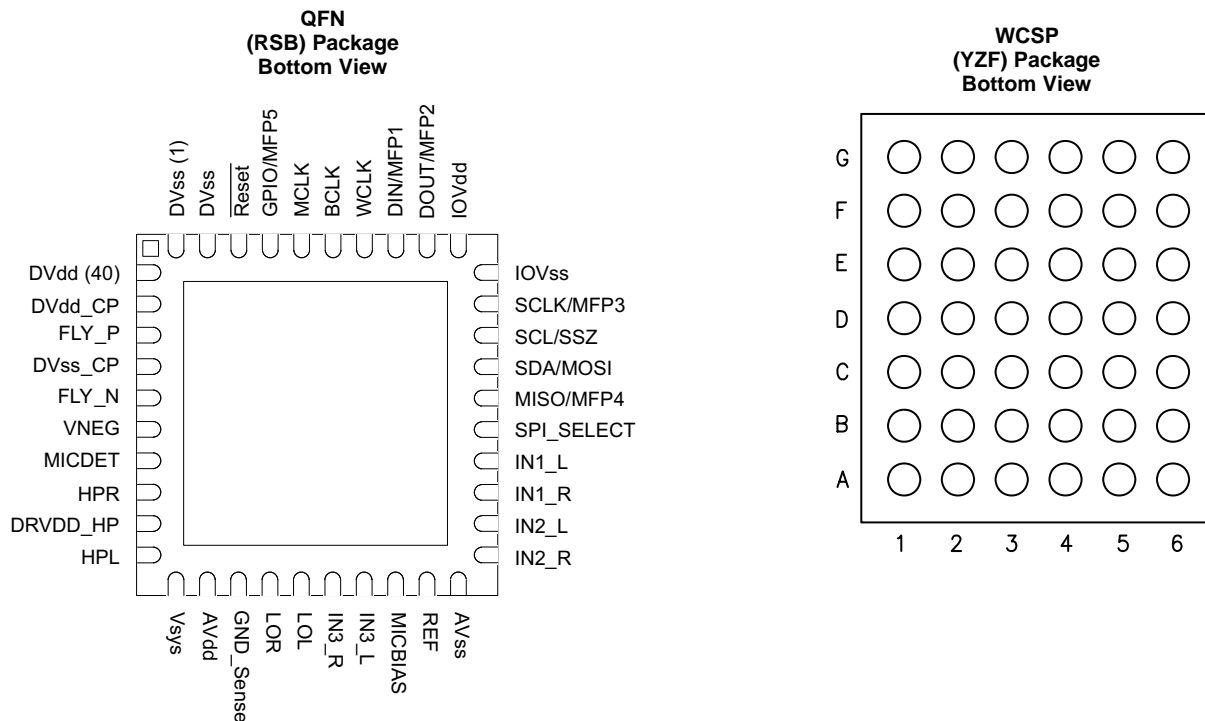
| Changes from Revision B (October 2012) to Revision C | Page |
|---|-----------|
| • Added <i>Pin Configuration and Functions</i> section, Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section | 1 |
| • Added Note 1 to the Pin Functions table | 4 |
| • Added "Audio input mux ac signal swing" to the Recommended Operating Conditions table | 7 |
| • Added the Digital Microphone PDM Timing (see Figure 5) section | 18 |

| Changes from Revision A (December 2010) to Revision B | Page |
|---|-----------|
| • Added WCSP package (YZF) | 1 |
| • Corrected typos and spelling errors throughout data sheet | 1 |
| • Updated block diagram to include Vsys pin | 1 |
| • Updated diagram to include Vsys pin | 36 |
| • Updated power supply section to include Vsys | 40 |

6 Device Comparison Table

| PART NUMBER | DESCRIPTION |
|-------------------------------|---|
| TLV320AIC3254 | Low power stereo audio codec with miniDSP. |
| TLV320AIC3204 | Same as TLV320AIC3204 but without miniDSP. |
| TLV320AIC3256 | Similar to TLV320AIC3254 but with ground centered headphone output. |
| TLV320AIC3206 | Same as TLV320AIC3256 but without miniDSP. |

7 Pin Configuration and Functions



Pin Functions

| PIN | | WCSP (YZF) BALL NO. | TYPE ⁽¹⁾ | DESCRIPTION |
|------------------|------------------|---------------------------|---------------------|--|
| NAME | QFN (RSB) NO. | | | |
| DVss | 1 | B2 | GND | Digital ground. Device substrate. |
| DVss | 2 | A1 | GND | Digital ground |
| RESET | 3 | C5 | DI | Hardware reset |
| GPIO MFP5 | 4 | B3 | DI/O | Primary function: General purpose digital IO Secondary function: CLKOUT output INT1 output INT2 output Audio serial data bus ADC word clock output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output Digital microphone clock output |
| MCLK | 5 | A2 | DI | Master clock input |
| BCLK | 6 | B4 | DI/O | Audio serial data bus (primary) bit clock |
| WCLK | 7 | A3 | DI/O | Audio serial data bus (primary) word clock |
| DIN MFP1 | 8 | A5 | DI | Primary function: Audio serial data bus data input Secondary function: Digital Microphone Input General Purpose Clock Input General Purpose Input |
| DOUT | 9 | A4 | DO | Primary function: |

(1) DI (Digital Input), DO (Digital Output), DIO (Digital Input/Output), AI (Analog Input), AO (Analog Output), AIO (Analog Input/Output)

Pin Functions (continued)

| PIN | | WCSP (YZF) BALL NO. | TYPE ⁽¹⁾ | DESCRIPTION |
|-------------|------------------|---------------------------|---------------------|---|
| NAME | QFN (RSB) NO. | | | |
| MFP2 | | | | Audio serial data bus data output Secondary function: General purpose output Clock output INT1 output INT2 output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output |
| IOVdd | 10 | A6 | PWR | Supply for IO buffers. 1.1V to 3.6V |
| IOVss | 11 | B5 | GND | Ground for IO buffers. |
| SCLK | 12 | C4 | DI | Primary function: (SPI_Select = 1) SPI serial clock Secondary function:: (SPI_Select = 0) Digital microphone input Audio serial data bus (secondary) bit clock input Audio serial data bus (secondary) DAC/common word clock input Audio serial data bus (secondary) ADC word clock input Audio serial data bus (secondary) data input General purpose input |
| SCL SS | 13 | B6 | DI | I ² C interface serial clock (SPI_Select = 0) SPI interface mode chip-select signal (SPI_Select = 1) |
| SDA MOSI | 14 | C3 | DI/O | I ² C interface mode serial data input (SPI_Select = 0) SPI interface mode serial data input (SPI_Select = 1) |
| MISO | 15 | D4 | DO | Primary function: (SPI_Select = 1) Serial data output Secondary function: (SPI_Select = 0) General purpose output CLKOUT output INT1 output INT2 output Audio serial data bus (primary) ADC word clock output Digital microphone clock output Audio serial data bus (secondary) data output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output |
| SPI_SELECT | 16 | C6 | DI | Control mode select pin (1 = SPI, 0 = I ² C) |
| IN1_L | 17 | D6 | AI | Multifunction analog input, Single-ended configuration: MIC 1 or Line 1 left Differential configuration: MIC or Line right, negative |
| IN1_R | 18 | E6 | AI | Multifunction analog input, Single-ended configuration: MIC 1 or Line 1 right Differential configuration: MIC or Line right, positive |
| IN2_L | 19 | F6 | AI | Multifunction analog input, Single-ended configuration: MIC 2 or Line 2 right Differential configuration: MIC or Line left, positive |
| IN2_R | 20 | G6 | AI | Multifunction analog input, Single-ended configuration: MIC 2 or Line 2 right Differential configuration: MIC or Line left, negative |
| AVss | 21 | E4, E5 | GND | Analog Ground |
| REF | 22 | G5 | AO | Reference voltage output for filtering |
| MICBIAS | 23 | G4 | AO | Microphone bias voltage output |

Pin Functions (continued)

| PIN | | WCSP (YZF) BALL NO. | TYPE ⁽¹⁾ | DESCRIPTION |
|-------------|------------------|---------------------------|---------------------|--|
| NAME | QFN (RSB) NO. | | | |
| IN3_L | 24 | F5 | AI | Multifunction analog input, Single-ended configuration: MIC3 or Line 3 left, Differential configuration: MIC or Line left, positive, Differential configuration: MIC or Line right, negative |
| IN3_R | 25 | F4 | AI | Multifunction analog input, Single-ended configuration: MIC3 or Line 3 right, Differential configuration: MIC or Line left, negative, Differential configuration: MIC or Line right, positive |
| LOL | 26 | G3 | AO | Left line output |
| LOR | 27 | F3 | AO | Right line output |
| GND_SENSE | 28 | E3 | AI | External ground reference for headphone interface –0.5V to 0.5V |
| AVdd | 29 | G2 | PWR | Analog voltage supply 1.5V–1.95V |
| Vsys | 30 | G1 | PWR | Power supply 1.5V–5.5V, Vsys must always be greater than or equal to AVdd and DVdd (Vsys ≥ AVdd, DVdd) |
| HPL | 31 | F1 | AO | Left headphone output |
| DRVdd_HP | 32 | F2 | PWR | Power supply for headphone output stage Ground-centered circuit configuration, 1.5V to 1.95V Unipolar circuit configuration, 1.5V to 3.6V |
| HPR | 33 | E1 | AO | Right headphone output |
| MICDET | 34 | E2 | AI | Microphone detection |
| VNEG | 35 | D1 | PWR | Negative supply for headphones. –1.8V to 0V Input when charge pump is disabled, Filtering output when charge pump is enabled |
| FLY_N | 36 | D2 | PWR | Negative terminal for charge-pump flying capacitor |
| DVss_CP | 37 | D3 | GND | Charge pump ground |
| FLY_P | 38 | C2 | PWR | Positive terminal for charge pump flying capacitor |
| DVdd_CP | 39 | C1 | PWR | Charge Pump supply; recommended to connect to DVdd |
| DVdd | 40 | B1 | PWR | Digital voltage supply 1.26V – 1.95V |
| Thermal Pad | Thermal Pad | N/A | N/A | Connect to PCB ground plane. Not internally connected. |

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | MIN | MAX | UNIT |
|---|-------|-------------|------|
| AVdd to AVss | –0.3 | 2.2 | V |
| DVdd to DVss | –0.3 | 2.2 | V |
| Vsys to DVss | –0.3 | 5.5 | V |
| IOVdd to IOVss | –0.3 | 3.9 | V |
| Digital Input voltage | IOVss | IOVdd + 0.3 | V |
| Analog input voltage | AVss | AVdd + 0.3 | V |
| Operating temperature range | –40 | 85 | °C |
| Junction temperature (T _J Max) | | 105 | °C |

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 Handling Ratings

| | | MIN | MAX | UNIT |
|--------------------|---------------------------|--|-----|------|
| T _{stg} | Storage temperature range | –55 | 125 | °C |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | | kV |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

| | | | | MIN | NOM | MAX | UNIT |
|--|---|---|------------------------|-------|-------|------------------------------------|-------|
| AV _{DD} | Power Supply Voltage Range | Referenced to AVss ⁽¹⁾ | | 1.5 | 1.8 | 1.95 | V |
| IOV _{DD} | | Referenced to IOVss ⁽¹⁾ | | 1.1 | | 3.6 | |
| Vsys | | Referenced to DVss ⁽¹⁾ | | 1.5 | 1.8 | 5.5 | |
| DVdd ⁽²⁾ | | Referenced to DVss ⁽¹⁾ | | 1.26 | 1.8 | 1.95 | |
| DVDD_CP | Power Supply Voltage Range | Referenced to DVss ⁽¹⁾ | | 1.26 | 1.8 | 1.95 | V |
| DRVDD_HP | | Referenced to AVss ⁽¹⁾ | Ground-centered config | 1.5 | 1.8 | 1.95 | |
| | | | Unipolar config | 1.5 | | 3.6 | |
| PLL Input Frequency | | Clock divider uses fractional divide (D > 0), P = 1, DV _{dd} ≥ 1.65V (See table in SLAA463, <i>Maximum TLV320AIC3206 Clock Frequencies</i>) | | 10 | | 20 | MHz |
| | | Clock divider uses integer divide (D = 0), P = 1, DV _{dd} ≥ 1.65V (See table in SLAA463, <i>Maximum TLV320AIC3206 Clock Frequencies</i>) | | 0.512 | | 20 | MHz |
| MCLK | Master Clock Frequency | MCLK; Master Clock Frequency; DV _{dd} ≥ 1.65V | | | | 50 | MHz |
| | | MCLK; Master Clock Frequency; DV _{dd} ≥ 1.26V | | | | 25 | |
| SCL | SCL Clock Frequency | | | | | 400 | kHz |
| Audio input max ac signal swing (IN1_L, IN1_R, IN2_L, IN2_R, IN3_L, IN3_R) | | CM = 0.75 V | | 0 | 0.530 | 0.75 or AVDD - 0.75 ⁽³⁾ | Vpeak |
| | | CM = 0.9 V | | 0 | 0.707 | 0.9 or AVDD - 0.9 ⁽³⁾ | Vpeak |
| LOL, LOR | Stereo line output load resistance | | | | 0.6 | 10 | kΩ |
| HPL, HPR | Stereo headphone output load resistance | Single-ended configuration | | | 14.4 | 16 | Ω |
| | Headphone output load resistance | Differential configuration | | | 24.4 | 32 | Ω |
| C _{Lout} | Digital output load capacitance | | | | | 10 | pF |
| TOPR | Operating Temperature Range | | | | −40 | | 85 °C |

(1) All grounds on board are tied together; they must not differ in voltage by more than 0.2V max, for any combination of ground signals.

(2) At DV_{dd} values lower than 1.65V, the PLL does not function. Please see table in SLAA463, *Maximum TLV320AIC3206 Clock Frequencies* for details on maximum clock frequencies.

(3) Whichever is smaller

8.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TLV320AIC3206 | | UNIT |
|-------------------------------|--|---------------|-------------|------|
| | | RSB (QFN) | YZF (DSGBA) | |
| | | 48 PINS | 42 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 32.3 | 49.7 | °C/W |
| R _{θJCTop} | Junction-to-case (top) thermal resistance | 22.5 | 0.1 | |
| R _{θJB} | Junction-to-board thermal resistance | 6.1 | 7.7 | |
| ψ _{JT} | Junction-to-top characterization parameter | 0.3 | 0.1 | |
| ψ _{JB} | Junction-to-board characterization parameter | 6 | 7.7 | |
| R _{θJCbot} | Junction-to-case (bottom) thermal resistance | 1.7 | – | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

8.5 Electrical Characteristics, ADC

At 25°C, V_{sys}, AV_{dd}, DV_{dd}, IOV_{dd}, DV_{dd_CP}, DRV_{dd_HP} = 1.8V, f_s (Audio) = 48kHz, C_{ref} = 1μF on REF PIN, PLL and Charge pump disabled unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|--|--|-------|-----|-----|------------------|
| AUDIO ADC (CM = 0.9V) | | | | | | |
| Input signal level (for 0dB output) | | Single-ended, CM = 0.9V | 0.5 | | | V _{RMS} |
| Device Setup | | 1kHz sine wave input Single-ended Configuration IN1_R to Right ADC and IN1_L to Left ADC, R _{IN} = 20kΩ, f _S = 48kHz, AOSR = 128, MCLK = 256 * f _S , PLL Disabled; AGC = OFF, Channel Gain = 0dB, Processing Block = PRB_R1, Power Tune = PTM_R4 | | | | |
| SNR | Signal-to-noise ratio, A-weighted ^{(1) (2)} | Inputs ac-short to ground | 80 | 93 | | dB |
| | | IN2_R, IN3_R routed to Right ADC and ac-short to ground IN2_L, IN3_L routed to Left ADC and ac-short to ground | 93 | | | |
| DR | Dynamic range A-weighted ^{(1) (2)} | −60dB full-scale, 1kHz input signal | 93 | | | dB |
| THD+N | Total Harmonic Distortion plus Noise | −3dB full-scale, 1kHz input signal | −84 | −70 | | dB |
| | | IN2_R, IN3_R routed to Right ADC IN2_L, IN3_L routed to Left ADC −3dB full-scale, 1kHz input signal | −84 | | | |
| AUDIO ADC (CM = 0.75V) | | | | | | |
| Input signal level (for 0dB output) | | Single-ended, CM = 0.75V, AVdd = 1.5V | 0.375 | | | V _{RMS} |
| Device Setup: | | 1kHz sine wave input Single-ended Configuration INR, IN2_R, IN3_R routed to Right ADC INL, IN2_L, IN3_L routed to Left ADC R _{IN} = 20kΩ, f _S = 48kHz, AOSR = 128, MCLK = 256 * f _S , PLL Disabled, AGC = OFF, Channel Gain = 0dB, Processing Block = PRB_R1 Power Tune = PTM_R4 | | | | |
| SNR | Signal-to-noise ratio, A-weighted ^{(1) (2)} | Inputs ac-short to ground | 90 | | | dB |

(1) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.

(2) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

Electrical Characteristics, ADC (continued)

At 25°C, V_{sys}, AV_{dd}, DV_{dd}, IOV_{dd}, DV_{dd_CP}, DRV_{dd_HP} = 1.8V, f_s (Audio) = 48kHz, C_{ref} = 1μF on REF PIN, PLL and Charge pump disabled unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|---|---|-----|------|-----|-------------------|
| DR | Dynamic range A-weighted ^{(1) (2)} | –60dB full-scale, 1kHz input signal | | 90 | | dB |
| THD+N | Total Harmonic Distortion plus Noise | –3dB full-scale, 1kHz input signal | | –81 | | dB |
| AUDIO ADC (Gain = 40dB) | | | | | | |
| | Input signal level (for 0dB output) | Differential Input, CM = 0.9V, Channel Gain = 40dB | | 10 | | mV _{RMS} |
| | Device Setup | 1kHz sine wave input Differential configuration IN1_L and IN1_R routed to Right ADC IN2_L and IN2_R routed to Left ADC R _{IN} = 10kΩ, f _s = 48kHz, AOSR = 128 MCLK = 256 * f _s PLL Disabled AGC = OFF Processing Block = PRB_R1, Power Tune = PTM_R4 | | | | |
| ICN | Idle-Channel Noise, A-weighted ^{(1) (2)} | Inputs ac-short to ground, input referred noise | | 2.8 | | μV _{RMS} |
| AUDIO ADC | | | | | | |
| | Gain Error | 1kHz sine wave input Single-ended configuration R _{IN} = 20kΩ, f _s = 48kHz, AOSR = 128, MCLK = 256 * f _s , PLL Disabled AGC = OFF, Channel Gain = 0dB Processing Block = PRB_R1, Power Tune = PTM_R4, CM = 0.9V | | 0.1 | | dB |
| | Input Channel Separation | 1kHz sine wave input at –3dBFS Single-ended configuration IN1_L routed to Left ADC IN1_R routed to Right ADC, R _{IN} = 20kΩ AGC = OFF, AOSR = 128, Channel Gain = 0dB, CM = 0.9V | | 109 | | dB |
| | Input Pin Crosstalk | 1kHz sine wave input at –3dBFS on IN2_L, IN2_L internally not routed. IN1_L routed to Left ADC ac-coupled to ground 1kHz sine wave input at –3dBFS on IN2_R, IN2_R internally not routed. IN1_R routed to Right ADC ac-coupled to ground Single-ended configuration R _{IN} = 20kΩ, AOSR = 128 Channel, Gain = 0dB, CM = 0.9V | | 108 | | dB |
| | PSRR | 217Hz, 100mVpp signal on AV _{dd} , Single-ended configuration, R _{IN} = 20kΩ, Channel Gain = 0dB; CM = 0.9V | | 55 | | dB |
| | ADC programmable gain amplifier gain | Single-Ended, R _{IN} = 10kΩ, PGA gain set to 0dB | | 0 | | dB |
| | | Single-Ended, R _{IN} = 10kΩ, PGA gain set to 47.5dB | | 47.5 | | dB |
| | | Single-Ended, R _{IN} = 20kΩ, PGA gain set to 0dB | | –6 | | dB |
| | | Single-Ended, R _{IN} = 20kΩ, PGA gain set to 47.5dB | | 41.5 | | dB |
| | | Single-Ended, R _{IN} = 40kΩ, PGA gain set to 0dB | | –12 | | dB |
| | | Single-Ended, R _{IN} = 40kΩ, PGA gain set to 47.5dB | | 35.5 | | dB |
| | ADC programmable gain amplifier step size | 1kHz tone | | 0.5 | | dB |

8.6 Electrical Characteristics, Bypass Outputs

At 25°C, V_{sys}, A_Vdd, D_Vdd, I_OVdd, D_Vdd_CP, D_RVdd_HP = 1.8V, f_s (Audio) = 48kHz, C_{ref} = 1μF on REF PIN, PLL and Charge pump disabled unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---------------------------|--|-----|-----|-----|-------------------|
| ANALOG BYPASS TO HEADPHONE AMPLIFIER, DIRECT MODE | | | | | | |
| Device Setup | | Load = 16Ω (single-ended), 50pF; Input and Output CM = 0.9V; Headphone Output on D _R Vdd_HP Supply; IN1_L routed to HPL and IN1_R routed to HPR; Channel Gain = 0dB | | | | |
| Gain Error | | | | 0.8 | | dB |
| Noise, A-weighted ⁽¹⁾ | | Idle Channel, IN1_L and IN1_R ac-shortcd to ground | | 3.3 | | μV _{RMS} |
| THD | Total Harmonic Distortion | 446mV _{rms} , 1kHz input signal | | –81 | | dB |
| ANALOG BYPASS TO LINE-OUT AMPLIFIER, PGA MODE | | | | | | |
| Device Setup | | Load = 10kΩ (single-ended), 50pF; Input and Output CM = 0.9V; LINE Output on D _R VDD_HP Supply; IN1_L, IN1_R routed to line out Channel Gain = 0dB | | | | |
| Gain Error | Gain Error | | | 0.8 | | dB |
| Noise, A-weighted ⁽¹⁾ | | Idle Channel, IN1_L and IN1_R ac-shortcd to ground | | 6.7 | | μV _{RMS} |
| | | Channel Gain = 40dB, Input Signal (0dB) = 5mV _{RMS} Inputs ac-shortcd to ground, Input Referred | | 3 | | μV _{RMS} |

(1) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

8.7 Electrical Characteristics, Microphone Interface

At 25°C, V_{sys}, AV_{dd}, DV_{dd}, IOV_{dd}, DV_{dd_CP}, DRV_{dd_HP} = 1.8V, fs (Audio) = 48kHz, C_{ref} = 1μF on REF PIN, PLL and Charge pump disabled unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---|-----|----------------------|-----|-------------------|
| MICROPHONE BIAS | | | | | |
| Bias voltage | <i>Bias voltage CM = 0.9V, DRV_{dd_HP} = 1.8V</i> | | | | |
| | Micbias Mode 0, Connect to AV _{dd} or DRV _{dd_HP} | | 1.5 | | V |
| | Micbias Mode 3, Connect to AV _{dd} | | AV _{dd} | | V |
| | Micbias Mode 3, Connect to DRV _{dd_HP} | | DRV _{dd_HP} | | V |
| | <i>CM = 0.75V, DRV_{dd_HP} = 1.8V</i> | | | | |
| | Micbias Mode 0, Connect to AV _{dd} or DRV _{dd_HP} | | 1.23 | | V |
| | Micbias Mode 1, Connect to AV _{dd} or DRV _{dd_HP} | | 1.43 | | V |
| | Micbias Mode 3, Connect to AV _{dd} | | AV _{dd} | | V |
| | Micbias Mode 3, Connect to DRV _{dd_HP} | | DRV _{dd_HP} | | V |
| MICROPHONE BIAS | | | | | |
| Bias voltage | <i>Bias voltage CM = 0.9V, DRV_{dd_HP} = 3.3V</i> | | | | |
| | Micbias Mode 0, Connect to DRV _{dd_HP} | | 1.5 | | V |
| | Micbias Mode 1, Connect to DRV _{dd_HP} | | 1.7 | | V |
| | Micbias Mode 2, Connect to DRV _{dd_HP} | | 2.5 | | V |
| | Micbias Mode 3, Connect to DRV _{dd_HP} | | DRV _{dd_HP} | | V |
| | <i>CM = 0.75V, DRV_{dd_HP} = 3.3V</i> | | | | |
| | Micbias Mode 0, Connect to DRV _{dd_HP} | | 1.23 | | V |
| | Micbias Mode 1, Connect to DRV _{dd_HP} | | 1.43 | | V |
| | Micbias Mode 2, Connect to DRV _{dd_HP} | | 2.1 | | V |
| | Micbias Mode 3, Connect to DRV _{dd_HP} | | DRV _{dd_HP} | | V |
| Output Noise | CM = 0.9V, Micbias Mode 2, A-weighted, 20Hz to 20kHz bandwidth, Current load = 0mA. | | 9.5 | | μV _{RMS} |
| Current Sourcing | Micbias Mode 2, Connect to DRV _{dd_HP} | | 3 | | mA |
| Inline Resistance | Micbias Mode 3, Connect to AV _{dd} | | 131 | | Ω |
| | Micbias Mode 3, Connect to DRV _{dd_HP} | | 89 | | |

8.8 Electrical Characteristics, Audio DAC Outputs

At 25°C, V_{sys}, AV_{dd}, DV_{dd}, IOV_{dd}, DV_{dd_CP}, DRV_{dd_HP} = 1.8V, f_s (Audio) = 48kHz, C_{ref} = 1μF on REF PIN, PLL and Charge pump disabled unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|--|-----|-------|-----|------------------|
| AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT (CM = 0.9V) | | | | | | |
| Device Setup | | Load = 10kΩ (single-ended), 56pF Line Output on AV _{dd} Supply Input and Output CM=0.9V DOSR = 128, MCLK = 256 x f _s , Channel Gain = 0dB, word length = 16 bits, Processing Block = PRB_P1, Power Tune = PTM_P3 | | | | |
| Full scale output voltage (0dB) | | | | 0.5 | | V _{RMS} |
| SNR | Signal-to-noise ratio A-weighted ^{(1) (2)} | All zeros fed to DAC input | 87 | 100 | | dB |
| DR | Dynamic range, A-weighted ^{(1) (2)} | –60dB 1kHz input full-scale signal, Word length = 20 bits | | 100 | | dB |
| THD+N | Total Harmonic Distortion plus Noise | –3dB full-scale, 1kHz input signal | | –81 | –70 | dB |
| DAC Gain Error | | 0dB, 1kHz input full scale signal | | 0.5 | | dB |
| DAC Mute Attenuation | | Mute | | 121 | | dB |
| DAC channel separation | | –1dB, 1kHz signal, between left and right HP out | | 108 | | dB |
| DAC PSRR | | 100mVpp, 1kHz signal applied to AV _{dd} | | 72 | | dB |
| | | 100mVpp, 217Hz signal applied to AV _{dd} | | 80 | | dB |
| AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT (CM = 0.75V) | | | | | | |
| Device Setup | | Load = 10kΩ (single-ended), 56pF Line Output on AV _{dd} Supply Input and Output CM = 0.75V; AV _{dd} = 1.5V DOSR = 128 MCLK=256 x f _s Channel Gain = 0dB word length = 20-bits Processing Block = PRB_P1 Power Tune = PTM_P4 | | | | |
| Full scale output voltage (0dB) | | | | 0.375 | | V _{RMS} |
| SNR | Signal-to-noise ratio, A-weighted ^{(1) (2)} | All zeros fed to DAC input | | 99 | | dB |
| DR | Dynamic range, A-weighted ^{(1) (2)} | –60dB 1kHz input full-scale signal | | 98 | | dB |
| THD+N | Total Harmonic Distortion plus Noise | –1dB full-scale, 1kHz input signal | | –77 | | dB |
| AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT (GROUND-CENTERED CIRCUIT CONFIGURATION) | | | | | | |
| Device Setup | | Load = 16Ω (single-ended), 56pF Input CM = 0.9V, Output CM = 0V DOSR = 128, MCLK = 256x* f _s , Channel Gain = 0dB word length = 16 bits; Processing Block = PRB_P1 Power Tune = PTM_P3 | | | | |
| FS1 | Full scale output voltage (for THD ≤ –40dB) | | | 0.65 | | V _{RMS} |
| SNR | Signal-to-noise ratio, A-weighted ^{(1) (2)} | All zeros fed to DAC input | 85 | 95 | | dB |
| DR | Dynamic range, A-weighted ^{(1) (2)} | –60dB 1kHz input full-scale signal, Word Length = 20 bits, Power Tune = PTM_P4 | | 93 | | dB |
| THD+N | Total Harmonic Distortion plus Noise | 500mV _{RMS} output (corresponds to FS1 – 2.3dB), 1-kHz input signal | | –70 | –55 | dB |

- (1) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
- (2) All performance measured with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

Electrical Characteristics, Audio DAC Outputs (continued)

At 25°C, V_{sys}, AV_{dd}, DV_{dd}, IOV_{dd}, DV_{dd_CP}, DRV_{dd_HP} = 1.8V, f_s (Audio) = 48kHz, C_{ref} = 1μF on REF PIN, PLL and Charge pump disabled unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--|-----|------|-----|------------------|
| DAC Gain Error | | 500mV _{RMS} output, 1kHz input full scale signal | | 0.5 | | dB |
| DAC Mute Attenuation | | Mute | | 118 | | dB |
| DAC channel separation | | –3dB, 1kHz signal, between left and right HP out | | 102 | | dB |
| DAC PSRR | | 100mV _{pp} , 1kHz signal applied to AV _{dd} | | 66 | | dB |
| | | 100mV _{pp} , 217Hz signal applied to AV _{dd} | | 77 | | dB |
| Power Delivered | | THD ≤ –40dB | | 26.5 | | mW |
| FS2 | Full scale output voltage (for THD ≤ –40dB) | Load = 32Ω | | 0.85 | | V |
| SNR | Signal-to-noise ratio, A-weighted ^{(1) (2)} | All zeros fed to DAC input, Load = 32Ω | | 96 | | dB |
| Power Delivered | | THD ≤ –40dB, Load = 32Ω | | 22.5 | | mW |
| AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT (UNIPOLAR CIRCUIT CONFIGURATION) | | | | | | |
| Device Setup | | Load = 16Ω (single-ended), 56pF, Headphone Output on AV _{dd} Supply, Input and Output CM = 0.9V, DOSR = 128, MCLK = 256 x f _s , Channel Gain = 0dB, Processing Block = PRB_P1, Power Tune = PTM_P3 | | | | |
| Full scale output voltage (0dB) | | | | 0.5 | | V _{RMS} |
| SNR | Signal-to-noise ratio, A-weighted ^{(1) (2)} | All zeros fed to DAC input | 87 | 100 | | dB |
| DR | Dynamic range, A-weighted ^{(1) (2)} | –60dB 1kHz input full-scale signal | | 100 | | dB |
| THD+N | Total Harmonic Distortion plus Noise | –3dB full-scale, 1kHz input signal | | –83 | –70 | dB |

8.9 Electrical Characteristics, Misc.

At 25°C, V_{sys}, AV_{dd}, DV_{dd}, IOV_{dd}, DV_{dd_CP}, DRV_{dd_HP} = 1.8V, f_s (Audio) = 48kHz, C_{ref} = 1μF on REF PIN, PLL and Charge pump disabled unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|--|--|-----|------|-----|-------------------|
| REFERENCE | | | | | | |
| Reference Voltage Settings | | CMMODE = 0 (0.9V) | | 0.9 | | V |
| | | CMMODE = 1 (0.75V) | | 0.75 | | |
| Reference Noise | | CM = 0.9V, A-weighted, 20Hz to 20kHz bandwidth, C _{REF} = 1μF | | 1.1 | | μV _{RMS} |
| Decoupling Capacitor | | | | 1 | | μF |
| Bias Current | | | | 120 | | μA |
| SHUTDOWN CURRENT | | | | | | |
| Device Setup | | DV _{dd} is provided externally, no clocks supplied, no digital activity, register values are retained | | | | |
| I _(total) | | Sum of all supply currents, all supplies at 1.8V | | <10 | | μA |

8.10 Electrical Characteristics, Logic Levels⁽¹⁾

At 25°C, AV_{DD}, DV_{DD}, IOV_{DD} = 1.8 V

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|--|-------------------------|-------------------------|-------------------------|------|
| LOGIC FAMILY CMOS | | | | | |
| V _{IH} Logic Level | I _{IH} = 5 μA, IOV _{DD} > 1.6V | 0.7 × IOV _{DD} | | | V |
| | I _{IH} = 5μA, 1.2V ≤ IOV _{DD} < 1.6V | 0.9 × IOV _{DD} | | | V |
| | I _{IH} = 5μA, IOV _{DD} < 1.2V | IOV _{DD} | | | V |
| V _{IL} | I _{IL} = 5 μA, IOV _{DD} > 1.6V | −0.3 | 0.3 × IOV _{DD} | | V |
| | I _{IL} = 5μA, 1.2V ≤ IOV _{DD} < 1.6V | | 0.1 × IOV _{DD} | | V |
| | I _{IL} = 5μA, IOV _{DD} < 1.2V | | 0 | | V |
| V _{OH} | I _{OH} = 2 TTL loads | 0.8 × IOV _{DD} | | | V |
| V _{OL} | I _{OL} = 2 TTL loads | | | 0.1 × IOV _{DD} | V |
| Capacitive Load | | | 10 | | pF |

(1) Applies to all DI, DO, and DIO pins shown in [Pin Configuration and Functions](#)

8.11 I²S/LJF/RJF Timing in Master Mode (see [Figure 1](#))

All specifications at 25°C, DV_{DD} = 1.8 V

| | | IOVDD=1.8V | | IOVDD=3.3V | | UNIT |
|-------------------------|--|------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| t _{d(WS)} | WCLK delay | | 30 | | 20 | ns |
| t _{d(DO-WS)} | WCLK to DOUT delay (For LJF Mode only) | | 20 | | 20 | ns |
| t _{d(DO-BCLK)} | BCLK to DOUT delay | | 22 | | 20 | ns |
| t _{s(DI)} | DIN setup | 8 | | 8 | | ns |
| t _{h(DI)} | DIN hold | 8 | | 8 | | ns |
| t _r | Rise time | | 24 | | 12 | ns |
| t _f | Fall time | | 24 | | 12 | ns |

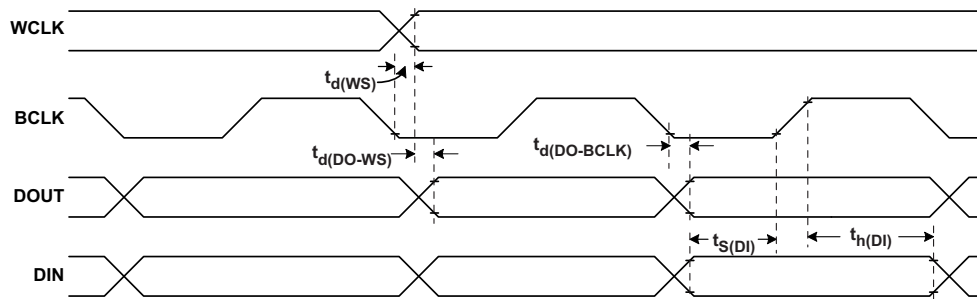


Figure 1. I²S/LJF/RJF Timing in Master Mode

8.12 I²S/LJF/RJF Timing in Slave Mode (see Figure 2)

| | | IOVDD=1.8V | | IOVDD=3.3V | | UNIT |
|------------------|--|------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| $t_{H(BCLK)}$ | BCLK high period | 35 | | 35 | | ns |
| $t_{L(BCLK)}$ | BCLK low period | 35 | | 35 | | |
| $t_{s(WS)}$ | WCLK setup | 8 | | 8 | | |
| $t_{h(WS)}$ | WCLK hold | 8 | | 8 | | |
| $t_{d(DO-WS)}$ | WCLK to DOUT delay (For LJF mode only) | | 20 | | 20 | |
| $t_{d(DO-BCLK)}$ | BCLK to DOUT delay | | 22 | | 22 | |
| $t_{s(DI)}$ | DIN setup | 8 | | 8 | | |
| $t_{h(DI)}$ | DIN hold | 8 | | 8 | | |
| t_r | Rise time | | 4 | | 4 | |
| t_f | Fall time | | 4 | | 4 | |

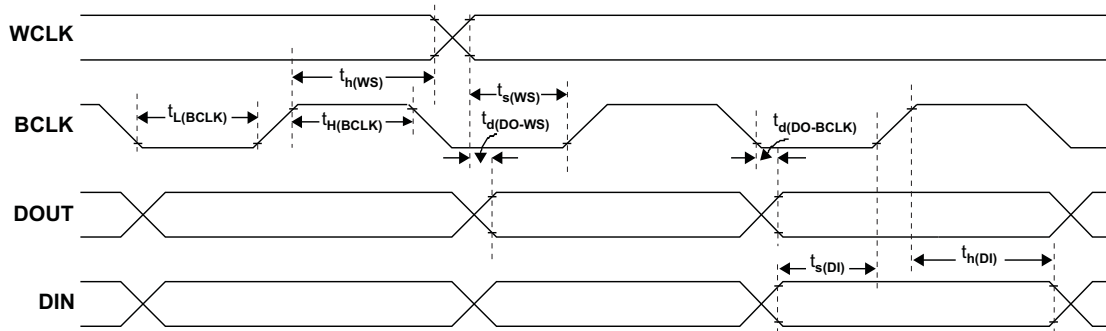


Figure 2. I²S/LJF/RJF Timing in Slave Mode

8.13 DSP Timing in Master Mode (see [Figure 3](#))

All specifications at 25°C, DVdd = 1.8 V

| | | IOVDD=1.8V | | IOVDD=3.3V | | UNIT |
|------------------|--------------------|------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| $t_{d(W)}$ | WCLK delay | | 30 | | 20 | ns |
| $t_{d(DO-BCLK)}$ | BCLK to DOUT delay | | 22 | | 20 | ns |
| $t_{s(DI)}$ | DIN setup | 8 | | 8 | | ns |
| $t_{h(DI)}$ | DIN hold | 8 | | 8 | | ns |
| t_r | Rise time | | 24 | | 12 | ns |
| t_f | Fall time | | 24 | | 12 | ns |

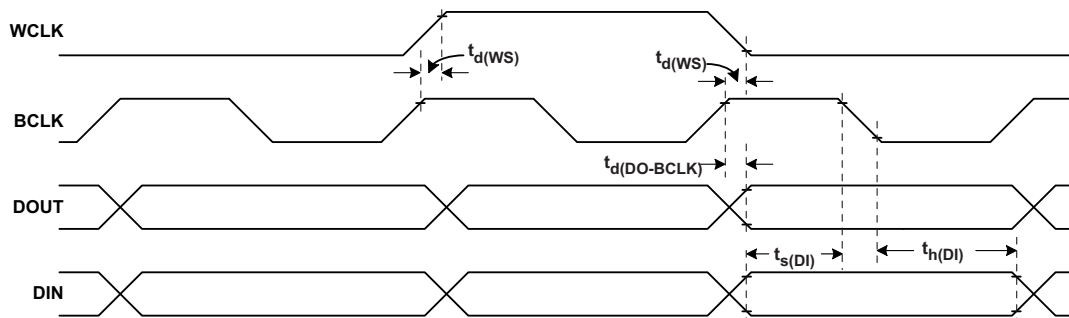


Figure 3. DSP Timing in Master Mode

8.14 DSP Timing in Slave Mode (see Figure 4)

| | | IOVDD=1.8V | | IOVDD=3.3V | | UNIT |
|------------------|--------------------|------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| $t_{H(BCLK)}$ | BCLK high period | 35 | | 35 | | ns |
| $t_{L(BCLK)}$ | BCLK low period | 35 | | 35 | | ns |
| $t_{s(WS)}$ | WCLK setup | 8 | | 8 | | ns |
| $t_{h(WS)}$ | WCLK hold | 8 | | 8 | | ns |
| $t_{d(DO-BCLK)}$ | BCLK to DOUT delay | | 22 | | 22 | ns |
| $t_{s(DI)}$ | DIN setup | 8 | | 8 | | ns |
| $t_{h(DI)}$ | DIN hold | 8 | | 8 | | ns |
| t_r | Rise time | | 4 | | 4 | ns |
| t_f | Fall time | | 4 | | 4 | ns |

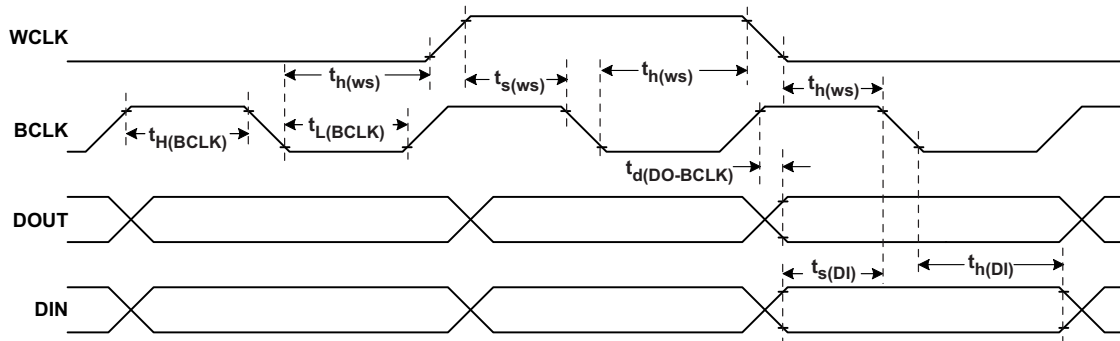


Figure 4. DSP Timing in Slave Mode

8.15 Digital Microphone PDM Timing (see [Figure 5](#))

Based on design simulation. Not tested in actual silicon.

| | | IOVDD = 1.8V | | IOVDD = 3.3V | | UNIT |
|-------|-----------|--------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| t_s | DIN setup | 20 | | 20 | | ns |
| t_h | DIN hold | 5 | | 5 | | ns |
| t_r | Rise time | | 4 | | 4 | ns |
| t_f | Fall time | | 4 | | 4 | ns |

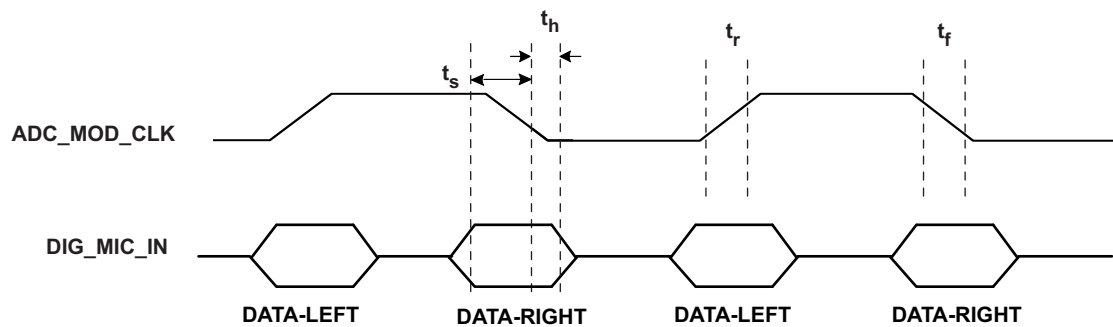


Figure 5. PDM Input Timing

8.16 I²C Interface Timing

| | | Standard-Mode | | | Fast-Mode | | | UNIT |
|---------------|--|---------------|-----|------|-------------|-----|-----|---------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| f_{SCL} | SCL clock frequency | 0 | | 100 | 0 | | 400 | kHz |
| $t_{H(STA)}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4.0 | | | 0.8 | | | μ s |
| t_{LOW} | LOW period of the SCL clock | 4.7 | | | 1.3 | | | μ s |
| t_{HIGH} | HIGH period of the SCL clock | 4.0 | | | 0.6 | | | μ s |
| $t_{SU(STA)}$ | Setup time for a repeated START condition | 4.7 | | | 0.8 | | | μ s |
| $t_{H(DAT)}$ | Data hold time: For I ² C bus devices | 0 | | 3.45 | 0 | | 0.9 | μ s |
| $t_{SU(DAT)}$ | Data set-up time | 250 | | | 100 | | | ns |
| t_r | SDA and SCL Rise Time | | | 1000 | $20+0.1C_b$ | | 300 | ns |
| t_f | SDA and SCL Fall Time | | | 300 | $20+0.1C_b$ | | 300 | ns |
| $t_{SU(STO)}$ | Set-up time for STOP condition | 4.0 | | | 0.8 | | | μ s |
| t_{BUF} | Bus free time between a STOP and START condition | 4.7 | | | 1.3 | | | μ s |
| C_b | Capacitive load for each bus line | | | 400 | | | 400 | pF |

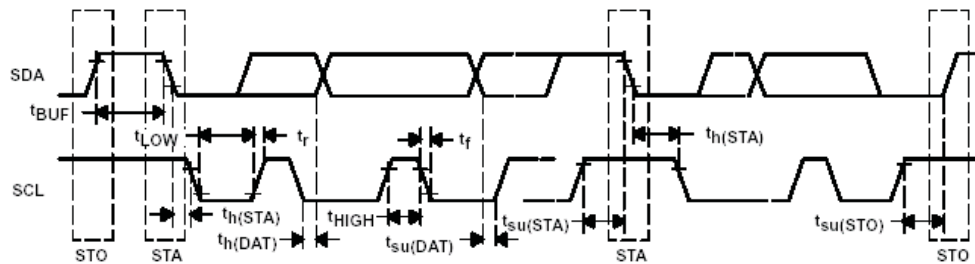


Figure 6. I²C Interface Timing

8.17 SPI Interface Timing

| | | IOVDD=1.8V | | | IOVDD=3.3V | | | UNIT |
|---------------|---------------------------|------------|-----|-----|------------|-----|-----|------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t_{sck} | SCLK Period | 100 | | | 50 | | | ns |
| t_{sckh} | SCLK Pulse width High | 50 | | | 25 | | | ns |
| t_{sckl} | SCLK Pulse width Low | 50 | | | 25 | | | ns |
| t_{lead} | Enable Lead Time | 30 | | | 20 | | | ns |
| t_{lag} | Enable Lag Time | 30 | | | 20 | | | ns |
| t_d | Sequential Transfer Delay | 40 | | | 20 | | | ns |
| t_a | Slave DOUT access time | | | 40 | | | 20 | ns |
| t_{dis} | Slave DOUT disable time | | | 40 | | | 20 | ns |
| t_{su} | DIN data setup time | 15 | | | 10 | | | ns |
| $t_{h(DIN)}$ | DIN data hold time | 15 | | | 10 | | | ns |
| $t_{v(DOUT)}$ | DOUT data valid time | | | 25 | | | 18 | ns |
| t_r | SCLK Rise Time | | | 4 | | | 4 | ns |
| t_f | SCLK Fall Time | | | 4 | | | 4 | ns |

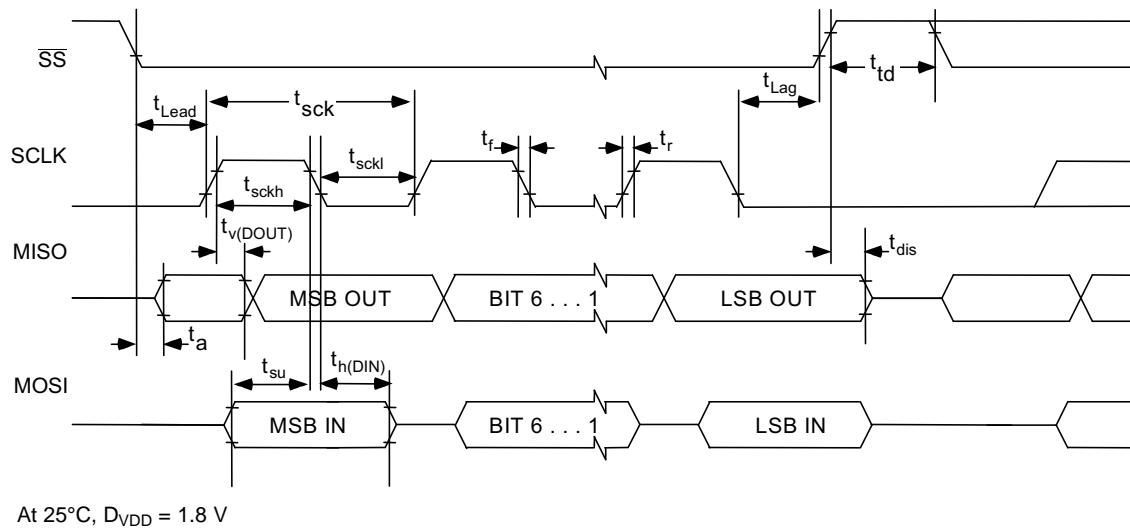


Figure 7. SPI Interface Timing Diagram

8.18 Typical Characteristics

8.18.1 Typical Performance

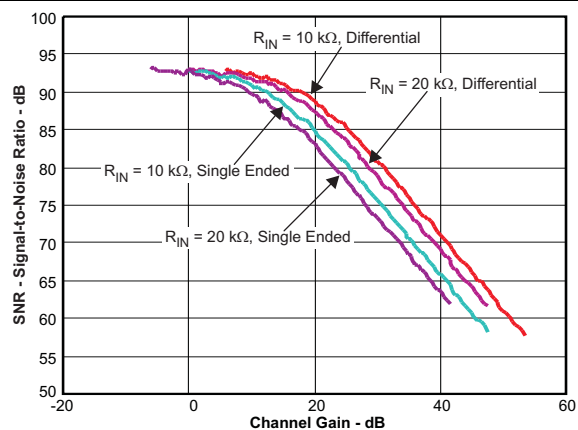


Figure 8. ADC SNR vs Channel Gain

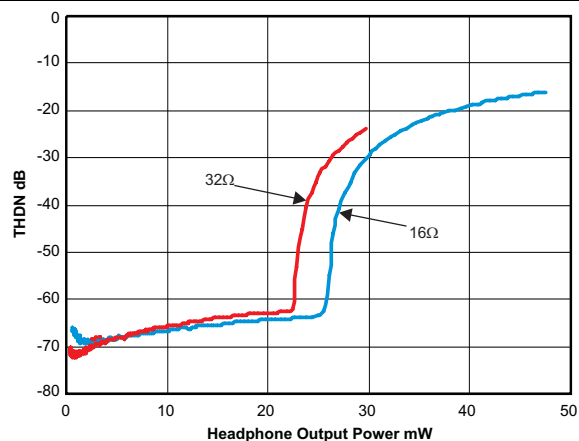


Figure 9. Total Harmonic Distortion GCHP Configuration vs Headphone Output Power

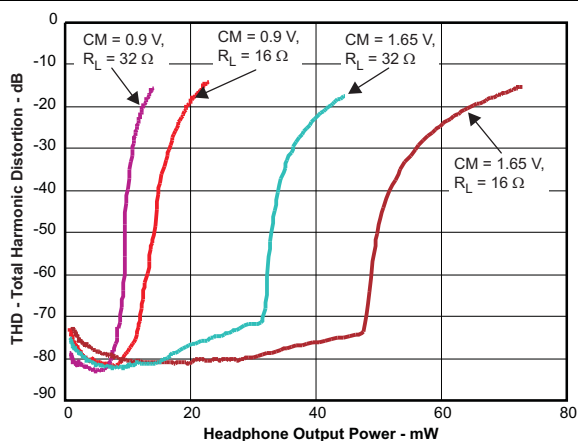


Figure 10. Total Harmonic Distortion Unipolar Configuration vs Headphone Output Power

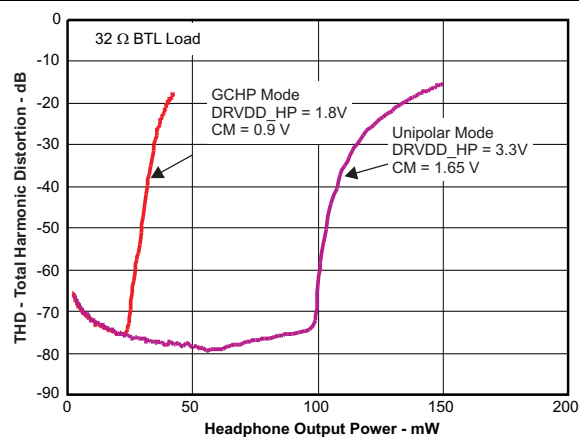


Figure 11. Total Harmonic Distortion vs Headphone Output Power

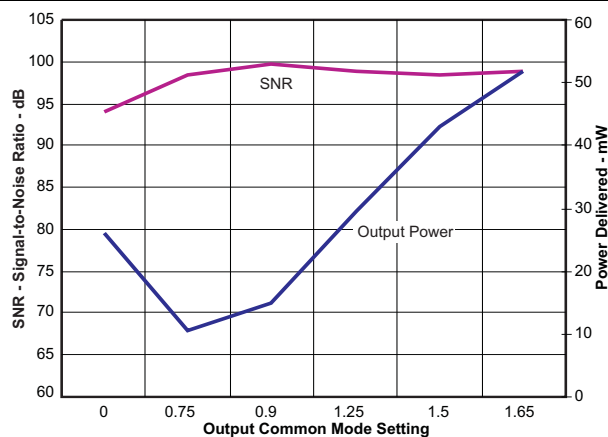


Figure 12. Headphone SNR and Output Power vs Output Common Mode Setting

8.18.2 FFT

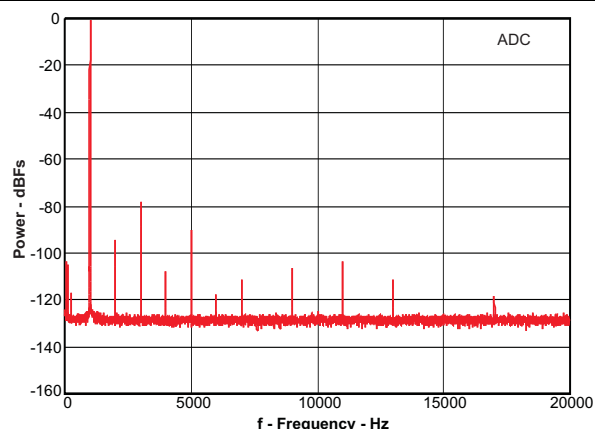


Figure 13. Single Ended Line Input to ADC FFT at -1dBr vs Frequency

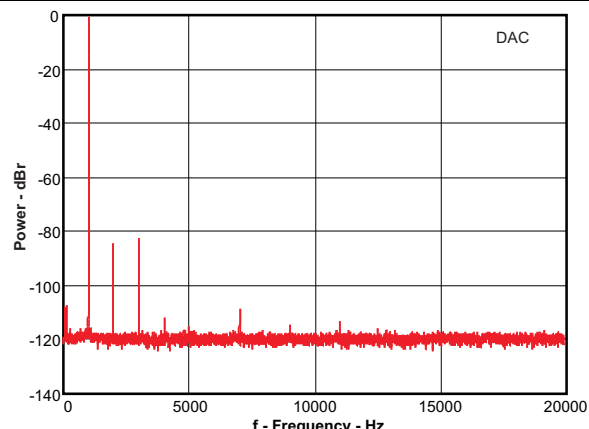


Figure 14. DAC Playback to Headphone FFT at -1dBFS (Unipolar Mode) vs Frequency

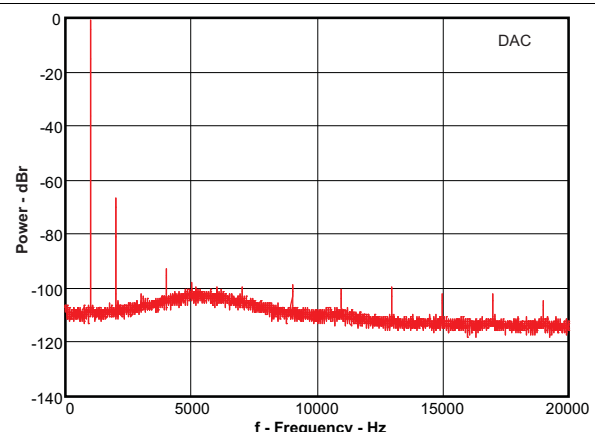


Figure 15. DAC Playback to Headphone FFT at -1dBFS (Ground-Centered Mode) vs Frequency

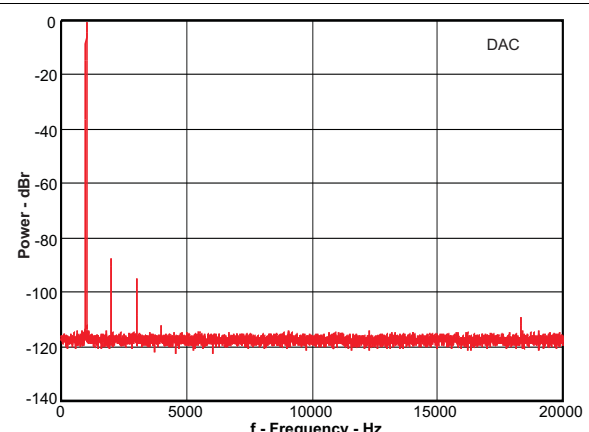


Figure 16. DAC Playback to Line-Out FFT at -1dBFS to Frequency

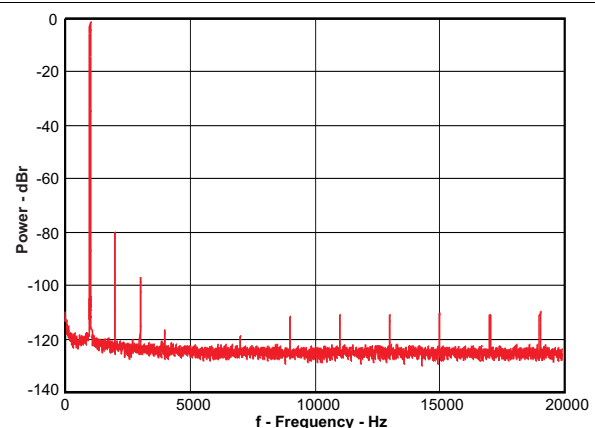


Figure 17. Line Input to Headphone FFT at 446 mVrms (Unipolar Mode) vs Frequency

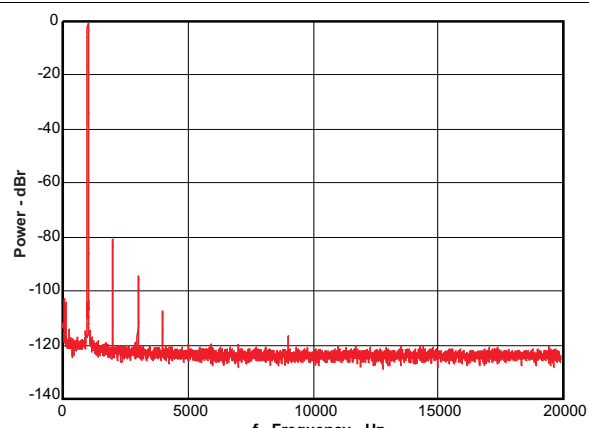


Figure 18. Line Input to Line-Out FFT at 446 mVrms (PGA Mode) vs Frequency

9 Parameter Measurement Information

All parameters are measured according to the conditions described in the [Specifications](#) section.

10 Detailed Description

10.1 Overview

The TLV320AIC3206 includes extensive register-based control of power, input/output channel configuration, gains, effects, pin-multiplexing and clocks, allowing precise targeting of the device to its application. Combined with the advanced PowerTune technology, the device covers operations from 8 kHz mono voice playback to audio stereo 192kHz DAC playback, making it ideal for portable battery-powered audio and telephony applications.

The record path of the TLV320AIC3206 covers operations from 8kHz mono to 192kHz stereo recording, and contains programmable input channel configurations covering single-ended and differential setups, as well as floating or mixing input signals. It also includes a digitally-controlled stereo microphone preamplifier and integrated microphone bias. Digital signal processing blocks can remove audible noise that may be introduced by mechanical coupling, e.g. optical zooming in a digital camera.

The integrated PowerTune technology allows the device to be tuned to an optimum power-performance trade-off. Mobile applications frequently have multiple use cases requiring very low power operation while being used in a mobile environment. When used in a docked environment power consumption typically is less of a concern, while minimizing noise is important. With PowerTune, the TLV320AIC3206 addresses both cases.

The device offers single supply operation from 1.5V-1.95V. Digital I/O voltages are supported in the range of 1.1V-3.6V.

The required internal clock of the TLV320AIC3206 can be derived from multiple sources, including the MCLK pin, the BCLK pin, the GPIO pin or the output of the internal PLL, where the input to the PLL again can be derived from the MCLK pin, the BCLK or GPIO pins. Although using the PLL ensures the availability of a suitable clock signal, PLL use is not recommended for the lowest power settings. The PLL is highly programmable and can accept available input clocks in the range of 512 kHz to 50 MHz.

10.2 Functional Block Diagram

Figure 19 shows the basic functional blocks of the device.

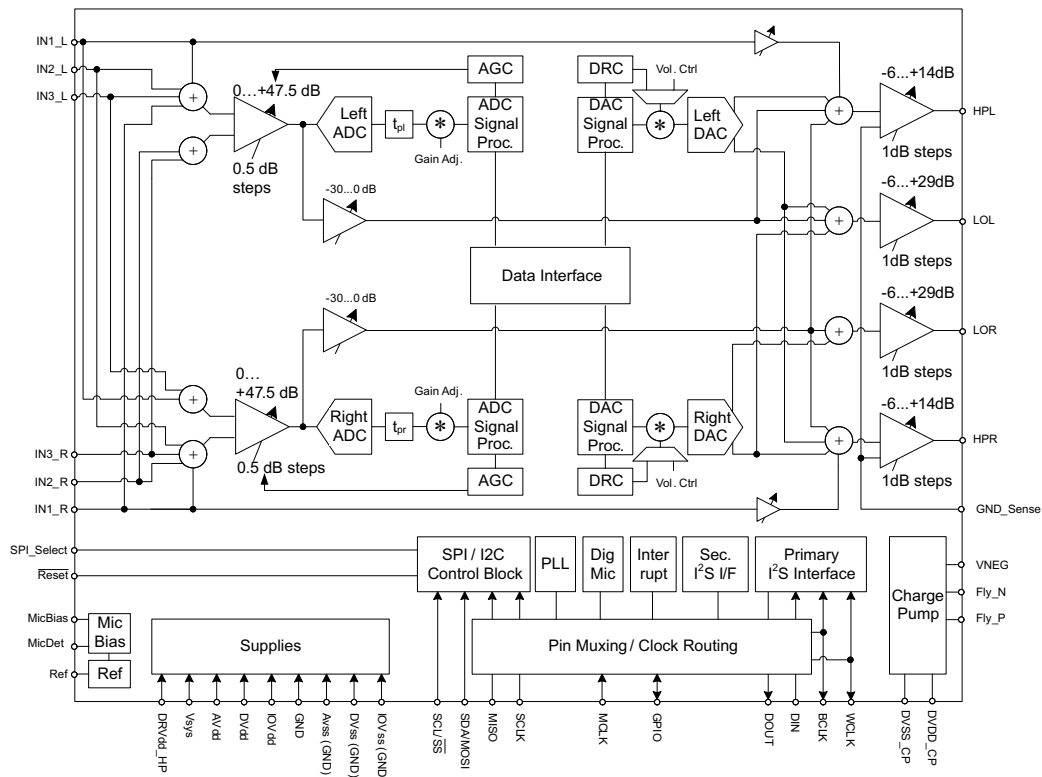


Figure 19. Block Diagram

10.3 Feature Description

10.3.1 Device Connections

10.3.1.1 Digital Pins

Only a small number of digital pins are dedicated to a single function; whenever possible, the digital pins have a default function, and also can be reprogrammed to cover alternative functions for various applications.

The fixed-function pins are Reset and the SPI_Select pin, which are HW control pins. Depending on the state of SPI_Select, the two control-bus pins SCL/SS and SDA/MOSI are configured for either I²C or SPI protocol.

Other digital IO pins can be configured for various functions via register control. An overview of available functionality is given in [Multifunction Pins](#).

Feature Description (continued)

10.3.1.1.1 Multifunction Pins

Table 1 shows the possible allocation of pins for specific functions. The PLL input, for example, can be programmed to be any of 4 pins (MCLK, BCLK, DIN, GPIO).

Table 1. Multifunction Pin Assignments

| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|----------|---------------------------------------|------------------------------------|------------------|------|-------------|--------------|-------------------------|-------------------------|------------------|
| | Pin Function | MCLK | BCLK | WCLK | DIN MFP1 | DOUT MFP2 | DMDIN/ MFP3/ SCLK | DMCLK/ MFP4/ MISO | GPIO MFP5 |
| A | PLL Input | S ⁽¹⁾ | S ⁽²⁾ | | E | | | | S ⁽³⁾ |
| B | Codec Clock Input | S ⁽¹⁾ ,D ⁽⁴⁾ | S ⁽²⁾ | | | | | | S ⁽³⁾ |
| C | I ² S BCLK input | | S,D | | | | | | |
| D | I ² S BCLK output | | E ⁽⁵⁾ | | | | | | |
| E | I ² S WCLK input | | | E, D | | | | | |
| F | I ² S WCLK output | | | E | | | | | |
| G | I ² S ADC word clock input | | | | | | E | | E |
| H | I ² S ADC WCLK out | | | | | | | E | E |
| I | I ² S DIN | | | | E, D | | | | |
| J | I ² S DOUT | | | | | E, D | | | |
| K | General Purpose Output I | | | | | E | | | |
| K | General Purpose Output II | | | | | | | E | |
| K | General Purpose Output III | | | | | | | | E |
| L | General Purpose Input I | | | | E | | | | |
| L | General Purpose Input II | | | | | | E | | |
| L | General Purpose Input III | | | | | | | | E |
| M | INT1 output | | | | | E | | E | E |
| N | INT2 output | | | | | E | | E | E |
| Q | Secondary I ² S BCLK input | | | | | | E | | E |
| R | Secondary I ² S WCLK in | | | | | | E | | E |
| S | Secondary I ² S DIN | | | | | | E | | E |
| T | Secondary I ² S DOUT | | | | | | | E | |
| U | Secondary I ² S BCLK OUT | | | | | E | | E | E |
| V | Secondary I ² S WCLK OUT | | | | | E | | E | E |
| X | Aux Clock Output | | | | | E | | E | E |

(1) S⁽¹⁾: The MCLK pin can drive the PLL and Codec Clock inputs **simultaneously**.

(2) S⁽²⁾: The BCLK pin can drive the PLL and Codec Clock and audio interface bit clock inputs **simultaneously**.

(3) S⁽³⁾: The GPIO/MFP5 pin can drive the PLL and Codec Clock inputs simultaneously.

(4) D: Default Function

(5) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin. (If GPIO/MFP5 has been allocated for General Purpose Output, it cannot be used as the INT1 output at the same time.)

10.3.1.2 Analog Pins

Analog functions can also be configured to a large degree. For minimum power consumption, analog blocks are powered down by default. The blocks can be powered up with fine granularity according to the application needs.

10.3.2 Analog Audio I/O

The analog IO path of the TLV320AIC3206 features a large set of options for signal conditioning as well as signal routing:

- 6 analog inputs which can be mixed and-or multiplexed in single-ended and-or differential configuration
- 2 programmable gain amplifiers (PGA) with a range of 0 to +47.5dB
- 2 mixer amplifiers for analog bypass

- 2 low power analog bypass channels
- Mute function
- Channel-to-channel phase adjustment
- Fast charge of ac-coupling capacitors
- Anti thump

10.3.2.1 Analog Bypass

The TLV320AIC3206 offers two analog-bypass modes. In either of the modes, an analog input signal can be routed from an analog input pin to an amplifier driving an analog output pin. Neither the ADC nor the DAC resources are required for such operation.

In analog low-power bypass mode, line-level signals can be routed directly from the analog inputs IN1_L to the left headphone amplifier (HPL) and IN1_R to HPR.

10.3.2.2 ADC Bypass Using Mixer Amplifiers

In addition to the analog low-power bypass mode, another bypass mode uses the programmable gain amplifiers of the input stage in conjunction with a mixer amplifier. With this mode, microphone-level signals can be amplified and routed to the line or headphone outputs, fully bypassing the ADC and DAC.

To enable this mode, the mixer amplifiers are powered on via software command.

10.3.2.3 Headphone Output

The stereo headphone drivers on pins HPL and HPR can drive loads with impedances down to 16Ω in single-ended DC-coupled headphone configurations. An integral charge pump generates the negative supply required to operate the headphone drivers in dc-coupled mode, where the common mode of the output signal is made equal to the ground of the headphone load using a ground-sense circuit. Operation of headphone drivers in dc-coupled (ground centered mode) eliminates the need for large dc-blocking capacitors.

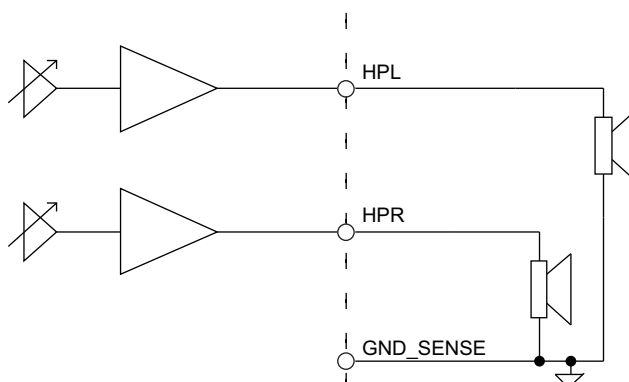


Figure 20. TLV320AIC3206 Ground-Centered Headphone Output

Alternatively the headphone amplifier can also be operated in a unipolar circuit configuration using DC blocking capacitors.

10.3.2.4 Line Outputs

The stereo line level drivers on LOL and LOR pins can drive a wide range of line level resistive impedances in the range of 600Ω to 10kΩ. The output common modes of line level drivers can be configured to equal either the analog input common-mode setting, or 1.65V. With output common-mode setting of 1.65V and DRVdd_HP supply at 3.3V the line-level drivers can drive up to 1Vrms output signal. The line-level drivers can drive out a mixed combination of DAC signal and attenuated ADC PGA signal. Signal mixing is register-programmable.

10.3.3 ADC

The TLV320AIC3206 includes a stereo audio ADC, which uses a delta-sigma modulator with a programmable oversampling ratio, followed by a digital decimation filter. The ADC supports sampling rates from 8kHz to 192kHz. In order to provide optimal system power management, the stereo recording path can be powered up one channel at a time, to support the case where only mono record capability is required.

The ADC path of the TLV320AIC3206 features a large set of options for signal conditioning as well as signal routing:

- Two ADCs
- Six analog inputs which can be mixed and-or multiplexed in single-ended and-or differential configuration
- Two programmable gain amplifiers (PGA) with a range of 0 to +47.5dB
- Two mixer amplifiers for analog bypass
- Two low power analog bypass channels
- Fine gain adjustment of digital channels with 0.1dB step size
- Digital volume control with a range of -12 to +20dB
- Mute function

In addition to the standard set of ADC features the TLV320AIC3206 also offers the following special functions:

- Channel-to-channel phase adjustment
- Fast charge of ac-coupling capacitors
- Anti thump
- Adaptive filter mode

10.3.3.1 ADC Processing

The TLV320AIC3206 ADC channel includes a built-in digital decimation filter to process the oversampled data from the to generate digital data at Nyquist sampling rate with high dynamic range. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay and sampling rate.

10.3.3.1.1 ADC Processing Blocks

The TLV320AIC3206 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

The choice between these processing blocks is part of the PowerTune strategy to balance power conservation and signal-processing flexibility. Less signal-processing capability reduces the power consumed by the device. [Table 2](#) gives an overview of the available processing blocks and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- Variable-tap FIR filter

The processing blocks are tuned for common cases and can achieve high anti-alias filtering or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first order IIR, BiQuad and FIR filters have fully user-programmable coefficients. The Resource Class Column (RC) gives an approximate indication of power consumption.

Table 2. ADC Processing Blocks

| Processing Blocks | Channel | Decimation Filter | 1st Order IIR Available | Number BiQuads | FIR | Required AOSR Value | Resource Class |
|-----------------------|---------|-------------------|-------------------------|----------------|--------|---------------------|----------------|
| PRB_R1 ⁽¹⁾ | Stereo | A | Yes | 0 | No | 128,64 | 6 |
| PRB_R2 | Stereo | A | Yes | 5 | No | 128,64 | 8 |
| PRB_R3 | Stereo | A | Yes | 0 | 25-Tap | 128,64 | 8 |
| PRB_R4 | Right | A | Yes | 0 | No | 128,64 | 3 |
| PRB_R5 | Right | A | Yes | 5 | No | 128,64 | 4 |
| PRB_R6 | Right | A | Yes | 0 | 25-Tap | 128,64 | 4 |
| PRB_R7 | Stereo | B | Yes | 0 | No | 64 | 3 |
| PRB_R8 | Stereo | B | Yes | 3 | No | 64 | 4 |
| PRB_R9 | Stereo | B | Yes | 0 | 20-Tap | 64 | 4 |
| PRB_R10 | Right | B | Yes | 0 | No | 64 | 2 |
| PRB_R11 | Right | B | Yes | 3 | No | 64 | 2 |
| PRB_R12 | Right | B | Yes | 0 | 20-Tap | 64 | 2 |
| PRB_R13 | Stereo | C | Yes | 0 | No | 32 | 3 |
| PRB_R14 | Stereo | C | Yes | 5 | No | 32 | 4 |
| PRB_R15 | Stereo | C | Yes | 0 | 25-Tap | 32 | 4 |
| PRB_R16 | Right | C | Yes | 0 | No | 32 | 2 |
| PRB_R17 | Right | C | Yes | 5 | No | 32 | 2 |
| PRB_R18 | Right | C | Yes | 0 | 25-Tap | 32 | 2 |

(1) Default

For more detailed information see the TLV320AIC3206 Application Reference Guide, [SLAA463](#).

10.3.4 DAC

The TLV320AIC3206 includes a stereo audio DAC supporting data rates from 8kHz to 192kHz. Each channel of the stereo audio DAC consists of a signal-processing engine with fixed processing blocks, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20kHz. To handle multiple input rates and optimize power dissipation and performance, the TLV320AIC3206 allows the system designer to program the oversampling rates over a wide range from 1 to 1024. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The TLV320AIC3206 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the sigma-delta modulator. The interpolation filter can be chosen from three different types depending on required frequency response, group delay and sampling rate.

The DAC path of the TLV320AIC3206 features many options for signal conditioning and signal routing:

- 2 headphone amplifiers
 - Ground-centered, bipolar operation or unipolar operation
 - Usable in single-ended or differential mode
 - Analog volume setting with a range of -6 to +14dB
- 2 line-out amplifiers
 - Usable in single-ended or differential mode
 - Analog volume setting with a range of -6 to +29dB
- Digital volume control with a range of -63.5 to +24dB
- Mute function
- Dynamic range compression (DRC)

In addition to the standard set of DAC features the TLV320AIC3206 also offers the following special features:

- Built in sine wave generation (beep generator)
- Digital auto mute
- Adaptive filter mode

10.3.4.1 DAC Processing Blocks — Overview

Table 3. Overview – DAC Predefined Processing Blocks

| Processing Block No. | Interpolation Filter | Channel | 1st Order IIR Available | Num. of Biquads | DRC | 3D | Beep Generator |
|-----------------------|----------------------|---------|-------------------------|-----------------|-----|-----|----------------|
| PRB_P1 ⁽¹⁾ | A | Stereo | No | 3 | No | No | No |
| PRB_P2 | A | Stereo | Yes | 6 | Yes | No | No |
| PRB_P3 | A | Stereo | Yes | 6 | No | No | No |
| PRB_P4 | A | Left | No | 3 | No | No | No |
| PRB_P5 | A | Left | Yes | 6 | Yes | No | No |
| PRB_P6 | A | Left | Yes | 6 | No | No | No |
| PRB_P7 | B | Stereo | Yes | 0 | No | No | No |
| PRB_P8 | B | Stereo | No | 4 | Yes | No | No |
| PRB_P9 | B | Stereo | No | 4 | No | No | No |
| PRB_P10 | B | Stereo | Yes | 6 | Yes | No | No |
| PRB_P11 | B | Stereo | Yes | 6 | No | No | No |
| PRB_P12 | B | Left | Yes | 0 | No | No | No |
| PRB_P13 | B | Left | No | 4 | Yes | No | No |
| PRB_P14 | B | Left | No | 4 | No | No | No |
| PRB_P15 | B | Left | Yes | 6 | Yes | No | No |
| PRB_P16 | B | Left | Yes | 6 | No | No | No |
| PRB_P17 | C | Stereo | Yes | 0 | No | No | No |
| PRB_P18 | C | Stereo | Yes | 4 | Yes | No | No |
| PRB_P19 | C | Stereo | Yes | 4 | No | No | No |
| PRB_P20 | C | Left | Yes | 0 | No | No | No |
| PRB_P21 | C | Left | Yes | 4 | Yes | No | No |
| PRB_P22 | C | Left | Yes | 4 | No | No | No |
| PRB_P23 | A | Stereo | No | 2 | No | Yes | No |
| PRB_P24 | A | Stereo | Yes | 5 | Yes | Yes | No |
| PRB_P25 | A | Stereo | Yes | 5 | Yes | Yes | Yes |

(1) Default

For more detailed information see the TLV320AIC3206 Application Reference Guide, [SLAA463](#).

10.3.5 PowerTune

The TLV320AIC3206 features PowerTune, a mechanism to balance power-versus-performance trade-offs at the time of device configuration. The device can be tuned to minimize power dissipation, to maximize performance, or to an operating point between the two extremes to best fit the application. The TLV320AIC3206 PowerTune modes are called PTM_R1 to PTM_R4 for the recording (ADC) path and PTM_P1 to PTM_P4 for the playback (DAC) path.

For more detailed information see the TLV320AIC3206 Application Reference Guide, [SLAA463](#).

10.3.6 Digital Audio IO Interface

Audio data flows between the host processor and the TLV320AIC3206 on the digital audio data serial interface, or audio bus. This very flexible bus includes left or right-justified data options, support for I²S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master-slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

The audio bus of the TLV320AIC3206 can be configured for left or right-justified, I²S, DSP, or TDM modes of operation, where communication with standard PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits by configuring Page 0, Register 27, D(5:4). In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies.

The bit clock is used to clock in and clock out the digital audio data across the serial bus. When in Master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider in Page 0, Register 30. The number of bit-clock pulses in a frame may need adjustment to accommodate various word lengths, and to support the case when multiple TLV320AIC3206s may share the same audio bus.

The TLV320AIC3206 also includes a feature to offset the position of start of data transfer with respect to the word-clock. Control the offset in terms of number of bit-clocks by programming Page 0, Register 28.

The TLV320AIC3206 also has the feature to invert the polarity of the bit-clock used to transfer the audio data as compared to the default clock polarity used. This feature can be used independently of the mode of audio interface chosen. Page 0, Register 29, D(3) configures bit clock polarity.

The TLV320AIC3206 further includes programmability (Page 0, Register 27, D(0)) to place the DOUT line into a hi-Z (3-state) condition during all bit clocks when valid data is not being sent. By combining this capability with the ability to program at what bit clock in a frame the audio data begins, time-division multiplexing (TDM) can be accomplished, enabling the use of multiple codecs on a single audio serial data bus. When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface are put into a hi-Z output condition.

By default when the word-clocks and bit-clocks are generated by the TLV320AIC3206, these clocks are active only when the codec (ADC, DAC or both) are powered up within the device. This intermittent clock operation reduces power consumption. However, it also supports a feature when both the word clocks and bit-clocks can be active even when the codec in the device is powered down. This continuous clock feature is useful when using the TDM mode with multiple codecs on the same bus, or when word-clock or bit-clocks are used in the system as general-purpose clocks.

10.3.7 Clock Generation and PLL

The TLV320AIC3206 supports a wide range of options for generating clocks for the ADC and DAC sections as well as interface and other control blocks. The clocks for ADC and DAC require a source reference clock. This clock can be provided on variety of device pins such as MCLK, BCLK or GPI pins. The CODEC_CLKIN can then be routed through highly-flexible clock dividers to generate the various clocks required for the ADC and DAC sections. In the event that the desired audio clocks cannot be generated from the reference clocks on MCLK, BCLK or GPIO, the TLV320AIC3206 also provides the option of using the on-chip PLL which supports a wide range of fractional multiplication values to generate the required clocks. Starting from CODEC_CLKIN the TLV320AIC3206 provides several programmable clock dividers to help achieve a variety of sampling rates for ADC, DAC and clocks for the processing block.

To minimize power consumption, the system ideally provides a master clock that is a suitable integer multiple of the desired sampling frequencies. In such cases, internal dividers can be programmed to set up the required internal clock signals at very low power consumption. For cases where such master clocks are not available, the built-in PLL can be used to generate a clock signal that serves as an internal master clock. In fact, this master clock can also be routed to an output pin and may be used elsewhere in the system. The clock system is flexible enough that it even allows the internal clocks to be derived directly from an external clock source, while the PLL is used to generate some other clock that is only used outside the TLV320AIC3206.

For more detailed information see the TLV320AIC3206 Application Reference Guide, [SLAA463](#).

10.3.8 Control Interfaces

The TLV320AIC3206 control interface supports SPI or I²C communication protocols, with the protocol selectable using the SPI_SELECT pin. For SPI, SPI_SELECT should be tied high; for I²C, SPI_SELECT should be tied low. Changing the state of SPI_SELECT during device operation is not recommended.

10.3.8.1 I²C Control

The TLV320AIC3206 supports the I²C control protocol, and will respond to the I²C address of 0011000. I²C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I²C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This circuit prevents two devices from conflicting; if two devices drive the bus simultaneously, there is no driver contention.

10.3.8.2 SPI Control

In the SPI control mode, the TLV320AIC3206 uses the pins SCL/ \overline{SS} as \overline{SS} , SCLK as SCLK, MISO as MISO, SDA/MOSI as MOSI; a standard SPI port with clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave devices (such as the TLV320AIC3206) depend on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register.

For more detailed information see the TLV320AIC3206 Application Reference Guide, [SLAA463](#).

10.4 Device Functional Modes

The following special functions are available to support advanced system requirements:

- Headset detection
- Interrupt generation
- Flexible pin multiplexing

For more detailed information see the TLV320AIC3206 Application Reference Guide, [SLAA463](#).

10.5 Register Map

10.5.1 Register Map Summary

Table 4. Summary of Register Map

| Decimal | | Hex | | DESCRIPTION |
|----------|----------|----------|-----------|---|
| PAGE NO. | REG. NO. | PAGE NO. | REG. NO. | |
| 0 | 0 | 0x00 | 0x00 | Page Select Register |
| 0 | 1 | 0x00 | 0x01 | Software Reset Register |
| 0 | 2 | 0x00 | 0x02 | Reserved Register |
| 0 | 3 | 0x00 | 0x03 | Reserved Register |
| 0 | 4 | 0x00 | 0x04 | Clock Setting Register 1, Multiplexers |
| 0 | 5 | 0x00 | 0x05 | Clock Setting Register 2, PLL P&R Values |
| 0 | 6 | 0x00 | 0x06 | Clock Setting Register 3, PLL J Values |
| 0 | 7 | 0x00 | 0x07 | Clock Setting Register 4, PLL D Values (MSB) |
| 0 | 8 | 0x00 | 0x08 | Clock Setting Register 5, PLL D Values (LSB) |
| 0 | 9-10 | 0x00 | 0x09-0x0A | Reserved Register |
| 0 | 11 | 0x00 | 0x0B | Clock Setting Register 6, NDAC Values |
| 0 | 12 | 0x00 | 0x0C | Clock Setting Register 7, MDAC Values |
| 0 | 13 | 0x00 | 0x0D | DAC OSR Setting Register 1, MSB Value |
| 0 | 14 | 0x00 | 0x0E | DAC OSR Setting Register 2, LSB Value |
| 0 | 15 | 0x00 | 0x0F | Reserved Register |
| 0 | 16 | 0x00 | 0x10 | Reserved Register |
| 0 | 17 | 0x00 | 0x11 | Reserved Register |
| 0 | 18 | 0x00 | 0x12 | Clock Setting Register 8, NADC Values |
| 0 | 19 | 0x00 | 0x13 | Clock Setting Register 9, MADC Values |
| 0 | 20 | 0x00 | 0x14 | ADC Oversampling (AOSR) Register |
| 0 | 21 | 0x00 | 0x15 | Reserved Register |
| 0 | 22 | 0x00 | 0x16 | Reserved Register |
| 0 | 23 | 0x00 | 0x17 | Reserved Register |
| 0 | 24 | 0x00 | 0x18 | Reserved Register |
| 0 | 25 | 0x00 | 0x19 | Clock Setting Register 10, Multiplexers |
| 0 | 26 | 0x00 | 0x1A | Clock Setting Register 11, CLKOUT M divider value |
| 0 | 27 | 0x00 | 0x1B | Audio Interface Setting Register 1 |
| 0 | 28 | 0x00 | 0x1C | Audio Interface Setting Register 2, Data offset setting |
| 0 | 29 | 0x00 | 0x1D | Audio Interface Setting Register 3 |
| 0 | 30 | 0x00 | 0x1E | Clock Setting Register 12, BCLK N Divider |
| 0 | 31 | 0x00 | 0x1F | Audio Interface Setting Register 4, Secondary Audio Interface |
| 0 | 32 | 0x00 | 0x20 | Audio Interface Setting Register 5 |
| 0 | 33 | 0x00 | 0x21 | Audio Interface Setting Register 6 |
| 0 | 34 | 0x00 | 0x22 | Digital Interface Misc. Setting Register |
| 0 | 35 | 0x00 | 0x23 | Reserved Register |
| 0 | 36 | 0x00 | 0x24 | ADC Flag Register |
| 0 | 37 | 0x00 | 0x25 | DAC Flag Register 1 |
| 0 | 38 | 0x00 | 0x26 | DAC Flag Register 2 |
| 0 | 39-41 | 0x00 | 0x27-0x29 | Reserved Register |
| 0 | 42 | 0x00 | 0x2A | Sticky Flag Register 1 |
| 0 | 43 | 0x00 | 0x2B | Interrupt Flag Register 1 |
| 0 | 44 | 0x00 | 0x2C | Sticky Flag Register 2 |
| 0 | 45 | 0x00 | 0x2D | Sticky Flag Register 3 |

Register Map (continued)

Table 4. Summary of Register Map (continued)

| Decimal | | Hex | | DESCRIPTION |
|----------|----------|----------|-----------|---|
| PAGE NO. | REG. NO. | PAGE NO. | REG. NO. | |
| 0 | 46 | 0x00 | 0x2E | Interrupt Flag Register 2 |
| 0 | 47 | 0x00 | 0x2F | Interrupt Flag Register 3 |
| 0 | 48 | 0x00 | 0x30 | INT1 Interrupt Control Register |
| 0 | 49 | 0x00 | 0x31 | INT2 Interrupt Control Register |
| 0 | 50-51 | 0x00 | 0x32-0x33 | Reserved Register |
| 0 | 52 | 0x00 | 0x34 | GPIO/MFP5 Control Register |
| 0 | 53 | 0x00 | 0x35 | DOOUT/MFP2 Function Control Register |
| 0 | 54 | 0x00 | 0x36 | DIN/MFP1 Function Control Register |
| 0 | 55 | 0x00 | 0x37 | MISO/MFP4 Function Control Register |
| 0 | 56 | 0x00 | 0x38 | SCLK/MFP3 Function Control Register |
| 0 | 57-59 | 0x00 | 0x39-0x3B | Reserved Registers |
| 0 | 60 | 0x00 | 0x3C | DAC Signal Processing Block Control Register |
| 0 | 61 | 0x00 | 0x3D | ADC Signal Processing Block Control Register |
| 0 | 62 | 0x00 | 0x3E | Reserved Register |
| 0 | 63 | 0x00 | 0x3F | DAC Channel Setup Register 1 |
| 0 | 64 | 0x00 | 0x40 | DAC Channel Setup Register 2 |
| 0 | 65 | 0x00 | 0x41 | Left DAC Channel Digital Volume Control Register |
| 0 | 66 | 0x00 | 0x42 | Right DAC Channel Digital Volume Control Register |
| 0 | 67 | 0x00 | 0x43 | Headset Detection Configuration Register |
| 0 | 68 | 0x00 | 0x44 | DRC Control Register 1 |
| 0 | 69 | 0x00 | 0x45 | DRC Control Register 2 |
| 0 | 70 | 0x00 | 0x46 | DRC Control Register 3 |
| 0 | 71 | 0x00 | 0x47 | Beep Generator Register 1 |
| 0 | 72 | 0x00 | 0x48 | Beep Generator Register 2 |
| 0 | 73 | 0x00 | 0x49 | Beep Generator Register 3 |
| 0 | 74 | 0x00 | 0x4A | Beep Generator Register 4 |
| 0 | 75 | 0x00 | 0x4B | Beep Generator Register 5 |
| 0 | 76 | 0x00 | 0x4C | Beep Generator Register 6 |
| 0 | 77 | 0x00 | 0x4D | Beep Generator Register 7 |
| 0 | 78 | 0x00 | 0x4E | Beep Generator Register 8 |
| 0 | 79 | 0x00 | 0x4F | Beep Generator Register 9 |
| 0 | 80 | 0x00 | 0x50 | Reserved Register |
| 0 | 81 | 0x00 | 0x51 | ADC Channel Setup Register |
| 0 | 82 | 0x00 | 0x52 | ADC Fine Gain Adjust Register |
| 0 | 83 | 0x00 | 0x53 | Left ADC Channel Volume Control Register |
| 0 | 84 | 0x00 | 0x54 | Right ADC Channel Volume Control Register |
| 0 | 85 | 0x00 | 0x55 | ADC Phase Adjust Register |
| 0 | 86 | 0x00 | 0x56 | Left Channel AGC Control Register 1 |
| 0 | 87 | 0x00 | 0x57 | Left Channel AGC Control Register 2 |
| 0 | 88 | 0x00 | 0x58 | Left Channel AGC Control Register 3 |
| 0 | 89 | 0x00 | 0x59 | Left Channel AGC Control Register 4 |
| 0 | 90 | 0x00 | 0x5A | Left Channel AGC Control Register 5 |
| 0 | 91 | 0x00 | 0x5B | Left Channel AGC Control Register 6 |
| 0 | 92 | 0x00 | 0x5C | Left Channel AGC Control Register 7 |
| 0 | 93 | 0x00 | 0x5D | Left Channel AGC Control Register 8 |

Register Map (continued)

Table 4. Summary of Register Map (continued)

| Decimal | | Hex | | DESCRIPTION |
|----------|----------|----------|-----------|--|
| PAGE NO. | REG. NO. | PAGE NO. | REG. NO. | |
| 0 | 94 | 0x00 | 0x5E | Right Channel AGC Control Register 1 |
| 0 | 95 | 0x00 | 0x5F | Right Channel AGC Control Register 2 |
| 0 | 96 | 0x00 | 0x60 | Right Channel AGC Control Register 3 |
| 0 | 97 | 0x00 | 0x61 | Right Channel AGC Control Register 4 |
| 0 | 98 | 0x00 | 0x62 | Right Channel AGC Control Register 5 |
| 0 | 99 | 0x00 | 0x63 | Right Channel AGC Control Register 6 |
| 0 | 100 | 0x00 | 0x64 | Right Channel AGC Control Register 7 |
| 0 | 101 | 0x00 | 0x65 | Right Channel AGC Control Register 8 |
| 0 | 102 | 0x00 | 0x66 | DC Measurement Register 1 |
| 0 | 103 | 0x00 | 0x67 | DC Measurement Register 2 |
| 0 | 104 | 0x00 | 0x68 | Left Channel DC Measurement Output Register 1 |
| 0 | 105 | 0x00 | 0x69 | Left Channel DC Measurement Output Register 2 |
| 0 | 106 | 0x00 | 0x6A | Left Channel DC Measurement Output Register 3 |
| 0 | 107 | 0x00 | 0x6B | Right Channel DC Measurement Output Register 1 |
| 0 | 108 | 0x00 | 0x6C | Right Channel DC Measurement Output Register 2 |
| 0 | 109 | 0x00 | 0x6D | Right Channel DC Measurement Output Register 3 |
| 0 | 110-127 | 0x00 | 0x6E-0x7F | Reserved Register |
| 1 | 0 | 0x01 | 0x00 | Page Select Register |
| 1 | 1 | 0x01 | 0x01 | Power Configuration Register 1 |
| 1 | 2 | 0x01 | 0x02 | Power Configuration Register 2 |
| 1 | 3 | 0x01 | 0x03 | Playback Configuration Register 1 |
| 1 | 4 | 0x01 | 0x04 | Playback Configuration Register 2 |
| 1 | 5-8 | 0x01 | 0x05-0x08 | Reserved Register |
| 1 | 9 | 0x01 | 0x09 | Output Driver Power Control Register |
| 1 | 10 | 0x01 | 0x0A | Common Mode Control Register |
| 1 | 11 | 0x01 | 0x0B | Over Current Protection Configuration Register |
| 1 | 12 | 0x01 | 0x0C | HPL Routing Selection Register |
| 1 | 13 | 0x01 | 0x0D | HPR Routing Selection Register |
| 1 | 14 | 0x01 | 0x0E | LOL Routing Selection Register |
| 1 | 15 | 0x01 | 0x0F | LOR Routing Selection Register |
| 1 | 16 | 0x01 | 0x10 | HPL Driver Gain Setting Register |
| 1 | 17 | 0x01 | 0x11 | HPR Driver Gain Setting Register |
| 1 | 18 | 0x01 | 0x12 | LOL Driver Gain Setting Register |
| 1 | 19 | 0x01 | 0x13 | LOR Driver Gain Setting Register |
| 1 | 20 | 0x01 | 0x14 | Headphone Driver Startup Control Register |
| 1 | 21 | 0x01 | 0x15 | Reserved Register |
| 1 | 22 | 0x01 | 0x16 | IN1L to HPL Volume Control Register |
| 1 | 23 | 0x01 | 0x17 | IN1R to HPR Volume Control Register |
| 1 | 24 | 0x01 | 0x18 | Mixer Amplifier Left Volume Control Register |
| 1 | 25 | 0x01 | 0x19 | Mixer Amplifier Right Volume Control Register |
| 1 | 26-50 | 0x01 | 0x1A-0x32 | Reserved Register |
| 1 | 51 | 0x01 | 0x33 | MICBIAS Configuration Register |
| 1 | 52 | 0x01 | 0x34 | Left MICPGA Positive Terminal Input Routing Configuration Register |
| 1 | 53 | 0x01 | 0x35 | Reserved Register |
| 1 | 54 | 0x01 | 0x36 | Left MICPGA Negative Terminal Input Routing Configuration Register |

Register Map (continued)

Table 4. Summary of Register Map (continued)

| Decimal | | Hex | | DESCRIPTION |
|----------|----------|-----------|-----------|---|
| PAGE NO. | REG. NO. | PAGE NO. | REG. NO. | |
| 1 | 55 | 0x01 | 0x37 | Right MICPGA Positive Terminal Input Routing Configuration Register |
| 1 | 56 | 0x01 | 0x38 | Reserved Register |
| 1 | 57 | 0x01 | 0x39 | Right MICPGA Negative Terminal Input Routing Configuration Register |
| 1 | 58 | 0x01 | 0x3A | Floating Input Configuration Register |
| 1 | 59 | 0x01 | 0x3B | Left MICPGA Volume Control Register |
| 1 | 60 | 0x01 | 0x3C | Right MICPGA Volume Control Register |
| 1 | 61 | 0x01 | 0x3D | ADC Power Tune Configuration Register |
| 1 | 62 | 0x01 | 0x3E | ADC Analog Volume Control Flag Register |
| 1 | 63 | 0x01 | 0x3F | DAC Analog Gain Control Flag Register |
| 1 | 64-70 | 0x01 | 0x40-0x46 | Reserved Register |
| 1 | 71 | 0x01 | 0x47 | Analog Input Quick Charging Configuration Register |
| 1 | 72-122 | 0x01 | 0x48-0x7A | Reserved Register |
| 1 | 123 | 0x01 | 0x7B | Reference Power-up Configuration Register |
| 1 | 124 | 0x01 | 0x7C | Charge Pump Control |
| 1 | 125 | 0x01 | 0x7D | Headphone Driver Configuration |
| 1 | 126-127 | 0x01 | 0x7E-0x7F | Reserved Register |
| 8 | 0 | 0x08 | 0x00 | Page Select Register |
| 8 | 1 | 0x08 | 0x01 | ADC Adaptive Filter Configuration Register |
| 8 | 2-7 | 0x08 | 0x02-0x07 | Reserved |
| 8 | 8-127 | 0x08 | 0x08-0x7F | ADC Coefficients Buffer-A C(0:29) |
| 9-16 | 0 | 0x09-0x10 | 0x00 | Page Select Register |
| 9-16 | 1-7 | 0x09-0x10 | 0x01-0x07 | Reserved |
| 9-16 | 8-127 | 0x09-0x10 | 0x08-0x7F | ADC Coefficients Buffer-A C(30:255) |
| 26-34 | 0 | 0x1A-0x22 | 0x00 | Page Select Register |
| 26-34 | 1-7 | 0x1A-0x22 | 0x01-0x07 | Reserved. |
| 26-34 | 8-127 | 0x1A-0x22 | 0x08-0x7F | ADC Coefficients Buffer-B C(0:255) |
| 44 | 0 | 0x2C | 0x00 | Page Select Register |
| 44 | 1 | 0x2C | 0x01 | DAC Adaptive Filter Configuration Register |
| 44 | 2-7 | 0x2C | 0x02-0x07 | Reserved |
| 44 | 8-127 | 0x2C | 0x08-0x7F | DAC Coefficients Buffer-A C(0:29) |
| 45-52 | 0 | 0x2D-0x34 | 0x00 | Page Select Register |
| 45-52 | 1-7 | 0x2D-0x34 | 0x01-0x07 | Reserved. |
| 45-52 | 8-127 | 0x2D-0x34 | 0x08-0x7F | DAC Coefficients Buffer-A C(30:255) |
| 62-70 | 0 | 0x3E-0x46 | 0x00 | Page Select Register |
| 62-70 | 1-7 | 0x3E-0x46 | 0x01-0x07 | Reserved. |
| 62-70 | 8-127 | 0x3E-0x46 | 0x08-0x7F | DAC Coefficients Buffer-B C(0:255) |

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The TLV320AIC3206 is a highly integrated stereo audio codec with flexible digital audio interface options. It enables many different types of audio platforms having a need for stereo audio record and playback and needing to interface with other devices in the system over a digital audio interface.

11.2 Typical Application

Figure 21 shows a typical circuit configuration for a system using the TLV320AIC3206.

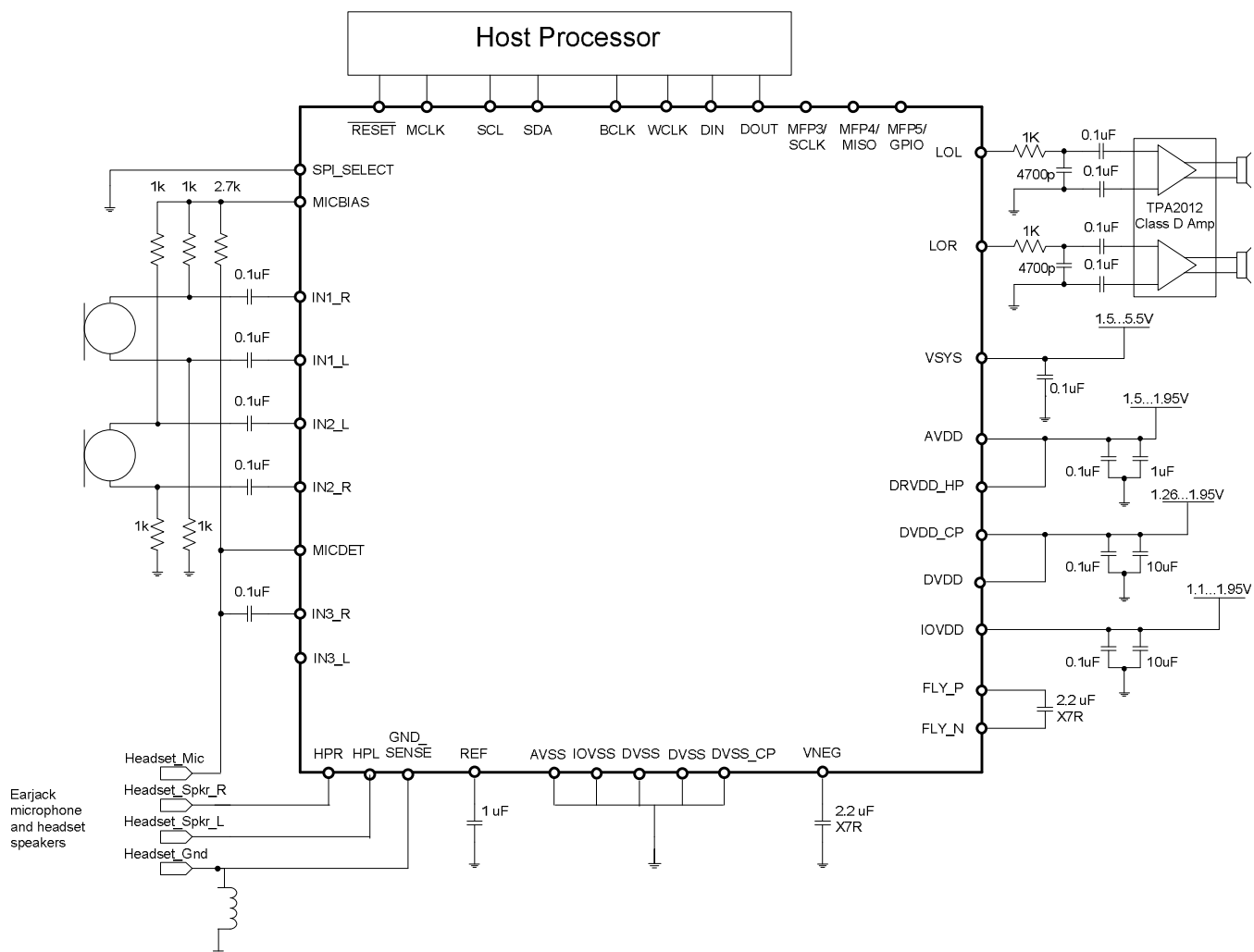


Figure 21. Typical Circuit Configuration

Typical Application (continued)

11.2.1 Design Requirements

11.2.1.1 Charge Pump Flying and Holding Capacitor

The TLV320AIC3206 features a built in charge-pump to generate a negative supply rail, VNEG from DVDD_CP. This negative voltage is used by the headphone amplifier to enable driving the output signal biased around ground potential. For proper operation of the charge pump and headphone amplifier, it is recommended that the flying capacitor connected between FLY_P and FLY_N terminals and the holding capacitor connected between VNEG and ground be of X7R type. It is recommended to use 2.2µF as capacitor values. Failure to use X7R type capacitor can result in degraded performance of charge pump and headphone amplifier.

11.2.1.2 Reference Filtering Capacitor

The TLV320AIC3206 has a built-in bandgap used to generate reference voltages and currents for the device. To achieve high SNR, the reference voltage on REF should be filtered using a 10-µF capacitor from REF terminal to ground.

11.2.1.3 MICBIAS

The TLV320AIC3206 has a built-in bias voltage output for biasing of microphones. No intentional capacitors should be connected directly to the MICBIAS output for filtering.

11.2.2 Detailed Design Procedures

11.2.2.1 Analog Input Connection

The analog inputs to TLV320AIC3206 should be ac-coupled to the device terminals to allow decoupling of signal source's common mode voltage with that of TLV320AIC3206's common mode voltage. The input coupling capacitor in combination with the selected input impedance of TLV320AIC3206 forms a high-pass filter.

$$F_c = 1/(2 \times \pi \times R_{eq} C_c) \quad (1)$$

$$C_c = 1/(2 \times \pi \times R_{eq} F_c) \quad (2)$$

For high fidelity audio recording application it is desirable to keep the cutoff frequency of the high pass filter as low as possible. For single-ended input mode, the equivalent input resistance R_{eq} can be calculated as

$$R_{eq} = R_{in} \times (1 + 2g)/(1+g) \quad (3)$$

where g is the analog PGA gain calculated in linear terms.

$$g = 10000 \times 2^{\text{floor}(G/6)}/R_{in} \quad (4)$$

where G is the analog PGA gain programmed in P1_R59-R60 (in dB) and R_{in} is the value of the resistor programmed in P1_R52-R57 and assumes $R_{in} = R_{cm}$ (as defined in P1_R52-R57).

For differential input mode, R_{eq} of the half circuit can be calculated as:

$$R_{eq} = R_{in} \quad (5)$$

where R_{in} is the value of the resistor programmed in P1_R52-R57, assuming symmetrical inputs.

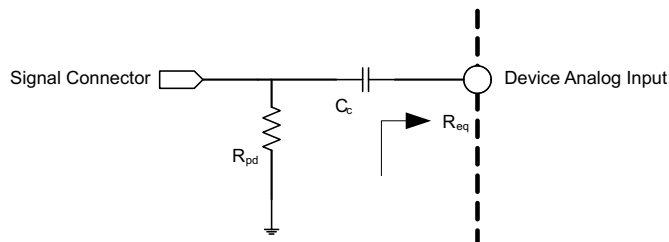


Figure 22. Analog Input Connection With Pull-down Resistor

Typical Application (continued)

When the analog signal is connected to the system through a connector such as audio jack, it is recommended to put a pull-down resistor on the signal as shown in Figure 22. The pulldown resistor helps keep the signal grounded and helps improve noise immunity when no source is connected to the connector. The pulldown resistor value should be chosen large enough to avoid loading of signal source.

Each analog input of the TLV320AIC3206 is capable of handling signal amplitude of 0.5 Vrms. If the input signal source can drive signals higher than the maximum value, an external resistor divider network as shown in Figure 23 should be used to attenuate the signal to less than 0.5Vrms before connecting the signal to the device. The resistor values of the network should be chosen to provide desired attenuation as well as Equation 6.

$$R_1 || R_2 \ll R_{eq} \quad (6)$$

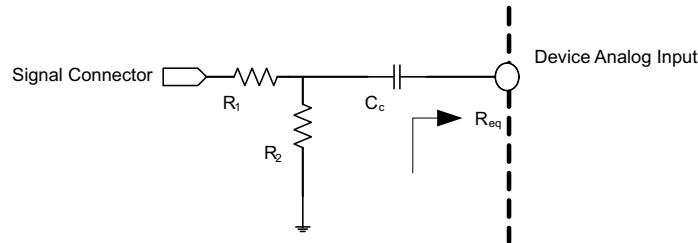


Figure 23. Analog Input Connection With Resistor Divider Network

Whenever any of the analog input terminals IN1_L, IN2_L, IN3_L, IN1_R, IN2_R or IN3_R are not used in an application, it is recommended to short the unused input terminals together (if convenient) and connect them to ground using a small capacitor (example 0.1 µF).

11.2.2.2 Analog Output Connection

The line and headphone outputs of the TLV320AIC3206 drive a signal biased around the device common mode voltage. To avoid loading the common mode with the load, it is recommended to connect the single-ended load through an ac-coupling capacitor. The ac-coupling capacitor in combination with the load impedance forms a high pass filter.

$$F_c = 1/(2 \times \pi \times R_L C_c) \quad (7)$$

$$C_c = 1/(2 \times \pi \times R_L F_c) \quad (8)$$

For high fidelity playback, the cutoff frequency of the resultant high-pass filter should be kept low. For example with R_L of 10 kΩ, using 1-µF coupling capacitor results in a cut-off frequency of 8 Hz.

For differential lineout configurations, the load should be directly connected between the differential outputs, with no coupling capacitor.

The TLV320AIC3206 supports headphone in single-ended configuration and drives the signal biased around ground. The headphone load can be directly connected between device terminals and ground.

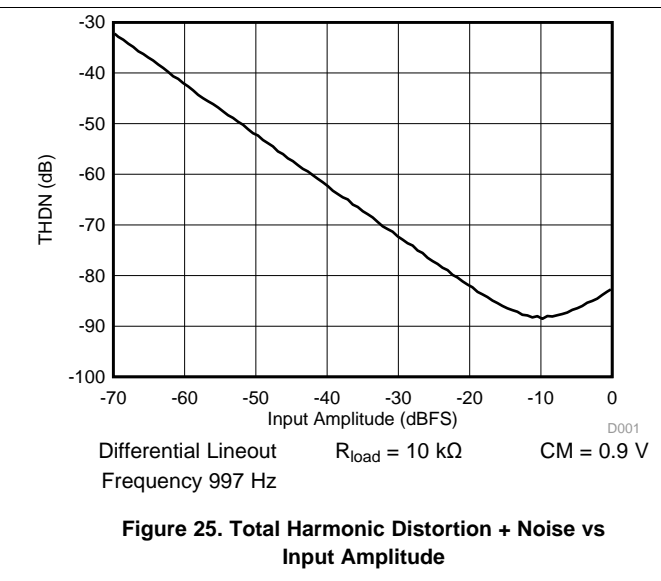
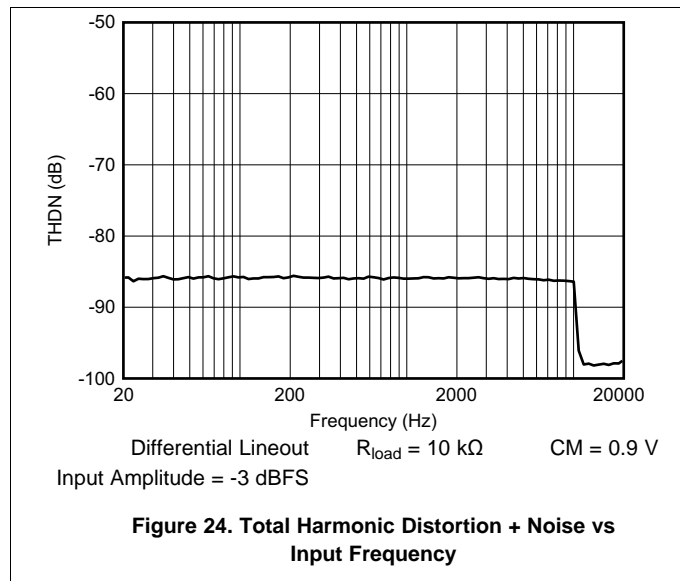
Whenever any of the analog output terminals LOL, LOR, HPL or HPR are not used in an application, they should be left open or not connected.

Typical Application (continued)

11.2.3 Application Curves

Figure 24 shows the excellent low-distortion performance of the TLV320AIC3206 in a system over the 20-Hz to 20-kHz audio spectrum.

Figure 25 shows the distortion performance of the TLV320AIC3206 in a system over the input amplitude range.



12 Power Supply Recommendations

Device power consumption largely depends on PowerTune configuration.

The device has an integrated charge pump. In ground-centered headphone configuration, all supplies can be conveniently supplied from a single 1.5V to 1.95V rail. The device has separate power domains for digital IO, digital core, analog core, charge-pump input and headphone drive, all of which can be connected together and be supplied from one source. For improved power efficiency, the digital core voltage can range from 1.26V to 1.95V. The IO voltage can be supplied in the range of 1.1V to 3.6V.

The device power supply Vsys can be supplied in the range of 1.5V to 5.5V. Vsys must always be greater than or equal to AVdd and DVdd voltages.

The AVDD, DRVDD_HP and DVDD_CP power inputs are used to power the analog circuits including analog to digital converters, digital to analog converters, programmable gain amplifiers, headphone amplifiers, charge pump etc. The analog blocks in TLV320AIC3206 have high power supply rejection ratio, however it is recommended that these supplies be powered by well regulated power supplies like low dropout regulators (LDO) for optimal performance. When these power terminals are driven from a common power source, the current drawn from the source will depend upon blocks enabled inside the device. However as an example when all the internal blocks powered are enabled the source should be able to deliver 150mA of current.

The DVDD powers the digital core of TLV320AIC3206, including the audio serial interface, control interfaces (SPI or I2C), clock generation and PLL. The DVDD power can be driven by high efficiency switching regulators or low drop out regulators. When the PRB modes are used then the peak current load on DVDD supply source could be approximately 20 mA.

The IOVDD powers the digital input and digital output buffers of TLV320AIC3206. The current consumption of this power depends on configuration of digital terminals as inputs or outputs. When the digital terminals are configured as outputs, the current consumption would depend on switching frequency of the signal and the load on the output terminal, which depends on board design and input capacitance of other devices connected to the signal.

Refer to [Figure 21](#) for recommendations on decoupling capacitors.

For more detailed information see the TLV320AIC3206 Application Reference Guide, [SLAA463](#).

13 Layout

13.1 Layout Guidelines

Each system design and PCB layout is unique. The layout should be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize TLV320AIC3206 performance:

- Connect the thermal pad to ground.
- The decoupling capacitors for the power supplies should be placed close to the device terminals. [Figure 21](#) shows the recommended decoupling capacitors for the TLV320AIC3206.
- Place the flying capacitor between FLY_P and FLY_N near the device terminals, with no VIAS in the trace between the device terminals and the capacitor. Similarly, keep the decoupling capacitor on VNEG near the device terminal with minimal VIAS in the trace between the device terminals, capacitor and PCB ground.
- The TLV320AIC3206 internal voltage references must be filtered using external capacitors. Place the filter capacitors on REF near the device terminals for optimal performance.
- The TLV320AIC3206 reduces crosstalk by a separate ground sense signal for the headphone jack. To optimize crosstalk performance, use a separate trace from the HPVSS_SENSE terminal to the headphone jack ground terminal, with no other ground connections along the length.
- For analog differential audio signals, the signals should be routed differentially on the PCB for better noise immunity. Avoid crossing of digital and analog signals to avoid undesirable crosstalk.

13.2 Layout Example

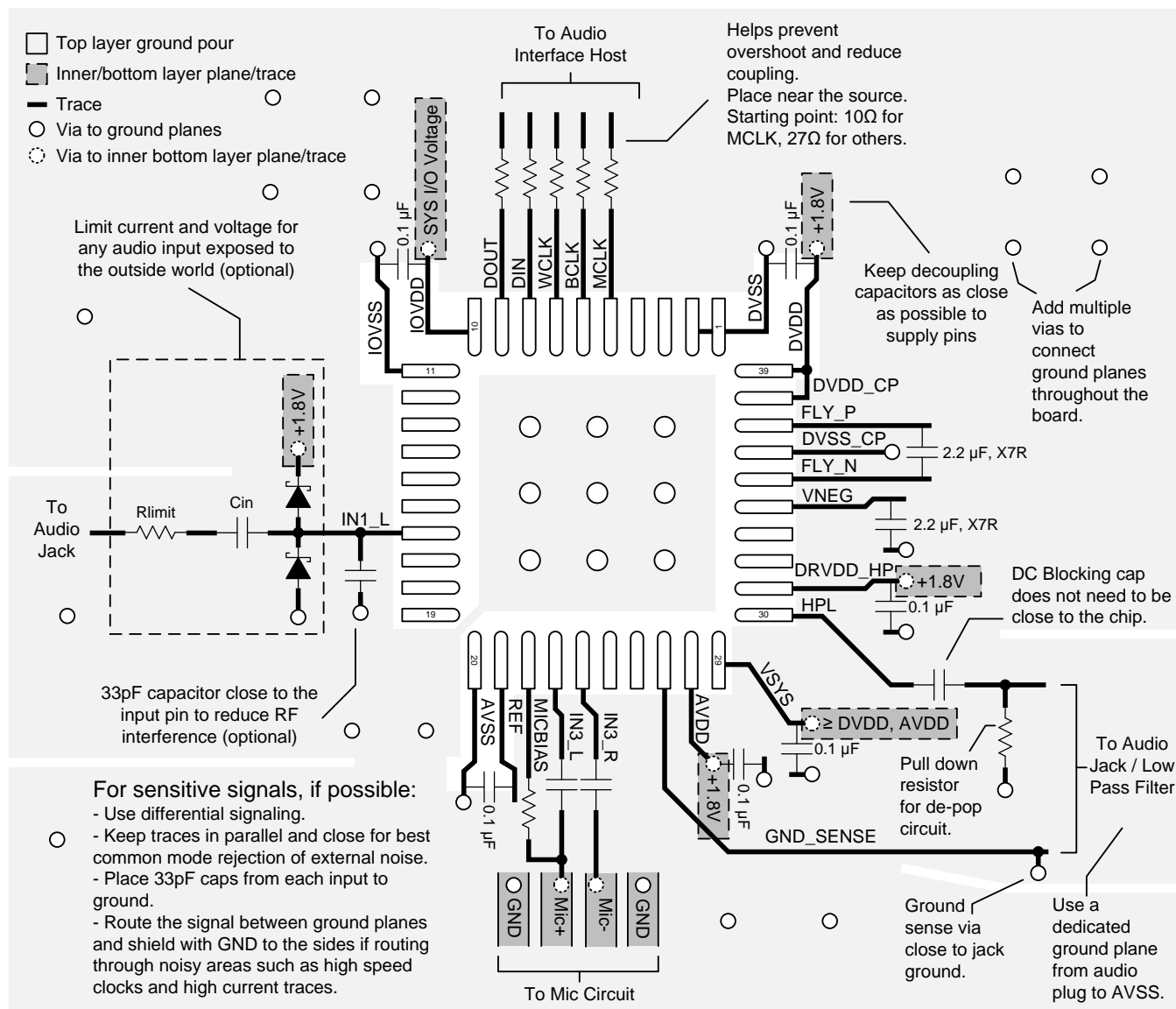


Figure 26. TLV320AIC3206 Layout

Example layout views can be found in the EVM User Guide:

- <http://www.ti.com/tool/TLV320AIC3206EVM-U>

14 Device and Documentation Support

14.1 Documentation Support

14.1.1 Related Documentation

TLV320AIC3206 Application Reference Guide, [SLAA463](#).

14.2 Trademarks

PowerTune is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

14.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV320AIC3206IRSB | ACTIVE | WQFN | RSB | 40 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | AIC 3206I | Samples |
| TLV320AIC3206IRSBT | ACTIVE | WQFN | RSB | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | AIC 3206I | Samples |
| TLV320AIC3206IYZFR | ACTIVE | DSBGA | YZF | 42 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | AIC3206I | Samples |
| TLV320AIC3206IYZFT | ACTIVE | DSBGA | YZF | 42 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | AIC3206I | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV320AIC3206IRSBR | WQFN | RSB | 40 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| TLV320AIC3206IRSBT | WQFN | RSB | 40 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| TLV320AIC3206IYZFR | DSBGA | YZF | 42 | 2500 | 330.0 | 12.4 | 3.5 | 3.7 | 0.81 | 8.0 | 12.0 | Q1 |
| TLV320AIC3206IYZFT | DSBGA | YZF | 42 | 250 | 330.0 | 12.4 | 3.5 | 3.7 | 0.81 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV320AIC3206IRSBR | WQFN | RSB | 40 | 3000 | 367.0 | 367.0 | 35.0 |
| TLV320AIC3206IRSBT | WQFN | RSB | 40 | 250 | 210.0 | 185.0 | 35.0 |
| TLV320AIC3206IYZFR | DSBGA | YZF | 42 | 2500 | 367.0 | 367.0 | 35.0 |
| TLV320AIC3206IYZFT | DSBGA | YZF | 42 | 250 | 367.0 | 367.0 | 35.0 |

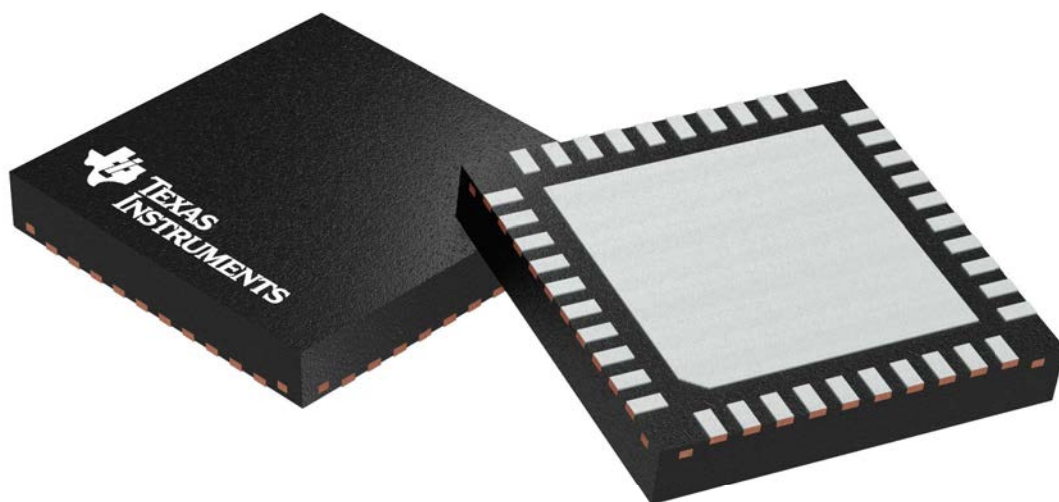
GENERIC PACKAGE VIEW

RSB 40

WQFN - 0.8 mm max height

5 x 5 mm, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

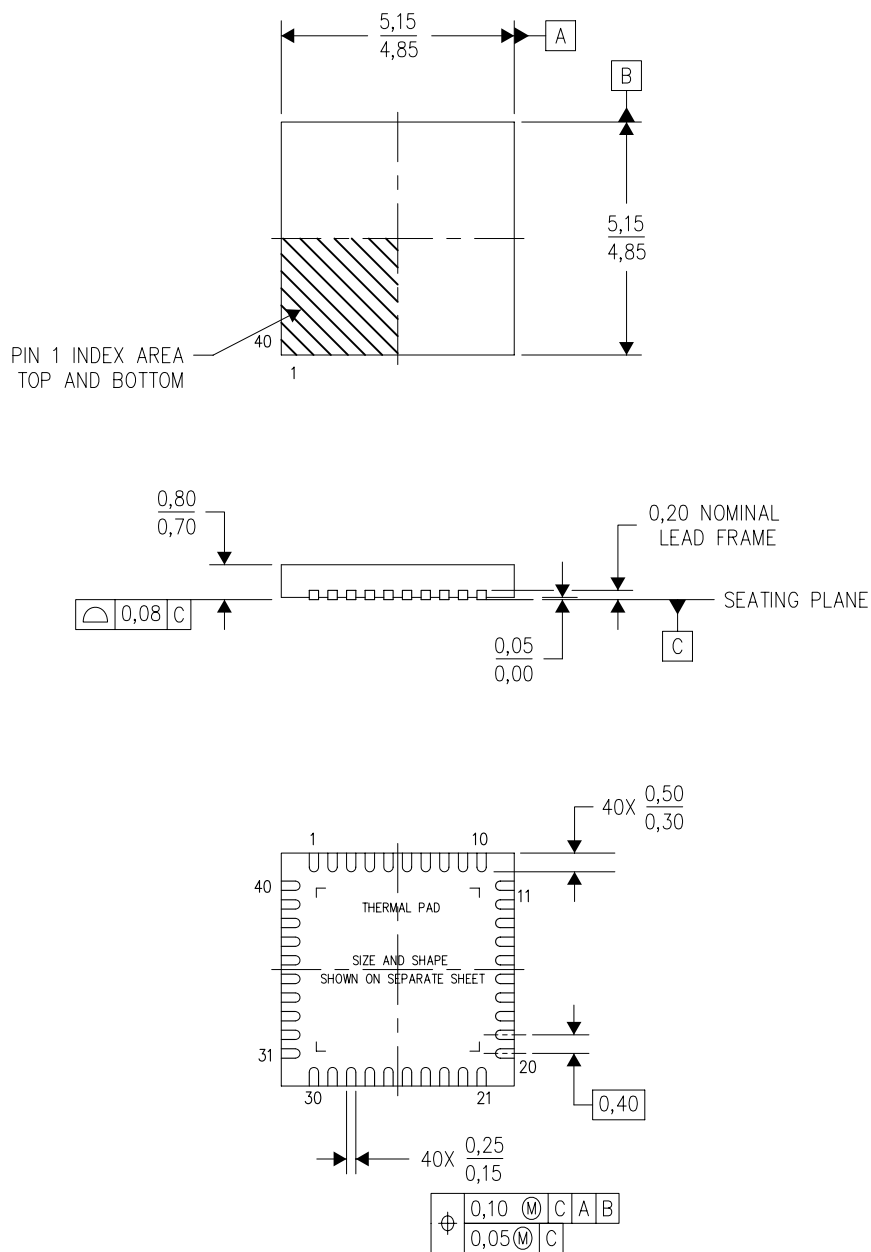


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207182/D

RSB (S-PWQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



4207182/C 05/11

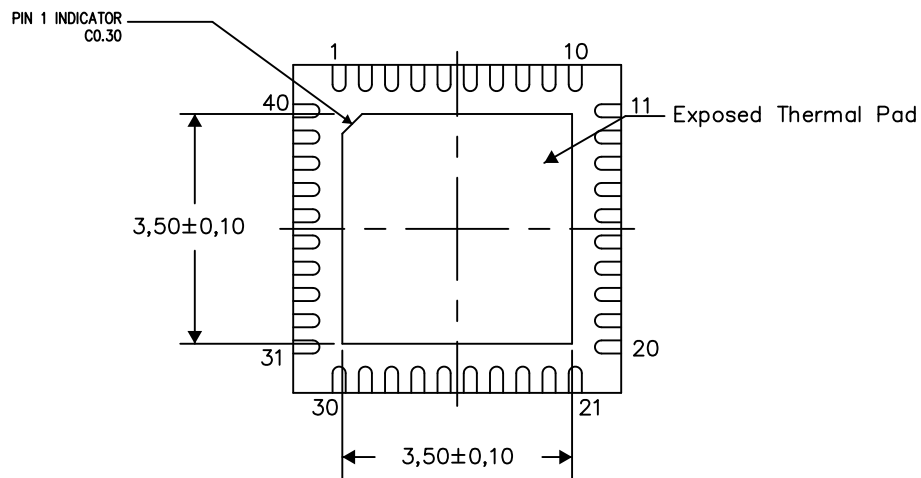
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

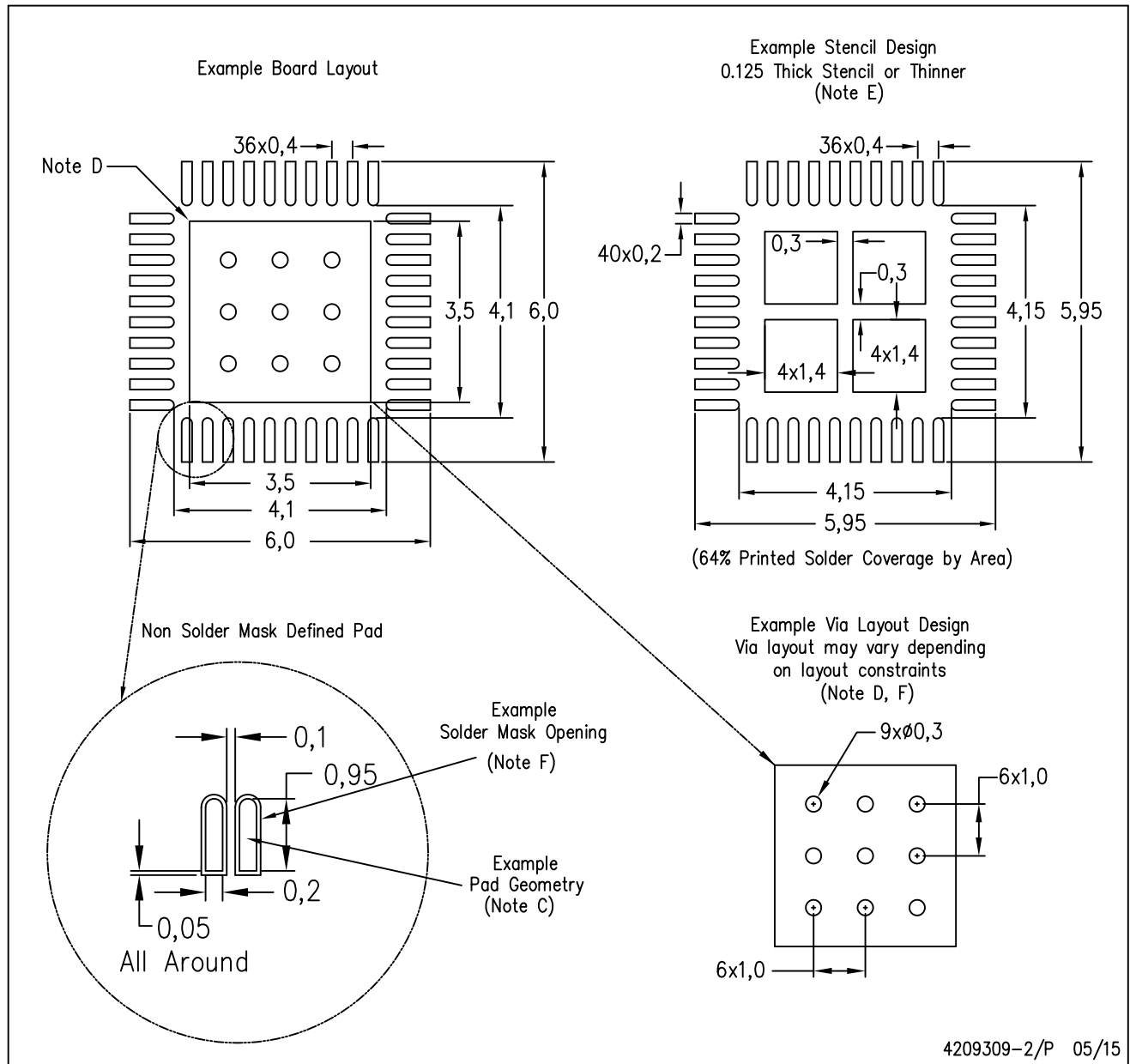
Exposed Thermal Pad Dimensions

4207183-2/R 05/15

NOTE: All linear dimensions are in millimeters

RSB (S-PWQFN-N40)

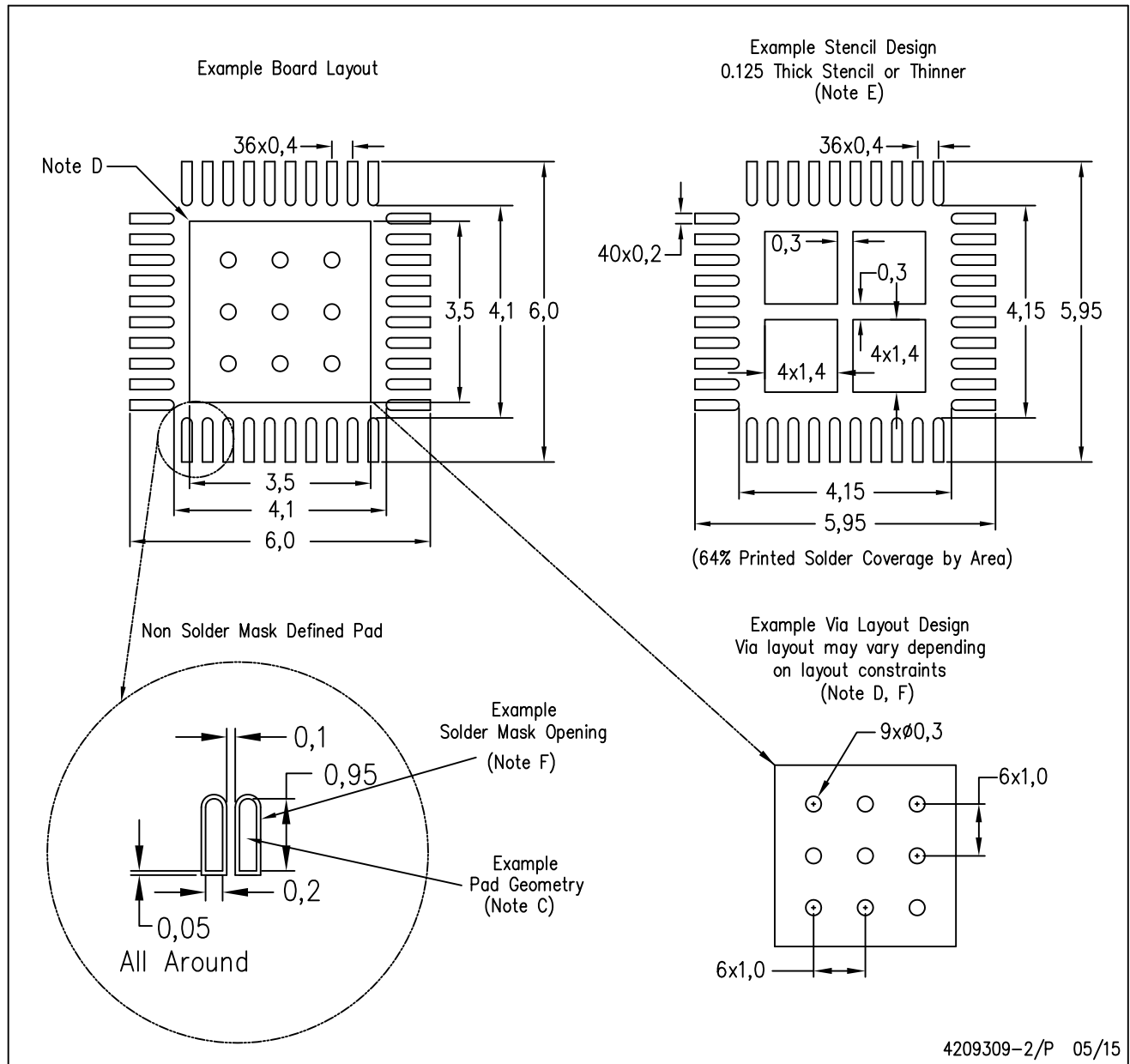
PLASTIC QUAD FLATPACK NO-LEAD



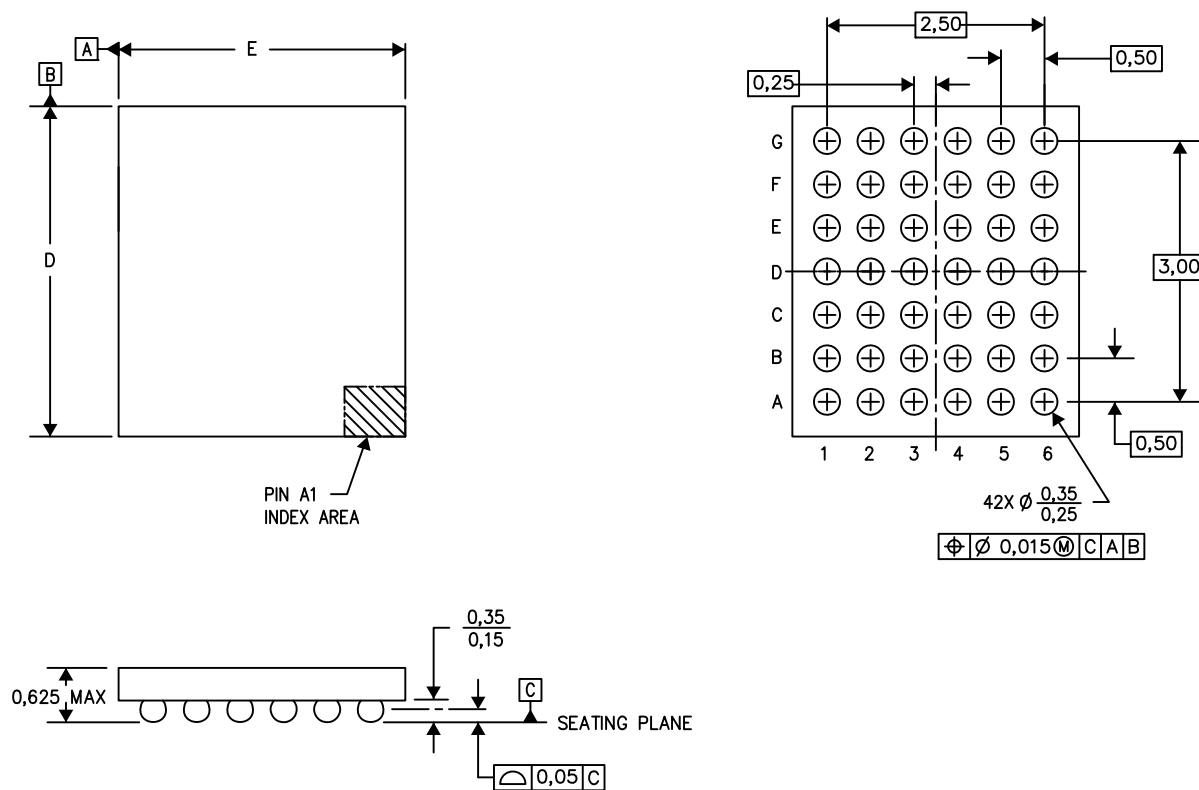
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RSB (S-PWQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



D: Max = 3.499 mm, Min = 3.439 mm

E: Max = 3.299 mm, Min = 3.239 mm

4205058-7/P 07/13

- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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