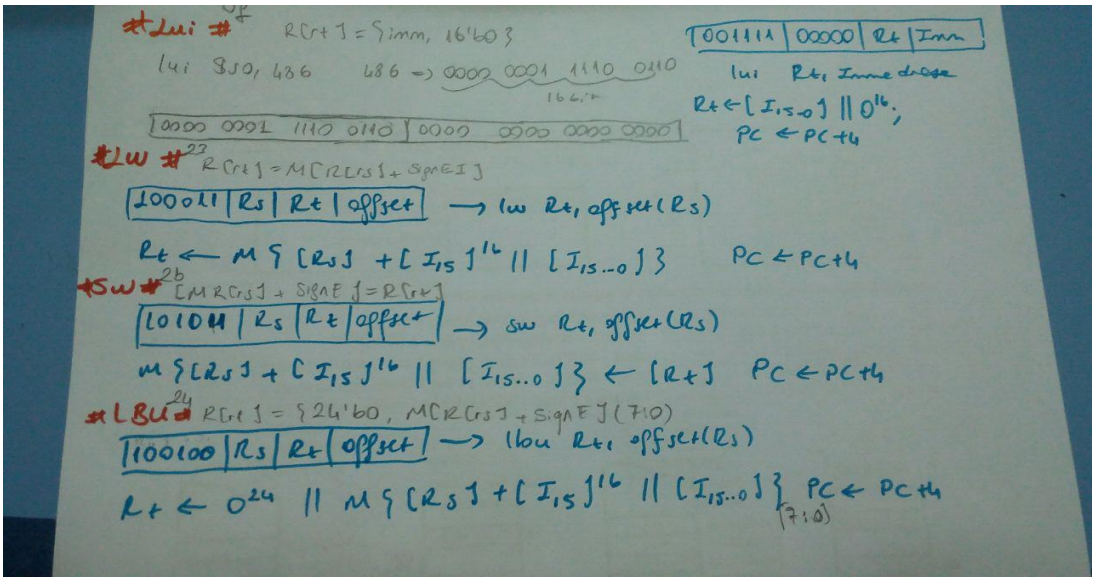
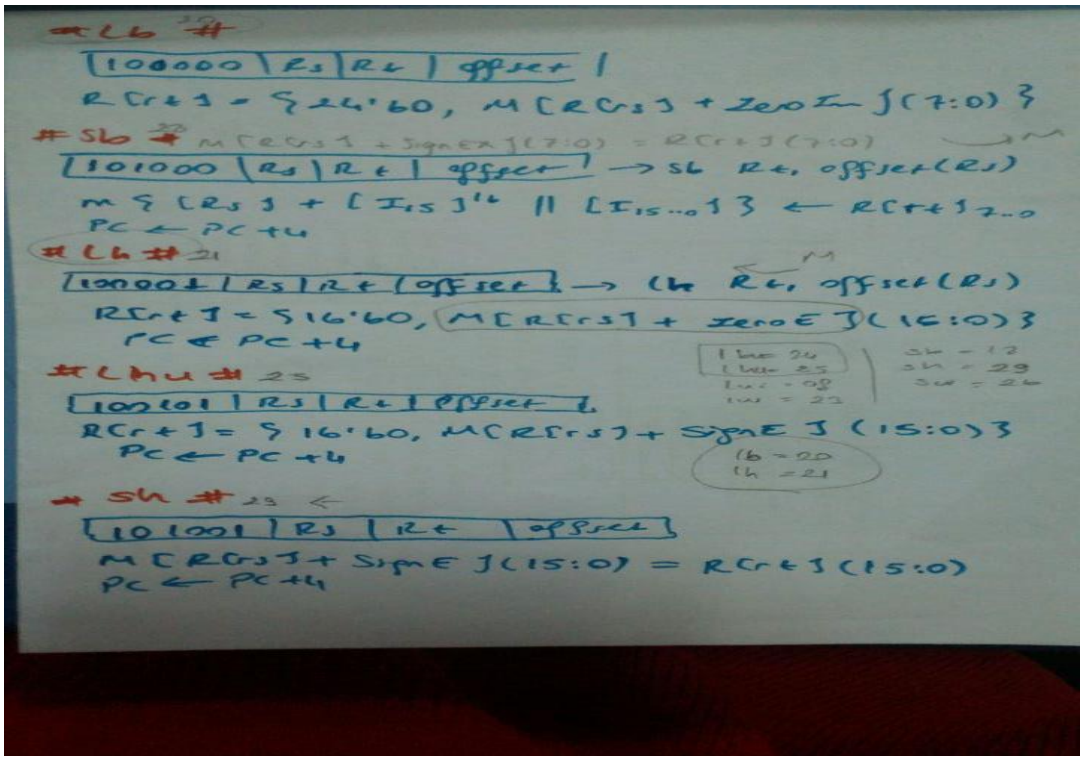
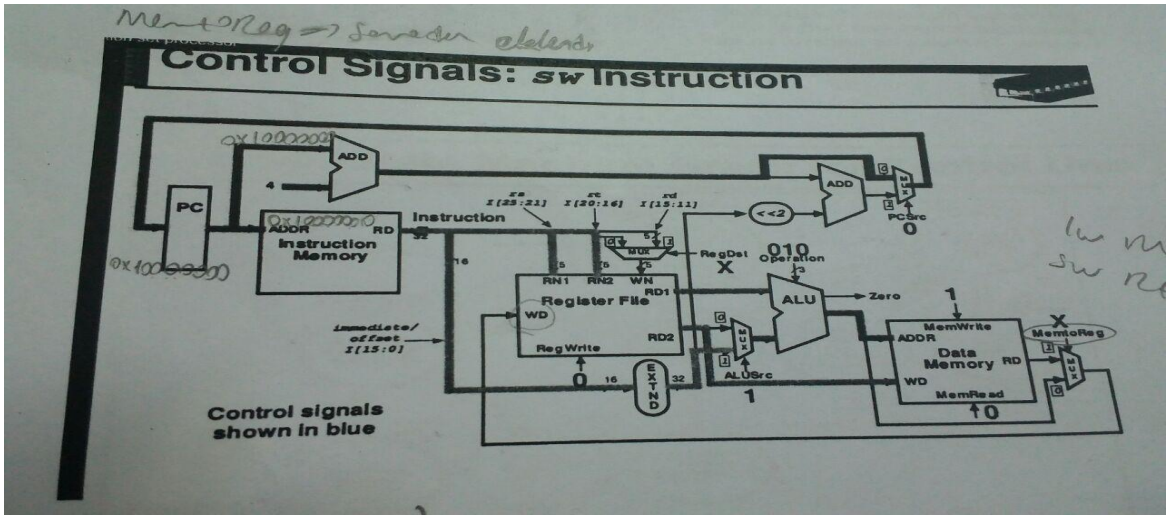
REPORT_HW3

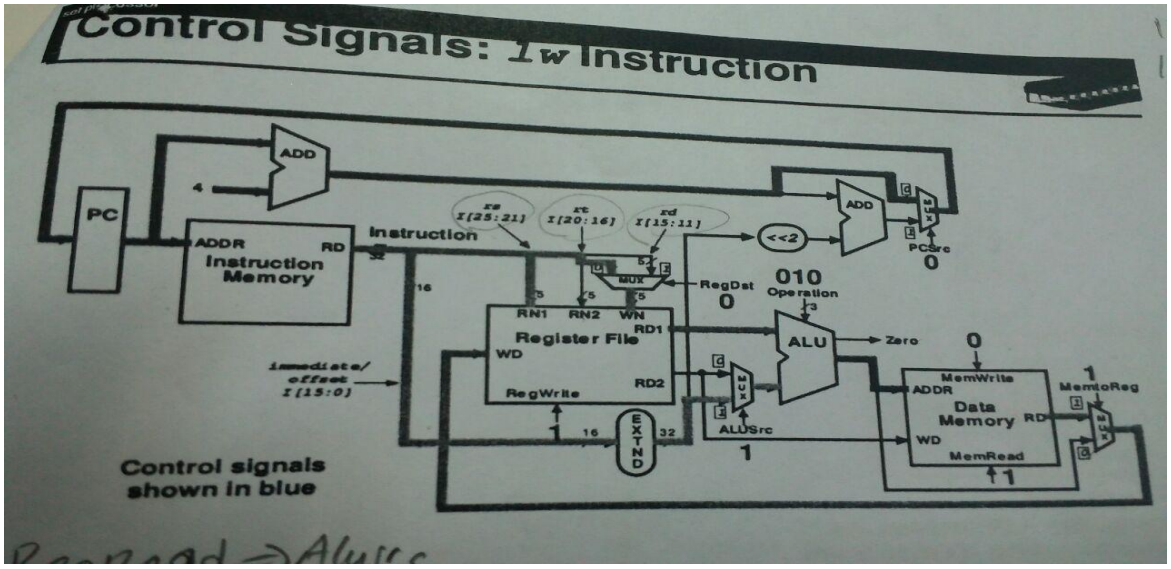
Odev icin hazirladigim instruction ve görevleri tablosu:



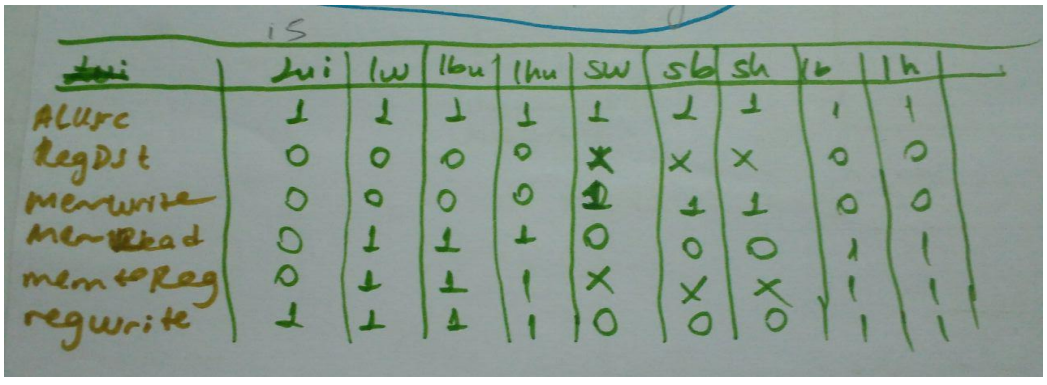


Asagidaki 2 gorsel sw ve lw icin datapath hareketleri ve sinyal değerlerini gösteriyor. Ben de bu değerlere ve yapiya gore ödevimi yaptim. Genellikle yaptigim işlemler opcode'a gore kontrol işlemleridir. Asagidaki yapiyi oluşturdum ve bu yapilari structuarl bir sekilde yazdım. ALU yerine 32BitAdder kullandim.





Bu değerleri ControlUnit'imde kullandim, gerekli sinyalleri bulabilmek icin.



	lui	lw	lbu	lhu	sw	sb	sh	lb	lh
ALUsrc	1	1	1	1	1	1	1	1	1
RegDst	0	0	0	0	X	X	X	0	0
MemWrite	0	0	0	0	1	1	1	0	0
MemRead	0	1	1	1	0	0	0	1	1
memtoReg	0	1	1	1	X	X	X	1	1
regwrite	1	1	1	1	0	0	0	1	1

Data Memery ve Register unitlerinde sorunlar vardir.

Mips32 icin yazdigim testbench sonuclaridir:

```
VSIM 5> step -current
# instruction = 00111100000010000000000000000101
# rs = 00000, opcode = 001111, rt = 01000, immediate = 0000000000000101
# ALUSrc = 1, RegWrite = 1, MemRead = 0, MemWrite = 0, RegDst = 0, MemtoReg = 0, opcode = 1111
# readD1 = 00000000000000000000000000000000, readD2 = 00000000000001010000000000000000, writeD = 00000000000001010000000000000000
# readR1 = 00000, readR2 = 01000, writeReg = 01000, regWrS = 1
# memoryReadData = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, address = 00000000000001010000000000000000
# rtContent = 00000000000001010000000000000000, MemRead = 0, MemWrite = 0
# writeData = 00000000000001010000000000000000, address = 00000000000001010000000000000000
# memoryReadData = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, MemtoReg = 0
# result = 00000000000001010000000000000000
#
#
#
# instruction = 10001101001100000000000000000101
# rs = 01001, opcode = 100011, rt = 10000, immediate = 0000000000000101
# ALUSrc = 1, RegWrite = 1, MemRead = 1, MemWrite = 0, RegDst = 0, MemtoReg = 1, opcode = 0011
# readD1 = 00000000000000000000000011110000, readD2 = 00000000000000000000000000010101, writeD = 00000000000000000000000000010101
# readR1 = 01001, readR2 = 10000, writeReg = 10000, regWrS = 1
# memoryReadData = 00000000000000000000000000010101, address = 00000000000000000000000011110101
# rtContent = 00000000000000000000000000010101, MemRead = 1, MemWrite = 0
# writeData = 00000000000000000000000000010101, address = 00000000000000000000000011110101
# memoryReadData = 00000000000000000000000000010101, MemtoReg = 1
# result = 00000000000000000000000000010101
#
#
#
# instruction = 10101101010100010000000000000101
# rs = 01010, opcode = 101011, rt = 10001, immediate = 0000000000000101
# ALUSrc = 1, RegWrite = 0, MemRead = 0, MemWrite = 1, RegDst = x, MemtoReg = x, opcode = 1011
# readD1 = 00000000000000000000111100000000, readD2 = 00000000000000000000000000010001, writeD = 0000000000000000000xxxx000x0x0x
# readR1 = 01010, readR2 = 10001, writeReg = xxxxx, regWrS = 0
# memoryReadData = 00000000000000000000000000010101, address = 00000000000000000000111100000101
# rtContent = 00000000000000000000000000010001, MemRead = 0, MemWrite = 1
# writeData = 0000000000000000000xxxx000x0x0x, address = 00000000000000000000111100000101
# memoryReadData = 00000000000000000000000000010101, MemtoReg = x
# result = 0000000000000000000xxxx000x0x0x
#
#
#
# instruction = 10010001011100100000000000000101
# rs = 01011, opcode = 100100, rt = 10010, immediate = 0000000000000101
# ALUSrc = 1, RegWrite = 1, MemRead = 1, MemWrite = 0, RegDst = 0, MemtoReg = 1, opcode = 0100
# readD1 = 00000000000000000000010000000000, readD2 = 00000000000000000000000xxxxxxxx, writeD = 00000000000000000000000xxxxxxxx
# readR1 = 01011, readR2 = 10010, writeReg = 10010, regWrS = 1
# memoryReadData = 00000000000000000000000000xxxxxxx, address = 00000000000000000000100000000101
# rtContent = 00000000000000000000000000xxxxxxx, MemRead = 1, MemWrite = 0
# writeData = 00000000000000000000000000xxxxxxx, address = 00000000000000000000100000000101
# memoryReadData = 00000000000000000000000000xxxxxxx, MemtoReg = 1
# result = 00000000000000000000000000xxxxxxx
#
#
#
# instruction = 10000001100100110000000000000101
# rs = 01100, opcode = 100000, rt = 10011, immediate = 0000000000000101
# ALUSrc = 1, RegWrite = 1, MemRead = 1, MemWrite = 0, RegDst = 0, MemtoReg = 1, opcode = 0000
# readD1 = 00000000000000000000000000100000, readD2 = 00000000000000000000000000000101, writeD = 00000000000000000000000000000101
# readR1 = 01100, readR2 = 10011, writeReg = 10011, regWrS = 1
# memoryReadData = 00000000000000000000000000000101, address = 00000000000000000000000000100101
# rtContent = 00000000000000000000000000000101, MemRead = 1, MemWrite = 0
# writeData = 00000000000000000000000000000101, address = 00000000000000000000000000100101
# memoryReadData = 00000000000000000000000000000101, MemtoReg = 1
# result = 00000000000000000000000000000101
#
#
#
# instruction = 10100001101101000000000000000101
# rs = 01101, opcode = 101000, rt = 10100, immediate = 0000000000000101
# ALUSrc = 1, RegWrite = 0, MemRead = 0, MemWrite = 1, RegDst = x, MemtoReg = x, opcode = 1000
# readD1 = 00000000000000000000000000001001, readD2 = 00000000000000000000000000010100, writeD = 0000000000000000000000000000xxxx
# readR1 = 01101, readR2 = 10100, writeReg = xxxxx, regWrS = 0
# memoryReadData = 00000000000000000000000000000101, address = 00000000000000000000000000001110
# rtContent = 00000000000000000000000000010100, MemRead = 0, MemWrite = 1
# writeData = 00000000000000000000000000000xxxx, address = 00000000000000000000000000001110
# memoryReadData = 00000000000000000000000000000101, MemtoReg = x
# result = 00000000000000000000000000000xxxx
#
```

```
#
# instruction = 10100111000101110000000000000101
# rs = 11000, opcode = 101001, rt = 10111, immediate = 0000000000000101
# ALUSrc = 1, RegWrite = 0, MemRead = 0, MemWrite = 1, RegDst = x, MemtoReg = x, opcode = 1001
# readD1 = 00000000000000000000000000011000, readD2 = 00000000000000000000000000010111, writeD = 0000000000000000000000000000xxx0x
# readR1 = 11000, readR2 = 10111, writeReg = xxxxx, regWrS = 0
# memoryReadData = 00000000000000000000000000000101, address = 00000000000000000000000000011101
# rtContent = 00000000000000000000000000010111, MemRead = 0, MemWrite = 1
# writeData = 0000000000000000000000000000xxx0x, address = 00000000000000000000000000011101
# memoryReadData = 00000000000000000000000000000101, MemtoReg = x
# result = 0000000000000000000000000000xxx0x
#
#
#
# instruction = 00111110000011001000000000000111
# rs = 00000, opcode = 001111, rt = 11001, immediate = 0000000000000111
# ALUSrc = 1, RegWrite = 1, MemRead = 0, MemWrite = 0, RegDst = 0, MemtoReg = 0, opcode = 1111
# readD1 = 00000000000000000000000000000000, readD2 = 00000000000001110000000000000000, writeD = 00000000000001110000000000000000
# readR1 = 00000, readR2 = 11001, writeReg = 11001, regWrS = 1
# memoryReadData = 00000000000000000000000000000101, address = 00000000000001110000000000000000
# rtContent = 00000000000001110000000000000000, MemRead = 0, MemWrite = 0
# writeData = 00000000000001110000000000000000, address = 00000000000001110000000000000000
# memoryReadData = 00000000000000000000000000000101, MemtoReg = 0
# result = 00000000000001110000000000000000
#
```

```
#
# instruction = 10001101000010010000000000000111
# rs = 01000, opcode = 100011, rt = 01001, immediate = 0000000000000111
# ALUSrc = 1, RegWrite = 1, MemRead = 1, MemWrite = 0, RegDst = 0, MemtoReg = 1, opcode = 0011
# readD1 = 00000000000000101000000000000000, readD2 = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, writeD = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
# readR1 = 01000, readR2 = 01001, writeReg = 01001, regWrS = 1
# memoryReadData = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, address = 00000000000000101000000000000111
# rtContent = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, MemRead = 1, MemWrite = 0
# writeData = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, address = 00000000000000101000000000000111
# memoryReadData = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, MemtoReg = 1
# result = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
#
#
#
# instruction = 10101110001010100000000000000111
# rs = 10001, opcode = 101011, rt = 01010, immediate = 0000000000000111
# ALUSrc = 1, RegWrite = 0, MemRead = 0, MemWrite = 1, RegDst = x, MemtoReg = x, opcode = 1011
# readD1 = 00000000000000000000000000010001, readD2 = 00000000000000000000111100000000, writeD = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
# readR1 = 10001, readR2 = 01010, writeReg = xxxxx, regWrS = 0
# memoryReadData = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, address = 00000000000000000000000000011000
# rtContent = 00000000000000000000111100000000, MemRead = 0, MemWrite = 1
# writeData = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, address = 00000000000000000000000000011000
# memoryReadData = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, MemtoReg = x
# result = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
#
```

```
#
# instruction = 10000101110101010000000000000101
# rs = 01110, opcode = 100001, rt = 10101, immediate = 0000000000000101
# ALUSrc = 1, RegWrite = 1, MemRead = 1, MemWrite = 0, RegDst = 0, MemtoReg = 1, opcode = 0001
# readD1 = 00000000000000000000000000001100, readD2 = 00000000000000000000000000010001, writeD = 00000000000000000000000000010001
# readR1 = 01110, readR2 = 10101, writeReg = 10101, regWrS = 1
# memoryReadData = 00000000000000000000000000010001, address = 00000000000000000000000000010001
# rtContent = 00000000000000000000000000010001, MemRead = 1, MemWrite = 0
# writeData = 00000000000000000000000000010001, address = 00000000000000000000000000010001
# memoryReadData = 00000000000000000000000000010001, MemtoReg = 1
# result = 00000000000000000000000000010001
#
#
#
# instruction = 10010101111101100000000000000101
# rs = 01111, opcode = 100101, rt = 10110, immediate = 0000000000000101
# ALUSrc = 1, RegWrite = 1, MemRead = 1, MemWrite = 0, RegDst = 0, MemtoReg = 1, opcode = 0101
# readD1 = 00000000000000000000000001100000, readD2 = 00000000000000000000000000000101, writeD = 00000000000000000000000000000101
# readR1 = 01111, readR2 = 10110, writeReg = 10110, regWrS = 1
# memoryReadData = 00000000000000000000000000000101, address = 00000000000000000000000001100101
# rtContent = 00000000000000000000000000000101, MemRead = 1, MemWrite = 0
# writeData = 00000000000000000000000000000101, address = 00000000000000000000000001100101
# memoryReadData = 00000000000000000000000000000101, MemtoReg = 1
# result = 00000000000000000000000000000101
#
```

```
# instruction = 10100010100011010000000000000111
# rs = 10100, opcode = 101000, rt = 01101, immediate = 0000000000000111
# ALUSrc = 1, RegWrite = 0, MemRead = 0, MemWrite = 1, RegDst = x, MemtoReg = x, opcode = 1000
# readD1 = 00000000000000000000000000010100, readD2 = 00000000000000000000000000001001, writeD = xxxxxxxxxxxxxxxxxxxxxxxx000xxxxx
# readR1 = 10100, readR2 = 01101, writeReg = xxxxx, regWrS = 0
# memoryReadData = xxxxxxxxxxxxxxxxxxxxxxxx00001100, address = 00000000000000000000000000011011
# rtContent = 00000000000000000000000000001001, MemRead = 0, MemWrite = 1
# writeData = xxxxxxxxxxxxxxxxxxxxxxxx000xxxxx, address = 00000000000000000000000000011011
# memoryReadData = xxxxxxxxxxxxxxxxxxxxxxxx00001100, MemtoReg = x
# result = xxxxxxxxxxxxxxxxxxxxxxxx000xxxxx
#
#
#
# instruction = 10000110101011100000000000000111
# rs = 10101, opcode = 100001, rt = 01110, immediate = 0000000000000111
# ALUSrc = 1, RegWrite = 1, MemRead = 1, MemWrite = 0, RegDst = 0, MemtoReg = 1, opcode = 0001
# readD1 = 00000000000000000000000000010001, readD2 = 00000000000000000000111100000000, writeD = xxxxxxxxxxxxxxxx0000111100000000
# readR1 = 10101, readR2 = 01110, writeReg = 01110, regWrS = 1
# memoryReadData = xxxxxxxxxxxxxxxx0000111100000000, address = 00000000000000000000000000011000
# rtContent = 00000000000000000000111100000000, MemRead = 1, MemWrite = 0
# writeData = xxxxxxxxxxxxxxxx0000111100000000, address = 00000000000000000000000000011000
# memoryReadData = xxxxxxxxxxxxxxxx0000111100000000, MemtoReg = 1
# result = xxxxxxxxxxxxxxxx0000111100000000
#
```

```
#
# instruction = 10010110110011110000000000000111
# rs = 10110, opcode = 100101, rt = 01111, immediate = 0000000000000111
# ALUSrc = 1, RegWrite = 1, MemRead = 1, MemWrite = 0, RegDst = 0, MemtoReg = 1, opcode = 0101
# readD1 = 00000000000000000000000000000101, readD2 = 00000000000000000000000000001100, writeD = xxxxxxxxxxxxxxxx0000000000001100
# readR1 = 10110, readR2 = 01111, writeReg = 01111, regWrS = 1
# memoryReadData = xxxxxxxxxxxxxxxx0000000000001100, address = 00000000000000000000000000001100
# rtContent = 00000000000000000000000000001100, MemRead = 1, MemWrite = 0
# writeData = xxxxxxxxxxxxxxxx0000000000001100, address = 00000000000000000000000000001100
# memoryReadData = xxxxxxxxxxxxxxxx0000000000001100, MemtoReg = 1
# result = xxxxxxxxxxxxxxxx0000000000001100
#
#
#
# instruction = 10100110111110000000000000000111
# rs = 10111, opcode = 101001, rt = 11000, immediate = 0000000000000111
# ALUSrc = 1, RegWrite = 0, MemRead = 0, MemWrite = 1, RegDst = x, MemtoReg = x, opcode = 1001
# readD1 = 00000000000000000000000000010111, readD2 = 00000000000000000000000000011000, writeD = xxxxxxxxxxxxxxxx000000000000xxxx0
# readR1 = 10111, readR2 = 11000, writeReg = xxxxx, regWrS = 0
# memoryReadData = xxxxxxxxxxxxxxxx0000000000001100, address = 00000000000000000000000000011110
# rtContent = 00000000000000000000000000011000, MemRead = 0, MemWrite = 1
# writeData = xxxxxxxxxxxxxxxx000000000000xxxx0, address = 00000000000000000000000000011110
# memoryReadData = xxxxxxxxxxxxxxxx0000000000001100, MemtoReg = x
# result = xxxxxxxxxxxxxxxx000000000000xxxx0
#
```

```
#
# instruction = 10010010010010110000000000000111
# rs = 10010, opcode = 100100, rt = 01011, immediate = 0000000000000111
# ALUSrc = 1, RegWrite = 1, MemRead = 1, MemWrite = 0, RegDst = 0, MemtoReg = 1, opcode = 0100
# readD1 = 00000000000000000000000000xxxxxxxx, readD2 = 00000000000000000000001000xxxxxxxx, writeD = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
# readR1 = 10010, readR2 = 01011, writeReg = 01011, regWrS = 1
# memoryReadData = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, address = 00000000000000000000000xxxxxxxxx
# rtContent = 00000000000000000000001000xxxxxxxx, MemRead = 1, MemWrite = 0
# writeData = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, address = 00000000000000000000000xxxxxxxxx
# memoryReadData = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, MemtoReg = 1
# result = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
#
#
#
# instruction = 10000010011011000000000000000111
# rs = 10011, opcode = 100000, rt = 01100, immediate = 0000000000000111
# ALUSrc = 1, RegWrite = 1, MemRead = 1, MemWrite = 0, RegDst = 0, MemtoReg = 1, opcode = 0000
# readD1 = 00000000000000000000000000000101, readD2 = 00000000000000000000000000001100, writeD = xxxxxxxxxxxxxxxxxxxxxxxx00001100
# readR1 = 10011, readR2 = 01100, writeReg = 01100, regWrS = 1
# memoryReadData = xxxxxxxxxxxxxxxxxxxxxxxx00001100, address = 00000000000000000000000000001100
# rtContent = 00000000000000000000000000001100, MemRead = 1, MemWrite = 0
# writeData = xxxxxxxxxxxxxxxxxxxxxxxx00001100, address = 00000000000000000000000000001100
# memoryReadData = xxxxxxxxxxxxxxxxxxxxxxxx00001100, MemtoReg = 1
# result = xxxxxxxxxxxxxxxxxxxxxxxx00001100
#
```