Lab 2: Inverter Characteristics and Ring Oscillator

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Objectives:

In this lab I will characterize the behavior of an inverter gate to determine the range of high and low output voltages for a range of input voltages. Next, I will design a ring oscillator using an odd number of inverter gates. I will use the oscilloscope to measure the frequency of the oscillator and derive the single state delay of a single inverter. This lab will also help me to become more familiar with the lab bench equipment.

Design:

A simple circuit is necessary to determine the output voltage range of an inverter gate, SN7404. A DC power source is set to 5 volts, which is the rating listed for each gate. The terminals of the DC power source are then connected to the power rails on the breadboard. A lead is then connected from the positive power rail to the Vcc pin on the logic gate chip, and the ground pin is connected to the ground rail on the breadboard. Finally, the digital multimeter is connected in parallel across the output to measure the output voltage.

The ring oscillator was designed using five inverter gates arranged as shown in figure 1. A single SN7404 gate is powered using a constant 5V source, and the input and output of each inverter is connected in a single loop. The lead of the oscilloscope are then connected in series after the fifth inverter to measure the frequency of the pulse as it propagates through the gates.

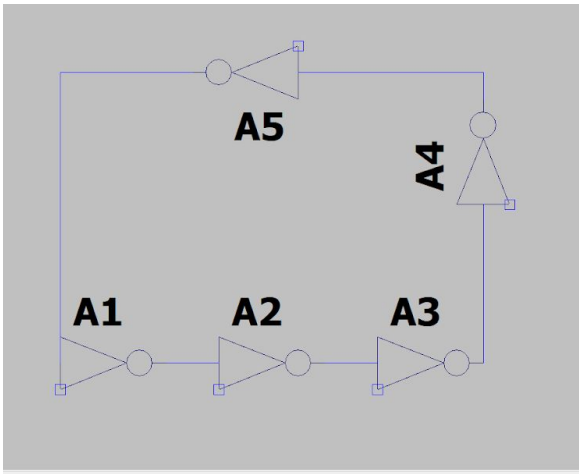

Fig. 1 Schematic for Ring Oscillator

Results:

The results below were recorded from the multimeter. Figure 2 is the Voltage Transfer Curve, which shows the output voltage versus the input voltage. A reading in the range of 3.9-4.3 V correlates to a high reading, while a reading in the range of 40-150 mV correlates to a low voltage readings.

Vin	Vout
0	4.002

0.5	4.001
1	3.433
1.2	2.9912
1.4	1.60619
1.45	1.14047
1.47	0.049259
1.5	0.04956
2	0.04923
2.5	0.04924
3	0.04922
3.5	0.049161
4	0.049115
4.5	0.049052
5	0.048971

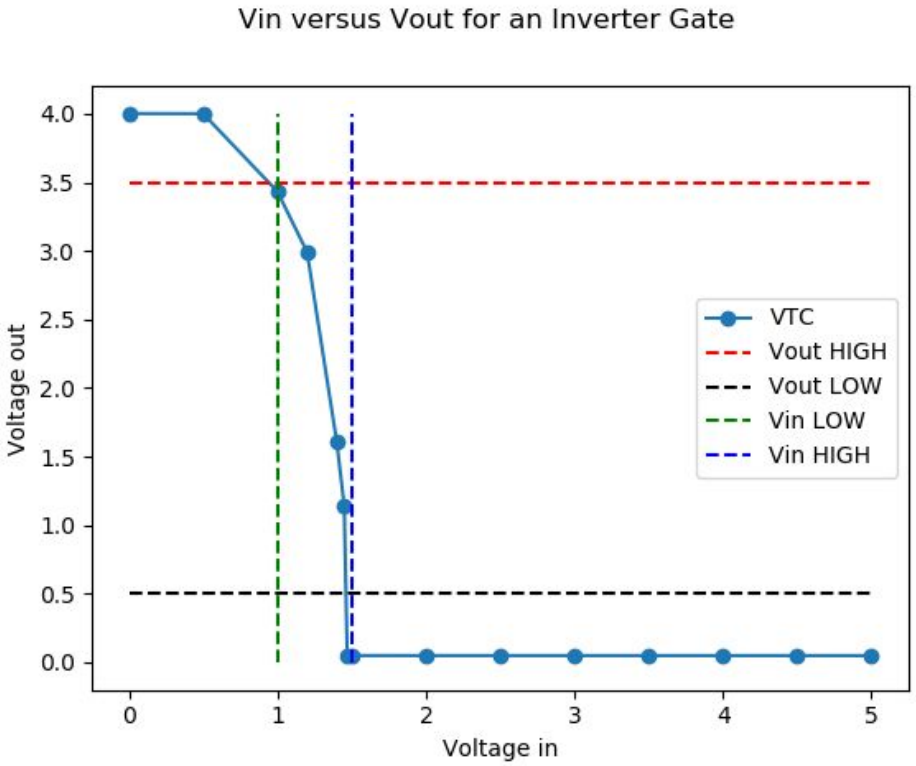

Figure 2. VTC Curve for inverter gate.

From the curve we can determine that the output voltage range is above 3.5 V for a high signal and below .5 V for a low signal. These values correspond to an input voltage below 1 V and

above 1.5 V respectively. These values were determined approximately using the procedure discussed in the lab report. The values in between are the noise margins for the inverter.

For part 2, the frequency and period of the ring oscillator was measured using the oscilloscope.

Period	78.844 ns
Frequency	12.727 MHz

These values can be used to calculate the single-stage delay of a single inverter. Let D = the delay of a single oscillator in seconds. If n is the number of gates used in the ring, than nD is the total time required for the signal to propagate through the loop one time. Since an odd number of inverters are used, the signal will be inverted after a single loop, so to return to the original value, it will take a two loops. Thus, the total period of one full oscillation, is $2 * n * D$. Since we have measured the Period, we can calculate the single state delay to be

$$D = 7.884\ ns$$

Conclusion:

In this lab we determined the VTC curve for a single inverter gate. The range of values was determined to be above 3.5 V for a high signal and below .5 V for a low signal. These values correspond to an input voltage below 1 V and above 1.5 V respectively. Additionally, the single-state delay of an inverter in a ring oscillator was found to be approximately 7.884 ns. In this lab I also became more familiar with using the bench equipment.

Questions:

Post Lab Questions

1. What range of input voltages corresponds to high and low output voltages?

   The output voltage range is above 3.5 V for a high signal and below .5 V for a low signal. These values correspond to an input voltage below 1 V and above 1.5 V respectively.

2. What is the frequency of a 21 stage oscillator with a delay of 10ns?

   Using the equation derived earlier, the period of this oscillator can be calculated to be

$T = 420\ ns$, which gives a frequency of $f = 2.381\ MHz$.

3. Are the signals P, Q, R, S from the lab report periodic and if so what are their periods?

   The signals at P,Q,R,S are all periodic with periods equal to the period measured at A. However, the signal at each point is out of phase with the gate next to it by D, the delay in seconds of a single inverter gate. Therefore, the P is out of phase with A by D, Q is out of phase by $2D$, R is out of phase by $3D$ and S is out of phase by $4D$.

Student Feedback Questions

What I liked about the lab: I liked getting to design a logic circuit and learning how to use the bench equipment, it was great getting to see everything working.

What I liked about the lab instructions: I liked the lab instructions, I thought that they were very detailed and gave good direction on how to perform the lab. I found figure 3 to be a little confusing and I think it could be more clear what trend it is trying to show.

Suggestions: I thought the lab was good and I feel more confident in using the equipment. I don't have any significant suggestions for the lab.