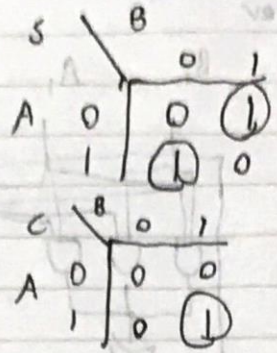
Drew Bertola, 627000567 Section 506
TA: Rachel Vell

Prelab #4 Adder Circuits

Half Adder

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

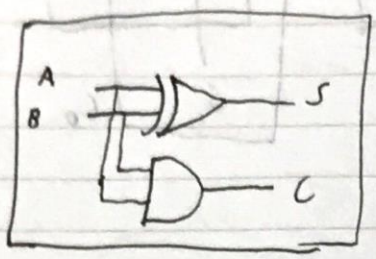


$S = A'B + B'A$

$S = A \oplus B$

$C = BA$

Diagram



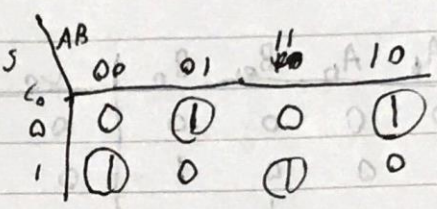
Total Gates w/o xor = 6

Total Gates with xor = 2

Less delay time and less gates when using XOR

Full Adder

A	B	C_0	S	C_1
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

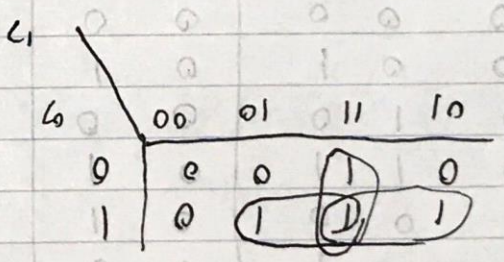


$S = C_0'A'B + C_0'AB' + C_0A'B' + C_0AB$

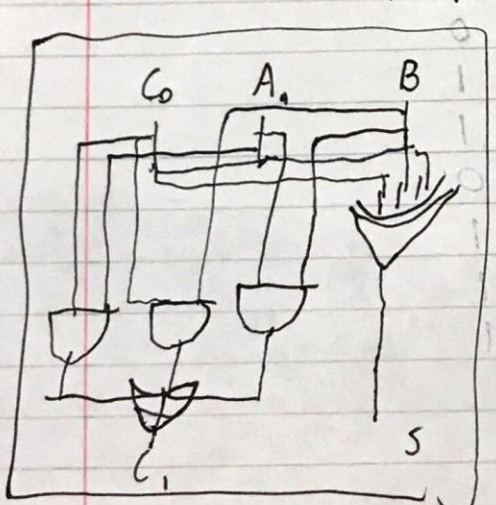
$S = A'(C_0'B + C_0B') + A(C_0'B_0' + C_0B)$

$S = A'(C \oplus B) + A(C \oplus B)'$

$\boxed{S = A \oplus (C \oplus B)}$

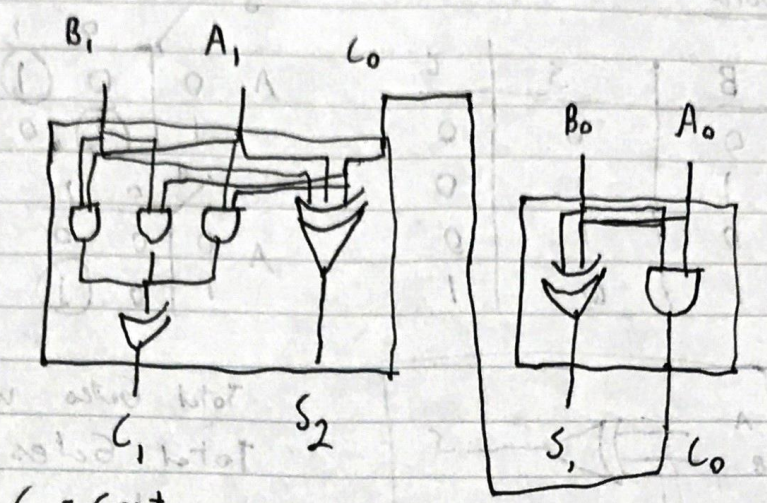


$C_0 = AB + CB + CA$



Diagram

Ripple Adder



$C_1 = C_{out}$

Truth Table

A_1	A_0	B_1	B_0	C_0	S_1	S_2	C_1
0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0
0	0	1	0	0	0	1	0
0	0	1	1	0	1	1	0
0	1	0	0	0	1	0	0
0	1	0	1	1	0	1	0
0	1	1	0	0	1	1	0
0	1	1	1	0	1	0	1
1	0	0	0	0	0	1	0
1	0	0	1	0	1	1	0
1	0	1	0	0	0	0	1
1	0	1	1	0	1	0	1
1	1	0	0	0	1	1	0
1	1	0	1	1	0	0	1
1	1	1	0	0	1	0	1
1	1	1	1	1	0	1	1