

System Spec

[illegible]

The diagram illustrates the hardware setup for an ESP32-WROOM-32 module. The power supply is connected to a +3.3V source through a 10k resistor (R9) and a 10uF capacitor (C16). The module's EN pin is connected to a 3.3V source through a 100nF capacitor (C19) and a 470nF capacitor (C12). The SW1 Restart button is connected to the module's SW pin through a 100nF capacitor (C14). The SW2 Boot button is connected to the module's SW pin through a 100nF capacitor (C27). The module's TX00/IO1 and RX00/IO1 pins are connected to the MCU's TX and RX pins. The module's TX, RX, DACDATA, and Mode_Switch pins are connected to the MCU's TX, RX, DACDATA, and Mode_SW pins. The module's BHClock, QDACDATA, DistortionFlag, DelayFlag, SDA, SCK, DAC/ADC_CLK, Pot3, Pot4, Pot1, and Pot2 pins are connected to the MCU's BHClock, QDACDATA, DistortionFlag, DelayFlag, SDA, SCK, DAC/ADC_CLK, Pot3, Pot4, Pot1, and Pot2 pins. The diagram also includes labels for 'Distortion and delay flags should be pulled high internally' and 'GPIO0 pulled-up internally'.

Analog Front End -- Guitar Input
 $Z_{in} \approx 1M\Omega$

Analog Rear end -- Output to Guitar
 $Z_{out} \approx 100\Omega$

AFE Section (Top):

- Input: Mono Jack (J4) with pins TL, SN, S, and GND.
- Offset: 1.65V, VrefD.
- HP-Filter: -3 db @ 17 Hz.
- Op-amp: OPA376xxD (U7).
- Output: DRight_Input1.
- Components: R24, R22, R27, C33, C35, R31, R32, C39, D11, D12.

Rear End Section (Bottom):

- Input: RightL_Codec_outD.
- Offset: 1.65V, VrefD.
- HP-Filter: -3dB @ 15.92Hz.
- Op-amp: OPA376xxD (U6).
- Output: J6 (NM/J4HCD2).
- Components: R20, R21, R23, R26, C32, C34, C37, C38, R28, R30, R33, R34.

Switch Modules (S1, S2):

- S1: FS57003PLT2B2M2QE. Pins 1-9. Outputs: DAFrontEnd, DelayFlag.
- S2: FS57003PLT2B2M2QE. Pins 1-9. Outputs: DAFrontEnd, DistortionFlag.

Notes:

- Remove R24, R31 and place R22 in order to bypass section.
- Remove R21, R28 and place R20 in order to bypass section.
- Optional - Clamp before exceeding Absolut Max of 3.6V.
- When S1 & S2 is off the signal goes back into the opamp. Thats why R10 is fairly big. This might cause problems, maybe not?
- 0V Reference.

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AUTO Programmer

The circuit diagram illustrates the AUTO Programmer setup. It features two NPN transistors, Q1 and Q2, both labeled SS8050-G. The base of Q1 is connected to the DTR signal line through a 10k resistor (R16). The base of Q2 is connected to the RTS signal line through a 10k resistor (R17). The emitter of Q1 is connected to GND. The emitter of Q2 is connected to the GPIO_0 signal line. The collector of Q1 is connected to the collector of Q2, which is then connected to GND.

Truth Table

DTR	RTS	ENABLE	GPIO	
1	1	1	1	Idle Mode
0	0	1	1	Idle Mode
1	0	0	1	MCU Reset
0	1	1	0	Download Mode

Output & Inputs

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Output Section:

- Resistor R29 (4.7k) connected to +3.3V.
- Capacitor C36 (100nF) connected to GND.
- GPIO2 signal line (green) connected to the output of a switch (J5).
- Note: **GPIO2 should not be pulled down! Make sure to verify this!**
- Mode switch $\tau = 4.7\text{ms}$

Input Section:

- 4x potentiometer connected to +3.3V, GND, and a 4.7M resistor.
- PotiD (pin 2) connected to the wiper of the potentiometer.
- PotiD (pin 4) and PotiD (pin 6) connected to the other two terminals of the potentiometer.