Analysing the ARM Cortex M3 Core and How It Is Integrated into the LPC1768 Microcontroller

The ARM Cortex M3 core processor, intended for microcontroller use, is specifically designed for response and power sensitive applications. The low-power and high-performance abilities, combined with its low-power peripherals, create a superior low-power embedded systems platform. This is what makes it one of the most popular choices in developing an Internet-connected device, proven by the fact that it has been deployed in billions of devices across a broad set of embedded applications.

Bus Width

The M3 includes three Advanced High-performance Bus(AHB)-Lite bus interfaces: the system bus, the I-code bus, and the D-code bus. The core buses are faster than the system bus, with one dedicated for instruction (I-code), and one for data access (D-code). This architecture allows for the code and data to be fetched simultaneously, resulting in improved performance. It supports 8, 16, and 32-bit wide transactions.

Instruction Set

The M3 features a Thumb-2 instruction set.

ARM instructions are a fixed length of 32 bits, thumb instructions are a fixed length of 16 bits. Thumb-2 instructions can be either 16-bit or 32-bits.

Peripheral Support

The M3 features include serial interfaces such as:

* Ethernet MAC
* USB 2.0 full-speed device
* Four UARTs with fractional baud rate generation
* SPI controller with synchronous, serial, full duplex communication, and programmable data length
* Three enhanced I2C bus interfaces
* I2S (Inter-IC Sound) interface for digital audio input or output, with fractional rate control

Other peripherals supported include:

* 70 General Purpose I/O (GPIO) pins with configurable pull-up/down resistors
* 12-bit Analog-to-Digital Converter (ADC)
* 10-bit Digital-to-Analog Converter (DAC)
* Four general purpose timers/counters
* One motor control
* Real-Time Clock (RTC)
* Watchdog Timer (WDT)

Security Features

The LPC1768 features three levels of Code Read Protection (CRP). This allows the user to enable different levels of security in the system so that access to the on-chip flash can be restricted.

Clocks

The Real-Time Clock (RTC) of the LPC1678 is a set of counters for measuring the passage of time to maintain a calendar and clock when system power is on, and optionally when it is off. It provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.

The RTC allows fine-tuning the count rate to provide less than 1 second per day error when operated at a constant voltage and temperature. It also contains a small set of backup registers (20 bytes) for holding data while the main part of the LPC1768 is powered off, as well as an alarm function that can wake up the LPC1768 from all reduced power modes with a time resolution of 1 s.

Memory Maps

The LPC1768 incorporates several distinct memory regions. The AHB peripheral area is 2 MB in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 1 MB in size, and is divided to allow for up to 64 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

The M3 allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register contained in the NVIC.

Interrupt Capability

The M3 has a Nested Vectored Interrupt Controller (NVIC) which controls system exceptions and peripheral interrupts. The LPC1768 supports 33 vectored interrupts, and has 32 programmable interrupt priority levels with hardware priority level masking. The tight coupling to the CPU allows for low interrupt latency, and efficient processing of late arriving interrupts.

A total of 42 pins on Port 0 and Port 2, no matter their selected function, can be programmed to generate an interrupt on a rising edge, a falling edge, or both. Each enabled interrupt can be used to wake up the chip from Power-down mode.

Power Requirements

Featuring exceptional 32-bit performance with low dynamic power, and thanks to integrated software-controlled sleep modes, extensive clock gating, and optional state retention, the M3 can deliver leading system energy efficiency.

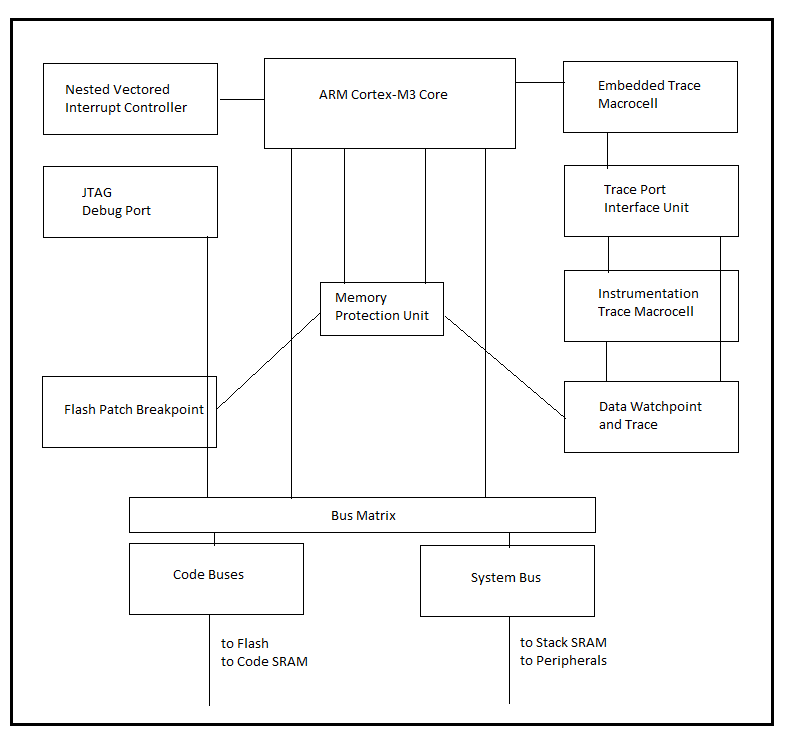
The LPC1768 has two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup Registers.

The RTC is designed to have extremely low power consumption. It will typically run from the main chip power supply, conserving battery power while the rest of the device is powered up. When operating from a battery, the RTC will continue working down to 2.1 V. Battery power can be provided from a standard 3 V Lithium button cell.

In Sleep mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

I/O pads are powered by the 3.3 V (VDD(3V3)) pins, while the VDD(REG)(3V3) pin powers the on-chip voltage regulator which in turn provides power to the CPU and most of the peripherals. A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

Block Diagram of M3 Core



Block Diagram of LPC1768

