CSE2312 (Fall 2022)
Homework #2

Notes:
With this homework, we move from abstract processor concepts to the ARM processor used on the RPi3b/3b+/4b when running 32-bit Raspberry Pi operating system.

We also start writing assembly functions for the RPi 3b/3b+/4b.

All numbers are in base-10 unless otherwise noted.

If part of a problem is not solvable, explain why in the answer area.

The target date to complete this homework set is September 13, 2022.

This homework set will not be graded, but please solve all of the problems to prepare for the quizzes and exams.

1. For each of the following operations, show the value of R0 in base-10 unsigned representation (e.g., If R0 = 16384, then R0 LSR #1 = 8192).

In the questions below, it using arithmetic operations on unsigned numbers is noted as abnormal.

For these questions, assume that the register R0 contains an unsigned 32-bit integer (e.g., uint32_t) with a value of 2048 (0x00000800).

a. R0 LSR #8: _____

b. R0 LSR #9: _____

c. R0 LSR #10: _____

d. R0 LSR #11: _____

e. R0 LSR #12: _____

f. R0 LSL #20: _____

g. R0 LSL #21: _____

h. R0 LSL #22: _____

i. R0 ASR #8: _____ (abnormal ASR usage)

For these questions, assume that the register R0 contains an unsigned 32-bit integer (e.g., uint32_t) with a value of 3758096384 (0xE0000000).

j. R0 LSL #1: _____

k. R0 LSR #1: _____

l. R0 ASR #1: _____ (abnormal ASR usage)

2. For each of the following operations, show the value of R0 in base-10 signed representation (e.g., If R0 = -64, then R0 ASR #1 = -32).

In the questions below, it using logical operations on signed numbers is noted as abnormal.

For these questions, assume that the register R0 contains a signed 32-bit integer (e.g., int32_t) with a value of -4 (0xFFFFFFFC)

R0 ASR #2: _____

R0 ASR #3: _____

R0 ASL #2: _____

R0 ASL #3: _____

R0 ASL #28: _____

R0 ASL #29: _____

R0 ASL #30: _____

R0 LSR #2: _____ (abnormal LSR usage)

Assume that the register R0 contains a signed 32-bit integer (e.g., int32_t) with a value of 8 (0x00000008).

R0 ASR #3: _____

R0 ASR #4: _____

R0 ASL #3: _____

R0 ASL #4: _____

R0 LSR #3: _____ (abnormal LSR usage)

3. For each of these C functions, specify the ARM7 register(s) in which each argument is passed and result is returned.

a. uint32_t fn4(uint16_t a, uint32_t b, int8_t c, uint32_t d)

   a is passed in: _____

   b is passed in: _____

   c is passed in: _____

   d is passed in: _____

   the result is returned in: _____

b. uint64_t fn2(uint64_t a, uint64_t b)

   a is passed in: _____

   b is passed in: _____

   the result is returned in: _____

4. Write 1-5 line assembly functions that implement the following C functions:

a. uint32_t subU32(uint32_t x, uint32_t y) // returns x-y

b. int32_t subS32(int32_t x, int32_t y) // returns x-y

c. uint64_t addU32_U64(uint32_t x, uint32_t y) // returns x+y

d. uint64_t addU64(uint64_t x, uint64_t y) // returns x+y

e. int32_t shiftRightS32 (int32_t x, uint8_t p) // returns x >> p = x*2^(-p) for p = 0..31

f. uint32_t shiftRightU32 (uint32_t x, uint8_t p) // returns x >> p = x*2^(-p) for p = 0..31

g. int32_t shiftLeftS32 (int32_t x, uint8_t p) // returns x << p = x*2^p for p = 0..31