CSE2312 (Fall 2022)
Homework #3

Notes:
With this homework, we continue writing simple assembly functions and look at the load-store instructions for the ARM processors used in the Rpi 3b/3b+/4b.

All numbers are in base-10 unless otherwise noted.

If part of a problem is not solvable, explain why in the answer area.

The target date to complete this homework set is October 4, 2022.

This homework set will not be graded, but please solve all of the problems to prepare for the quizzes and exams.

1. Write 1-5 line assembly functions that implement the following C functions:

a. int16_t maxS16(int16_t x, int16_t y) // returns the maximum of x, y

b. uint32_t maxU32(uint32_t x, uint32_t y) // returns the maximum of x, y

c. bool isGreaterThanU16(uint16_t x, uint16_t y) // returns 1 if x>y, 0 else

d. bool isGreaterThanS16(int16_t x, int16_t y) // returns 1 if x>y, 0 else

e. uint16_t shiftU16(uint16_t x, int8_t p) // return x*2^p for p = -31..31

f. bool isBitSetU32(uint32_t x, uint32_t bit) // returns 1 if the requested bit is set in x, 0 else

g. bool isMultOf4U32(uint32_t x) // returns 1 if x is an integer multiple of 4, 0 else (e.g, 0, 4, 8, 12, 16, … are integer multiples of 4)

h. bool isEqualU16(uint16_t x, uint16_t y) // returns 1 if x=y, 0 if x!=y

2. Assuming R0 contains 0x34000000, R1 contains 0xCD1258EF, R2 contains 0x00000002 and R3 contains 0x00000001, write the contents of the memory locations below after the STR instruction writes to memory, assuming that each operation is independent. If a number not known, mark the blank with an "X".

a. STR R1, [R0]; assuming little-endian convention:

Value at address 0x34000000 is _____

Value at address 0x34000001 is _____

Value at address 0x34000002 is _____

Value at address 0x34000003 is _____

b. STRH R1, [R0]; assuming little-endian convention:

Value at address 0x34000000 is _____

Value at address 0x34000001 is _____

Value at address 0x34000002 is _____

Value at address 0x34000003 is _____

c. STRB R1, [R0]; assuming little-endian convention:

Value at address 0x34000000 is _____

Value at address 0x34000001 is _____

Value at address 0x34000002 is _____

Value at address 0x34000003 is _____

d. STR R1, [R0]; assuming big-endian convention:

Value at address 0x34000000 is _____

Value at address 0x34000001 is _____

Value at address 0x34000002 is _____

Value at address 0x34000003 is _____

e. STRH R1, [R0]; assuming big-endian convention:

Value at address 0x34000000 is _____

Value at address 0x34000001 is _____

Value at address 0x34000002 is _____

Value at address 0x34000003 is _____

f. STRB R1, [R0]; assuming big-endian convention:

Value at address 0x34000000 is _____

Value at address 0x34000001 is _____

Value at address 0x34000002 is _____

Value at address 0x34000003 is _____

g. STRB R1, [R0, R3]; assuming big-endian convention:

Value at address 0x34000000 is _____

Value at address 0x34000001 is _____

Value at address 0x34000002 is _____

Value at address 0x34000003 is _____

h. STRH R1, [R0, R2]; assuming little-endian convention:

Value at address 0x34000000 is _____

Value at address 0x34000001 is _____

Value at address 0x34000002 is _____

Value at address 0x34000003 is _____

3. Assuming the memory locations contain the data below.

Address	Data
0x53400000	0x23
0x53400001	0x58
0x53400002	0x32
0x53400003	0x8B
0x53400004	0x9A
0x53400005	0xCD
0x53400006	0xDE

What is the value of R0 (all 32-bits in hex) after each of the following instructions executes assuming big-endian convention:

a. LDR R0, [R1] assuming R1 = 0x53400000

b. LDRH R0, [R1, R2] assuming R1 = 0x53400000 and R2 = 2

c. LDRSH R0, [R1] assuming R1 = 0x53400004

d. LDRB R0, [R1] assuming R1 = 0x53400005

e. LDRSB R0, [R1] assuming R1 = 0x53400006

f. LDRSB R0, [R1, R2] assuming R1 = 0x53400000 and R2 = 3