TU Berlin WiSe 2014/2015

Computer Arithmetics

Lab Assignment 2: Moving Average Filter

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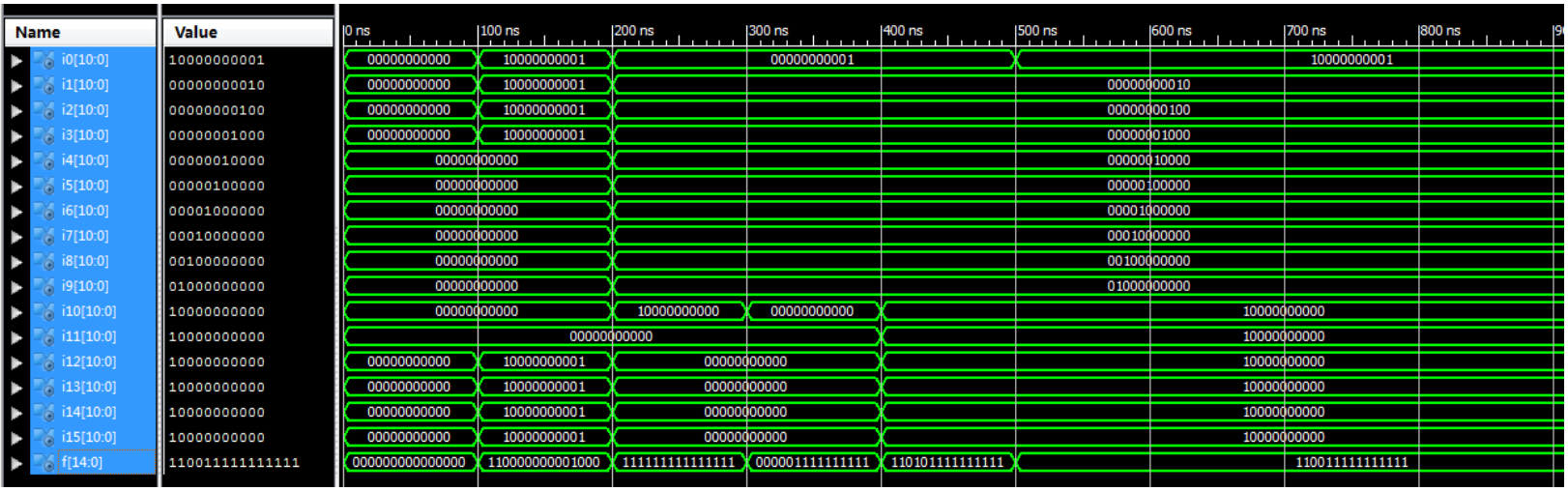
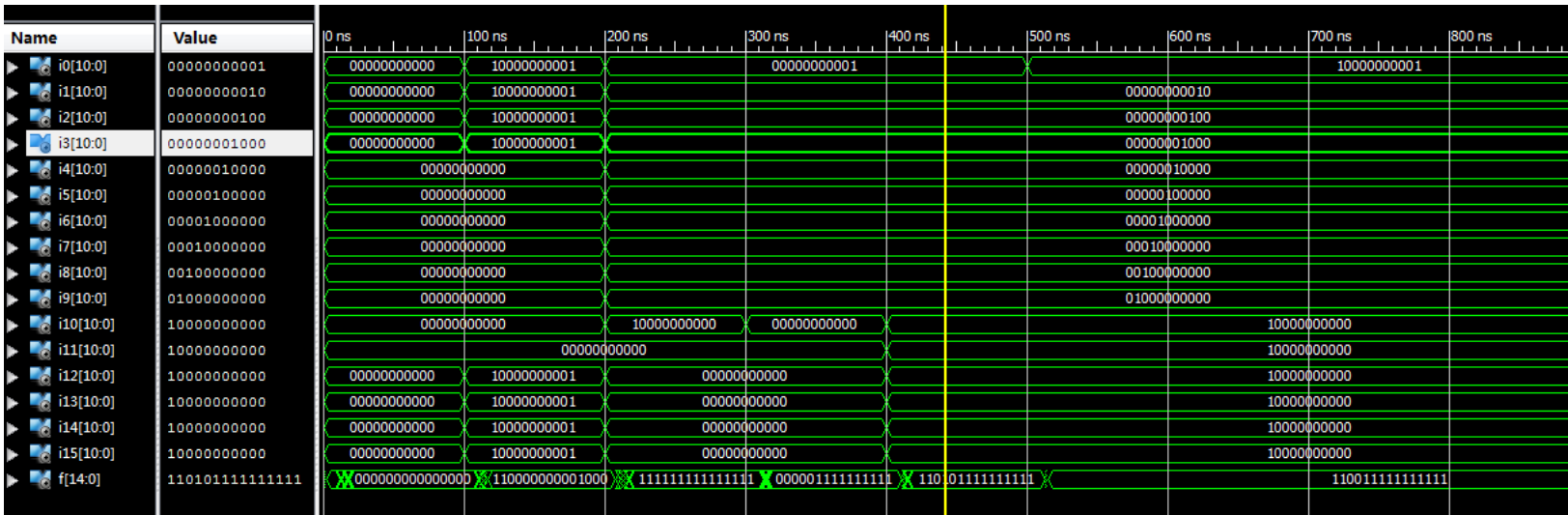
A1) The waveform for the 16bit Carry Save Adder:

Behavior:

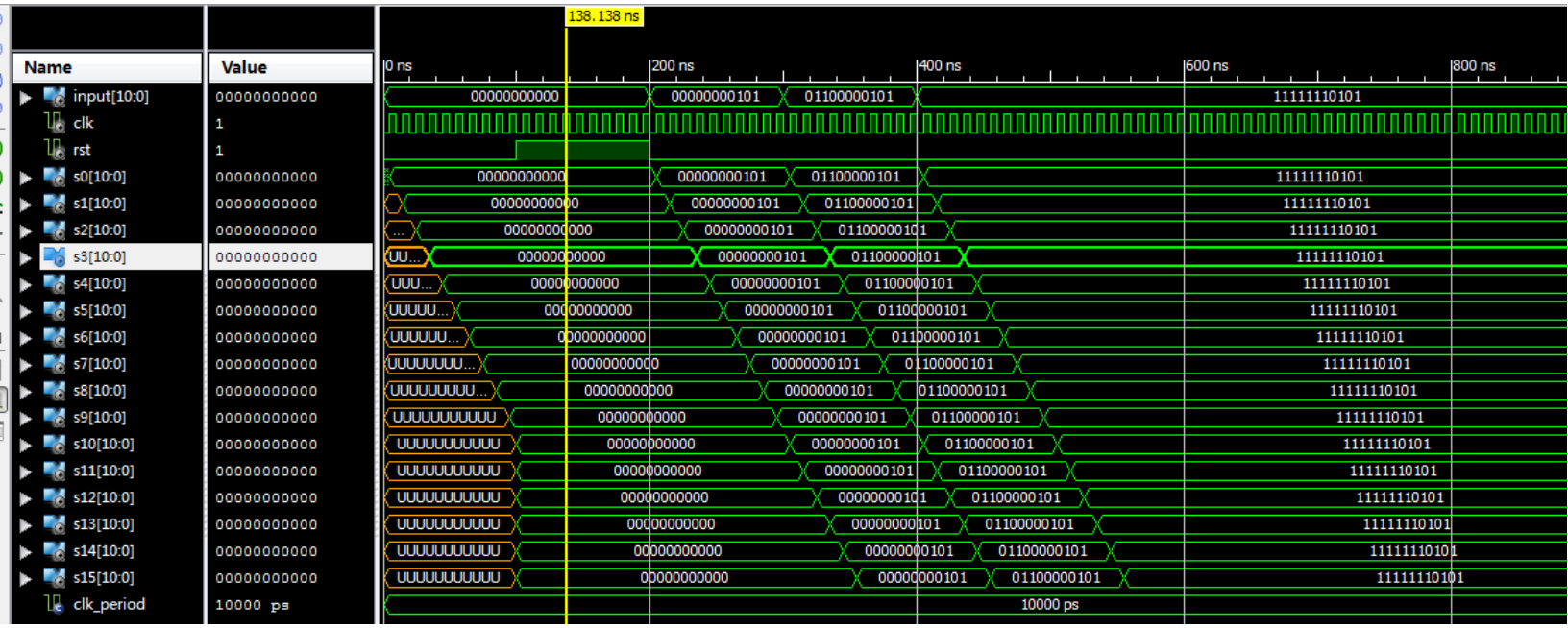


Post Place & Route:

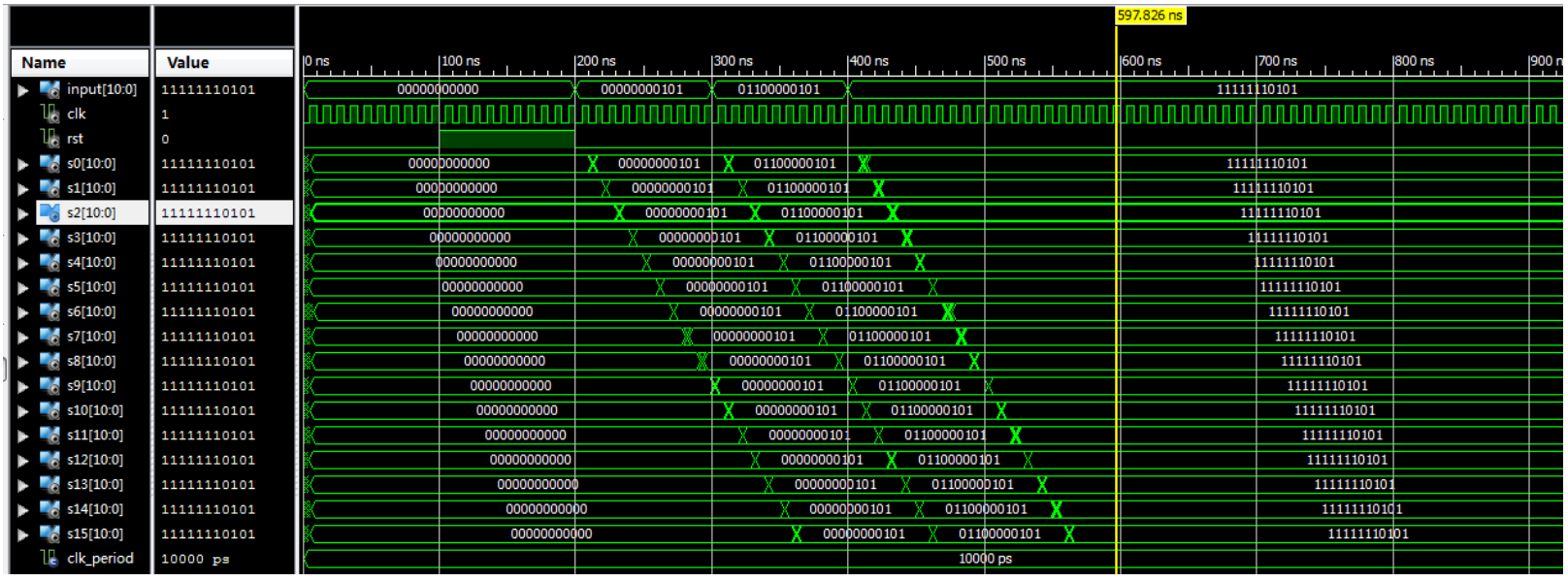


A2) The waveform for the Register:

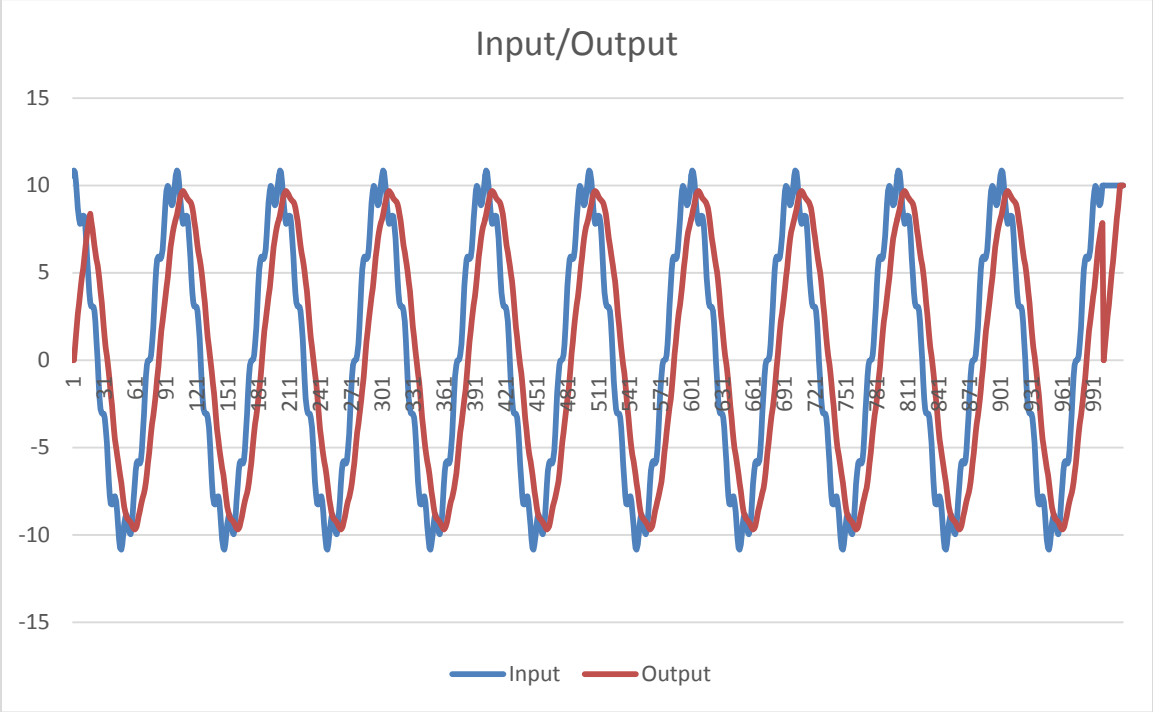
Behavior:



Post Place & Route:



B) Input and output plot diagram:



Frequency analysis:

According to the software ISE, we have the following values

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Data Sheet report:
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All values displayed in nanoseconds (ns)

Setup/Hold to clock clk
------------+------------+------------+------------------+--------+
            |Max Setup to|Max Hold to |                  | Clock  |
Source      | clk (edge) | clk (edge) |Internal Clock(s) | Phase  |
------------+------------+------------+------------------+--------+
sin<0>      |    0.486(R)|    0.738(R)|clk_BUFGP         |   0.000|
sin<1>      |   -0.054(R)|    1.169(R)|clk_BUFGP         |   0.000|
sin<2>      |    0.053(R)|    1.089(R)|clk_BUFGP         |   0.000|
sin<3>      |   -0.451(R)|    1.492(R)|clk_BUFGP         |   0.000|
sin<4>      |   -0.418(R)|    1.461(R)|clk_BUFGP         |   0.000|
sin<5>      |   -0.490(R)|    1.519(R)|clk_BUFGP         |   0.000|
sin<6>      |    0.594(R)|    0.655(R)|clk_BUFGP         |   0.000|
sin<7>      |   -0.234(R)|    1.318(R)|clk_BUFGP         |   0.000|
sin<8>      |    0.718(R)|    0.557(R)|clk_BUFGP         |   0.000|
sin<9>      |    0.885(R)|    0.424(R)|clk_BUFGP         |   0.000|
sin<10>     |    0.924(R)|    0.395(R)|clk_BUFGP         |   0.000|
------------+------------+------------+------------------+--------+
```

Clock clk to Pad

Destination	clk (edge) to PAD	Internal Clock(s)	Clock Phase
sout<0>	18.678(R)	clk_BUFGP	0.000
sout<1>	19.711(R)	clk_BUFGP	0.000
sout<2>	20.910(R)	clk_BUFGP	0.000
sout<3>	22.196(R)	clk_BUFGP	0.000
sout<4>	23.163(R)	clk_BUFGP	0.000
sout<5>	23.770(R)	clk_BUFGP	0.000
sout<6>	25.433(R)	clk_BUFGP	0.000
sout<7>	26.511(R)	clk_BUFGP	0.000
sout<8>	28.697(R)	clk_BUFGP	0.000
sout<9>	30.037(R)	clk_BUFGP	0.000
sout<10>	30.497(R)	clk_BUFGP	0.000

From them, we could expect a period of:

T = 30.497 + 0.490 = 30.987 ns

And this is satisfied for maximum frequency which is showed in the slid (10MHz).

In reality, a higher period is needed in some case.