TU Berlin
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Computer Arithmetic: Circuit Perspectives

LAB Assignment 4:

Aim

In this lab assignment, we will implement a 23x23 bits floating point multiplier, according to the following block diagram:

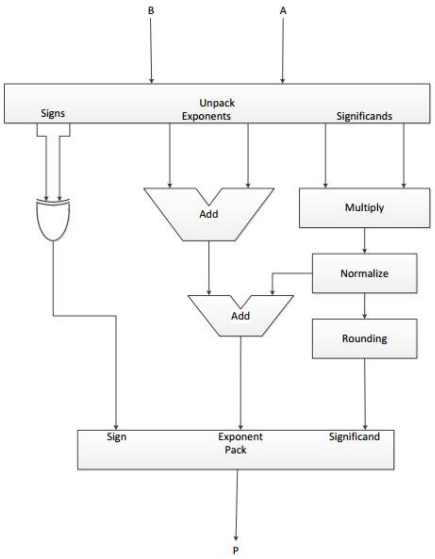

Figure 1 Floating Point Number Multiplier

Implementation

Compared to the advised implementation of the subject, our project have the following differences:

- We used CLA adders instead of CSA since we already had a functioning implementation for the CLA.
- We used the first adder to add the two biased exponents and take in account the carry from the normalization, and the second one to subtract 127 by adding it's two's complemented binary value, "10000001".
- To check for overflows and underflows, we simply look at the most significant bits of the biased exponents and compare them to the most significant bit of the resulting exponent.

Simulation results

We got the following waveforms for our multiplier, in behavioral and post route modes.

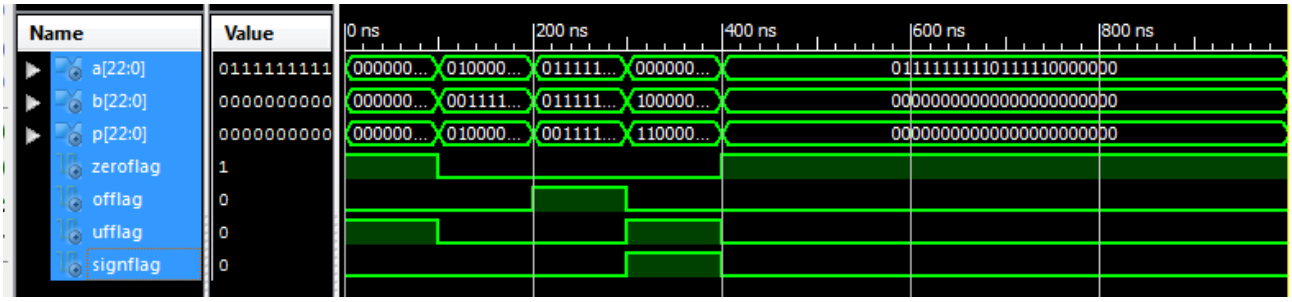

Figure 1- Behavioral simulation

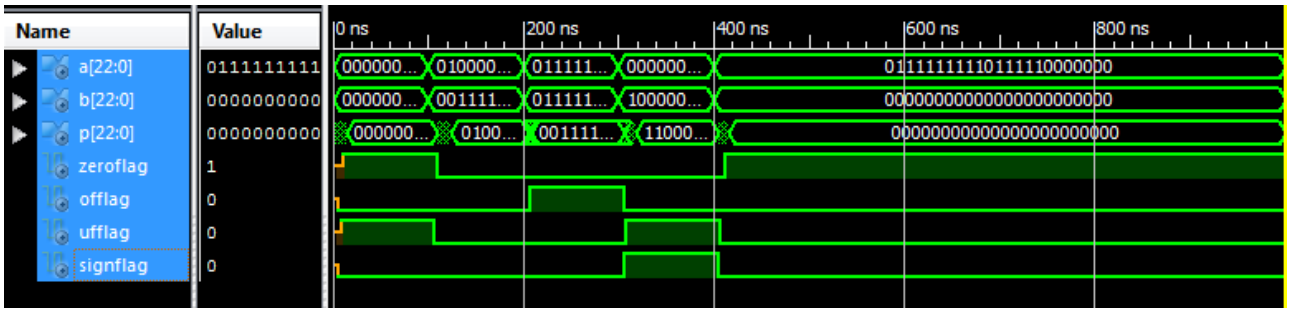

Figure 2- Post route simulation

We can see that all flags are properly working, and notice a slight delay of approximately 15 ns in post route simulation for generating the output.

Performance analysis

According to the timing report, the critical path delay is of 33,000 ns, between the pins B(12) and the over-flow flag. From this, we can calculate the maximum frequency at which we can operate the systems, which is $f = \frac{1}{critical\ path\ delay} = 0.0303\ GHz$

The device utilization is summarized in the table below:

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	474	9,312	5%	
Number of occupied Slices	248	4,656	5%	
Number of Slices containing only related logic	248	248	100%	
Number of Slices containing unrelated logic	0	248	0%	
Total Number of 4 input LUTs	474	9,312	5%	
Number of bonded IOBs	73	232	31%	
Average Fanout of Non-Clock Nets	3.70			

Figure 3 - Device utilization summary