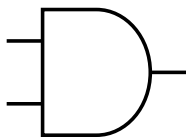


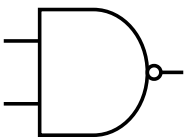
Logic Gates

Kai
2025



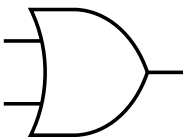
AND

input	output
0 0	0
0 1	0
1 0	0
1 1	1



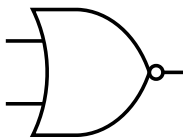
NAND

input	output
0 0	1
0 1	1
1 0	1
1 1	0



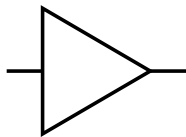
OR

input	output
0 0	0
0 1	1
1 0	1
1 1	1



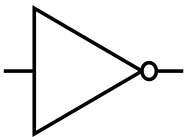
NOR

input	output
0 0	1
0 1	0
1 0	0
1 1	0



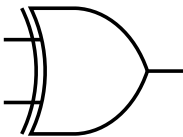
buffer

input	output
0	0
1	1



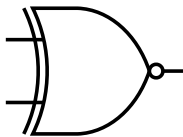
NOT

input	output
0	1
1	0



XOR

input	output
0 0	0
0 1	1
1 0	1
1 1	0

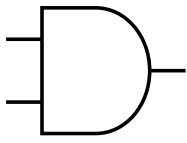


XNOR

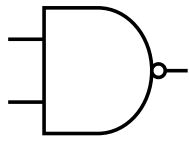
input	output
0 0	1
0 1	0
1 0	0
1 1	1

Log tables: pg 78

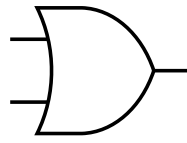
NAND = not AND
 XOR = exclusive OR
 buffer = does nothing
 NOT = inverter



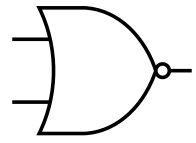
input	output



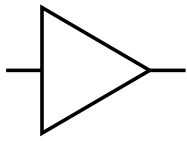
input	output



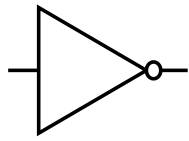
input	output



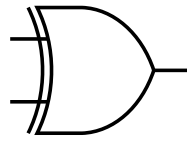
input	output



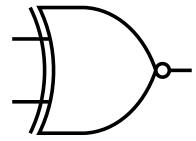
input	output



input	output

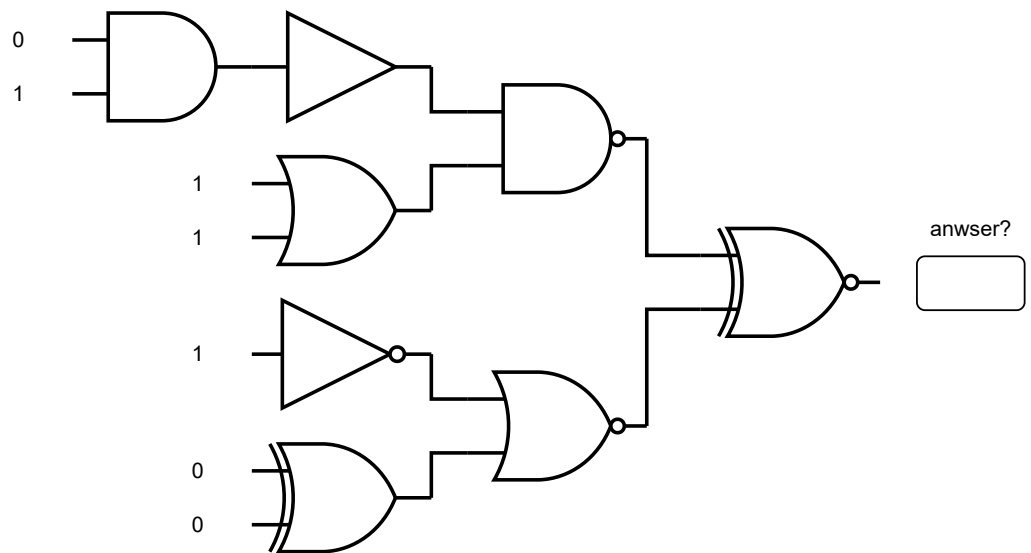


input	output



input	output

my own questions:

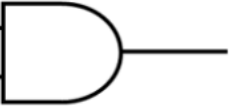
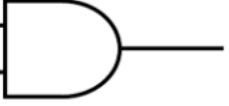
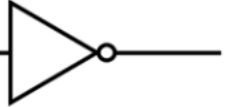
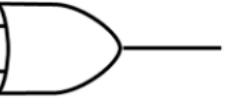
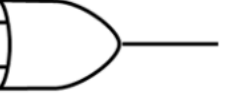
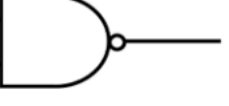


Draw an inverter:	Draw an OR gate:	Draw an exclusive NOR:
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LC HL 2024

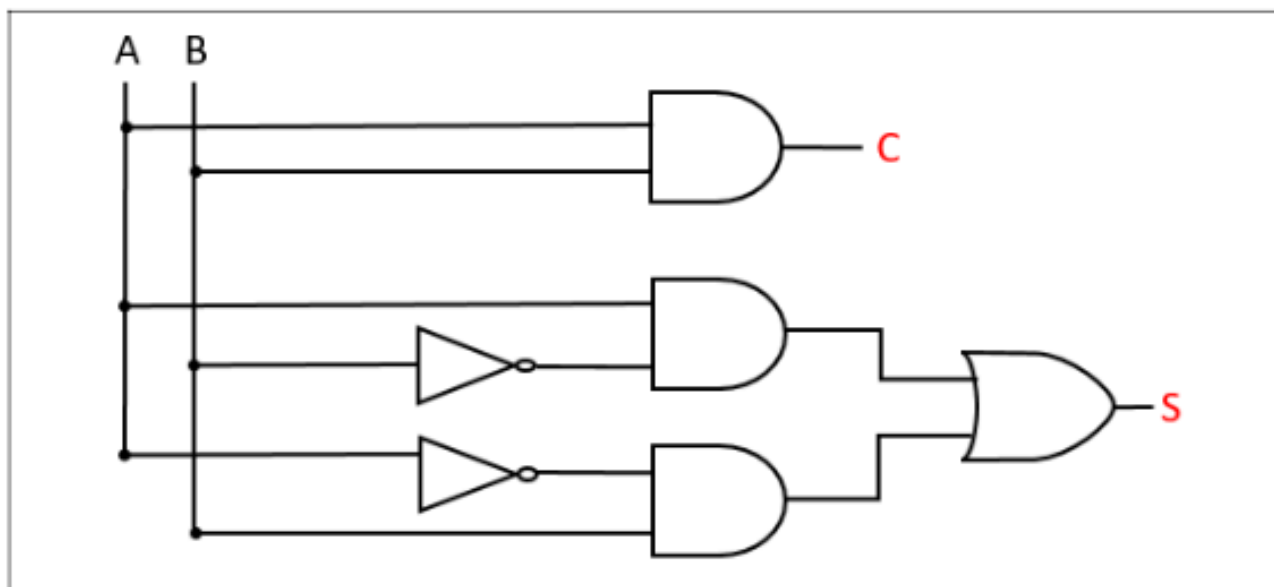
Question 1

Logic gates have one or more inputs and a single output. For each logic gate in Column A in the table below enter the output, either 0 or 1, in Column B.

Column A Logic gate with input(s)	Column B Output (0 or 1)
<div> <div>1</div> <div>1</div>  </div>	
<div> <div>0</div> <div>1</div>  </div>	
<div> <div>1</div>  </div>	
<div> <div>1</div> <div>0</div>  </div>	
<div> <div>0</div> <div>0</div>  </div>	
<div> <div>1</div> <div>1</div>  </div>	

Question 5

The half-adder logic circuit shown below generates two outputs, *S* and *C*, from two inputs, *A* and *B*.



(a) What is the value of *C* when the inputs *A* and *B* are both 0?

(b) What is the value of *S* when the inputs *A* and *B* are both 1?