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DRILL CHART: TOP to GND1				
ALL UNITS ARE IN MILLIMETERS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	0.1	+0.076/-0.1	PLATED	221

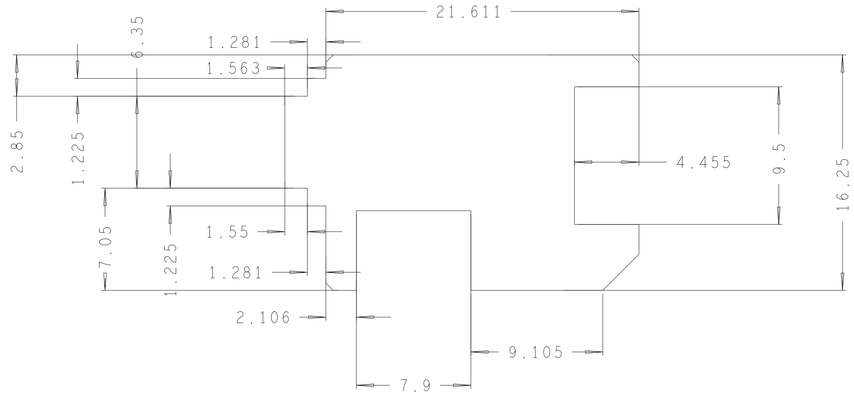
DRILL CHART: GND1 to SIGNAL_1				
ALL UNITS ARE IN MILLIMETERS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	0.1	+0.0762/-0.1	PLATED	176

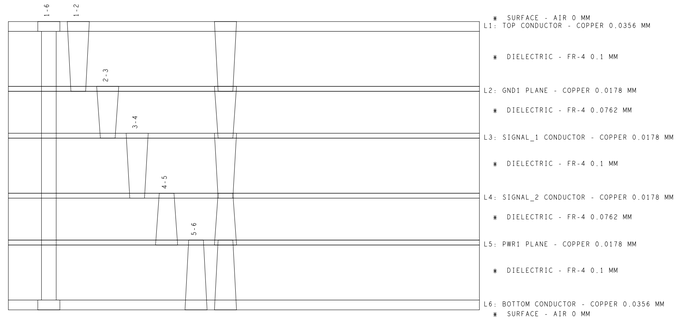
DRILL CHART: SIGNAL_1 to SIGNAL_2				
ALL UNITS ARE IN MILLIMETERS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	0.1	+0.0762/-0.1	PLATED	159

DRILL CHART: SIGNAL_2 to PWR1				
ALL UNITS ARE IN MILLIMETERS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	0.1	+0.076/-0.1	PLATED	110

DRILL CHART: PWR1 to BOTTOM				
ALL UNITS ARE IN MILLIMETERS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	0.1	+0.076/-0.1	PLATED	97

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILLIMETERS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	0.65	+0.076/-0.076	NON-PLATED	1
▬	1.1x0.5	+0.076/-0.076	PLATED	2
▫	1.3x0.6	+0.1/-0.1	PLATED	2
▬	1.5x0.5	+0.076/-0.076	PLATED	4
▯	1.6x0.6	+0.1/-0.1	PLATED	2
◦	0.95x0.65	+0.1/-0.1	NON-PLATED	1





NOTES: Unless otherwise specified

1. General Requirement:
   a. Board shall be built per IPC-A-600 and IPC-6012, class II, latest revision.
   b. Board shall be electrically tested per current revision of IPC 6012 and IPC 9252 class II. Completed electrical test Boards must be marked in permanent non-conductive ink next to supplier UL recognition mark.
   c. Configuration of the printed circuit board not specifically dimensioned on the drawing shall be controlled by the gerber data.
   d. Bow and Twist: shall not exceed .007" per inch.
   e. Fabrication Tolerances: end product trace widths and lands shall not vary more than the smaller of .001" or 20% of the trace width from the gerber data.
   f. PCB fabrication process and materials must be compliant with the Hazadous Substances (RoHS) Directive and compatible with Pb Free assembly process.
   g. Theiving is allowed on all layers with 0.050" squares on 0.100" pitch and 0.100" min away from any designed features (i.e. vias, pads, traces, etc.).
2. Impedance Control:

   a .157 traces on top and bottom to be 85ohm +/- 10%
   b. .1016mm traces on internal layers 3 and 4 to be 85ohm +/- 10%

3. Material:
   a. Glass epoxy, natural color, laminated polyclad 370hr. Tg of 170C minimum. The final thickness measured over plating to be 0.60 MM, +/- 10%.
4. Surface Finish:
   a. All external metal finish not covered by soldermask shall be plated 118 - 250 microinches of Electroless Nickel and 2 - 8 microinches of Immersion Gold (ENIG).
5. Via:
   a. All non test point top side vias to be encroached (hole size +5 mils) with soldermask.
   b. All non test point bottom side vias to be encroached (hole size +5 mils) and post plug after ENIG process.
   c. All vias to be plugged.
   d. All BGA vias and test points vias are to be free of soldermask.
   e. Tangency is allowed on vias provided tear dropping is applied to the entry of the trace to the pad. All other plated holes shall have a minimum annular ring of .001".
6. Drilling:
   a. All hole symbols may not be shown in the drawing. See Drill chart for details.
   b. Diameters in the drill table are finished hole sizes with +/-0.003" tolerance unless otherwise specified in the drill table.
7. Marking:
   a. Soldermask,photo-imaged liquid polymer on both sides of boards in accordance with IPC-SM-840, Type B, Class 2, over bare copper. Soldermask color to be White.
   b. Component Marking: Silkscreen Bottom side with black, non-conductive epoxy ink. Lands and exposed plated areas to be free of ink.

UNLESS OTHERWISE SPECIFIED	Google
DIMENSIONS ARE IN METRIC TOLERANCES ON: DIMENSIONS +/- .05 ANGLES +/- 5°	TWINKIE
	FAB DRAWING
	SIZE D · DWG NO 180-10114 · REV 04

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