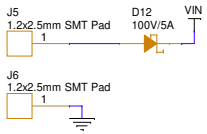
Power Entry (VIN=12-42V)

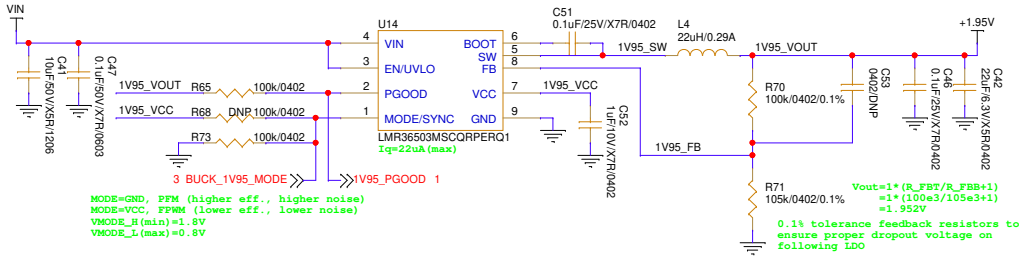


Total Sleep Mode VIN Iq:
LMR36503-Q1 (+1.95V active): 22uA
LMR36503-Q1 (+10V shutdown): 1.6uA
LM5156 (DIS_PVDD shutdown): 5uA
PXN040-100QSJ (half-bridge Idss leakage): 3uA*2
STM32 current from +1.95V: TBD

22+1.6+5+3*2=34.6uA

Pd_sd=34.6uA*12V=0.415mW
Pd_sd=34.6uA*42V=1.453mW

VIN=12-42V, VOUT=1.95V, IOUT=300mA, Sequence #0



3 SMPS management provided in the HAL and BSP

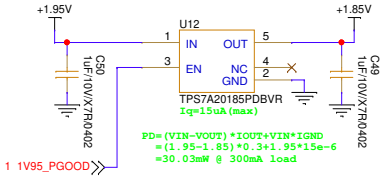
The SMPS is an external component managed by the microcontroller GPIOs, so the software functions to control it are located in the BSP (board support package). It is the responsibility of the user application to ensure that the rules described in *Section 2.2* are implemented and that the power transitions are allowed, as there is no safeguard mechanism in the HAL or the BSP.

The SPMS pins are defined in *Table 4*.

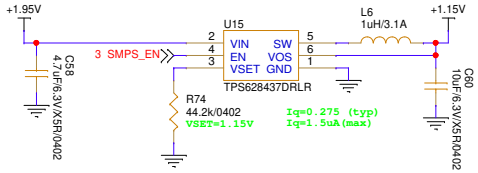
Table 4. SMPS pin definitions

Pins	Mandatory	Type	Function
SMPS_SW	Yes	Out	Control switch to enable SMPS supply on VDD12 pins
SMPS_EN	No	Out	Control SMPS on/off
SMPS_PG	No	In	Check SMPS power good
SMPS_V1	No	Out	Select SMPS voltage

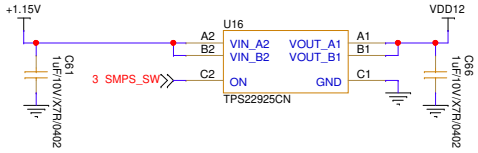
VIN=1.95V, VOUT=1.85V, IOUT=300mA, Sequence #1



VIN=1.95V, VOUT=1.15V, IOUT=0.6A, Sequence controlled by MCU



VIN=1.15V, VOUT=1.15V, IOUT=0.6A, Sequence controlled by MCU



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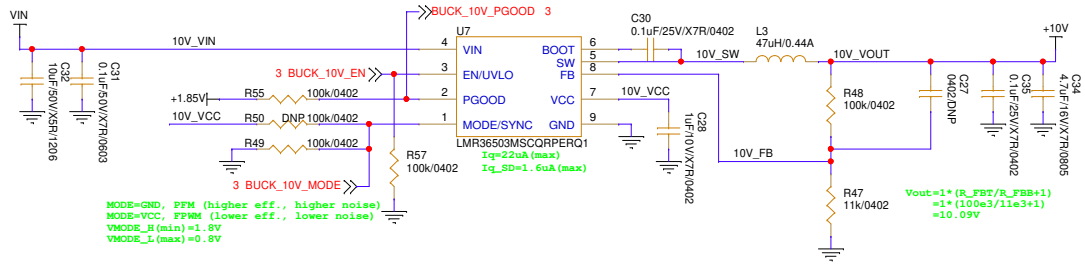
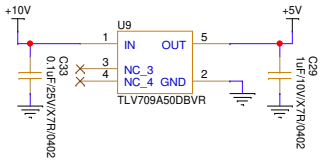
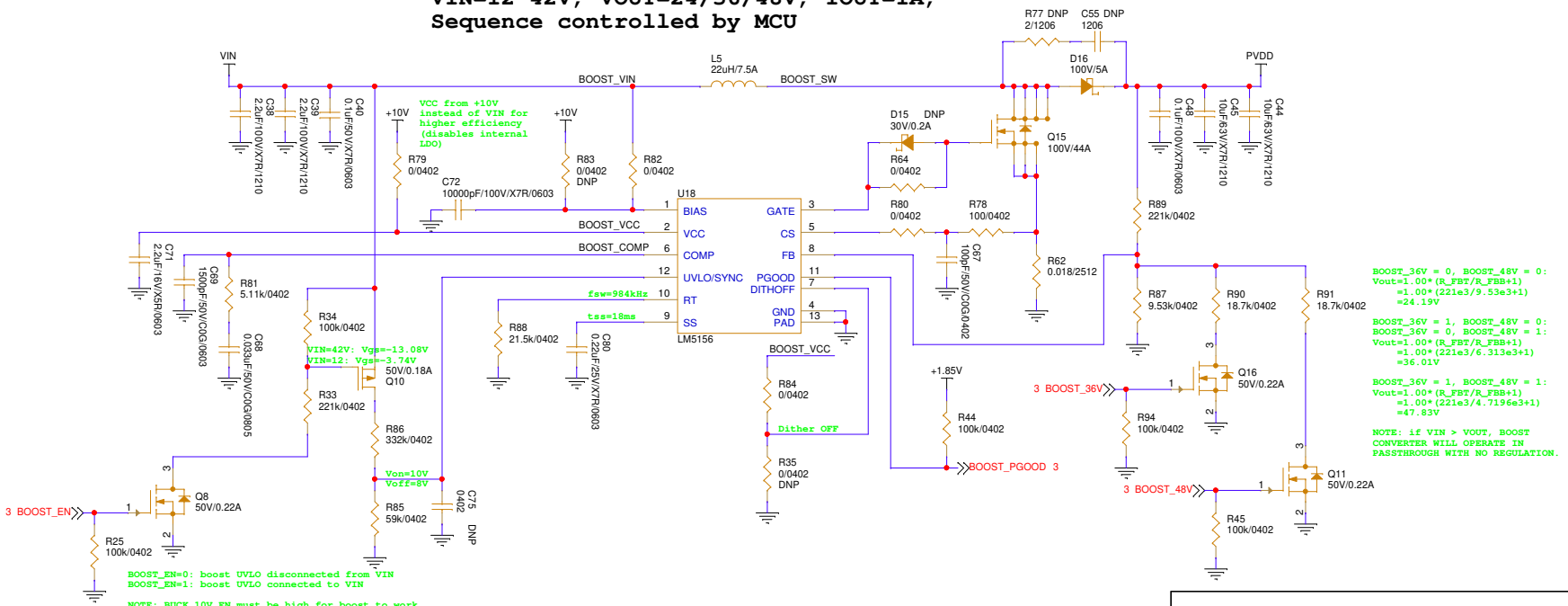
VIN=12-42V, VOUT=10V, IOUT=300mA, Sequence controlled by MCU



VIN=10V, VOUT=5V, IOUT=10mA, Sequence controlled by MCU



VIN=12-42V, VOUT=24/36/48V, IOUT=1A, Sequence controlled by MCU



Title	Amplifier Power Management	
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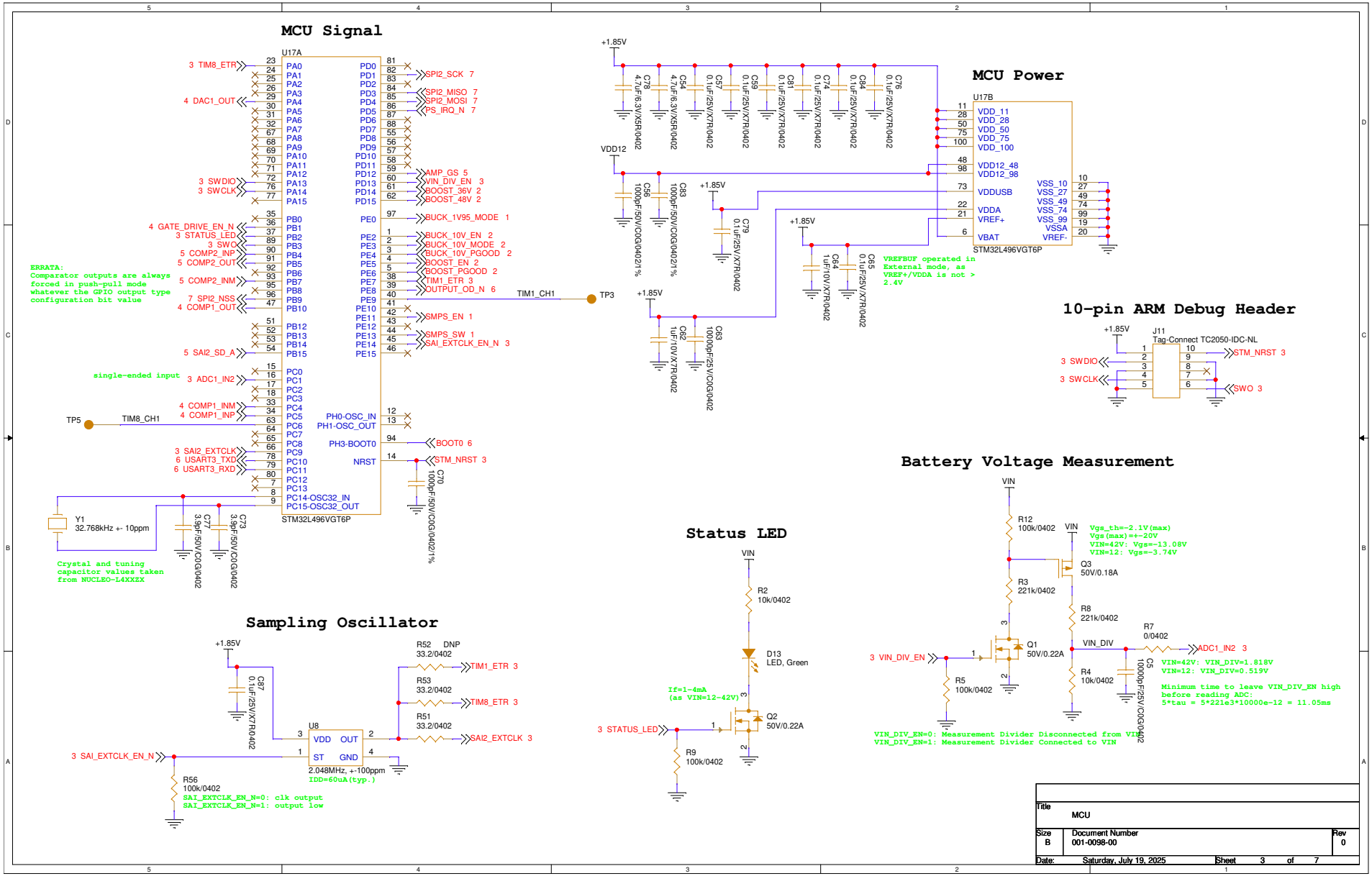
MCU Signal
U17A
STM32L496VGT6P
ERRATA:
Comparator outputs are always forced in push-pull mode whatever the GPIO output type configuration bit value
single-ended input
Crystal and tuning capacitor values taken from NUCLEO-L4XXZX
Y1
32.768kHz +- 10ppm
TP5
TP3
TIM8_CH1
TIM1_CH1
MCU Power
U17B
STM32L496VGT6P
VREFBUF operated in External mode, as VREF+/VDDA is not > 2.4V
10-pin ARM Debug Header
J11
Tag-Connect TC2050-IDC-NL
Battery Voltage Measurement
Vgs_th=-2.1V(max)
Vgs(max)=+-20V
VIN=42V: Vgs=-13.08V
VIN=12: Vgs=-3.74V
VIN=42V: VIN_DIV=1.818V
VIN=12: VIN_DIV=0.519V
Minimum time to leave VIN_DIV_EN high before reading ADC:
5*tau = 5*221e3*10000e-12 = 11.05ms
VIN_DIV_EN=0: Measurement Divider Disconnected from VIN
VIN_DIV_EN=1: Measurement Divider Connected to VIN
Status LED
If=1-4mA (as VIN=12-42V)
D13
LED, Green
Sampling Oscillator
2.048MHz, +-100ppm
IDD=60uA(typ.)
SAI_EXTCLK_EN_N=0: clk output
SAI_EXTCLK_EN_N=1: output low
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MCU
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B
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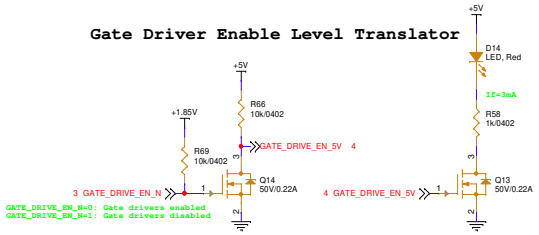
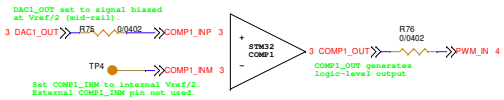
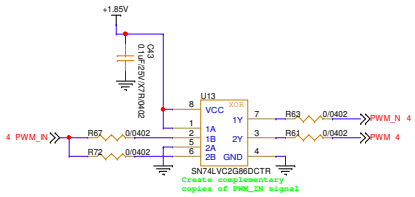
Gate Driver Enable Level Translator



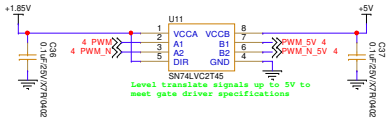
Gate Driver Signal Source



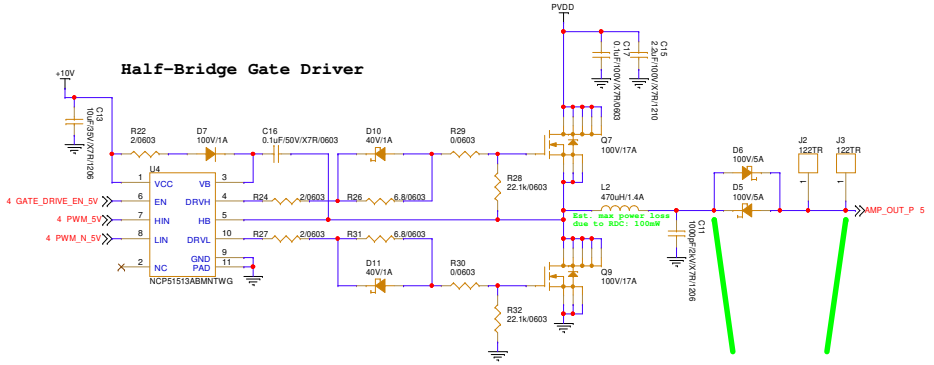
Complementary Gate Drive Generation



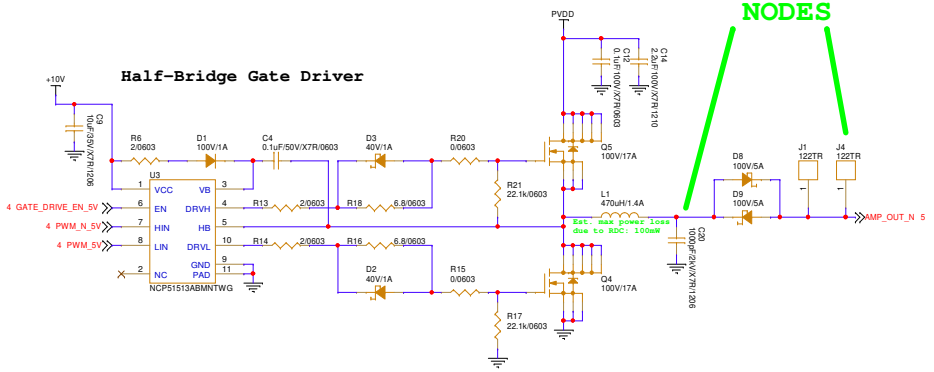
Gate Driver Level Translation



Half-Bridge Gate Driver



Half-Bridge Gate Driver



NOTE: HIGH-VOLTAGE NODES

Title	Discrete Power Stage	
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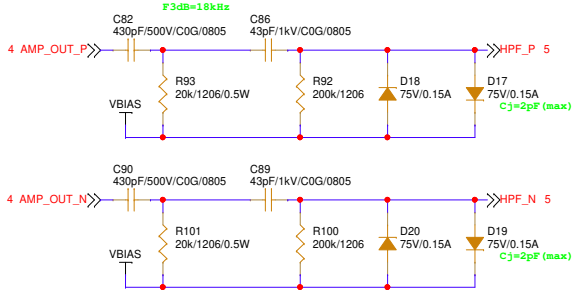
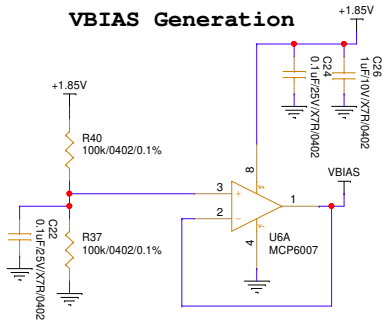
Transducer HPF & TR Clamp



VBIAS Generation



RX Connection Explanation:

The RX signal conditioning needs to present a relatively high impedance to the transducer for two reasons:

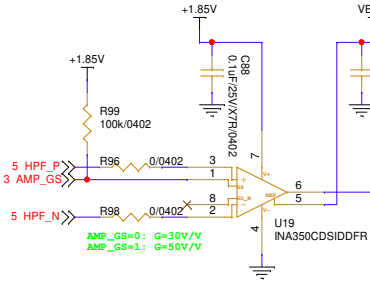
Reason1: to avoid loading down the output of the transducer in receive mode.

Reason2: to avoid presenting a short circuit when power stage is transmitting.

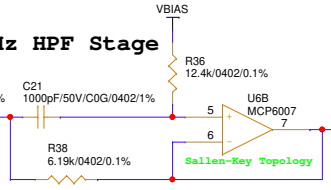
This could be done in several ways, but as this design requires reduction of low frequencies outside the TX/RX band of interest, it is accomplished by means of a two-stage cascaded RC high-pass filter.

The signal is then passed to a low-power, low-cost instrumentation amplifier, to another active HPF, and finally to the on-chip comparator of the STM32 MCU.

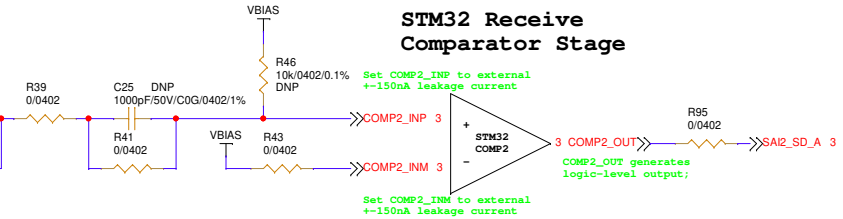
Instrumentation Amplifier



18kHz HPF Stage



STM32 Receive Comparator Stage



Title	RX Signal Conditioning	
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UART & BOOT0 Connectors

J8
1.2x2.5mm SMT Pad
1
R60 33.2/0402
USART3_RXD 3

J7
1.2x2.5mm SMT Pad
1
R59 33.2/0402
USART3_TXD 3

USART3 is used during ROM bootloader operation

NOTE: USART3 operates at +1.85V logic levels - do NOT use +3.3V UART adapter.

+1.85V
R54
10k/0402
J9
1.2x2.5mm SMT Pad
1
BOOT0_N
Q12
50V/0.18A
BOOT0 3
R42
10k/0402

BOOT0=0 / BOOT0_N=1: Flash Boot
BOOT0=1 / BOOT0_N=0: ROM Bootloader

See STMicro AN2606 for full description of ROM bootloader

BOOT0_N will float at +1.85V. Short to GND to access ROM bootloader

Open-Drain Output Level Translation

+1.85V
C19
0.1uF/25V/X7R/0402
3 OUTPUT_OD_N
U5
1 VCCA
2 A1
3 A2
5 DIR
8 VCCB
7 B1
6 B2
4 GND
SN74LVC2T45
OUTPUT_OD_N_5V 6
+5V
C18
0.1uF/25V/X7R/0402

Level translate signals up to 5V to meet low-side driver specifications

OUTPUT_OD_N=0: Output Disabled (i.e. floating high)
OUTPUT_OD_N=1: Output Enabled (i.e. pulled low)

NOTE: it is required that BUCK_10V_EN=1, otherwise the open-drain output is not functional (+5V supply is controlled by BUCK_10V_EN)

Open-Drain Power Output (Vmax=60V, Imax=1.3A)

+1.85V
R19
100k/0402
D4
75V/0.15A
J10
1.2x2.5mm SMT Pad
OUTPUT_OD
1
Q6
ZXMS6004N8-13
6 OUTPUT_OD_N_5V
R23
100k/0402

Diode-blocked pullup to +1.85V. Can be pulled up to ~60V as end-user requirements dictate.

Title: External User Interface		
Size: A	Document Number: 001-0098-00	Rev: 0
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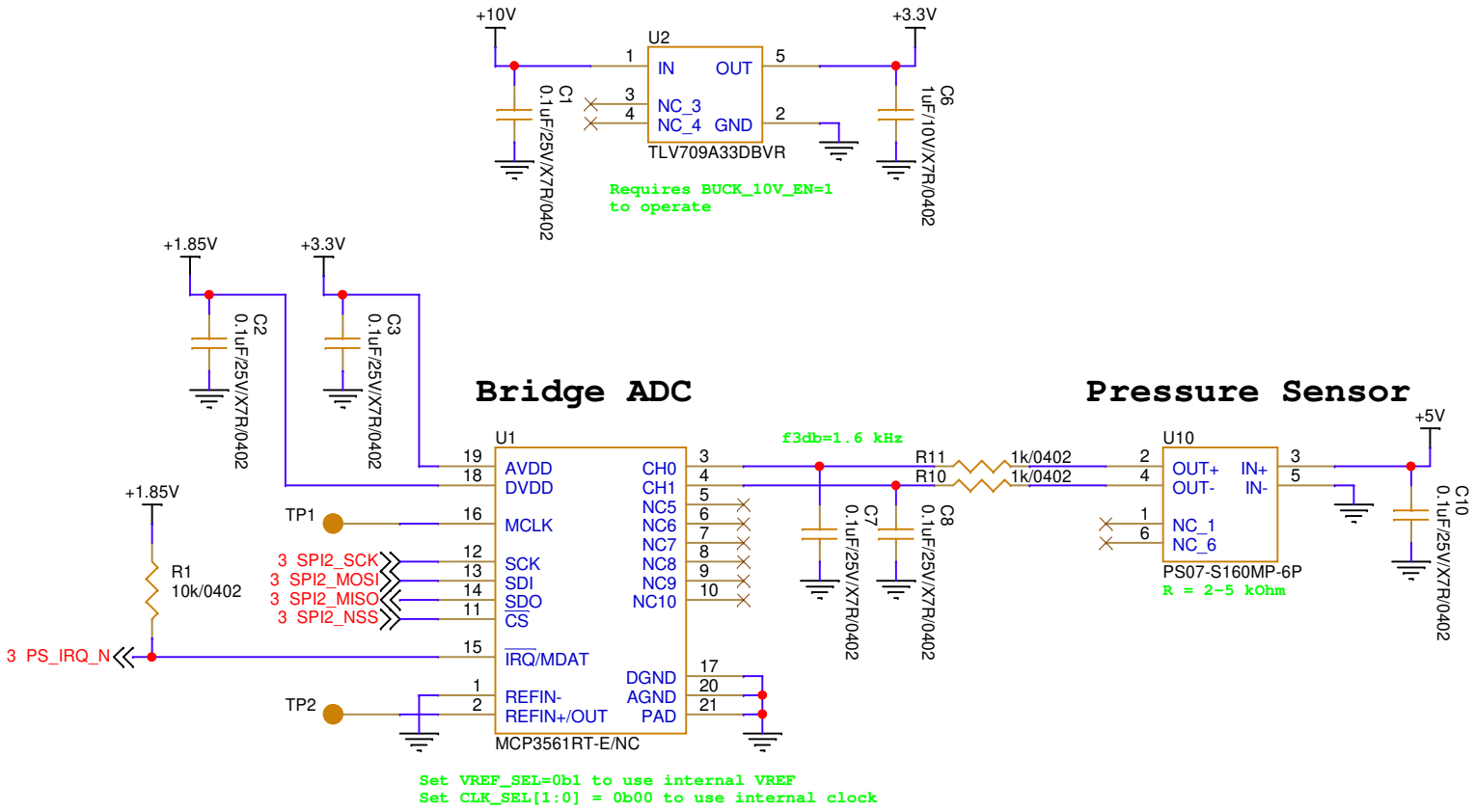
VIN=10V, VOUT=3.3V, IOUT=10mA, Sequence controlled by MCU



Title: Pressure Sensor		
Size: A	Document Number: 001-0098-00	Rev: 0
Date: Wednesday, July 23, 2025	Sheet 7 of 7	