DEVIN MAYA 3/14/24

CSE 120 Homework 6

Q1 (10 pts)

Given the following processor configuration of P1.

Assume:

- base CPI=1
- L1 hit occurs within base CPI
- L1 access time = 1 cycle (accounted for within base CPI)
- L1 miss rate = 20%
- L2 access time = 10 cycles
- L2 miss rate = 85%
- Main memory access time = 140 cycles
- 40% of instructions access L1 data cache.

a. Find the AMAT of P1 (5 pts)

b. Find the global CPI of P1 (5 pts)

Average Memory Access Time (AMAT)

Given the processor configuration for a hypothetical RISC-V processor, we calculate the AMAT as follows:

Solution

Using the provided values, the AMAT is calculated to be:

$$\begin{aligned} \text{AMAT} &= 1 + (0.20 \times (10 + (0.85 \times 140))) \\ &= 1 + (0.20 \times 129) \\ &= 1 + 25.8 \\ &= 26.8 \text{ cycles} \end{aligned}$$

Global CPI Calculation

Given the calculated AMAT and the instruction access rate to L1 data cache, the global CPI is determined as:

Solution

Incorporating the AMAT into the global CPI calculation yields:

$$\begin{aligned} \text{Global CPI} &= 1 + (0.40 \times 26.8) \\ &= 1 + 10.72 \\ &= 11.72 \end{aligned}$$

Q2 (12 pts)

For each configuration (a-c), state how many bits are needed for the following from Virtual Address:

- Physical address
- Page Offset
- Virtual page number (VPN)
- Physical page number (PPN)

a. 36-bit Virtual Address, 32-KiB pages, 24-bit Physical Address (4 pts)

b. 40-bit Virtual Address, 16-KiB pages, 2 GiB of Physical address space (4 pts)

c. 64-bit Virtual Address, 16-MiB pages, 8 GiB of Physical address space (4 pts)

Q2 Solutions

For each configuration (a-c), we calculate the bits needed for Physical address, Page Offset, Virtual page number (VPN), and Physical page number (PPN).

a. **36-bit Virtual Address, 32-KiB pages, 24-bit Physical Address**

   - Page Offset: 15 bits (2^{15} bytes for 32 KiB)
   - VPN: $36 - 15 = 21$ bits
   - PPN: $24 - 15 = 9$ bits

b. **40-bit Virtual Address, 16-KiB pages, 2 GiB of Physical address space**

- Page Offset: 14 bits (2^{14} bytes for 16 KiB)
- VPN: $40 - 14 = 26$ bits
- PPN: Since we have 2 GiB of physical space, we need 31 bits to address it, hence PPN is $31 - 14 = 17$ bits.

c. **64-bit Virtual Address, 16-MiB pages, 8 GiB of Physical address space**

  - Page Offset: 24 bits (2^{24} bytes for 16 MiB)
  - VPN: $64 - 24 = 40$ bits
  - PPN: For 8 GiB, we need 33 bits to address it, hence PPN is $33 - 24 = 9$ bits.

Q3 (16 pts)

The following list is a stream of virtual addresses as seen on a system: 0x4bff, 0x3a20, 0x3ab0, 0x7aff, 0x2cc0, 0x2124, 0x8056. Assume 4-KB pages and a four-entry fully associative TLB with LRU replacement policy.

The following table is the initial state of the TLB (before we pass the virtual address stream) with the numbers in the table being in base 10.

Valid	Tag	Physical Page #	MRU
1	11	16	2
1	7	4	3
1	3	6	4
0	4	9	1

The MRU column in the above table works as follows: The older an entry is, the lower its MRU number will be. Each time an entry is used, its MRU number is set to 4 (since it is now the most-recently used), and the other numbers are adjusted downward accordingly. For example, if the TLB row is referenced at the index shown below:

```
MRU
---
2
3  <-
4
1
```

If a TLB entry at index 2 is accessed, the MRU values are updated to reflect this access, making the entry at index 2 the most recently used:

```
MRU
---
2
4   <-
3
1
```

On a TLB Miss (due to a tag-virtual page mismatch), we would need to look for the translation in the page table. Remember that we use the virtual page number to index the page table. The following table is the initial state of the Page Table (before we pass the virtual address stream) with the numbers in the table being in base 10.

Initial Page Table:

Index	Valid	Physical Page # or On Disk
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	11
6	0	Disk
7	1	4
8	0	Disk
9	0	Disk
10	1	3
11	1	16 (largest PPN)

On a Page Fault, the pages must be brought in from disk and assigned the next largest unused Physical page number (i.e., starting at 17 in our case). The following questions below are based on the above information:

a. Fill out the table below indicating a TLB Hit, Miss, or Page Fault for each successive virtual address reference. (7 pts) **Address Reference Outcomes:**

Address	Result (H, M, PF)
0x4bff	M
0x3a20	H
0x3ab0	H
0x7aff	H
0x2cc0	PF
0x2124	M
0x8056	PF

b. Show the final state of the TLB and Page table after accessing all 7 virtual address references. Both tables MUST show the correct value of all column entries. (9 pts)

Final State of TLB and Page Table

TLB Table (Final State):

Valid	Tag	Physical Page #	MRU
1	0x2cc	17	4
1	0x212	18	3
1	0x805	19	2
1	0x7af	4	1

Final Page Table:

Index	Valid	Physical Page # or On Disk
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	11
6	0	Disk
7	1	4
8	0	Disk
9	0	Disk
10	1	3
11	1	16
12	1	17
13	1	18
14	0	Disk
15	1	19