VLSIFlow

ASIC Design

INTERVIEW QUESTIONS

1. What is Body Effect? The threshold voltage of a MOSFET is influenced by the voltage applied to its bulk
(back contact). The voltage difference between the source and bulk (VBS) changes the width of the depletion region, thus affecting the threshold voltage. **2. What are Standard Cells?** In semiconductor design, standard cells are predefined blocks that represent basic
logic functions (like NAND, NOR gates) used in ASIC design. They simplify the design process by allowing designers to focus on high-level logic rather than individual components, making it easier to scale designs to complex SoCs (System on Chips).

3. What are Design Rule Check (DRC) and Layout Vs Schematic (LVS)?

- **DRC** ensures that the physical layout adheres to the design rules of the foundry.
- **LVS** ensures that the physical layout matches the schematic representation of the design. Both are crucial steps in the verification process before manufacturing.

4. What is Antenna Effect?

The antenna effect occurs when a metal layer accumulates charge during the fabrication process, which can damage the gate oxide of a transistor. It is critical to follow antenna rules to avoid these effects.

5. What are the Steps in Semiconductor Device Fabrication?

- Wafer processing: Wet cleans, photolithography, ion implantation, etching, CVD, PVD, etc.
- Die preparation: Wafer mounting, die cutting, IC packaging, bonding, encapsulation, and testing.

6. What is a Clock Distribution Network?

In synchronous digital systems, the clock distribution network ensures that the clock signal reaches all components in the system. It must deliver clean and sharp signals with minimal skew to avoid race conditions and ensure proper synchronization.

7. What is Clock Gating?

Clock gating is a technique used to save power by disabling the clock signal to portions of the circuit when not needed. This reduces unnecessary power consumption and increases efficiency.

8. What is a Netlist?

A netlist describes the connectivity of components in a circuit, specifying how different instances (components) are connected through nets (wires). It serves as the basis for further steps like simulation, verification, and layout.

9. What is Physical Timing Closure?

Physical timing closure involves modifying a design's physical layout to meet timing requirements. It ensures that all timing constraints are satisfied after placement, routing, and clock-tree synthesis, especially in submicron technologies.

10. What is Physical Verification?

Physical verification ensures that the layout conforms to the design rules. It includes DRC, LVS, XOR checks, ERC, and antenna checks to confirm that the design is manufacturable and performs as expected.

11. What is a Stuck-at Fault?

A stuck-at fault is a type of fault used in test pattern generation, where a signal or output is assumed to be permanently stuck at a logical 1 or 0. This fault model helps in identifying manufacturing defects.

12. What are Different Logic Families?

Some common logic families include:

- CMOS (Complementary Metal-Oxide Semiconductor)
- TTL (Transistor-Transistor Logic)
- ECL (Emitter-Coupled Logic)
- BiCMOS (Bipolar CMOS)
- I2L (Integrated Injection Logic)

13. What are Different Types of IC Packaging?

ICs can be packaged in various forms, including:

- BGA (Ball Grid Array)
- QFP (Quad Flat Package)
- DIP (Dual In-line Package)

- LQFP (Low-Profile Quad Flat Package)
- Flip Chip, etc.

14. What is Substrate Coupling?

Substrate coupling refers to the interference between digital and analog signals in a mixed-signal IC. It happens when signals couple through the substrate, affecting performance and creating noise, especially in RF and mixed-signal designs.

15. What is Latchup?

Latchup is a failure mode in CMOS circuits where a parasitic structure forms a short circuit between the power supply rails, leading to overcurrent and possibly device damage. A power cycle is required to reset the state.

CMOS Interview Questions & Answers

1. **What is latch-up?**
    - o Latch-up is a failure mechanism in CMOS circuits where parasitic silicon-controlled rectifiers (SCRs) form between the power rails (VDD and VSS). This leads to a short circuit and causes excessive current flow, potentially damaging the device permanently. It can occur due to improper layout or voltage spikes that trigger the parasitic elements.
2. **Why is NAND gate preferred over NOR gate for fabrication?**
    - o NAND gates are preferred over NOR gates in CMOS design because:
        - **Electron mobility** in NMOS is higher than hole mobility in PMOS, making NAND gates faster.
        - **Gate leakage** in NAND structures is lower.
        - The **delay profile** in NAND gates is more symmetric compared to NOR gates, which show significant delay differences (with high resistance in PMOS leading to higher delays in NOR).
3. **What is Noise Margin? Explain the procedure to determine it.**
    - o Noise Margin refers to the tolerance a circuit has to noise on its input signals before it affects the output. To determine it, evaluate the voltage levels of a logic gate at the input and output, then compute the difference between the input voltage that would cause a logical change and the output voltage levels that indicate a change.

4. **Explain sizing of the inverter.**

   - Inverter sizing involves adjusting the width of the NMOS and PMOS transistors to match the desired load capacitance and achieve the desired rise/fall time. The goal is to optimize speed, power, and area by balancing the transistor widths.

5. **How do you size NMOS and PMOS transistors to increase the threshold voltage?**

   - To increase the threshold voltage (Vth), you can adjust the transistor's channel length or modify the doping concentrations in the channel. Increasing the size (width) of the PMOS relative to NMOS can also help balance the output characteristics, but Vth specifically relates to process and material changes.

6. **What happens to delay if you increase load capacitance?**

   - Increasing load capacitance increases the delay because more charge needs to be transferred to switch the output state. This requires more time to charge/discharge the capacitance.

7. **What happens to delay if we include a resistance at the output of a CMOS circuit?**

   - Including resistance at the output increases the delay (RC delay) because the resistance adds to the time it takes to charge or discharge the capacitance at the output, thereby slowing down the signal transition.

8. **What are the limitations in increasing the power supply to reduce delay?**

   - While increasing the power supply can reduce delay, it also leads to higher power dissipation and excessive heat generation. This requires increasing the die size to dissipate the heat, which is not always practical.

9. **How does resistance of metal lines vary with increasing thickness and increasing length?**

   - The resistance (R) of metal lines is given by R=ρ·lAR = \frac{\rho \cdot l}{A}, where ρ\rho is resistivity, ll is the length, and AA is the cross-sectional area. As the length increases, resistance increases; as the thickness increases, resistance decreases due to the larger cross-sectional area.

10. **For CMOS logic, what techniques can minimize power consumption?**

- Techniques include minimizing load capacitance, lowering the supply voltage (Vdd), and reducing the operating frequency. Additionally, using dynamic power management techniques and optimizing circuit layout to reduce unnecessary switching can help reduce power consumption.

11. **What is charge sharing? Explain the charge sharing problem while sampling data from a bus.**

    - Charge sharing occurs when two or more capacitive nodes share charge, leading to incorrect voltage levels. This is problematic when sampling data from a bus, as the charge from the bus could be redistributed across multiple nodes, resulting in a mismatch of logical levels. This can be minimized by ensuring that the load capacitance is significantly larger than the input capacitance.

12. **Why do we gradually increase the size of inverters in buffer design? Why not give the output of a circuit to one large inverter?**

    - A single large inverter cannot efficiently drive a large capacitive load. Gradually increasing the size of the inverters (i.e., using multiple stages) allows for better performance by balancing the drive capabilities of each stage and preventing the signal from being degraded by excessive capacitance or slow transitions.

13. **What is latch-up? Explain latch-up with the cross section of a CMOS inverter. How do you avoid latch-up?**

    - Latch-up occurs when parasitic transistors in the CMOS structure form a conductive path between VDD and VSS, causing excessive current to flow. This is typically avoided by using proper layout techniques, ensuring proper spacing between transistors, and using guard rings to prevent triggering parasitic elements.

14. **Give the expression for CMOS switching power dissipation.**

    - The CMOS switching power dissipation is given by P=C·V2·fP = C \cdot V^2 \cdot f, where CC is the load capacitance, VV is the supply voltage, and ff is the switching frequency.

15. **What is body effect?**

    - Body effect refers to the variation in the threshold voltage (Vth) of a MOSFET due to the voltage difference between the body (substrate) and the source. As the source-to-body voltage increases, the threshold voltage increases, which can affect the performance of the device.

16. **Why is the substrate in NMOS connected to ground and in PMOS to VDD?**

    - The substrate in NMOS is connected to ground to ensure the source-substrate junction is reverse biased, preventing current from leaking into the substrate. Similarly, the PMOS substrate is connected to VDD to maintain the reverse bias between the source and the substrate.

17. **What is the fundamental difference between a MOSFET and BJT?**

    - The MOSFET is a voltage-controlled device where current flows due to electrons (NMOS) or holes (PMOS), while the BJT is a current-controlled device that relies on both electron and hole movement for current conduction.

18. **Which transistor has higher gain: BJT or MOS and why?**

    - BJTs have higher gain because their current is exponentially related to the input voltage, providing higher transconductance. In contrast, MOSFETs follow a square law relationship, which results in lower transconductance.

19. **Why do we gradually increase the size of inverters in buffer design when trying to drive a high capacitive load? Why not give the output of a circuit to one large inverter?**

    - Gradually increasing the size ensures that each stage is capable of driving its respective load while minimizing the overall delay. A large inverter would require excessive time to charge or discharge the large load capacitance, slowing down the signal.

20. **In CMOS technology, why do we design the size of PMOS to be higher than NMOS?**

    - PMOS transistors have lower mobility for charge carriers (holes) compared to NMOS transistors (electrons). To achieve balanced rise and fall times, the PMOS transistor is sized larger to compensate for its slower charge accumulation and discharge characteristics.

21. **Why PMOS and NMOS are sized equally in transmission gates?**

    - In transmission gates, both PMOS and NMOS transistors work together to pass a signal, and their roles are complementary. Therefore, they are sized equally to maintain symmetry and avoid distortion in the transmitted signal.

22. **What happens when the PMOS and NMOS are interchanged in an inverter?**

o Interchanging PMOS and NMOS transistors in an inverter will result in incorrect logic behavior. The inverter may still function as a buffer, but the output logic levels will be degraded, and the voltage transitions will not properly represent the input logic.

23. **What are the five important design techniques to follow when doing a layout for digital circuits?**

- Ensure consistent height for standard cells.
- Use metal layers in a consistent direction for routing (horizontal or vertical).
- Maximize the use of substrate contacts in empty spaces.
- Avoid using poly over long distances due to high resistance.
- Maintain symmetry in the design for ease of routing and performance optimization.

24. **What is metastability? When/why does it occur and how can it be avoided?**

o Metastability occurs when a flip-flop or latch does not settle into a stable state within the required time, often due to setup or hold time violations. It can be avoided by using multiple flip-flops in series (typically 2-3) to filter out intermediate states and ensure stable operation.

25. **In a NAND gate, if signal A arrives later than signal B, which one should be placed closer to the output for optimal delay?**

o The signal that arrives later (A) should be placed closer to the output to minimize delay, as it will have less impact on the speed of the overall gate.

digital design interview questions and answers for VLSI and ASIC roles:

1) Explain setup time and hold time. What will happen if there are setup time and hold time violations? How can these be overcome?

- **Setup time** is the minimum time before the clock edge that the input signal must remain stable to be reliably captured.
- **Hold time** is the minimum time after the clock edge that the input signal must remain stable.

- If there are **setup time violations**, the data is not captured correctly because it changes too close to the clock edge.
- If there are **hold time violations**, the data might change too soon after the clock edge, leading to incorrect data capture.
- **Overcoming violations**: These can be mitigated by reducing the clock period, improving timing margins, or increasing the size of buffers or flip-flops to ensure proper data setup and hold times.

2) What is skew, what are the problems associated with it, and how can you minimize it?

- **Clock skew** is the difference in arrival times of the clock signal at different components of the circuit.
- It can cause **timing violations** like **setup** and **hold violations** if the clock signal arrives too early or too late at certain flip-flops.
- To minimize skew, proper **clock tree design**, **balanced clock distribution**, and **delays management** should be implemented.

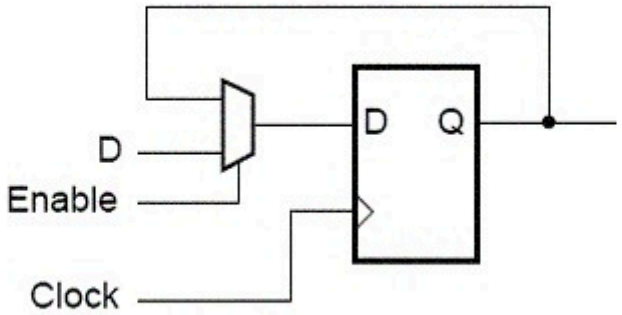
3) What is slack?

- **Slack** is the difference between the required time (when an event must occur) and the actual arrival time (when it happens).
- If slack is **positive**, the design meets the timing requirements. If it's **negative**, it indicates a timing violation.
- Slack is calculated as:
  Slack = Required Time - Actual Time.

4) What is a glitch? What causes it and how can it be overcome?

- A **glitch** is an undesired transition or change in logic state that occurs due to imperfect synchronization of signals.
- **Causes** include conflicting signals or improper timing in combinational circuits.
- **Overcoming glitches**: This can be achieved by ensuring proper synchronization, using **edge-triggered** flip-flops, and applying **deglitching** techniques like additional filtering logic.

a) Using a Feedback Path



b) Corresponding Timing Diagram

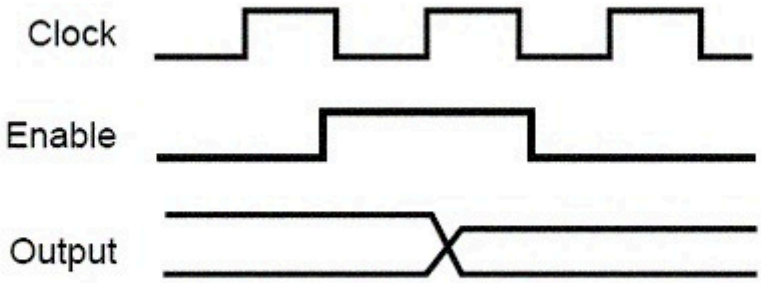


Figure 2-13: **Synchronous Design Using Data Feedback**

The following figure shows a gated clock. The gated clock's corresponding timing diagram shows that this implementation can lead to clock glitches, which can cause the flip-flop to clock at the wrong time.

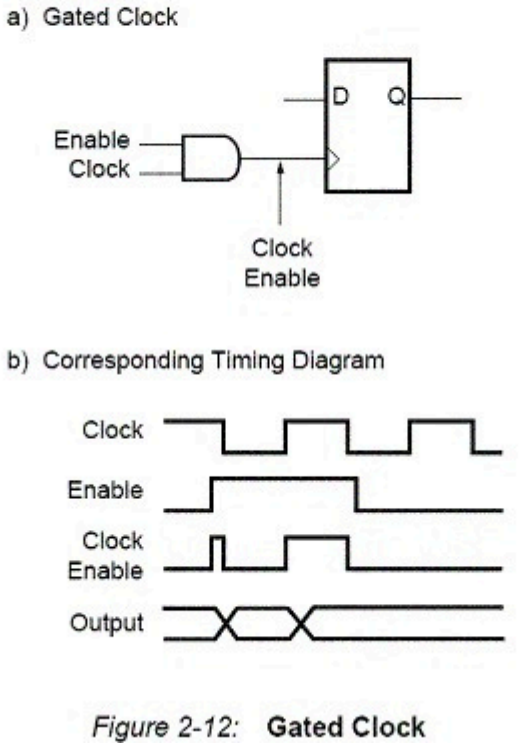


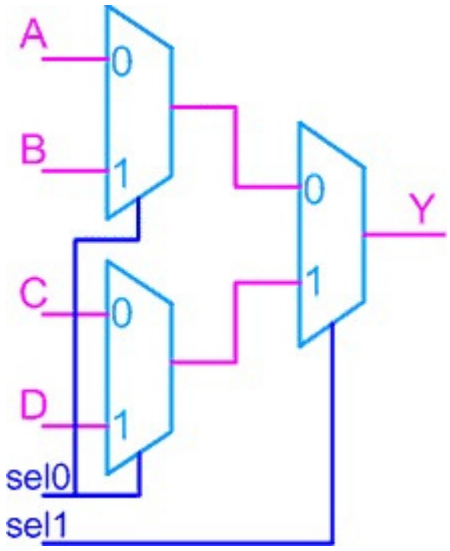
Figure 2-12: **Gated Clock**

5) What is the difference between a latch and a flip-flop?

- **Latch**: A level-sensitive device that changes state as long as the enable signal is active.
- **Flip-flop**: An edge-sensitive device that changes state only on the rising or falling edge of the clock.
- Flip-flops are typically used in sequential circuits due to their edge-triggered behavior.

6) How can you implement a 4:1 MUX using only 2:1 MUX?

- A 4:1 MUX can be implemented using three 2:1 MUXes as follows:
  - First, select two 2:1 MUXes to create two outputs (A and B).
  - Then, use another 2:1 MUX to select between the two outputs (A and B) based on the final control bit.



7) What is the difference between Mealy and Moore state machines?

- **Mealy Machine**: The output depends on both the current state and the input.
- **Moore Machine**: The output depends only on the current state.
- **Advantages**: Mealy machines can be more compact and faster because the output depends on inputs directly, whereas Moore machines avoid glitches because the output only depends on the state.

8) What is the significance of RAS and CAS in SDRAM?

- **RAS (Row Address Strobe)** and **CAS (Column Address Strobe)** are control signals used in SDRAM for addressing memory.
- **RAS** latches the row address, while **CAS** latches the column address, ensuring proper timing for accessing memory cells.

9) How can you achieve a 180-degree phase shift without using an inverter?

- A **180-degree phase shift** can be achieved using **digital clock managers (DCM)**, **phase-locked loops (PLLs)**, or specialized **differential buffers** such as **BUFDS** available in FPGAs.

10) What is the difference between binary and one-hot encoding for FSMs?

- **Binary Encoding**: Requires fewer flip-flops (log2 of the number of states) but results in a more complex combinational logic for state transitions.

- **One-hot Encoding**: Requires one flip-flop per state (i.e., for n states, you need n flip-flops). It's simpler to implement in FPGA and provides faster state transitions with less combinational logic, but uses more flip-flops.

11) How to calculate maximum operating frequency?

- The maximum operating frequency of a digital circuit is determined by the **critical path delay**, which is the longest time it takes for a signal to propagate from the input to the output.
- The maximum operating frequency (f_max) is given by:
  f_max = 1 / (Critical Path Delay).

12) How to avoid underflow or overflow in a FIFO?

- FIFO size should be chosen based on the input and output rates.
- In cases where the clock frequencies of two domains differ, the FIFO depth can be calculated using the formula: FIFO Depth = (Time interval between writes and reads) / (Time per entry).

13) How do you implement an AND gate using a MUX?

- For an AND gate, use a **2:1 MUX** where one input is connected to 0 and the other to A. The selection line should be connected to B to implement the AND logic:
  Output = A AND B.