TECHNISCHE UNIVERSITÄT DRESDEN

Faculty of Computer Science Institute for Computer Engineering, Chair for VLSI-Design, Test and Architecture

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Summerschool

Modeling and Designing Dependable Embedded Systems

— Lab 4 —

Problem 1 Implement the following **entity**:

```
entity trigger is
  generic(
    THRESHOLD : positive     -- Trigger Threshold
  );
  port(
    clk : in  std_logic;     -- Clock

    rst : in  std_logic;     -- Reset
    evt : in  std_logic;     -- Count Event
    trg : out std_logic      -- Threshold Reached
  );
end trigger;
```

so that it asserts its output trg whenever the number of observed events since startup or the most recent reset reaches the THRESHOLD parameter. An event is to be counted when the input evt is asserted at a rising clock edge.

Verify the correct operation of your design within a suitable testbench.

Problem 2 Implement the following **entity**:

```
entity collect is
  generic(
    BITS : positive          -- Number of Bits making up a Word
  );
  port(
    clk : in  std_logic;     -- Clock
    rst : in  std_logic;     -- Reset

    din  : in  std_logic;                          -- Serial Bit Input (MSB first)
    dout : out std_logic_vector(N-1 downto 0); -- Parallel Word Output
    strb : out std_logic                           -- Output Strobe
  );
end trigger;
```

which is to collect the bits from the serial input line din into a data word of the specified bit width. Whenever a data word has been completed, the assembled data word is output to dout and strb is asserted.

Verify the correct operation of your design within a suitable testbench.