TECHNISCHE UNIVERSITÄT DRESDEN

**Faculty of Computer Science** Institute for Computer Engineering, Chair for VLSI-Design, Test and Architecture

Dresden, July 1, 2014

Summerschool

# Modeling and Designing Dependable Embedded Systems

## — Lab 1 —

**Problem 1** Create a ModelSim project and a new design file `hello.vhdl`. Implement a „Hello World" application printing a hello and a goodbye message. Simulate it.

**Problem 2** Within your **architecture**, copy your main **process** into several concurrent instances. Adapt the **report**s of these **process**es so that you can identify the individual outputs. Simulate the design and determine the order of these outputs. How does it match your implementation? Explain.

**Problem 3** Force an explicit order on the outputs by introducing delta cycles. Verify your result by simulation. Interleave or embrace the hello and goodbye messages of the processes in different ways. Verify that you have achieved what you have intended for all those variations.

**Problem 4** In your design, change the time units of all **wait** statements from nanoseconds (ns) into to minutes (min). How does this impact the simulation run? Explain.