TECHNISCHE UNIVERSITÄT DRESDEN

Faculty of Computer Science Institute for Computer Engineering, Chair for VLSI-Design, Test and Architecture

Dresden, July 1, 2014

Summerschool

Modeling and Designing Dependable Embedded Systems

— Lab 2 —

Problem 1 Assume three signals a,b,c of type std_logic without explicit initialization and the following **architecture**:

```
process
begin
  wait for 10 ns;
  a <= '0';
  wait for 10 ns;
  a <= '1';
  wait; -- forever
end process;
```

```
process
begin
  wait for 5 ns;
  b <= '0';
  wait for 10 ns;
  b <= '1';
  wait; -- forever
end process;
c <= a and b;
```

(a) Draw the waveform of these signals as you expect them.

(b) Simulate the design.

(c) Verify your expectations and correct them if necessary. Explain.

Problem 2 Assume two signals a1, a2 of type std_logic with the following drivers:

```
a1 <= '0', not a1 after 5 ns;
```

```
process
begin
  a2 <= '0';
  wait for 5 ns;
  a2 <= not a2;
  wait; -- forever
end process;
```

(a) Draw the waveform of these signals as you expect them.

(b) Simulate the design.

(c) Verify your expectations and correct them if necessary. Explain.
Hint: Try different signal initializations to trace the reason for the observed behavior.

Problem 3 Implementation of single bit adders:

(a) Implement a combinational process that implements a half adder.

(b) Implement a process to generate signal waveforms to check your half adder implementation *exhaustively*. Check its correct operation by simulation.

(c) Expand your design by appropriate processes so that its overall computation realizes a full adder. Verify its correct operation by expanding your stimuli accordingly.

Problem 4 Implement a process that produces an incrementing 10-bit unsigned value, i.e. binary counter. Add further combinational processes to compute:

- the parity,
- the bitwise inversion, and
- the triple value (without using multiplication)

of the current counter value.