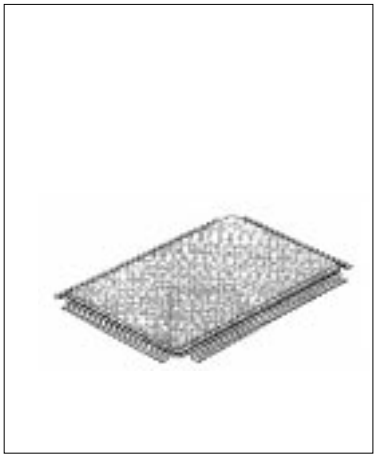
INTRODUCTION



100 QFP
The KS0068B is a dot matrix LCD driver & controller LSl which is fabricated by low power CMOS technology.

FUNCTION

- Character type dot matrix LCD driver & controller
- Internal driver: 16 common and 60 segment signal output.
- Display character format; 5× 7 dots + cursor, 5× 10 dots + cursor
- Easy interface with a 4-bit or 8-bit MPU
- Display character pattern:
  5× 7 dots format: 192 kinds, 5× 10 dots format: 32kinds
- The special character pattern can be programmable by Character Generator RAM directly.
- A customer character pattern can be programmable by mask option (KS0068B-00; Standard type)

KS0068B-00
English, Japanese Numberal

- Automatic power on reset function.
- It can drive a maximum 80 characters by using the kS0065B or KS0063B, KS0068B externally.
- It is possible to read both Character Generator and Display Data RAM from MPU.

FEATURES

- Internal Memory
  - Character Generator ROM: 8320bits
  - Character Generator RAM: 512 bits
  - Display Data RAM: 80× 8bits for 80 digits.
- Power Supply Voltage; +5V± 10%, +3V± 10%
- Supply voltage for display: 0~-5V(V_5)
- CMOS process
- 1/8 duty, 1/11 duty or 1/16 duty: selectable
  (1/8 duty; 5× 7 dots format 1 line, 1/11 duly; 5 x 10 dots format I line, 1/16 duty: 5× 7 dots format 2 line)
- 100 QFP or bare chip available.

BLOCK DIAGRAM

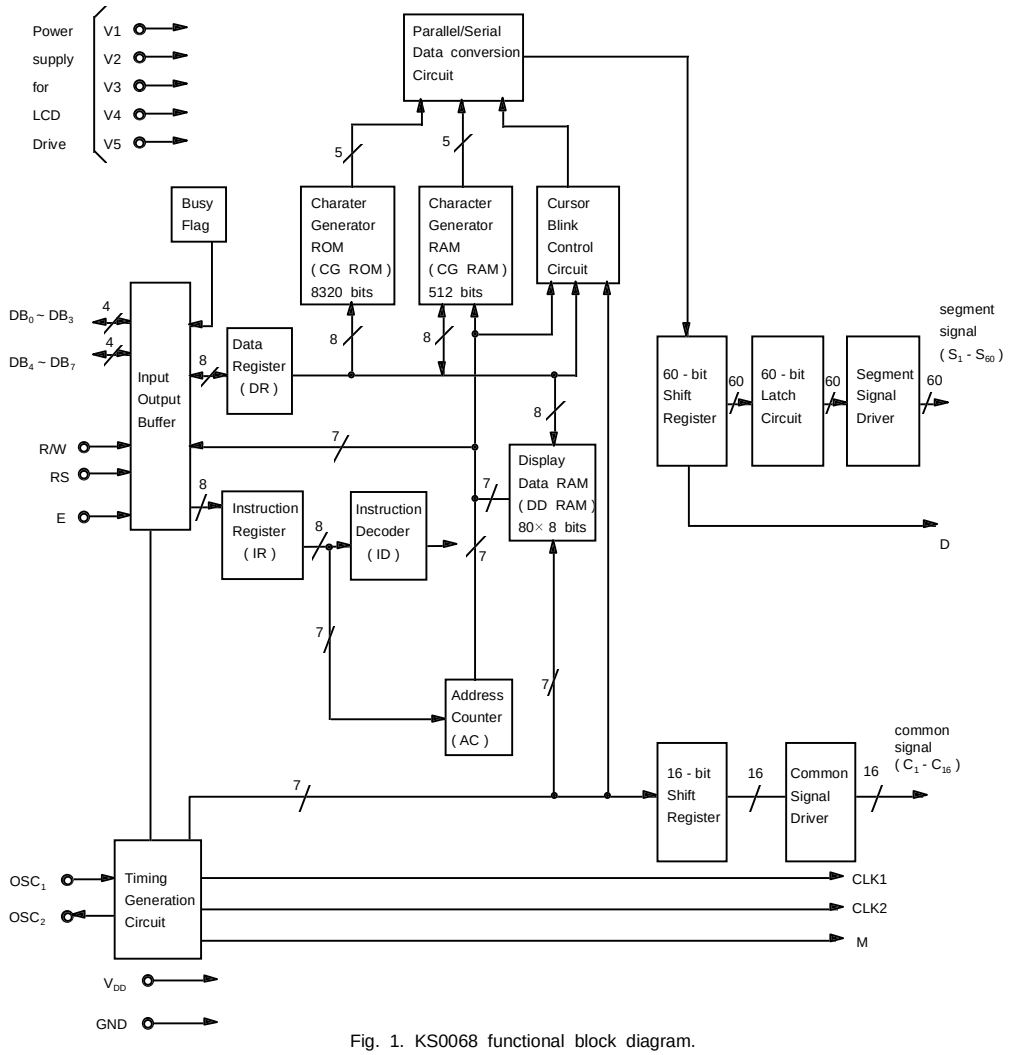


Fig. 1. KS0068 functional block diagram.

PIN CONFIGURATION

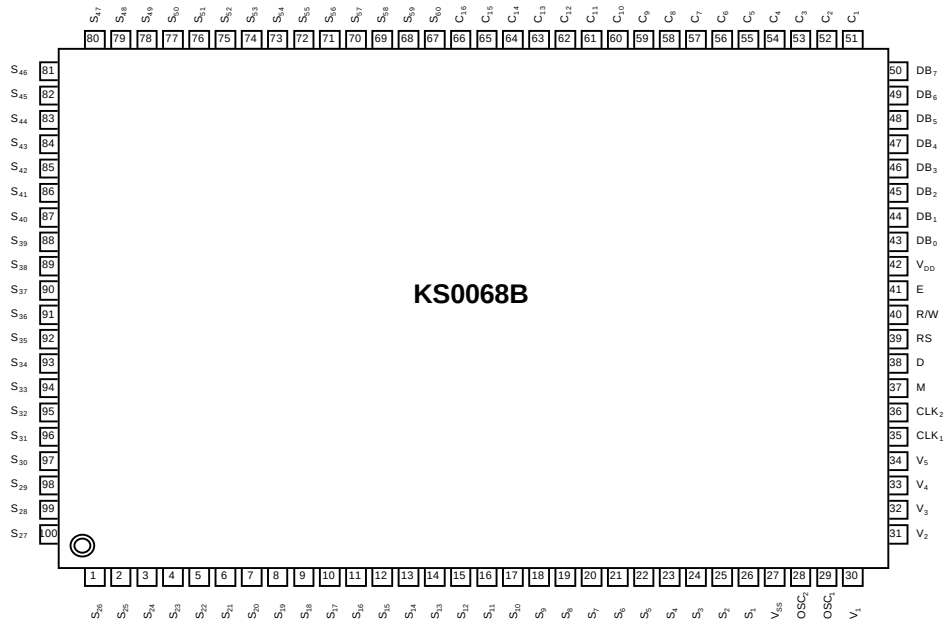
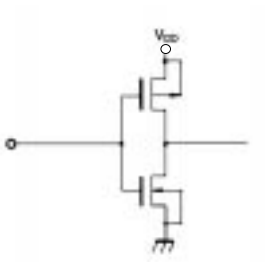
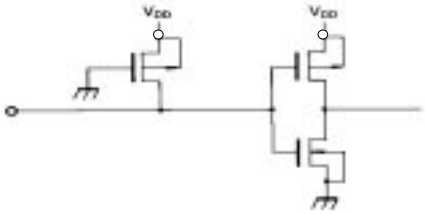
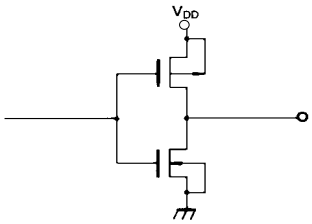
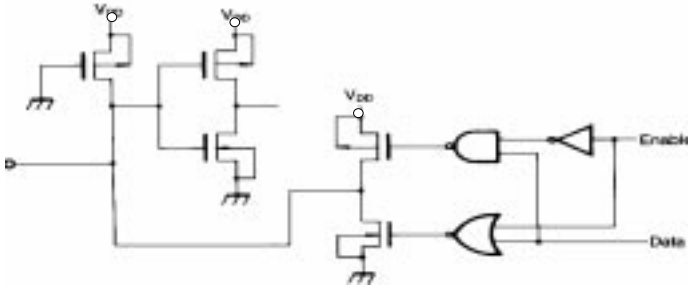


Fig2. 100QFP Top View

PIN DESCRIPTION

PIN(No).	INPUT/OUTPUT	NAME	DESCRIPTION	INTERFACE
V_{DD}(42)	Power	Operating Voltage	for logical circuit (2.7V ~ 5.5V)	Power Supply
V_{SS}(GND) (27)			0V (GND)	
V_1-V_5(30-34)		Negative Supply Voltage	Bias voltage level for LCD driving	
S_1-S_{60} (1-26, 67-100)	Output	Segment output	Segent signal output for LCD driving	LCD
C_1-C_{16} (51-66)	Output	Common output	Common signal output for LCD driving	LCD
OSC_1, OSC_2 (29) (28)	Input (OSC1) Output (OSC2)	Oscillator	Both pin connected to Rf resistor or ceramic resonator for internal oscillator circuit. In case of external frequency use only, the frequency is input to OSC1 terminal.	Resistor or Ceramic Resonator
CLK1 (35)	Output	Data latch clock	Clock output terminal for the serially transfered data to be latched to the driver.	KS0065B or KS0063B
CLK2 (36)		Data shift clock	Clock output terminal used when D terminal data output shifts the inside of the driver.	
M (37)		Alternated signal for LCD driver output	The alternating signal to convert LCD drive waveform to AC	
D (38)		Display data interface	Character pattern data, which is corresponding to each common signal, is supplied to driver serially. High: Selection Low: Non selection	
E(41)	Input	Enable	Start enable signal to read or write the data	MPU
R/W(40)		Read/Write	R/W signal input is used to select the read/write mode High: Read mode Low: Write mode	
RS (39)		Register select	register selection input High: Data register (for read and write) Low: Instruction register (for write), Busy flag, address counter (for read)	
DB_0-DB_7 (43-50)	Input/Output	Data interface	Used for data transfer between the MPU and KS0068. These terminals are for data bus with bidirectional three-state. Initial 4 bit (DB_0-DB_3) are not used during 4-bit operation (DB_7 can be used as a busy flag)	

Internal logic of input/output terminal

Input/Output	Logic diagram		Applicable pin
Input	No Pull up		E
	with pull up		RS, R/W
Output			CLK1, CLK2 M,D
Input Output			DB_0-DB_7

MAXIMUM ABSOLUTE LIMIT (Ta=25℃)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	-0.3~+7.0	V
Driver Supply Voltage	V_{LCD}	V_{DD}-11.5~V_{DD}+0.3	V
Input Voltage	V_{IN}	-0.3 ~ V_{DD}+0.3	V
Power Dissipation	P_D	500	mW
Operating Temperature	T_{OPR}	-30~+85	℃
Storage Temperature	T_{STG}	-55~+125	℃

* Voltage greater than above may damage to the circuit ($V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$)

ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD}=+5V± 10%, V_{SS}=0V, T_a=-30 ~ +85℃)

Characteristic		Symbol	Test condition		Min	Typ	Max	Unit	Applicable Pin
Operating Voltage		V_{DD}	-		4.5	-	5.5	V	
Operating Current (*1)		I_{DD1}	Ceramic resonator fosc=250KHz		-	0.65	0.9	mA	
		I_{DD2}	Resistor oscillation external clock operation fosc=270KHz		-	0.45	0.7		
Input Voltage 1	High	V_{IH1}	-		2.2	-	V_{DD}	V	E, DB_0-DB_7, R/W, RS
	Low	V_{IL1}	-		-0.3	-	0.6		
Input Voltage 2	High	V_{IH2}	-		V_{DD} -1.0	-	V_{DD}		OSC1
	Low	V_{IL2}	-		-0.2	-	1.0		
Output Voltage 1	High	V_{OH1}	I_{OH}=-0.205mA		2.4	-	-		DB_0-DB_7
	Low	V_{OL1}	I_{OL}=1.2mA		-	-	0.4		
Output Voltage 2	High	V_{OH2}	I_O=-40㎂		0.9V_{DD}	-	-		CLK1, CLK2, M, D
	Low	V_{OL2}	I_O=40㎂		-	-	0.1V_{DD}		
Voltage Drop (*2)	COM	Vd_{COM}	I_O=± 0.1mA		-	-	1		C1-C16
	SEG	Vd_{SEG}			-	-	1		S1-S60
Input Leakage Current		I_{LKG}	V_{IN}=0 or V_{DD}		-1	-	1	㎂	E
Input Low Current		I_{IN}	V_{DD}=5V (test pull up R)		-50	-125	-250		RS,R/W
External Clock	Frequency(*3)	f_{EC}	-		125	250	350	KHz	OSC1
	Duty	duty			45	50	55	%	
	Rise time	t_R			-	-	0.2	㎲	
	Fall time	t_F			-	-	0.2	㎲	
Internal Clock Frequency(*3)		f_{OSC1}	Rf=91KΩ ± 2%		190	270	350	KHz	OSC1, OSC2
Ceramic Resonator OSC Frequency (*3)		f_{OSC2}			245	250	255		
LCD driving voltage(*4)		V_{LCD1}	V_{DD}-V_5	1/5 bias	3.0	-	10.0	V	V_1-V_5
		V_{LCD2}		1/6 bias	3.0	-	10.0		

Note: *1) Applies to the current value flown in terminal V_{DD} when power is input as follows; V_{DD}=5V, GND=0V, V1=3.4V, V2=1.8V, V3=0.2V, V4=-1.4V and V5=-3V.

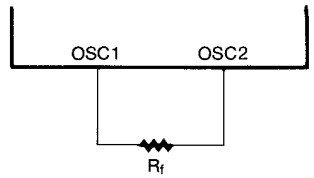
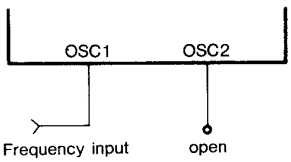
*2) Applied to the voltage drop occuring from terminals V_{DD}, V1, V4 and V5 to each common terminal (C1-C16) when 0.1mA is flown in or out to and from all COM and SEG terminals, and also to voltage drop occuring from terminals V_{DD}, V2, V3 and V5 to each SEG terminal (S1-S60). When the output level is at V_{DD}, V1 or V2 level, 0.1mA is flown out, while 0.1mA flow in when the output level is at V3, V4 or V5 level. This occurs when 5V or -5V is input to V_{DD}, V1 and V3 or to V2, V4, and V5 respectively.

DC Characteristics (V_{DD}=+3V± 10%, V_{SS}=0V, T_a=-30 ~ +85℃)

Characteristic		Symbol	Test condition	Min	Typ	Max	Unit	Applicable Pin
Operating Voltage		V_{DD}	-	2.7	3.0	3.3	V	
Operating Current (*1)		I_{DD1}	Ceramic resonator fosc=250KHz	-	0.3	0.5	mA	
		I_{DD2}	Resistor oscillation external clock operation fosc=270KHz	-	0.17	0.3		
Input Voltage 1	High	V_{IH1}	-	1.9	-	V_{DD}	V	E, DB_0-DB_7, R/W, RS
	Low	V_{IL1}	-	-0.3	-	0.4		
Input Voltage 2	High	V_{IH2}	-	0.7V_{DD}	-	V_{DD}		OSC1
	Low	V_{IL2}	-	-	-	0.2V_{DD}		
Output Voltage 1	High	V_{OH1}	I_{OH}=-0.1mA	2.0	-	-		DB_0-DB_7
	Low	V_{OL1}	I_{OL}=0.1mA	-	-	0.4		
Output Voltage 2	High	V_{OH2}	I_O=-40㎂	0.8V_{DD}	-	-		CLK1, CLK2, M, D
	Low	V_{OL2}	I_O=40㎂	-	-	0.2V_{DD}		
Voltage Drop (*2)	COM	Vd_{COM}	I_O=± 0.05mA	-	-	1		C1-C16
	SEG	Vd_{SEG}		-	-	1.5		S1-S60
Input leakage current		I_{LKG}	V_{IN}=0 or V_{DD}	-1	-	1	㎂	E
Input Low Current		I_{IN}	V_{DD}=3V (test pull up R)	-10	-50	-120		RS,R/W
External Clock	Frequency (*3)	f_{EC}	-	125	250	350	KHz	OSC1
	Duty	duty		45	50	55	%	
	Rise time	t_R		-	-	0.2	㎲	
	Fall time	t_F		-	-	0.2	㎲	
Internal clock Frequency(*3)		f_{OSC}	Rf=75KΩ ± 2%	190	270	350	KHz	OSC1, OSC2
LCD Driving Voltage(*4)		V_{LCD1}	V_{DD}-V_5 1/5 bias	3.0	-	10.0	V	V_1-V_5
		V_{LCD2}	1/4 bias	3.0	-	10.0		

Note: *1) : The supply current value from V_{DD} when power condition is as follows
V_{DD} = 5V, V_{SS} = 0V, V5 = -2V
V_{DD} = 3V, V_{SS} = 0V, V5 = -2V
*2) : The voltage drop from LCD bias terminals V_{DD}, V1, V4 and V5 to each common terminal (C1-C16) and also to voltage drop LCD bias terminals V_{DD}, V2, V3 and V5 to each segment terminal (S1-S80)
*3) and *4) : Refer to oscillator circuit and input the voltage listed in the table bellow to v1 ~ v5.

*3) Oscillator circuit

Resistor circuit	External clock cirucit
 R_f: 91kΩ±2%	

*4) Input the voltage listed in the table below to V_1-V_5

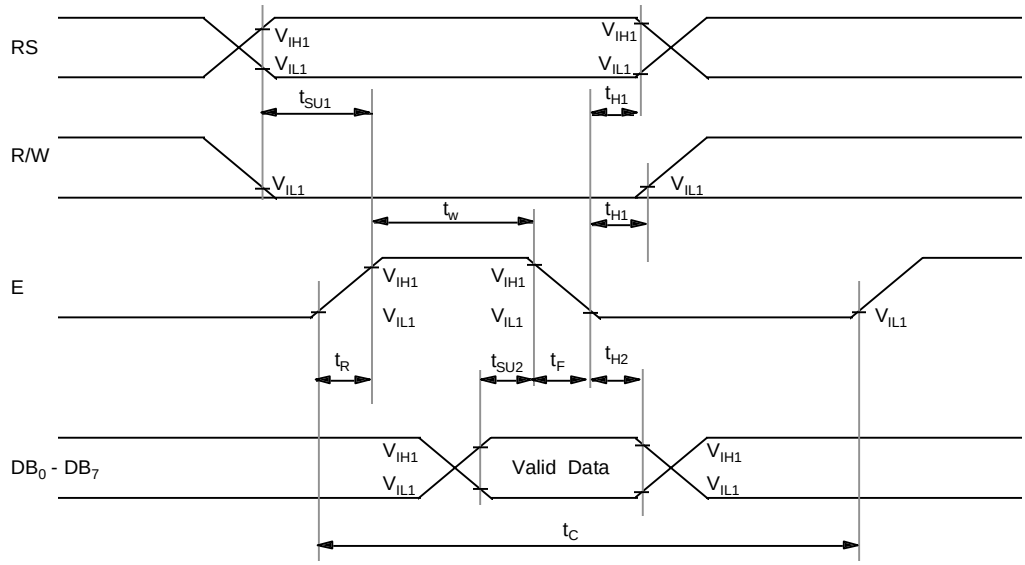
Duty / Bias / Power supply	1/8, 1/11	1/16
	1/4	1/5
V_1	V_{DD}-V_{LCD}/4	V_{DD}-V_{LCD}/5
V_2	V_{DD}-V_{LCD}/2	V_{DD}-2V_{LCD}/5
V_3	V_{DD}-V_{LCD}/2	V_{DD}-3V_{LCD}/5
V_4	V_{DD}-3V_{LCD}/4	V_{DD}-4V_{LCD}/5
V_5	V_{DD}-V_{LCD}	V_{DD}-V_{LCD}

*V_{LCD} is the LCD driving voltage, refer to the initial set of the instruction code.

AC Characteristics (V_{DD}=5V± 10%, V_{SS}=0V, Ta=-30 ~ +85℃)

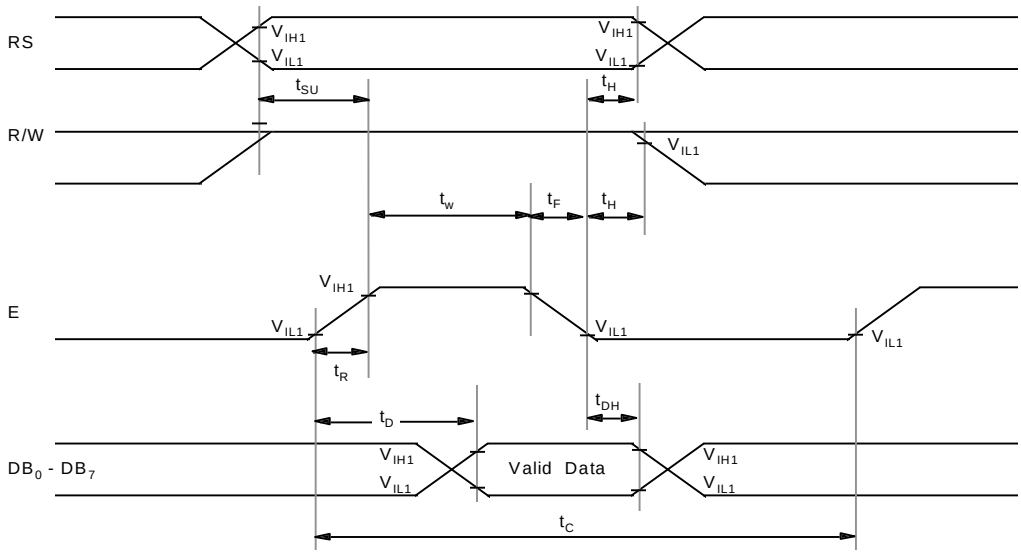
(1) Write mode (Writing data from Micom to KS0068B)

Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
E Cycle Time	t_c	500	-	-	ns	E
E Rise Time	t_R	-	-	25	ns	E
E Fall Time	t_F	-	-	25	ns	E
E Pulse Width (High, Low)	t_W	220	-	-	ns	E
R/W And RS Set-Up Time	t_{SU1}	40	-	-	ns	R/W, RS
R/W And RS Hold Time	t_{H1}	10	-	-	ns	R/W, RS
Data Set-Up Time	t_{SU2}	60	-	-	ns	DB_0~DB_7
Data Hold Time	t_{H2}	10	-	-	ns	DB_0~DB_7



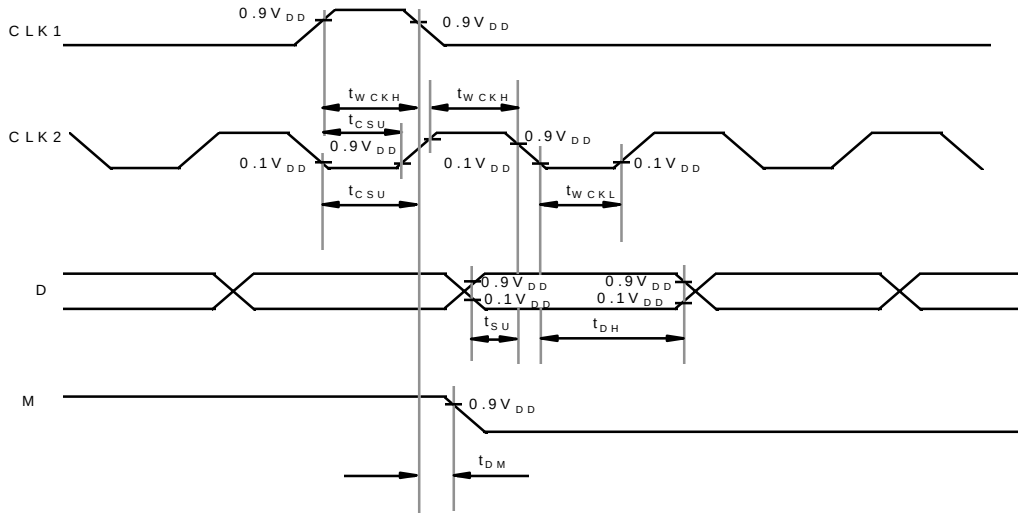
(2) Read mode (Reading data from KS0068B to Micom)

Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
E Cycle Time	t_c	500	-	-	ns	E
E Rise Time	t_R	-	-	25	ns	E
E Fall Time	t_F	-	-	25	ns	E
E Pulse Width (High, Low)	t_W	220	-	-	ns	E
R/W And RS Set-Up Time	t_{SU}	40	-	-	ns	R/W, RS
R/W And RS Hold Time	t_H	10	-	-	ns	R/W, RS
Data Output Delay Time	t_D	-	-	120	ns	DB_0~DB_7
Data Hold Time	t_{DH}	20	-	-	ns	DB_0~DB_7



(3) Interface mode with KS0065B, KS0063B

Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
Clock Pulse Width High	t_{WCKH}	800	-	-	ns	CLK
Clock Pulse Width Low	t_{WCKL}	800	-	-	ns	CLK
Data Set-Up Time	t_{SU}	300	-	-	ns	D
Data Hold Time	t_{DH}	300	-	-	ns	D
Clock Set-Up Time	t_{CSU}	500	-	-	ns	CLK
M Delay Time	t_{DM}	-1000	-	1000	ns	M



AC Characteristics (V_{DD}=3V± 10%, V_{SS}=0V, Ta=-30 ~ +85℃)

(1) Write mode (Writing data from Micon to KS0068B)

Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
E Cycle Time	t_c	1400	-	-	ns	E
E Rise Time	t_R	-	-	25	ns	E
E Fall Time	t_F	-	-	25	ns	E
E Pulse Width (High, Low)	t_W	400	-	-	ns	E
R/W And RS Set-Up Time	t_{SU1}	60	-	-	ns	R/W, RS
R/W And RS Hold Time	t_{H1}	20	-	-	ns	R/W, RS
Data Set-Up Time	t_{SU2}	140	-	-	ns	DB_0~DB_7
Data Hold Time	t_{H2}	10	-	-	ns	DB_0~DB_7

(2) Read mode (Reading data from KS0068B to Micom)

Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
E Cycle Time	t_c	1400	-	-	ns	E
E Rise Time	t_R	-	-	25	ns	E
E Fall Time	t_F	-	-	25	ns	E
E Pulse Width (High, Low)	t_W	400	-	-	ns	E
R/W And RS Set-Up Time	t_{SU}	60	-	-	ns	R/W, RS
R/W And RS Hold Time	t_H	20	-	-	ns	R/W, RS
Data Output Delay Time	t_D	-	-	360	ns	DB_0~DB_7
Data Hold Time	t_{DH}	5	-	-	ns	DB_0~DB_7

(3) Interface mode with KS0065B, KS0063B

Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
Clock Pulse Width High	t_{WCKH}	800	-	-	ns	CLK
Clock Pulse Width Low	t_{WCKL}	800	-	-	ns	CLK
Data Set-Up Time	t_{SU}	300	-	-	ns	D
Data Hold Time	t_{DH}	300	-	-	ns	D
Clock Set-Up Time	t_{CSU}	500	-	-	ns	CLK
M Delay Time	t_{DM}	-1000	-	1000	ns	M

CONTROL and DISPLAY COMMAND

Command	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Excution time (fosc=250KHz)	Remark
DISPLAY CLEAR	L	L	L	L	L	L	L	L	L	H	1.64ms	
RETURN HOME	L	L	L	L	L	L	L	L	H	X	1.64ms	cursor move to first digit
ENTRY MODE SET	L	L	L	L	L	L	L	H	I/D	SH	40㎲	•I/D; set cursor move direction I/D: H Increase; L Decrease •SH: Specifies shift of display SH: H display is shifted; L display is not shifted
DISPLAY ON/OFF	L	L	L	L	L	L	H	D	C	B	40㎲	•Display D: H Display on; L Display off •Cursor C: H Cursor on; L Cursor off •Blinking B: H Blinking on; L Blinking off
SHIFT	L	L	L	L	L	H	S/C	R/L	X	X	40㎲	SC: H Display shift; L Cursor move R/L: H Right shift; L Left shift
SET FUNCTION	L	L	L	L	H	DL	N	F	X	X	40㎲	DL: H 8 bits interface; L 4 bits interface N: H 2 line display; L 1 line display F: H 5× 10 dots; L 5× 7 dots

Table 1.

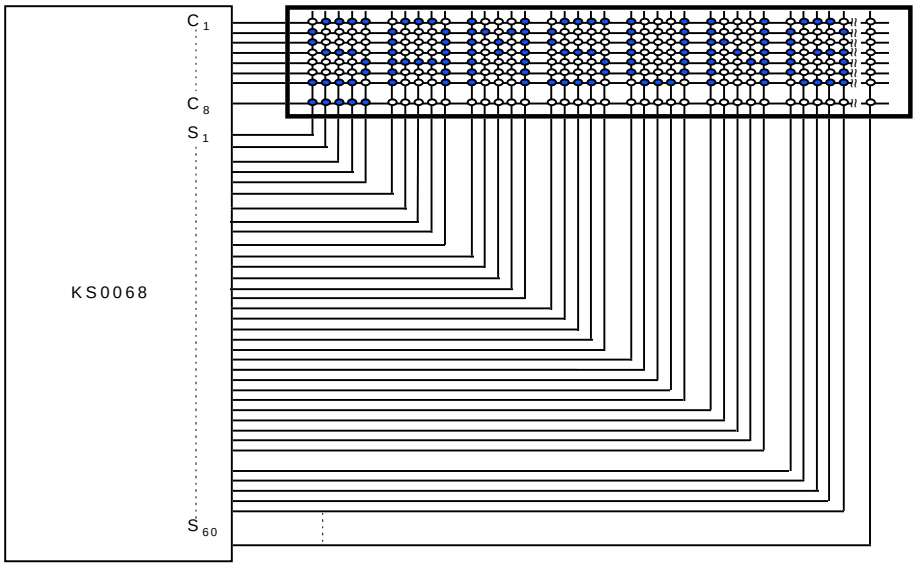
CONTROL and DISPLAY COMMAND(continued)

Command	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Excution time (fosc=250KHz)	Remark
SET CG RAM ADDRESS	L	L	L	H	CG RAM address (corresponds to cursor address)						40㎲	CG RAM Data is sent and received after this setting
SET DD RAM ADDRESS	L	L	H	DD RAM address							40㎲	DD RAM Data is sent and recevied after this setting
READ BUSY FLAG & ADDRESS	L	H	BF	Address Counter used for Both DD & CG RAM address							0㎲	BF H Busy; L Ready - Reads BF indication internal operating is being performed. - reads address counter contents
WRITE DATA	H	L	Write Data								46㎲	Write data into DD or CGRAM
READ DATA	H	H	Read Data								46㎲	Read data from DD or CGRAM

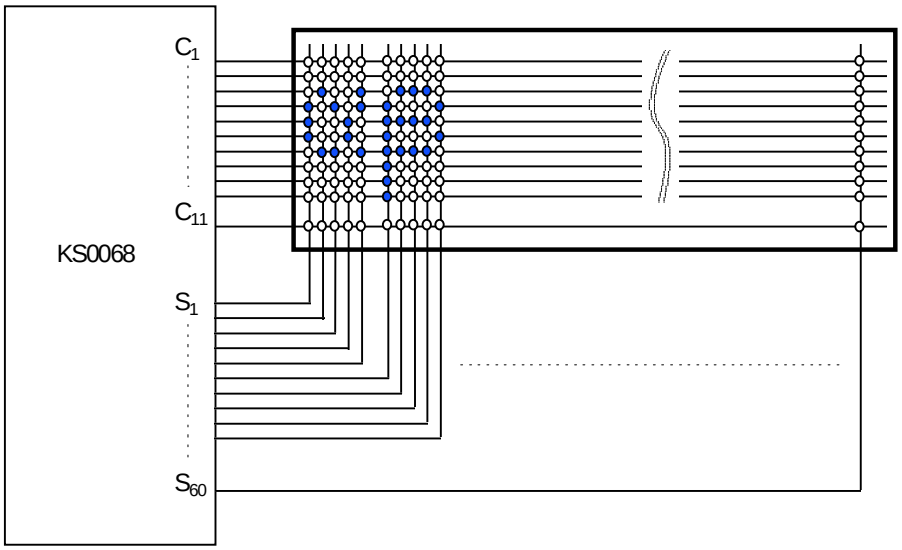
X : Don't care

APPLICATION INFORMATION ACCORDING TO LCD PANEL

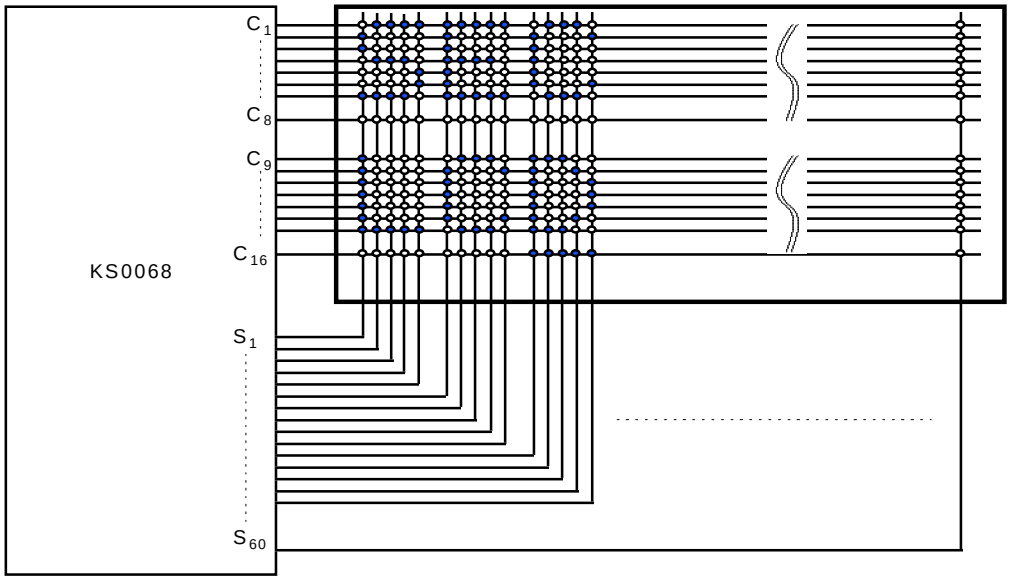
1) LCD Pandel: 12 character× 1 line, character format; 5× 7 dots + 1 cursor line (1/4 bias, 1/8 duty)



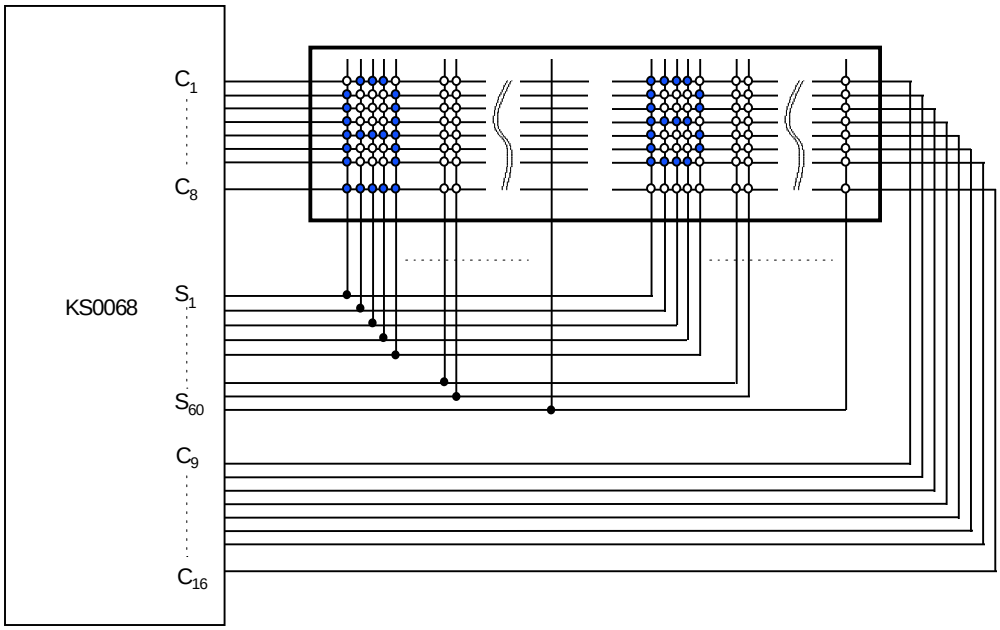
2) LCD Panel: 12 character× 1 line, character format; 5× 10 dots + 1 cursor line (1/4 bias, 1/11 duty)



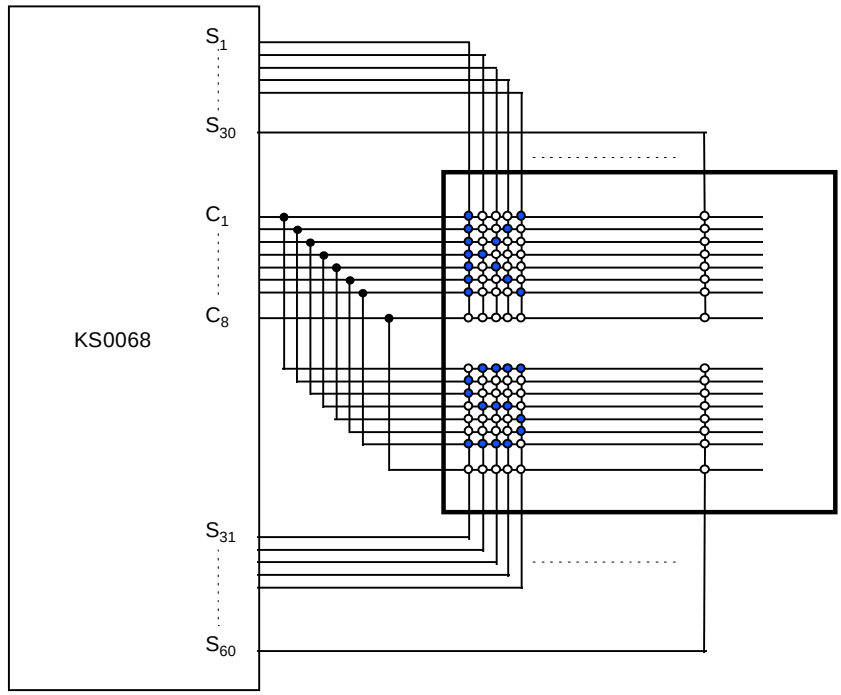
3) LCD Panel : 12 character × 2 line character format; 5× 7 dots + 1 cursor line (1/5 bias, 1/16 duty)



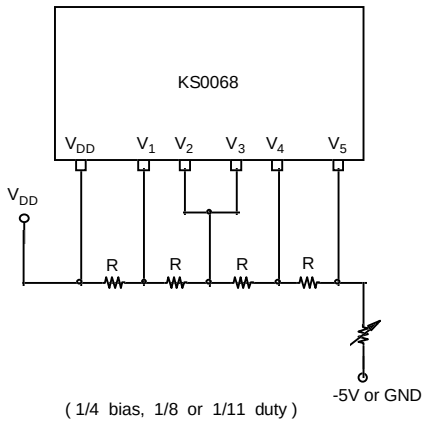
4) LCD Panel : 24 character × 1 line, character format; 5 × 7 dots + 1 dots + 1 cursor line (1/5 bias, 1/16 duty)



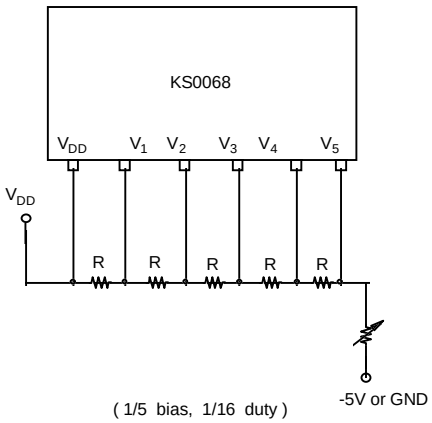
5) LCD Panel : 6 character × 2 line character format; 5 × 7 dots + 1 cursor line (1/4 bias, 1/8 duty)



BIAS VOLTAGE DIVIDE CIRCUIT

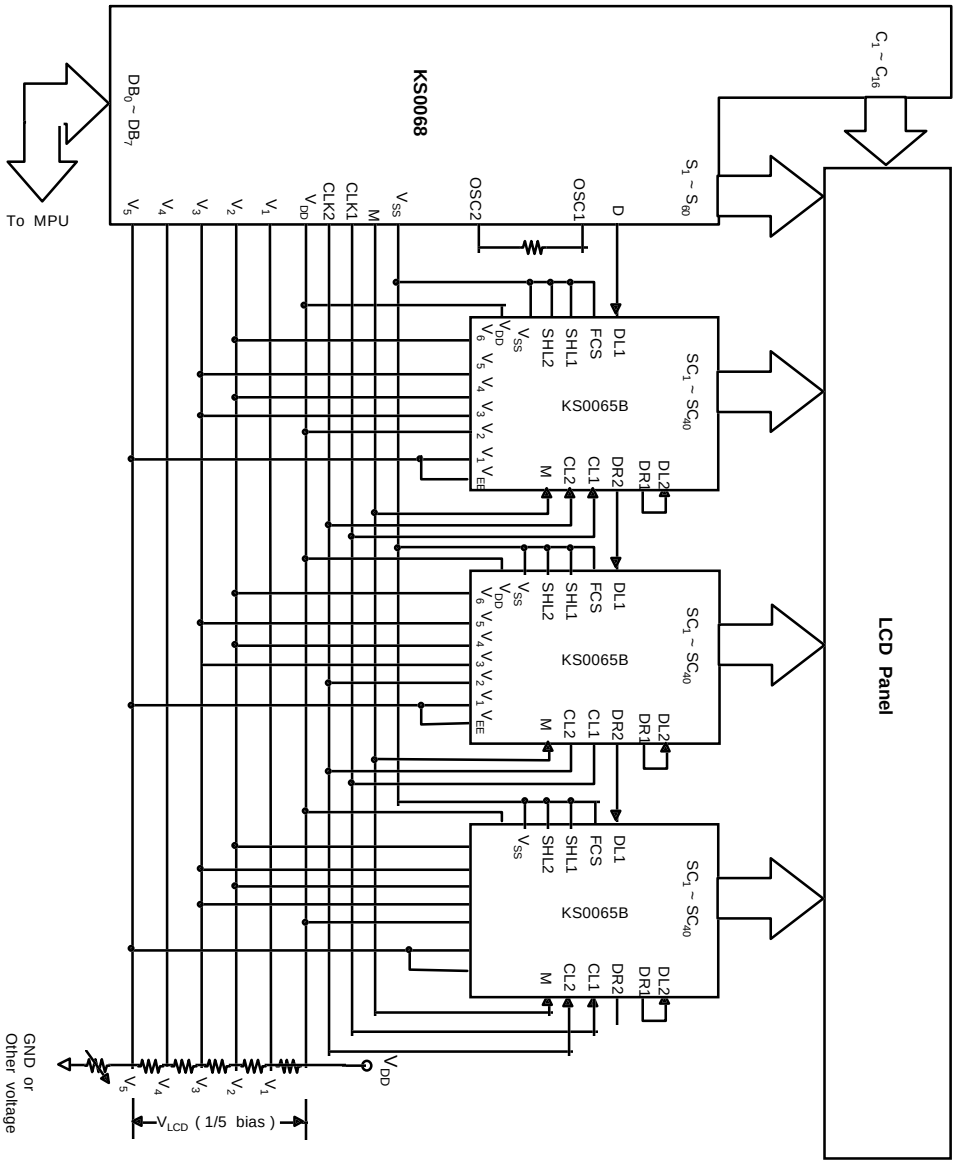


(1/4 bias, 1/8 or 1/11 duty)



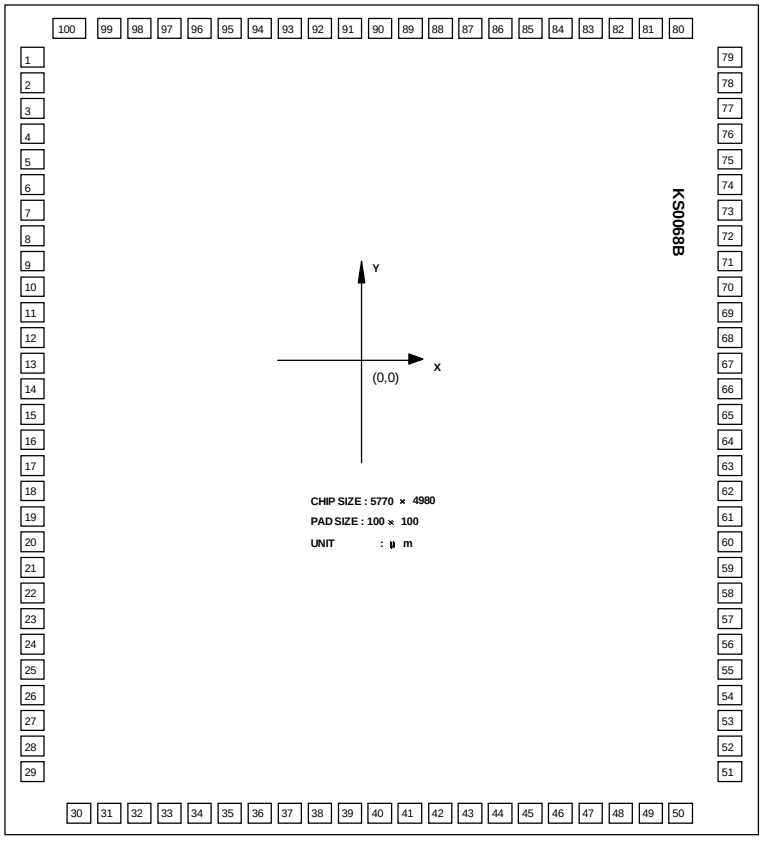
(1/5 bias, 1/16 duty)

APPLICATION CIRCUIT



When KS0065B is externally connected to the KS0068, you can increase the number of display digits up to 80 characters.

PAD DIAGRAM



* **KS0068B** Marking : easy to find the PAD No.72,81

PAD LOCATION

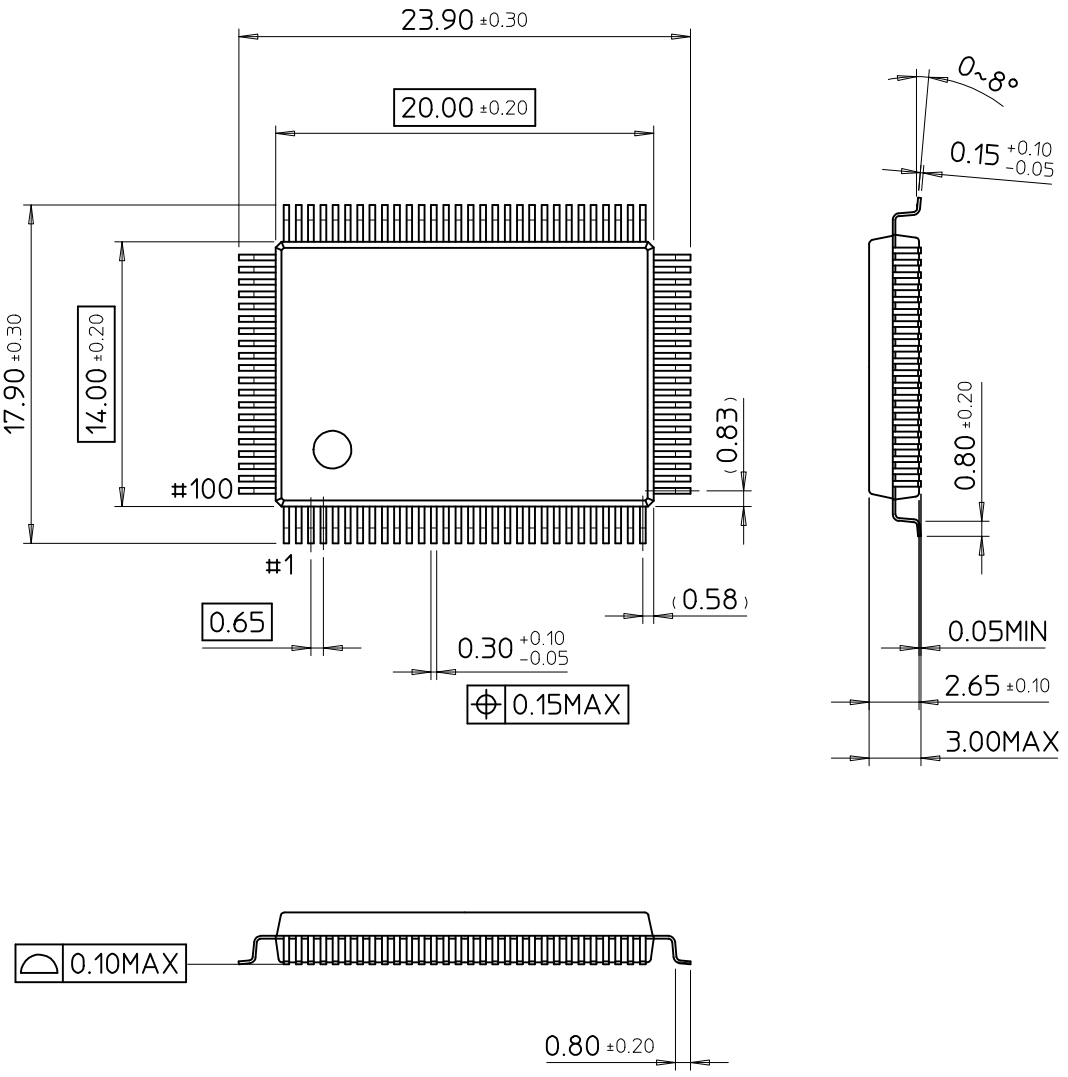
UNIT (μ m)

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y
1	SEG26	-1684	1686	35	CLK1	-453	-2358	69	SEG58	1684	436
2	SEG25	-1684	1560	36	CLK2	-328	-2358	70	SEG57	1684	560
3	SEG24	-1684	1436	37	M	-203	-2358	71	SEG56	1684	686
4	SEG23	-1684	1310	38	D	-78	-2358	72	SEG55	1684	810
5	SEG22	-1684	1186	39	RS	47	-2358	73	SEG54	1684	936
6	SEG21	-1684	1060	40	R/W	172	-2358	74	SEG53	1684	1060
7	SEG20	-1684	936	41	E	297	-2358	75	SEG52	1684	1186
8	SEG19	-1684	810	42	VDD	422	-2358	76	SEG51	1684	1310
9	SEG18	-1684	686	43	DB0	547	-2358	77	SEG50	1684	1436
10	SEG17	-1684	560	44	DB1	672	-2358	78	SEG49	1684	1560
11	SEG16	-1684	436	45	DB2	797	-2358	79	SEG48	1684	1686
12	SEG15	-1684	310	46	DB3	922	-2358	80	SEG47	1249	2358
13	SEG14	-1684	186	47	DB4	1047	-2358	81	SEG46	1124	2358
14	SEG13	-1684	60	48	DB5	1172	-2358	82	SEG45	999	2358
15	SEG12	-1684	-64	49	DB6	1297	-2358	83	SEG44	874	2358
16	SEG11	-1684	-190	50	DB7	1422	-2358	84	SEG43	749	2358
17	SEG10	-1684	-314	51	COM1	1684	-1814	85	SEG42	624	2358
18	SEG9	-1684	-440	52	COM2	1684	-1690	86	SEG41	499	2358
19	SEG8	-1684	-564	53	COM3	1684	-1564	87	SEG40	374	2358
20	SEG7	-1684	-690	54	COM4	1684	-1440	88	SEG39	249	2358
21	SEG6	-1684	-814	55	COM5	1684	-1314	89	SEG38	124	2358
22	SEG5	-1684	-940	56	COM6	1684	-1190	90	SEG37	-1	2358
23	SEG4	-1684	-1064	57	COM7	1684	-1064	91	SEG36	-126	2358
24	SEG3	-1684	-1190	58	COM8	1684	-940	92	SEG35	-251	2358
25	SEG2	-1684	-1314	59	COM9	1684	-814	93	SEG34	-376	2358
26	SEG1	-1684	-1440	60	COM10	1684	-690	94	SEG33	-501	2358
27	VSS	-1684	-1702	61	COM11	1684	-564	95	SEG32	-626	2358
28	OSC2	-1684	1868	62	COM12	1684	-440	96	SEG31	-751	2358
29	OSC1	-1684	-1994	63	COM13	1684	-314	97	SEG30	-876	2358
30	V1	-1078	-2358	64	COM14	1684	-190	98	SEG29	-1001	2358
31	V2	-953	-2358	65	COM15	1684	-64	99	SEG28	-1126	2358
32	V3	-828	-2358	66	COM16	1684	60	100	SEG27	-1251	2358
33	V4	-703	-2358	67	SEG60	1684	186				
34	V5	-578	-2358	68	SEG59	1684	310				

Standard Character Pattern (KS0068B-00)

100-QFP-1420C

Dimensions in Milimeters



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