Operating Systems W9L2 - Memory Management II (ctd)

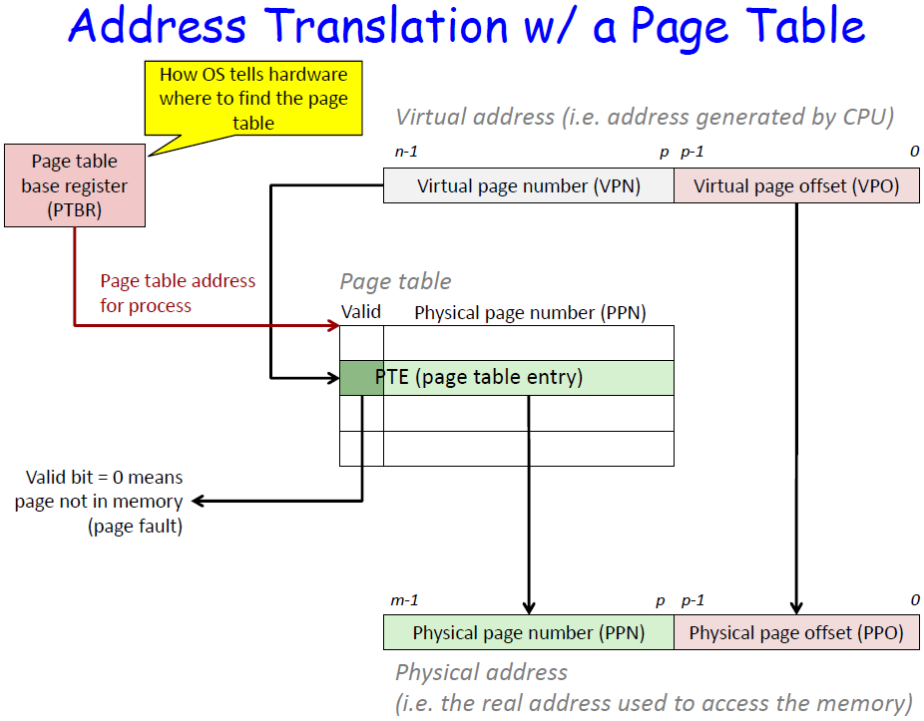
Class	Operating Systems
Created	@Oct 28, 2020 2:41 PM
Materials	
Reviewed	☐
Type	Lecture

> ! Discussed next lab for roughly first 20 minutes of class

More on Virtual Memory

- Virtual addresses created by CPU
- Different page sizes differ → MMU is designed such that OS can adjust based on the default page size
- MMUs are per core, but the explanations are all assuming single core

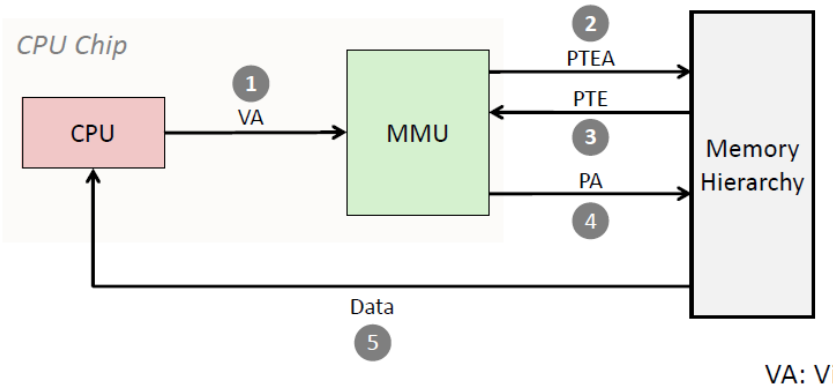
▼ Address Translation w/ a Page Table Diagram



- Info about each process is stored in a *process control block* (recall from earlier lectures
  - The page table base address is stored here, loaded by the PTBR when process scheduled for execution
  - Only the OS (kernel level) can access PTBR

▼ Page Hit and Page Fault Diagrams

Address Translation: Page Hit



VA: Virtual Address
PA: Physical Address
PTE: Page Table Entry
PTEA: PTE Address

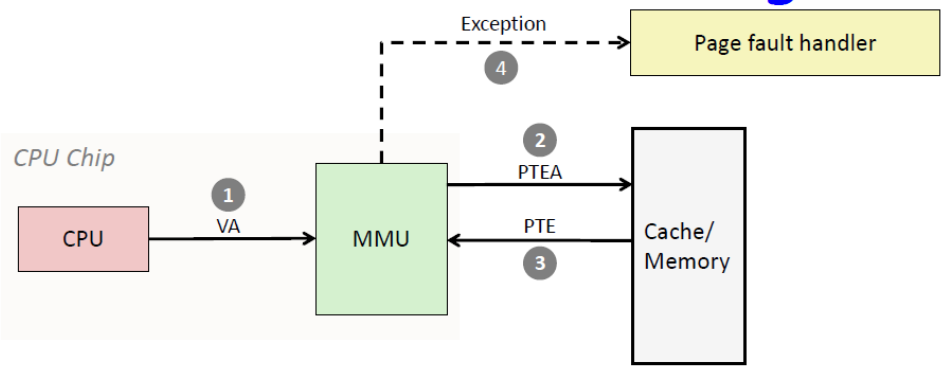
1) Processor sends virtual address to MMU

2-3) MMU fetches PTE from page table in memory

4) MMU sends physical address to cache/memory

5) Cache/memory sends data word to processor

Address Translation: Page Fault



1) Processor sends virtual address to MMU

2-3) MMU fetches PTE from page table in memory

4) Valid bit is zero, so MMU triggers page fault exception in kernel

If VA is invalid, then kill process (SIGSEGV)

If VA has been paged out to disk, then swaps in faulted page, update page table, resume faulted process

- Two main challenges with translating

1. Speed — Each request needs to access memory *twice*
2. Size — One page table per process and page tables can already be huge

Speeding up Virtual Memory

- **TLB:** Translation Lookaside Buffer
- More references than number of pages made by programs, so only a fraction of our page table is used

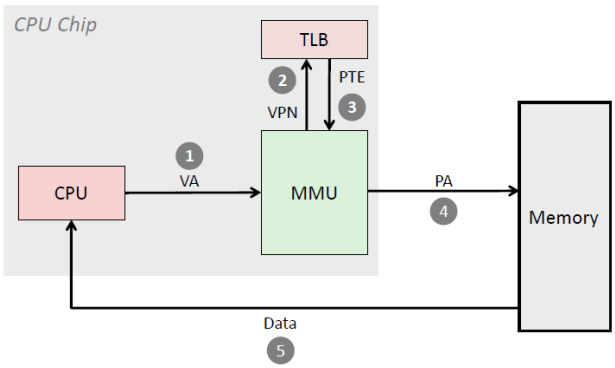
▼ TLB makes use of this observation

- **Solution:** *Translation Lookaside Buffer* (TLB)
  - Small hardware cache inside the MMU (i.e. on chip)
  - Maps virtual page numbers to physical page numbers address without going to the page table
  - Contains complete page table entries for small number of pages

- TLB is a small hardware cash and therefore fast to access

▼ TLB Hit and Miss Diagrams

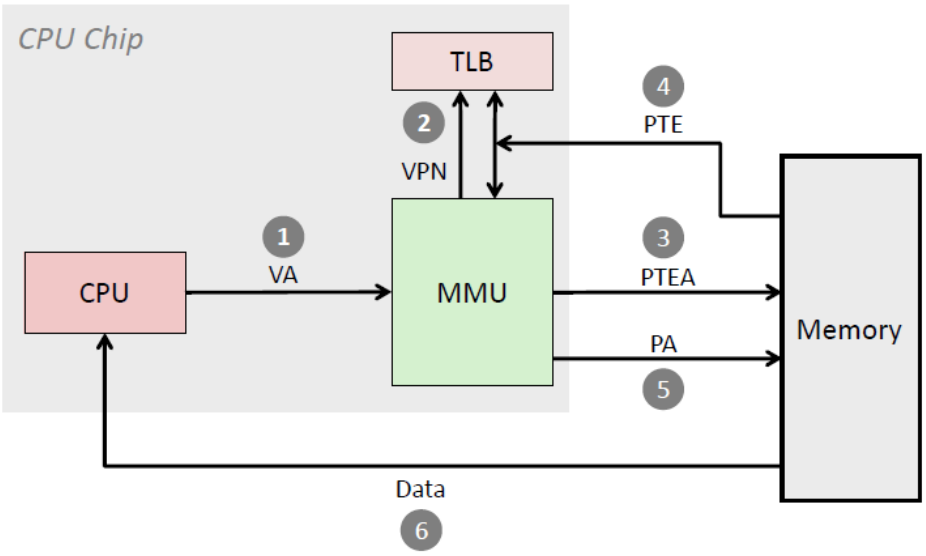
TLB Hit



A TLB hit eliminates a memory access

VA: Virtual Address **PA:** Physical Address **PTE:** Page Table Entry

TLB Miss



A TLB miss incurs an additional memory access (the PTE)

Fortunately, TLB misses are rare.

- Given cache memory (not main memory hierarchy) also solves our other problem (size/speed)

Apologies for the shorter notes today- was trying to follow what the prof was saying as he went over the diagrams.