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Senodia
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SH3001

6-Axis IMU

Package: 14-Pin LGA
Dimension: 3.0×2.5×1.0 mm^3
Document Revision: Rev1.6

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1 Basic Descriptions

1.1 SH3001

SH3001 is a highly integrated and low power 6-Axis inertial measurement unit (IMU) that combines both acceleration and angular rate measurement in one chip.
The device integrates:

- 16-bit digital 3-axis accelerometer with $\pm 2g$, $\pm 4g$, $\pm 8g$ and $\pm 16g$ range
- 16-bit digital 3-axis gyroscope with $\pm 125dps$, $\pm 250dps$, $\pm 500dps$, $\pm 1000dps$, $\pm 2000dps$ range

1.2 Features and Benefits

- Compact and small size, 14-Pin LGA package with 3.0×2.5 mm^2 footprint
- Wide operating temperature range: -40^{o}C - 85^{o}C
- Wide power supply range: VDD 1.71V-3.60V and independent VDDIO 1.71V-3.60V
- User-programmable low-pass filter for both accelerometer and gyroscope
- User-programmable interrupts
- On-chip digital output temperature sensor
- Configurable secondary digital interface for AUX devices
- 1kB on-chip FIFO for accelerometer, gyroscope, temperature and AUX sensor data
- 2 independent programmable I/O pins for interrupt
- RoHS compliant, halogen and lead free

1.3 Applications

- Mobile phones
- Smart watches,wristbands and fitness trackers
- Motion-enabled game and application framework
- Motion-based game controllers
- Augmented and virtual reality glasses and controllers
- Attitude monitoring
- Smart toys

Contents

List of Figures

List of Tables

2 Functional Diagram

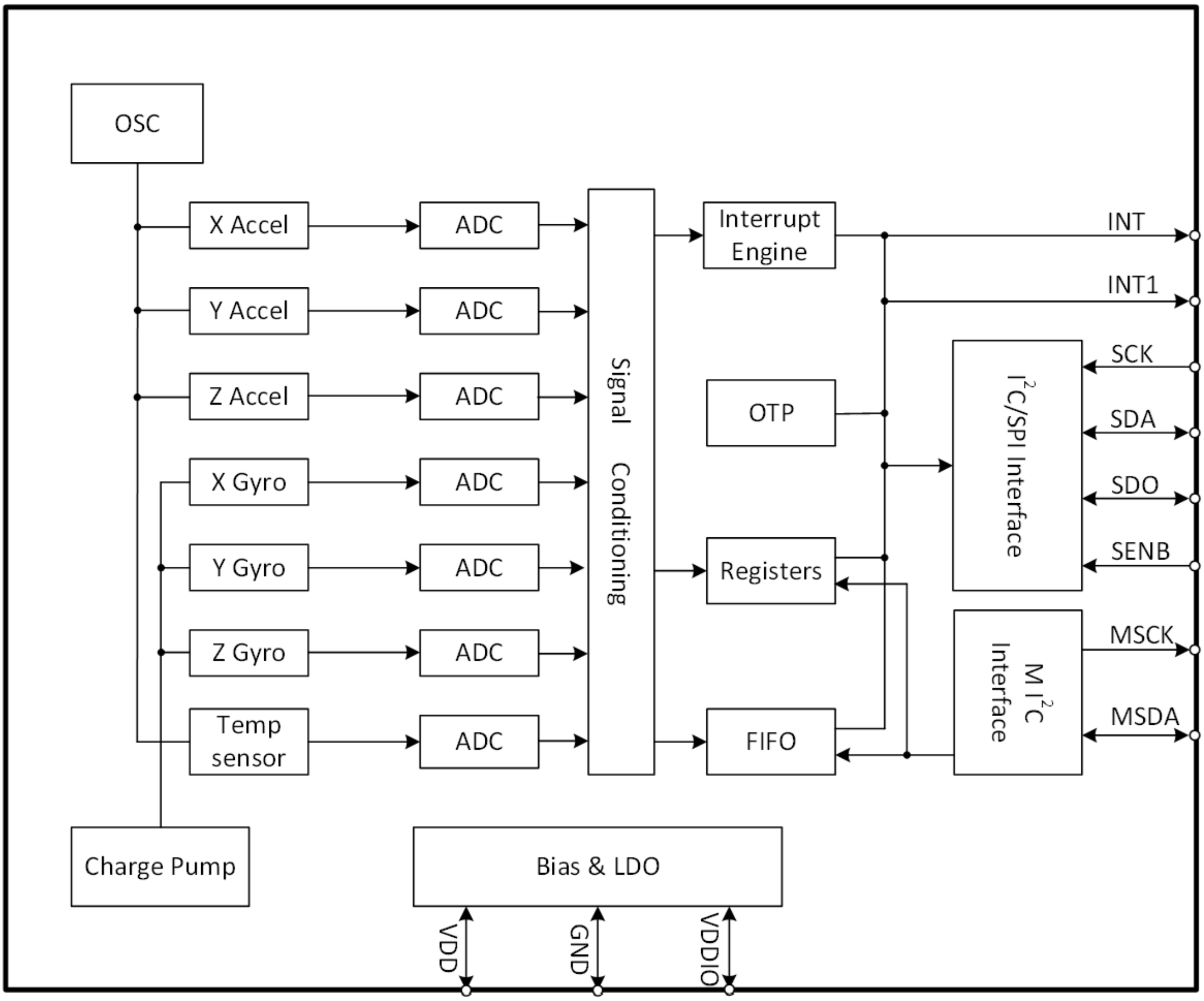

Figure 1: Functional diagram of the device

3 SH3001 Specifications

All parameters specified are tested at VDD=3.0V and T=25^{o}C, unless otherwise noted.

3.1 Gyroscope Specifications

Table 1: Gyroscope specifications

Parameter	Condition	Min	Typ	Max	Unit
Full Scale Range	Selectable via serial digital interface		$\pm$ 125		dps
			$\pm$ 250		dps
			$\pm$ 500		dps
			$\pm$ 1000		dps
			$\pm$ 2000		dps
Sensitivity	Selectable via serial digital interface		262		LSB/dps
			131		LSB/dps
			65.5		LSB/dps
			32.8		LSB/dps
			16.4		LSB/dps
Nonlinearity	Best fit straight line		$\pm$ 0.2		$\%FS$
Cross-axis Sensitivity			$\pm$ 1		$\%$
Sensitivity Temperature Drift	-40°C - 85°C		$\pm$ 0.02		$\%/^{o}C$
Zero Rate Temperature Drift	-40°C - 85°C		$\pm$ 0.05		$dps/^{o}C$
Zero Rate Offset			$\pm$ 1		dps
Output Noise Density			10		$mdps/\sqrt{Hz}$
Output Data Rate	Selectable via serial digital interface		31		Hz
			63		Hz
			125		Hz
			250		Hz
			500		Hz
			1000		Hz
			2000		Hz
			4000		Hz
			8000		Hz
			16000		Hz
			32000		Hz

3.2 Accelerometer Specifications

Table 2: Accelerometer specifications

Parameter	Condition	Min	Typ	Max	Unit
Full Scale Range	Selectable via serial digital interface		± 2		g
			± 4		g
			± 8		g
			± 16		g
Sensitivity	Selectable via serial digital interface		16384		LSB/g
			8192		LSB/g
			4096		LSB/g
			2048		LSB/g
Nonlinearity	Best fit straight line		± 0.5		$\%FS$
Cross-axis Sensitivity			± 2		$\%$
Sensitivity Temperature Drift	-40°C - 85°C		± 0.01		$\%/^oC$
Zero_g Temperature Drift	-40°C - 85°C		± 1		$mg/^oC$
Zero_Offset			± 50		mg
Output Noise Density			220		$\mu g/\sqrt{Hz}$
Output Data Rate	Selectable via serial digital interface		16		Hz
			31		Hz
			63		Hz
			125		Hz
			250		Hz
			500		Hz
			1000		Hz
			2000		Hz
			4000		Hz
			8000		Hz

3.3 Temperature Sensor Specifications

Table 3: Temperature sensor specifications

Parameter	Condition	Min	Typ	Max	Unit
Operating Range		-40		85	^oC
25 ^{o}C Output			2500 [1]		LSB
Resolution [2]			12		bit
Sensitivity			16		$LSB/^oC$
Sensitivity Error		-1		1	%
Output Data Rate	Selectable via serial digital interface		500		Hz
			250		Hz
			125		Hz
			63		Hz

1. This is just an empirical value. Using the factory calibrated room temperature offset is recommended for calculating the temperature value.
2. The temperature sensor reading is a 12-bit unsigned value. Refer to 5.2 for further information on how to convert the readings to degrees centigrade.

3.4 Power Modes

Table 4: Power modes

Mode	Condition	Min	Typ	Max	Unit
Normal	High performance		1650		μA
Sleep	Accel only		162		μA
Power Down			14		μA

3.5 Electrical Characteristics

Table 5: Electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDD	Supply Voltage		1.71	3.00	3.60	*V*
VDDIO	Supply Voltage I/O		1.71	1.80	3.60	*V*
Idd	Supply Current	VDD=3.0V		1.65		*mA*
V_{IL}	Digital Low-level Input Voltage				0.3VDDIO	*V*
V_{IH}	Digital High-level Input Voltage		0.7VDDIO			*V*
V_{OL}	Digital Low-level Output Voltage				0.2	*V*
V_{OH}	Digital High-level Output Voltage		VDDIO-0.2			*V*

3.6 Digital Interface Characteristics

3.6.1 Serial Peripheral Interface (SPI)

Subject to general operation conditions like VDD, operating temperature and PCB design.

Table 6: SPI interface characteristics

Symbol	Parameter	Min	Max	Unit
t_{sck}	SPI Clock Period	1		μs
f_{sck}	SPI Frequency		1	MHz
t_{sucsb}	CSB Setup Time	20		ns
t_{hcsb}	CSB Hold Time	20		ns
t_{susdi}	SDI Setup Time	20		ns
t_{hsdi}	SDI Sold Time	20		ns
t_{vdsdo}	SDO Valid Time		120	ns
t_{hsdo}	SDO Hold Time	20		ns
t_{dissdo}	SDO Disable Time		150	ns

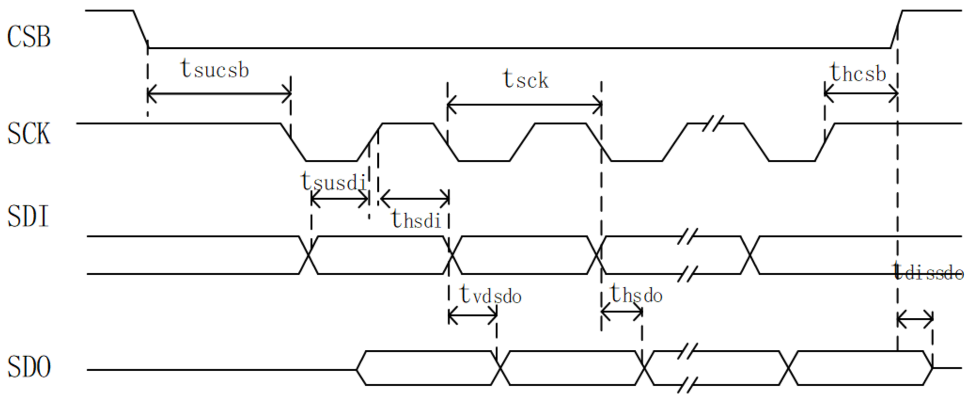

Figure 2: SPI timing diagram

3.6.2 Inter-Integrated Circuit (I^2C)

Subject to general operation conditions like VDD, operating temperature and PCB design.

Table 7: I^2C interface characteristics

Symbol	Parameter	Min	Max	Unit
f_{sck}	I^2C Frequency		1	MHz
t_{low}	I^2C Clock Low Time	0.5		μs
t_{high}	I^2C Clock High Time	0.3		μs
t_{sudat}	SDA Data Setup Time	150		ns
t_{hdat}	SDA Data Hold Time	0	1	μs
t_{sursta}	Repeat Start Condition Setup Time	0.5		μs
t_{hsta}	Start Condition Hold Time	0.5		μs
t_{susp}	Stop Condition Setup Time	0.5		μs

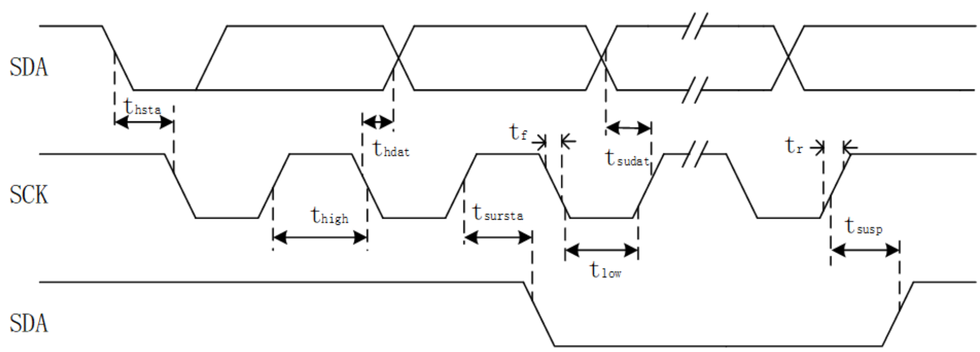

Figure 3: I^2C timing diagram

3.7 Absolute Maximum Ratings

Table 8: Absolute maximum ratings

Parameter	Rating	Unit
Voltage at Supply Pin	-0.6 - 3.6	V
Operating Temperature Range	-40 - 85	^oC
Storage Temperature Range	-40 - 105	^oC
ESD (HBM)	2000	V
ESD (MM)	200	V
Latch_up	JEDEC78E Class I, ±200mA	NA
Mechanical Shock	10000g@0.2ms half sine	NA

Note: Stress above those listed as 'Absolute Maximum Ratings' may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4 Pin Description

4.1 Pin Out View

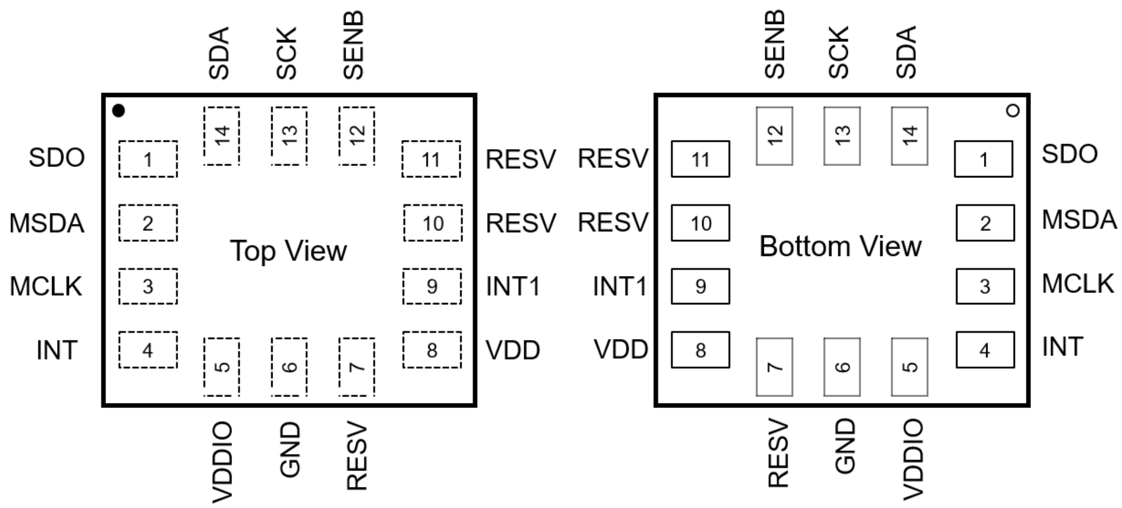

Figure 4: The pin out view of SH3001

4.2 Pin Descriptions

Table 9: Pin descriptions

Pin No.	Pin Name	Description
1	SDO	I^{2}C slave address LSB (A0), serial data output in SPI
2	MSDA	Auxiliary I^{2}C serial data. Connect to external sensors or VDDIO.
3	MCLK	Auxiliary I^{2}C serial clock. Connect to external sensors or VDDIO.
4	INT	Interrupt digital output(totem pole or open-drain). Connect to VDDIO.
5	VDDIO	Digital I/O supply voltage.
6	GND	Ground for power supply.
7	RESV	No connect or connect to VDDIO or GND.
8	VDD	Power supply voltage and digital supply voltage.
9	INT1	Interrupt 1 digital output(totem pole or open-drain). Connect to VDDIO.
10	RESV	No connect or connect to GND or VDDIO.
11	RESV	No connect or connect to VDDIO or connect to GND.
12	SENB	I^{2}C/SPI (CSB) protocol select. 1: SPI idle mode/ I^{2}C communication enabled; 0: SPI communication mode/ I^{2}C disabled.
13	SCK	I^{2}C serial clock, SPI serial clock.
14	SDA	I^{2}C serial data, serial data input SDI in SPI.

5 Functional Explanations

5.1 Six–Axis MEMS Sensor With 16-bit ADCs and Signal Conditioning

SH3001 consists of a three-axis angular rate sensor and a three-axis acceleration sensor. It detects rotation and acceleration on the X, Y and Z axes. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate or the acceleration. For each axis an on-chip 16-bit ADC is used to digitize the output voltage. The full-range of the gyroscope is programmable at $\pm 125\ dps$, $\pm 250\ dps$, $\pm 500\ dps$, $\pm 1000\ dps$ and $\pm 2000\ dps$ and the full-range of the accelerometer is programmable at $\pm 2\ g$, $\pm 4\ g$, $\pm 8\ g$ and $\pm 16\ g$.

5.2 Digital Output Temperature Sensor

An on-chip temperature sensor is used to measure chip temperature of SH3001. It is enabled by setting 0x20[7] to '1' and 0xD5[2] to '0'. The readings from the sensor can be read from the TEMP_DATA registers (0x0D[3:0] and 0x0C[7:0]) and the factory calibrated room temperature offset is stored in the ROOM_TEMP registers (0x20[3:0] and 0x21[7:0]).

Both temperature readings and room temperature are 12-bit unsigned values and the temperature value can be converted to degrees centigrade by using the following formula:
Temperature (^oC) = (TEMP_DATA - ROOM_TEMP)/16 + 25

5.3 Auxiliary I²C Serial Interface

SH3001 contains an auxiliary I^2C bus which allows an external system processor to act as master and directly communicates to external sensors connected to the secondary I^2C bus pins (MSDA and MSCK) by setting 0xFD[0] to '1'. This is useful for configuring external devices, or for keeping SH3001 in a low-power mode. In this mode, the secondary I^2C bus control logic (third-party sensor interface block) of the SH3001 is disabled, and the secondary I^2C pins MSDA and MSCK are connected to the main I^2C bus through analog switches.

5.4 FIFO

SH3001 contains a 1kB FIFO that is accessible via the serial interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyroscope data, accelerometer data, temperature readings and auxiliary I^2C device input. Down sampling of both gyroscope and accelerometer data can be configured in register 0x39.

It can work in 4 modes determined by register 0x35[1:0].

Disable: FIFO is not operational and it remains empty.

FIFO Mode: Data from measurements are stored in FIFO. When the number of samples in FIFO equals the level specified in the watermark register (0x37[2:0] and 0x36[7:0]), the watermark interrupt is fired. FIFO continues to accumulate data until it is full and then stops collecting data. The watermark interrupt continues to occur until the number of samples in FIFO is less than the value stored in the watermark register.

Stream Mode: Data from measurements are stored in FIFO. When the number of samples in FIFO equals the level specified in the watermark register, the watermark interrupt bit is set. FIFO continues accumulating samples and holds the latest samples, discarding older data as new data arrives; The watermark interrupt continues to occur until the number of samples in FIFO is less than the value stored in the watermark register.

Trigger Mode: FIFO accumulates samples, holding the latest samples from measurements. After a trigger event occurs and an interrupt is sent, FIFO keeps the last n samples (where n is the value specified by the watermark register) and then operates in FIFO mode, collecting new samples only when FIFO is not full.

Note that the FIFO data should be read first because setting the device into FIFO disable mode clears FIFO.

5.5 Interrupt

5.5.1 General Features

SH3001 contains 13 programmable interrupts and utilizes output pin INT or INT1 to send signal to an external microprocessor as an interrupt event occurs. Interrupts can be enabled or disabled by configuring interrupt control registers. The status register will be read by the external microprocessor to check the types of interrupt. There are three interrupt modes: automatically clear, latched and non-latched. New data ready interrupt is automatically cleared after a fixed time. Other interrupts can be configured as latched (set 0x44[6] to ’0’) or non-latched(set 0x44[6] to ’1’) modes. Non-latched interrupts will be cleared after a defined period of time (defined by 0x45). For latched interrupts, there are two ways to clear the interrupts: random read clear (set 0x44[4] to ’1’) or status read clear (set 0x44[4] to ’0’).

The interrupt pins can be set as either open-drain output or normal output by configuring register 0x44[2] for pin INT1 and 0x44[0] for pin INT. When setting register value to ’1’ (’0’), the output pin is open-drain (normal) output. The active level of interrupt pins is determined by register 0x44[7]. When setting register 0x44[7] to ’0’(’1’), the active level of interrupt pins is active high (low).

All the thresholds for interrupts are unsigned values.

Table 10: Interrupts supported by SH3001

Index	Interrupt Name	Enable	Pin Assigning	Flag
1	Inactivity Interrupt	0x40[5]	0x79[6]	0x10[0] & 0x14[7:4]
2	Activity Interrupt	0x40[4]	0x79[5]	0x10[1] & 0x14[7:4]
3	Double Tap Interrupt	0x40[3]	0x79[3]	0x10[2] & 0x14[3:0]
4	Single Tap Interrupt	0x40[2]	0x79[2]	0x10[3] & 0x14[3:0]
5	Tap Interrupt	0x40[2]/[3]	0x79[4]	0x10[4] & 0x14[3:0]
6	Flat Interrupt	0x40[1]	0x79[1]	0x10[5]
7	Orient Interrupt	0x40[0]	0x79[0]	0x10[6]
8	Free Fall Interrupt	0x41[0]	0x7A[1]	0x10[7]
9	Water Mark Interrupt	0x41[4]	0x7A[5]	0x11[0]
10	Gyro Data Ready Interrupt	0x41[3]	0x7A[4]	0x11[1]
11	Acc Data Ready Interrupt	0x41[1]	0x7A[2]	0x11[3]
12	Low-G Interrupt	0x40[7]	0x7A[0]	0x12[0]
13	High-G interrupt	0x40[6]	0x79[7]	0x12[7:4]

5.5.2 Inactivity Interrupt

Inactivity detection uses consecutive acceleration values to detect lack of motion. Inactivity interrupt is enabled (disabled) by writing '1' ('0') to register 0x40[5]. There are two types of operation for inactivity detection: AC Mode and DC Mode. By writing '1' ('0') to register 0x4F[3], AC Mode (DC Mode) operation is selected.

In AC Mode operation for inactivity detection, if the slopes of all axes is lower than preset threshold defined by 0x57, and hold time is longer than that set in 0x58, the interrupt is fired.

In DC Mode operation, the square of current acceleration magnitude is compared with the $INACT\_THR$ defined by the INACT_INT_THR registers (0x7C: high byte, 0x7B: middle byte and 0x57: low byte) to determine whether inactivity is detected. The square of current acceleration magnitude is defined as follows:

$$Curr\_Acc^2 = |acc\_x^2 + acc\_y^2 + acc\_z^2 - 1G^2| \tag{1}$$

The reference 1G in the above equation is defined by the register 0x7E and 0x7D. If $Curr\_Acc^2 < 64 \times INACT\_THR$, inactivity interrupt is fired.

Each axis can be individually selected to participate in detecting inactivity. The axis participates the inactivity detection is determined by register 0x4F[2:0]. A setting of 0 excludes the selected axis from participation. If all axes are excluded, the function is disabled. For inactivity detection, all participating axes are logically AND, causing the inactivity function to trigger when all of the participating axes are less than the threshold for at least a period of time specified in register 0x58.

The interrupt status is stored in register 0x10[0] and 0x14[7:4]. The inactivity interrupt supplies additional information about the detected inactivity. The axis that triggers the interrupt is indicated by register 0x14[6:4] that contains a value of '1'. The sign of the triggering slope is held in register 0x14[7] until the interrupt is retriggered. If register 0x14[7] = '0' ('1'), the sign is positive (negative).

5.5.3 Activity Interrupt

Activity detection uses consecutive acceleration values to detect changes in motion. Activity detection interrupt is enabled (disabled) by writing '1' ('0') to register 0x40[4]. There are two types of operation for activity detection: AC Mode and DC Mode. By writing '1' ('0') to register 0x4F[7], AC Mode (DC Mode) operation is selected.

The activity interrupt threshold is defined by register 0x55.

In DC Mode operation, the current acceleration magnitude is compared directly with activity interrupt threshold to determine whether activity is detected.

In AC Mode operation for activity detection, the acceleration value at the start of activity detection is taken as a reference value. New samples of acceleration are then compared to this reference value. If the magnitude of the difference exceeds the activity interrupt threshold, activity interrupt is fired.

Activity interrupt is generated only after a predefined number of consecutive acceleration values exceed the value defined by 0x55. The number is set by the register 0x56.

Each axis can be individually selected to participate in detecting activity. The axis participates activity detection is determined by register 0x4F[6:4]. A setting of '0' excludes the selected axis from participation. If all axes are excluded, the function is disabled. For activity detection, all participating axes are logically OR, causing the activity function to trigger when any of the participating axes exceeds the activity threshold for consecutive number of samples defined by register 0x56.

The interrupt status is stored in register 0x10[1]. The activity interrupt supplies additional information about the detected activity. The axis which triggers the interrupt is given by register 0x14[6:4] that contains a value of '1'. The sign of the triggering slope is held in register 0x14[7] until the interrupt is retriggered. If register 0x14[7] = '0 ('1'), the sign is positive (negative).

5.5.4 Double & Single Tap Interrupt

A tap event is detected if a pre-defined slope of the acceleration of at least one axis exceeds the threshold. Two different tap events are distinguished : a 'Single Tap' is a single event within a certain time and a 'Double Tap' consists of a single tap followed by a second event within a defined period of time.

- Step 1: The absolute value/64 of an axis is more than preset threshold through 0x51.
- Step 2: The large value last time should shorter than the period defined by 0x52; Single Tap is recognized, but need to prove no Double Tap.
- Step 3: Disable value comparator before the duration end which is set by 0x53.
- Step 4: Compare absolute value with threshold within the duration set by 0x54; If no large sample detected in this duration, Single Tap Interrupt is fired. Else go to Step 5.
- Step 5: If the large value last time is longer than the period defined by 0x52, Single Tap is proved. Otherwise, Double Tap is proved.

5.5.5 Tap Interrupt

Both Single Tap and Double Tap will cause Tap Interrupt.

5.5.6 Flat Interrupt

The flat detection feature gives information about the orientation of the device's z-axis relative to the g-vector. It recognizes whether the device is in a flat position or not. The flat angle θ is defined as:

$$\theta = atan(\sqrt{\frac{acc\_x^2 + acc\_y^2}{acc\_z^2}}) \tag{2}$$

in the above equation, acc_x, acc_y, acc_z are the x, y and z axis outputs of the accelerometer. If $acc\_x = acc\_y = 0$ and $acc\_z = 1g$, $\theta = 0$, indicating that the device is in a totally flat position. Similarly, the value of $8 \times tan^2\theta$ is compared with the threshold value defined by 0x4E[5:0] by the interrupt engine. If $8 \times tan^2\theta$ is less than the threshold and keeps enough time defined in 0x4E[7:6], Flat Interrupt is fired.

5.5.7 Orientation Interrupt

The orientation interrupt informs on an orientation change of the sensor with respect to the gravitational field vector g. There are the orientations upward/downward and orthogonal to that portrait upright, landscape left, portrait downside, and landscape right.
The sensor orientation is defined by the angles φ and θ (φ is rotation around the stationary z axis and θ is rotation around the stationary y axis). Therefore the magnitudes of the acceleration vectors are calculated as follows:

$$\begin{cases} acc\_x = 1g \times sin\theta \times cos\varphi \\ acc\_y = -1g \times sin\theta \times sin\varphi \\ acc\_z = 1g \times cos\theta \end{cases} \tag{3}$$

According to equation 3, if the outputs of three axes are given, the orientation angles are calculated as follows:

$$\begin{cases} \varphi = -atan(\frac{acc\_y}{acc\_x}) \\ \\ \theta = atan(\sqrt{\frac{acc\_x^2+acc\_y^2}{acc\_z^2}}) \end{cases} \tag{4}$$

Depending on the value of orientation angles the orientation of the device in space is determined and stored in the orientation status register 0x15[2:0] . There are three orientation calculation modes: symmetrical, high-asymmetrical and low-asymmetrical. The mode is selected by the register 0x47[1:0].
The engine uses 16-bit acceleration data for the orientation recognition. For upside or downside orientation, 0x15[2] has the definition:
$0 \rightarrow$ Upward $acc\_z > 0$
$1 \rightarrow$ Downward $acc\_z < 0$
Both portrait/landscape and upside/downside recognition use a hysteresis (*hyst*) which is decided by 0x4D and 0x4C. For each orientation mode, 0x47[1:0] has different meanings as shown in the following tables.

Table 11: Meaning of the orient mode register in symmetrical mode

0x15[1:0]	Name	Condition
00	Landscape left	$\|acc\_y\| < \|acc\_x\| - hyst \quad \& \quad acc\_x \geq 0$
01	Landscape right	$\|acc\_y\| < \|acc\_x\| - hyst \quad \& \quad acc\_x \leq 0$
10	Portrait upside down	$\|acc\_y\| > \|acc\_x\| + hyst \quad \& \quad acc\_y \leq 0$
11	Portrait upright	$\|acc\_y\| > \|acc\_x\| + hyst \quad \& \quad acc\_y \geq 0$

Table 12: Meaning of the orient mode register in high-asymmetrical mode

0x15[1:0]	Name	Condition
00	Landscape left	$\|acc\_y\| < 2 \times (\|acc\_x\| - hyst) \quad \& \quad acc\_x \geq 0$
01	Landscape right	$\|acc\_y\| < 2 \times (\|acc\_x\| - hyst) \quad \& \quad acc\_x \leq 0$
10	Portrait upside down	$\|acc\_y\| > 2 \times \|acc\_x\| + hyst \quad \& \quad acc\_y \leq 0$
11	Portrait upright	$\|acc\_y\| > 2 \times \|acc\_x\| + hyst \quad \& \quad acc\_y \geq 0$

Table 13: Meaning of the orient mode register in low-asymmetrical mode

0x15[1:0]	Name	Condition
00	Landscape left	$\|acc\_y\| < (\|acc\_x\| - hyst)/2 \quad \& \quad acc\_x \geq 0$
01	Landscape right	$\|acc\_y\| < (\|acc\_x\| - hyst)/2 \quad \& \quad acc\_x \leq 0$
10	Portrait upside down	$\|acc\_y\| > \|acc\_x\|/2 + hyst \quad \& \quad acc\_y \leq 0$
11	Portrait upright	$\|acc\_y\| > \|acc\_x\|/2 + hyst \quad \& \quad acc\_y \geq 0$

It is possible to block the Orientation Interrupt. The Orientation Interrupt blocking feature is configured via 0x47[3:2]. The value of '1.5g' is defined by 0x49 and 0x48. The value of the slope threshold is defined by 0x4B and 0x4A.

The meaning of 0x47[3:2] is listed as follows:
'00': Orientation Interrupt blocking is disabled.
'01': Orientation Interrupt will be blocked if the device is close to the horizontal position or acceleration of any axis is larger than 1.5g.
'10': Orientation Interrupt will be blocked if the device is close to the horizontal position or acceleration of any axis is larger than 1.5g or the slope is larger than 0.2g.
'11': Orientation Interrupt will be blocked if the device is close to the horizontal position or the slope is larger than 0.4g or acceleration of any axis is larger than 1.5g or another orientation change is detected within 100ms.

5.5.8 FIFO Watermark Interrupt

Generate interrupt when FIFO data count is equal to the hold level defined in 0x37[2:0] and 0x36.

5.5.9 Gyroscope Data Ready Interrupt

Generate interrupt when gyroscope data is ready. If interrupt is not latched, INT can be consider as a clock signal with programmable duty cycle and right INT_Length settings.

5.5.10 Accelerometer Data Ready Interrupt

Generate interrupt when accelerometer data is ready. If interrupt is not latched, INT can be consider as a clock signal with programmable duty cycle and right INT_Length settings.

5.5.11 Free-fall Interrupt

Free-fall detection detects whether the device is falling. If the sum of absolute accelerations of all three axes $|acc\_x| + |acc\_y| + |acc\_z|$ is less than the threshold set by register 0x5E for a period time longer than the value is specified in the register 0x5F, free-fall interrupt is generated. The free-fall interrupt is enabled (disabled) by writing '1' ('0') to register 0x41[0] and the interrupt status is stored in register 0x10[7].

The register 0x5E defines the threshold value. The meaning of register 0x5E depends on the range setting. The sum of absolute acceleration of all axes $|acc\_x| + |acc\_y| + |acc\_z|$ is compared with the value in register 0x5E to determine if a free-fall event occurred.

The register 0x5F defines the time value representing the minimum time that the value of all axes must be less than register 0x5E to generate a free-fall interrupt. The scale factor is 2ms/LSB. A value of 0 may result in undesirable behavior if the free-fall interrupt is enabled. Values between 100 ms and 350 ms (0x32 to 0xAF) are recommended.

5.5.12 Low-G Interrupt

Low-G interrupt is based on the comparison of acceleration data against a low-g threshold defined in 0x5C. If the absolute values of the acceleration of all axes are lower than the threshold and last time is longer than the period defined in 0x5D, Low-G interrupt is fired.

5.5.13 High-G Interrupt

High-G Interrupt is based on the comparison of acceleration data against a high-g threshold defined in 0x5A. If the absolute value of enabled axis is larger than the high-g threshold and last time is longer than the period defined in 0x5B,High-G interrupt is fired .

6 Digital Interfaces

6.1 General Description

SH3001 has both primary (I^{2}C and SPI configurable) and secondary interfaces. The secondary interface supports I^{2}C only. The secondary I^{2}C bus allows an external processor to act as master and communicates with the external device connected to the secondary I^{2}C bus pins (MSDA and MSCK). This is useful for configuring a magnetometer along with SH3001 to build a 9-DoF solution. In this mode, the secondary I^{2}C bus control logic of SH3001 is disabled, and the secondary I^{2}C pins MSDA and MSCK are connected to the main I^{2}C bus through analog switches.

The diagram below shows an application processor can communicate with an external digital output sensor connected to SH3001 through the auxiliary I^{2}C bus.

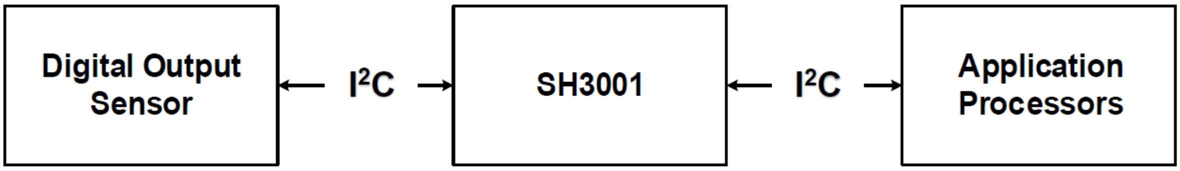

Figure 5: Connection diagram through the auxiliary I^{2}C bus

6.2 Primary Interfaces

By default, SH3001 operates in I^{2}C mode. It can also be configured to operate in SPI mode. I^{2}C and SPI digital interfaces share partly the same pins.

6.2.1 Primary Interface I^{2}C/SPI Protocol Selection

The protocol is automatically selected based on the chip select CSB pin behavior after power-up. At power-up, SH3001 is in I^{2}C mode. If CSB is connected to VDDIO during power-up and not changed then SH3001 works in I^{2}C mode. The interface switches from I^{2}C to SPI mode if a 'high' to 'low' transition happens on CSB pin.

6.2.2 Primary SPI Interface

The SPI interface of SH3001 is compatible with two modes, '00' (CPOL ='0' and CPHA='0') and '11' (CPOL ='1' and CPHA ='1'). The automatic selection between '00' and '11' is controlled based on the value of SCK after a falling edge of CSB. The page1 or page2 registers can be accessed by setting register 0x7F[0] to '0' or '1'.
The basic write, read and multiple write, read operations are illustrated in below waveforms.

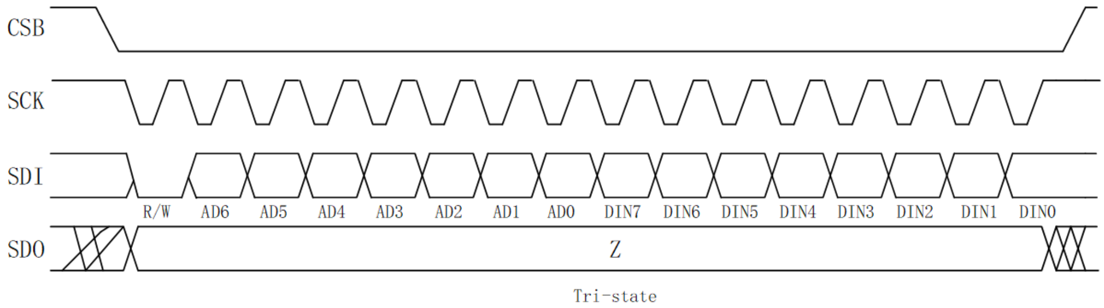

Figure 6: 4-wire SPI write sequence

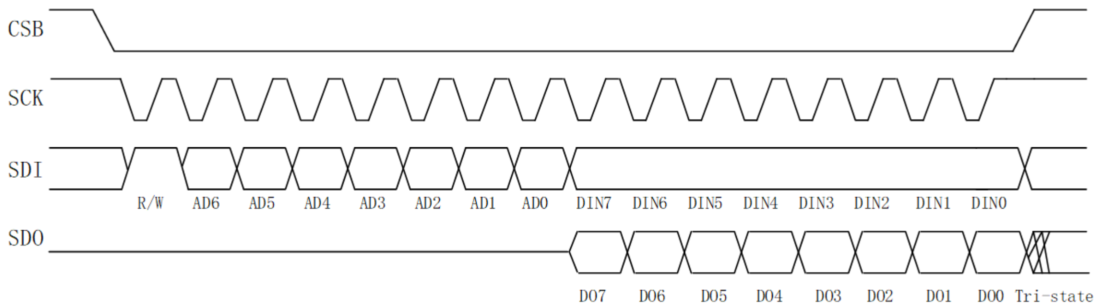

Figure 7: 4-wire SPI read sequence

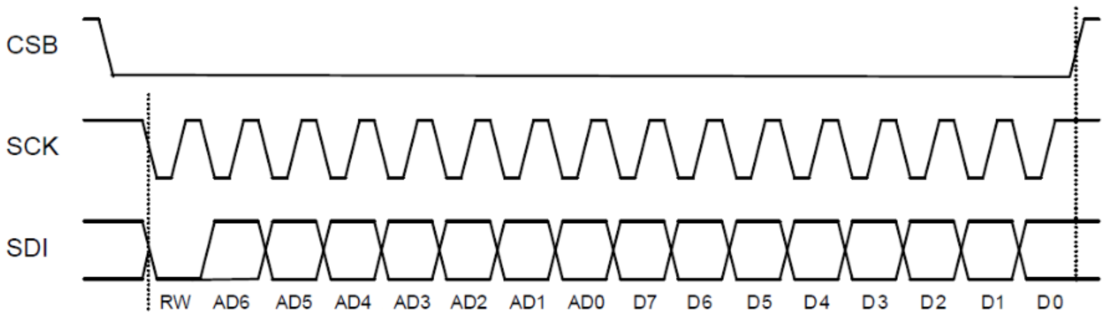

Figure 8: 3-wire SPI read and write sequence

The data bits shown in above waveforms are:
Bit[0]: Read/Write bit. When ’0’, the data SDI is written into the chip. When ’1’, the data SDO are read out from them chip.
Bit[1:7]: Address AD[6:0].
Bit[8:15]: In write mode, these are the data from SDI written into the address AD. In read mode, these are data read from the address AD.

Multiple read and write operations are done by keeping CSB low and continuing the data transaction and only the first address is written, addresses are automatically incremented internally as long as CSB stays active.

Multiple read and write are shown in figures below:

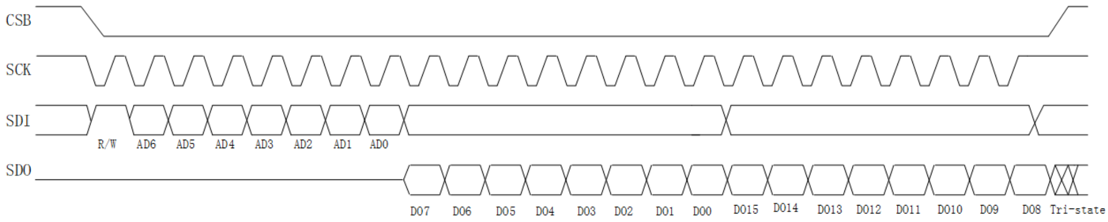

Figure 9: 4-wire SPI multiple read sequence

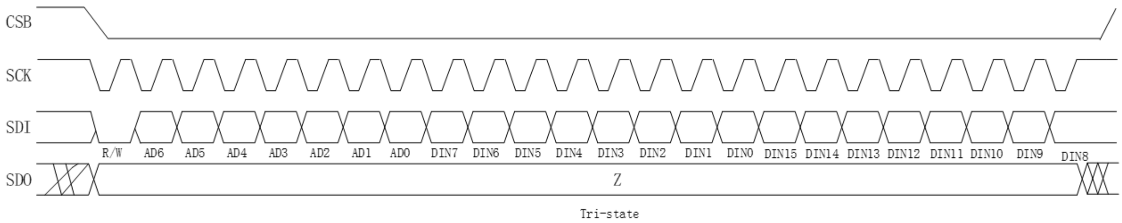

Figure 10: 4-wire SPI multiple write sequence

6.2.3 Primary I^{2}C Interface

The I^{2}C interface of SH3001 is a slave bus. There are two signals associated with the I^{2}C bus: the serial clock SCL and serial data SDA. The SDA is a bi-directional line used to send or receive data from the interface. Both lines must be connected to VDDIO through external pull-up resistors.

The default I^{2}C address of SH3001 is 0b0110110. It is used if the SDO pin is pulled to 'GND'. The alternative address 0b0110111 is selected by pulling SDO to 'VDDIO'.

The I^{2}C bus is implemented with both fast mode (400 kHz) and standard mode.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver then must pull the SDA line 'low' so it remains low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The transaction begins with a start (ST) condition generated by master, followed by 7 bits slave address (SAD) and 1 read/write bit, then the master sends the one byte register address (RAD). If it is a read operation, a repeated start (SR) condition must be issued after the register address byte. If it is a write operation, the master will transmit data which will be written into the register addressed by register address byte. The slave sends out slave acknowledge condition (ACK) after the slave address issued by master matches its slave address, and after master sends out register address and receives data byte written by master. The master must assert master acknowledge condition (MACK) after receives data from slave.

Data are transferred in byte format with MSB sent out first. The number of bytes transferred is unlimited until no master acknowledge (MNACK) condition asserted by master for read operation, or when master issues stop condition for write operation.

Master	ST	SAD+W		RADR		DATA		SP
Slave			ACK		ACK		ACK	

Figure 11: I^{2}C single byte write

Master	ST	SAD+W		RADR		RS	SAD+R			MNACK	SP
Slave			ACK		ACK			ACK	DATA		

Figure 12: I^{2}C single byte read

Master	ST	SAD+W		RADR		DATA		DATA		SP
Slave			ACK		ACK		ACK		ACK	

Figure 13: I^{2}C multiple bytes write

Master	ST	SAD+W		RADR		RS	SAD+R			MACK		MNACK	SP
Slave			ACK		ACK			ACK	DATA		DATA		

Figure 14: I^{2}C multiple bytes read

7 Register Descriptions

7.1 Register Descriptions

7.1.1 Register 0x00 - 0x05: Accelerometer Data

Name: ACC_XDATA_L
Address: 0x00

Bit	Access	Default	Description
[7:0]	RO		Low byte of acc X-axis data

Name: ACC_XDATA_H
Address: 0x01

Bit	Access	Default	Description
[7:0]	RO		High byte of acc X-axis data

Name: ACC_YDATA_L
Address: 0x02

Bit	Access	Default	Description
[7:0]	RO		Low byte of acc Y-axis data

Name: ACC_YDATA_H
Address: 0x03

Bit	Access	Default	Description
[7:0]	RO		High byte of acc Y-axis data

Name: ACC_ZDATA_L
Address: 0x04

Bit	Access	Default	Description
[7:0]	RO		Low byte of acc Z-axis data

Name: ACC_ZDATA_H
Address: 0x05

Bit	Access	Default	Description
[7:0]	RO		High byte of acc Z-axis data

7.1.2 Register 0x06 - 0x0B: Gyroscope Data

Name: GYRO_XDATA_L
Address: 0x06

Bit	Access	Default	Description
[7:0]	RO		Low byte of gyro X-axis data

Name: GYRO_XDATA_H
Address: 0x07

Bit	Access	Default	Description
[7:0]	RO		High byte of gyro X-axis data

Name: GYRO_YDATA_L
Address: 0x08

Bit	Access	Default	Description
[7:0]	RO		Low byte of gyro Y-axis data

Name: GYRO_YDATA_H
Address: 0x09

Bit	Access	Default	Description
[7:0]	RO		High byte of gyro Y-axis data

Name: GYRO_ZDATA_L
Address: 0x0A

Bit	Access	Default	Description
[7:0]	RO		Low byte of gyro Z-axis data

Name: GYRO_ZDATA_H
Address: 0x0B

Bit	Access	Default	Description
[7:0]	RO		High byte of gyro Z-axis data

7.1.3 Register 0x0C - 0x0D: Temperature Data

Name: TEMP_DATA_L
Address: 0x0C

Bit	Access	Default	Description
[7:0]	RO		Low 8 bits of temperature data

Name: TEMP_DATA_H
Address: 0x0D

Bit	Access	Default	Description
[7:4]			Reserved
[3:0]	RO		High 4 bits of temperature data

7.1.4 Register 0x0F: Chip ID

Name: CHIP_ID
Address: 0x0F

Bit	Access	Default	Description
[7:0]	RO	01100001	The default Chip ID of this device is 0x61

7.1.5 Register 0x10 - 0x15: Interrupt Status

Name: INTERRUPT_STATUS_0
Address: 0x10

Bit	Access	Default	Description
7	RO	0	Free-fall Interrupt status. 1: Active; 0: Not Active
6	RO	0	Orientation Interrupt status. 1: Active; 0: Not Active
5	RO	0	Flat Interrupt status. 1: Active; 0: Not Active
4	RO	0	Tap Interrupt status. 1: Active; 0: Not Active
3	RO	0	Single Tap Interrupt status. 1: Active; 0: Not Active
2	RO	0	Double Tap Interrupt status. 1: Active; 0: Not Active
1	RO	0	Activity Interrupt status. 1: Active; 0: Not Active
0	RO	0	Inactivity Interrupt status. 1: Active; 0: Not Active

Name: INTERRUPT_STATUS_1
Address: 0x11

Bit	Access	Default	Description
[7:4]			Reserved
3	RO	0	Acc Data Ready Interrupt status. 1: Active; 0: Not Active
2	RO	0	Acc FIFO Watermark Interrupt status. 1: Active; 0: Not Active
1	RO	0	Gyro Ready Interrupt status. 1: Active; 0: Not Active
0	RO	0	Gyro FIFO Watermark Interrupt status. 1: Active; 0: Not Active

Name: INTERRUPT_STATUS_2
Address: 0x12

Bit	Access	Default	Description
7	RO	0	Sign of acceleration that trigger High-G Interrupt. 1: Negative; 0: Positive
6	RO	0	Whether High-G Interrupt is triggered by X axis. 1: Yes; 0: No
5	RO	0	Whether High-G Interrupt is triggered by Y axis. 1: Yes; 0: No
4	RO	0	Whether High-G Interrupt is triggered by Z axis. 1: Yes; 0: No
[3:1]			Reserved
0	RO	0	Low-G Interrupt status, 1: Active; 0: Not Active

Name: INTERRUPT_STATUS_3
Address: 0x14

Bit	Access	Default	Description
7	RO	0	Sign of acceleration that trigger Activity or Inactivity Interrupt. 1: Negative; 0: Positive
6	RO	0	Whether Activity or Inactivity Interrupt is triggered by X axis. 1: Yes; 0: No
5	RO	0	Whether Activity or Inactivity Interrupt is triggered by Y axis. 1: Yes; 0: No
4	RO	0	Whether Activity or Inactivity Interrupt is triggered by Z axis. 1: Yes; 0: No
3	RO	0	Sign of acceleration that trigger Single or Double Tap Interrupt. 1: Negative; 0: Positive
2	RO	0	Whether Single or Double Tap Interrupt is triggered by X axis. 1: Yes; 0: No
1	RO	0	Whether Single or Double Tap Interrupt is triggered by Y axis. 1: Yes; 0: No
0	RO	0	Whether Single or Double Tap Interrupt is triggered by Z axis. 1: Yes; 0: No

Name: INTERRUPT_STATUS_4
Address: 0x15

Bit	Access	Default	Description
[7:3]			Reserved
2	RO	0	Orientation Interrupt Value of Z-axis. 1: Downward ; 0: Upward
[1:0]	RO	00	Orientation Interrupt Value of X and Y-axis. 00: Landscape left; 01: Landscape right; 10: Portrait upside down; 11: Portrait upright

7.1.6 Register 0x16 - 0x17: FIFO Status

Name: FIFO_STATUS_0
Address: 0x16

Bit	Access	Default	Description
[7:0]	RO	00000000	Lower 8 bits of FIFO entries count

Name: FIFO_STATUS_1
Address: 0x17

Bit	Access	Default	Description
[7:6]			Reserved
5	RO	0	Whether FIFO Watermark has been reached. 1: Yes 0: No
4	RO	0	Whether FIFO is full. 1: Yes 0: No
3	RO	0	Whether FIFO is empty. 1: Yes 0: No
[2:0]	RO	000	Higher 3 bits of FIFO entries count

7.1.7 Register 0x18: FIFO Data

Name: FIFO_Data
Address: 0x18

Bit	Access	Default	Description
[7:0]	RO	00000000	FIFO Data

7.1.8 Register 0x20 - 0x21 & 0xD5: Temperature Sensor Configuration

Name:TEMP_SENSOR_CONFIG0
Address: 0x20

Bit	Access	Default	Description
7	RW	1	Temp Sensor Enable (Digital). 0: Disable; 1: Enable
6			Reserved
[5:4]	RW	11	Temp Sensor ODR. 00: 500Hz; 01: 250Hz; 10: 125Hz; 11: 63Hz
[3:0]	RW		High 4 bits of room temperature

Name:TEMP_SENSOR_CONFIG1
Address: 0x21

Bit	Access	Default	Description
[7:0]	RW		Low 8 bits of room temperature

Name:TEMP_SENSOR_CONFIG2
Address: 0xD5

Bit	Access	Default	Description
[7:3]			Reserved
[2]	RW	1	Temp Sensor Enable (Analog). 0: Enable; 1: Disable
[1:0]			Reserved

7.1.9 Register 0x22 - 0x26: Accelerometer Configuration

Name:ACC_CONFIG_0
Address: 0x22

Bit	Access	Default	Description
7	RW	0	Acc work mode. 1: Low power mode; 0: Normal mode
6	RW	0	Acc ADC dither enable. 1: Enable, 0: Disable
[5:1]			Reserved
0	RW	1	Acc digital filter enable. 1: Enable; 0: Disable

Name:ACC_CONFIG_1
Address: 0x23

Bit	Access	Default	Description
[7:4]			Reserved
[3:0]	RW	0000	Acc ODR configuration. 0000: 1000Hz; 0001: 500Hz; 0010: 250Hz; 0011: 125Hz; 0100: 63Hz; 0101: 31Hz; 0110: 16Hz; 1000: 2000Hz; 1001: 4000Hz 1010: 8000Hz

Name:ACC_CONFIG_2
Address: 0x25

Bit	Access	Default	Description
[7:3]			Reserved
[2:0]	RW	010	Acc range configuration. 010: ± 16g; 011: ± 8g; 100: ± 4g; 101: ± 2g

Name:ACC_CONFIG_3
Address: 0x26

Bit	Access	Default	Description
[7:5]	RW	001	Acc low pass filter cut-off frequency configuration, 000: ODR × 0.40; 001: ODR × 0.25; 010: ODR × 0.11; 011: ODR × 0.04; 100: ODR × 0.02
4			Reserved
3	RW	0	Whether bypass acc low pass filter, 1: Yes; 0: No
[2:0]			Reserved

7.1.10 Register 0x28 - 0x2B & 0x8F & 0x9F & 0xAF: Gyroscope Configuration

Name: GYRO_CONFIG_0
Address: 0x28

Bit	Access	Default	Description
[7:5]			Reserved
4	RW	0	Whether shut down gyroscope as Inactivity Interrupt detected. 1: Yes; 0: No
[3:1]			Reserved
0	RW	1	Gyroscope digital filter enable. 1:Enable; 0:Disable

Name: GYRO_CONFIG_1
Address: 0x29

Bit	Access	Default	Description
[7:4]			Reserved
[3:0]	RW	0000	Gyroscope ODR. 0000: 1000Hz; 0001: 500Hz; 0010: 250Hz; 0011: 125Hz; 0100: 63Hz; 0101: 31Hz; 1000: 2kHz; 1001: 4kHz; 1010: 8kHz; 1011: 16kHz; 1100: 32kHz

Name: GYRO_CONFIG_2
Address: 0x2B

Bit	Access	Default	Description
[7:5]			Reserved
4	RW	0	Gyroscope digital LPF bypass enable. 1: Enable; 0: Disable
[3:2]	RW	00	Gyroscope digital LPF cut-off frequency configuration, refer to Table 14
[1:0]			Reserved

Table 14: Gyroscope digital LPF cut-off frequency configuration (unit: Hz)

ODR (Hz) / 0x2B[3:2]	32k	16k	8k	4k	1000	500	250	125	63	31
00	2000	1600	1313	1138	363	181	90	45	23	11
01	1525	1000	438	438	320	160	80	40	20	10
10	1138	638	313	313	250	125	63	31	15	8
11	863	438	213	219	200	100	50	25	13	6

Name: GYRO_CONFIG_3
Address: 0x8F

Bit	Access	Default	Description
[7:3]			Reserved
[2:0]	RW	110	Gyroscope X-axis full scale range. 010: 125dps; 011: 250dps; 100: 500dps; 101: 1000dps; 110: 2000dps

Name: GYRO_CONFIG_4
Address: 0x9F

Bit	Access	Default	Description
[7:3]			Reserved
[2:0]	RW	110	Gyroscope Y-axis full scale range. 010: 125dps; 011: 250dps; 100: 500dps; 101: 1000dps; 110: 2000dps

Name: GYRO_CONFIG_5
Address: 0xAF

Bit	Access	Default	Description
[7:3]			Reserved
[2:0]	RW	110	Gyroscope Z-axis full scale range. 010: 125dps; 011: 250dps; 100: 500dps; 101: 1000dps; 110: 2000dps

7.1.11 Register 0x32: SPI Configuration

Name: SPI_CONFIG
Address: 0x32

Bit	Access	Default	Description
[7:1]			Reserved
0	RW	0	SPI work mode configuration. 1: 3-wire mode; 0: 4-wire mode

7.1.12 Register 0x35 - 0x39: FIFO Configuration

Name: FIFO_CONFIG_0
Address: 0x35

Bit	Access	Default	Description
7	RW	0	1: Reset FIFO controller; 0: Normal operation mode
[6:2]			Reserved
[1:0]	RW	00	FIFO mode select. 00: Disable; 01: FIFO Mode; 10: Stream Mode; 11: Trigger Mode

Name: FIFO_CONFIG_1
Address: 0x36

Bit	Access	Default	Description
[7:0]	RW	00000000	FIFO watermark level setup bit[7:0]

Name: FIFO_CONFIG_2
Address: 0x37

Bit	Access	Default	Description
[7:6]			Reserved
5	RW	0	Whether external sensor Z data is in FIFO. 1: Yes; 0: No
4	RW	0	Whether external sensor Y data is in FIFO. 1: Yes; 0: No
3			Reserved
[2:0]	RW	000	FIFO watermark level setup bit[10:8]

Name: FIFO_CONFIG_3
Address: 0x38

Bit	Access	Default	Description
7	RW	0	Whether external sensor X data is in FIFO. 1: Yes; 0: No
6	RW	0	Whether temperature sensor data is in FIFO. 1: Yes; 0: No
5	RW	0	Whether gyroscope Z axis data is in FIFO. 1: Yes; 0: No
4	RW	0	Whether gyroscope Y axis data is in FIFO. 1: Yes; 0: No
3	RW	0	Whether gyroscope X axis data is in FIFO. 1: Yes; 0: No
2	RW	0	Whether accelerometer Z axis data is in FIFO. 1: Yes; 0: No
1	RW	0	Whether accelerometer Y axis data is in FIFO. 1: Yes; 0: No
0	RW	0	Whether accelerometer X axis data is in FIFO. 1: Yes; 0: No

Name: FIFO_CONFIG_4
Address: 0x39

Bit	Access	Default	Description
7	RW	0	Accel data down sample for FIFO enable. 1: Enable; 0: Disable
[6:4]	RW	000	Accel data down sample ratio to ODR. 000: 1/2; 001: 1/4; 010: 1/8; 011: 1/16; 100: 1/32; 101: 1/64; 110: 1/128; 111: 1/256
3	RW	0	Gyro data down sample for FIFO enable. 1: Enable; 0: Disable
[2:0]	RW	000	Gyro data down sample ratio to ODR. 000: 1/2; 001: 1/4; 010: 1/8; 011: 1/16; 100: 1/32; 101: 1/64; 110: 1/128; 111: 1/256

7.1.13 Register 0x3A - 0x3B: Master I^{2}C Configuration

Name: MI^{2}C_CONFIG_0
Address: 0x3A

Bit	Access	Default	Description
7	RW	0	1: Master I^{2}C reset; 0: Master I^{2}C normal operation
6	RW	0	Master I^{2}C read mode. 1: Auto; 0: Manual
5	RO	0	Master I^{2}C failure flag
4	RO	0	Master I^{2}C success flag
[3:2]			Reserved
1	RW	0	1: Master I^{2}C enabled, auto clear after master I^{2}C operation is done; 0: Master I^{2}C is idle
0	RW	0	1: Master I^{2}C read operation; 0: Master I^{2}C write operation

Name: MI^{2}C_CONFIG_1
Address: 0x3B

Bit	Access	Default	Description
[7:6]			Reserved
[5:4]	RW	00	Master I^{2}C read mode ODR. 00: 200Hz; 01: 100Hz; 10: 50Hz; 11: 25Hz
[3:0]	RW	0000	Master I^{2}C operation frequency selection. N is the decimal value of [3:0], 1MHz/(6+3×N) is the operation frequency.

7.1.14 Register 0x3C - 0x3D: Master I^{2}C Command

Name: MI^{2}C_COMM_0
Address: 0x3C

Bit	Access	Default	Description
[7:1]	RW	0000000	Slave I^{2}C address
0			Reserved

Name: MI^{2}C_COMM_1
Address: 0x3D

Bit	Access	Default	Description
[7:0]	RW	00000000	Command send to I^{2}C device

7.1.15 Register 0x3E: Master I^{2}C Write Data

Name: MI^{2}C_WRT_DATA
Address: 0x3E

Bit	Access	Default	Description
[7:0]	RW	00000000	Data write to I^{2}C device

7.1.16 Register 0x3F: Master I^{2}C Read Out Data

Name: MI^{2}C_RAD_DATA
Address: 0x3F

Bit	Access	Default	Description
[7:0]	RO	00000000	Data read out from I^{2}C device

7.1.17 Register 0x40 - 0x41: Interrupt Enable

Name: INTERRUPT_EN_0
Address: 0x40

Bit	Access	Default	Description
7	RW	0	Low-G Interrupt enable. 1: Enable; 0: Disable
6	RW	0	High-G Interrupt enable. 1: Enable; 0: Disable
5	RW	0	Inactivity Interrupt enable. 1: Enable; 0: Disable
4	RW	0	Activity Interrupt enable. 1: Enable; 0: Disable
3	RW	0	Double Tap Interrupt enable. 1: Enable; 0: Disable
2	RW	0	Tap Interrupt enable. 1: Enable; 0: Disable
1	RW	0	Flat Interrupt enable. 1: Enable; 0: Disable
0	RW	0	Orientation Interrupt enable. 1: Enable; 0: Disable

Name: INTERRUPT_EN_0
Address: 0x41

Bit	Access	Default	Description
[7:5]			Reserved
4	RW	0	FIFO Gyroscope Watermark Interrupt enable. 1: Enable; 0: Disable
3	RW	0	Gyroscope Data Ready Interrupt enable. 1: Enable; 0: Disable
2	RW	0	FIFO Accelerometer Watermark Interrupt enable. 1: Enable; 0: Disable
1	RW	0	Accelerometer Data Ready Interrupt enable. 1: Enable; 0: Disable
0	RW	0	Free-fall Interrupt enable. 1: Enable; 0: Disable

7.1.18 Register 0x44: Interrupt Configuration

Name: INTERRUPT_CONFIG
Address: 0x44

Bit	Access	Default	Description
7	RW	0	Interrupt output pin INT active level. 1: Low; 0: High
6	RW	0	1: Interrupt is not latched and will be auto clear after defined period of time; 0: Interrupt is latched and will be clear after read interrupt status register
5			Interrupt output pin INT1 active level. 1: Low; 0: High
4	RW	0	Interrupt flag clear mode. 1: Clear interrupt status by any register read operation; 0: Clear interrupt status by reading the interrupt status register
3			Reserved
2	RW	1	Interrupt output pin INT1 mode. 1: Normal output; 0: Open-drain output
1			Reserved
0	RW	1	Interrupt output pin INT mode. 1: Normal output; 0: Open-drain output

7.1.19 Register 0x45: Interrupt Count Limit

Name: INTERRUPT_CONT_LIM
Address: 0x45

Bit	Access	Default	Description
[7:0]	RW	00000000	If interrupt is not latched set by register 0x44[6], interrupt pin will be auto cleared when interrupt last time is longer than the time define in this register. This counter is based on 512Hz clock.

7.1.20 Register 0x46 - 0x4D: Orientation Interrupt Configuration

Name: ORIENT_INT_CONFIG_0
Address: 0x46

Bit	Access	Default	Description
7			Reserved
6	RW	0	Up-down Orientation Interrupt Enable. 1: Enable; 0: Disable
[5:0]	RW	000000	$tan^2\theta$ for Orientation Interrupt

Name: ORIENT_INT_CONFIG_1
Address: 0x47

Bit	Access	Default	Description
[7:4]			Reserved
[3:2]	RW	00	Orientation interrupt blocking mode. 00: No blocking; 01: θ blocking or acceleration in any axis >1.5g;10: θ blocking or acceleration slope in any axis > 0.2g or acceleration in any axis > 1.5g; 11: θ blocking or acceleration slope in any axis > 0.4g or acceleration in any axis > 1.5g and value of orient is not stable for at least 100ms.
[1:0]	RW	00	Orientation mode. 00/11: Symmetrical; 01: High-asymmetrical; 10: Low-asymmetrical

Name: ORIENT_INT_CONFIG_2
Address: 0x48

Bit	Access	Default	Description
[7:0]	RW	00000000	Low byte of the 1.5g value for orientation blocking

Name: ORIENT_INT_CONFIG_3
Address: 0x49

Bit	Access	Default	Description
[7:0]	RW	00000000	High byte of the 1.5g value for orientation blocking

Name: ORIENT_INT_CONFIG_4
Address: 0x4A

Bit	Access	Default	Description
[7:0]	RW	00000000	Low byte of the slope value for orientation blocking

Name: ORIENT_INT_CONFIG_5
Address: 0x4B

Bit	Access	Default	Description
[7:0]	RW	00000000	High byte of the slope value for orientation blocking

Name: ORIENT_INT_CONFIG_6
Address: 0x4C

Bit	Access	Default	Description
[7:0]	RW	00000000	Low byte of hysteresis value for orientation blocking

Name: ORIENT_INT_CONFIG_7
Address: 0x4D

Bit	Access	Default	Description
[7:0]	RW	00000000	High byte of hysteresis value for orientation blocking

7.1.21 Register 0x4E: Flat Interrupt Configuration

Name: FLAT_INT_CONFIG
Address: 0x4E

Bit	Access	Default	Description
[7:6]	RW	01	Flat time threshold. 01: 500; 10: 1000; 11: 2000. The unit is *ms*.
[5:0]	RW	000000	$tan^2\theta$ for Flat Interrupt

7.1.22 Register 0x4F - 0x50 & 0x55 - 0x58 & 0x7B - 0x7E: Activity & Inactivity Interrupt Configuration

Name: ACT_INACT_CONFIG_0
Address: 0x4F

Bit	Access	Default	Description
7	RW	0	Activity Interrupt Mode. 1: AC Mode; 0: DC Mode
6	RW	0	X-axis Activity Interrupt enable. 1: Enable; 0: Disable
5	RW	0	Y-axis Activity Interrupt enable. 1: Enable; 0: Disable
4	RW	0	Z-axis Activity Interrupt enable. 1: Enable; 0: Disable
3	RW	0	Inactivity Interrupt Mode. 1: AC Mode; 0: DC Mode
2	RW	0	X-axis Inactivity Interrupt enable. 1: Enable; 0: Disable
1	RW	0	Y-axis Inactivity Interrupt enable. 1: Enable; 0: Disable
0	RW	0	Z-axis Inactivity Interrupt enable. 1: Enable; 0: Disable

Name: TAP_ACT_INACT_CONFIG
Address: 0x50

Bit	Access	Default	Description
[7:4]			Reserved
3	RW	0	X-axis Tap Interrupt enable. 1: Enable; 0: Disable
2	RW	0	Y-axis Tap Interrupt enable. 1: Enable; 0: Disable
1	RW	0	Z-axis Tap Interrupt enable. 1: Enable; 0: Disable
0	RW	0	Link Activity/Inactivity status. 1: If the previous status is activity, only Inactivity Interrupt can be generated. If the previous status is inactivity, only Activity Interrupt can be generated; 0: Activity/Inactivity will trigger interrupt no matter what previous status is.

Name: ACT_INT_THR
Address: 0x55

Bit	Access	Default	Description
[7:0]	RW	00000000	Threshold for Activity Interrupt. Absolute value is used in DC mode, and the delta value of two consecutive samples is used in AC mode. The threshold is range dependent and the value defined by 1 LSB is 0.24mg, 0.48mg, 0.97mg and 1.95mg as the range is set to $\pm 2g$, $\pm 4g$, $\pm 8g$ and $\pm 16g$,respectively.

Name: ACT_INT_TIME
Address: 0x56

Bit	Access	Default	Description
[7:0]	RW	00000000	The number of consecutive samples that acceleration must be greater than the value defined by register 0x55 for Activity Interrupt to be declared.

Name: INACT_INT_THR_L
Address: 0x57

Bit	Access	Default	Description
[7:0]	RW	00000000	Low byte of Inactivity Interrupt threshold.

Name: INACT_INT_TIME
Address: 0x58

Bit	Access	Default	Description
[7:0]	RW	00000000	The amount of time that acceleration must be less than the value in the inactivity threshold register for Inactivity Interrupt to be declared. The unit is *s*.

Name: INACT_INT_THR_M
Address: 0x7B

Bit	Access	Default	Description
[7:0]	RW	00000000	Middle byte of Inactivity Interrupt threshold

Name: INACT_INT_THR_H
Address: 0x7C

Bit	Access	Default	Description
[7:0]	RW	00000000	High byte of Inactivity Interrupt threshold

Name: INACT_INT_1G_L
Address: 0x7D

Bit	Access	Default	Description
[7:0]	RW	00000000	Low byte of 1G value for Inactivity Interrupt

Name: INACT_INT_1G_H
Address: 0x7E

Bit	Access	Default	Description
[7:0]	RW	00000000	High byte of 1G value for Inactivity Interrupt

7.1.23 Register 0x50 - 0x54: Tap Interrupt Configuration

Name: TAP_ACT_INACT_CONFIG
Address: 0x50

Bit	Access	Default	Description
[7:4]			Reserved
3	RW	0	X-axis Tap Interrupt enable. 1: Enable; 0: Disable
2	RW	0	Y-axis Tap Interrupt enable. 1: Enable; 0: Disable
1	RW	0	Z-axis Tap Interrupt enable. 1: Enable; 0: Disable
0	RW	0	Link Activity/Inactivity status. 1: If the previous status is activity, only Inactivity Interrupt can be generated. If the previous status is inactivity, only Activity Interrupt can be generated; 0: Activity/Inactivity will trigger interrupt no matter what previous status is.

Name: TAP_INT_THR
Address: 0x51

Bit	Access	Default	Description
[7:0]	RW	00000000	Acceleration threshold for TAP Interrupt

Name: TAP_INT_DUR
Address: 0x52

Bit	Access	Default	Description
[7:0]	RW	00000000	Time threshold for TAP Interrupt. The unit is *ms*.

Name: TAP_INT_LAT
Address: 0x53

Bit	Access	Default	Description
[7:0]	RW	00000000	The wait time from the detection of a tap event to the start of the time window during which a possible second tap event can be detected. The unit is *ms*.

Name: DOUBLETAP_INT_WIN
Address: 0x54

Bit	Access	Default	Description
[7:0]	RW	00000000	The amount of time after the expiration of the latency time during which a second valid tap can be begin. The unit is *ms*.

7.1.24 Register 0x59 - 0x5D: High-G & Low-G Interrupt Configuration

Name: H&L-G_INT_CONFIG_0
Address: 0x59

Bit	Access	Default	Description
7	RW	0	High-G Interrupt of all axes enable. 1: Enable; 0: Disable
6	RW	0	High-G Interrupt of X-axis enable. 1: Enable; 0: Disable
5	RW	0	High-G Interrupt of Y-axis enable. 1: Enable; 0: Disable
4	RW	0	High-G Interrupt of Z-axis enable. 1: Enable; 0: Disable
[3:1]			Reserved
0	RW	0	Low-G Interrupt of all axes enable. 1: Enable; 0: Disable

Name: HIGH-G_INT_THR
Address: 0x5A

Bit	Access	Default	Description
[7:0]	RW	00000000	The acceleration threshold of High-G Interrupt. 1 LSB equals to 0.5mg, 1mg, 2mg and 4mg as the range is ±2g, ±4g, ±8g and ±16g respectively.

Name: HIGH-G_INT_TIME
Address: 0x5B

Bit	Access	Default	Description
[7:0]	RW	00000000	Minimum time that the acceleration value of all axes must be greater than the value set by 0x5A to generate a High-G Interrupt. The counter is based on 512 Hz clock.

Name: LOW-G_INT_THR
Address: 0x5C

Bit	Access	Default	Description
[7:0]	RW	00000000	The acceleration threshold of Low-G Interrupt. 1 LSB equals to 0.5mg, 1mg, 2mg and 4mg as the range is ±2g, ±4g, ±8g and ±16g respectively.

Name: LOW-G_INT_TIME
Address: 0x5D

Bit	Access	Default	Description
[7:0]	RW	00000000	Minimum time that the acceleration value of all axes must be smaller than the value set by 0x5C to generate a Low-G Interrupt. The counter is based on 512 Hz clock.

7.1.25 Register 0x5E - 0x5F: Free Fall Interrupt Configuration

Name: FREE-FALL_INT_THR
Address: 0x5E

Bit	Access	Default	Description
[7:0]	RW	00000000	The acceleration threshold of Free-fall Interrupt. 1 LSB equals to 0.5mg, 1mg, 2mg and 4mg as the range is ±2g, ±4g, ±8g and ±16g respectively.

Name: FREE-FALL_INT_TIME
Address: 0x5F

Bit	Access	Default	Description
[7:0]	RW	00000000	Minimum time that the acceleration value of all axes must be smaller than the value set by 0x5E to generate a Free-Fall Interrupt. The counter is based on 512 Hz clock.

7.1.26 Register 0x79 - 0x7A: Interrupt Pin Mapping

Name: INT_PINMP_0
Address: 0x79

Bit	Access	Default	Description
7	RW	0	High-G Interrupt pin mapping. 1: INT1; 0: INT
6	RW	0	Inactivity Interrupt pin mapping. 1: INT1; 0: INT
5	RW	0	Activity Interrupt pin mapping. 1: INT1; 0: INT
4	RW	0	Double and Single Tap pin mapping 1: INT1; 0: INT
3	RW	0	Double Tap Interrupt pin mapping. 1: INT1; 0: INT
2	RW	0	Single Tap Interrupt pin mapping. 1: INT1; 0: INT
1	RW	0	Flat Interrupt pin mapping. 1: INT1; 0: INT
0	RW	0	Orientation Interrupt pin mapping. 1: INT1; 0: INT

Name: INT_PINMP_1
Address: 0x7A

Bit	Access	Default	Description
[7:6]			Reserved
5	RW	0	Gyroscope FIFO Watermark Interrupt pin mapping. 1: INT1; 0: INT
4	RW	0	Gyroscope Data Ready Interrupt pin mapping. 1: INT1; 0: INT
3	RW	0	Accelerometer FIFO Watermark Interrupt pin mapping. 1: INT1; 0: INT
2	RW	0	Accelerometer Data Ready Interrupt pin mapping. 1: INT1; 0: INT
1	RW	0	Free-fall Interrupt pin mapping. 1: INT1; 0: INT
0	RW	0	Low-G Interrupt pin mapping. 1: INT1; 0: INT

7.1.27 Register 0x7F: SPI Register Access

Name: SPI_CONFIG
Address: 0x7F

Bit	Access	Default	Description
[7:1]			Reserved
[0]	RW	0	0: Access SPI Page1 registers; 1: Access SPI Page2 registers

7.1.28 Register 0xFD: Auxiliary I^2C Configuration

Name: AUX_I^2C_CONFIG
Address: 0xFD

Bit	Access	Default	Description
[7:1]			Reserved
[0]	RW	0	Auxiliary I^2C working mode. 0: Normal Mode; 1: I^2C bypass to MI^2C

8 Application Hints

8.1 Orientation of Axes

The diagram below shows the orientation of the axes of sensitivity and the polarities of rotation. Note the pin1 marker in the figure.

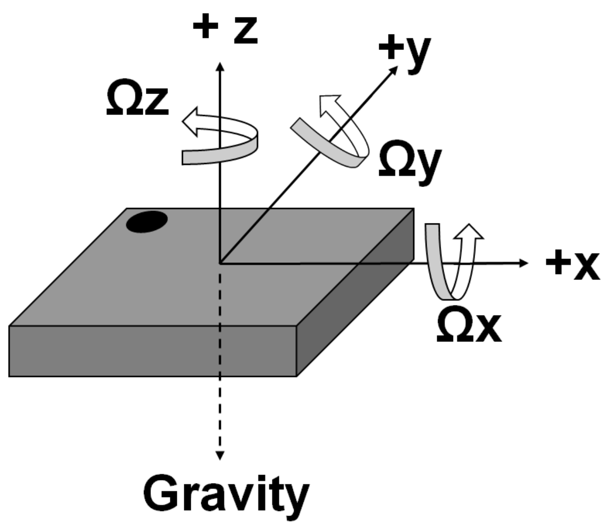

Figure 15: Orientation of axes sensitivity and polarity of rotation

8.2 Typical Application Circuits

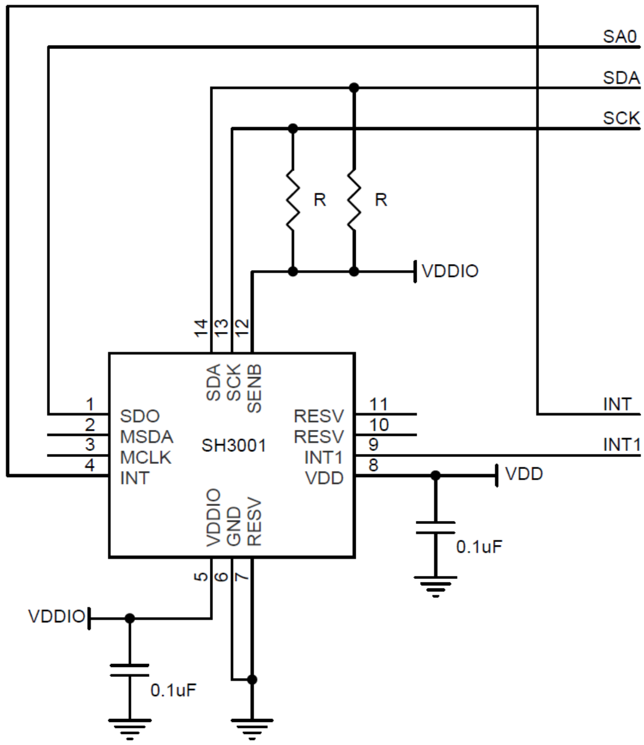

Figure 16: Reference application circuitry using only primary I^{2}C interface

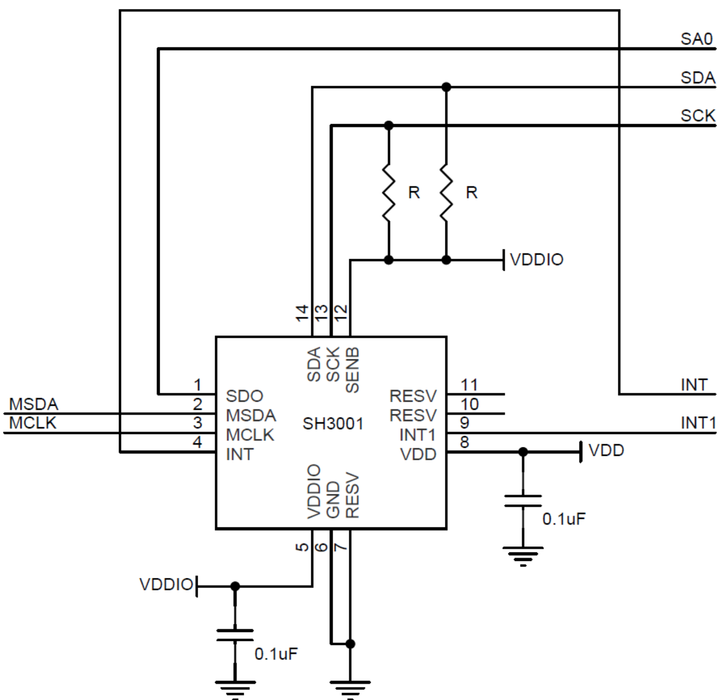

Figure 17: Reference application circuitry using primary and secondary I^{2}C interface

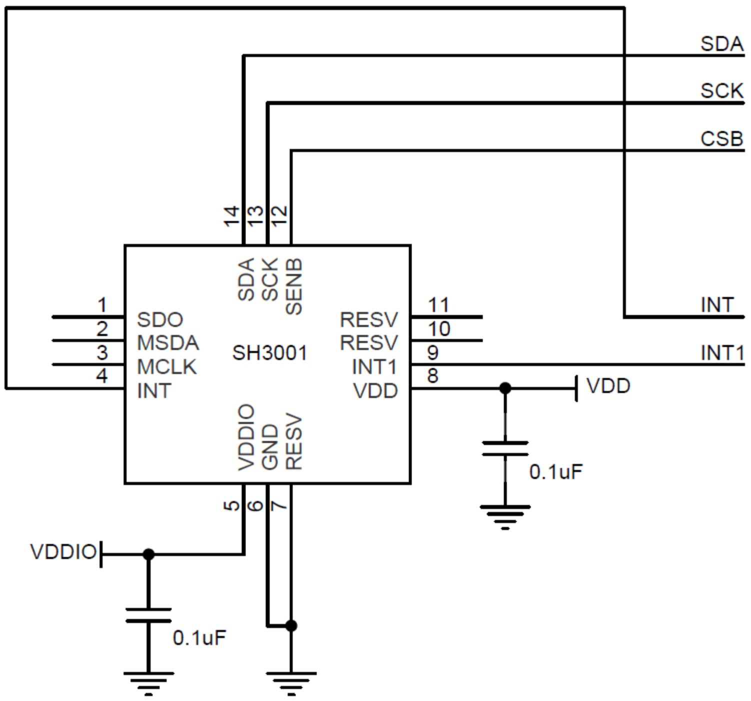

Figure 18: Reference application circuitry using SPI 3-wire interface

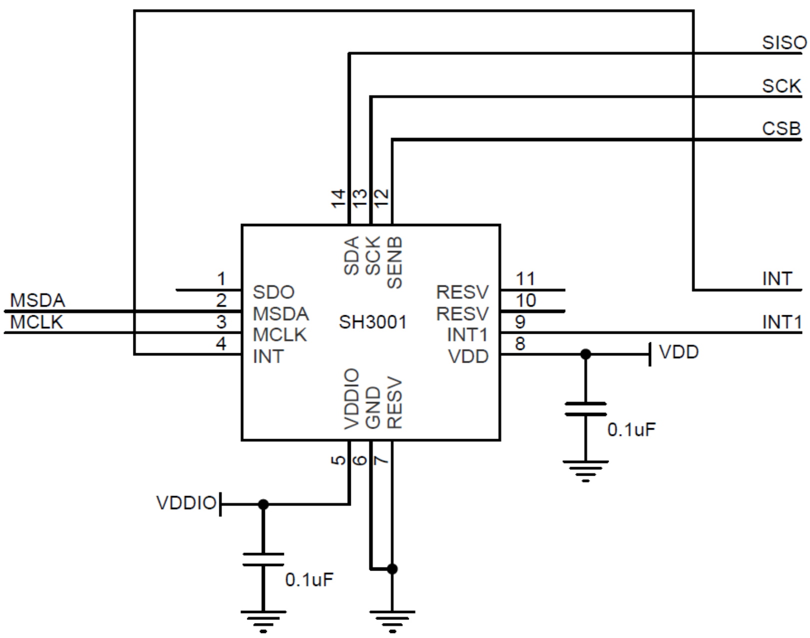

Figure 19: Reference application circuitry using SPI 3-wire and secondary I^2C interface

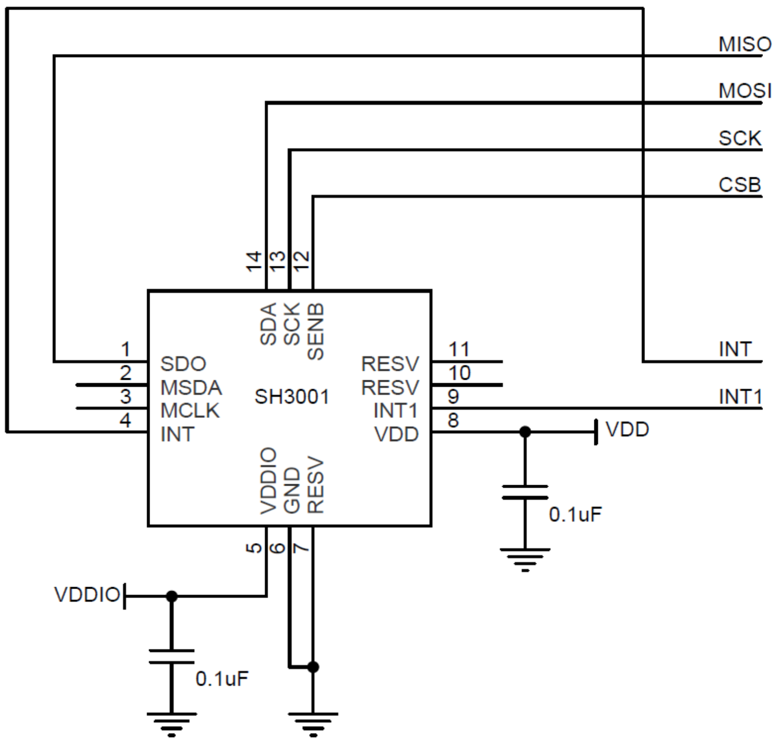

Figure 20: Reference application circuitry using SPI 4-wire interface

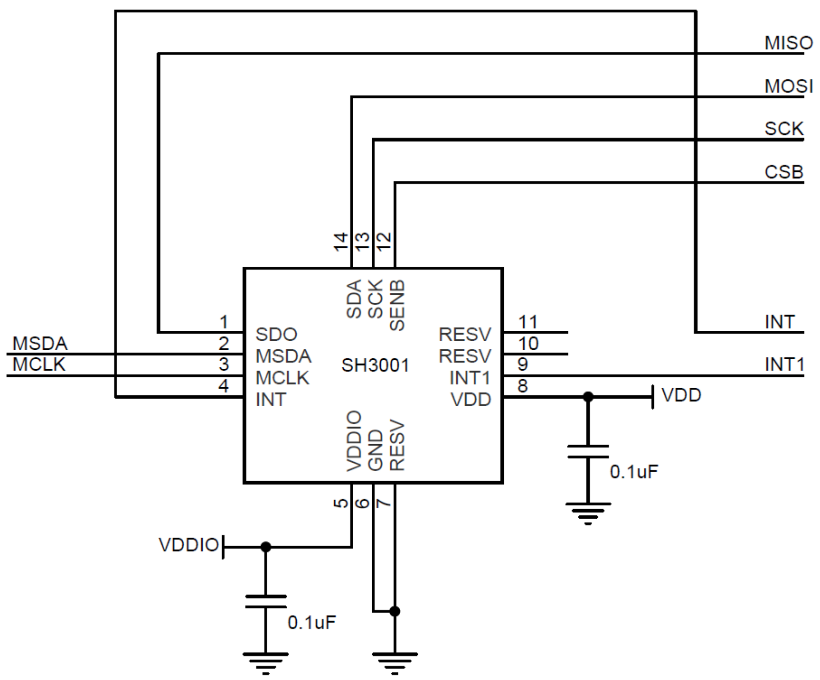

Figure 21: Reference application circuitry using SPI 4-wire and secondary I^2C interface

8.3 Package Information

8.3.1 Device Outline Dimensions

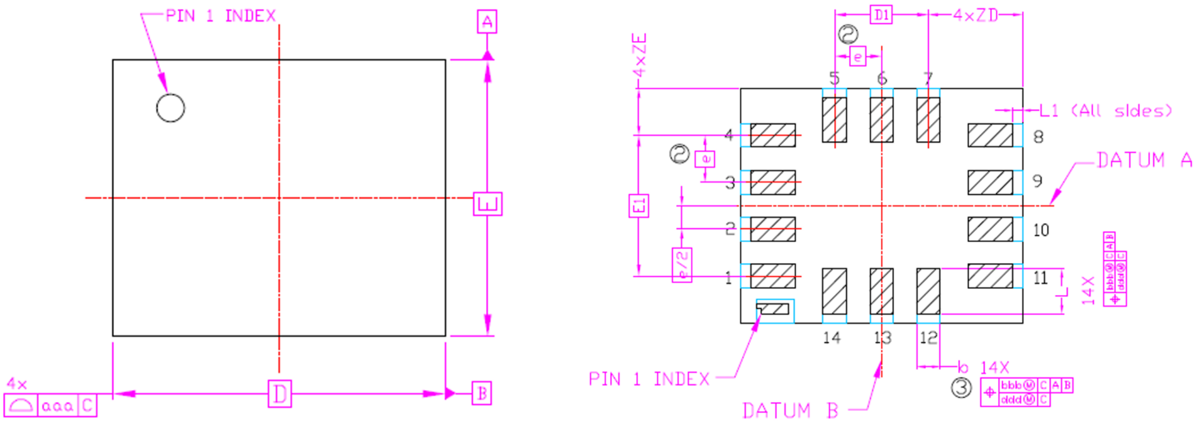

Figure 22: Top & bottom view of the device

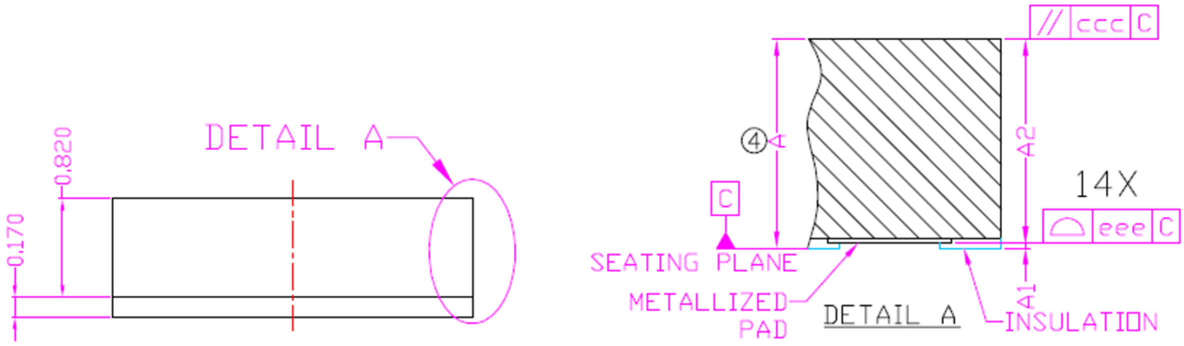

Figure 23: Side view of the device

Table 15: Dimension references (unit: *mm*)

Ref	Min	Typ	Max	Ref	Min	Typ	Max
A	0.93	0.99	1.05	D1		1.00 BSC	
A1			0.03	E1		1.50 BSC	
A2			1.02	ZD		1.00 BSC	
b	0.2	0.25	0.3	ZE		0.50 BSC	
L	0.425	0.475	0.525	e		0.50 BSC	
D	2.90	3.00	3.10	L1	0.00	0.10	0.20
E	2.40	2.50	2.60				

Note: The dimensional tolerance of `aaa`, `bbb` and `ccc` is 0.10 *mm* and that of `ddd` and `eee` is 0.08 *mm*.

8.3.2 Package Laser Mark

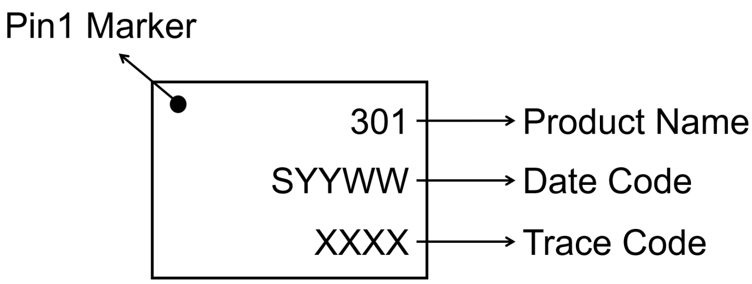

Figure 24: Package laser mark

8.3.3 Packaging Direction

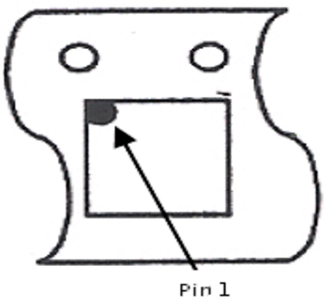

Figure 25: Packaging direction

8.3.4 Packaging Label

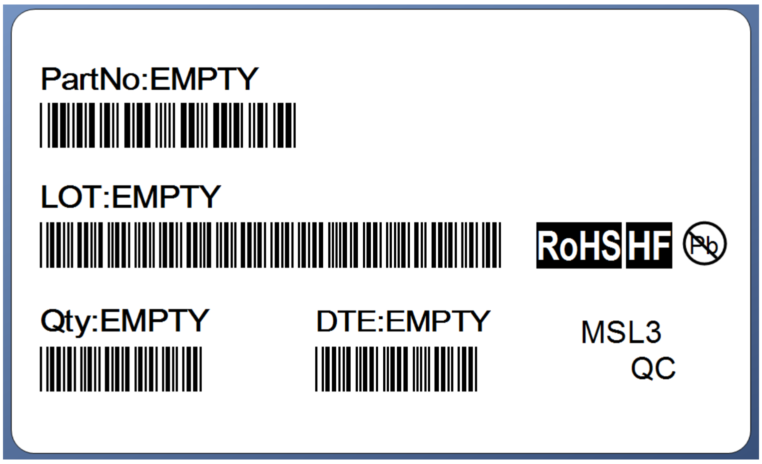

Figure 26: Packaging label example

8.3.5 Packaging of Product

Figure 27: Packaging of the product

8.4 Soldering Guidelines

The device fulfils the lead-free soldering requirements of the IPC/JEDEC J-STD-020 Pb-free standard. Reflow soldering with a peak temperature T_p of 260^oC.

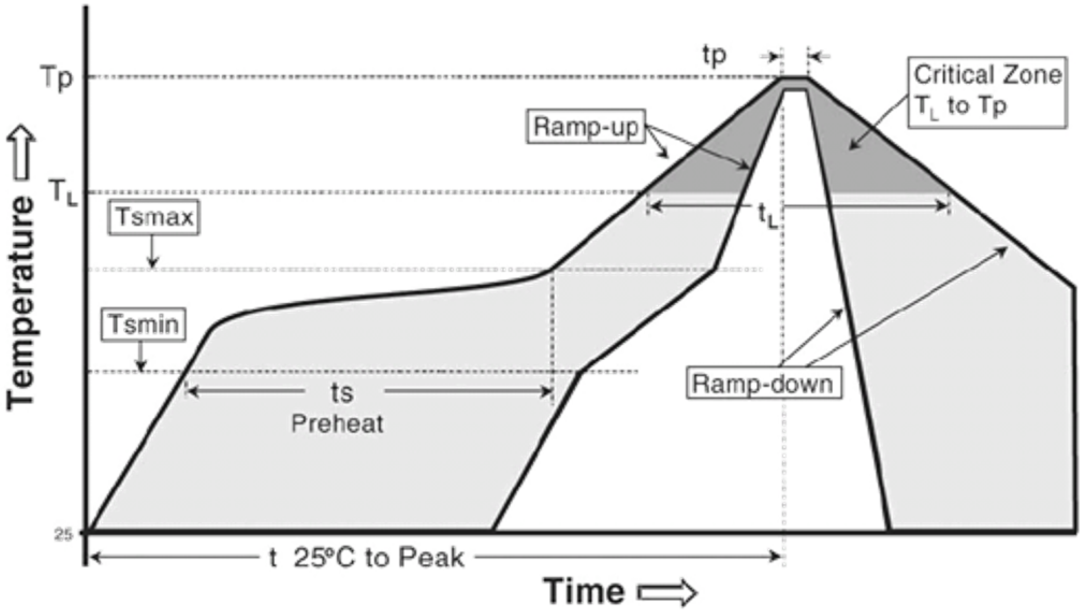

Figure 28: Recommended soldering reflow condition

Table 16: Recommended soldering reflow condition

Profile Feature	**Pb-free Assembly**
Average ramp-up rate (Ts_{max} to T_p)	3 $^oC/s$ max
Preheat - Temperature Min (Ts_{min}) - Temperature Max (Ts_{max}) - Time (Ts_{min} to Ts_{max}) (ts)	 150 ^oC 200 ^oC 60 - 80 s
Time maintained above: - Temperature (T_L) - Time (t_L)	 217 ^oC 60 - 150 s
Peak Temperature (T_p)	260 ^oC
Time within 5 ^oC of actual Peak Temperature	20 - 40 s
Ramp-down rate	6 $^oC/s$ max
Time 25 ^oC to Peak Temperature	8 min max

8.5 Storage Condition

The storage condition follows JEDEC J-STD-020, MSL3.

9 Reliability

9.1 Reliability Standard

SH3001 reliability test plan follows JEDEC 47I standards, 'Stress-Test-Driven Qualification of Integrated Circuits'.

10 Environment Compliant

SH3001 is compliant with RoHS 2.0 standards and meet HF requirements.

11 Disclaimer

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12 Revision History

Date	Revision	Changes
2019-12-12	1.0	Preliminary version
2020-09-16	1.2	Add basic description
2021-03-05	1.3	Update some register descriptions
2021-05-10	1.5	Update temperature sensor related register descriptions
2021-09-01	1.6	Update packaging information