A 0.7–2.7-GHz Blocker-Tolerant Compact-Size Single-Antenna Receiver for Wideband Mobile Applications

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***Abstract*—Passive-mixer-first receivers have recently demonstrated flexible, low-noise, and high-linearity performance. Likewise, capacitive coupling element antennas have been demonstrated to be a viable choice for mobile handset integration. This paper combines these two advances into a single-antenna wideband receiver that achieves a 0.7–2.7-GHz reception band. The compact-size wideband tunable antenna achieves an efficiency of 45%–69% and occupies a volume of 2500 mm^3. The front-end integrated circuit achieves an input compression point of +5 dBm with a noise figure of 4 dB while occupying only 0.3 mm^2 of active die area. Additionally, an interface impedance study is performed to find the optimal impedances around the passive mixer and to demonstrate the different design tradeoffs of a passive-mixer-first receiver. A local oscillator duty-cycle adjustment circuit and its effect on the receiver performance is also presented.**

***Index Terms*—Blocker filtering, capacitive coupling element (CCE) antenna, duty cycle, impedance tuning, passive mixer, receiver, software-defined radio (SDR), wideband receiver.**

I. Introduction

MODERN portable devices require high-capacity access to the Internet to deliver full functionality to the user. A recent report predicts that mobile data traffic will grow fifteenfold from 2012 to 2017 [1]. This places great strain on the telecommunications industry to provide solutions that will meet this demand using the existing spectrum allocation.

Current solutions for transceivers, which are capable of operating on multiple and widely spaced bands with divergent parameters, involve the utilization of multiple narrowband radios [2]. Typically, these are combined with a plethora of discrete filters, switches, duplexers, power amplifiers, and multiple antennas to fulfill the specified requirements of different standards. This becomes a massive engineering effort while taking up a lot of printed-circuit board (PCB) real estate, and the challenge will only increase as the inter-band carrier aggregation scheme of the long-term evolution advanced (LTE-A) [3] standard is implemented in mobile handsets.

A software-defined radio (SDR) has been long proposed as a solution to enable flexible and efficient use of the radio spectrum by dynamically adjusting its operating parameters [4]. However, the tuning of the radio interfaces has proved to be difficult and is one of the key obstacles to a truly flexible SDR implementation [5].

Mixer-first receivers have recently demonstrated the potential to become a true SDR solution with good flexibility, linearity, and noise performance [6]–[8]. While there are still unresolved issues, such as the harmonic mixing, the topology has gained much momentum. Furthermore, similar to digital transmitters [9] and synthesizers [10], mixer-first receivers are fundamentally performing a sampling operation at the input, and thus, will benefit from the continuously decreasing line width by making their switches faster and more efficient.

Simultaneously, inherently nonresonant antennas with capability for very wide and continuous frequency tuning ranges have been introduced [11], [12]. Capacitive coupling element (CCE) antennas are a viable candidate for mobile SDR with operation across a broad frequency range. Unlike most resonant antennas, the geometrical structure of CCE antennas does not exhibit inherent frequency selectivity, which makes it easily tunable.

In this paper, we utilize these two advances in a single-antenna SDR receiver capable of operating on the LTE bands from 0.7 to 2.7 GHz. To our knowledge, this is the first demonstration of a mixer-first receiver with a CCE antenna. Also, this paper will show that, in terms of receiver performance, a non-50-Ω input impedance is indeed highly beneficial for the overall performance.

Section II will first present system considerations before the antenna design and measurements are introduced in Section III. In Section IV, the interface impedance tradeoff study is first discussed, followed by the integrated circuit (IC) design of the key blocks in the receiver in Section V. The last part of Section V presents the experimental results of the standalone receiver IC. Over-the-air system measurements are shown in Section VI and key findings are discussed before conclusions in Section VII.

II. System Considerations

Interfacing a wideband receiver with an antenna that is capable of a large tuning range poses different kinds of requirements on matching than in the conventional case, where the

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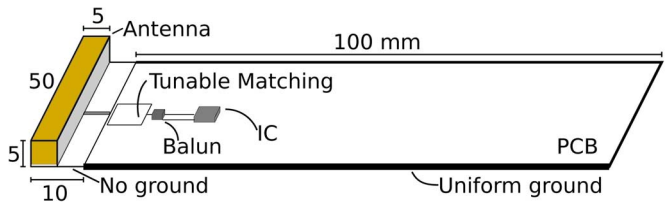

Fig. 1. System diagram showing physical dimensions of the antenna and the board together with the component placements. The thicker line on the side reflects that the bottom ground plane is used as a radiating element together with the CCE. Dimensions in millimeters.

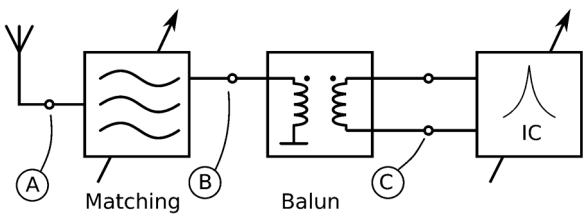

Fig. 2. Block diagram of the system input configuration.

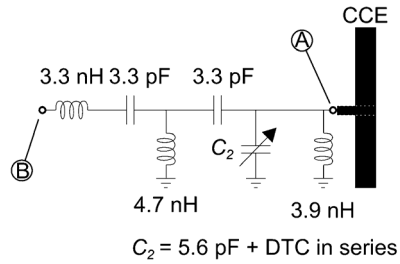

Fig. 3. Tuning circuit of a tunable CCE antenna [14].

input is matched at frequency points defined by the supported systems. The antenna and receiver reactances vary heavily over frequency, and handling this behavior is one key to wideband matching.

The physical description of our system and the block diagram of the key interfaces are shown in Figs. 1 and 2, respectively. Fig. 1 depicts the relative locations of the interface key components, namely, the antenna element, the tunable matching, the balun, and the integrated receiver circuit (IC). All of the components are placed on a printed circuit board (PCB) that is $110 \times 50 \times 5$ mm in size, which makes it suitable for mobile handset integration.

There are certain requirements and limitations in the IC interface (node C, Fig. 2). First, the performance of a mixer-first receiver is optimized when it is presented with a sufficiently large antenna impedance, as will be shown in Section IV-B. On the other hand, the single-ended CCE antenna impedance is inherently low, which interfaces poorly with the desired high IC input impedance. Second, local oscillator (LO) noise and receiver linearity issues are alleviated by using balanced (differential) input signaling. However, compact size balanced antennas do not reach low-band (<1 GHz) operation in mobile handsets [13]. We have addressed these problems by using a balun, depicted in Fig. 2, which accomplishes unbalanced–balanced and impedance transformations simultaneously (from node B to C in Fig. 2). Due to the fundamental limitations of small antennas, the CCE antenna cannot be instantaneously matched across all frequencies without separate matching circuitry. Hence, we still need reconfigurable matching, as is shown in Fig. 2.

III. Widely Tunable Compact Handset Antenna

A. Background

The handset form factors and the volume dedicated for antennas limit the design of antennas in mobile terminals. The conductive chassis of the handset can be exploited in improving the radiation properties of the antenna at the lower frequencies of operation [15]–[17]. However, even then it is difficult to implement a compact antenna that performs well across a wide and continuous frequency range instantaneously.

In an SDR that operates at the frequencies of cellular communications, the antenna does not need to satisfy the broadband operation instantaneously. Instead, a tuning circuit can be used to change the operating frequency of the antenna dynamically [18]. The main requirement for a broadband tunable antenna is that the inherent impedance of the antenna must allow tuning of the impedance to the RF front-end interface impedance at all desired frequencies. One type of such antennas is the CCE antenna [11]. It has been shown that the inherently nonselective CCE can be matched at any frequency used for mobile communications [12], [19].

B. Implementation

The goal for the antenna design in this paper was to implement a compact mobile handset antenna with a wide continuous tuning range from 0.7 up to 2.7 GHz. Although the current cellular systems do not use all the frequencies within the target range, we wanted to implement the continuous antenna tuning range to show that the wide frequency range without gaps could be realized in the SDR paradigm. Furthermore, for simultaneous multi-band reception like in LTE-A carrier aggregation, a single multi-feed CCE antenna could be utilized together with an additional receive path, as is presented in [14].

The selected antenna solution relies on the CCE concept, specifically on the versatile CCE geometry presented in [20]. The tuning method was selected to be as simple as possible: a single tunable component with supporting fixed matching components, as is shown in Fig. 3 [14]. A tunable shunt capacitance is the easiest way to implement tuning across a wide continuous band without significant power losses in the tuning circuit. In this case, a digitally tunable capacitor (DTC) based on a CMOS switch bank was selected. The 5-bit DTC (PE64904 by Peregrine Semiconductor) has 32 binary states corresponding to capacitances from 1.12 to 5.18 pF (DTC codes 0–31). The impedance matching topology, shown in Fig. 3, consists of six lumped reactances including the DTC, which forms a parallel resonator with the inductor at node A. This configuration maximizes the tuning range for the CCE with the given circuit complexity. Due to the versatility of the CCE concept, the solution can be utilized for both the final IC interface and the 50-Ω interface.

To test the operability of the antenna, it was first matched to the conventional 50 Ω with the component values shown in Fig. 3 [14]. The impedance and the total efficiency were then

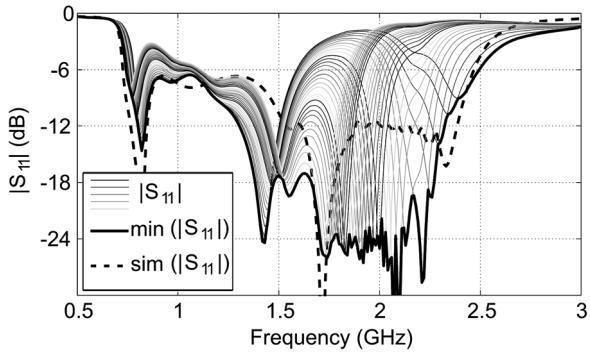

Fig. 4. Impedance matching result of the tunable antenna with respect to 50 Ω. Dashed line represents the minimum contour line of simulated results.

TABLE I
ANTENNA PERFORMANCE COMPARISON

	This work[1]	[33]	[34][1]	[35][1]
Freq. (GHz)	**0.75-2.5**	0.7–0.96 1.71–2.69	0.82–0.96 1.5–2.5	0.7–0.96 1.71–2.69
Effic. (%)	**45–69**	63–91	47–73	35–71
Ant.vol.(mm^3)	**2500**	4400	1500	6235
Area[2](mm^2)	**110×50**	115×55	105×60	102×50

[1] Tunable antenna [2] Including ground plane and ground clearance

measured and compared to similar recently published antennas to show the "raw" antenna performance in an easily comparable format. Fig. 4 shows the measured impedance matching of the tunable antenna in the 32 DTC states, relative to 50 Ω. The achieved impedance matched band, with the traditional return-loss criterion $L_{\rm retn} \geq 6$ dB, is 0.75–2.5 GHz. The reached total efficiency across the 0.75–2.5-GHz range is 45%–69% (from -1.6 to -3.5 dB). The DTC settling time is 15 μs, which is sufficiently small for cellular systems given that the DTC state only needs to be switched when the operation band is changed, as is seen in Fig. 4.

A comparison featuring the key performance characteristics of the proposed tunable antenna and other recently published mobile terminal antennas is presented in Table I. Papers presenting much wider continuous tuning ranges for mobile handset antennas exist, e.g., 442–2896 MHz for a similar size antenna in [21], but the tuning circuits do not contain real switches. Our results indicate that the performance of the presented antenna is competitive, given the compact size and the wide continuous tuning range.

IV. MIXER-FIRST RECEIVER DESIGN

A. Background

The mixer-first receiver topology is one of the most promising candidates to fulfill the SDR paradigm. The topology stems from the N-path filtering concept that was first conceived in the 1960s [22]. Recently, the passive mixer has been utilized to create an RF implementation of the N-path filter. With one mixer, the circuit can form a down-converting N-path filter [6]–[8], [23]–[25], as is shown in Fig. 5(a). In the receiver use, the baseband impedance $Z_{\rm BB}$ is typically implemented with a trans-impedance amplifier, as is depicted in Fig. 5(a). The

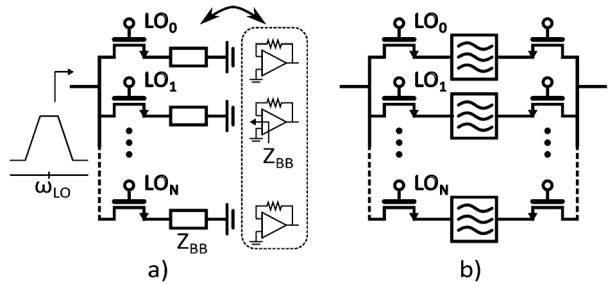

Fig. 5. (a) N-path filter with down-conversion and amplifiers. The impedance $Z_{\rm BB}$ is synthesized with the amplifier and feedback. (b) N-path filter (bandpass or notch) utilizing two mixers and baseband filtering in (b).

structure can also be used as a high-Q RF load with center frequency that can be tuned with the LO frequency [26], [27].

With two mixers the signal is first down-converted then filtered and then up-converted to the original RF frequency, as is shown in Fig. 5(b). The resulting bandpass filter or notch filter can act in a feedforward loop [28], a feedback loop [29], or as a standalone filter [30], [31] to attenuate unwanted signals.

The most recent advances with passive-mixer-first receivers include eight-phase mixing [6] with harmonic recombination that improves the harmonic rejection of the third and fifth harmonics and noise performance. Another recent paper introduces a noise canceling topology [32] to further improve the noise performance of the mixer-first receiver [7].

B. Mixer-First Receiver Design Tradeoffs

The N-path filter and the more recent applications using the passive mixer have been analyzed extensively in [26] and [36]–[40]. We will extend on these and show through simulations how the selection of different impedances on both sides of the passive mixer and the switch resistance itself affect the overall performance. We will approach this by first taking an intuitive approach to the problem, and then by showing that the simulation results confirm our initial findings.

The simulation model used in the tradeoff study consists of a balanced input, a quadrature transistor-level passive mixer, and an ideal operational amplifier model, as is presented in Fig. 6. The input impedance of the amplifier, due to the Miller effect, is $R_L = R_{\rm fb}/(1+A)$. This impedance is in parallel with the shunt capacitor $C_{\rm bb}$ and together they form the baseband low-pass load impedance, as is depicted in Fig. 7(a). Due to the transparency of the passive-mixer, the antenna sees this impedance up-converted around the LO frequency. This helps to keep the signal swing of the out-of-band blockers minimal, thus reducing distortion in the mixer.

For the analysis, the mixer-first receiver can be converted to a very simple passive circuit, as is shown in Fig. 7(a). The available power $P_{\rm av}$ at the antenna is the maximum power that the antenna can capture at any given location. The goal is to maximize the power $P_{\rm in}$ that is actually inserted into the receiver, and further, to maximize the power P_L delivered to the load. To maximize the $P_{\rm in}$, the antenna source resistance should ideally be matched so that $R_S = R_{\rm SW} + R_L$. In order to minimize the mixer impact on the noise figure (NF), the loss associated to the mixer needs to be minimized. Intuitively, this means that the

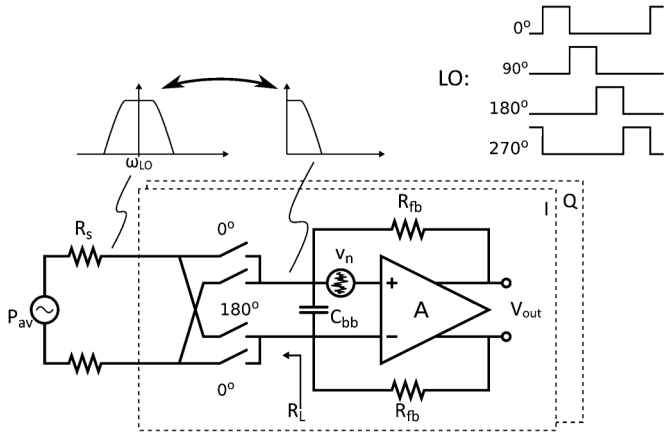

Fig. 6. Simulation model for the tradeoff study.

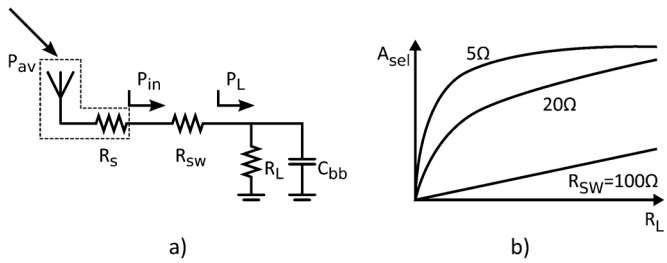

Fig. 7. (a) Intuitive model for the receiver input and (b) relative input power selectivity against load impedance R_L.

switch resistance $R_{\rm SW}$ needs to be minimized as well. In practical cases, the switch resistance has a lower limit and a maximum switch size that is set by the capacitive burden of the LO drive and the RF operating frequency. Since the mixer loss is actually dependent on the relative sizes of R_S, $R_{\rm SW}$, and R_L, we can further improve the power delivered to the load and the NF by maximizing the load and source impedances around the mixer. However, the impedance level is limited by the parasitics and the achievable antenna impedance on the RF side.

To study the selectivity of the receiver input, we can study how the effective load impedance, formed by R_L and $C_{\rm bb}$, behaves around dc. This is possible because, to a certain extent, the behavior is the same around the dc and LO frequencies. The -3-dB bandwidth $\rm BW_{3\ dB}$ of the low-pass *RC* response gives the connection between R_L and $C_{\rm bb}$

$$C_{\rm bb} = \frac{1}{R_L {\rm BW}_{3\ {\rm dB}}}. \tag{1}$$

We can then express the relative input selectivity at frequency offset $f_{\rm sel} = k{\cdot}{\rm BW}_{3\ {\rm dB}}$ with

$$A_{\rm sel} = \frac{P_{\rm DC}}{P_{f_{\rm sel}}} = \frac{\left|(R_{\rm SW}+R_L)\left(R_S+R_{\rm SW}+\frac{R_L}{1+j*k}\right)^2\right|}{\left|\left(R_{\rm SW}+\frac{R_L}{1+j*k}\right)(R_S+R_{\rm SW}+R_L)^2\right|}. \tag{2}$$

Looking closer at (2), we can see that if the selectivity is examined at infinity $(k=\infty)$, then two of the terms go to zero. The remaining equation shows that the power selectivity at the input is maximized by minimizing the switch resistance $R_{\rm SW}$, and if the matching condition $R_S = R_{\rm SW} + R_L$ is enforced,

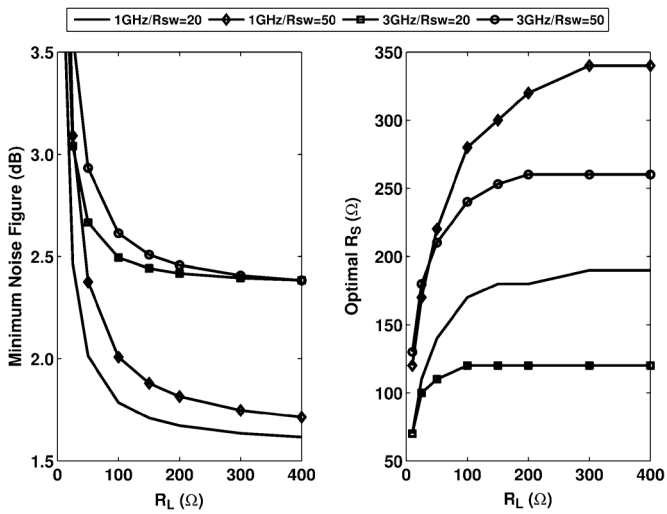

Fig. 8. Minimum NF and the corresponding optimum source resistance R_S versus baseband input resistance R_L. Four different switch resistance $R_{\rm SW}$ and LO frequency cases are shown in both figures.

by making the load resistance R_L large. An example where the selectivity is examined closer to the dc $(k = 20)$ is depicted in Fig. 7(b), where the behavior explained earlier is clearly visible. The switch resistance has a more profound effect on the selectivity than the load resistance.

To further investigate the influence of the interface impedances around the passive mixer, we have performed simulations with transistor-level RF large-signal models based on 65-nm CMOS technology. Values for the simulation are chosen such that they reflect the actual implementation. The simulation setup, which is depicted in Fig. 6, includes an input noise source for the baseband amplifier that has a value of 500 pV/$\sqrt{\rm Hz}$. The amplifier has a gain (A) of 100, which determines the used $R_{\rm fb}$ value through the Miller effect. The common-mode (CM) voltage of the switches is set to half of the supply voltage and the capacitor value $C_{\rm bb}$ is scaled such that the -3-dB bandwidth is maintained at 10 MHz in all simulation cases. To capture the variation in RF performance over a wide range, LO center frequencies of 1 and 3 GHz were used in all simulations.

Fig. 8 shows how the minimum NF and the optimal source resistance behave against different design factors. The minimum NF simulation clearly confirms the intuitive findings based on the model in Fig. 7(a): it is highly beneficial to select a load resistance R_L that is sufficiently high. This partially results from the fact that less noise is being injected into the baseband amplifier input by the $R_{\rm fb}$ and partially from smaller losses inside the mixer. Furthermore, the switch resistance (simulation with 20 and 50 Ω) has only a small effect on the noise, as is depicted by the results. The RF frequency has a clear and expected effect on the noise, i.e., the capacitances of the switch degrade the high-frequency noise performance. In Fig. 8, the optimal source resistance, corresponding to each minimum NF value, suggests that the source resistance follows the load resistance value like in the intuitive case. However, there is significant variation in the optimal R_S value across the LO frequency and the switch size. The smaller switch sizes (higher $R_{\rm SW}$) result in less parasitic capacitance, and thus, higher source values (250 and 340 Ω)

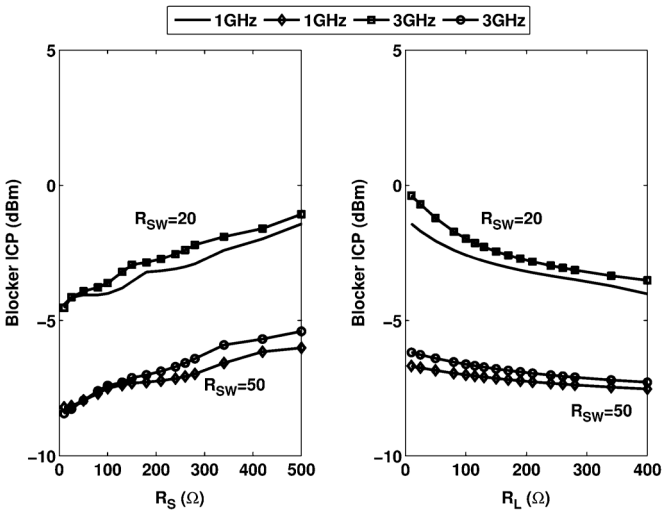

Fig. 9. Blocker ICP for varying R_S ($R_L = 200\ \Omega$) and R_L ($R_S = 200\ \Omega$) values at four different switch resistance and LO frequency combinations. The test blocker is located at a 50 MHz offset from the LO.

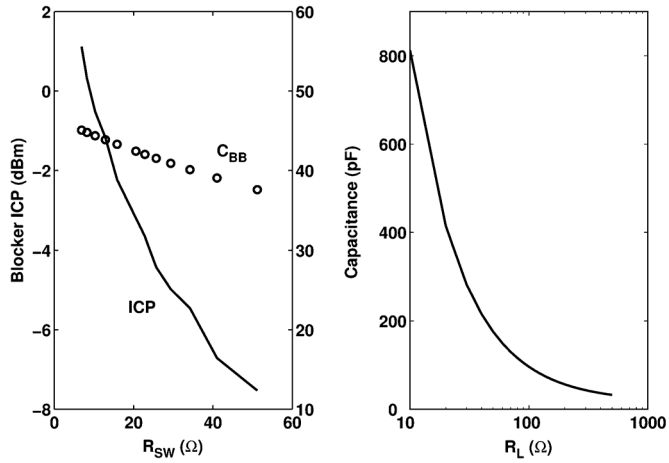

Fig. 10. Blocker input compression and corresponding baseband filtering capacitor value for varying switch resistance. Test blocker located at 50-MHz offset from LO. Additionally, to give perspective, baseband capacitor variation is shown against the baseband input resistance. The −3-dB bandwidth at the baseband input is fixed to 10 MHz in all cases.

are obtained. For the larger switch sizes, the optimal value for the source resistance is 120 and 190 Ω at the 1- and 3-GHz LO frequencies, respectively. In practical cases, package parasitics further load the mixer input and, therefore, a lower optimal source resistance value would be expected. Moreover, the choice of the R_S is always a compromise between the optimal resistance values over the operating frequency range.

The mixer linearity was studied through blocker ICP simulations. The results, performed for $R_L = 200\ \Omega$ and $R_S = 200\ \Omega$, are presented in Fig. 9. The simulation with fixed $R_L = 200\ \Omega$ shows that the linearity of the receiver is optimized by using large switches ($R_{\rm SW} = 20\ \Omega$). Choosing a higher source impedance also improves the linearity since the blocker power is rejected more effectively at the input. The simulation with fixed $R_S = 200\ \Omega$ shows again that large switches are beneficial. However, the linearity is degraded as the load impedance is increased. The increase in R_L results in a smaller capacitor to be seen by the source, which is due to the scaling of the filtering capacitor $C_{\rm bb}$ to maintain a constant bandwidth. The blocker power values depicted in the simulation results are the values that are actually inserted into the receiver [$P_{\rm in}$ in Fig. 7(a)], i.e., part of the power is also rejected by the mismatch of high source and low load impedance at the blocker frequency.

Finally, to demonstrate how the linearity and filtering capacitor are related to switch size, a simulation depicted in Fig. 10 was conducted. The result illustrates that the linearity is greatly affected by the switch resistance while the change in the filtering capacitor $C_{\rm bb}$ is modest. For comparison, the same dependency of the capacitor value is plotted against the baseband input impedance value on the right side of Fig. 10. Clearly, low values of R_L result in an implementation where die size is dictated by the capacitor.

To summarize this tradeoff study, the following conclusions can be drawn.

- The switch resistance $R_{\rm SW}$ should be as small as possible, given the limitations of LO power consumption and operating frequency range.
- A high antenna impedance R_S level is preferable for the best noise and linearity performance. However, this is often limited by the practical issues like input parasitics and antenna implementation.
- A high load impedance R_L results in lower noise and smaller layout size with a small penalty in linearity performance.

V. Mixer-First Receiver Implementation

A. Receive Path

Fig. 11 shows the complete receiver architecture including the transformer, the quadrature passive mixers, the low-noise transconductance stages (LN-gm), the output operational amplifiers (Opamp), and the LO path with duty-cycle control. The input transformer is a commercial 1:4 balun, which limits the receiver operating frequency to 0.7–2.7 GHz. In addition to the single-ended-to-differential conversion, the transformer provides a high impedance to the IC and performs impedance scaling to the antenna.

A four-phase mixer is used to limit the required input LO frequency range and to minimize the LO power consumption. The passive mixer is implemented with low-V_t devices to maximize the overdrive voltage and to minimize the switch resistance (20 Ω). The choice of the switch size was concluded to be an effective compromise between the noise, linearity, operating bandwidth, and power consumption, as was previously studied. The low-V_t devices are biased to approximately half of the supply voltage to ensure proper turn-off voltages and to avoid switch leakage during the presence of large blockers. However, this bias voltage is controllable through a voltage division block, which is buffered to the baseband input (CM Ctrl.). A triple-well configuration was used to tie the bulk to the same potential with the source and to isolate the mixer from the substrate. Additionally, the baseband dc offsets are compensated with current-steering D-to-A converters (offset IDACs).

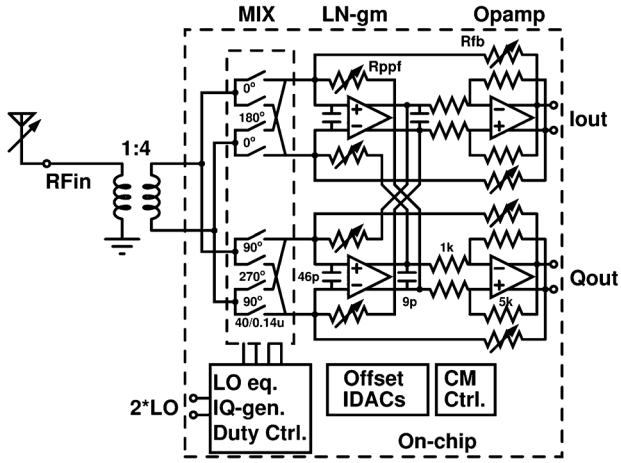

Fig. 11. Wideband receiver architecture overview with a quadrature passive mixer, a two-stage baseband filter and an LO chain.

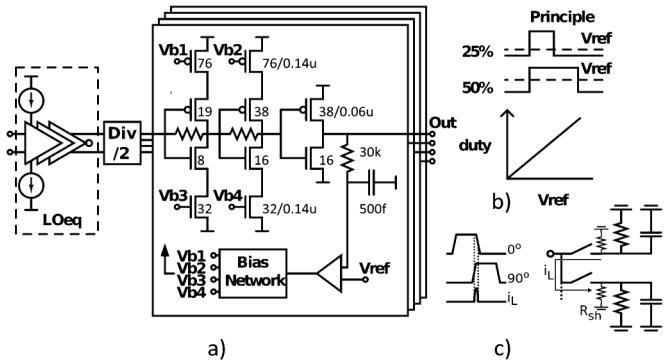

Fig. 12. (a) LO path block diagram with duty-cycle control, (b) operating principle, and (c) leakage mechanism with overlapping LO pulses.

Low-noise performance has been achieved with a differential LN-gm that uses a pMOS differential pair with a width/length (W/L) ratio of 1200, a 100-kHz $1/f$ noise corner, and a 7-mA current consumption. A local CM feedback with a 1-pF capacitor provides additional rejection for high-frequency interference. The cross-connected 3-bit polyphase resistors (Rppf) over the first stage perform complex input impedance tuning. According to simulations, the capacitance at the input of the mixer shifts the input impedance to the capacitive side of the Smith's chart and to perform matching, complex impedance tuning only in the inductive direction is needed.

The Opamp stage uses a lead-compensated two-stage amplifier with the driver stages drawing 22-mA current due to the 50-Ω requirement. The input stage of the opamp utilizes a W/L ratio of 2000 to achieve low noise and high linearity. By controlling the values of the adjustable 3-bit feedback resistance (Rfb in Fig. 11) and mixer switch series resistance (through duty cycle or overdrive voltage), the input matching impedance at the transformer input can be tuned between 28–330 Ω to accommodate the antenna interface. Furthermore, the feedback resistor enables bandwidth and gain control by adjusting the filtering *RC* product and by adjusting the switch resistance to feedback resistance ratio that controls the gain.

B. LO Drive Path

With the mixer-first topology, the LO signal chain design is emphasized since it directly affects the noise, linearity, and bandwidth performance of the receiver. We have implemented two circuits that improve the LO drive performance.

First, the LO equalization [LOeq in Fig. 12(a)] mitigates amplitude and phase imbalance by equalizing the input signal with regulated differential inverters. The circuit is capable of correcting an LO amplitude and phase imbalance of 5% and 5° to 0.03% and 0.6° at the divider input, respectively. Thus, it ensures good quality quadrature signals at the divider output.

Second, we have added a duty-cycle regulation loop to our LO drivers. The implementation and operating principle of the duty-cycle control circuitry for one of the LO quadrature paths is presented in Fig. 12. The dc component of the LO signal is linearly related to the duty cycle, as is depicted in Fig. 12(b). Therefore, by sampling the dc voltage of the output signal and comparing it to a reference voltage, we can offset the inverter chain bias points (Vb1–Vb4) such that the resulting signal has the desired duty cycle. Each of the inverter chains has a separate feedback that equalizes differences in gain and offsets. However, phase differences between the input signals are not equalized (LOeq is used for that). Additionally, the duty-cycle control helps to maintain signal waveform integrity at higher frequencies, where the LO clock signal is less ideal, by compensating the inverter bias points to boost the gain as frequency increases.

The feedback operational amplifier together with the inverter chain introduce a significant amount of dc gain to the loop. To ensure stability, the loop has been designed with a phase margin of 57°. The reference voltage for the opamp is generated with a 3-bit resistor network, which allows us to control the duty cycle from 15% to 52.5% in 2.5% steps. When the duty-cycle code exceeds 25%, the switches in the passive mixer start to conduct simultaneously. As depicted in Fig. 12(c), this creates a leakage current i_L from one baseband branch to another, which can be modeled with a shunt impedance R_{sh} that is in parallel with the baseband input impedance. The gain and NF of the receiver degrade as a direct consequence of this leakage, but the linearity is also improved, as will be shown in Section V-C. The LO chain consumes 14 mA from the supply with a 4-GHz input signal.

C. RFIC Measurement Results

The receiver was fabricated using a 65-nm CMOS technology and occupies an active area of 0.3 mm^2. The die micrograph with the measurement PCB and the balun are shown in Fig. 13. Fig. 14 shows the measured gain, NF, and third-order input intercept point (IIP3) of the receiver with the balun from 0.7 to 2.7 GHz. The gain of the receiver varies from 41 to 43 dB while the IIP3 is from $+17$ to $+20$ dBm (50- and 98-MHz offset test tones). The NF of the receiver varies from 4.2 to 6.0 dB. The balun has approximately an 1-dB impact on the NF. The results in Fig. 14 show that with the duty-cycle regulation, the gain droop and NF degradation can be mitigated at high frequencies. The blocker NF for a -15-dBm blocker was 5 dB and the rejection for third and fifth harmonics were 10 and 33 dB, respectively.

A second-order intermodulation intercept point (IIP2) (50- and 52-MHz offset test tones) better than 60 dBm was observed for in-phase (I)- and quadrature (Q)-branch dc-offset control

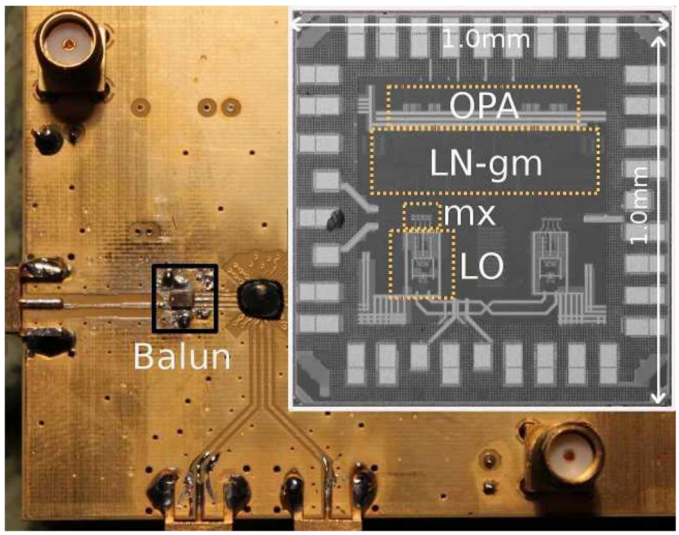

Fig. 13. Chip micrograph and the characterization PCB.

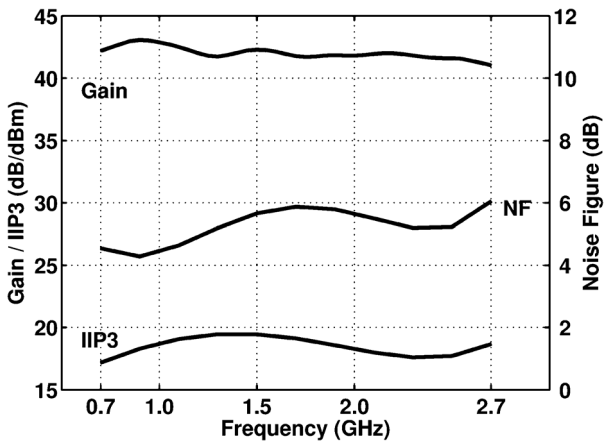

Fig. 14. Receiver gain, NF, and third-order intercept point over the reception band.

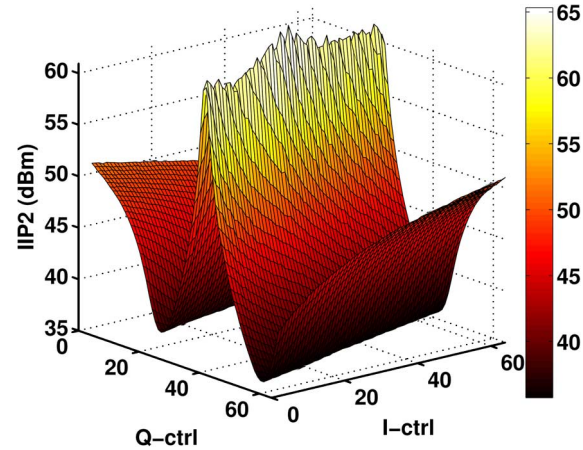

Fig. 15. IIP2 of the receiver against I- and Q-branch offset IDAC codes.

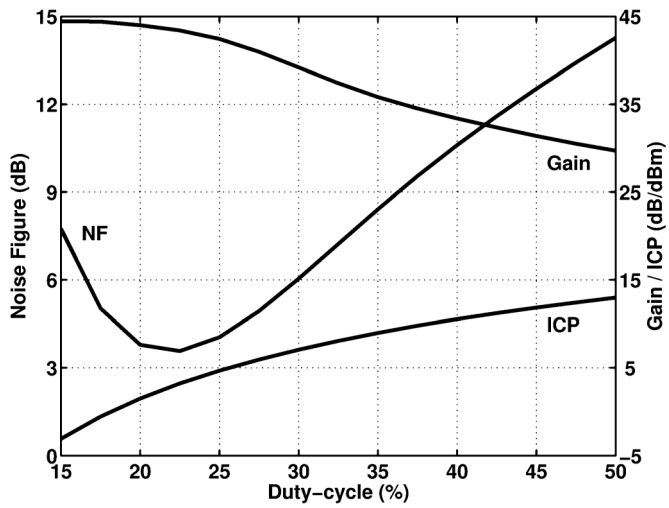

Fig. 16. Receiver gain, NF, and blocker ICP as a function of the LO duty cycle control.

codes that also result in low output dc offsets. A measurement result at 1 GHz from the Q-branch output against all I- and Q-codes is depicted in Fig. 15. With the optimal offset codes from IIP2 measurements, the LO leakage was less than −60 dBm over the entire band. The IQ amplitude and phase imbalance from the baseband output with a 1-MHz test signal were less than 0.5 dB and 0.5°, respectively.

Fig. 16 presents the performance of the receiver with different duty-cycle values at the RF frequency of 1 GHz. There is a clear optimal point for the receiver NF (3.5 dB) between duty cycles of 20% and 25%, which is where minimum switch resistance and signal leakage are achieved simultaneously. Increasing the duty cycle further decreases the effective series resistance of the mixer switches and causes the LO phases to overlap, which results in signal leaking from one branch to another. This decreases the signal gain, degrades the NF, and improves the −1-dB blocker input compression point (blocker ICP) (240-MHz offset) from −3 to +13 dBm, as depicted in Fig. 16. This result demonstrates that noise and linearity performance can be exchanged 10 dB by adjusting the duty cycle from 25% to 50%. The NF results at 50% duty cycle also explain why passive mixers conventionally have been considered to have poor noise performance. Table II shows the RF integrated circuit (RFIC) measurement results compared to recent similar IC implementations and simulations. The interface optimization allowed the reduction of the active area of the design while maintaining state-of-the-art performance. As can be seen from Table II, the duty-cycle control has no adverse effects on the performance while it ads a tradeoff possibility to our design.

VI. System-Level Experimental Results

The system experiments were executed in four parts: first, the system interface was co-designed prior to implementation of the RFIC; second, the characterization measurements were conducted to verify the antenna and RFIC functionality; third, the interface was verified with simulated and measured data; and fourth, the system measurements were conducted. Compared to conventional antenna or RFIC measurements, system validation involved making some nontrivial measurements. Many of these measurements were performed to normalize the input power at

TABLE II
RFIC RESULTS AND COMPARISON TABLE

	Simulated	**Measured**	[6]	[7]	[8]	[25]
Architecture	**MX+BB+ LO**	**MX+BB+ LO**	MX+BB+ LO	2xMX+ BB+LO	MX+BB +LO	LNA+MX+ BB+LO+SX
Freq. (GHz)	**0.7-2.7**	**0.7-2.7**	0.1-2.4	0.08-2.7	0.2-2.0	0.4-3[2]
Req LO range (GHz)	**1.4-5.4**	**1.4-5.4**	0.4-4.8	0.32-10.8	0.8-8	0.8-6
Gain (dB)	**41**	**40**	40-70	70	19	70
NF (dB)	**3.0-4.5**[1]	**3.2-5**[1]	3-10	1.5-2.4	6.5	3
OB-IIP3 (dBm)	**+17**	**+17**	+25	+13.5	+11	+10
IIP2 (dBm)	**na**	**+60**	+56	+54	+65	+70
1dB ICP (dBm)	**+10**	**+5**	+5	-1	na	-8
IQ imbal. (dB/°)	**na**	**0.5/0.5**	na	na	na	na
Power (mW)	**30-40**[3]	**31-42**[3]	37-70	35-78	67	30-55
Supply (V)	**1.2**	**1.2**	1.2/2.5	1.3	1.2	1.1/2.5
Active area (mm^2)	**0.27**	**0.27**	0.75	1.2	0.13	2
CMOS Technology	**65 nm**	**65 nm**	65 nm	40 nm	65 nm	40 nm

[1] Without 1-dB balun loss [2] Estimated −3-dB bandwidth [3] Excluding 50-Ω BB drivers

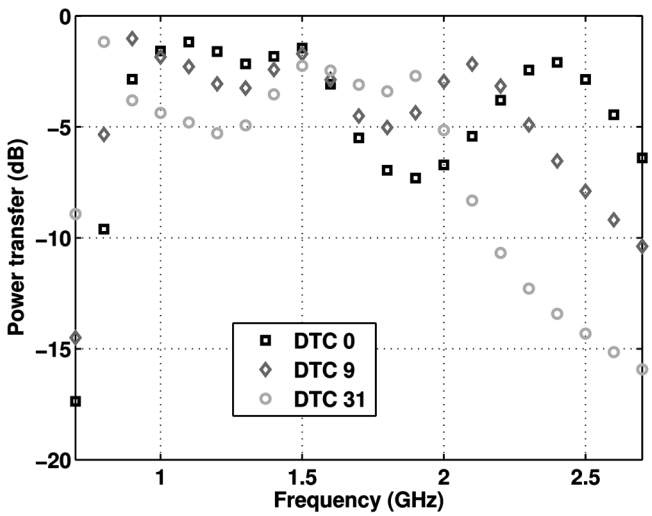

Fig. 17. Simulated power transfer from the antenna through the impedance matching circuit and balun transformer to the IC.

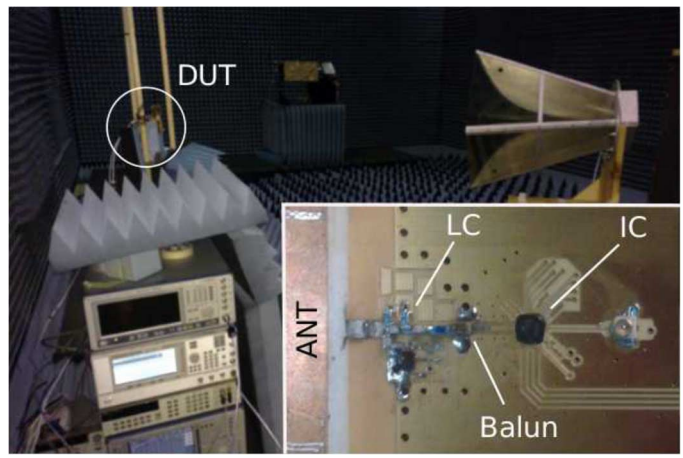

Fig. 18. System measurement setup with an inset of the PCB with the antenna element, matching (LC) components, balun, and IC.

the antenna, and thus, avoid the approximative link budget calculations. Additionally, in order to achieve reliable and repeatable measurements, a number of interference and setup related issues were solved; e.g., interference leaking through the reference and control lines was observed and fixed during the sensitivity measurements.

During the interface verification, the tunable matching circuit was optimized with circuit simulations so that it allowed maximum average power transfer from the antenna to the IC (between nodes A and C in Fig. 2). An impedance transforming 1:4 commercial balun (Anaren Xinger BD0826J50200AHF) was selected to alleviate the impedance matching of the antenna to a suitable IC impedance. The simulated result of this optimization with three different DTC states is presented in Fig. 17. The simulation result shows that the impedance at the antenna–IC interface is suitable across the frequency band of 0.7–2.7 GHz.

To verify the functionality of the interface arrangement, the inherently low-impedance CCE antenna and the mixer-first receiver were assembled on a four-layer Rogers (4350B/4403) PCB substrate and measured over the air with the help of a transmitting dual-polarized Vivaldi antenna. The measurement arrangement and the PCB are depicted in Fig. 18. The PCB inset shows the implementation of the system with the antenna element on the left (ANT), matching circuit in the middle (LC) followed by the Balun and the IC. The ground plane was kept as uniform as possible to avoid resonating slots and, thus, to keep the antenna performance realistic. The measurements were performed in an anechoic chamber as is depicted in Fig. 18. Due to practical reasons such as control line length, RF signaling, and attenuation, part of the equipment had to be placed near the test fixture and covered with absorbers. The propagating wave on the ground shield of the signaling cables (LO, bus, supply, and bias) was suppressed with ferrite beads.

The measured frequency response of the system is presented in Fig. 19 for three different DTC tuning codes. The measurement includes all the dissipative and reflective losses of the system, and thus, the measured gain is lower than for the IC characterization measurement in Fig. 14. Compared to the default (DTC 0) code, we were able to achieve up to 3-dB im-

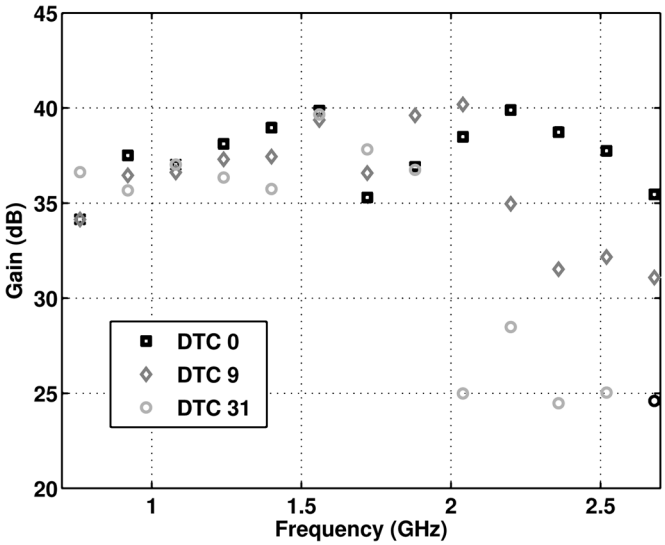

Fig. 19. System frequency response with the reception antenna.

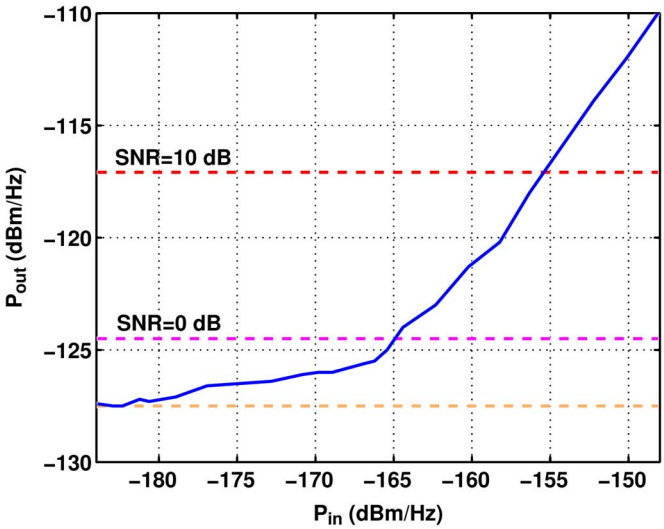

Fig. 20. System sensitivity measurement with the reception antenna.

provement in system gain at certain frequencies by tuning the DTC codes. At 1.7-GHz frequency, the system displays a noticeable reduction in gain. The radiation resistance minimum of the CCE poses an unfavorable impedance environment to the DTC at this frequency, thus increasing losses [41].

The sensitivity measurement of the receiver at 1 GHz is shown in Fig. 20, where also the signal-to-noise ratio (SNR) levels of 0 and 10 dB are depicted. The NF of the system can be approximated from

$$\mathrm{NF} = 174 - 10\log(\mathrm{BW}) - \mathrm{SNR}_{\mathrm{out}} + P_{\mathrm{in}} \qquad (3)$$

where BW is the bandwidth, $\mathrm{SNR}_{\mathrm{out}}$ is the desired SNR, and P_{in} is the input power level where the SNR level is met. The approximation gives an overall system NF of 9 dB including all losses. We approximated the 9-dB NF to consist of the following contributions: antenna loss 2–3 dB, matching and balun 2–3 dB, and IC 4 dB.

In linearity measurements, providing the antenna with sufficient power was challenging. With a very linear RFIC and a total path loss of over 40 dB to the antenna, the power at the receiving antenna is too small and the intermodulation products easily fall under the noise floor. Due to this reason, blocker ICP measurements could not be performed. However, with the test tones of 1.050 and 1.098 GHz, we measured an third-order intermodulation intercept point (IIP3) of +17 dBm, which is in line with the RFIC results.

During the measurements, the tuning of the receiver feedback resistor (R_{fb} in Fig. 11) was found to contribute very small changes to the actual frequency response shape of the system. There are two possible reasons for this. First, the transformer efficiently suppresses all impedance changes visible at the balanced side to the unbalanced side, due to both the transforming ratio and the internal matching of the component. Second, any transmission line between the receiver and the balun will shift the impedance on the Smith's chart, and thus, affect the intended matching impedance. To optimize performance, it would be beneficial to implement the transformer on-chip to circumvent this interface dilemma. In a more general case, a wideband SDR interface needs to minimize the lengths of all RF traces, as it is difficult to guarantee an ideal matching impedance over a wide bandwidth.

VII. Conclusion

A concept demonstrator of a mobile-handset-size single-antenna SDR receiver with wide bandwidth was presented. The work included considerations of the antenna-IC interface, where the system design choices were discussed. It was shown that with a 5-bit DTC, a compact reference CCE antenna achieved continuos tuning range of 0.75–2.5 GHz together with 45%–69% total efficiency to a 50-Ω measurement interface. Together with the presented receiver, the tuning range was extended up to 2.7 GHz. The antenna compares favorably to other recently published antennas of the same volume.

Special attention in the design was paid to the interface impedances between the antenna and IC. From the study, it was concluded that in terms of noise, linearity, power, and operating bandwidth of the receiver, it is desirable to choose a high interface impedance. On the other hand, the antenna has inherently low unbalanced radiation resistance so a reasonable compromise was needed. We used a 1:4 impedance transforming balun to satisfy the higher input impedance requirement.

The SDR receiver IC demonstrated an NF of 3.2–5 dB and a blocker ICP of +5 dBm, while occupying only 0.3 mm^2 of active die area. LO duty-cycle adjustment was proposed as means to regulate the LO signal and trade off the receiver noise and linearity by 10 dB. The performance of the IC is comparable to other state-of-the-art receivers.

The system measurements showed that we were able to maintain the performance of the RFIC receiver with a slight degradation. The interface arrangement proved that the low-resistance CCE antenna and the high-input impedance receiver can successfully be made interoperable. Finally, the system measurements showed that it is paramount to minimize the SDR interface transmission line lengths in order to avoid excessive phase rotation of the signal over the reception band, especially with the balun. In practice, the phase rotation is always present in a wideband radio interface and requires tight codesign between the antenna and receiver engineers to properly match the antenna and

the receiver. To our knowledge, this is the first demonstration of a compact-size single-antenna single-input receiver covering the LTE bands from 0.7 to 2.7 GHz.

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