Middle East Technical University   Department of Computer Engineering

CENG 232

Logic Design

Spring '2017-2018

Lab 3

Part 1 Due Date: 4 April 2018, Wednesday, 23:59
Part 2 Due Date: 11 April 2018, Wednesday, 23:59
No late submissions

1 Introduction

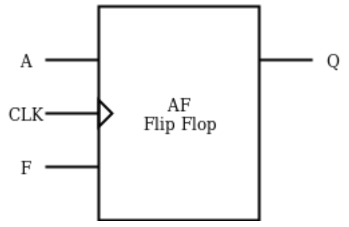
This assignment aims to make you familiar with Verilog language, related software tools, and the FPGA boards. There are two parts in this assignment. The first part is a Verilog simulation of an imaginary flip-flop design, which you are required to implement and test on your own. The second part consists of simulation and implementation (on FPGA) of MarsAdventure system.

2 Part 1: AF - Flip Flop (Individual Work)

This part of the lab will be performed and submitted individually (NOT WITH YOUR GROUP PARTNER !). You are given a specification of a new type of flip-flop, and a new chip that uses the flip-flop. Your task is to implement these in Verilog, and prove that they work according to their specifications by simulation.

2.1

Implement the following AF flip-flop in Verilog with respect to the provided truth table. An AF flip-flop has 4 operations when inputs A and F are: 00 (complement), 01 (no change), 10 (set to 1), 11 (set to 0). Please note that the AF Flip-Flop changes its state only at rising clock edges.



2.2

Implement the following chip that contains two AF flip-flops which has output Y.

Use the following module definitions for the modules:

```
module af(input a, input f, input clk, output reg q)
module ic1500(input a0, input f0, input a1, input f1, input clk, output q0, output q1, output y)
```

Table 1: AF - flip-flop truth table.

A	F	Q	Qnext
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

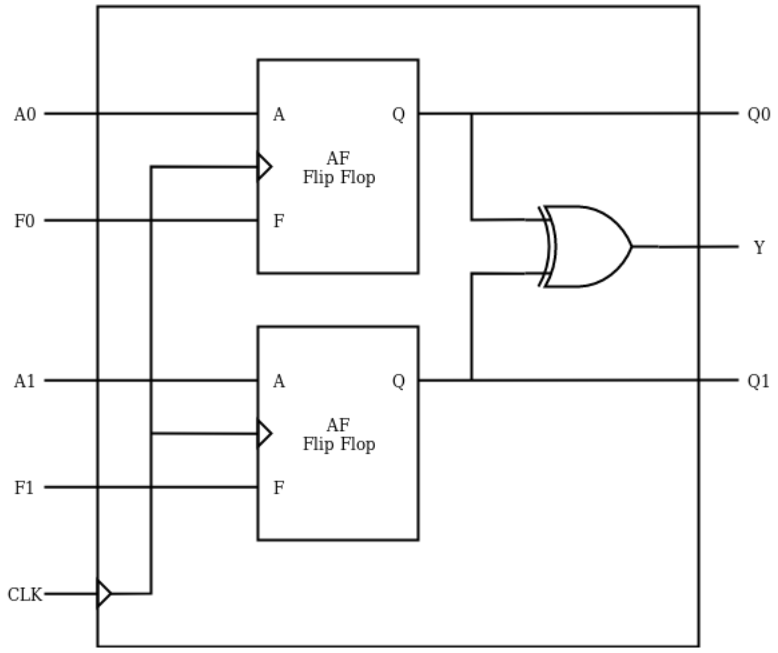


Figure 1: ic1500 module, inputs and outpus.

2.3 Simulation

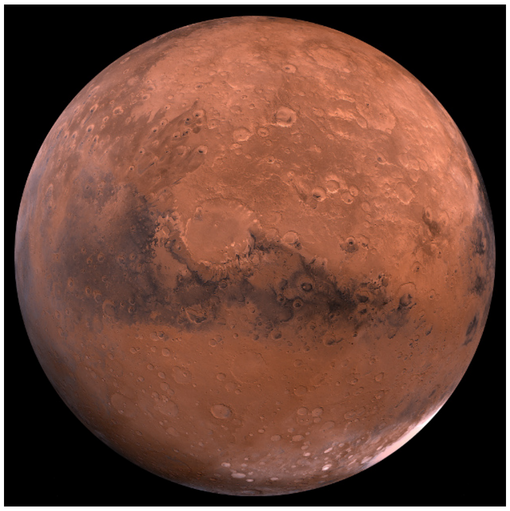
A sample testbench for af-flipflop module will be provided to you. It is your responsibility to extend the testbench, and also to write a testbench for ic1500 module.

2.4 Deliverables

- Implement both modules in a single Verilog file: lab3_1.v. Do NOT submit your testbenches. You can share your testbenches on the newsgroup.
- Submit the file through the COW system before the given deadline. **April 4, 2018, 23:59**
- This part is supposed to be done individually, not with your partner. Any kind of cheating is not allowed.

3 Part 2: MarsAdventure (Teamwork)

This part of the lab will be performed and submitted with your group partner. Only submit a single copy per group.



3.1 Problem Definition

Not too distant future...

Humankind was beginning to move to Mars. That was the first attempt to transfer humankind to Mars. As a successful and intelligent student, you were a member of the crew too. Everything went well until a horrible crash took place, just before the landing. Luckily, you survived from that crash and successfully landed to Mars. But as a side effect you lost contact with any member of the crew. At the place where you landed, there were people around you but they weren't humans... So, you started to live with them. The bad thing was, you were not able to understand their language. To learn their language, you decided to design a hardware that helps you to memorize words of their language.

The first thing you understand was, each **word** consisted of 5 bits. There were two different **languages** spoken by local residents. You named these different residents as **hipsterians** and **nerdians**. Each **word** can be a member of: **hipsterians** language, **nerdians** language, member of both of them or not a member of any of them.

As you are a systematically working, computer engineer wanna be; you generated your own specifications before implementing the system:

1. Each **word** spoken by Mars residents consists of a 5-bit number.
2. If a **word** consists of at least one consecutive 0s (ex. 00 or 000 or 0000 etc.), then this word is a member of **hipsterians** language.
3. If a **word** consists of at least one consecutive 1s (ex. 11 or 111 or 1111 etc.), then this word is a member of **nerdians** language.
4. The current number of **words** memorized from any language is recorded for each language separately. If a word is memorized from a language, the current number of words memorized from that language should be updated.
5. You have two **modes** in this system. The in-mode is active when the **mode** option is 1, out-mode is active when the **mode** option is 0.
6. If the system is in the in-mode, number of words in that language should be increased by one. If the system is in the out-mode, number of words in that language should be decreased by one.
7. To not memorize wrong words for the wrong language, you come with a **selection** option idea. **selection** option is 0 for **hipsterians** language and 1 for **nerdians** language.
8. If a word is a member of **hipsterians** language and the selection is 0, then the system should update (can be an increase or decrease) the number of words for **hipsterians**. If a word is a member of **hipsterians** and the selection is 1, then the system should not update the number. Instead of it, it should give a warning. Vice versa is correct for **nerdians**. If a word is a member of **nerdians** language and the selection is 1, then the system should update (can be an increase or decrease) the number of words for **nerdians**. If a word is a member of **nerdians** and the selection is 0, then the system should not update the number. Instead of it, it should give a warning.

9. If a word is a member of both languages, the system will increase the number of words for the language that is currently selected by the **selection** option. The number of words for the other language should not change.
10. If a word is not a member of any of the languages, the system should give a warning independent from the **selection** option and should not update the number of words for both of the languages.
11. Initially, number of words in both languages are 0.
12. If an out action is applied when the number of words for a language is 0, it should stay at 0 (without any warning).
13. When in out-mode, the word won't be checked if it is registered before. (Actually we don't have memory, we only check if the word is satisfying the conditions or not.)
14. Similarly, in in-mode the word won't be checked if it is registered before.
15. The number of words for languages will be shown in decimal form with two digits.
16. The number of words for languages varies between 0 and 20. (2 is one digit and 0 is one digit)
17. If number of words exceeds 20, it should be returned to 0. (20 is included, after 20 it returns to 0.)

3.2 Sample Input/Output

- The values in **Current State** column, which are seperated by "**,**" are defined as: **word**, **selection**, **mode**, **hipsterians1**, **hipsterians0** , **nerdians1**, **nerdians0** respectively. (**hipsterians1** is the most significant digit of number of **hipsterians**, **hipsterians0** is the least significant digit of **hipsterians**. Same is applied for **nerdians**)
- The values in **Next State** column, which are seperated by "**,**" are defined as: **hipsterians1**, **hipsterians0**, **nerdians1**, **nerdians0**, **warning**, respectively.

Table 2: Sample inputs and outputs.

current state	CLK	next state
10010, 0, 1, 0, 0, 0, 0	$\uparrow$	0, 1, 0, 0, 0
00110, 1, 1, 0, 2, 1, 9	$\uparrow$	0, 2, 2, 0, 0
01010, 1, 1, 1, 8, 0, 0	$\uparrow$	1, 8, 0, 0, 1
01000, 0, 0, 1, 8, 0, 0	$\uparrow$	1, 7, 0, 0, 0
01100, 1, 0, 1, 8, 0, 0	$\uparrow$	1, 8, 0, 0, 0
00110, 0, 1, 0, 2, 1, 9	$\uparrow$	0, 3, 1, 9, 0

3.3 Input/Output Specifications

- **word** represents 5-bit code.
- **CLK** is the clock input for the module.
- **selection** is used for the selection of the language.
  selection = 0 $\Rightarrow$ hipsterians language
  selection = 1 $\Rightarrow$ nerdians language
- **mode** is used to indicate whether a word is added to the word count or a word is removed from word count.
  mode = 0 $\Rightarrow$ word is removed (out-mode)
  mode = 1 $\Rightarrow$ word is added (in-mode)
- **hipsterians1**, **hipsterians0** and **nerdians1**, **nerdians0** shows the number of words in each of the languages. Where 1 is the most significant digit and 0 is the least significant bit.
- **warning** shows the warning situations.
  warning = 0 $\Rightarrow$ no warning occured.
  warning = 1 $\Rightarrow$ warning occured.

Table 3: Inputs and output variables

Name	Type	Size
word	Input	5 bits
Clock (CLK)	Input	1 bit
selection	Input	1 bit
mode	Input	1 bit
hipsterians1	Output	8 bits
hipsterians0	Output	8 bits
nerdians1	Output	8 bits
nerdians0	Output	8 bits
warning	Output	1 bit

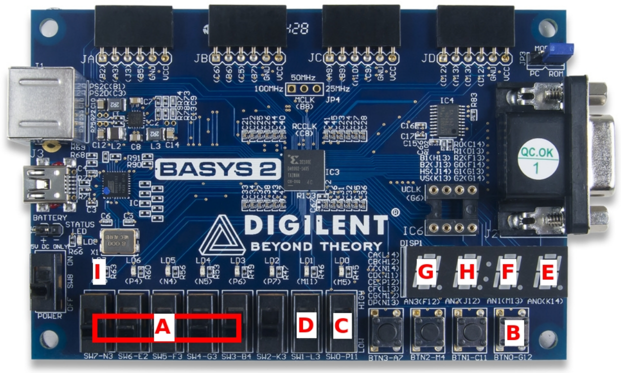
3.4 FPGA Implementation

You will be provided with a Board232.v file (and a ready-to-use Xilinx project), which will bind inputs and outputs of the FPGA board with your Verilog module. You are required to test your Verilog module on the FPGA boards. After the submission date, you will make a demo to course assistants.

Table 4: Button descriptions.

Name	FPGA Board	Description
word	SW7, SW6, SW5, SW4, SW3	Left-most 5 switches (A)
Clock (CLK)	BTN0	Right-most button (B)
selection	SW0	Right-most switch (C)
mode	SW1	The switch next to SW0 (D)
hipsterians0	7-segment display	Right-most 7-segment display (E)
hipsterians1	7-segment display	Second right-most 7-segment display (F)
nerdians1	7-segment display	Left-most 7-segment display (G)
nerdians0	7-segment display	Second left-most 7-segment display (H)
warning	LD7	Left-most led (I)

Figure 2: Board with the button informations.



3.5 Deliverables

- Implement your module in a single Verilog file: lab3_2.v. Do NOT submit your testbenches.You may share your testbenches on the newsgroup.
- Submit the file through the COW system before the given deadline. **April 11, 2018, 23:59**

- This part is supposed to be done with your group partner. Make sure both of you take roles in implementation of the project. Any kind of inter-group cheating is not allowed.
- Use the newsgroup metu.ceng.course.232 for any questions regarding the homework.
- You will make a demo with the FPGA board the next week after the submissions (in your lab session hours). The exact dates and place will be announced later.