Ceng 3010
Computer Organization

Term Project II
Designing 16 bit Single Cycle Risc Machine

Report

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Introduction

Now days, Computers are mainstream in quotidian activities. RISC Processor is a CPU design strategy that uses simplified instructions for higher performance with faster execution of instruction. It also reduces the delay in execution. It uses general instructions rather than specialized instructions. They are less costly to design, test and manufacture. This has helped in implementation of RISC in technological field. Its range of application includes signal processing, convolution application, supercomputers such as K computers and wider base for smart phones.

The Features Of Design

- 16-bit RISC-based single-cycle design processor. The processor should support the following instruction set;

  add sub and or

  slt slti j jr

  jal sll srl beq

  bne mult muli lui

  lw sw

- 8 registers with a length of 16 bits.

- -The multiplication instructions supports 8 x 8-bit multiplication in mul, and multiplication of the lower half of the register with immediate value in the muli instruction.

- Grouped instructions according to their types, the design for the datapath, and control.

- single-cycle processor approach.

- 1K bytes of IM and DM, and processors supports, as much capability as possible like loops (branches), procedures, and their calls.

The Architecture Of Design

Instruction design

R-Type

4-bit OpCode------3-bit Rs------3-bit Rt-----3-bit Rd----------3-bit Function Code

Given add,sub,and,or,slt,sll,srl,mult is R-type instructions.

R types generaly have same opcode which is 4’h8

The function code sends alu to AluOp codes

The instructions which have 4’h8

Function code = 3’b001 for Add R[rd] = R[rs] + R[rt]

Function code = 3’b010 for And R[rd] = R[rs] & R[rt]

Function code = 3’b011 for Sub R[rd] = R[rs] - R[rt]

Function code = 3’b100 for Or R[rd] = R[rs] | R[rt]

Function code = 3’b101 for Slt R[rd] = (R[rs] < R[rt]) ? 1 : 0

Function code = 3’b111 for Mult R[rd] = R[rs] * R[rt]

Function code = 3’b000 for default::

The instructions which have not 4’h8

Op code = 4’b1010 for sll R[rd] = R[rt] << shamt

Op code = 4’b0110 for srl R[rd] = R[rt] >> shamt

The Architecture Of Design

Instruction design

I-Type

4-bit OpCode----------3-bit Rs----------3-bit Rt----------6-bit Immediate

Given Muli,Slti,lui,lw,sw,beq,bne,ori,addi is I-type instructions.

The OpCode of I type instructions are

Op code = 4’b1100 for slti R[rt] = (R[rs] < SignExtImm)? 1 : 0

Op code = 4’b1110 for lui R[rt] = {imm, 16’b0}

Op code = 4’b1111 for lw R[rt] = M[R[rs]+SignExtImm]

Op code = 4’b0011 for sw M[R[rs]+SignExtImm] = R[rt]

Op code = 4’b0000 for beq if(R[rs]==R[rt]) PC=PC+4+BranchAddr

Op code = 4’b0101 for ori R[rt] = R[rs] | ZeroExtImm

Op code = 4’b1011 for addi R[rt] = R[rs] + SignExtImm

The Architecture Of Design

Instruction design

J-Type

4-bit OpCode----------12-bit Immediate

Given j,jr,jal is J-type instructions.

The OpCode of J type instructions are

Op code = 4’b0001 for j	PC=JumpAddr
Op code = 4’b1001 for jal	R[5]=PC+8;PC=JumpAddr

Registers

Register [0], Register [1], Register [2], Register [3], Register [4], Register [7]

are General purpose registers.

Register [5]

reserved for return address which is for jal instruction.

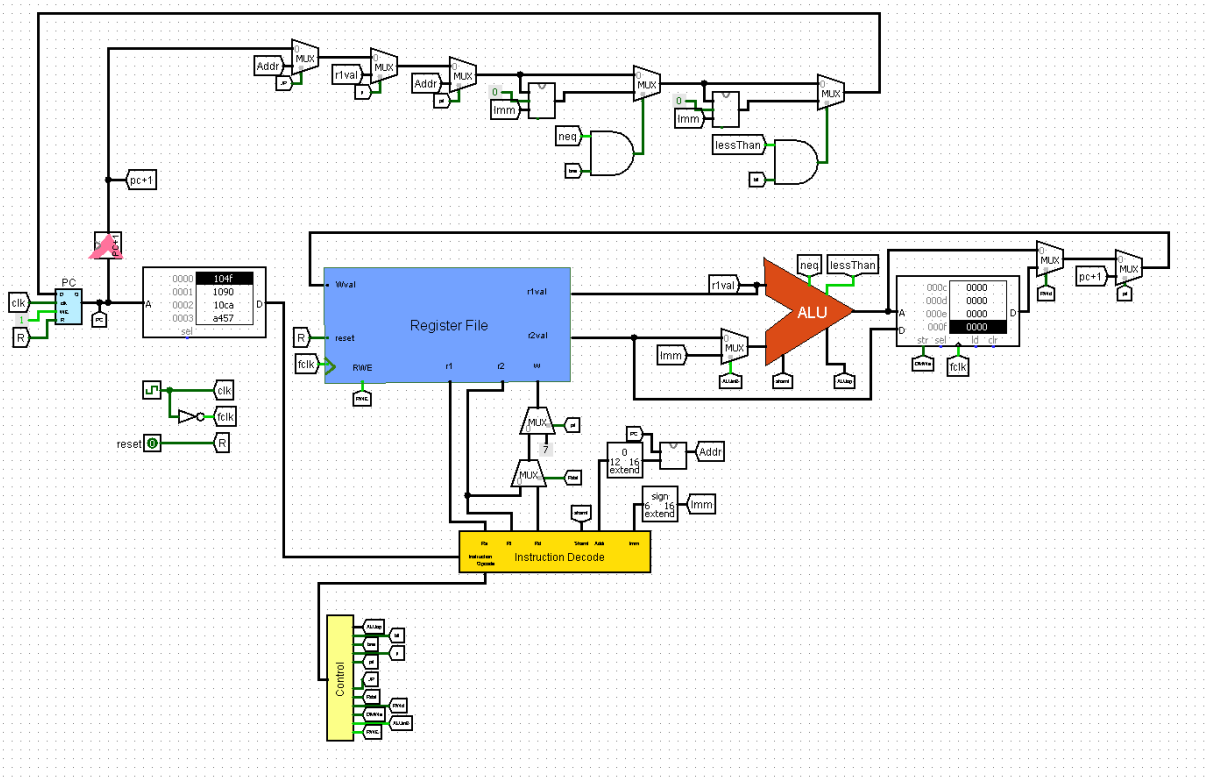
Register [6]

reserved for stack pointer which is 128 at beginning.

The Architecture Of Design

DATAPATH

The below block schematic shows the overall architecture of the processor. The designed RISC processor .The blocks present in the architecture are: ALU, Control Unit, Instruction Memory, Data Memory, Program Counter, Register File and various MUX units.

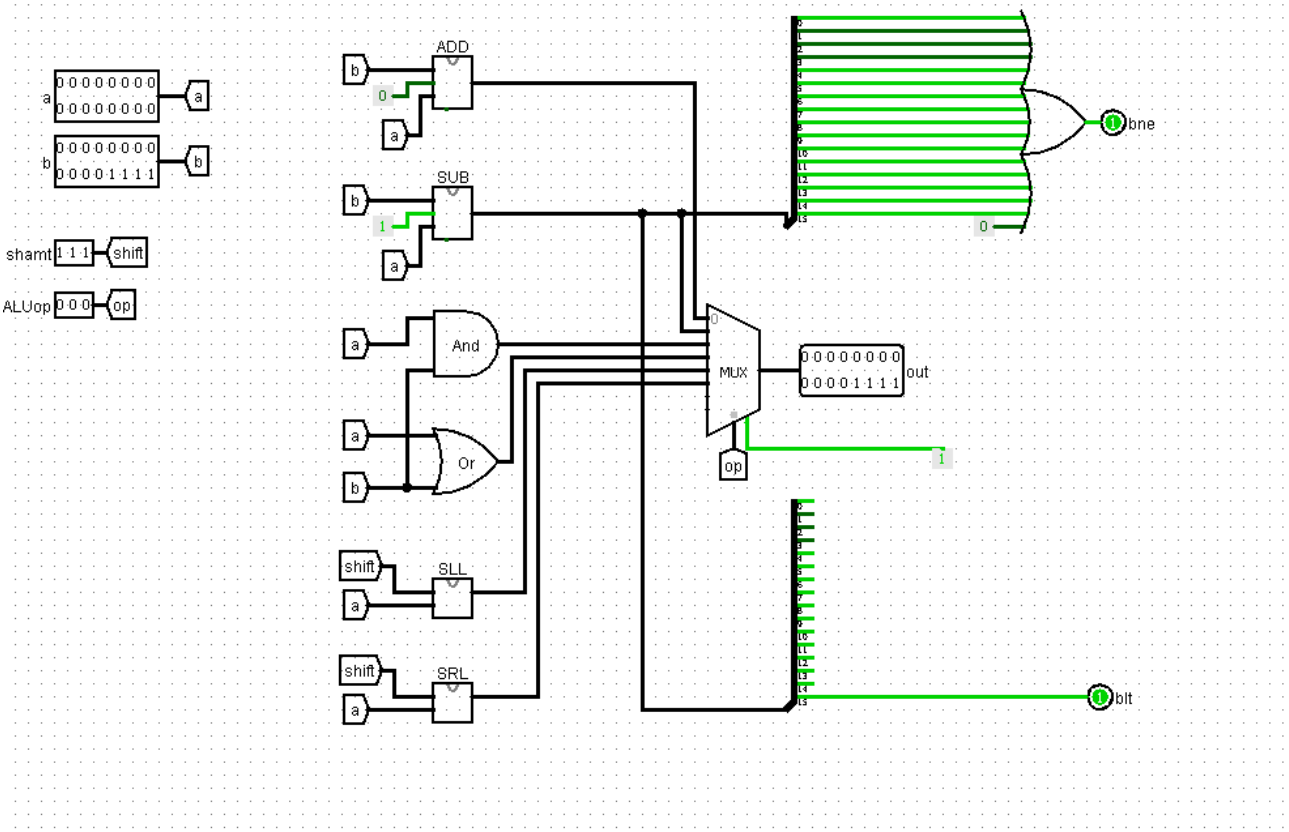


Data Path refers to the collection of various units in the CPU like ALU, control unit, various registers, multipliers and buses. The Verilog HDL code for the datapath includes interconnection of the various blocks present in the architecture.

The Architecture Of Design

ALU

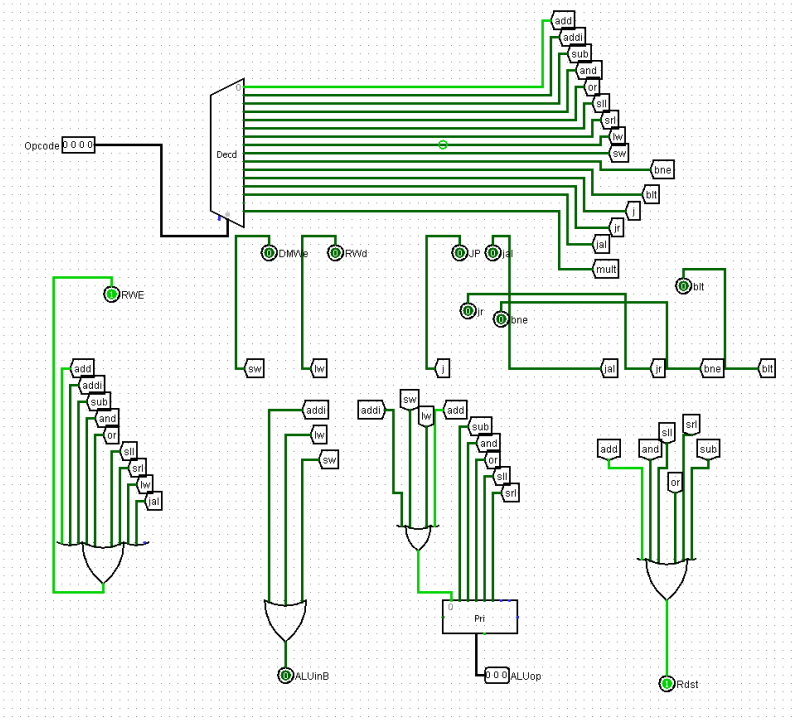
The arithmetic logical unit (ALU) we have designed is a very simple one. Its functions include basic arithmetic operations, bit shifting operations and logical operations.



The Architecture Of Design

Control Unit

The control unit (CU) is a component of the processor. It tells the computer's memory, arithmetic and logic unit and input and output devices how to respond to the instructions that have been sent to the processor. It directs the operation of the other units by providing timing and control signals. Most computer resources are managed by the CU. Hardwired control units are implemented through use of combinational logic units, featuring a finite number of gates that can generate specific results based on the instructions that were used to invoke those responses. Hardwired control units are generally faster than the micro programmed designs. The Design for the control unit is shown below.



Verilog Design

Design Utilization Summary

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	144	126,800	1%
Number used as Flip Flops	144		
Number used as Latches	0		
Number used as Latch-thrus	0		
Number used as AND/OR logics	0		
Number of Slice LUTs	1,048	63,400	1%
Number used as logic	1,014	63,400	1%
Number using O6 output only	974		
Number using O5 output only	13		
Number using O5 and O6	27		
Number used as ROM	0		
Number used as Memory	32	19,000	1%
Number used as Dual Port RAM	0		
Number used as Single Port RAM	32		
Number using O6 output only	32		
Number using O5 output only	0		
Number using O5 and O6	0		
Number used as Shift Register	0		

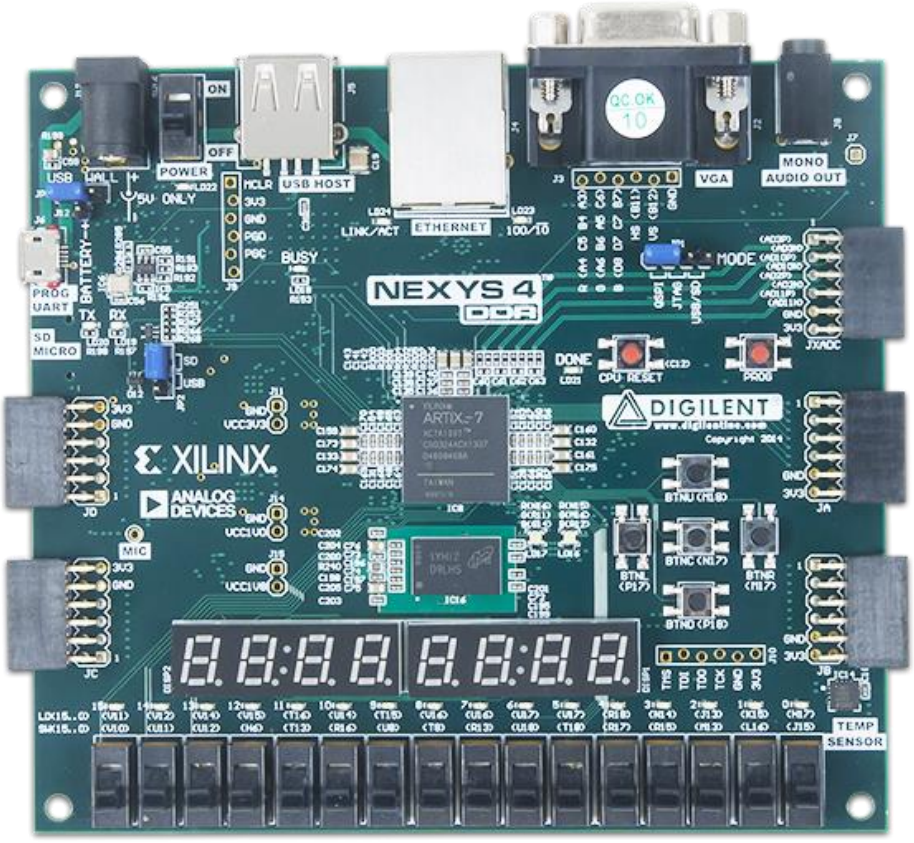
Verilog Design

Design Testbench Summary

FPGA Design

FPGA Board Description

The Nexys 4 DDR board is a complete, ready-to-use digital circuit development platform based on the latest Artix-7™ Field Programmable Gate Array (FPGA) from Xilinx®. generous external memories, and collection of USB, Ethernet, and other ports, the Nexys4 DDR can host designs ranging from introductory combinational circuits to powerful embedded processors. Several built-in peripherals, including an accelerometer, temperature sensor, MEMs digital microphone, a speaker amplifier, and several I/O devices allow the Nexys4 DDR to be used for a wide range of designs without needing any other components.



The Nexys4 DDR board includes a single 100 MHz crystal oscillator

15,850 logic slices, each with four 6-input LUTs and 8 flip-flops

4,860 Kbits of fast block RAM

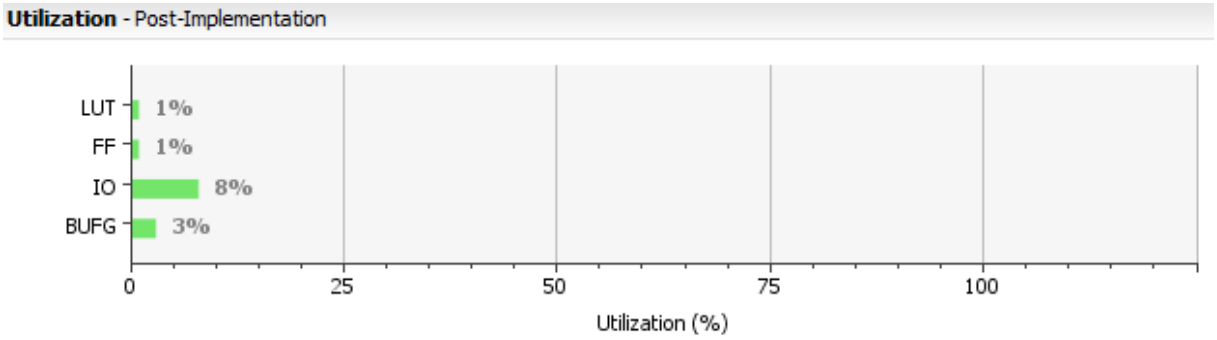
More about inside the link

https://digilent.com/reference/programmable-logic/nexys-4-ddr/reference-manual

FPGA Design

FPGA Board Utilization and Timing Summary

Low usage of LookUp Table(lut) and FlipFlops(FF) this design work perfectly on the given board



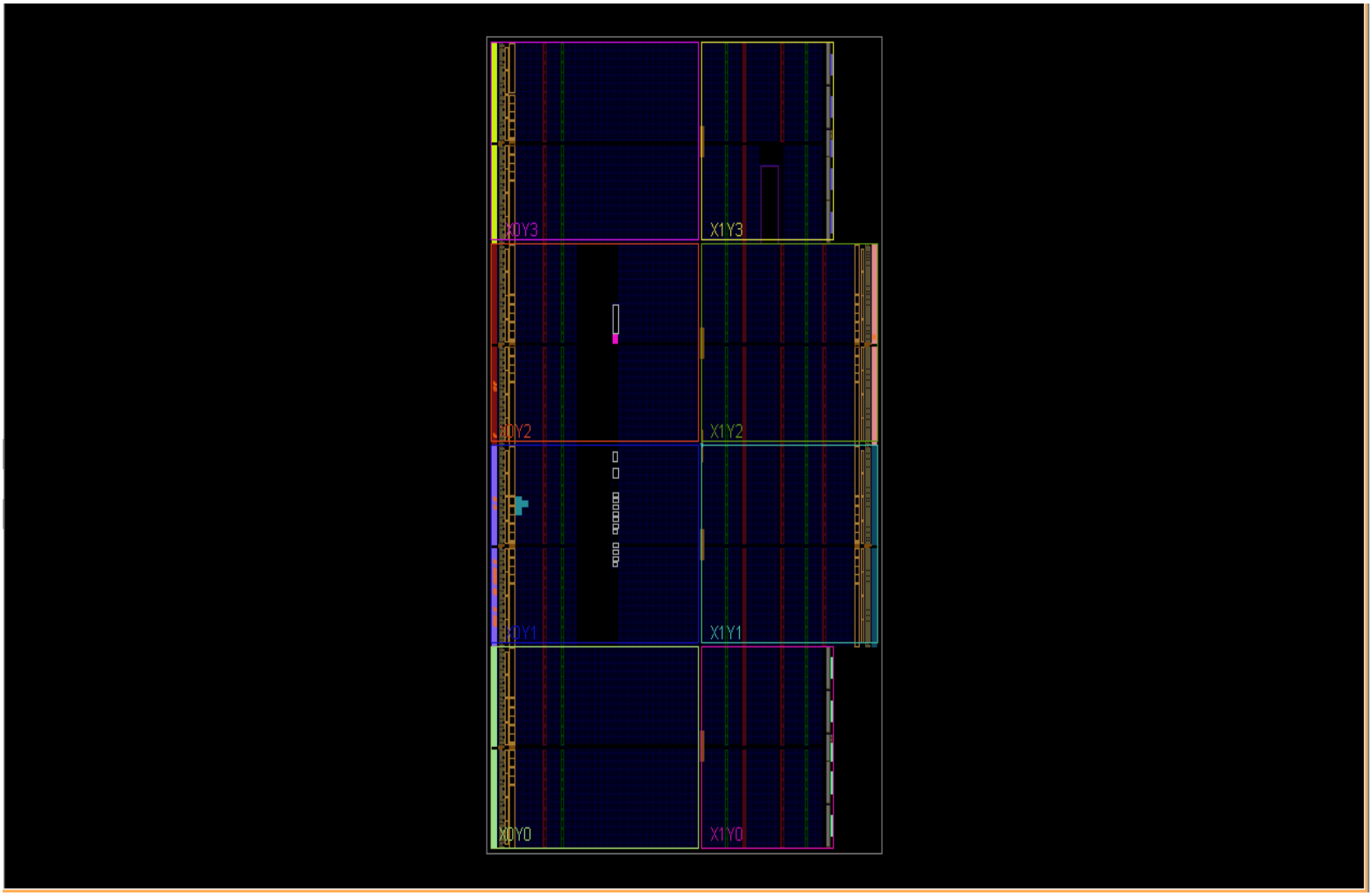
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5,708 ns	Worst Hold Slack (WHS):	0,352 ns	Worst Pulse Width Slack (WPWS):	4,500 ns
Total Negative Slack (TNS):	0,000 ns	Total Hold Slack (THS):	0,000 ns	Total Pulse Width Negative Slack (TPWS):	0,000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	8	Total Number of Endpoints:	8	Total Number of Endpoints:	9

All user specified timing constraints are met.

Because of the high value of Worst negative slack (WNS) this design work on higher frequency of clock which is currently on 100 mHz

FPGA Design

Implemented FPGA design



Summary

Thus, we have designed and simulated a 16-bit RISC processor using Verilog and verified its working by simulation. The processor can be extended to a 32 or even a 64-bit processor in the future by simple changes in the code and the datapath can be altered to include various new blocks which is not possible on a traditional processor unit.