Strathmore
UNIVERSITY

SCHOOL OF COMPUTING AND ENGINEERING SCIENCES (SCES)
BACHELORS OF SCIENCE (INFORMATION AND COMMUNICATION SYSTEMS)
END OF SEMESTER REVISION TUTORIALS
ICS 3111: MICROPROCESSORS

DATE: JUNE 2024 SAMPLE QUESTIONS

A. Lesson 1: Introduction to Microprocessors

1. Define the following terms
   - ✓ Microprocessor
   - ✓ Microcontroller
   - ✓ ALU
   - ✓ CPU
2. Briefly describe the historical perspectives of Intel microprocessors
3. Using a well labelled diagram, illustrate how the data bus, control bus and address bus are interconnected to the CPU, Input devices, Output devices, and Memory, explain the function of each component in your diagram

B. Lesson 2: Overview of Other Microprocessors

1. Explain the functions of at least 8 control bus pins of a 80186 microprocessor
2. Model a block diagram of the internal architecture of the 80286 microprocessor and explain the how it works with regard to input/ output data flows and data processing
3. Name the various Intel microprocessors that hit the market in the years between 2007 to 2020 and explain their differences in features/ capabilities

C. Lesson 3: Internal Architecture of 8085 Microprocessor

1. Describe the functions of at least five flags available in the 8085
2. State four special function registers of the 8085 and describe their work
3. Using a diagram explain how the internal layout of the 8085 microprocessor components functions to ensure effective data flow (IN and OUT) and data processing

D. Lesson 4: 8085 Pin Out Diagram

1. Discuss the operational purposes of the following pins with respect to 8085 microprocessor
   - ✓ RESET OUT
   - ✓ HOLDA
   - ✓ X2
   - ✓ AD5
   - ✓ READY
   - ✓ ALE
   - ✓ IO/M
   - ✓ INTA
2. Describe the bus structure/ bus design of the 8085
3. State at least five specifications of the 8085 microprocessors

E. Lesson 5: Machine Cycles

1. Describe how the IO/M, S1, S2, RD, WR, and INTA Control lines manage the various machine cycle operations
2. Outline the key differences between a machine cycle and an instruction cycle
3. With respect to logic states of a microprocessor explain the interpretation of the following status of a control line
    - ✓ ACTIVE HIGH
    - ✓ ACTIVE LOW
    - ✓ TRI-STATE
    - ✓ UNSPECIFIED

F. Lesson 6: Demultiplexing the Data/Address Buses

1. Using a well labelled diagram, describe how latches are utilized to demultiplex the data bus/address bus of the 8085 microprocessor
2. State and explain three advantages of a demultiplexed data bus in a microprocessor system
3. Discuss the operational functions and difference between higher-order address and lower order address

G. Lesson 7: Memory Design, Sizing and Address Mapping

1. Draw the circuit layout diagram of a Flip-Flops based 8-bit storage element, illustrating the connection of the data bus into and out of the unit, connection of WR and RD control lines and the EN (address line)
2. Describe the address map with diagrams showing how 1K (1028x8) memory is mapped. Show all the control signals
3. Calculate the number of memory chips needed to design 8K byte memory if the available chip size is 1024x1, and develop the memory map with illustrations in diagrams.

H. Lesson 8: Instruction Set

1. Describe the operations carried out by the microprocessor upon execution of the following instructions
    - ✓ ADI 96H
    - ✓ MOV D, C
    - ✓ CMA
    - ✓ JPE 2002h
    - ✓ POP
2. State and explain the five groups under which to classify the instructions available in the 8085 instruction set, giving examples for each group
3.

I. Lesson 9: Simple Assembly Language Programs

1. Write an Assembly Language Program (ALP) to find the largest number from the data set of three numbers (e.g. 98, 75, and 99). Include all the components of an ALP in your code
2. A set of 10 readings is stored in a memory starting at 8050H, write an ALP to sort the readings in ascending order. Include all the sections of an ALP
3. Write an ALP to multiply two unsigned numbers stored in memory locations 8050H and 8051H using repeated addition method. Provide all the sections of an ALP.

J. Lesson 10: I/O Interfacing

1. State two methods of decoding, as applied in I/O interfacing and explain their differences using diagrams to illustrate each technique
2. Discuss the difference between I/O mapped interfacing and Memory Mapped interfacing. Use diagrams to illustrate your concepts considering a 8085 microprocessor context for the various buses

3. Model a circuit diagram to illustrate the generation of IOW, IOR, MEMW and MEMR signals from the IO/M, RD and WR control signals of a 8085 microprocessor, using NANDs gates

K. Lesson 11: Instructions Data Flow Timing Diagrams

1. Define the following elements with respect to data flow timing diagrams for different instructions.
   - ✓ T-state
   - ✓ Instruction Cycle
   - ✓ Machine Cycle
2. Develop the data flow timing diagram for the following instructions
   - ✓ MOV C, A
   - ✓ Out 8-bit
   - ✓ SUBB
   - ✓ ORI 8-bit
   - ✓ PUSH
3. Outline and explain the sequence of events/steps that the processor will go through when executing each of the instructions listed in question 2 above.

L. Lesson 12: Timing (timers) and Counting (counters)

1. Compute the delay time achieved by a microprocessor when executing the following lines of code:

```
        MVI B, 89H
LOOP2:  MVI C, FFH
LOOP1:  DCR C
        JNZ LOOP1
        DCR B
        JNZ LOOP2
```

2. Explain the procedure followed in designing a time delay in a program, use a simple flow chart to illustrate your concept
3. State and explain at least three applications where counting and timing operations are applied in microprocessor/ microcontroller systems

M. Lesson 13: Interrupts

1. Considering the five interrupts available in the 8085 microprocessor, use a diagram to illustrate and explain how resetting, masking, and enabling of the interrupts is achieved
2. Describe the use of the SIM and RIM instructions in carrying out operations in the SIM Register and RIM register
3. Assuming the microprocessor is completing an RST 7.5 interrupt request, write an ALP to check to see whether RST 6.5 is pending. If it is pending, enable RST 6.5 without affecting any other interrupts; otherwise return to the main program