SAM D21 Family Silicon Errata and Data Sheet Clarification

SAM D21 Family

The SAM D21 family of devices that you have received conform functionally to the current Device Data Sheet (DS40001882D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1.

The errata described in this document will be addressed in future revisions of the SAM D21 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. SAM D21 Family Silicon Device Identification

Part Number	Device Identification (DID[31:0])	Revision (DID.REVISION[3:0])						
		A	B	C	D	E	F	G
ATSAMD21J18A	0x10011x00	0x0	0x1	0x2	0x3	N/A	N/A	N/A
ATSAMD21J17A	0x10011x01							
ATSAMD21J16A	0x10011x02							
ATSAMD21J15A	0x10011x03							
ATSAMD21G18A	0x10011x05							
ATSAMD21G18AU	0x10011x0F							
ATSAMD21G17A	0x10011x06							
ATSAMD21G17AU	0x10011x10							
ATSAMD21G16A	0x10011x07							
ATSAMD21G15A	0x10011x08							
ATSAMD21E18A	0x10011x0A							
ATSAMD21E17A	0x10011x0B							
ATSAMD21E16A	0x10011x0C							
ATSAMD21E15A	0x10011x0D							

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Part Number	Device Identification (DID[31:0])	Revision (DID.REVISION[3:0])						
		A	B	C	D	E	F	G
ATSAMD21J16B	0x10011x20	N/A	N/A	N/A	N/A	0x4	0x5	N/A
ATSAMD21J15B	0x10011x21							
ATSAMD21G16B	0x10011x23							
ATSAMD21G15B	0x10011x24							
ATSAMD21E16B	0x10011x26							
ATSAMD21E16BU	0x10011x55							
ATSAMD21E15B	0x10011x27	N/A	N/A	N/A	N/A	0x4	0x5	N/A
ATSAMD21E15BU	0x10011x56							
ATSAMD21G16L	0x10011x57							
ATSAMD21E16L	0x10011x3E							
ATSAMD21E15L	0x10011x3F							
ATSAMD21E16CU	0x10011x62	N/A	N/A	N/A	N/A	N/A	0x5	N/A
ATSAMD21E15CU	0x10011x63							
ATSAMD21E17D	0x10011x94	N/A	N/A	N/A	N/A	N/A	N/A	0x6
ATSAMD21E17DU	0x10011x95							
ATSAMD21E17L	0x10011x97							
ATSAMD21G17D	0x10011x93							
ATSAMD21G17L	0x10011x96							
ATSAMD21J17D	0x10011x92							

Note: Refer to the “Device Service Unit” chapter in the current Device Data Sheet (DS40001882D) for detailed information on Device Identification and Revision IDs for your specific device.

1 Silicon Errata Summary

Table 2. Errata Summary

Module	Feature	Item Number	Issue Summary	Affected Revisions						
				A	B	C	D	E	F	G
XOSC32K	Automatic Gain Control	1.1.1	The automatic amplitude control of the XOSC32K does not work.	X	X	X	X	X	X	X
XOSC32K	External Reset	1.1.2	If the external XOSC32K fails, the external reset will not reset the GCLKs sourced by the XOSC32K.	X	X	X	X	X	X	X
DFLL48M	Write Access to DFLL Register	1.2.1	The DFLL clock must be requested before being configured.	X	X	X	X	X	X	X
DFLL48M	False Out of Bound Interrupt	1.2.2	If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated.	X	X	X	X	X	X	X
DFLL48M	DFLL Status Bits (PCLKSR Register)	1.2.3	The DFLL status bits in the PCLKSR register during the USB Clock Recovery mode can be incorrect after a USB suspend state.	X	X	X	X	X	X	X
FDPLL	Lock Flag May Clear Randomly	1.3.1	The lock flag (DPLLSTATUS.LOCK) may clear randomly.	X						
FDPLL	FDPLL96M Operation Below 0°C Temperature	1.3.2	96 MHz Fractional Digital Phased Locked Loop (FDPLL96M) operation above 64 MHz is not functional below 0°C.	X	X	X	X			
FDPLL	Lock Time-out Values	1.3.3	The FDPLL lock time-out values are different from the parameters in the data sheet.	X						

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Module	Feature	Item Number	Issue Summary	Affected Revisions						
				A	B	C	D	E	F	G
FDPLL	DPLLRATIO Register FDPLL Ratio Value	1.3.4	When FDPLL ratio value in the DPLLRATIO register is changed on the fly, STATUS.DPLLLDRTO will not be set even though the ratio is updated.	X	X	X	X	X	X	X
ADC	Linearity Error in Single-Shot Mode	1.4.1	In Single-Shot mode and at +125°C, ADC conversions have linearity errors.	X	X	X	X			
DEVICE	APB Clock	1.5.1	If APB clock is stopped and the GCLK is running, APB read access to read-synchronized registers will freeze the system.	X	X	X	X	X	X	X
DEVICE	VDDIN POR Threshold	1.5.2	When VDDIN is lower than the POR threshold during power rise or fall, an internal pull-up resistor is enabled on pins with PTC functionality.	X	X	X				
DEVICE	Digital Pin Output in Stand-by Mode	1.5.3	Digital pin outputs from Timer/Counters, AC, GCLK, and SERCOM do not change the value during Stand-by Sleep mode.	X	X					
DEVICE	NVM User Row Mapping Value for WDT	1.5.4	The WDT Window bitfield default value on silicon is not as specified in the NVM User Row Mapping table in the current data sheet.			X	X			
DEVICE	SYSTICK Calibration Value	1.5.5	The SYSTICK calibration value specified in the data sheet is incorrect.	X	X	X	X	X	X	
DEVICE	High Leakage Current on VDDIO	1.5.6	When external reset is active it causes a high leakage current on VDDIO.	X	X	X	X	X		
DAC	EMPTY Flag is Set When Leaving Stand-by Mode	1.6.1	DAC.INTFLAG.EMPTY will be set after exiting Sleep mode.	X	X	X	X	X	X	X
DMAC	Consecutive Write Instructions to CRCDATAIN	1.7.1	If data is written to CRCDATAIN in two consecutive instructions, the CRC computation may be incorrect.	X	X	X	X	X	X	
DMAC	Linked Descriptors	1.7.2	When at least one channel using linked descriptors is already active, enabling another DMA channel can result in a channel Fetch Error or an incorrect descriptor fetch.	X	X	X	X	X	X	
DSU	Debugger and DSU Cold-plugging Procedure	1.8.1	If a debugger has issued a DSU Cold-Plugging procedure and then released the CPU from the resulting CPU Reset Extension, the CPU will be held in CPU Reset Extension after any upcoming reset event.	X	X	X	X			
DSU	Pause-on-Error is Not Functional	1.8.2	The MBIST Pause-on-Error feature is not functional.	X	X	X	X	X	X	
DSU	CRC32 Computation Failure	1.8.3	The DSU CRC32 computation is not functional on RAM.	X	X	X	X			
EIC	Interrupts	1.9.1	When the EIC is configured to generate an interrupt on a low level or rising edge or both edges with the filter enabled, a spurious flag may appear.	X	X	X	X	X	X	
I^2S	Transmit Serializer	1.10.1	In LSBIT mode, the I^2S RX serializer only works when the slot size is 32 bits.	X	X	X	X	X	X	X
I^2S	I^2S is Not Functional	1.10.2	The I^2S is not functional.	X						
I^2S	Software Reset	1.10.3	The software reset, SWRST, does not propagate inside the I2S module.		X					
I^2S	Slave Mode	1.10.4	The I^2S is not functional in Slave mode.		X					
I^2S	CPU Clock/I2S Clock Ratio	1.10.5	Depending on the CPU clock/I^2S clock ratio, the SYNCBUSY.CKEN0 flag is occasionally stuck.		X					
I^2S	PDM2 Mode	1.10.6	The PDM2 mode does not function.		X					
I^2S	Rx Serializer	1.10.7	The Rx serializer in the RIGHT Data Slot Formatting Adjust mode does not function when the slot size is not 32 bits.		X	X	X			
I^2S	Slave Mode (CTRLB Register)	1.10.8	In I^2C Slave mode, writing the CTRLB register when in the AMATCH or DRDY interrupt service routines can cause the state machine to reset.	X	X	X	X	X		
NVMCTRL	CRC32 is Not Executed	1.11.1	When the device is secured and the EEPROM emulation area configured to none, the CRC32 is not executed on the entire Flash area	X	X	X	X			
NVMCTRL	Spurious Writes	1.11.2	The default value of MANW in NVM.CTRLB is '0', which can lead to spurious writes to the NVM.	X	X	X	X	X	X	X
NVMCTRL	NVMCTRL.INTFLAG.READY	1.11.3	The NVMCTRL.INTFLAG.READY bit is not updated after a `RWWEEER` command and will keep holding a '1' value.					X		
PTC	WCOMP Interrupt Flag	1.12.1	The WCOMP interrupt flag is not stable.	X	X	X	X			

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Module	Feature	Item Number	Issue Summary	Affected Revisions						
				A	B	C	D	E	F	G
PORT - I/O Pin Controller	PA24 and PA25 Inputs	1.13.1	PA24 and PA25 cannot be used as an input when configured as GPIO with continuous sampling.	X	X	X	X			
PORT - I/O Pin Controller	PA07 Status During Internal Start-up	1.13.2	While the internal start-up is not completed, the PA07 pin is driven low by the device.	X	X	X	X			
PORT - I/O Pin Controller	PA24 and PA25 Pull-up/Pull-down Configuration	1.13.3	On PA24 and PA25 pins, the pull-up and pull-down configuration is not disabled automatically when alternative pin function is enabled with the exception for USB.	X	X	X	X	X	X	X
PORT - I/O Pin Controller	PA24 and PA25 Pull-down Functionality	1.13.4	Pull-down functionality is not available on GPIO pins, PA24 and PA25.	X	X	X	X	X		
PORT - I/O Pin Controller	Write Protect	1.13.5	Non-debugger IOBUS writes to PAC Write-protected registers are not prevented when the PORT is PAC Write-protected.	X	X	X	X	X	X	X
PM	Debug Logic and Watchdog Reset	1.14.1	In Debug mode, if a Watchdog Reset occurs, the debug session is lost.	X	X	X	X			
PM	Power-down Modes and Wake-up From Sleep	1.14.2	In Standby, Idle1, and Idle2 Sleep modes, the device may not wake from sleep.	X	X	X				
SERCOM	I^2C Slave SCL Low Extend Time-out	1.15.1	The I^2C Slave SCL low extend time-out and Master SCL low extend time-out cannot be used if SCL low time-out is disabled.	X	X	X	X			
SERCOM	I2C Transaction in Debug Mode	1.15.2	In I2C master mode, an ongoing transaction is stopped when the current byte transaction is completed and the corresponding interrupt is triggered if enabled.	X	X	X	X			
SERCOM	SPI with Slave Select Low Detection	1.15.3	If the SERCOM is enabled in SPI mode with SSL detection enabled and CTRLB.RXEN =1, an erroneous slave select low interrupt can be generated.	X	X	X	X	X		
SERCOM	USART in Auto-baud Mode	1.15.4	In USART Auto-baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.	X	X	X	X	X	X	
SERCOM	NACK and Repeated Start in I^2C Master Mode	1.15.5	For High-Speed Master Read operations, sending a NACK forces a STOP to be issued making repeated start not possible in that mode.	X	X	X	X	X	X	X
SERCOM	SERCOM-USART: Collision Detection	1.15.6	In USART operating mode with Collision Detection enabled, the SERCOM will not abort the current transfer as expected if a collision is detected.	X	X	X	X	X	X	X
SERCOM	SERCOM-USART: USART in Debug Mode	1.15.7	In USART operating mode, if DBGCTRL.DBGSTOP=1, data transmission is not halted after entering Debug mode.	X	X	X	X	X	X	X
SERCOM	SERCOM-I^2C: Slave Mode with DMA	1.15.8	In I^2C Slave Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register.	X	X	X	X	X	X	X
SERCOM	SERCOM-I^2C: I^2C Mode in 10-bit Address	1.15.9	10-bit addressing in I^2C Slave mode is not functional.	X	X	X	X	X	X	X
SERCOM	SERCOM-SPI: Data Preload	1.15.10	In SPI Slave mode and with Slave Data Preload Enabled, the first data sent from the slave will be a dummy byte.	X	X	X	X	X	X	X
SERCOM	CLKHOLD Bit Status in I^2C	1.15.11	STATUS.CLKHOLD bit can be written whereas it is a read-only status bit in both Master and Slave modes.	X	X	X	X	X	X	X
SERCOM	Quick Command I^2C	1.15.12	When Quick command is enabled (CTRLB.QCEN=1), the software can issue a repeated Start by either writing CTRLB.CMD or ADDR.ADDR bitfields. If in these conditions, SCL Stretch Mode is CTRLA.SCLSM=1, a bus error will be generated.	X	X	X	X	X	X	X
SERCOM	Repeated Start I^2C	1.15.13	For High-Speed Master Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start making repeated start not possible in that mode.	X	X	X	X	X	X	X
SERCOM	Slave Mode I^2C	1.15.14	In Slave mode, BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR STATUS register bits are not automatically cleared when INTFLAG.AMATCH is cleared.	X	X	X	X	X	X	X
TCC	WAVE/WAVEB Registers Hardware Exception	1.16.1	When the Peripheral Access Controller (PAC) protection is enabled, writing to the WAVE or WAVEB registers will not cause a hardware exception.	X	X	X	X			

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Module	Feature	Item Number	Issue Summary	Affected Revisions						
				A	B	C	D	E	F	G
TCC	Interrupts and Wake-up From Stand-by Mode	1.16.2	The TCC interrupts, FAULT1, FAULT0, FAULTB, FAULTA, DFS, ERR, and CNT, cannot wake the device from Stand-by mode.	X						
TCC	Extra Count Cycle	1.16.3	If an input event triggered STOP action is performed simultaneously as the counter overflows, the first pulse width of the subsequent counter start can be altered with one prescaled clock cycle.	X	X	X	X			
TCC	OVF Flag and DMA	1.16.4	If the OVF flag in the INTFLAG register is already set when enabling the DMA, this will trigger an immediate DMA transfer and overwrite the current buffered value in the TCC register.	X						
TCC	MCx Flag and DMA	1.16.5	If the MCx flag in the INTFLAG register is set when enabling the DMA, this will trigger an immediate DMA transfer and overwrite the current buffered value in the TCC register.	X	X	X	X			
TCC	Two-ramp Mode	1.16.6	In Two-ramp mode, two events will be generated per cycle, one on each ramp's end.	X	X	X	X			
TCC	SYNCBUSY Bit in Stand-by Mode	1.16.7	When waking up from the Stand-by Power Save mode, the SYNCBUSY.CTRLB, SYNCBUSY.STATUS,SYNCBUSY.COUNT, SYNCBUSY.PATT, SYNCBUSY.WAVE, SYNCBUSY.PER and SYNCBUSY.CCx bits may be locked to '1'.	X	X	X	X			
TCC	Retrigger in Dual Slope Mode	1.16.8	In Dual-Slope mode a retrigger event does not clear the TCC counter.	X	X	X	X			
TCC	CTRLA.RUNDSTDBY Enable Protection	1.16.9	When the RUNSTDBY bit is written after the TCC is enabled, the respective TCC APB bus is stalled and the RUNDSTBY bit in the TCC CTRLA register is not enabled-protected.	X	X	X	X			
TCC	Fault Filtering of Inverted Fault	1.16.10	TCC fault filtering on inverted fault is not functional.	X	X	X	X			
TCC	Recoverable Fault and Blanking Operation	1.16.11	When blanking is enabled, a recoverable fault that occurs during the first increment of a rising TCC is not blanked.	X	X	X	X			
TCC	RAMP 2 Mode	1.16.12	In RAMP 2 mode with Fault keep, qualified and restart, and if a fault occurred at the end of the period during the qualified state, the switch to the next ramp can have two restarts.	X	X	X	X	X		
TCC	CAPTMARK is Not Functional	1.16.13	FCTRLX.CAPTURE[CAPTMARK] does not function as described in the data sheet.					X	X	
TCC	Capture Using PWP/PPW Mode	1.16.14	When a capture is done using PWP or PPW mode, CC0 and CC1 are always fill with the period. It is not possible to get the pulse width.					X		
TCC	Advance Capture Mode	1.16.15	Advance capture mode does not work.	X	X	X	X	X	X	
TCC	MAX Capture Mode	1.16.16	In Capture mode while using MAX Capture mode, with the Timer set in up counting mode, if an input event occurred within two cycles before TOP, the value captured is '0' instead of TOP.	X	X	X	X	X	X	
TCC	Dithering Mode	1.16.17	Using TCC in Dithering mode with external retrigger events can lead to an unexpected stretch of right-aligned pulses, or a shrink of left-aligned pulses.	X	X	X	X	X	X	
TCC	TCC0/WO[6] on PA16 and TCC0/WO[7] on PA17	1.16.18	TCC0/WO[6] on PA16 and TCC0/WO[7] on PA17 are not available.	X						
TCC	Interrupt Flags	1.16.19	The TCC interrupt flags are not always properly set when using asynchronous TCC features.					X		
TCC	PATTB	1.16.20	The PATTB register write will not update the PATT register on an update condition.					X	X	X
TCC	PERBUF	1.16.21	In downcounting mode, the Lock Update bit (CTRLB.LUPD) does not protect against a PER register update from the PERBUF register.	X	X	X	X	X	X	X
TCC	TCC with EVSYS in SYNC/RESYNC Mode	1.16.22	TCC Peripheral is not compatible with an EVSYS channel in SYNC or RESYNC Mode.	X	X	X	X	X	X	X
TCC	Prescale	1.16.23	A DMA transfer to the TCC CC register may not initiate when using the TCC MCx as the trigger source (CTRLB.TRIGSRC) and the TCC Prescale (CTRLA.PRESCALE) value is set to 64/256/1024.					X	X	X

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Module	Feature	Item Number	Issue Summary	Affected Revisions						
				A	B	C	D	E	F	G
TC	Spurious TC Overflow	1.17.1	Spurious TC overflow and Match/Capture events may occur.	X	X	X	X			
TC	TC with EVSYS in SYNC/RESYNC Mode	1.17.2	TC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode.	X	X	X	X	X	X	X
USB	FLENC Register	1.18.1	The FLENC register negative sign management is not correct.	X						
Voltage Regulator	Low-Power Mode Above +85°C	1.19.1	The voltage regulator in Low-Power mode is not functional at temperatures above +85°C.	X	X	X	X			
SYSCTRL	XOSC	1.20.1	The XOSC can prevent entry into Stand-by mode regardless of XOSC.RUNSTDBY value.					X	X	X
SYSCTRL	BOD33	1.20.2	The BOD33 interrupt may not be generated second time if VDDANA does not increase above the user-defined threshold (BOD.LEVEL[5:0]) while in Active mode.			X	X	X	X	X

Table of Contents

1. Errata Issues

The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

1.1 32.768 kHz Crystal Oscillator (XOSC32K)

1.1.1 Automatic Gain Control

The automatic amplitude control of the XOSC32K does not work.

Workaround
Use the XOSC32K with Automatic Amplitude control disabled (XOSC32K.AAMPEN = 0).

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.1.2 External Reset

If the external XOSC32K fails, neither the external pin RST, nor the GCLK software reset can reset the GCLK generators using XOSC32K as the source clock.

Workaround
Do a power cycle to reset the GCLK generators after an external XOSC32K failure.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.2 48 MHz Digital Frequency-Locked Loop (DFLL48M)

1.2.1 Write Access to DFLL Register

The DFLL clock must be requested before being configured; otherwise, a write access to a DFLL register can freeze the device.

Workaround
Write a '0' to the DFLL ONDEMAND bit in the DFLLCTRL register before configuring the DFLL module.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.2.2 False Out of Bound Interrupt

If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. These interrupts will be generated even if the final calibration values at DFLL48M lock are not at maximum or minimum, and therefore, may be false out of bounds interrupts.

Workaround

Enable the DFLL Out Of Bounds (DFLLOOB) interrupt when configuring the DFLL in closed loop mode. In the DFLLOOB ISR verify the COARSE and FINE calibration bits and process as needed.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.2.3 DFLL Status Bits (PCLKSR Register)

The DFLL status bits in the PCLKSR register during the USB Clock Recovery mode can be incorrect after a USB suspend state.

Workaround

Do not monitor the DFLL status bits in the PCLKSR register during the USB Clock Recovery mode.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.3 96 MHz Fractional Digital Phase-Locked Loop (FDPLL)

1.3.1 Lock Flag May Clear Randomly

The lock flag (DPLLSTATUS.LOCK) may clear randomly. When the lock flag randomly clears, DPLLLCKR and DPLLLCKF interrupts will also trigger, and the DPLL output is masked.

Workaround

Set DPLLCTRLB.LBYPASS to '1' to disable masking of the DPLL output by the lock status.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X							

1.3.2 FDPLL96M Operation Below 0°C Temperature

96 MHz Fractional Digital Phased Locked Loop (FDPLL96M) operation above 64 MHz is not functional below 0°C.

Workaround

None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.3.3 Lock Time-out Values

The FDPLL lock time-out values are different from the parameters in the data sheet.

Workaround

The time-out values are:

- DPLLCTRLB.LTIME[2:0] = 4 : 10 ms
- DPLLCTRLB.LTIME[2:0] = 5 : 10 ms
- DPLLCTRLB.LTIME[2:0] = 6 : 11 ms
- DPLLCTRLB.LTIME[2:0] = 7 : 11 ms

Affected Silicon Revisions

A	B	C	D	E	F	G	
X							

1.3.4 DPLLRATIO Register FDPLL Ratio Value

When FDPLL ratio value in the DPLLRATIO register is changed on the fly, STATUS.DPLLLDRTO will not be set even though the ratio is updated.

Workaround

Monitor the INTFLAG.DPLLLDRTO instead of STATUS.DPLLLDRTO to get the status for DPLLRATIO update.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.4 Analog-to-Digital Controller (ADC)

1.4.1 Linearity Error in Single-shot Mode

In Single-shot mode and at +125°C, ADC conversions have linearity errors.

Workarounds

1. At +125°C, do not use the ADC in Single-shot mode. Instead, use the ADC in Free-running mode only.
2. At +125°C, use the ADC in Single-shot mode only with VDDANA > 3V.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.5 Device

1.5.1 APB Clock

If APB clock is stopped and the GCLK is running, APB read access to read-synchronized registers will freeze the system. The CPU and the DAP AHB-AP are stalled, and as a consequence, debug operation is impossible.

Workaround

Do not make read access to read-synchronized registers when the APB clock is stopped and GCLK is running. To recover from this condition, power cycle the device or reset the device using the $\overline{\text{RESET}}$ pin.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.5.2 VDDIN POR Threshold

When VDDIN is lower than the POR threshold during power rise or fall, an internal pull-up resistor is enabled on pins with PTC functionality (see *PORT Function Multiplexing* in the current data sheet). This behavior will be present even if PTC functionality is not enabled on the pin. The POR level is defined in the *Power-On Reset (POR) Characteristics* chapter of the current data sheet.

Workaround

Use a pin without PTC functionality if the pull-up could damage your application during power up.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X					

1.5.3 Digital Pin Output in Stand-by Mode

Digital pin outputs from Timer/Counters, Analog Comparator (AC), Generic Clock Controller (GCLK), and SERCOM (I^2C and SPI) do not change the value during Stand-by Sleep mode.

Workaround

Set the voltage regulator in Normal mode before entering Stand-by Sleep mode to keep digital pin output enabled. This is done by setting the RUNSTDBY bit in the VREG register.

Affected Silicon Revisions

A	B	C	D	E	F	G	

X	X						

1.5.4 NVM User Row Mapping Value for WDT

The WDT Window bitfield default value on silicon is not as specified in the *NVM User Row Mapping* table in the current data sheet. The data sheet defines the default value as 0x5, while it on silicon this value is 0xB.

Workaround

None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
		X	X				

1.5.5 SYSTICK Calibration Value

The SYSTICK calibration value specified in the data sheet is incorrect.

Workaround

The correct SYSTICK calibration value is 0x40000000. This value should not be used to initialize the Systick RELOAD value register, which should be initialized instead with a value depending on the main clock frequency and on the tick period required by the application. For a detailed description of the SYSTICK module, refer to the official ARM® Cortex®-M0+ documentation.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X		

1.5.6 High Leakage Current on VDDIO

When external reset is active it causes a high leakage current on VDDIO.

Workaround

Minimize the time external reset is active.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X			

1.6 Digital-to-Analog Controller (DAC)

1.6.1 EMPTY Flag is Set When Leaving Stand-by Mode

When DAC.CTRLA.RUNSTDBY = 0 and DATABUF is written (not empty), and if the device goes to Stand-by Sleep mode before a Start Conversion event, DAC.INTFLAG.EMPTY will be set after exiting Sleep mode.

Workaround
After waking from Stand-by mode, ignore and clear the flag DAC.INTFLAG.EMPTY.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.7 Direct Memory Access Controller (DMAC)

1.7.1 Consecutive Write Instructions to CRCDATAIN

If data is written to CRCDATAIN in two consecutive instructions, the CRC computation may be incorrect.

Workaround
Add a `NOP` instruction between each write to the CRCDATAIN register.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X		

1.7.2 Linked Descriptors

When at least one channel using linked descriptors is already active, enabling another DMA channel (with or without linked descriptors) can result in a channel Fetch Error (FERR) or an incorrect descriptor fetch.

This occurs if the channel number of the channel being enabled is lower than the channel already active.

Workaround
When enabling a DMA channel while other channels using linked descriptors are already active, the channel number of the new channel enabled must be greater than the other channel numbers.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X		

1.8 Device Service Unit (DSU)

1.8.1 Debugger and DSU Cold-plugging Procedure

If a debugger has issued a DSU Cold-Plugging procedure and then released the CPU from the resulting CPU Reset Extension, the CPU will be held in CPU Reset Extension after any upcoming reset event.

Workaround
The CPU must be released from the CPU Reset Extension either by writing a one in the DSU STATUSA.CRSTEXT register or by applying an external reset with SWCLK high or by power cycling the device.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.8.2 Pause-on-Error is Not Functional

The MBIST Pause-on-Error feature is not functional.

Workaround
None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X		

1.8.3 CRC32 Computation Failure

The DSU CRC32 computation is not functional on RAM.

Workaround
Before using the CRC32 on RAM, execute the following code:

```
*(volatile unsigned int* 0x41007058) &= ~0x30000UL;
```

After using the CRC32, execute the following code:

```
*(volatile unsigned int* 0x41007058) |= 0x20000UL;
```

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.9 External Interrupt Controller (EIC)

1.9.1 Interrupts

When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag may appear for the dedicated pin on the INTFLAG.EXTINT[x] register as soon as the EIC is enabled using the CTRLA ENABLE bit.

Workaround
Clear the INTFLAG bit once the EIC is enabled and before enabling the interrupts.

Affected Silicon Revisions

A	B	C	D	E	F	G	

X	X	X	X	X	X		

1.10 Integrated Inter-IC Sound (I^2S)

1.10.1 Transmit Serializer

In LSBIT mode (i.e., SERCTRL.BITREV is set), the I^2S RX serializer only works when the slot size is 32 bits.

Workaround
In SERCTRL.SERMODE RX, SERCTRL.BITREV LSBIT must be used with CLKCTRL.SLOTSIZE 32.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.10.2 I^2S is Not Functional

The I^2S is not functional.

Workaround
None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X							

1.10.3 Software Reset

The software reset, SWRST, does not propagate inside the I^2S module. As a consequence, Slave mode may not be reconfigured correctly and may result in unexpected behavior of the SYNCBUSY register.

Workaround
None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
	X						

1.10.4 Module is Not Functional in Slave Mode

The I^2S is not functional in Slave mode (i.e., when (FSSEL = 1, SCKSEL = 1).

Workaround
None. FSSEL and SCKSEL must be '0'.

Affected Silicon Revisions

A	B	C	D	E	F	G	
	X						

1.10.5 CPU Clock/I²S Clock Ratio

Depending on the CPU clock/I²S clock ratio, the SYNCBUSY.CKEN0 flag is occasionally stuck at '1' when starting a new audio stream with CTRLA.SWRST = 1, CTRLA.ENABLE = 1, and CTRLA.CKEN0 = 1.

Workaround

Disable the IP by writing a '0' to CTRLA.ENABLE before resetting it (CTRLA.SWRST = 1).

Affected Silicon Revisions

A	B	C	D	E	F	G	
	X						

1.10.6 PDM2 Mode is Not Functional

The PDM2 mode (i.e., when using two PDM microphones) does not function.

Workaround

None. Only one PDM microphone can be connected. Therefore, the I²S controller should be configured in normal Receive mode with one slot.

Affected Silicon Revisions

A	B	C	D	E	F	G	
	X						

1.10.7 Rx Serializer

The Rx serializer in the RIGHT Data Slot Formatting Adjust mode (SERCTRL.SLOTADJ clear) does not function when the slot size is not 32 bits.

Workaround

In SERCTRL.SERMODE RX, SERCTRL.SLOTADJ RIGHT must be used with CLKCTRL.SLOTSIZE 32.

Affected Silicon Revisions

A	B	C	D	E	F	G	
	X	X	X				

1.10.8 Slave Mode (CTRLB Register)

In I²C Slave mode, writing the CTRLB register when in the AMATCH or DRDY interrupt service routines can cause the state machine to reset.

Workaround
Write CTRLB.ACKACT to '0' using the following sequence:

```
// If higher priority interrupts exist, then disable so that the
// following two writes are atomic.
SERCOM - STATUS.reg = 0;
SERCOM - CTRLB.reg = 0;
// Re-enable interrupts if applicable.
```

Write CTRLB.ACKACT to '1' using the following sequence:

```
SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;
```

Otherwise, only write to CTRLB in the AMATCH or DRDY interrupts if it is to close out a transaction.

When not closing a transaction, clear the AMATCH interrupt by writing a '1' to its bit position instead of using CTRLB.CMD. The DRDY interrupt is automatically cleared by reading/writing to the DATA register in Smart mode. If not in Smart mode, DRDY should be cleared by writing a '1' to its bit position.

Code Replacements Examples:

Current:

```
SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_ACKACT;
```

Change to:

```
 SERCOM - STATUS.reg = 0;
SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;
SERCOM - CTRLB.reg &= ~SERCOM_I2CS_CTRLB_ACKACT;
SERCOM - CTRLB.reg = 0;
/* ACK or NACK address */
SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_CMD(0x3);
// CMD=0x3 clears all interrupts, so to keep the result similar,
// CMD=0x3 clears all interrupts, so to keep the result similar,
// PREC is cleared if it was set.
if (SERCOM - INTFLAG.bit.PREC) SERCOM - INTFLAG.reg = SERCOM_I2CS_INTFLAG_PREC;
SERCOM - INTFLAG.reg = SERCOM_I2CS_INTFLAG_AMATCH;
```

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X			

1.11 Non-Volatile Memory Controller (NVMCTRL)

1.11.1 CRC32 is Not Executed on the Entire Flash Area

When the device is secured and the EEPROM emulation area configured to none, the CRC32 is not executed on the entire Flash area but up to the on-chip Flash size minus half a row.

Workaround
When using CRC32 on a protected device with the EEPROM emulation area configured to none, compute the reference CRC32 value to the full chip Flash size minus a half row.

Affected Silicon Revisions

A	B	C	D	E	F	G	

X	X	X	X				

1.11.2 Spurious Writes

The default value of MANW in NVM.CTRLB is '0', which can lead to spurious writes to the NVM if a data write is done through a pointer with a wrong address corresponding to the NVM area.

Workaround

Set MANW in the NVM.CTRLB register to '1' at start-up

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.11.3 NVMCTRL.INTFLAD.READY Bit

The NVMCTRL.INTFLAG.READY bit is not updated after a `RWWEEER` command and will keep holding a '1' value. If a new `RWWEEER` command is issued it can be accepted even if the previous `RWWEEER` command is ongoing. The ongoing NVM `RWWEER` command will be aborted, and the content of the row under erase will be unpredictable.

Workaround

Perform a dummy write to the page buffer right before issuing a `RWWEEER` command. This will cause the INTFLAG.READY bit to behave as expected.

Affected Silicon Revisions

A	B	C	D	E	F	G	
				X			

1.12 Peripheral Touch Controller (PTC)

1.12.1 WCOMP Interrupt Flag

The WCOMP interrupt flag is not stable. The WCOMP interrupt flag will not always be set as described in the data sheet.

Workaround

Do not use the WCOMP interrupt. Instead, use the WCOMP event.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.13 PORT - I/O Pin Controller

1.13.1 PA24 and PA25 Inputs

PA24 and PA25 cannot be used as an input when configured as GPIO with continuous sampling (cannot be read by PORT).

Workarounds

1. Use PA24 and PA25 for peripherals or only as output pins.
2. Configure PA31 to PA24 for on-demand sampling (CTRL[31:24] all zeroes) and access the IN register through the APB (not the IOBUS), to allow waiting for on-demand sampling.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.13.2 PA07 Status During Internal Start-up

While the internal start-up is not completed, the PA07 pin is driven low by the device. Then, as with all of the other pins, it is configured as a High Impedance pin.

Workaround

None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.13.3 PA24 and PA25 Pull-up/Pull-down Configuration

On PA24 and PA25 pins the pull-up and pull-down configuration is not disabled automatically when alternative pin function is enabled, with the exception for USB.

Workaround

For PA24 and PA25 pins, the GPIO pull-up and pull-down must be disabled before enabling alternative functions on them.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.13.4 PA24 and PA25 Pull-down Functionality

Pull-down functionality is not available on GPIO pins, PA24 and PA25

Workaround

None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X			

1.13.5 Write-Protect

The non-debugger IOBUS writes to the PAC Write-protected registers are not prevented when the PORT is PAC Write-protected.

Workaround

None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.14 Power Manager (PM)

1.14.1 Debug Logic and Watchdog Reset

In Debug mode, if a Watchdog Reset occurs, the debug session is lost.

Workaround

A new debug session must be restart after a Watchdog Reset.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.14.2 Power-down Modes and Wake-up From Sleep

In Standby, Idle1, and Idle2 Sleep modes, the device may not wake from sleep. An External Reset, Power on Reset, or Watchdog Reset will start the device again.

Workaround

The SLEEPPRM bits in the NVMCTRL.CTRLB register must be written to 3 (NVMCTRL - CTRLB.bit.SLEEPPRM = 3) to ensure correct operation of the device. The average power consumption of the device will increase with 20 µA compared to the values in the *Electrical Characteristics* chapter of the current data sheet.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X					

1.15 Serial Communication Interface (SERCOM)

1.15.1 I2C Slave SCL Low Extend Time-out

The I²C Slave SCL low extend time-out (CTRLA.SEXTTOEN) and Master SCL low extend time-out (CTRLA.MEXTTOEN) cannot be used if SCL low time-out (CTRLA.LOWTOUT) is disabled. When SCTRLA.LOWTOUT = 0, GCLK_SERCOM_SLOW is not requested.

Workaround

To use the Master or Slave SCL low extend time-outs, enable the SCL low time-out (CTRLA.LOWTOUT = 1).

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.15.2 I²C Transaction in Debug Mode

In I²C master mode, an ongoing transaction should be stalled immediately when DBGCTRL.DBGSTOP is set and the CPU enters Debug mode. Instead, it is stopped when the current byte transaction is completed and the corresponding interrupt is triggered if enabled.

Workaround

In I²C master mode, keep DBGCTRL.DBGSTOP = 0 when in Debug mode.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.15.3 SPI with Slave Select Low Detection

If the SERCOM is enabled in SPI mode with SSL detection enabled (CTRLB.SSDE) and CTRLB.RXEN = 1, an erroneous slave select low interrupt (INTFLAG.SSL) can be generated.

Workaround

Enable the SERCOM first with CTRLB.RXEN = 0. In a subsequent write, set CTRLB.RXEN = 1.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X			

1.15.4 USART in Auto-baud Mode

In USART Auto-baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.

Workaround

None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X		

1.15.5 NACK and Repeated Start in I²C Master Mode

For High-Speed Master Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued, making repeated start not possible in that mode.

Workaround

None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.15.6 SERCOM-USART: Collision Detection

In USART Operating mode with Collision Detection enabled (CTRLB.COLDEN=1), the SERCOM will not abort the current transfer as expected if a collision is detected, and if the SERCOM APB Clock is lower than the SERCOM Generic Clock.

Workaround

The SERCOM APB clock must always be higher than the SERCOM Generic Clock to support collision detection.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.15.7 SERCOM-USART: USART in Debug Mode

In USART operating mode, if DBGCTRL.DBGSTOP=1, data transmission is not halted after entering Debug mode.

Workaround

None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.15.8 SERCOM-I²C: Slave Mode with DMA

In I²C Slave Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register. Because a NACK was received, the transfer on the I²C bus will not occur causing the loss of this data.

Workaround

Configure the DMA transfer size to the number of data to be received by the I²C master. DMA cannot be used if the number of data to be received by the master is unknown.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.15.9 SERCOM-I²C: I²C Mode in 10-bit Address

10-bit addressing in I²C Slave mode is not functional.

Workaround

None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.15.10 SERCOM-SPI: Data Preload

In SPI Slave mode and with Slave Data Preload Enabled (CTRLB.PLOADEN=1), the first data sent from the slave will be a dummy byte if the master cannot keep the Slave Select (SS) line low until the end of transmission.

Workarounds

In SPI Slave mode, the Slave Select pin (SS) must be kept low by the master until the end of the transmission if the Slave Data Preload feature is used (CTRLB.PLOADEN=1).

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.15.11 CLKHOLD Bit Status in I²C

STATUS.CLKHOLD bit can be written whereas it is a read-only status bit in both Master and Slave modes.

Workarounds

Do not clear STATUS.CLKHOLD bit to preserve the current clock hold state.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.15.12 Quick Command I²C

When Quick command is enabled (CTRLB.QCEN=1), the software can issue a repeated Start by either writing CTRLB.CMD or ADDR.ADDR bit fields. If, in these conditions, SCL Stretch Mode is CTRLA.SCLSM=1, a bus error will be generated.

Workarounds

Use Quick Command mode (CTRLB.QCEN=1) only if SCL Stretch Mode is CTRLA.SCLSM=0.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.15.13 Repeated Start I²C

For High-Speed Master Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start, making repeated start is not possible in that mode.

Workarounds

None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.15.14 Slave Mode I²C

In Slave mode, the BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR STATUS register bits are not automatically cleared when INTFLAG.AMATCH is cleared.

Workarounds

PERBUFlear the STATUS register bits, such as BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR by writing these STATUS bits to 1, when INTFLAG.AMATCH is cleared.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.16 Timer/Counter for Control Applications (TCC)

1.16.1 WAVE/WAVEB Registers Hardware Exception

When the Peripheral Access Controller (PAC) protection is enabled, writing to the WAVE or WAVEB registers will not cause a hardware exception.

Workaround

None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.16.2 Interrupts and Wake-up From Stand-by Mode

The TCC interrupts, FAULT1, FAULT0, FAULTB, FAULTA, DFS, ERR, and CNT, cannot wake the device from Stand-by mode.

Workaround

Do not use the TCC interrupts, FAULT1, FAULT0, FAULTB, FAULTA, DFS, ERR, and CNT, to wake the device from Stand-by mode.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X							

1.16.3 Extra Count Cycle

If an input event triggered STOP action is performed at the same time as the counter overflows, the first pulse width of the subsequent counter start can be altered with one prescaled clock cycle.

Workaround

None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.16.4 OVF Flag and DMA

If the OVF flag in the INTFLAG register is already set when enabling the DMA, this will trigger an immediate DMA transfer and overwrite the current buffered value in the TCC register.

Workaround

None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X							

1.16.5 MCx Flag and DMA

If the MCx flag in the INTFLAG register is set when enabling the DMA, this will trigger an immediate DMA transfer and overwrite the current buffered value in the TCC register.

Workaround
None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.16.6 Two-ramp Mode

In Two-ramp mode, two events will be generated per cycle, one on each ramp's end. EVCTRL.CNTSEL.END cannot be used to identify the end of a double ramp cycle.

Workaround
None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.16.7 SYNCBUSY Bit in Stand-by Mode

When waking up from the Stand-by Power Save mode, the SYNCBUSY.CTRLB, SYNCBUSY.STATUS, SYNCBUSY.COUNT, SYNCBUSY.PATT, SYNCBUSY.WAVE, SYNCBUSY.PER and SYNCBUSY.CCx bits may be locked to '1'.

Workaround
After waking up from Stand-by Power Save mode, perform a software reset of the TCC if you are using the SYNCBUSY.CTRLB, SYNCBUSY.STATUS, SYNCBUSY.COUNT, SYNCBUSY.PATT, SYNCBUSY.WAVE, SYNCBUSY.PER or SYNCBUSY.CCx bits

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.16.8 Retrigger in Dual Slope Mode

In Dual Slope mode a retrigger event does not clear the TCC counter.

Workaround
None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.16.9 CTRLA.RUNDSTDBY Enable Protection

When the RUNSTDBY bit is written after the TCC is enabled, the respective TCC APB bus is stalled and the RUNDSTBY bit in the TCC CTRLA register is not enabled-protected.

Workaround
None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.16.10 Fault Filtering of Inverted Fault

TCC fault filtering on inverted fault is not functional.

Workaround
Use only non-inverted faults.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.16.11 Recoverable Fault and Blanking Operation

When blanking is enabled, a recoverable fault that occurs during the first increment of a rising TCC is not blanked.

Workaround
None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.16.12 RAMP 2 Mode

In RAMP 2 mode with Fault keep, qualified and restart, and if a fault occurred at the end of the period during the qualified state, the switch to the next ramp can have two restarts.

Workaround
Avoid faults few cycles before the end or the beginning of a ramp.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X			

1.16.13 CAPTMARK is Not Functional

FCTRLX.CAPTURE[CAPTMARK] does not function as described in the data sheet. CAPTMARK cannot be used to identify captured values triggered by fault inputs source A or B on the same channel.

Workaround

Use two different channels to timestamp FaultA and FaultB.

Affected Silicon Revisions

A	B	C	D	E	F	G	
				X	X		

1.16.14 Capture Using PWP/PPW Mode

When a capture is done using PWP or PPW mode, CC0 and CC1 are always fill with the period. It is not possible to get the pulse width.

Workaround

Use the PWP feature on TC instead of TCC

Affected Silicon Revisions

A	B	C	D	E	F	G	
				X			

1.16.15 Advance Capture Mode

Advance capture mode (CAPTMIN CAPTMAX LOCMIN LOCMAX DERIV0) doesn’t work if an upper channel is not in one of these mode. For example, when CC[0]=CAPTMIN, CC[1]=CAPTMAX, CC[2]=CAPTEN, and CC[3]=CAPTEN, CAPTMIN and CAPTMAX will not work.

Workaround

Basic capture mode must be set in lower channel and advance capture mode in upper channel.

For example, CC[0]=CAPTEN , CC[1]=CAPTEN , CC[2]=CAPTMIN, CC[3]=CAPTMAX

All capture will be done as expected.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X		

1.16.16 MAX Capture Mode

In Capture mode while using MAX Capture mode, with the Timer set in up counting mode, if an input event occurred within two cycles before TOP, the value captured is '0' instead of TOP.

Workarounds

1. If the event is controllable, the capture event should not occur when the counter is within two cycles before the TOP value.

2. Use the Timer in Down Counter mode and capture the MIN value instead of the MAX value.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X		

1.16.17 Dithering Mode

Using TCC in Dithering mode with external retrigger events can lead to an unexpected stretch of right-aligned pulses, or a shrink of left-aligned pulses.

Workaround

Do not use retrigger events/actions when the TCC is configured in Dithering mode.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X		

1.16.18 TCC0/WO[6] on PA16 and TCC0/WO[7] on PA17 Are Not Available

TCC0/WO[6] on PA16 and TCC0/WO[7] on PA17 are not available.

Workaround

None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X							

1.16.19 Interrupt Flags

The TCC interrupt flags INTFLAG.ERR, INTFLAG.DFS, INTFLAG.UFS, INTFLAG.CNT, INTFLAG.FAULTA,INTFLAG.FAULTB, INTFLAG.FAULT0, INTFLAG.FAULT1 are not always properly set when using asynchronous TCC features.

Workaround

Do not use these flags when using asynchronous TCC features.

Affected Silicon Revisions

A	B	C	D	E	F	G	
				X			

1.16.20 PATTB

The PATTB register write will not update the PATT register on an update condition.

Workaround
Write directly to the PATT register when an update is required.

Affected Silicon Revisions

A	B	C	D	E	F	G	
				X	X	X	

1.16.21 PERBUF
In down-counting mode, the Lock Update bit (CTRLB.LUPD) does not protect against a PER register update from the PERBUF register.

Workaround
None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.16.22 TCC with EVSYS in SYNC/RESYNC Mode
TCC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode.

Workaround
Use TCC with an EVSYS channel in ASYNC mode.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.16.23 Prescale
A DMA transfer to the TCC.CC register may not initiate when using the TCC MCx as the trigger source (CTRLB.TRIGSRC), and the TCC Prescale (CTRLA.PRESCALE) value is set to 64/256/1024.

Workaround
Use the TCC.CCB for DMA transfers, or the GCLK division register (GENDIV.DIV) to divide the TCC input clock to a range that is suitable to match the required 64/256/1024 prescale clock values. To ensure this does not have an impact on other modules in the system, the divided GCLK used to supply the TCC peripheral with its input clock should not source other peripheral modules.

Affected Silicon Revisions

A	B	C	D	E	F	G	
				X	X	X	

1.17 Timer/Counter (TC)

1.17.1 Spurious TC Overflow

Spurious TC overflow and Match/Capture events may occur.

Workaround

Do not use the TC overflow and Match/Capture events. Use the corresponding interrupts instead.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.17.2 TC with EVSYS in SYNC/RESYNC Mode

TC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode.

Workaround

Use TC with an EVSYS channel in ASYNC mode.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X	X	X	X	

1.18 Universal Serial Bus (USB)

1.18.1 FLENC Register

The FLENC register negative sign management is not correct.

Workaround

The following rule must be used for negative values:

- FLENC 0x8 (hex) is equal to '0' decimal.
- FLENC 0x9 to 0xF (hex) are equal to -1 to -7 decimal instead of -7 to -1.

Affected Silicon Revisions

A	B	C	D	E	F	G	
X							

1.19 Voltage Regulator

1.19.1 Low-Power Mode Above +85°C

The voltage regulator in Low-Power mode is not functional at temperatures above +85°C.

Workaround
Enable normal mode on the voltage regulator in Stand-by Sleep mode.

Example code:

```
// Set the voltage regulator in normal mode configuration in Stand-by Sleep mode
SYSCTRL->VREG.bit.RUNSTDBY = 1;
```

Affected Silicon Revisions

A	B	C	D	E	F	G	
X	X	X	X				

1.20 SYSCTRL

1.20.1 XOSC

The XOSC can prevent entry into Stand-by mode regardless of XOSC.RUNSTDBY value.

Workaround
Change the clock source for gclk0 to the internal RC OSC, and then disable the XOSC before entering Standby mode.

Affected Silicon Revisions

A	B	C	D	E	F	G	
				X	X	X	

1.20.2 BOD33

The BOD33 interrupt may only generate once if VDDANA does not increase above the user-defined threshold (BOD.LEVEL[5:0]) when in Active mode. If in Standby mode, when the BOD33 interrupt is generated, the device will have to be in Active mode while VDDANA increases above BOD.LEVEL to re-enable the BOD33 interrupt.

Workaround
None.

Affected Silicon Revisions

A	B	C	D	E	F	G	
		X	X	X	X	X	

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest revision of the device Data Sheet (DS40001882D). The corrected information is shown in **BOLD** type.

2.1 System Controller - XOSC (Chapter 17 of the Device Data Sheet)

The descriptions of the AMPGC and GAIN[2:0] bit fields in the SYSCTRL.XOSC register are incorrect. The corrected information is shown in **BOLD** type.

Bit 11 - AMPGC Automatic Amplitude Gain Control

The configuration of the oscillator gain is mandatory and should follow the maximum frequency gain recommendations.

Bits 10:8 – GAIN[2:0] Oscillator Gain

These bits select the gain for the oscillator. The listed maximum frequencies are recommendations, and might vary based on capacitive load and crystal characteristics.

2.2 Electrical Characteristics - Crystal Oscillator (XOSC) Characteristics (Chapter 37, 38, 39, and 40 of the Device Data Sheet)

The Electrical Characteristics section (Chapters 37 to 40) provides an equation for calculating the external load capacitance used for an external crystal oscillator. The equation as shown in “Crystal Oscillator Chacteristics” is in error. The corrected information is shown in **BOLD** type. The correct equation is as follows:

Load Capacitance Equation

$$C_{LOAD} = ([C_{XIN} + C_{LEXT}] * [C_{XOUT} + C_{LEXT}]) / ([C_{XIN} + C_{LEXT} + C_{LEXT} + C_{XOUT}]) + C_{STRAY}$$

Where:

C_{LOAD} = Crystal Mfg. C_{LOAD} specification

C_{XIN} = XOSC XIN pin data sheet specification

C_{XOUT} = XOSC XOUT pin data sheet specification

C_{LEXT} = Required external crystal load capacitor

C_{STRAY} (Osc PCB capacitance) = 1.5 pf per 12.5 mm (0.5 inches) (TRACE W = 0.175 mm, H = 36 µm, T = 113 µm)

2.3 Schematic Checklist - Crystal Oscillator (Chapter 42 of the Device Data Sheet)

The load capacitor values shown in figure 42-6 and table 42-5 should not be used. CLEXT should be calculated from the Load Capacitance Equation listed below. The corrected information is shown in **BOLD** type.

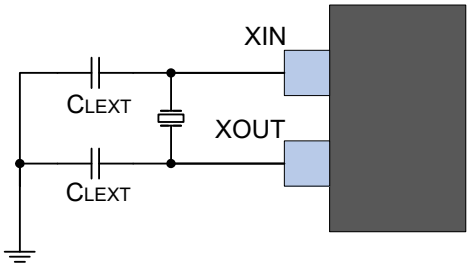

Table 2-1. Crystal Oscillator Checklist

Signal Name	Recommended Pin Connection	Description
XIN	Load capacitor C_{LEXT}(1)(2)	External crystal between 0.4 to 30 MHz
XOUT	Load capacitor C_{LEXT}(1)(2)	

Load Capacitance Equation

$C_{LOAD} = ([C_{XIN} + C_{LEXT}] * [C_{XOUT} + C_{LEXT}]) / ([C_{XIN} + C_{LEXT} + C_{LEXT} + C_{XOUT}]) + C_{STRAY}$

Where:

C_{LOAD} **= Crystal Mfg.** C_{LOAD} **specification**

C_{XIN} **= XOSC XIN pin data sheet specification**

C_{XOUT} **= XOSC XOUT pin data sheet specification**

C_{LEXT} **= Required external crystal load capacitor**

C_{STRAY} **(Osc PCB capacitance) = 1.5 pf per 12.5 mm (0.5 inches) (TRACE W = 0.175 mm, H = 36 µm, T = 113 µm)**

3. Appendix A: Revision History

Rev D Document (04/2019)
The following Data Sheet Clarifications were added:

- System Controller - XOSC
- Electrical Characteristics - Crystal Oscillator (XOSC) Characteristics
- Schematic Checklist - Crystal Oscillator

Rev C Document (11/2018)
The following errata is added:

- 1.16.23 Prescale

Rev B Document (9/2018)
The following Errata Issues were added:

- 1.13.5 Write-Protect
- 1.15.5 NACK and Repeated Start in I2C Master Mode
- 1.15.6 SERCOM-USART: Collision Detection
- 1.15.7 SERCOM-USART: USART in Debug Mode
- 1.15.8 SERCOM-I2C: Slave Mode with DMA
- 1.15.9 SERCOM-I2C: I2C Mode in 10-bit Address
- 1.15.10 SERCOM-SPI: Data Preload
- 1.15.11 CLKHOLD Bit Status in I2C
- 1.15.12 Quick Command I2C
- 1.15.13 Repeated Start I2C
- 1.15.14 Slave Mode I2C
- 1.16.20 PATTB
- 1.16.21 PERBUF
- 1.16.22 TCC with EVSYS in SYNC/RESYNC Mode
- 1.17.2 TC with EVSYS in SYNC/RESYNC Mode
- 1.20.1 XOSC
- 1.20.2 BOD33

Rev A Document (4/2018)
Initial release of this document.

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