

## **Part IV**

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### **Advanced Modeling, Analysis, and Control Techniques**



## Techniques of Design-Oriented Analysis: The Feedback Theorem

### 13.1 Introduction to Part IV

Part IV of this text develops analytical tools needed to understand and design larger power electronic systems. It builds on the basic modeling and analysis techniques developed in Part II to analyze and simulate complex feedback circuits, including those having input EMI filters, current-mode control, or digital control.

As introduced in Chap. 8, *Design-Oriented Analysis* (D-OA) is a collection of analytical tools that aid the analysis of complex circuits and systems, with the goal of deriving tractable equations that are useful for design. Part IV covers three more advanced techniques of D-OA that are based on linear superposition and the *null double injection* analysis technique. The goal of these techniques is the further development of analytical tools that aid in the design of complex analog systems, including development of additional approximation methods and of more powerful analytical methods.

The closed-loop switching regulator block diagram studied in Sect. 9.1 employs idealized blocks that do not explicitly represent input and output impedances or bidirectional signal flow. While this often is a useful approach, there are cases where interactions between circuit elements are not easily characterized as unidirectional blocks that do not significantly load each other. Middlebrook's *General Feedback Theorem* [106] is a general technique that allows determination of loop gains and other important transfer functions of a circuit, without need for identification of blocks. This technique can be viewed as a generalization of the loop gain measurement techniques described in Sect. 9.6, to perform analytical "thought experiments" to find the transfer functions obtained by null double injection in the feedback circuit.

The single-loop version of the feedback theorem is derived in Sect. 13.2, based on linear superposition and null double injection. Two common circuit examples are then examined. The effect of the bandwidth of a practical op amp on the behavior of a PD compensator circuit is determined in Sect. 13.3. The feedback theorem is employed to find the closed-loop transfer functions of a buck regulator in Sect. 13.4. This analysis is extended in Chap. 17 to examine the effect of an input EMI filter on a buck regulator, and in Chap. 18 to examine the effect of an EMI filter on a current-mode regulator system.

*Averaged switch modeling* is a subset of the subject of averaged converter modeling, and leads to results that are equivalent to the models developed in Chap. 8. This technique is par-

ticularly well suited to SPICE-based simulation of converters, and is developed in Chap. 14. Averaged switch modeling also exposes the fundamental *direct* and *indirect power* conversion mechanisms that are inherent in high-efficiency electronic power conversion circuits. Averaged switch modeling is extended to ac modeling of the discontinuous conduction mode in Chap. 15.

The *Extra Element Theorem* exposes how a known transfer function is changed by addition of a new network element; this theorem is introduced in Chap. 16. A classic application of the EET is the addition of an input EMI filter to a closed-loop switching regulator, and damping of this filter so that it does not degrade regulator performance and stability. Input filter analysis and design is covered in Chap. 17. The *n-Extra Element Theorem* (*n-EET*) is an extension of the EET to cover the simultaneous addition of multiple elements to a circuit. A useful application of the *n-EET* is the treatment of all reactive components as extra elements: a transfer function can be written as a normalized rational fraction with little or no algebra.

*Current-mode control* is a popular approach to control of switching converters, in which the peak transistor current replaces the duty cycle as the control variable that is commanded by the compensator output. This approach contains an inherent inner current feedback loop, which can improve control response but complicates the analysis. The Tan model [107] of current-model control systems is developed in Chap. 18.

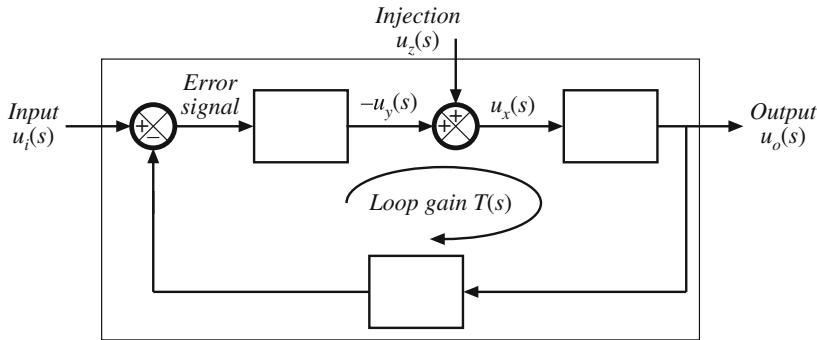
With the advent of high-performance low-cost microcontrollers, digital control of switching converters has proliferated. *Digital control techniques* for switching power converters are introduced in Chap. 19. The basic issues of sampling, quantization, and discrete time effects are described and characterized. Techniques for design of digital compensators are developed.

## 13.2 The Feedback Theorem

Middlebrook's Feedback Theorem is an application of the technique of *null double injection*, to derive the important transfer functions of a closed-loop feedback circuit. In the presence of the input signal source, a test source is injected at a suitable point within the feedback circuit, and key quantities are derived under conditions of setting one of the independent inputs to zero, or of adjusting the two independent sources such that a dependent signal is nulled to zero. The null double injection technique relies on linear superposition to find the desired transfer functions under these null or zeroed conditions. The feedback theorem is stated in Sect. 13.2.1, and is derived in Sect. 13.2.2.

### 13.2.1 Basic Result

Consider the feedback circuit represented by Fig. 13.1. The independent input source of this circuit is  $u_i(s)$  and the output is  $u_o(s)$  (the generic symbol  $u$  is employed; these signals may be voltages, currents, or other quantities). The circuit includes a feedback loop having loop gain  $T(s)$ ; in the laboratory, we could measure this loop gain using the voltage injection method of Sect. 9.6.1 or the current injection method of Sect. 9.6.2. Voltage or current injection using a source  $u_z(s)$  is also illustrated in Fig. 13.1.



**Fig. 13.1** A feedback circuit contains an input source  $u_i(s)$ , output  $u_o(s)$ , and injection source  $u_z(s)$

As noted in Sects. 9.6.1 and 9.6.2, the accuracy of the loop gain measured via the injection method depends on the degree of loading at the injection point, according to Eqs. (9.96) and (9.100). In a practical laboratory experiment, some inaccuracy may be unavoidable. However, for the purposes of theoretical analysis, we may choose to inject at an *ideal injection point* where the impedance inequalities (9.96) or (9.100) are exactly satisfied. In such an analytical “thought experiment,” we inject at a point immediately following an ideal voltage source or current source whose value depends directly on the error signal of the feedback loop. Specifically, we inject at an ideal point that satisfies both of the following criteria:

- A signal  $u_z$  is injected directly after a source  $u_y$ , that is proportional to the error signal of the feedback loop.
- The forward portion of the feedback loop must contain no parallel paths that allow the amplified error signal to reach the output without passing through the ideal injection point. If the injection point is shorted to ground, *i.e.*, if  $u_x = 0$ , then none of the amplified error signal should reach the output.

Injection at an ideal point satisfying both of the above requirements will lead to an exact expression for the physical loop gain  $T(s)$ .

The system of Fig. 13.1 contains two independent sources,  $u_i(s)$  and the injection source  $u_z(s)$ . There are three dependent quantities: the output  $u_o(s)$ , and the signals  $u_y(s)$  and  $u_x(s)$ , immediately before and after the injection source. Note the minus sign associated with  $u_y$  in Fig. 13.1: this is needed to cancel the minus sign associated with negative feedback and obtain the correct loop gain polarity. We can define thought experiments in which an independent source is set to zero, or in which a dependent source is nulled. These thought experiments allow solution for the gains  $G_\infty(s)$ ,  $G_0(s)$ ,  $T(s)$ , and  $T_n(s)$ , and finally for the overall transfer function:

$$G(s) = \frac{u_o}{u_i} = G_\infty \frac{T}{1+T} + G_0 \frac{1}{1+T} \quad (13.1)$$

Each thought experiment is described in detail below.

**Loop gain  $T(s)$ :** The input  $u_i(s)$  is set to zero. In the presence of the injection source  $u_z(s)$ , the circuit is solved for the loop gain  $T(s)$ :

$$T(s) = \left. \frac{u_y(s)}{u_x(s)} \right|_{u_i=0} \quad (13.2)$$

In practice, we assume that we know  $u_x(s)$ , and follow how it propagates around the feedback loop to find  $u_y(s)$ . When the above conditions for an ideal injection point are satisfied, then the resulting  $T(s)$  will have the physical interpretation of the circuit loop gain.

**Ideal forward gain**  $G_\infty(s)$ : In the presence of the input  $u_i(s)$ , the signal  $u_z(s)$  is injected and is adjusted as necessary to null  $u_y(s)$ . Under these conditions, referred to as *null double injection*, the circuit is solved to find  $u_o(s)$ . The ideal forward gain is

$$G_\infty(s) = \left. \frac{u_o(s)}{u_i(s)} \right|_{u_y \rightarrow 0} \quad (13.3)$$

The quantity  $u_y$  is dependent on both independent sources  $u_i$  and  $u_z$ , and hence there is some choice of  $u_i$  and  $u_z$  that will cause  $u_y$  to be nulled to zero. Note that *nulling*  $u_y$  is not the same as *shorting*  $u_y$ : the null condition takes place in the original circuit, and results from a specific selection of values of the independent sources. Specifically, nulling  $u_y$  effectively also nulls the error signal because of the conditions satisfied by the ideal injection point. Hence  $G_\infty$  is the gain from the input  $u_i$  to the output  $u_o$  under the condition that the error signal is nulled to zero: the output is perfectly regulated. It can be verified that the gain  $G(s)$  of Eq. (13.1) reduces to  $G_\infty$  under the condition that  $T \rightarrow \infty$ .

If the feedback circuit employs a conventional operational amplifier, then nulling  $v_y$  is equivalent to employing the principle of virtual ground, in accordance with common practice in the analysis of op amp circuits. In an op amp circuit with negative feedback,  $G_\infty$  coincides with the gain when an ideal op amp is present.

**Gain**  $G_0(s)$ : In this thought experiment, null double injection is performed as follows: in the presence of the input  $u_i(s)$ , the signal  $u_z(s)$  is injected and is adjusted as necessary to null  $u_x(s)$ . Under these conditions, the circuit is solved to find  $u_o(s)$ . The gain  $G_0$  is

$$G_0(s) = \left. \frac{u_o(s)}{u_i(s)} \right|_{u_x \rightarrow 0} \quad (13.4)$$

Note that nulling  $u_x$  effectively prevents the amplified error signal from reaching the output, because of the conditions satisfied by the ideal injection point. Hence  $G_0$  is the gain from the input  $u_i$  to the output  $u_o$  under the condition that the feedback loop does not control the output. It can be verified that the gain  $G(s)$  of Eq. (13.1) reduces to  $G_0$  under the condition that  $T \rightarrow 0$ .

The physical interpretation of  $G_0$  depends on the quantity being analyzed. For an amplifier in which  $u_i$  and  $u_o$  are the input and output voltages,  $G_0$  has the interpretation of *direct forward transmission through the feedback path*. With  $u_x$  nulled, there is no way for the input signal to reach the output via the forward path of the loop, and so  $G_0$  must result from signals reaching the output by flowing (backwards!) through the feedback path. In the case of disturbance transfer functions such as a closed-loop  $Z_{out}$  or  $G_{vg}$ , the  $G_0$  term represents the open-loop disturbance transfer function.

**Null loop gain**  $T_n(s)$ : In the presence of the input  $u_i(s)$ , the signal  $u_z(s)$  is injected and is adjusted as necessary to null the output  $u_o(s)$ . Note that this is another case of null double injection. Under these conditions, the circuit is solved for the null loop gain  $T_n(s)$ :

$$T_n(s) = \left. \frac{u_y(s)}{u_x(s)} \right|_{u_o \rightarrow 0} \quad (13.5)$$

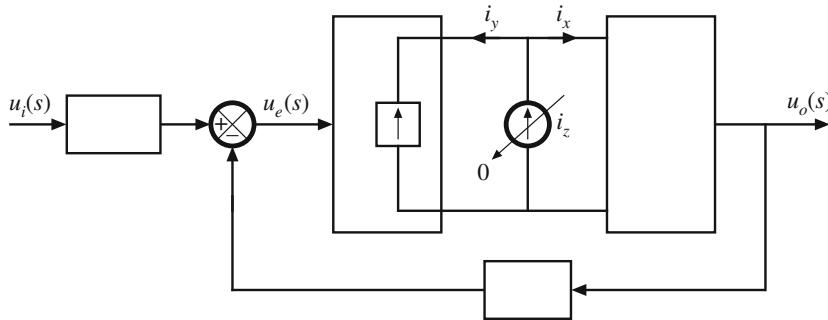
Solution for  $T_n$  is similar to the analysis of  $T$ , although it is usually somewhat simpler because  $T_n$  does not depend on the load impedance. The null loop gain  $T_n$  has less physical interpretation than does  $T$ ; it is related to the other above quantities according to the *reciprocity relationship*:

$$\frac{T_n(s)}{T(s)} = \frac{G_\infty(s)}{G_0(s)} \quad (13.6)$$

Hence one can solve for three of the four gains, whichever is easiest, then employ the reciprocity relationship to find the fourth gain. Finally, the overall closed-loop gain  $G(s)$  is found by evaluation of Eq. (13.1).

### 13.2.2 Derivation

The basic results of Sect. 13.2.1 can be derived through the use of superposition and null double injection in the several thought experiments described.



**Fig. 13.2** Current injection  $i_z = u_z$  at an ideal injection point in a feedback loop. The original condition is illustrated, in which  $i_z$  is set to zero

**Original condition:**  $u_z = 0$ , in the presence of the input  $u_i$ . Figure 13.2 illustrates current injection at an ideal injection point, with the original condition  $i_z = 0$ . In this case, the closed-loop forward gain  $G(s)$  is given by

$$u_o \Big|_{u_z=0} = Gu_i \quad (13.7)$$

This is the definition of  $G(s)$ . Additionally, under this condition we can express  $i_x$  and  $i_y$  in terms of the input  $u_i$ :

$$i_x \Big|_{i_z=0} = -i_y \Big|_{i_z=0} = G_a(s)u_i \quad (13.8)$$

For the current injection illustrated in Fig. 13.2,  $u_x = i_x$  and  $u_y = i_y$ . Equation (13.8) is the definition of  $G_a(s)$ . Both  $G(s)$  and  $G_a(s)$  are unknowns at this point. It is desired to eliminate  $G_a$ , and to solve for  $G$ .

**Injection of  $u_z$ :** Figure 13.3 illustrates the case in which the input  $u_i$  is set to zero, and current injection  $i_z = u_z$  is applied. Under these conditions, we can express  $i_y$  as some function of  $i_x$  as follows:

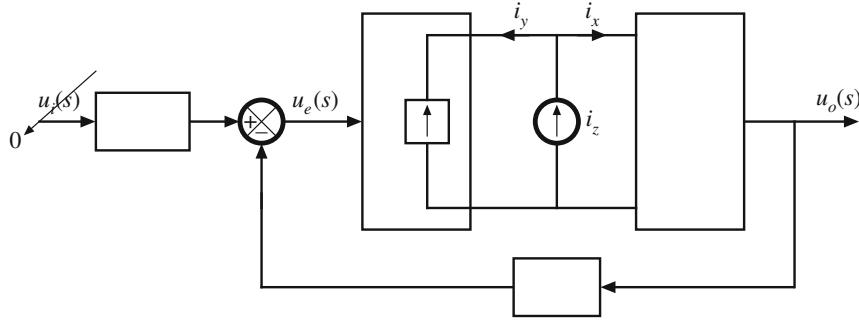
$$i_y \Big|_{u_i=0} = T(s) i_x \Big|_{u_i=0} \quad (13.9)$$

This is the definition of the loop gain  $T(s)$ .

Under these conditions, we can also express the quantities  $i_x$  and  $i_y$  as functions of the injection source  $i_z$ , by writing the node equation at the injection point:

$$i_x + i_y = i_z \quad (13.10)$$

By substitution of Eq. (13.9) into Eq. (13.10) and solution for  $i_x$  and  $i_y$ , we can find that



**Fig. 13.3** Current injection  $i_z = u_z$ , with the input  $u_i$  set to zero

$$i_x \Big|_{u_i=0} = \frac{1}{1+T} i_z \quad (13.11)$$

$$i_y \Big|_{u_i=0} = \frac{T}{1+T} i_z \quad (13.12)$$

Also under these conditions, we can express the output  $u_o$  in terms of the injection source  $i_z$  as

$$u_o \Big|_{u_i=0} = G_b(s) i_x \Big|_{u_i=0} = \frac{G_b}{1+T} i_z \quad (13.13)$$

This is the definition of  $G_b$ . It is desired to eliminate  $G_b$ .

**In the presence of both  $u_i$  and  $u_z = i_z$ :** we can employ superposition to express the dependent quantities  $i_x$ ,  $i_y$ , and  $u_o$  as functions of the two independent inputs  $u_i$  and  $i_z$ . For  $i_x$ , we can write

$$i_x = i_x \Big|_{i_z=0} + i_x \Big|_{u_i=0} \quad (13.14)$$

Substitution of Eqs. (13.8) and (13.11) into Eq. (13.14) leads to the general expression for  $i_x$ :

$$i_x = G_a u_i + \frac{1}{1+T} i_z \quad (13.15)$$

We can find a similar expression for  $i_y$ :

$$i_y = i_y \Big|_{i_z=0} + i_y \Big|_{u_i=0} \quad (13.16)$$

Substitution of Eqs. (13.8) and (13.12) into Eq. (13.16) leads to the general expression for  $i_y$ :

$$i_y = -G_a u_i + \frac{T}{1+T} i_z \quad (13.17)$$

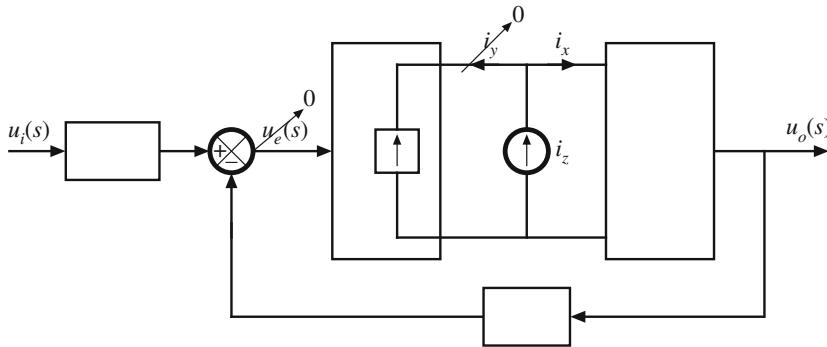
The output  $u_o$  can be expressed via superposition as

$$u_o = u_o \Big|_{i_z=0} + u_o \Big|_{u_i=0} \quad (13.18)$$

Substitution of Eqs. (13.7) and (13.13) into Eq. (13.18) leads to the general expression for  $u_o$ :

$$u_o = G u_i + \frac{G_b}{1+T} i_z \quad (13.19)$$

Next, we perform the “thought experiments” described in Sect. 13.2.1.



**Fig. 13.4** In the presence of  $u_i$ , adjust  $i_z = u_z$  to null  $i_y$

**Null double injection, nulling  $i_y$ :** In the presence of the input  $u_i$ , adjust  $i_z$  as necessary to null  $i_y$ , as illustrated in Fig. 13.4. Under these conditions, Eq. (13.17) becomes

$$0 = -G_a u_i + \frac{T}{1+T} i_z \Big|_{i_y \rightarrow 0} \quad (13.20)$$

and Eq. (13.19) becomes

$$u_o \Big|_{i_y \rightarrow 0} = G u_i + \frac{G_b}{1+T} i_z \Big|_{i_y \rightarrow 0} \quad (13.21)$$

Elimination of  $i_z$  from Eqs. (13.20) and (13.21) leads to

$$u_o \Big|_{i_y \rightarrow 0} = G u_i + \frac{G_a G_b}{T} u_i \quad (13.22)$$

We can define

$$G_\infty = G + \frac{G_a G_b}{T} \quad (13.23)$$

Hence

$$u_o \Big|_{i_y \rightarrow 0} = G_\infty u_i \quad (13.24)$$

In this thought experiment, we adjust  $i_z$  as necessary to null  $i_y$ . Since  $i_y$  is directly proportional to the error signal, nulling  $i_y$  also nulls the error signal. Hence the gain  $G_\infty$  has the physical interpretation of the ideal forward gain of the loop, with zero error.

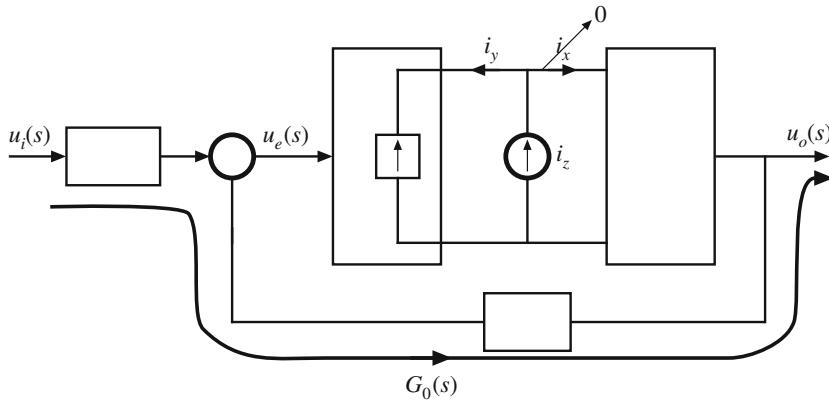
**Null double injection, nulling  $i_x$ :** In the presence of the input  $u_i$ , adjust  $i_z$  as necessary to null  $i_x$ , as illustrated in Fig. 13.5. Under these conditions, Eq. (13.15) becomes

$$0 = G_a u_i + \frac{1}{1+T} i_z \Big|_{i_x \rightarrow 0} \quad (13.25)$$

Equation (13.19) becomes

$$u_o \Big|_{i_x \rightarrow 0} = G u_i + \frac{G_b}{1+T} i_z \Big|_{i_x \rightarrow 0} \quad (13.26)$$

Elimination of  $i_z$  from Eqs. (13.25) and (13.26) leads to



**Fig. 13.5** In the presence of  $u_i$ , adjust  $i_z = u_z$  to null  $i_x$

$$u_o \Big|_{i_x \rightarrow 0} = G u_i - G_a G_b u_i \quad (13.27)$$

We can define

$$G_0 = G - G_a G_b \quad (13.28)$$

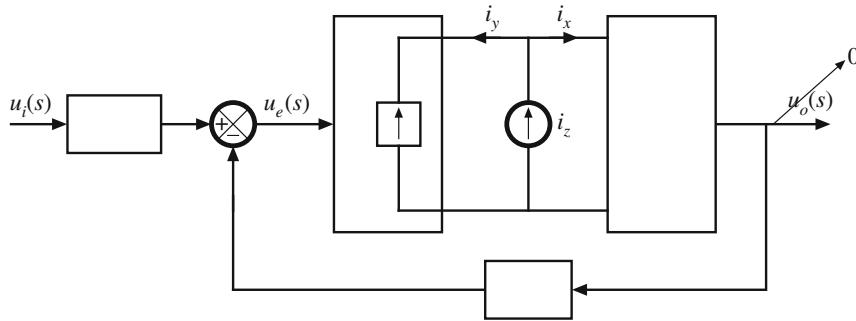
Hence

$$u_o \Big|_{i_x \rightarrow 0} = G_0 u_i \quad (13.29)$$

In this thought experiment, we adjust  $i_z$  as necessary to null  $i_x$ . Consequently, there is no transmission of the amplified error signal through the forward path:  $i_x = 0$ . In the system depicted in Fig. 13.5, the only other way to obtain a nonzero output is via the feedback path, assuming that

signals are capable of propagating in either direction through this path. Hence, the gain  $G_0$  has the physical interpretation of *direct forward transmission through the feedback path*.

In later examples, we will see that  $G_0$  may have the interpretation of the open-loop gain from disturbances to the output. In these examples, the system architecture is more complex than is envisioned in Fig. 13.5.



**Fig. 13.6** In the presence of  $u_i$ , adjust  $i_z = u_z$  to null  $u_o$

**Null double injection, nulling  $u_o$ :** In the presence of the input  $u_i$ , adjust  $i_z$  as necessary to null  $u_o$ , as illustrated in Fig. 13.6. Note that the output  $u_o$  is *not* shorted. For example, in the case where the output  $u_o$  is a voltage, this null condition implies that zero current flows through the load impedance, and any current produced by the output block must flow directly into the feedback path.

Under these conditions, Eq. (13.19) becomes

$$0 = G u_i + \frac{G_b}{1 + T} i_z \Big|_{u_o \rightarrow 0} \quad (13.30)$$

Equation (13.15) becomes

$$i_x = G_a u_i + \frac{1}{1 + T} i_z \Big|_{u_o \rightarrow 0} \quad (13.31)$$

And Eq. (13.17) becomes

$$i_y = -G_a u_i + \frac{T}{1 + T} i_z \Big|_{u_o \rightarrow 0} \quad (13.32)$$

We can eliminate  $u_i$  and  $i_z \Big|_{u_o \rightarrow 0}$  from the above equations, and solve for the relationship between  $i_y$  and  $i_x$  under the condition that the output  $u_o$  is nulled. After performing some algebra, we obtain the following result:

$$i_y \Big|_{u_o \rightarrow 0} = \frac{TG + G_a G_b}{G - G_a G_b} i_x \Big|_{u_o \rightarrow 0} \quad (13.33)$$

We can define

$$T_n = \frac{i_y}{i_x} \Big|_{u_o \rightarrow 0} = \frac{TG + G_a G_b}{G - G_a G_b} \quad (13.34)$$

The *null loop gain*  $T_n$  is the transfer function from  $i_x$  to  $i_y$  under the condition that, in the presence of the input  $u_i$ , the injection source  $i_z$  is adjusted to null the output  $u_o$ . The null loop gain  $T_n$  has less physical interpretation than the loop gain  $T$ ; it is similar except that the effects of output loading are removed. Hence  $T_n$  is somewhat simpler to compute than  $T$ . The next paragraphs give a simple way to relate  $T$  and  $T_n$ , and hence computation of  $T_n$  can be a useful step in the computation of  $T$ .

**Final result:** With the above definitions, one can solve the feedback circuit for the quantities  $G_0$ ,  $G_\infty$ ,  $T$ , and  $T_n$ . One can determine the closed-loop transfer function  $G$  in terms of these quantities, by eliminating the intermediate quantities  $G_a$  and  $G_b$  from the above equations and solving for  $G$  in terms of  $G_0$ ,  $G_\infty$ ,  $T$ , and  $T_n$ . From Eq. (13.28), we have

$$G_0 = G - G_a G_b \quad (13.35)$$

From Eq. (13.23),

$$G_\infty = G + \frac{G_a G_b}{T} \quad (13.36)$$

which can be rewritten as

$$G_\infty T = TG + G_a G_b \quad (13.37)$$

From Eq. (13.34), we have

$$T_n = \frac{TG + G_a G_b}{G - G_a G_b} \quad (13.38)$$

Substitution of Eqs. (13.35) and (13.37) into Eq. (13.38) leads to the reciprocity relationship

$$T_n = \frac{G_\infty T}{G_0} \quad \text{or} \quad \frac{T_n}{T} = \frac{G_\infty}{G_0} \quad (13.39)$$

This important relationship implies that we need only to solve for three of the gains  $G_0$ ,  $G_\infty$ ,  $T$ , and  $T_n$ ; the fourth can be found from Eq. (13.39). Further, if the three gains are expressed in factored pole-zero form, then the fourth gain that results from Eq. (13.39) will also be factored.

Now eliminate the quantity  $G_a G_b$  from Eqs. (13.35) and (13.36), and use the result to solve Eqs. (13.35) to (13.39) for  $G$ . After a few lines of algebra, the following result is obtained:

$$G = G_\infty \frac{\left(1 + \frac{1}{T_n}\right)}{\left(1 + \frac{1}{T}\right)} = G_\infty \frac{T}{1+T} + G_0 \frac{1}{1+T} \quad (13.40)$$

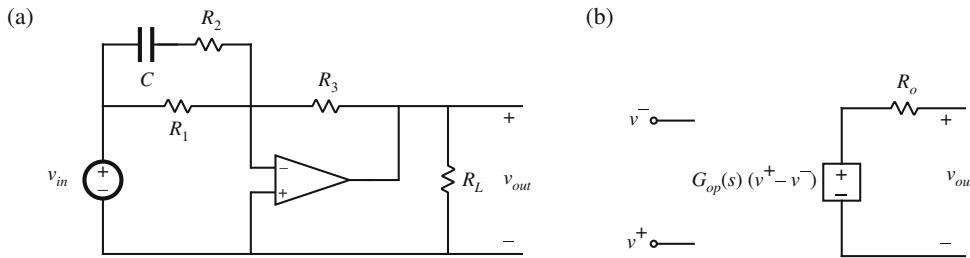
This is the desired expression for the closed-loop gain  $G$ . Note that, for large loop gain,

$$G \rightarrow G_\infty \quad \text{for} \quad \|T\| \rightarrow \infty \quad (13.41)$$

So  $G_\infty$  is the closed-loop forward gain with large loop gain. For small loop gain,

$$G \rightarrow G_0 \quad \text{for} \quad \|T\| \rightarrow 0 \quad (13.42)$$

Hence  $G_0$  is the closed-loop forward gain when the loop gain tends to zero.



**Fig. 13.7** Op amp PD compensator circuit example: (a) circuit schematic, (b) op amp equivalent circuit model

### 13.3 Example: Op Amp PD Compensator Circuit

As a first example of application of the feedback theorem, let us analyze the op amp circuit illustrated in Fig. 13.7a. With an ideal op amp, this lead-lag circuit exhibits a transfer function having a zero and pole, and is suitable as a PD compensator in feedback loops requiring improvement of phase margin. To examine the impact of the frequency response and output impedance of a practical op amp, we will model the op amp using the equivalent circuit illustrated in Fig. 13.7b. The positive and negative input ports are modeled with infinite input impedance, and a Thevenin-equivalent circuit models the output port. The op amp gain is

$$G_{op}(s) = \frac{G_{op0}}{\left(1 + \frac{s}{\omega_1}\right)} \quad (13.43)$$

For this example, the op amp model values are

$$G_{op0} = 10^5 \Rightarrow 100 \text{ dB} \quad f_1 = \frac{\omega_1}{2\pi} = 10 \text{ Hz}$$

$$R_o = 50 \Omega$$

This typical op amp internal gain \$G\_{op}\$ exhibits a dc gain of 100 dB and a pole at 10 Hz; its magnitude Bode plot is given in Fig. 13.8. The op amp unity gain frequency is 1 MHz: for frequencies above 10 Hz, the magnitude asymptote follows the equation

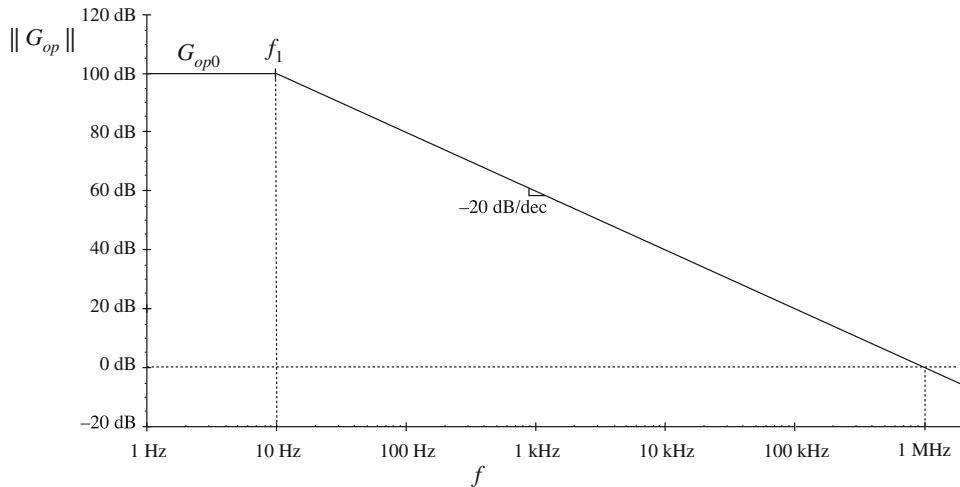
$$\|G_{op}\| \approx \frac{1 \text{ MHz}}{f} \quad (13.44)$$

The element values are

$$\begin{aligned} R_1 &= 1.6 \text{ k}\Omega & R_2 &= 16 \Omega & R_L &= 100 \Omega \\ R_3 &= 1.6 \text{ k}\Omega & C &= 0.1 \mu\text{F} \end{aligned}$$

To analyze this feedback circuit, we insert the op amp model of Fig. 13.7b into the circuit of Fig. 13.7a, leading to the equivalent circuit illustrated in Fig. 13.9.

To apply the feedback theorem, we first identify an ideal injection point. The error signal of this op amp feedback circuit can be taken to be the op amp differential input voltage \$(v^+ - v^-)\$: when this voltage is zero, the op amp circuit operates ideally with zero error. In the op amp model of Fig. 13.7b, the dependent voltage source is proportional to \$(v^+ - v^-)\$, and hence we can employ voltage injection immediately following this source as illustrated in Fig. 13.9: this will



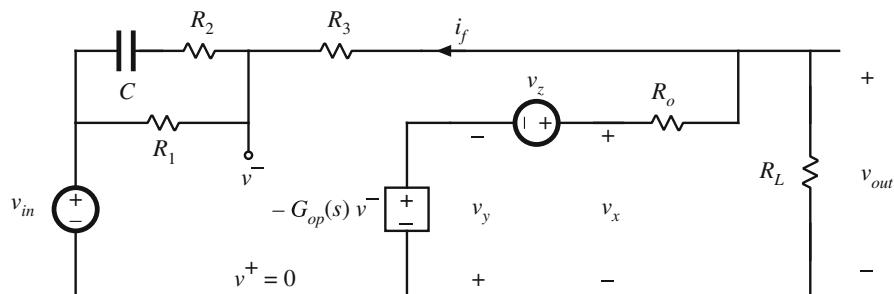
**Fig. 13.8** The op amp internal gain exhibits a single-pole response with a unity gain frequency of 1 MHz

cause  $v_y$  to be directly proportional to the error signal  $(v^+ - v^-)$ . With this choice of injection point, we can solve the circuit to find  $G_0$ ,  $G_\infty$ ,  $T$ , and  $T_n$  as described in Sect. 13.2.1.

The ideal forward gain  $G_\infty$  is found according to Eq. (13.3). For this example, we obtain

$$G_\infty(s) = \left. \frac{v_{out}(s)}{v_{in}(s)} \right|_{v_y \rightarrow 0} \quad (13.45)$$

As with all examples of null double injection, the key to easily solving for this gain is to begin with the null condition and its implications. When  $v_y$  is nulled, the dependent voltage source  $-G_{op}v^-$  is also nulled, which implies that  $v^-$  is nulled. Hence, the current  $i_f$  can be related to the input voltage  $v_{in}$  as follows:



**Fig. 13.9** PD compensator circuit, with the op amp equivalent circuit model inserted. Voltage injection at the output of the dependent voltage source is included

$$\begin{aligned}
 i_f &= -\frac{v_{in} - v^-}{R_1 \left| \left( R_2 + \frac{1}{sC} \right) \right|_{v^- \rightarrow 0}} \\
 &= -\frac{v_{in}}{R_1 \left| \left( R_2 + \frac{1}{sC} \right) \right|} \quad (13.46)
 \end{aligned}$$

The null condition also allows us to easily relate the output voltage  $v_{out}$  to  $i_f$ :

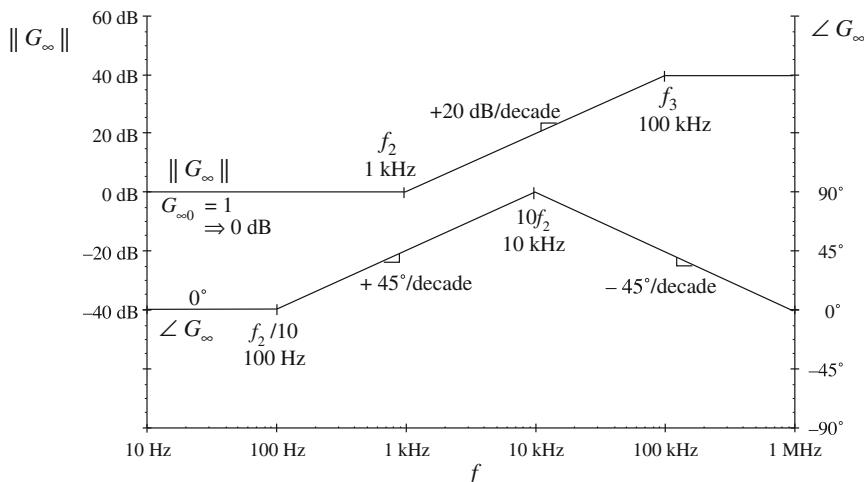
$$\begin{aligned}
 v_{out} &= v^- + i_f R_3 \Big|_{v^- \rightarrow 0} \\
 &= i_f R_3 \quad (13.47)
 \end{aligned}$$

Substitution of Eq. (13.46) into (13.47) leads to the expression for  $G_\infty$ :

$$G_\infty = -\frac{R_3}{R_1 \left| \left( R_2 + \frac{1}{sC} \right) \right|} = -\frac{R_3}{R_1} \frac{1 + s(R_1 + R_2)C}{1 + sR_2C} \quad (13.48)$$

For this op amp circuit example, the steps in determination of  $G_\infty$  coincide with use of the “virtual ground” principle commonly employed in beginning circuit analysis classes: nulling  $v_y$  leads to  $v^+ = v^-$ . The above analysis then follows. Indeed, the null double injection analysis of  $G_\infty$  can be viewed as a generalization to arbitrary feedback circuits.

Substitution of numerical values into Eq. (13.48) reveals that  $G_\infty$  contains a DC gain  $G_{\infty 0}$ , zero at frequency  $f_2$ , and pole at frequency  $f_3$ , as follows:



**Fig. 13.10** Bode plot of  $G_\infty$ , op amp example

$$\|G_{\infty 0}\| = \frac{R_3}{R_1} = 1 \Rightarrow 0 \text{ dB} \quad (13.49)$$

$$f_2 = \frac{1}{2\pi(R_1 + R_2)C} = 1 \text{ kHz} \quad (13.50)$$

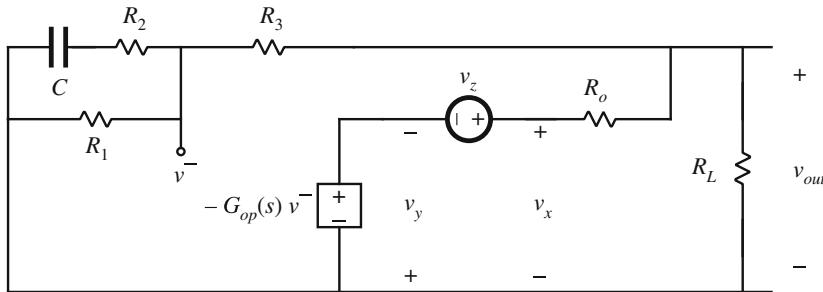
$$f_3 = \frac{1}{2\pi R_2 C} = 100 \text{ kHz} \quad (13.51)$$

A Bode plot of  $G_\infty$  is given in Fig. 13.10. This transfer function is typical of a PD compensator that might be employed to improve the phase margin of a switching converter feedback system having a crossover frequency in the vicinity of 10 kHz.

The loop gain  $T(s)$  is found according to Eq. (13.2). For this example, we obtain

$$T(s) = \left. \frac{v_y(s)}{v_x(s)} \right|_{v_{in}=0} \quad (13.52)$$

Under the condition that the input voltage  $v_{in}$  is set to zero, the equivalent circuit of Fig. 13.9 reduces to Fig. 13.11.



**Fig. 13.11** Determination of loop gain  $T(s)$

To find the loop gain  $T(s)$ , we take  $v_x$  as given and solve the circuit for  $v_y$ . This can be done in several steps: first find the transfer function from  $v_x$  to  $v_{out}$ , then the transfer function from  $v_{out}$  to  $v^-$ , and then the transfer function from  $v^-$  to  $v_y$ . The loop gain can then be expressed as

$$T(s) = \left( \frac{v_{out}}{v_x} \right) \left( \frac{v^-}{v_{out}} \right) \left( \frac{v_y}{v^-} \right) \quad (13.53)$$

The first two terms of Eq. (13.53) are voltage divider transfer functions, while the third is the op amp internal gain  $G_{op}$ . Hence we can express Eq. (13.53) as:

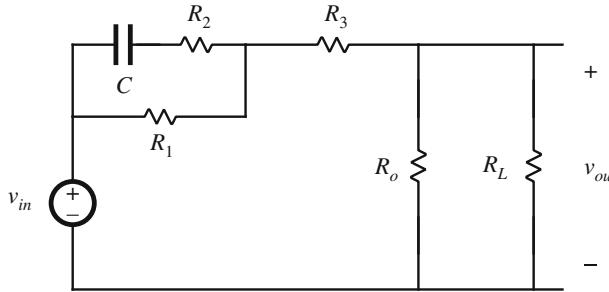
$$T(s) = \underbrace{\frac{R_L \left[ R_3 + R_1 \left( R_2 + \frac{1}{sC} \right) \right]}{R_o + R_L \left[ R_3 + R_1 \left( R_2 + \frac{1}{sC} \right) \right]}}_{\frac{v_{out}}{v_x}} \underbrace{\frac{R_1 \left( R_2 + \frac{1}{sC} \right)}{R_3 + R_1 \left( R_2 + \frac{1}{sC} \right)}}_{\frac{v^-}{v_{out}}} \underbrace{\left( G_{op}(s) \right)}_{\frac{v_y}{v^-}} \quad (13.54)$$

We could simplify this expression via algebraic manipulations, to express  $T(s)$  in factored form. However, it is easier to find the factored  $T(s)$  by use of the reciprocity relationship, Eq. (13.39). Hence, the construction of the Bode plot of  $T(s)$  is reserved for later, after  $G_0$  and  $T_n$  have been found.

The direct forward transmission gain  $G_0(s)$  is found as defined in Ex. (13.4). For this example, we obtain

$$G_0(s) = \frac{v_{out}(s)}{v_{in}(s)} \Big|_{\substack{v_x \rightarrow 0 \\ v_z \text{ null}}} \quad (13.55)$$

In the model of Fig. 13.9, in the presence of the input  $v_{in}$  we adjust the injection source  $v_z$  such that  $v_x$  is nulled. Under these conditions, the dependent voltage source  $-G_{op}v^-$  does not influence the output, and the circuit reduces to Fig. 13.12, with  $R_o$  effectively in parallel with  $R_L$ .



**Fig. 13.12** Determination of direct forward transmission through feedback path,  $G_0$

It can be seen that  $G_0$  is a voltage divider transfer function:

$$\begin{aligned} G_0(s) &= \frac{v_{out}(s)}{v_{in}(s)} \Big|_{\substack{v_x \rightarrow 0 \\ v_z \text{ null}}} \\ &= \frac{R_o \| R_L}{R_o \| R_L + R_3 + R_1 \| \left( R_2 + \frac{1}{sC} \right)} \end{aligned} \quad (13.56)$$

This expression can be simplified via algebraic manipulation to the following factored form:

$$G_0(s) = \frac{R_o \| R_L}{R_1 + R_3 + R_o \| R_L} \frac{1 + sC(R_1 + R_2)}{1 + sC(R_2 + R_1 \| (R_3 + R_o \| R_L))} \quad (13.57)$$

The expression for  $G_0$  is in the following standard normalized form:

$$G_0 = G_{00} \frac{\left(1 + \frac{s}{\omega_2}\right)}{\left(1 + \frac{s}{\omega_4}\right)} \quad (13.58)$$

with

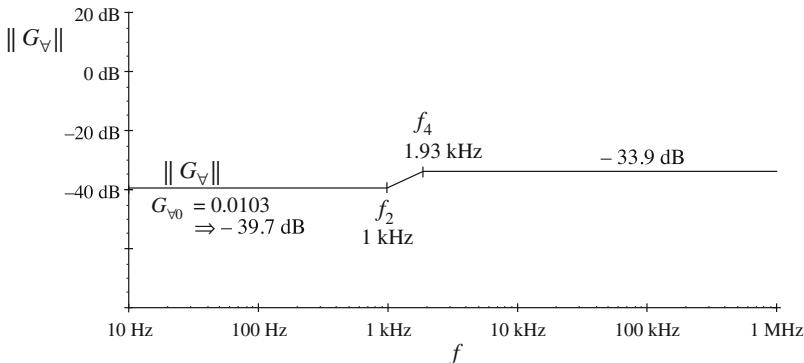
$$\begin{aligned} G_{00} &= \frac{R_o \| R_L }{R_1 + R_3 + R_o \| R_L} = 0.0103 \Rightarrow -39.7 \text{ dB} \\ f_2 &= \frac{\omega_2}{2\pi} = \frac{1}{2\pi C(R_1 + R_2)} = 1 \text{ kHz} \\ f_4 &= \frac{\omega_4}{2\pi} = \frac{1}{2\pi C(R_2 + R_1 \| (R_3 + R_o \| R_L))} = 1930 \text{ Hz} \end{aligned} \quad (13.59)$$

Figure 13.13 contains the Bode plot of  $G_0(s)$ .  $\|G_0\|$  is small in this example, and is unlikely to influence  $G(s)$  over frequencies of interest. However, this computation assists in determination of the factored  $T(s)$ .

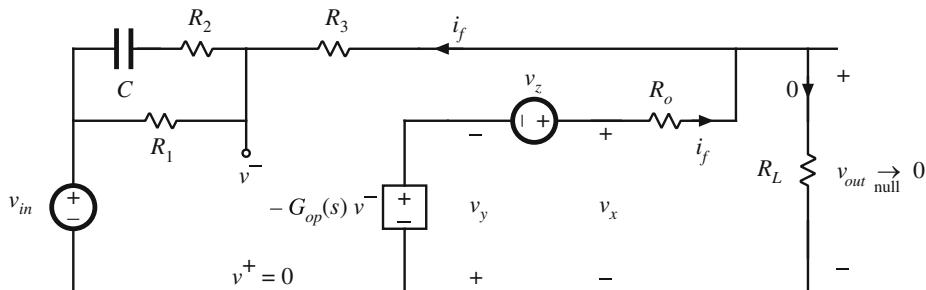
The null loop gain  $T_n(s)$  is found as defined in Eq. (13.5). For this example, we obtain

$$T_n(s) = \left. \frac{v_y(s)}{v_x(s)} \right|_{v_o \rightarrow 0} \quad (13.60)$$

In the model of Fig. 13.14: in the presence of the input  $v_{in}$ , we adjust the injection source  $v_z$  such that the output  $v_{out}$  is nulled. Under these conditions, we find the transfer function from  $v_x$  to  $v_y$ .



**Fig. 13.13** Bode plot of the magnitude of  $G_0$



**Fig. 13.14** Determination of null loop gain  $T_n$

The null condition implies that there is no voltage across the load resistor  $R_L$  and hence there is no current through the load resistor. The op amp output current is

$$i_f = \frac{v_x}{R_o} \quad (13.61)$$

Since the load current is zero, the current  $i_f$  flows through  $R_3$ . Since the load voltage is zero, we can express  $v^-$  as:

$$v^- = -i_f R_3 \quad (13.62)$$

The voltage  $v_y$  is related to  $v^-$  by the op amp gain  $G_{op}$ :

$$v_y = G_{op}(s)v^- \quad (13.63)$$

Hence, we can express the null loop gain as

$$T_n(s) = \underbrace{\left(\frac{1}{R_o}\right)}_{\frac{i_f}{v_x}} \underbrace{(-R_3)}_{\frac{v^-}{i_f}} \underbrace{\left(G_{op}(s)\right)}_{\frac{v_y}{v^-}} \quad (13.64)$$

The expression for  $T_n$  is considerably simpler than the expression for  $T$ , because the load impedance does not affect  $T_n$ . The null loop gain contains the same poles as  $G_{op}(s)$ .

We can now employ the reciprocity relationship, Eq. (13.39), to find a factored expression for the loop gain  $T(s)$ :

$$T = \frac{G_0 T_n}{G_\infty} \quad (13.65)$$

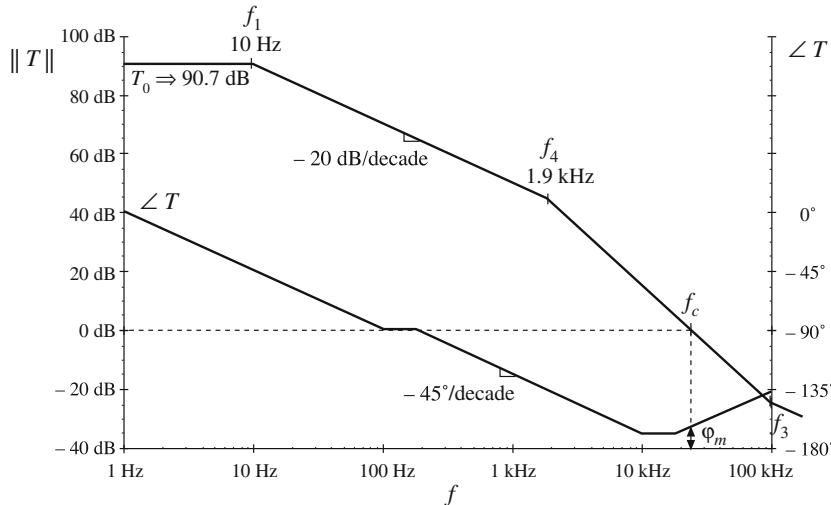
Insertion of Eqs. (13.64), (13.58), and (13.48) into Eq. (13.65) leads to the following expression for the loop gain:

$$\begin{aligned} T(s) &= \underbrace{\left(-\frac{R_3}{R_o} G_{op}(s)\right)}_{T_n} \underbrace{\left(G_{00} \frac{\left(1 + \frac{s}{\omega_2}\right)}{\left(1 + \frac{s}{\omega_4}\right)}\right)}_{G_0} \underbrace{\left(-\frac{R_1}{R_3} \frac{\left(1 + \frac{s}{\omega_3}\right)}{\left(1 + \frac{s}{\omega_2}\right)}\right)}_{\frac{1}{G_\infty}} \\ &= T_0 \frac{\left(1 + \frac{s}{\omega_3}\right)}{\left(1 + \frac{s}{\omega_1}\right) \left(1 + \frac{s}{\omega_4}\right)} \end{aligned} \quad (13.66)$$

with

$$\begin{aligned} T_0 &= \frac{R_1}{R_o} G_{op0} G_{00} \\ &= 33000 \Rightarrow 90.7 \text{ dB} \end{aligned} \quad (13.67)$$

Figure 13.15 contains a sketch of the magnitude and phase asymptotes of this loop gain. It can be seen that  $T(s)$  contains a DC gain of 90.7 dB, poles at 10 Hz and 1.9 kHz, and a zero at 100 kHz. The crossover frequency  $f_c$  can be estimated using the magnitude asymptote between the 1.9 kHz pole and the 100 kHz zero; over this range of frequencies, we can express the magnitude asymptote as:



**Fig. 13.15** Sketch of the magnitude and phase asymptotes of the loop gain  $T(s)$

$$T(s) = T_0 \frac{\left(1 + \frac{s}{\omega_3}\right)}{\left(\frac{s}{\omega_1}\right)\left(\frac{s}{\omega_4}\right)}$$

$$\|T\| \approx T_0 \frac{(1)}{\left(\frac{\omega}{\omega_1}\right)\left(\frac{\omega}{\omega_4}\right)} \quad (13.68)$$

At the crossover frequency  $f_c$ , the magnitude of  $T$  is equal to unity. Insertion of  $\omega = \omega_c$  with  $\|T\| = 1$  into Eq. (13.68) leads to

$$1 = T_0 \frac{\omega_1 \omega_4}{\omega_c^2} \quad (13.69)$$

Hence the crossover frequency is

$$f_c = \frac{\omega_c}{2\pi} = \sqrt{T_0 f_1 f_4}$$

$$= 25.2 \text{ kHz} \quad (13.70)$$

We can estimate the phase margin as follows. Since the crossover frequency is more than a decade above both pole frequencies, the poles contribute a total of  $-180^\circ$  to  $\angle T(f_c)$ . The zero at  $f_3 = 100 \text{ kHz}$  contributes phase

$$\tan^{-1} \frac{f_c}{f_3} = 14.2^\circ \quad (13.71)$$

Hence, the phase of  $T$  at the crossover frequency is

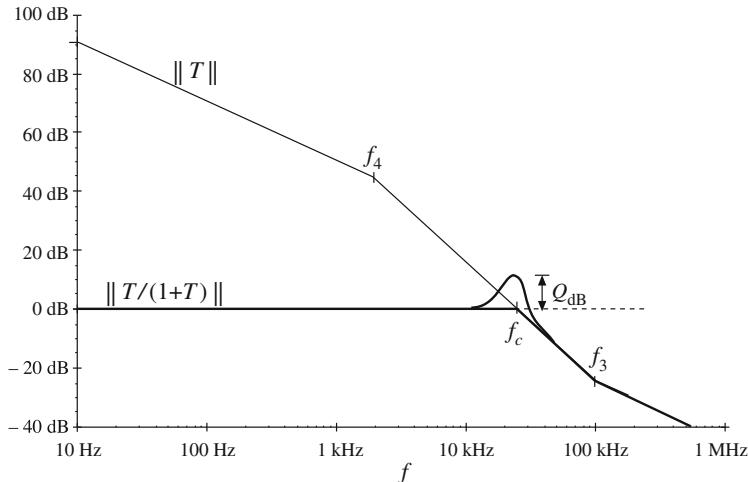
$$\angle T(f_c) = -180^\circ + 14.2^\circ = -165.8^\circ \quad (13.72)$$

The phase margin is

$$\varphi_m = 180^\circ + \angle T(f_c) = 14.2^\circ \quad (13.73)$$

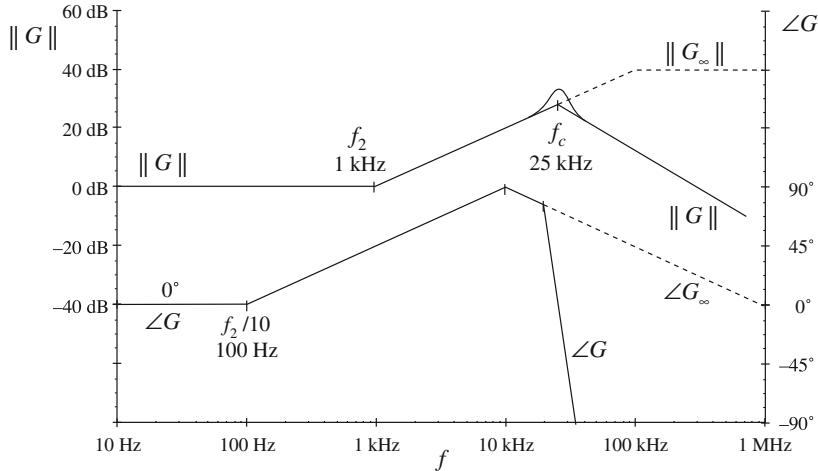
Although the phase margin is positive, it is not very large. This implies that the closed-loop transfer function  $T/(1+T)$  contains complex poles at  $f_c$  having high  $Q$  determined by evaluation of Eq. (9.41):

$$Q = \frac{\sqrt{\cos \varphi_m}}{\sin \varphi_m} = 4 \Rightarrow 12 \text{ dB} \quad (13.74)$$



**Fig. 13.16** Graphical construction of the closed-loop transfer function  $T/(1 + T)$

The graphical construction method can now be employed to construct the closed-loop transfer function  $T/(1 + T)$  according to Eq. (9.11). The result is illustrated in Fig. 13.16. Below the crossover frequency  $f_c$ ,  $\|T\|$  is large and hence  $T/(1 + T)$  is approximately equal to 1. There are two poles at the crossover frequency, having  $Q$  factor given by Eq. (13.74). At frequencies above  $f_c$ , the transfer function  $\|T/(1 + T)\|$  follows  $\|T\|$ .



**Fig. 13.17** Graphical construction of the closed-loop transfer function  $G$

Finally, the closed-loop transfer function  $G = v_{out}/v_{in}$  can be found using Eq. (13.1), with the result illustrated in Fig. 13.17.  $G$  is given by

$$G = G_\infty \frac{T}{1+T} + G_0 \frac{1}{1+T} \quad (13.75)$$

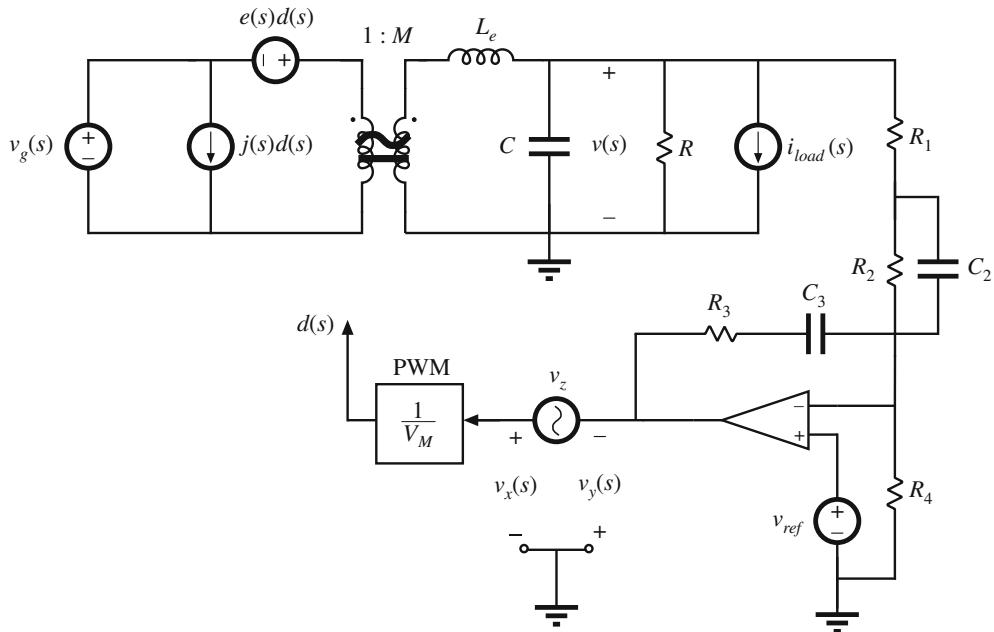
The term  $G_0/(1+T)$  is small, and is found to be insignificant below 30 MHz. Hence  $G$  follows  $G_\infty$  below the crossover frequency, where  $T/(1+T) \approx 1$ . The  $T/(1+T)$  term introduces its resonance at the crossover frequency, and  $G$  differs significantly from  $G_\infty$  at frequencies above  $f_c$ . The op amp is unable to produce the required gain at frequencies above 25 kHz, causing the closed-loop transfer function to differ significantly from the prediction obtained using the traditional op amp virtual ground principle.

If this op amp circuit is employed as a PD compensator in a switching converter feedback loop, the compensator resonance at 25 kHz may seriously degrade the stability of the converter feedback loop. The resonance may introduce additional converter crossover frequencies, and the converter phase margin at frequencies approaching or exceeding 25 kHz may be substantially reduced. It would be possible to make  $G$  follow  $G_\infty$  at higher frequencies by employing an op amp whose unity gain frequency is larger: the PD circuit  $f_c$  could be increased from 25 kHz to 100 kHz by increasing the op amp unity gain frequency from 1 MHz to 4 MHz.

### 13.4 Example: Closed-Loop Regulator

As a second example, consider application of the feedback theorem to the closed-loop buck regulator of Sect. 9.5.4, with the compensator circuit of Fig. 15.29. Figure 13.18 shows the small-signal canonical model of the CCM converter power stage (from Fig. 7.38), along with the feedback and PID compensator circuit, and with injection  $\hat{v}_z$  applied.

The output of this system is taken to be the output voltage  $v$ . There are three independent inputs: the reference voltage  $v_{ref}$ , the power input  $v_g$ , and the load current variation  $i_{load}$ . In



**Fig. 13.18** Application of feedback theorem to buck regulator example

the small-signal model, we can employ superposition to express the output perturbation  $\hat{v}$  as a function of input perturbations  $\hat{v}_{ref}$ ,  $\hat{v}_g$ , and  $\hat{i}_{load}$ :

$$\hat{v}(s) = G_r(s)\hat{v}_{ref}(s) + G_g(s)\hat{v}_g(s) - Z_o\hat{i}_{load} \quad (13.76)$$

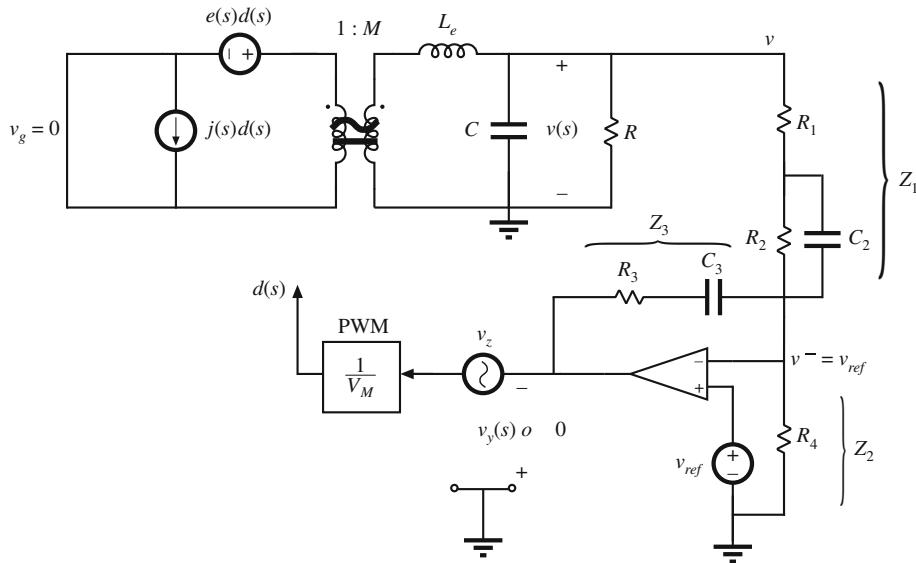
The closed-loop transfer functions  $G_r$ ,  $G_g$ , and  $Z_o$  can each be found through application of the feedback theorem, and can be expressed in the form of Eq. (13.1). Specifically, we can express Eq. (13.76) as:

$$\begin{aligned} \hat{v}(s) = & \left( G_{\infty r} \frac{T}{1+T} + G_{0r} \frac{1}{1+T} \right) \hat{v}_{ref}(s) + \left( G_{\infty g} \frac{T}{1+T} + G_{0g} \frac{1}{1+T} \right) \hat{v}_g(s) \\ & - \left( Z_{\infty o} \frac{T}{1+T} + Z_{0o} \frac{1}{1+T} \right) \hat{i}_{load} \end{aligned} \quad (13.77)$$

The terms  $G_{\infty r}$  and  $G_{0r}$  are found using the feedback theorem with  $\hat{v}_g$  and  $\hat{i}_{load}$  set to zero, and the terms  $G_{\infty g}$  and  $G_{0g}$  are found using the feedback theorem with  $\hat{v}_{ref}$  and  $\hat{i}_{load}$  set to zero. The terms  $Z_{\infty o}$  and  $Z_{0o}$  are found using the feedback theorem with  $\hat{v}_g$  and  $\hat{v}_{ref}$  set to zero. The loop gain  $T$  is found with  $\hat{v}_g$ ,  $\hat{v}_{ref}$ , and  $\hat{i}_{load}$  all set to zero. In the following analysis, the operational amplifier is treated as ideal.

The closed-loop reference-to-output ideal forward gain  $G_{\infty r}(s)$  is found with  $\hat{v}_g$  and  $\hat{i}_{load}$  set to zero and with  $\hat{v}_y$  nulled:

$$G_{\infty r}(s) = \left. \frac{\hat{v}}{\hat{v}_{ref}} \right|_{\substack{\hat{v}_g=0, \hat{i}_{load}=0 \\ \hat{v}_y \rightarrow 0}} \quad (13.78)$$

**Fig. 13.19** Determination of  $G_{\infty r}$ 

The small-signal model with these conditions is illustrated in Fig. 13.19. Nulling  $\hat{v}_y$  in the presence of  $\hat{v}_{ref}$  causes the negative input of the ideal op amp  $\hat{v}^-$  to be equal to  $\hat{v}_{ref}$ . But  $\hat{v}^-$  and  $\hat{v}$  are related according to the voltage divider ratio of the feedback network:

$$\hat{v}^- = \hat{v} \frac{Z_2 \| Z_3}{Z_2 \| Z_3 + Z_1} = \hat{v}_{ref} \quad (13.79)$$

where the error amplifier impedances are

$$Z_1 = R_1 + \left( R_2 \parallel \frac{1}{sC_2} \right) \quad (13.80)$$

$$Z_2 = R_4 \quad (13.81)$$

$$Z_3 = R_3 + \frac{1}{sC_3} \quad (13.82)$$

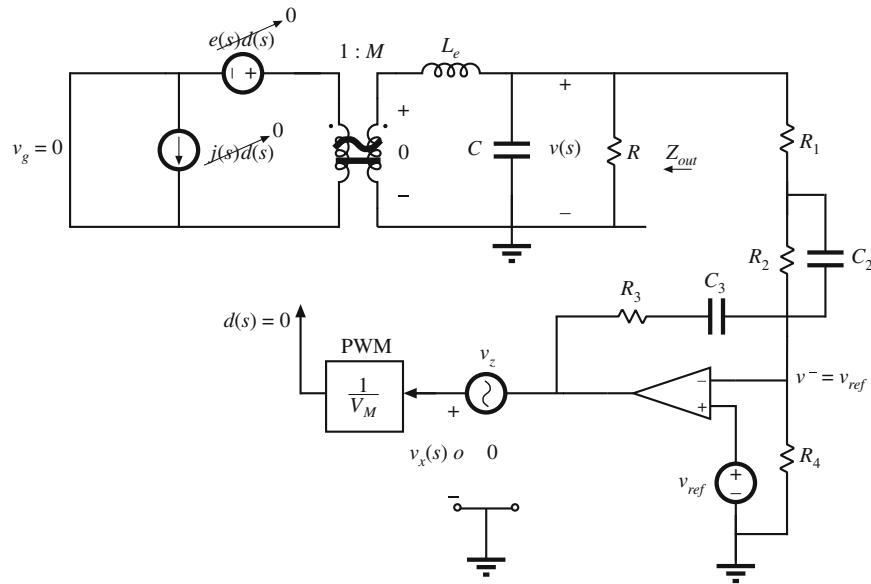
Therefore,  $G_{\infty r}$  is equal to:

$$G_{\infty r} = \frac{Z_2 \| Z_3 + Z_1}{(Z_2 \| Z_3)} \quad (13.83)$$

At dc, this gain reduces to

$$G_{\infty r}(0) = \frac{R_4 + R_1 + R_2}{R_4} \quad (13.84)$$

In a dc regulator having constant  $v_{ref}$ , the dynamics of Eq. (13.83) are irrelevant, and the ideal output voltage is equal to  $G_{\infty r}(0)V_{ref}$ . When the reference can vary, then the poles and zeroes of Eq. (13.83) may introduce significant dynamics.

Fig. 13.20 Determination of  $G_{0r}$ 

The direct forward transmission through the feedback path  $G_{0r}$  is

$$G_{0r}(s) = \frac{\hat{v}}{\hat{v}_{ref}} \Bigg|_{\begin{subarray}{l} \hat{v}_g = 0, \hat{i}_{load} = 0 \\ \hat{v}_x \rightarrow 0 \end{subarray}} \quad (13.85)$$

The small-signal model with these conditions is illustrated in Fig. 13.20. Nulling  $\hat{v}_x$  causes no amplified error signal to reach the output  $\hat{v}$  via the forward path of the loop: nulling  $\hat{v}_x$  also nulls  $\hat{d}$ , and hence the  $\hat{d}$  sources of the power stage model are also zero. As illustrated in Fig. 13.20, the secondary voltage of the ideal transformer model becomes zero.

The  $\hat{v}_{ref}$  signal can nonetheless have a small influence on the output  $\hat{v}$ . With the assumption that the op amp is ideal, its positive and negative input terminals are equal and hence  $\hat{v}^- = \hat{v}_{ref}$ . The output voltage  $\hat{v}$  is related to  $\hat{v}^- = \hat{v}_{ref}$  through the voltage divider ratio

$$\hat{v} = \hat{v}^- \frac{Z_{out}}{Z_{out} + Z_1} \quad (13.86)$$

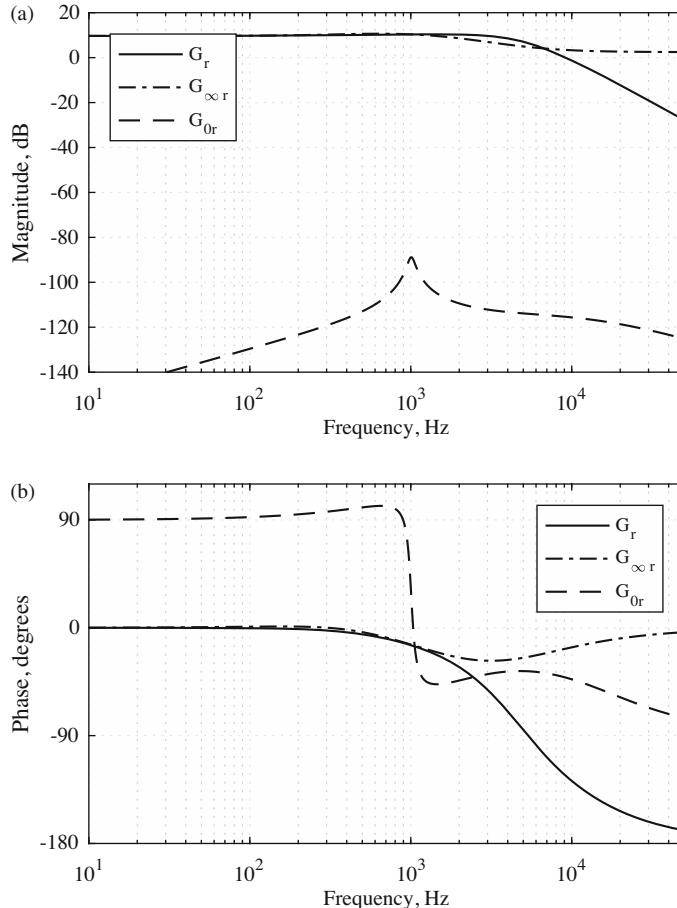
where the converter open-loop output impedance is

$$Z_{out} = R \left\| \frac{1}{sC} \right\| sL_e \quad (13.87)$$

and the feedback network impedance  $Z_1$  is given by Eq. (13.80). Hence,  $G_{0r}$  is

$$G_{0r} = \frac{Z_{out}}{Z_{out} + Z_1} \quad (13.88)$$

Thus, the direct forward transmission of the reference signal through the feedback path is nonzero.

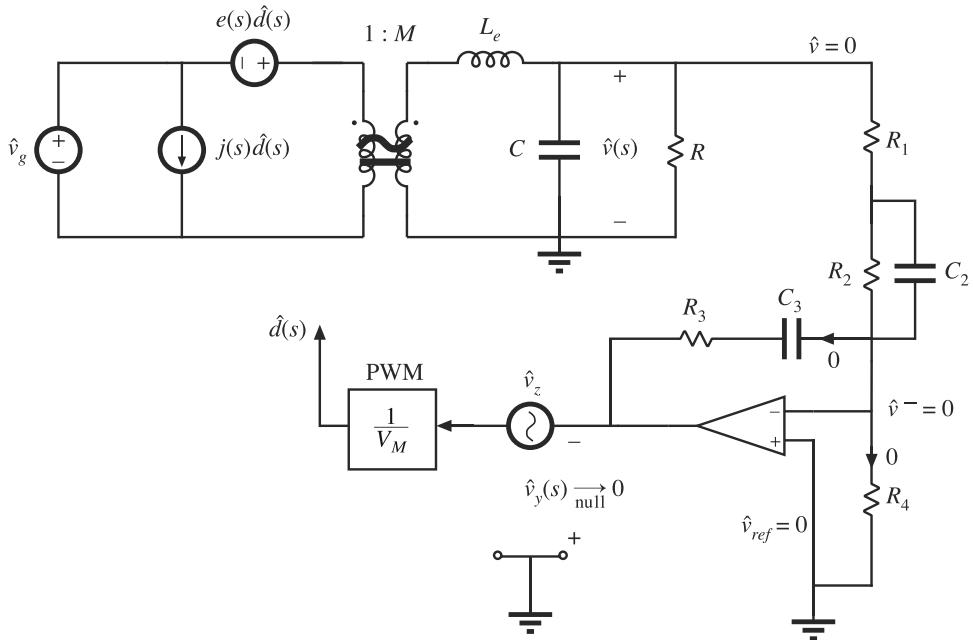


**Fig. 13.21** Magnitude and phase Bode plots of the transfer functions  $G_{\infty r}$ ,  $G_{0r}$ , and  $G_r$  for the buck regulator example. Dashed curves: ideal reference-to-output gain  $G_{\infty r}$  and direct forward transmission through feedback path  $G_{0r}$ . Solid curves: reference-to-output transfer function  $G_r$ .

Figure 13.21 contains plots of the transfer functions  $G_{\infty r}$ ,  $G_{0r}$ , and  $G_r$  for the power stage element values of Sect. 9.5.4 and the compensator circuit values of Fig. 15.29. Specifically, the power stage parameters are  $L = 50 \mu\text{H}$ ,  $C = 500 \mu\text{F}$ ,  $R = 3 \Omega$ ,  $V_g = 28 \text{ V}$ ,  $V = 15 \text{ V}$ . The compensator and feedback circuit parameters are  $V_{ref} = 5 \text{ V}$ ,  $V_M = 4 \text{ V}$ ,  $R_1 = 11 \text{ k}\Omega$ ,  $R_2 = 85 \text{ k}\Omega$ ,  $R_3 = 120 \text{ k}\Omega$ ,  $R_4 = 47 \text{ k}\Omega$ ,  $C_2 = 1.1 \text{ nF}$ ,  $C_3 = 2.7 \text{ nF}$ . It can be seen that the transfer function  $G_r(s)$  follows the ideal gain  $G_{\infty r}(s)$  from dc up to the 5 kHz bandwidth of the feedback loop, in accordance with the description of Sect. 9.2.2. The direct forward transmission term  $G_{0r}$  is small and does not influence  $G_r(s)$  at frequencies below half of the switching frequency.

The ideal forward gain from  $\hat{v}_g$  to the output  $\hat{v}$  is

$$G_{\infty g}(s) = \frac{\hat{v}}{\hat{v}_g} \Big|_{\begin{subarray}{l} \hat{v}_{ref}=0, \hat{i}_{load}=0 \\ \hat{v}_y \rightarrow 0 \end{subarray}} \quad (13.89)$$



**Fig. 13.22** Determination of  $G_{\infty g}$

The small-signal model with these conditions is illustrated in Fig. 13.22. Nulling  $\hat{v}_y$  in the presence of  $\hat{v}_{ref} = 0$  causes  $\hat{v}^-$  to be zero. Consequently the voltage across  $R_4$  and also across the  $R_3 - C_3$  branches are zero, and so there is no current through those elements. This implies that there is no current through the  $R_1 - R_2 - C_2$  branch, and hence no voltage across it either. Therefore the output voltage  $\hat{v}$  must be zero. So

$$G_{\infty g} = 0 \quad (13.90)$$

In the limit of infinite loop gain,  $\hat{v}_g$  variations do not influence the output  $\hat{v}$ .

The gain  $G_{0g}$  is the open-loop disturbance transfer function from  $\hat{v}_g$  to  $\hat{v}$ , and is defined as

$$G_{0g}(s) = \left. \frac{\hat{v}}{\hat{v}_g} \right|_{\substack{\hat{v}_{ref}=0, \hat{v}_{load}=0 \\ \hat{v}_x \rightarrow 0}} \quad (13.91)$$

The small-signal model with these conditions is illustrated in Fig. 13.23. Nulling  $\hat{v}_x$  causes  $\hat{d}$  to be zero. Consequently the voltage at the output of the dc transformer model is equal to  $M\hat{v}_g$ . The output voltage is equal to this voltage multiplied by the filter transfer function  $H_e(s)$ . So

$$G_{0g} = M H_e(s) \quad (13.92)$$

The gain  $G_{0g}$  coincides with the open-loop line-to-output transfer function  $G_{vg}(s)$ .

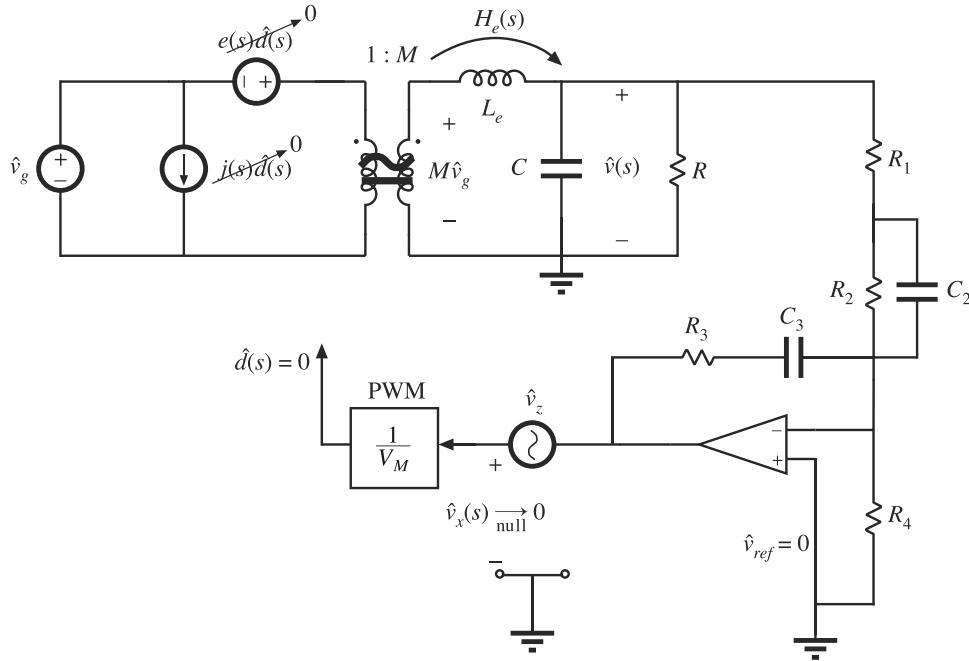


Fig. 13.23 Determination of \$G\_{0g}\$

Figure 13.24 contains plots of the transfer functions \$G\_{0g}\$ and \$G\_g\$, again for the power stage element values of Sect. 9.5.4 and the compensator circuit values of Fig. 15.29. The closed-loop line-to-output transfer function \$G\_g(s)\$ follows the open-loop disturbance transfer function \$G\_{vg} = G\_{0g}\$ above the crossover frequency of 5 kHz, as discussed in Sect. 9.2.1. Below the crossover frequency, \$G\_g\$ is reduced by the factor \$1/(1 + T)\$.

The quantity \$Z\_{\infty o}\$ is the regulator output impedance under the conditions that the feedback loop operates ideally, with zero error. \$Z\_{\infty o}\$ is defined as:

$$Z_{\infty o}(s) = -\frac{\hat{v}}{\hat{i}_{load}} \Bigg|_{\begin{array}{l} \hat{v}_{ref}=0, \hat{v}_g=0 \\ \hat{v}_x \rightarrow 0 \end{array}} \quad (13.93)$$

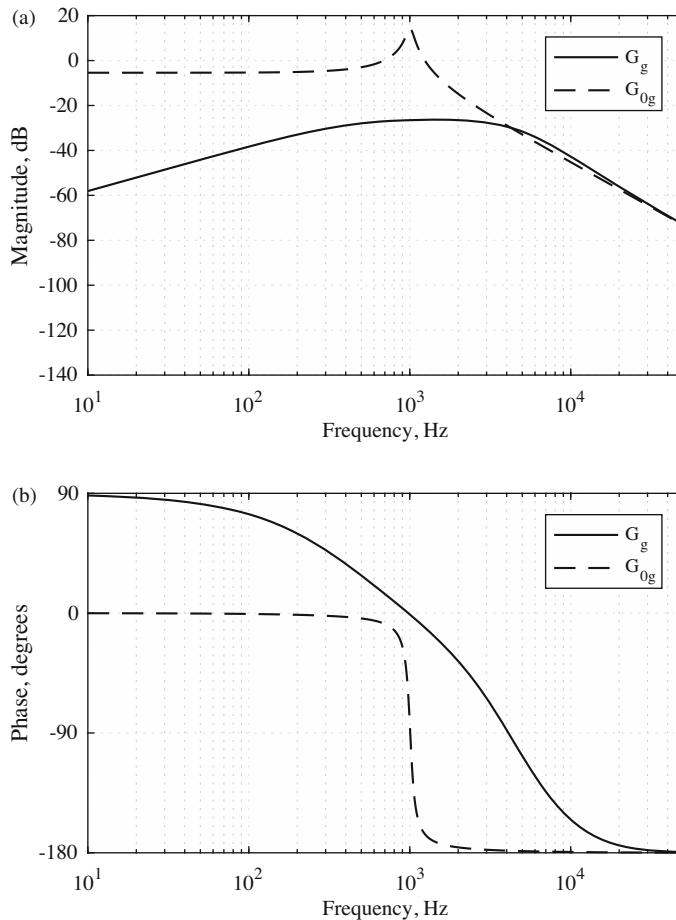
Figure 13.25 illustrates the small-signal model under these conditions. With \$\hat{v}\_{ref}\$ set to zero and with \$\hat{v}\_x\$ nulled, \$\hat{v}^-\$ is also nulled. Then there is no voltage across the elements \$R\_4\$, \$R\_3\$, or \$C\_3\$, and hence the currents through these elements are zero. Consequently the currents through the elements \$R\_1\$, \$R\_2\$, and \$C\_2\$ are zero, and hence the voltages across these elements are also nulled. Therefore \$\hat{v} = \hat{v}^- = 0\$. So the regulator ideal output impedance is

$$Z_{\infty o}(s) = -\frac{0}{\hat{i}_{load}} = 0 \quad (13.94)$$

When the regulator operates ideally, load current disturbances do not affect the output voltage.

The quantity \$Z\_{0o}\$ is the regulator output impedance under open-loop conditions, with \$\hat{v}\_x\$ set to zero. \$Z\_{0o}\$ is defined as:

$$Z_{0o}(s) = -\frac{\hat{v}}{\hat{i}_{load}} \Bigg|_{\begin{array}{l} \hat{v}_{ref}=0, \hat{v}_g=0 \\ \hat{v}_x=0 \end{array}} \quad (13.95)$$



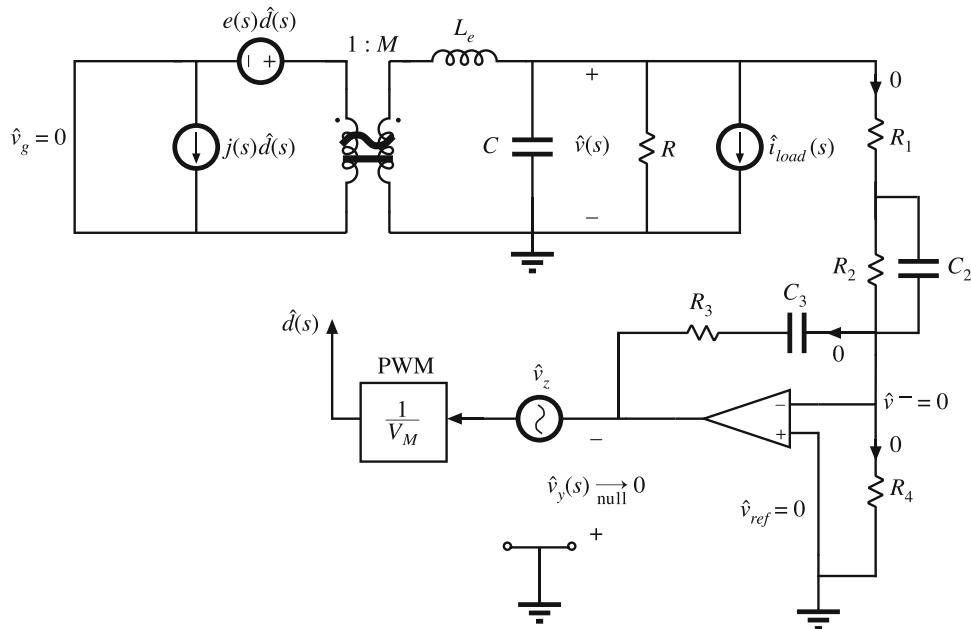
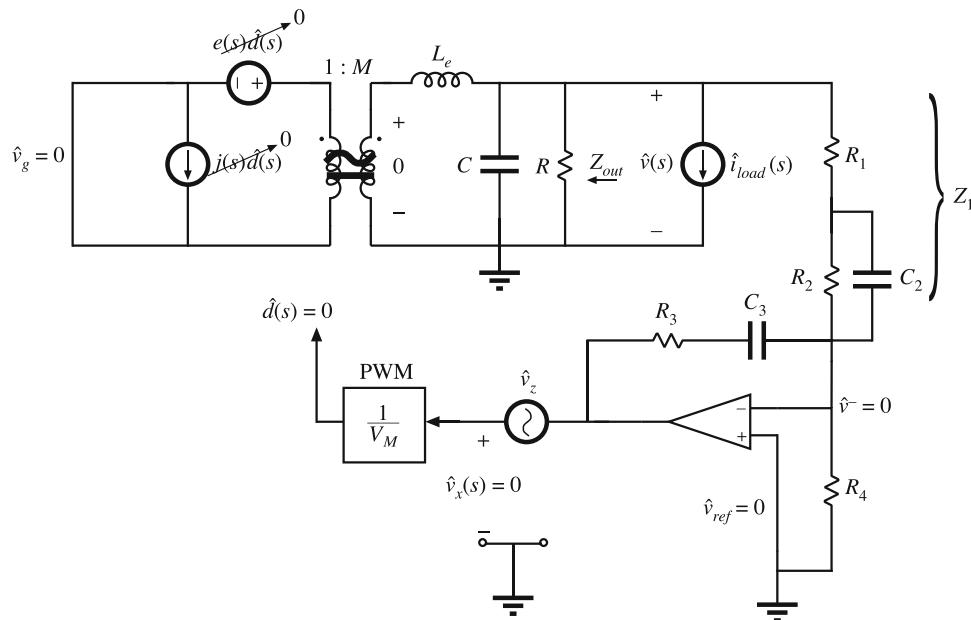
**Fig. 13.24** Magnitude and phase Bode plots of the transfer functions  $G_{0g}$  and  $G_g$  for the buck regulator example. Dashed curves: disturbance transfer function  $G_{0g} = G_{vg}$ . Solid curves: closed-loop line-to-output transfer function  $G_g$

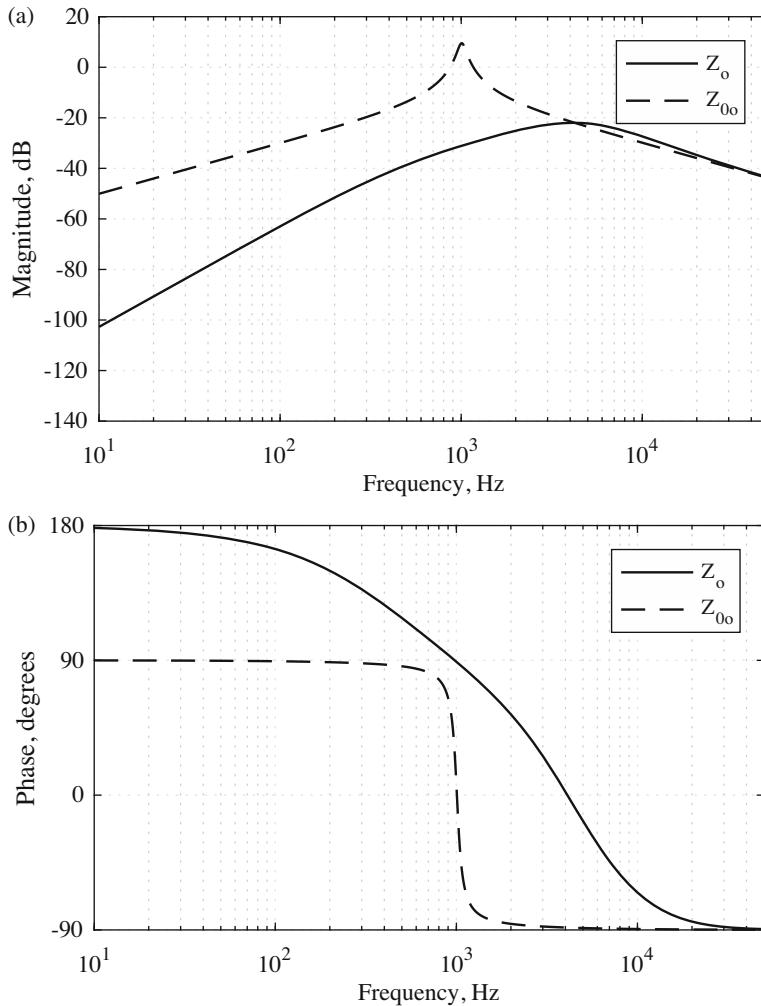
Figure 13.26 illustrates the small-signal model under these conditions. With  $\hat{v}_{ref}$  set to zero and with  $\hat{v}_x$  set to zero,  $\hat{d}$  is zero and the transformer voltage is zero. Since  $\hat{v}_{ref}$  is zero,  $\hat{v}^- = 0$ . The output impedance is then

$$Z_{0o}(s) = -\frac{\hat{v}}{\hat{i}_{load}} = Z_{out} \parallel Z_1 \quad (13.96)$$

where  $Z_{out}$  is the power stage output impedance given by Eq. (13.87) and  $Z_1$  is the feedback network impedance given by Eq. (13.80). In the usual case where  $Z_{out}$  is much smaller than  $Z_1$ , this expression reduces to  $Z_{out}$ .

Figure 13.27 contains plots of the transfer functions  $Z_{0o}$  and  $Z_o$  for the power stage element values of Sect. 9.5.4 and the compensator circuit values of Fig. 15.29. The closed-loop output impedance  $Z_o(s)$  follows the open-loop output impedance  $Z_{out} = Z_{0o}$  above the crossover frequency of 5 kHz, as discussed in Sect. 9.2.1. Below the crossover frequency,  $Z_o$  is reduced by the factor  $1/(1 + T)$  relative to  $Z_{out}$ .

Fig. 13.25 Determination of ideal output impedance  $Z_{\infty}$ Fig. 13.26 Determination of open-loop output impedance  $Z_0$

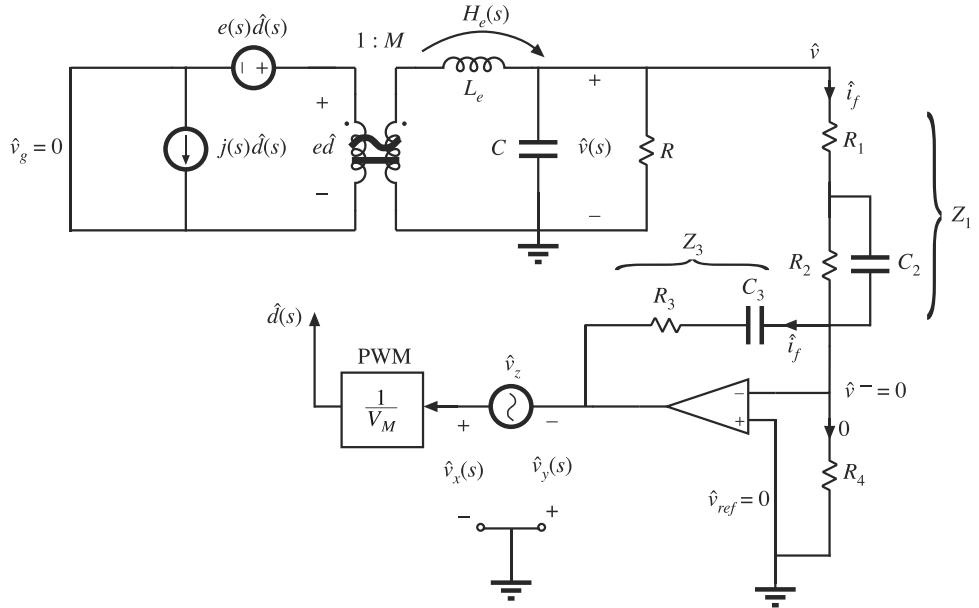


**Fig. 13.27** Magnitude and phase Bode plots of the transfer functions  $Z_{0o}$  and  $Z_o$  for the buck regulator example. Dashed curves: disturbance transfer function  $Z_{0o} = Z_{out}$ . Solid curves: closed-loop line-to-output transfer function  $Z_o$

The loop gain  $T(s)$  is

$$T(s) = \left. \frac{\hat{v}_y}{\hat{v}_x} \right|_{\begin{subarray}{l} \hat{v}_{ref}=0, \hat{i}_{load}=0 \\ \hat{v}_g=0 \end{subarray}} \quad (13.97)$$

The small-signal model with these conditions is illustrated in Fig. 13.28. To find  $T(s)$ , we begin with the signal  $\hat{v}_x$ , and find how it propagates around the loop to the  $\hat{v}_y$  point. Under these conditions, the output voltage  $\hat{v}$  is equal to  $\hat{v}_x$  multiplied by the PWM gain ( $1/V_M$ ) and by the converter control-to-output gain  $G_{vd}(s)$ .

**Fig. 13.28** Determination of loop gain  $T(s)$ 

$$\hat{v} = G_{vd}(s) \left( \frac{1}{V_M} \right) \hat{v}_x \quad (13.98)$$

By solution of the model of Fig. 13.28, the power stage control-to-output transfer function is

$$G_{vd}(s) = e(s) M H_e(s) \quad (13.99)$$

with  $H_e(s)$  equal to the transfer function of the canonical model  $L_e-C$  output filter.

With  $\hat{v}_{ref}$  set to zero, the ideal op amp causes  $\hat{v}^- = 0$ , and hence there is no current through  $R_4$ . The transfer function from  $\hat{v}$  to  $\hat{v}_y$  is given by the inverting amplifier formula:

$$\frac{\hat{v}_y}{\hat{v}} = \frac{Z_3}{Z_1} \quad (13.100)$$

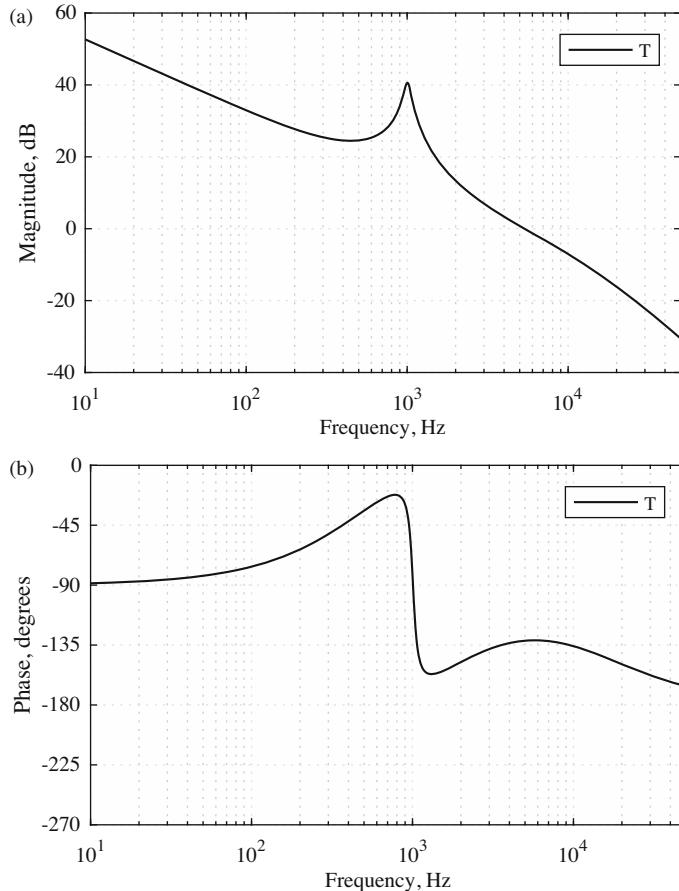
where  $Z_1$  is given by Eq. (13.80) and  $Z_3$  is given by Eq. (13.82). The loop gain is the product of Eqs. (13.98) and (13.100):

$$T(s) = G_{vd}(s) \left( \frac{1}{V_M} \right) \left( \frac{Z_3}{Z_1} \right) \quad (13.101)$$

Figure 13.29 contains plots of the loop gain  $T(s)$  for the power stage element values of Sect. 9.5.4 and the compensator circuit values of Fig. 15.29.

In summary, the closed-loop transfer function from the reference  $\hat{v}_{ref}$  to the output  $\hat{v}$  is

$$G_r(s) = \frac{Z_2 \| Z_3}{Z_1 + (Z_2 \| Z_3)} \frac{T}{1+T} + \frac{Z_{out}}{Z_1 + Z_{out}} \frac{1}{1+T} \quad (13.102)$$



**Fig. 13.29** Magnitude and phase Bode plots of the loop gain  $T(s)$  for the buck regulator example

The closed-loop transfer function from input voltage disturbances  $\hat{v}_g$  to the output  $\hat{v}$  is

$$G_g(s) = \frac{MH_e}{1 + T} \quad (13.103)$$

The closed-loop output impedance is

$$Z_o = \frac{Z_{out} \| Z_1}{1 + T} \quad (13.104)$$

with  $T$  given by Eq. (13.101). The canonical model parameters of Table 7.1 for the buck converter are substituted as appropriate into the above expressions.

This closed-loop regulator example includes three independent sources: the reference  $\hat{v}_{ref}$  and disturbances  $\hat{v}_g$  and  $\hat{i}_{load}$ . Superposition is employed to apply the feedback theorem three times, once for each independent input, and we find a  $G_0$  and  $G_\infty$  term associated with each source. The  $G_{\infty r}$  term has the physical interpretation of the ideal closed-loop gain from the

reference to the output, and corresponds to the  $1/H$  term identified in Sect. 9.2.2. The  $G_{0r}$  term has the physical interpretation of direct forward transmission from  $\hat{v}_{ref}$  through the feedback path to the output. The disturbance transfer function  $G_{0g}$  is the open-loop line-to-output transfer function, and coincides with  $G_{vg}(s)$  of the open-loop converter. In this example,  $G_{\infty g}$  is zero: when the feedback loop operates ideally, no  $\hat{v}_g$  disturbances reach the output.

The feedback theorem provides a general way to define and determine the loop gain  $T$ . Although we have found three closed-loop transfer functions from the three independent sources to the output, there is a single physical feedback loop in the system, and a single expression for the loop gain.

## 13.5 Summary of Key Points

1. The Feedback Theorem employs null double injection and linear superposition to determine closed-loop gains and other important transfer functions of a feedback circuit, without need to break the circuit into blocks that are noninteracting and unidirectional. An ideal injection point is identified, and then certain “thought experiments” are performed that lead to derivation of analytical expressions for the important transfer functions of the closed-loop circuit.
2. A given closed-loop gain  $G(s)$  is expressed in terms of an ideal gain  $G_\infty$  (the limiting transfer function with infinite loop gain), a gain  $G_0$  (the limiting transfer function for zero loop gain), and the loop gain  $T$ . The Feedback Theorem provides a simplified framework for deriving these quantities.
3. An operational amplifier circuit intended for use as a PD compensator is analyzed using the Feedback Theorem. In this example, the  $G_\infty$  gain is found to be the transfer function when the op amp is ideal. The  $G_0$  gain arises from direct forward transmission of the input signal through the feedback path. The actual transfer function  $G$  is found to deviate significantly from  $G_\infty$  at high frequencies where the op amp has insufficient internal gain; this can significantly degrade the behavior of the PD compensator.
4. A closed-loop buck converter with PID compensator circuit is analyzed via the Feedback Theorem, to derive the closed-loop transfer functions from the reference input and line input to the output, as well as the closed-loop output impedance. This example illustrates how the Feedback Theorem is useful for analyzing closed-loop disturbance transfer functions as well as the reference-to-output transfer function.

## PROBLEMS

- 13.1** A feedback amplifier is shown in Fig. 13.30 including voltage injection  $v_z$  suitable for application of the Feedback Theorem. The objective in this problem is to solve for the amplifier gain

$$G = \left. \frac{v_o}{v_i} \right|_{v_z=0}$$

using the Feedback Theorem. Derive expressions for  $G_\infty$ ,  $T$ ,  $G_0$ , and  $T_n$ , and show that the reciprocity relationship holds. Your expressions should be in terms of the circuit parameter values  $R_1$ ,  $R_2$ ,  $C$ ,  $R_o$ ,  $A_o$ .

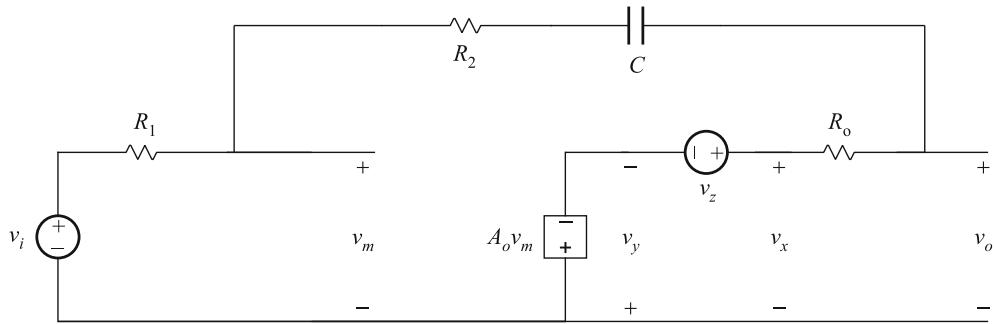


Fig. 13.30 Feedback amplifier of Problem 13.1

- 13.2** A feedback amplifier is shown in Fig. 13.31 including current injection \$i\_z\$ suitable for application of the Feedback Theorem. The objective in this problem is to solve for the amplifier gain

$$G = \left. \frac{v_o}{v_i} \right|_{i_z=0}$$

using the Feedback Theorem. Derive expressions for \$G\_\infty\$, \$T\$, \$G\_0\$, and \$T\_n\$, and show that the reciprocity relationship holds. Your expressions should be in terms of the circuit parameter values \$R\_1\$, \$C\$, and \$g\_m\$.

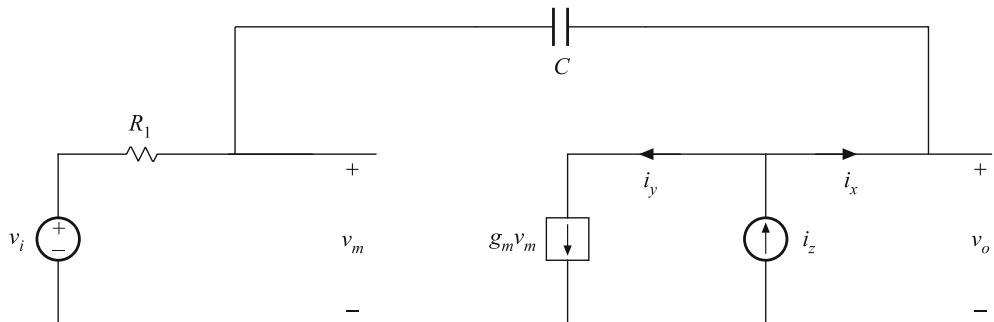
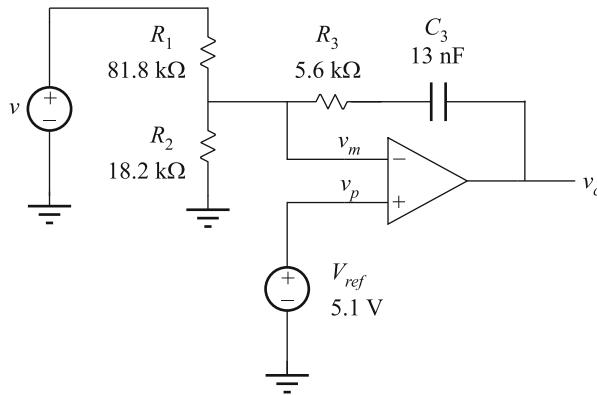


Fig. 13.31 Feedback amplifier of Problem 13.2

- 13.3** Figure 13.32 shows a PI compensator circuit in the closed-loop switching voltage regulator of Problem 9.5. The PI compensator is constructed around an op amp provided in a standard PWM controller chip. The input to the compensator is the regulator output voltage \$v\$, and the output of the compensator is voltage \$v\_c\$. The reference voltage \$V\_{ref}\$ is constant. The purpose of this problem is to show how the Feedback Theorem can be used in the design of the PI compensator circuit. The closed-loop transfer function of interest is

$$G(s) = \left. \frac{\hat{v}_c}{\hat{v}} \right|_{\hat{v}_{ref}=0}$$



**Fig. 13.32** PI compensator constructed around a transconductance amplifier, Problem 13.3

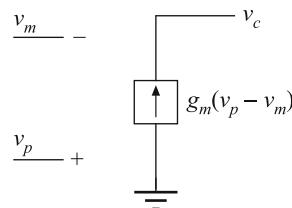
- (a) Assuming the op amp in Fig. 13.32 is ideal, show that

$$G_\infty(s) = \left. \frac{\hat{v}_c}{\hat{v}} \right|_{\text{ideal op-amp}} = G_{\infty\infty} \left( 1 + \frac{\omega_1}{s} \right)$$

and derive expressions for the salient features of  $G_\infty(s)$  in terms of  $R_1$ ,  $R_2$ ,  $R_3$ ,  $C_3$ . Compute the numerical values for  $G_{\infty\infty}$  and  $f_1$ . Note that the assumption that the op amp is ideal (in a negative-feedback circuit) is equivalent to the assumption that the error signal is nulled in the Feedback Theorem terms. Hence, the transfer function found in this part of the problem is equal to  $G_\infty$  of the Feedback Theorem.

Assuming  $G(s) \approx G_\infty(s)$ , the closed-loop voltage regulator shown in Problem 9.5 should be stable with adequate phase margin. A designer made this assumption, built the circuit, and expected to obtain stable operation with well regulated output voltage. In lab experiments, however, the switched-mode voltage regulator is found to be unstable, producing oscillating voltages and currents. Knowing that you are familiar with the Feedback Theorem, the designer asks you for assistance.

Looking through the PWM controller datasheet, you realize that the op amp provided is not really a standard op amp with a large voltage gain and a low output impedance but instead a *transconductance amplifier*, which can be modeled as a controlled current source, as shown in Fig. 13.33.



**Fig. 13.33** Model of the transconductance amplifier in Problem 13.3

Furthermore, you find that the transconductance  $g_m$  of the amplifier can be as low as  $g_{mmin} = 100 \mu\text{A/V}$  and as high as  $g_{mmax} = 1 \text{ mA/V}$  due to process and temperature variations. You realize that the problem is well suited for application of the Feedback Theorem and you proceed in several steps to address the stability problem encountered by the designer.

- (b) Using the current injection technique, find analytical expressions for  $G_o$ ,  $T$ , and  $T_n$  in the PI compensator of Fig. 13.32, taking into account the amplifier model shown in Fig. 13.33. Express the transfer functions in the standard factored pole-zero forms, and derive expressions for the salient features in terms of  $R_1$ ,  $R_2$ ,  $R_3$ ,  $C_3$ , and  $g_m$ . Show that the reciprocity relationship holds.
- (c) Using the results of part (b), derive an expression for the closed-loop transfer function  $G(s)$ , and show that  $G(s)$  can be written as

$$G(s) = \frac{\hat{v}_c}{\hat{v}} \Big|_{\hat{v}_{ref}=0} = G'_{\infty\infty} \left( 1 + \frac{\omega'_1}{s} \right)$$

Calculate and put in a table numerical values for  $G'_{\infty\infty}$  and  $\omega'_1$  for the two extreme values of  $g_m$ ,  $g_{mmin}$  and  $g_{mmax}$ , and compare these values to  $G_{\infty\infty}$  and  $f_1$  found in part (a). Explain why the switched-mode voltage regulator using the compensator of Fig. 13.32 may become unstable.

- (d) Suggest how to change the component values in the PI compensator in Fig. 13.32 so that  $G_\infty(s)$  remains the same as found in part (a), and so that the compensator gain  $G(s)$  closely approximates the ideal  $G_\infty(s)$  for all possible values of the transconductance  $g_m$ .

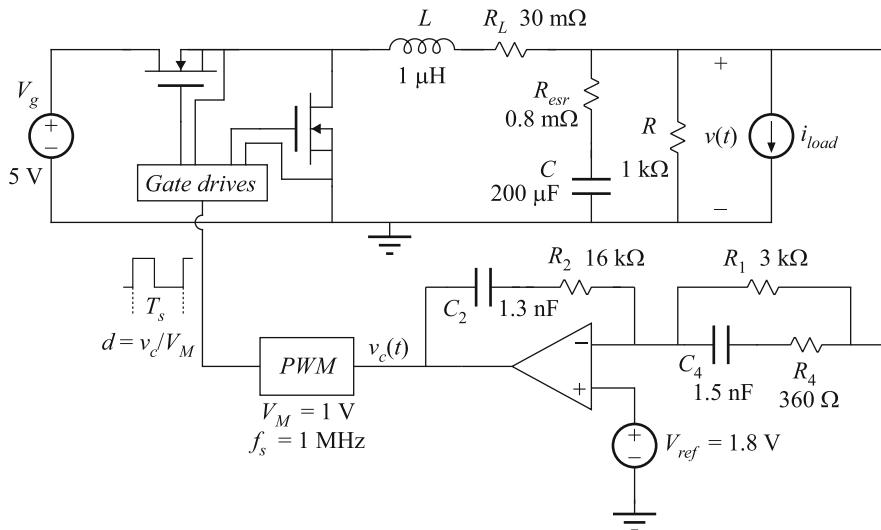
**13.4** A model of an op amp is shown in Fig. 13.7b. In the model,  $R_o = 100 \Omega$ , and

$$G_{op}(s) = A_o \frac{1}{\left( 1 + \frac{s}{\omega_1} \right) \left( 1 + \frac{s}{\omega_2} \right)}$$

where  $A_o = 10^5 \rightarrow 100 \text{ dB}$ ,  $f_1 = 10 \text{ Hz}$ , and  $f_2 = 1 \text{ MHz}$ .

- a) The op amp is used to construct closed-loop amplifiers with three different ideal closed-loop gains: (i)  $G_\infty = 1$ ,  $G_\infty = -1$ , and (iii)  $G_\infty = 10$ . Sketch circuit diagrams of these three closed-loop amplifiers and choose resistance values.
- b) For each of the closed-loop amplifiers considered in part (a), sketch the magnitude and phase responses of the loop gain  $T(s)$  and determine numerical values for the crossover frequency and the phase margin.
- c) For each of the closed-loop amplifiers considered in part (a), derive an expression for the closed-loop gain  $G(s)$  using the Feedback Theorem. Your expression should be in the standard normalized form. Sketch the magnitude and phase responses and annotate the plots with salient features of  $G(s)$ .

**13.5** A point-of-load (POL) voltage regulator using a synchronous buck converter is shown in Fig. 13.34. Losses can be neglected except for the losses due to the inductor resistance  $R_L$  and the capacitor equivalent series resistance  $R_{esr}$ . The PID compensator is constructed around an op amp. In this problem, you may assume that the op amp has ideal characteristics. The pulse-width modulator has a very large input resistance, so that a voltage injection source  $\hat{v}_z$  can be ideally inserted between the compensator and the PWM.



**Fig. 13.34** Synchronous buck voltage regulator with a PID compensator, Problems 13.5 and 13.6

- Derive an expression for the loop gain  $T(s)$ . The expression should be in standard normalized form. Salient features of  $T(s)$  should be expressed in terms of the circuit parameters shown in Fig. 13.34. Plot the magnitude and phase responses of the loop gain, and determine numerical values for the crossover frequency  $f_c$  and the phase margin  $\varphi_m$ .
- In this part of the problem, the objective is to determine the closed-loop output impedance  $Z_o(s) = -\hat{v}/\hat{i}_{load}$  of the POL voltage regulator using the Feedback Theorem. Derive expressions for  $Z_{\infty o}$ ,  $Z_{0o}$ , and the null loop gain  $T_{nz}$  in standard normalized forms. Show that the reciprocity relationship holds. Plot the magnitude and phase responses of  $Z_o(s)$ .
- In this part of the problem, the objective is to determine the closed-loop line-to-output transfer function  $G_g(s) = \hat{v}/\hat{v}_g$  using the Feedback Theorem. Derive expressions for  $G_{\infty g}$ ,  $G_{0g}$ , and the null loop gain  $T_{ng}$  in standard normalized forms. Show that the reciprocity relationship holds. Plot the magnitude and phase responses of  $G_g(s)$ .
- In this part of the problem, the objective is to determine the closed-loop reference-to-output response  $G_r(s) = \hat{v}/\hat{v}_{ref}$  using the Feedback Theorem. Derive expressions for  $G_{\infty r}$ ,  $G_{0r}$ , and the null loop gain  $T_{nr}$  in standard normalized forms. Show that the reciprocity relationship holds. Plot the magnitude and phase responses of  $G_r(s)$ .
- Modify the PID compensator circuit so that  $T(s)$  remains exactly the same as found in part (a), and so that the ideal reference-to-output response has unity gain at all frequencies, *i.e.*, so that  $G_{\infty r} = 1$ .

**13.6** A model of the op amp used to construct the PID compensator in the voltage regulator of Fig. 13.34 is shown in Fig. 13.7b. In the model,  $R_o = 0$ , and

$$G_{op}(s) = \frac{\omega_{GBW}}{s}$$

where  $f_{GBW}$  is the unity gain frequency, also referred to as the *gain-bandwidth product* of the op amp. The objective in this problem is to examine how finite  $f_{GBW}$  of the op amp affects closed-loop performance of the voltage regulator in Fig. 13.34. The transfer function of interest is the PID compensator gain

$$G_c(s) = -\frac{\hat{v}_c}{\hat{v}}$$

- a) For the closed-loop amplifier that implements the PID compensator, derive expressions for the loop gain  $T_c(s)$ , the ideal forward gain  $G_{c\infty}$ , and the direct forward transmission  $G_{c0}$ . The expressions should be in terms of the circuit parameters shown in Fig. 13.34 and  $\omega_{GBW}$ . Overlay Bode plots of the magnitude and phase of  $G_c$  for three different values of  $f_{GBW}$ : (i)  $f_{GBW} = 1$  MHz, (ii)  $f_{GBW} = 10$  MHz, and (iii)  $f_{GBW} = 25$  MHz.
  - b) Consider loop gain  $T(s)$  in the voltage regulator of Fig. 13.34, taking into account  $G_c(s)$  found in part (a). Overlay Bode plots of the magnitude and phase of  $T(s)$  for the three different values of  $f_{GBW}$  considered in part (a). For each  $f_{GBW}$ , calculate numerical values of the crossover frequency  $f_c$  and the phase margin  $\varphi_m$ , and compare to the results obtained assuming an ideal op amp, *i.e.*, assuming that  $G_c = G_{c\infty}$ . Comment on how large the gain-bandwidth product of the op amp should be so that the impact on the closed-loop performance of the voltage regulator in Fig. 13.34 can be neglected.
- 13.7** Do Problem 9.7. Verify the result for the closed-loop transfer function  $\hat{i}_g(s)/\hat{v}_{ref}(s)$  using the Feedback Theorem. Then, using the Feedback Theorem, derive an expression for the closed-loop input admittance
- $$Y_g = \frac{\hat{i}_g}{\hat{v}_g}$$
- Plot the magnitude and phase responses of  $Y_g$ . In what range of frequencies is the magnitude of  $Y_g$  approximately equal to the ideal  $Y_{g\infty}$ .
- 13.8** Do Problem 9.8. Then find the closed-loop output impedance  $Z_o$  using the Feedback Theorem and verify that the specifications are met: magnitude of the closed-loop output impedance should be less than  $0.2 \Omega$  over the entire frequency range 0 to 20 kHz.
- 13.9** Do Problem 9.9. Then, using the Feedback Theorem, derive an expression for the closed-loop reference-to-output response  $G_r = \hat{v}/\hat{v}_{ref}$ . Plot the magnitude and phase responses of  $G_r$ . Over what range of frequencies is the magnitude of  $G_r$  approximately equal to the ideal  $G_{r\infty}$ ?



## Circuit Averaging, Averaged Switch Modeling, and Simulation

Circuit averaging is another well-known technique for derivation of converter equivalent circuits. Rather than averaging the converter state equations, with the circuit averaging technique we average the converter waveforms directly. All manipulations are performed on the circuit diagram, instead of on its equations, and hence the circuit averaging technique gives a more physical interpretation to the model. Since circuit averaging involves averaging and small-signal linearization, it is equivalent to state-space averaging. However, in many cases circuit averaging is easier to apply, and allows the small-signal ac model to be written almost by inspection. The circuit averaging technique can also be applied directly to a number of different types of converters and switch elements, including phase-controlled rectifiers, PWM converters operated in discontinuous conduction mode or with current programming, and quasi-resonant converters—these are described in later chapters. However, in other cases it may lead to involved models that are less easy to analyze and understand. To overcome this problem, the circuit averaging and state-space averaging approaches can be combined. Circuit averaging was developed before state-space averaging, and is described in [16]. Because of its generality, there was a later resurgence of interest in circuit averaging of switch networks [70–76, 108].

The techniques of circuit averaging and averaged switch modeling are developed in Sect. 14.1. These techniques are employed to model SEPIC and boost converter examples, and both dc and small-signal ac converter models are developed.

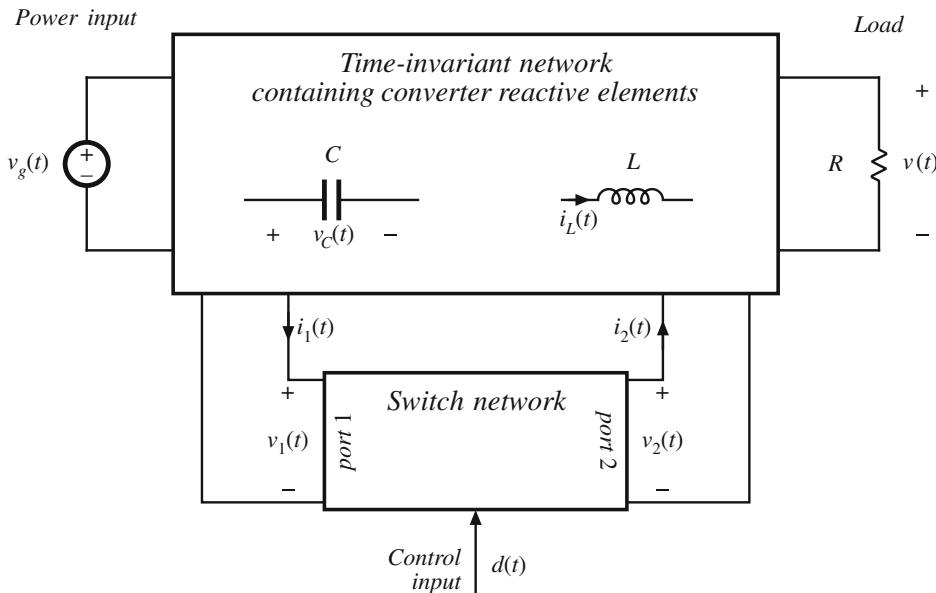
The averaged switch model also exposes the fundamental energy conversion process by which a switched-mode circuit can convert power from one voltage to another with high efficiency: dc or low-frequency ac is converted (inverted) to high-frequency ac by the switching of the PWM transistor. This ac power is then converted back (rectified) to dc or low-frequency ac by the diode or other switching element. This power is called the *indirect power* that flows within the converter. Indirect power and its relationship to the averaged switch model is discussed in Sect. 14.1.4.

The averaged switch model lends itself well to simulation. When the semiconductor switches are replaced with an averaged switch model, circuit simulation programs such as SPICE are able to plot small-signal ac transfer functions of switching converter systems. This is a very useful application of the averaged switch modeling approach. SPICE simulation of converters operating in the continuous conduction mode is developed in Sect. 14.3. Averaged switch modeling of converters operating in the discontinuous conduction mode is developed in Chap. 15, along with averaged simulations of DCM.

## 14.1 Circuit Averaging and Averaged Switch Modeling

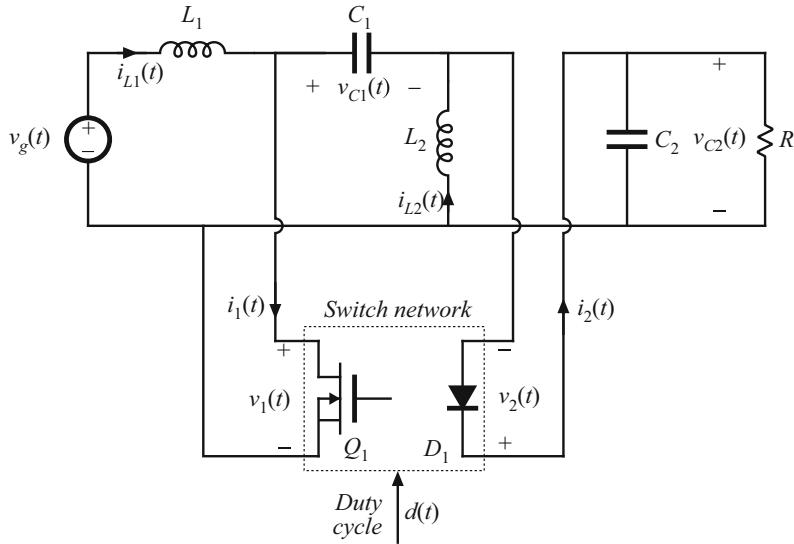
The key step in circuit averaging is to replace the converter switches with voltage and current sources, to obtain a time-invariant circuit topology. The waveforms of the voltage and current generators are defined to be identical to the switch waveforms of the original converter. Once a time-invariant circuit network is obtained, then the converter waveforms can be averaged over one switching period to remove the switching harmonics. Any nonlinear elements in the averaged circuit model can then be perturbed and linearized, leading to the small-signal ac model.

In Fig. 14.1, the switching elements are separated from the remainder of the converter. The converter therefore consists of a switch network containing the converter switching elements, and a time-invariant network containing the reactive and other remaining elements. Figure 14.1 illustrates the simple case in which there are two single-pole single-throw (SPST) switches; the switches can then be represented using a two-port network. In more complicated systems containing multiple transistors or diodes, such as in polyphase converters, the switch network may contain more than two ports.

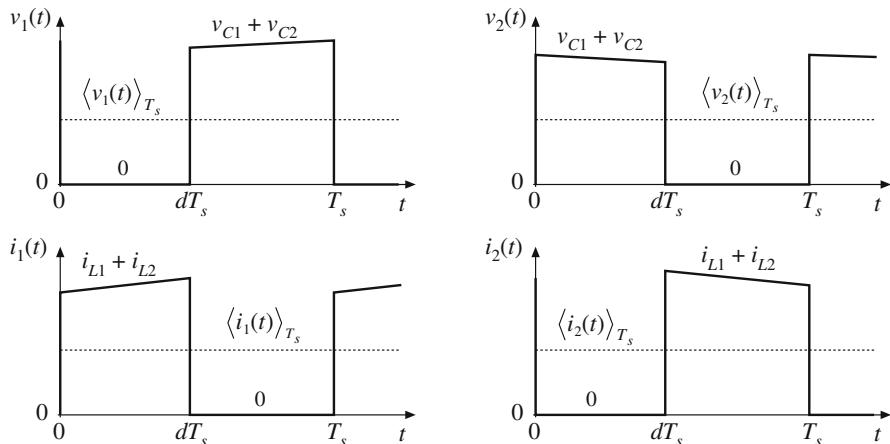


**Fig. 14.1** A switching converter can be viewed as a switch network connected to a time-invariant network

The central idea of the *averaged switch modeling* approach is to find an averaged circuit model for the switch network. The resulting averaged switch model can then be inserted into the converter circuit to obtain a complete averaged circuit model of the converter. An important advantage of the averaged switch modeling approach is that the same model can be used in many different converter configurations. It is not necessary to rederive an averaged circuit model for each particular converter. Furthermore, in many cases, the averaged switch model simplifies



**Fig. 14.2** Schematic of the SEPIC, arranged in the form of Fig. 14.1



**Fig. 14.3** Switch network terminal waveforms in the CCM SEPIC

converter analysis and yields good intuitive understanding of the converter steady-state and dynamic properties.

The first step in the process of finding an averaged switch model for a switch network is to sketch the converter in the form of Fig. 14.1, in which a switch network containing only the converter switching elements is explicitly defined. The CCM SEPIC example shown in Fig. 14.2 is used to illustrate the process. There is usually more than one way to define the two ports of the switch network; a natural way to define the two-port switch network of the SEPIC is illustrated in Fig. 14.2. The switch network terminal waveforms  $v_1(t)$ ,  $i_1(t)$ ,  $v_2(t)$ , and  $i_2(t)$  are illustrated

in Fig. 14.3 for CCM operation. Note that it is not necessary that the ports of the switch network be electrically connected within the switch network itself. Furthermore, there is no requirement that any of the terminal voltage or current waveforms of the switch network be nonpulsating.

### 14.1.1 Obtaining a Time-Invariant Circuit

The next step of the circuit averaging technique is to replace the switch network with dependent voltage and current sources, so that the circuit connections do not vary in time. The switch network defined in the SEPIC is shown in Fig. 14.4a. As with any two-port network, two of the four terminal voltages and currents can be taken as independent inputs to the switch network. The remaining two voltages and/or currents are viewed as dependent outputs of the switch network. In general, the choice of independent inputs is arbitrary, as long as the inputs can indeed be independent in the given converter circuit. For CCM operation, one can choose one terminal current and one terminal voltage as the independent inputs. For this example, let us select  $i_1(t)$  and  $v_2(t)$  as the switch network independent inputs. In addition, the duty cycle  $d(t)$  is the independent control input. Hence the dependent outputs are taken to be  $v_1(t)$  and  $i_2(t)$ .

In Fig. 14.4b, the ports of the switch network are replaced by dependent voltage and current sources. The waveforms of these dependent sources are defined to be identical to the actual dependent outputs  $v_1(t)$  and  $i_2(t)$  given in Fig. 14.3. Since all waveforms in Fig. 14.4b match the waveforms of Figs. 14.4a and 14.3, the circuits are electrically equivalent. So far, no approximations have been made.

### 14.1.2 Circuit Averaging

The next step is determination of the average values of the switch network terminal waveforms in terms of the converter state variables (inductor currents and capacitor voltages) and the converter independent inputs (such as the input voltage and the transistor duty cycle). The basic assumption is made that the natural time constants of the converter network are much longer than the switching period  $T_s$ . This assumption coincides with the requirement for small switching ripple. One may average the waveforms over a time interval which is short compared to the system natural time constants, without significantly altering the system response [16]. Hence, when the basic assumption is satisfied, it is a good approximation to average the converter waveforms over the switching period  $T_s$ . The resulting averaged model predicts the low-frequency behavior of the system, while neglecting the high-frequency switching harmonics. In the SEPIC example, by use of the usual small-ripple approximation, the average values of the switch network terminal waveforms of Fig. 14.3 can be expressed in terms of the independent inputs and the state variables as follows:

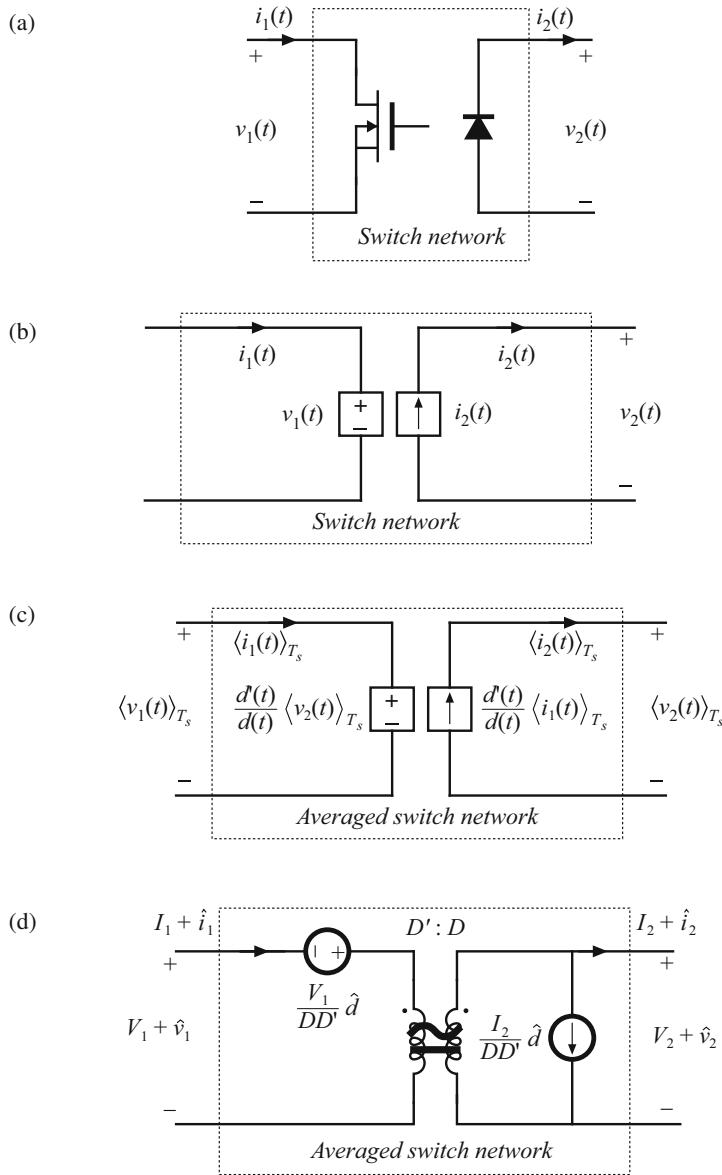
$$\langle v_1(t) \rangle_{T_s} = d'(t) (\langle v_{C1}(t) \rangle_{T_s} + \langle v_{C2}(t) \rangle_{T_s}) \quad (14.1)$$

$$\langle i_1(t) \rangle_{T_s} = d(t) (\langle i_{L1}(t) \rangle_{T_s} + \langle i_{L2}(t) \rangle_{T_s}) \quad (14.2)$$

$$\langle v_2(t) \rangle_{T_s} = d(t) (\langle v_{C1}(t) \rangle_{T_s} + \langle v_{C2}(t) \rangle_{T_s}) \quad (14.3)$$

$$\langle i_2(t) \rangle_{T_s} = d'(t) (\langle i_{L1}(t) \rangle_{T_s} + \langle i_{L2}(t) \rangle_{T_s}) \quad (14.4)$$

We have selected  $\langle i_1(t) \rangle_{T_s}$  and  $\langle v_2(t) \rangle_{T_s}$  as the independent inputs of the averaged switch network. The dependent outputs of the averaged switch network are then  $\langle i_2(t) \rangle_{T_s}$  and  $\langle v_1(t) \rangle_{T_s}$ . The next step is to express, if possible, the switch network dependent outputs  $\langle i_2(t) \rangle_{T_s}$  and  $\langle v_1(t) \rangle_{T_s}$  as



**Fig. 14.4** Derivation of the averaged switch model for the CCM SEPIC: (a) switch network; (b) switch network where the switches are replaced with dependent sources whose waveforms match the switch terminal dependent waveforms; (c) large-signal, nonlinear averaged switch model obtained by averaging the switch network terminal waveforms in (b); (d) dc and ac small-signal averaged switch model

functions *solely* of the switch network independent inputs  $\langle i_1(t) \rangle_{T_s}$ ,  $\langle v_2(t) \rangle_{T_s}$ , and the control input  $d(t)$ . In this step, the averaged switch outputs should not be written as functions of other converter signals such as  $\langle v_g(t) \rangle_{T_s}$ ,  $\langle v_{C1}(t) \rangle_{T_s}$ ,  $\langle v_{C2}(t) \rangle_{T_s}$ ,  $\langle i_{L1}(t) \rangle_{T_s}$ ,  $\langle i_{L2}(t) \rangle_{T_s}$ , etc.

We can use Eqs. (14.2) and (14.3) to write

$$\langle i_{L1}(t) \rangle_{T_s} + \langle i_{L2}(t) \rangle_{T_s} = \frac{\langle i_1(t) \rangle_{T_s}}{d(t)} \quad (14.5)$$

$$\langle v_{C1}(t) \rangle_{T_s} + \langle v_{C2}(t) \rangle_{T_s} = \frac{\langle v_2(t) \rangle_{T_s}}{d(t)} \quad (14.6)$$

Substitution of these expressions into Eqs. (14.1) and (14.4) leads to

$$\langle v_1(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle v_2(t) \rangle_{T_s} \quad (14.7)$$

$$\langle i_2(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle i_1(t) \rangle_{T_s} \quad (14.8)$$

The averaged equivalent circuit for the switch network, that corresponds to Eqs. (14.7) and (14.8), is illustrated in Fig. 14.4c. Upon completing the averaging step, the switching harmonics have been removed from all converter waveforms, leaving only the dc and low-frequency ac components. This large-signal, nonlinear, time-invariant model is valid for frequencies sufficiently less than the switching frequency. Averaging the waveforms of Fig. 14.3 modifies only the switch network; the remainder of the converter circuit is unchanged. Therefore, the averaged circuit model of the converter is obtained simply by replacing the switch network with the averaged switch model. The switch network of Fig. 14.4a can be identified in any two-switch converter, such as the buck, boost, buck-boost, SEPIC, or Ćuk. If the converter operates in continuous conduction mode, the derivation of the averaged switch model follows the same steps, and the result shown in Fig. 14.4c is the same for all of these converter topologies. This means that the model of Fig. 14.4c can be used as a general large-signal averaged switch model for all two-switch converters operating in CCM.

### 14.1.3 Perturbation and Linearization

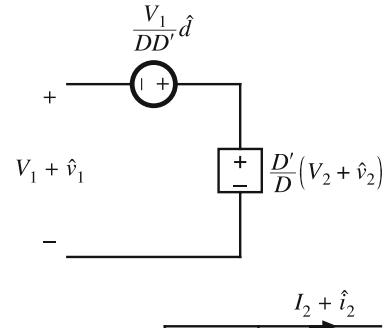
The model of Fig. 14.4c is nonlinear, because the dependent generators given by Eqs. (14.7) and (14.8) are nonlinear functions of  $d(t)$ ,  $\langle i_2(t) \rangle_{T_s}$ , and  $\langle v_1(t) \rangle_{T_s}$ . To construct a small-signal ac model, we perturb and linearize Eqs. (14.7) and (14.8) in the usual fashion. Let

$$\begin{aligned} d(t) &= D + \hat{d}(t) \\ \langle v_1(t) \rangle_{T_s} &= V_1 + \hat{v}_1(t) \\ \langle i_1(t) \rangle_{T_s} &= I_1 + \hat{i}_1(t) \\ \langle v_2(t) \rangle_{T_s} &= V_2 + \hat{v}_2(t) \\ \langle i_2(t) \rangle_{T_s} &= I_2 + \hat{i}_2(t) \end{aligned} \quad (14.9)$$

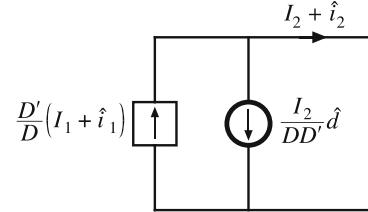
With these substitutions, Eq. (14.7) becomes

$$(D + \hat{d})(V_1 + \hat{v}_1) = (D' - \hat{d})(V_2 + \hat{v}_2) \quad (14.10)$$

**Fig. 14.5** Linearization of the dependent voltage source



**Fig. 14.6** Linearization of the dependent current source



It is desired to solve for the dependent quantity  $V_1 + \hat{v}_1$ . Equation (14.10) can be manipulated as follows:

$$D(V_1 + \hat{v}_1) = D'(V_2 + \hat{v}_2) - \hat{d}(V_1 + V_2) - \hat{d}\hat{v}_1 - \hat{d}\hat{v}_2 \quad (14.11)$$

The terms  $\hat{d}(t)\hat{v}_1(t)$  and  $\hat{d}(t)\hat{v}_2(t)$  are nonlinear, and are small in magnitude provided that the ac variations are much smaller than the quiescent values [as in Eq. (7.33)]. When the small-signal assumption is satisfied, these terms can be neglected. Upon eliminating the nonlinear terms and solving for the switch network dependent output  $V_1 + \hat{v}_1$ , we obtain

$$\begin{aligned} (V_1 + \hat{v}_1) &= \frac{D'}{D}(V_2 + \hat{v}_2) - \hat{d}\left(\frac{V_1 + V_2}{D}\right) \\ &= \frac{D'}{D}(V_2 + \hat{v}_2) - \hat{d}\left(\frac{V_1}{DD'}\right) \end{aligned} \quad (14.12)$$

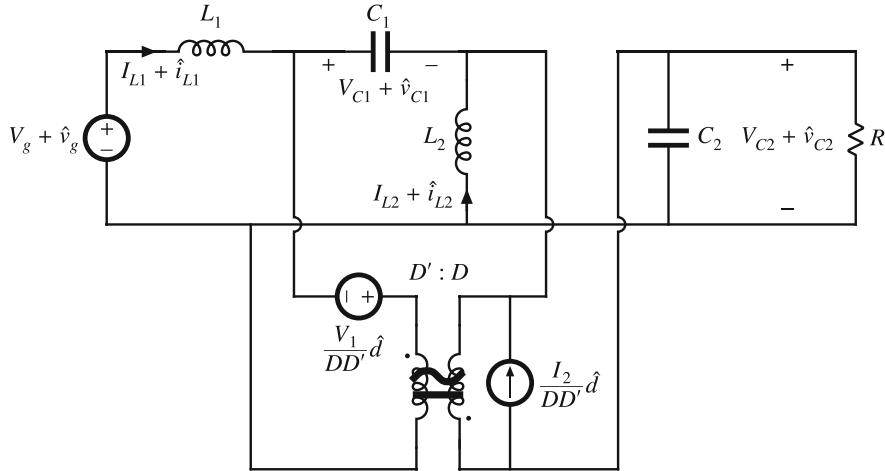
The term  $(V_1/DD')\hat{d}(t)$  is driven by the control input  $\hat{d}_2$  and hence can be represented by an independent voltage source as in Fig. 14.5. The term  $(D'/D)(V_2 + \hat{v}_2(t))$  is equal to the constant value  $(D'/D)$  multiplied by the port 2 independent voltage  $(V_2 + \hat{v}_2(t))$ . This term is represented by a dependent voltage source in Fig. 14.5. This dependent source will become the primary winding of an ideal transformer.

In a similar manner, substitution of the relationships (14.9) into Eq. (14.8) leads to:

$$(D + \hat{d})(I_2 + \hat{i}_2) = (D' - \hat{d})(I_1 + \hat{i}_1) \quad (14.13)$$

The terms  $\hat{i}_1(t)\hat{d}(t)$  and  $\hat{i}_2(t)\hat{d}(t)$  are nonlinear, and can be neglected when the small-signal assumption is satisfied. Elimination of the nonlinear terms, and solution for  $I_2 + \hat{i}_2$ , yields

$$\begin{aligned} (I_2 + \hat{i}_2) &= \frac{D'}{D}(I_1 + \hat{i}_1) - \hat{d}\left(\frac{I_1 + I_2}{D}\right) \\ &= \frac{D'}{D}(I_1 + \hat{i}_1) - \hat{d}\left(\frac{I_2}{DD'}\right) \end{aligned} \quad (14.14)$$



**Fig. 14.7** A dc and small-signal ac averaged circuit model of the CCM SEPIC

The term  $(I_2/DD')\hat{d}(t)$  is driven by the control input  $\hat{d}(t)$ , and is represented by an independent current source in Fig. 14.6. The term  $(D'/D)(I_1 + \hat{i}_1(t))$  is dependent on the port 1 current  $(I_1 + \hat{i}_1(t))$ . This term is modeled by a dependent current source in Fig. 14.6; this source will become the secondary winding of an ideal transformer. Equations (14.12) and (14.14) describe the averaged switch network model of Fig. 14.4d. Note that the model contains both dc and small-signal ac terms: one equivalent circuit is used for both the dc and the small-signal ac models. The transformer symbol contains both a solid line indicating that it is an ideal transformer capable of passing dc voltages and currents, and a sinusoidal line which indicates that small-signal ac variations are modeled. The averaged switch model of Fig. 14.4d reveals that the switch network performs the functions of: (i) transformation of dc and small-signal ac voltage and current levels according to the  $D':D$  conversion ratio and (ii) introduction of ac voltage and current variations into the converter circuit, driven by the control input  $d(t)$ . When this model is inserted into Fig. 14.2, the dc and small-signal ac SEPIC model of Fig. 14.7 is obtained. This model can now be solved to determine the steady-state voltages and currents as well as the small-signal converter transfer functions.

The reference directions of the switch network waveforms in Figs. 14.2 and 14.3 are defined such that these waveforms are positive or zero for this example. The dc components of the averaged waveforms of Figs. 14.4 and 14.7 lead to average power flowing into port 1 of the switch network, and flowing out of port 2. Since no losses are modeled, the averaged switch network is lossless (for  $\hat{d} = 0$ ), and the port 1 input power is equal to the port 2 output power, with voltages and currents transformed by the switch network conversion ratio  $D/D'$ .

In summary, the circuit averaging method involves replacing the switch network with equivalent voltage and current sources, such that a time-invariant network is obtained. The converter waveforms are then averaged over one switching period to remove the switching harmonics. The large-signal model is perturbed and linearized about a quiescent operating point, to obtain a dc and a small-signal averaged switch model. Replacement of the switch network with the averaged switch model yields a complete averaged circuit model of the converter.

#### 14.1.4 Indirect Power

The averaged switch models of Figs. 14.1, 14.4d, and 14.7 contain a dc transformer that transfers average power from input port 1 to output port 2 of the switch network. Yet, in the original circuits of Figs. 14.4a and 14.2, there is no direct connection between the transistor port 1 and the diode port 2. What is the physical mechanism in the circuit that leads to transmission of average power between ports 1 and 2? The existence and operation of such a mechanism are key to the validity and justification of the averaged switch model.

Let us examine in more detail the power flowing into port 1 of the switch network, as defined by the port 1 voltage  $v_1(t)$  and current  $i_1(t)$  waveforms of Fig. 14.3. The instantaneous power flowing into port 1 can be expressed as:

$$p_1(t) = v_1(t)i_1(t) \quad (14.15)$$

We can express the instantaneous voltage  $v_1(t)$  and current  $i_1(t)$  in terms of their dc (average) components and high-frequency ac (switching) components as follows:

$$\begin{aligned} v_1(t) &= \langle v_1(t) \rangle_{T_s} + \tilde{v}_1(t) \\ i_1(t) &= \langle i_1(t) \rangle_{T_s} + \tilde{i}_1(t) \end{aligned} \quad (14.16)$$

where  $\tilde{v}_1(t)$  and  $\tilde{i}_1(t)$  are the high-frequency switching components of  $v_1(t)$  and  $i_1(t)$ , respectively. By definition, these quantities are purely ac and have zero average:

$$\begin{aligned} \langle \tilde{v}_1(t) \rangle_{T_s} &= 0 \\ \langle \tilde{i}_1(t) \rangle_{T_s} &= 0 \end{aligned} \quad (14.17)$$

The dc or low-frequency components of  $v_1(t)$  and  $i_1(t)$  are  $\langle v_1(t) \rangle_{T_s}$  and  $\langle i_1(t) \rangle_{T_s}$ , averaged according to Eq. (7.3) as usual. We can express the port 1 instantaneous power as

$$\begin{aligned} p_1(t) &= (\langle v_1 \rangle_{T_s} + \tilde{v}_1(t))(\langle i_1 \rangle_{T_s} + \tilde{i}_1(t)) \\ &= \langle v_1 \rangle_{T_s} \langle i_1 \rangle_{T_s} + \langle v_1 \rangle_{T_s} \tilde{i}_1(t) + \langle i_1 \rangle_{T_s} \tilde{v}_1(t) + \tilde{v}_1(t) \tilde{i}_1(t) \end{aligned} \quad (14.18)$$

The net energy flowing into port 1 over one switching period is

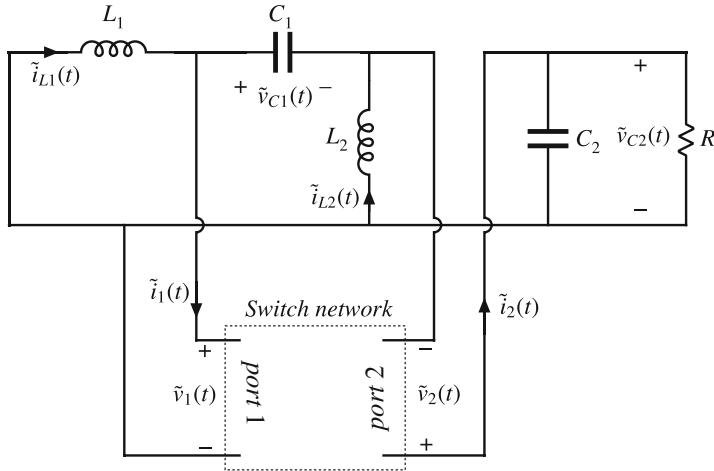
$$P_1 = \langle p_1(t) \rangle_{T_s} \quad (14.19)$$

In this discussion, we do not model losses and consider the transistor as an ideal switch. With this ideal switch assumption, the average port 1 power is zero:

$$P_1 = \langle p_1(t) \rangle_{T_s} = 0 \quad (14.20)$$

Now substitute Eq. (14.18) into Eq. (14.20). Equation (14.17) implies that the cross-product terms  $\langle v_1 \rangle_{T_s} \tilde{i}_1(t)$  and  $\langle i_1 \rangle_{T_s} \tilde{v}_1(t)$  have zero average. Hence we obtain

$$0 = \langle v_1 \rangle_{T_s} \langle i_1 \rangle_{T_s} + \langle \tilde{v}_1(t) \tilde{i}_1(t) \rangle_{T_s} \quad (14.21)$$



**Fig. 14.8** Circuit modeling only the switching-frequency components of the converter waveforms

This can be rearranged as

$$\langle v_1 \rangle_{T_s} \langle i_1 \rangle_{T_s} = -\langle \tilde{v}_1(t) \tilde{i}_1(t) \rangle_{T_s} \quad (14.22)$$

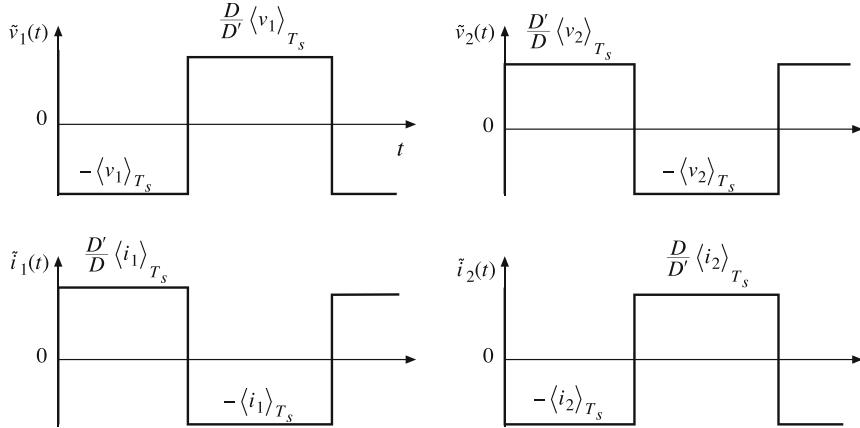
The quantity  $\langle v_1 \rangle_{T_s} \langle i_1 \rangle_{T_s}$  is the dc power flowing into the switch network port 1 of the averaged model. Equation (14.22) shows that the transistor operating as an ideal switch converts this into ac average power  $\langle \tilde{v}_1(t) \tilde{i}_1(t) \rangle_{T_s}$  that flows out of port 1. This ac average power is transmitted at the switching frequency and its harmonics (see Sect. 20.1 for a detailed explanation of average power in nonsinusoidal systems). The transistor behaves as an inverter, converting dc power into ac power at the switching frequency. This ac power is called *indirect power* [9, 109].

The ac components  $\tilde{v}_1(t)$  and  $\tilde{i}_1(t)$  are not included in the averaged model, and hence the averaged model is unable to represent how the ac power flows through the converter. We could sketch a circuit that models the high-frequency components of the converter waveforms, such as  $\tilde{v}_1(t)$ ,  $\tilde{i}_1(t)$ , etc. Figure 14.8 is obtained from Fig. 14.2 by the dc (average) components of the converter waveforms to zero; the remaining signals of the circuit occur at the switching frequency and its harmonics. It is assumed that  $v_g(t)$  contains only dc, so the input voltage source is set to zero. As noted above, port 1 of the switch network becomes a source of switching harmonics and ac power.

Figure 14.9 illustrates the waveforms  $\tilde{v}_1(t)$ ,  $\tilde{i}_1(t)$ ,  $\tilde{v}_2(t)$ , and  $\tilde{i}_2(t)$ , for operation in continuous conduction mode with small ripple in the inductor currents and capacitor voltages. Under these conditions, the inductors behave nearly as open circuits at the switching frequency, and the capacitors behave nearly as short circuits. In consequence, the indirect power flows out of port 1, through capacitor  $C_1$ , and into port 2.

We can write the equations of the instantaneous and average power in port 2 of the switch network in a similar manner. The instantaneous power flowing out of port 2 is

$$p_2(t) = v_2(t) i_2(t) \quad (14.23)$$



**Fig. 14.9** Switching-frequency components of the switch network waveforms, SEPIC example

The reference polarities of  $v_2(t)$  and  $i_2(t)$  have been chosen such that both of these waveforms are positive. In consequence, positive  $p_2(t)$  represents generated power that flows out of switch network port 2. The instantaneous voltage  $v_2(t)$  and current  $i_2(t)$  are expressed in terms of their dc (average) components and high-frequency ac (switching) components as follows:

$$\begin{aligned} v_2(t) &= \langle v_2 \rangle_{T_s} + \tilde{v}_2(t) \\ i_2(t) &= \langle i_2 \rangle_{T_s} + \tilde{i}_2(t) \end{aligned} \quad (14.24)$$

By definition,  $\tilde{v}_2(t)$  and  $\tilde{i}_2(t)$  are purely ac and have zero average:

$$\begin{aligned} \langle \tilde{v}_2(t) \rangle_{T_s} &= 0 \\ \langle \tilde{i}_2(t) \rangle_{T_s} &= 0 \end{aligned} \quad (14.25)$$

The port 2 instantaneous power is

$$\begin{aligned} p_2(t) &= (\langle v_2 \rangle_{T_s} + \tilde{v}_2(t))(\langle i_2 \rangle_{T_s} + \tilde{i}_2(t)) \\ &= \langle v_2 \rangle_{T_s} \langle i_2 \rangle_{T_s} + \langle v_2 \rangle_{T_s} \tilde{i}_2(t) + \langle i_2 \rangle_{T_s} \tilde{v}_2(t) + \tilde{v}_2(t) \tilde{i}_2(t) \end{aligned} \quad (14.26)$$

The net energy flowing out of port 2 over one switching period is

$$P_2 = \langle p_2(t) \rangle_{T_s} \quad (14.27)$$

Again, we do not model losses and consider the diode as an ideal switch. With this ideal switch assumption, the average port 2 power is zero:

$$P_2 = \langle p_2(t) \rangle_{T_s} = 0 \quad (14.28)$$

Now substitute Eq. (14.26) into Eq. (14.28). Equation (14.25) implies that the cross-product terms  $\langle v_2 \rangle_{T_s} \tilde{i}_2(t)$  and  $\langle i_2 \rangle_{T_s} \tilde{v}_2(t)$  have zero average. Hence we obtain

$$0 = \langle v_2 \rangle_{T_s} \langle i_2 \rangle_{T_s} + \langle \tilde{v}_2(t) \tilde{i}_2(t) \rangle_{T_s} \quad (14.29)$$

This can be rearranged as

$$\langle v_2 \rangle_{T_s} \langle i_2 \rangle_{T_s} = -\langle \tilde{v}_2(t) \tilde{i}_2(t) \rangle_{T_s} \quad (14.30)$$

So port 2 behaves as a rectifier that converts the ac indirect power flowing into port 2 (from the remainder of the converter) into dc power. This dc power flows out of port 2, and is the port 2 power of the averaged model.

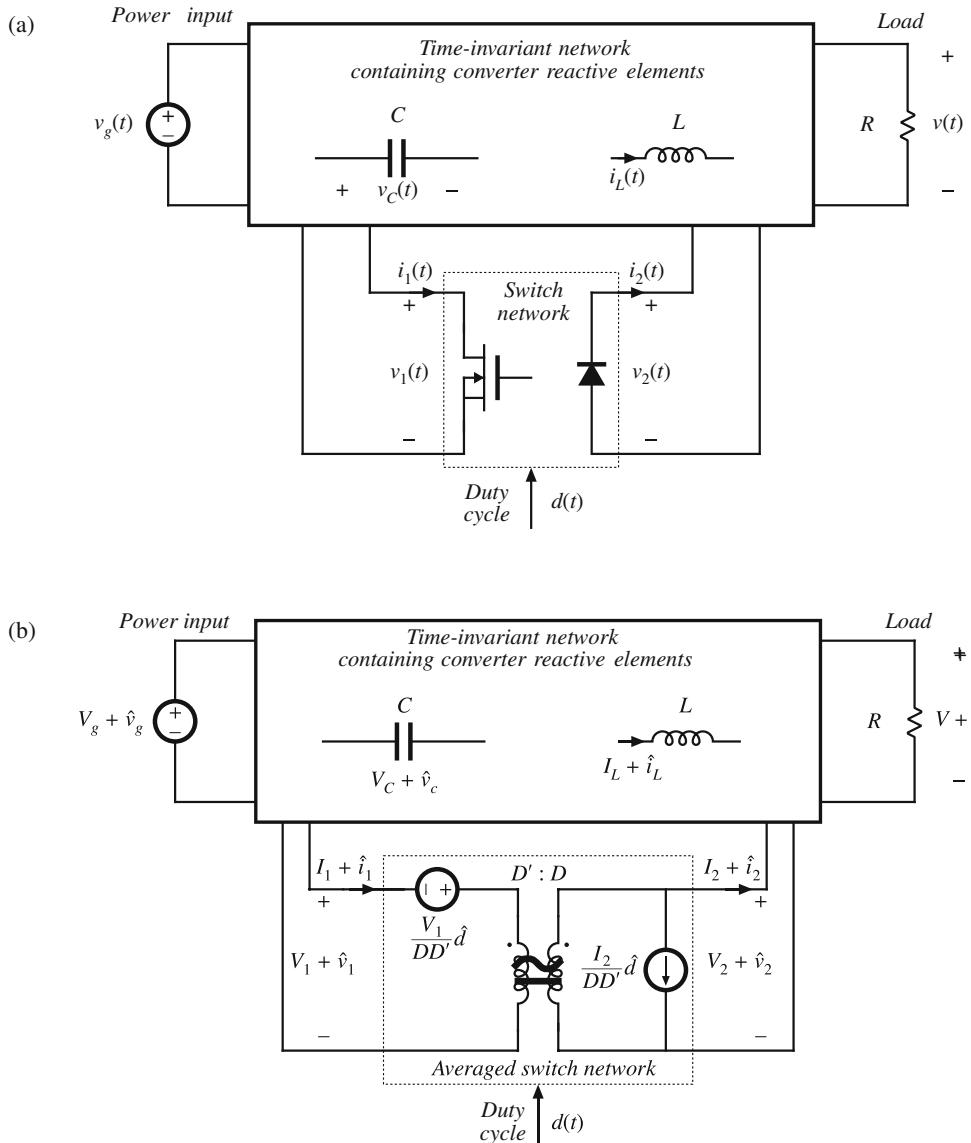
Thus, dc power flows into port 1 of the switch network. The switching transistor performs the function of inversion, converting the dc power into ac indirect power that flows out of switch network port 1 and through the remainder of the converter circuit including its reactive elements. This ac indirect power then flows into port 2 of the switch network, where the switching diode performs the function of rectification to convert the indirect power back to dc. This dc power constitutes the port 2 power of the averaged switch model.

It can be observed that the process of average switch modeling requires assumptions to be made about the time-invariant network and the waveforms of its reactive elements, which are then employed in modeling the switch network itself. The derivation summarized in Fig. 14.4 relies on these assumptions. For example, when the inductor current or capacitor voltage ripple is large, then the switch network models of Figs. 14.4c,d are not valid averaged representations of the switch network of Fig. 14.4a. Additional analysis is required, that accounts for how the reactive elements respond to the operation of the switch network, and how the ac indirect power propagates out of the switch network port 1, through the converter reactive elements, and into the switch network port 2. Averaged switch models for the discontinuous conduction mode are developed in Chap. 15, and for resonant switch converters in Chap. 23.

In converters that include a dc path between the converter input  $V_g$  and output  $V$  terminals for at least one subinterval, the indirect power can be smaller than the converter input power. The remaining power is called *direct power*; the direct power flows from the converter input to the output without the intermediate steps of high-frequency inversion and rectification. The buck and boost converters exhibit direct power flow, while the buck-boost, SEPIC, Ćuk, and all transformer-isolated converters do not. In general, we expect the indirect power conversion path to incur higher loss than direct conversion: direct power is subject only to dc conduction losses, while indirect power conversion incurs dc conduction losses as well as magnetics ac losses and semiconductor switching loss. Hence, converters that operate with a lower fraction of indirect power conversion can be expected to exhibit higher efficiency.

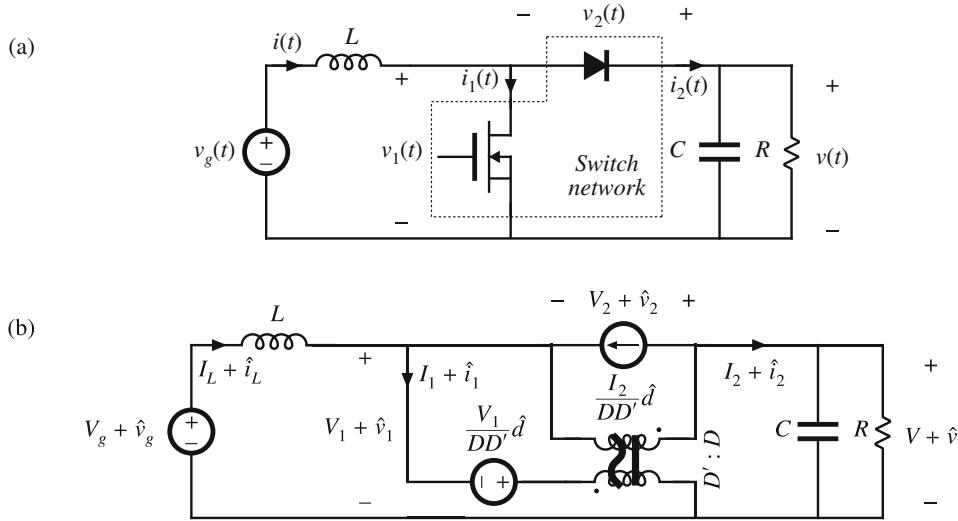
## 14.2 Additional Configurations of Switch Networks

The switch network of Fig. 14.4a can be identified in all two-switch converters, including buck, boost, SEPIC, Ćuk, etc. As illustrated in Fig. 14.10, a complete averaged circuit model of the converter can be constructed simply by replacing the switch network with the averaged switch model. For example, Fig. 14.11 shows an averaged circuit model of the boost converter obtained by identifying the switch network of Fig. 14.4a and replacing the switch network with the model of Fig. 14.4d.



**Fig. 14.10** Construction of an averaged circuit model for a two-switch converter operating in CCM: (a) the converter circuit with the general two-switch network identified; (b) dc and ac small-signal averaged circuit model obtained by replacing the switch network with the averaged model

So far, we have described derivation of the averaged switch model for the general two-switch network where the ports of the switch network coincide with the switch ports. No connections are assumed between the switches within the switch network itself. As a result, this switch network and its averaged model can be used to easily construct averaged circuit models of many two-switch converters, as illustrated in Fig. 14.10. It is important to note, however, that



**Fig. 14.11** Construction of an averaged circuit model for an ideal boost converter example: converter circuit with the switch network of Fig. 14.4a identified; (b) a dc and small-signal ac averaged circuit model obtained by replacing the switch network with the model of Fig. 14.4d

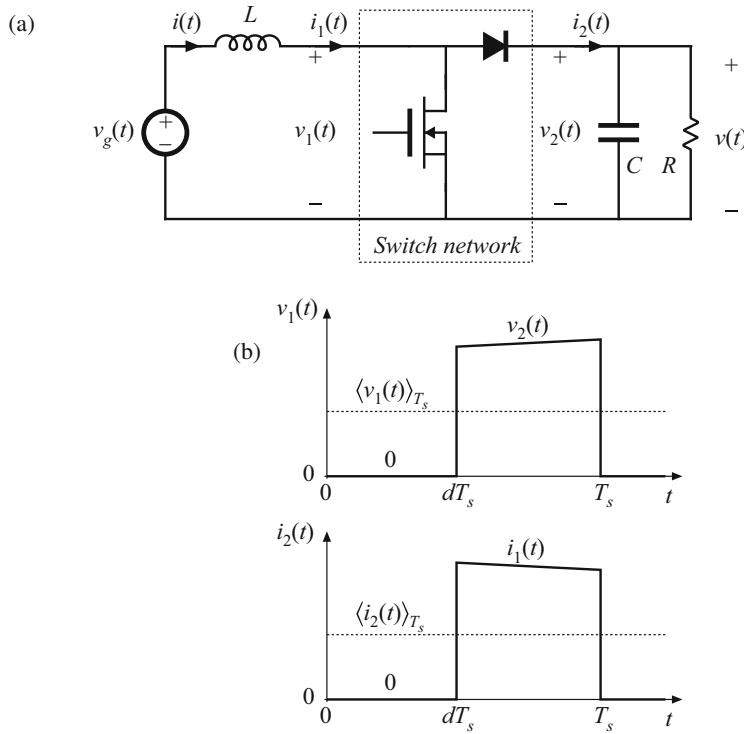
the definition of the switch network ports is not unique. Different definitions of the switch network lead to equivalent, but not identical, averaged switch models. The alternative forms of the averaged switch model may result in simpler circuit models, or models that provide better physical insight. Two alternative averaged switch models, better suited for analyses of boost and buck converters, are described in this section.

Consider the ideal boost converter of Fig. 14.12a. The switch network contains the transistor and the diode, as in Fig. 14.11a, but the switch network ports are defined differently. Let us proceed with the derivation of the corresponding averaged switch model. The switch network terminal waveforms are shown in Fig. 14.12b. Since  $i_1(t)$  and  $v_2(t)$  coincide with the converter inductor current and capacitor voltage, it is convenient to choose these waveforms as the independent inputs to the switch network. The steps in the derivation of the averaged switch model are illustrated in Fig. 14.13.

First, we replace the switch network with dependent voltage and current generators as illustrated in Fig. 14.13b. The voltage generator  $v_1(t)$  models the dependent voltage waveform at the input port of the switch network, i.e., the transistor voltage. As illustrated in Fig. 14.12b,  $v_1(t)$  is zero when the transistor conducts, and is equal to  $v_2(t)$  when the diode conducts:

$$v_1(t) = \begin{cases} 0, & 0 < t < dT_s \\ v_2(t), & dT_s < t < T_s \end{cases} \quad (14.31)$$

When  $v_1(t)$  is defined in this manner, the inductor voltage waveform is unchanged. Likewise,  $i_2(t)$  models the dependent current waveform at port 2 of the network, i.e., the diode current. As illustrated in Fig. 14.12b,  $i_2(t)$  is equal to zero when the transistor conducts, and is equal to  $i_1(t)$  when the diode conducts:



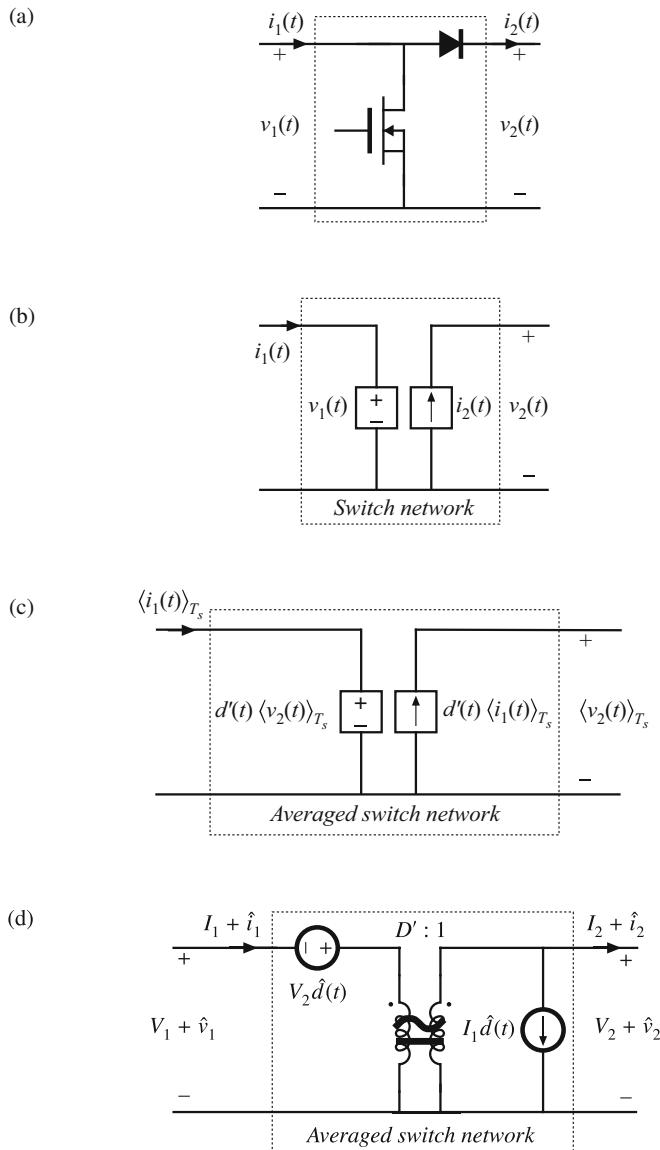
**Fig. 14.12** An ideal boost converter example: (a) converter circuit showing another possible definition of the switch network; (b) terminal waveforms of the switch network

$$i_2(t) = \begin{cases} 0, & 0 < t < dT_s \\ i_1(t), & dT_s < t < T_s \end{cases} \quad (14.32)$$

With  $i_2(t)$  defined in this manner, the capacitor current waveform is unchanged. Therefore, the original converter circuit shown in Fig. 14.12a and the circuit obtained by replacing the switch network of Fig. 14.13a with the switch network of Fig. 14.13b are electrically identical. So far, no approximations have been made. Next, we remove the switching harmonics by averaging all signals over one switching period, as in Eq. (7.3). The results are

$$\begin{aligned} \langle v_1(t) \rangle_{T_s} &= d'(t) \langle v_2(t) \rangle_{T_s} \\ \langle i_2(t) \rangle_{T_s} &= d'(t) \langle i_1(t) \rangle_{T_s} \end{aligned} \quad (14.33)$$

Here we have assumed that the switching ripples of the inductor current and capacitor voltage are small, or at least linear functions of time. The averaged switch model of Fig. 14.13c is now obtained. This is a large-signal, nonlinear model, which can replace the switch network in the original converter circuit, for construction of a large-signal nonlinear circuit model of the converter. The switching harmonics have been removed from all converter waveforms, leaving only the dc and low-frequency ac components.



**Fig. 14.13** Derivation of the averaged switch model for the CCM boost of Fig. 14.12: (a) switch network; (b) switch network where the switches are replaced with dependent sources whose waveforms match the switch terminal dependent waveforms; (c) large-signal, nonlinear averaged switch model obtained by averaging the switch network terminal waveforms in (b); (d) dc and ac small-signal averaged switch network model

The model can be linearized by perturbing and linearizing the converter waveforms about a quiescent operating point, in the usual manner. Let

$$\begin{aligned}\langle v_g(t) \rangle_{T_s} &= V_g + \hat{v}_g(t) \\ d(t) = D + \hat{d}(t) \Rightarrow d'(t) &= D' - \hat{d}(t) \\ \langle i(t) \rangle_{T_s} = \langle i_1(t) \rangle_{T_s} &= I + \hat{i}(t) \\ \langle v(t) \rangle_{T_s} = \langle v_2(t) \rangle_{T_s} &= V + \hat{v}(t) \\ \langle v_1(t) \rangle_{T_s} &= V_1 + \hat{v}_1(t) \\ \langle i_2(t) \rangle_{T_s} &= I_2 + \hat{i}_2(t)\end{aligned}\tag{14.34}$$

The nonlinear voltage generator at port 1 of the averaged switch network has value

$$(D' - \hat{d}(t))(V + \hat{v}(t)) = D'(V + \hat{v}(t)) - V\hat{d}(t) - \hat{v}(t)\hat{d}(t)\tag{14.35}$$

The term  $\hat{v}(t)\hat{d}(t)$  is nonlinear, and is small in magnitude provided that the ac variations are much smaller than the quiescent values [as in Eq. (7.33)]. When the small-signal assumption is satisfied, this term can be neglected. The term  $V\hat{d}(t)$  is driven by the control input, and hence can be represented by an independent voltage source. The term  $D'(V + \hat{v}(t))$  is equal to the constant value  $D'$  multiplied by the output voltage ( $V + \hat{v}(t)$ ). This term is dependent on the output capacitor voltage; it is represented by a dependent voltage source. This dependent source will become the primary winding of an ideal transformer.

The nonlinear current generator at the port 2 of the averaged switch network is treated in a similar manner. Its current is

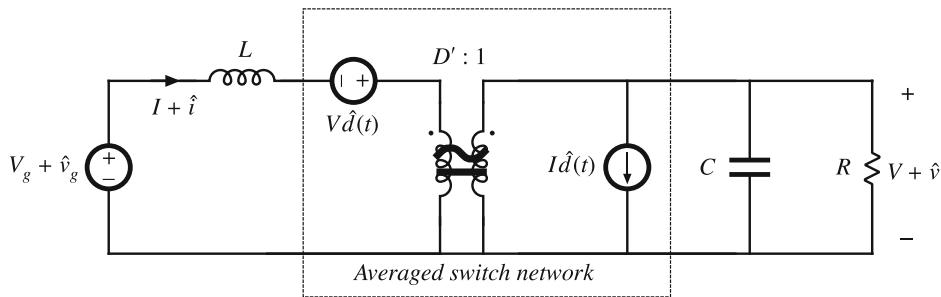
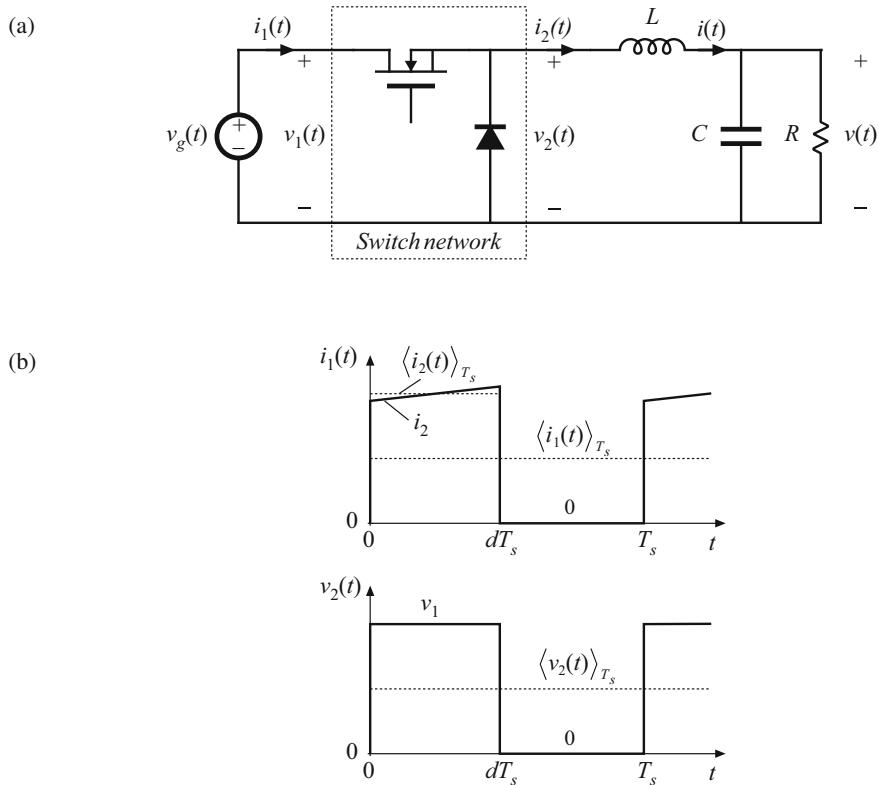
$$(D' - \hat{d}(t))(I + \hat{i}(t)) = D'(I + \hat{i}(t)) - I\hat{d}(t) - \hat{i}(t)\hat{d}(t)\tag{14.36}$$

The term  $\hat{i}(t)\hat{d}(t)$  is nonlinear, and can be neglected provided that the small-signal assumption is satisfied.

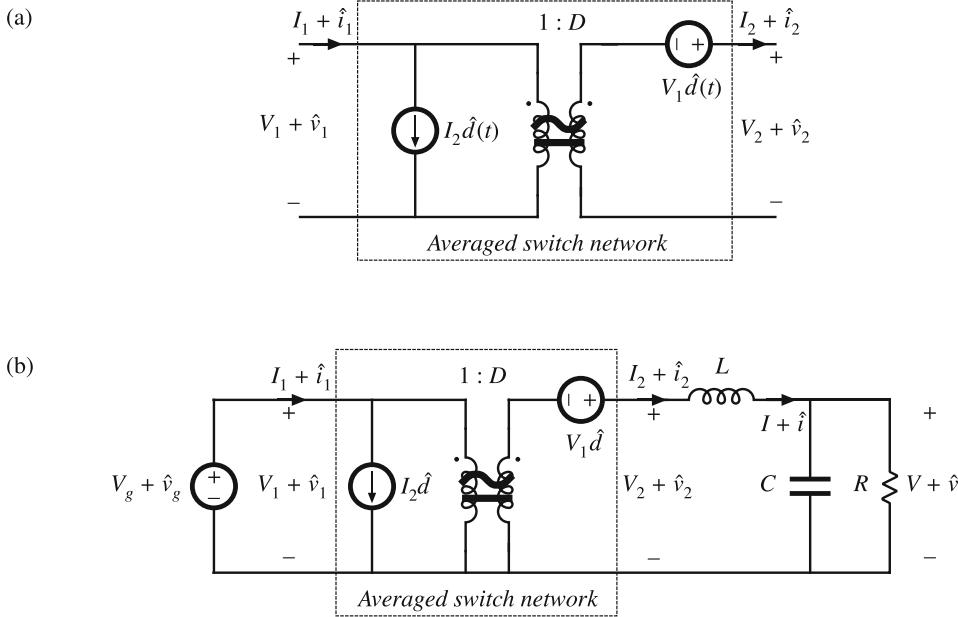
The term  $I\hat{d}(t)$  is driven by the control input  $\hat{d}(t)$ , and is represented by an independent current source. The term  $D'(I + \hat{i}(t))$  is dependent on the inductor current ( $I + \hat{i}(t)$ ). This term is modeled by a dependent current source; this source will become the secondary winding of an ideal transformer.

Upon elimination of the nonlinear terms, and replacement of the dependent generators with an ideal  $D':1$  transformer, the combined dc and small-signal ac averaged switch model of Fig. 14.13d is obtained. Figure 14.14 shows the complete averaged circuit model of the boost converter.

It is interesting to compare the models of Figs. 14.11b and 14.14. The two averaged circuit models of the boost converter are equivalent—they result in the same steady-state solution, and the same converter transfer functions. However, since both ports of the switch network in Fig. 14.12a share the same reference ground, the resulting averaged circuit model in Fig. 14.14 is easier to solve, and gives better physical insight into steady-state operation and dynamics of the boost converter. The circuit model of Fig. 14.14 reveals that the switch network performs the functions of: (i) transformation of dc and small-signal ac voltage and current levels according to the  $D':1$  conversion ratio and (ii) introduction of ac voltage and current variations into the converter circuit, driven by the control input  $d(t)$ . The model of Fig. 14.14 obtained using the circuit averaging approach is identical to the model of Fig. 7.18b obtained using the basic ac modeling technique of Sect. 7.2.

**Fig. 14.14** Dc and small-signal ac averaged circuit model of the boost converter**Fig. 14.15** Buck converter example: **(a)** converter circuit, **(b)** switch waveforms

Next, we consider the CCM buck converter of Fig. 14.15, where the switch network ports are defined to share a common ground terminal. The derivation of the corresponding averaged switch model follows the same steps as in the SEPIC and the boost examples. Let us select  $v_1(t)$  and  $i_2(t)$  as the independent terminal variables of the two-port switch network, since these quantities coincide with the applied converter input voltage  $v_g(t)$  and the inductor current  $i(t)$ ,



**Fig. 14.16** Averaged switch modeling, buck converter example: (a) dc and small-signal ac averaged switch model; (b) Averaged circuit model of the buck converter obtained by replacement of the switch network by the averaged switch model

respectively. We then need to express the averaged dependent terminal waveforms  $\langle i_1(t) \rangle_{T_s}$  and  $\langle v_2(t) \rangle_{T_s}$  as functions of the control input  $d(t)$  and of  $\langle v_1(t) \rangle_{T_s}$  and  $\langle i_2(t) \rangle_{T_s}$ . Upon averaging the waveforms of Fig. 14.15b, one obtains

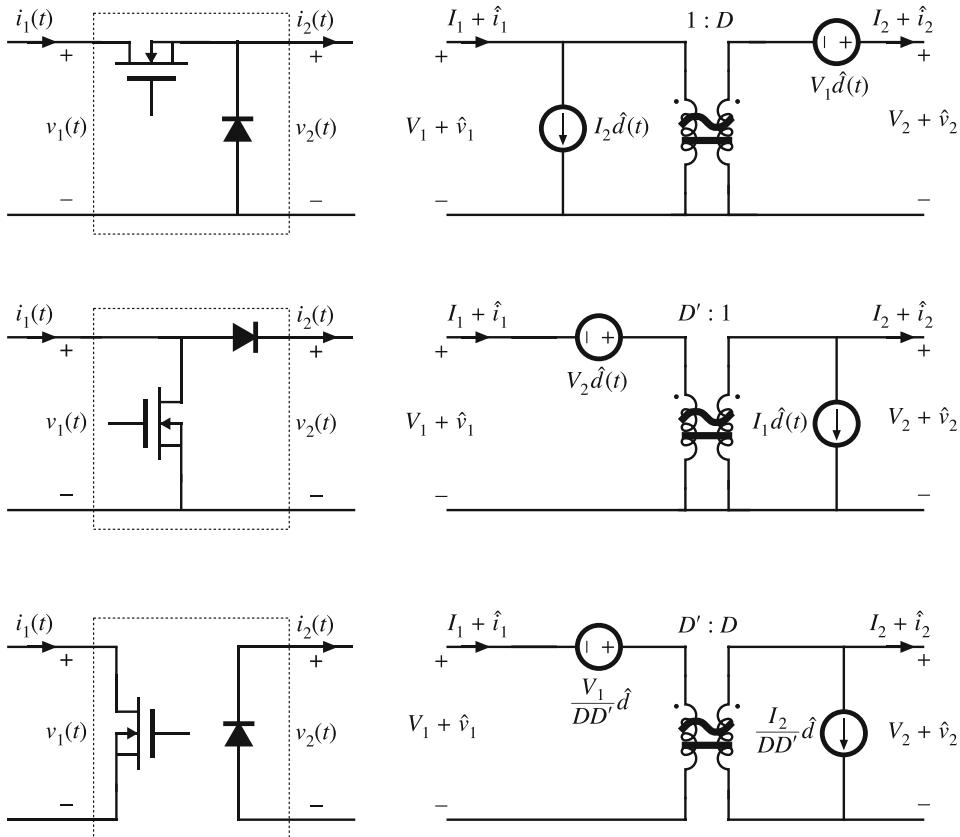
$$\begin{aligned}\langle i_1(t) \rangle_{T_s} &= d(t) \langle i_2(t) \rangle_{T_s} \\ \langle v_2(t) \rangle_{T_s} &= d(t) \langle v_1(t) \rangle_{T_s}\end{aligned}\quad (14.37)$$

Perturbation and linearization of Eq. (14.37) then leads to

$$\begin{aligned}I_1 + \hat{i}_1(t) &= D(I_2 + \hat{i}_2(t)) + I_2 \hat{d}(t) \\ V_2 + \hat{v}_2(t) &= D(V_1 + \hat{v}_1(t)) + V_1 \hat{d}(t)\end{aligned}\quad (14.38)$$

An equivalent circuit corresponding to Eq. (14.38) is illustrated in Fig. 14.16a. Replacement of the switch network in Fig. 14.15a with the averaged switch model of Fig. 14.16a leads to the converter averaged circuit model of Fig. 14.16b. The circuit model of Fig. 14.16b reveals that the switch network performs the functions of: (i) transformation of dc and small-signal ac voltage and current levels according to the  $1:D$  conversion ratio and (ii) introduction of ac voltage and current variations into the converter circuit, driven by the control input  $d(t)$ . The model is easy to solve for both dc conversion ratio and small-signal frequency responses. It is identical to the model shown in Fig. 7.18a.

The three basic switch networks—the buck switch network, the boost switch network, and the general two-switch network—together with the corresponding averaged switch models are shown in Fig. 14.17.



**Fig. 14.17** Three basic switch networks, and their CCM dc and small-signal ac averaged switch models: (a) the buck switch network, (b) the boost switch network, and (c) the general two-switch network

### 14.3 Simulation of Averaged Circuit Models

Computer simulation can be a powerful tool in the engineering design process. Starting from design specifications, an initial design typically includes selection of system and circuit configurations, as well as component types and values. In this process, component and system models are constructed based on vendor-supplied data, and by applications of analysis and modeling techniques. These models, validated by experimental data whenever possible, are the basis upon which the designer can choose parameter values and verify the achieved performance against the design specifications. One must take into account the fact that actual parameter values will not match their nominal values because of inevitable production tolerances, changes in environmental conditions (such as temperature), and aging. In the design verification step, worst-case analysis (or other reliability and production yield analysis) is performed to judge whether the specifications are met under all conditions, i.e., for expected ranges of component parameter values. Computer simulation is very well suited for this task: using reliable models and appropriate simulation setups, the system performance can be tested for various sets of component

parameter values. One can then perform design iterations until the worst-case behavior meets specifications, or until the system reliability and production yield are acceptably high.

In the design verification of power electronic systems by simulation, it is often necessary to use component and system models of various levels of complexity:

1. *Detailed, complex models that attempt to accurately represent physical behavior of devices.* Such models are necessary for tasks that involve finding switching times, details of switching transitions and switching loss mechanisms, or instantaneous voltage and current stresses. Component vendors often provide libraries of such device models. To complete a detailed circuit model, one must also carefully examine effects of packaging and board interconnects. With fast switching power semiconductors, simulation time steps of a few nanoseconds or less may be required, especially during on/off switching transitions. Because of the complexity of detailed device models, and the fine time resolution, the simulation tasks can be time consuming. In practice, time-domain simulations using detailed device models are usually performed on selected parts of the system, and over relatively short time intervals. Tools available to perform transient simulations of switched-mode power converter using detailed device models include variants of SPICE [110] such as LTspice and PSpice.
2. *Simplified device models.* Since an on/off switching transition usually takes a small fraction of a switching cycle, the basic operation of switching power converters can be explained using simplified, idealized device models. For example, a MOSFET can be modeled as a switch with a small (ideally zero) on-resistance  $R_{on}$  when on, and a very large off-resistance (ideally an open circuit) when off. Such simplified models yield physical insight into the basic operation of switching power converters, and provide the starting point for developments of analytical models described throughout this book. Simplified device models are also useful for time-domain simulations aimed at verifying converter and controller operation, switching ripples, current and voltage stresses, and responses to load or input transients. Since device models are simple, and details of switching transitions are ignored, tasks that require simulations over many switching cycles can be completed efficiently using circuit simulators. Various approaches have been developed to support fast transient simulation of switching power converters based on idealized, piecewise-linear device models [111–117], or a combination of piecewise-linear and nonlinear models [118]. Simulation tools based on piecewise-linear device models include PLECS and SIMPLIS.
3. *Averaged converter models.* Averaged models that are well suited for prediction of converter steady-state and dynamic responses are discussed throughout this book. These models are essential design tools because they provide physical insight and lead to analytical results that can be used in the design process to select component parameter values for a given set of specifications. In the design verification step, simulations of averaged converter models can be performed to test for losses and efficiency, steady-state voltages and currents, stability, and large-signal transient responses. Since switching transitions and ripples are removed by averaging, simulations over long time intervals and over many sets of parameter values can be completed efficiently. As a result, averaged models are also well suited for simulations of large electronic systems that include switching converters. Furthermore, since large-signal averaged models are nonlinear, but time-invariant, small-signal ac simulations can be used to generate various frequency responses of interest. Selected references on averaged converter modeling for simulation include [119–129].

Based on the material presented in Sect. 14.1, averaged switch models for computer simulation of converters operating in continuous conduction mode are described in this section. It is

assumed that the reader is familiar with basics of SPICE circuit simulations. SPICE subcircuit netlists are included to help explain details of model implementation and simulation analysis options. Usually, instead of writing netlists, the user would enter circuit diagrams and analysis options from a front-end schematic capture tool.

### 14.3.1 Simulation Model of the Ideal CCM Averaged Switch Network

The central idea of the *averaged switch modeling* described in Sect. 14.1 is to identify a switch network in the converter, and then to find an averaged circuit model. The resulting averaged switch model can then be inserted into the converter circuit to obtain a complete model of the converter. An important feature of the averaged switch modeling approach is that the same model can be used in many different converter configurations; it is not necessary to rederive an averaged equivalent circuit for each particular converter. This feature is also very convenient for construction of averaged circuit models for simulation. A general-purpose subcircuit represents a large-signal nonlinear averaged switch model. The converter averaged circuit for simulation is then obtained by replacing the switch network with this subcircuit. Based on the discussion in Sect. 14.1, subcircuits that represent CCM averaged switch models are described in this section.

The large-signal averaged switch model for the general two-switch network of Fig. 14.4a is shown in Fig. 14.4c. A SPICE subcircuit implementation of this model is shown in Fig. 14.18. The subcircuit has five nodes. The transistor port of the averaged switch network is connected between the nodes 1 and 2, while the diode port is comprised of nodes 3 and 4. The duty ratio  $d = v(5)$  is the control input to the subcircuit at the node 5. The quantity  $v(5)$  is a voltage that is equal to the duty cycle, and that lies in the range zero to one volt. Figure 14.18c shows the netlist of the subcircuit. The netlist consists of only four lines of code and several comment lines (the lines starting with \*). The .subckt line defines the name (CCM1) of the subcircuit and the interface nodes. The value of the controlled voltage source  $E_t$ , which models the transistor port of the averaged switch network, is written according to Eq. (14.7):

$$\langle v_1(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle v_2(t) \rangle_{T_s} \quad (14.39)$$

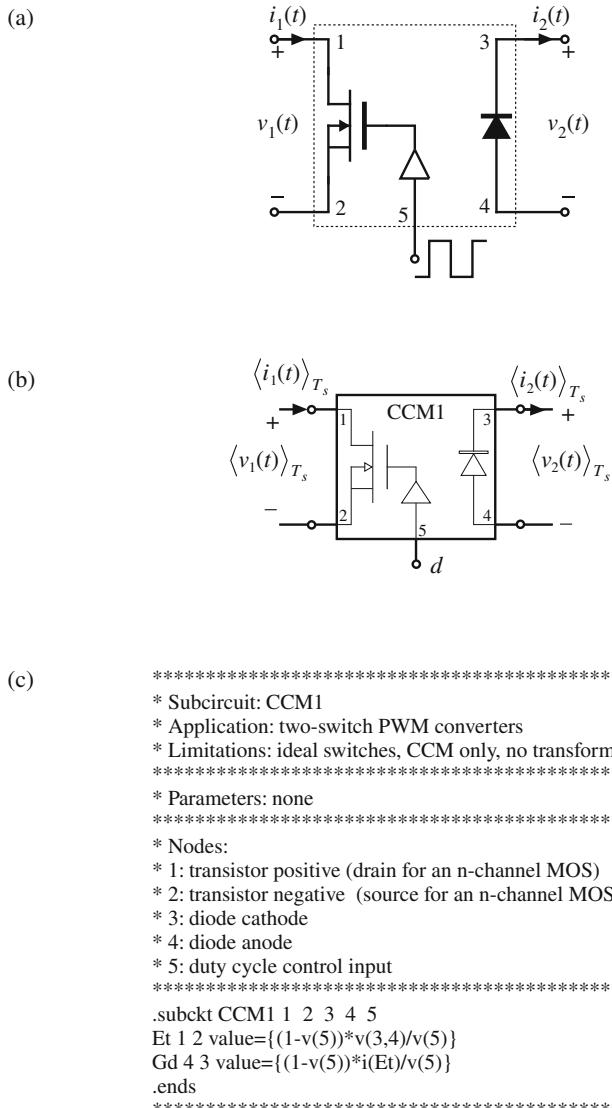
Note that  $v(3, 4)$  in the subcircuit of Fig. 14.18 is equal to the switch network independent input  $\langle v_2(t) \rangle_{T_s}$ . Also,  $d(t) = v(5)$ , and  $d'(t) = 1 - d(t) = 1 - v(5)$ . The value of the controlled current source  $G_d$ , which models the diode port, is computed according to Eq. (14.8):

$$\langle i_2(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle i_1(t) \rangle_{T_s} \quad (14.40)$$

The switch network independent input  $\langle i_1(t) \rangle_{T_s}$  equals the current  $i(E_t)$  through the controlled voltage source  $E_t$ . The .ends line completes the subcircuit netlist.

An advantage of the subcircuit CCM1 of Fig. 14.18 is that it can be used to construct an averaged circuit model for simulation of any two-switch PWM converter operating in continuous conduction mode, subject to the assumptions that the switches can be considered ideal, and that the converter does not include a step-up or step-down transformer. The subcircuit can be further refined to remove these limitations. In converters with an isolation transformer, the right-hand side of Eqs. (14.39) and (14.40) should be divided by the transformer turns ratio.

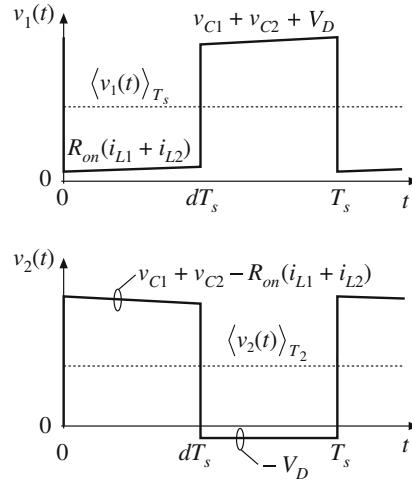
A disadvantage of the model in Fig. 14.18 is that Eqs.(14.39) and (14.40) have a discontinuity at duty cycle equal to zero. In applications of the subcircuit, it is necessary to restrict the duty-cycle to the range  $0 < D_{min} \leq d \leq 1$ .



**Fig. 14.18** Averaged switch model CCM1: (a) the general two-switch network; (b) symbol for the averaged switch subcircuit model; (c) SPICE netlist of the subcircuit

### 14.3.2 Averaged Switch Modeling and Simulation of Conduction Losses

An averaged switch model can be refined to include switch conduction losses. Consider again the SEPIC of Fig. 14.2. Suppose that the transistor on-resistance is  $R_{on}$  and the diode forward voltage drop  $V_D$  are approximately constant. In this example, all other conduction or switching losses are neglected. Our objective is to derive an averaged switch model that includes conduction losses caused by the voltage drops across  $R_{on}$  and  $V_D$ . Let us define the switch network as in



**Fig. 14.19** The switch network terminal voltages  $v_1(t)$  and  $v_2(t)$  for the case when the transistor on-resistance is  $R_{on}$  and the diode forward voltage drop is  $V_D$

Fig. 14.4a. The waveform of the switch network terminal currents are the same as in Fig. 14.3, but the voltage waveform are affected by the voltage drops across  $R_{on}$  and  $V_D$  as shown in Fig. 14.19. We select  $i_1(t)$  and  $i_2(t)$  as the switch network independent inputs, as in Sect. 14.1.1. The average values of  $v_1(t)$  and  $v_2(t)$  can be found as follows:

$$\langle v_1(t) \rangle_{T_s} = d(t)R_{on}(\langle i_{L1}(t) \rangle_{T_s} + \langle i_{L2}(t) \rangle_{T_s}) + d'(t)(\langle v_{C1}(t) \rangle_{T_s} + \langle v_{C2}(t) \rangle_{T_s} + V_D) \quad (14.41)$$

$$\langle v_2(t) \rangle_{T_s} = d(t)(\langle v_{C1}(t) \rangle_{T_s} + \langle v_{C2}(t) \rangle_{T_s} - R_{on}(\langle i_{L1}(t) \rangle_{T_s} + \langle i_{L2}(t) \rangle_{T_s})) + d'(t)(-V_D) \quad (14.42)$$

Next, we proceed to eliminate  $\langle i_{L1}(t) \rangle_{T_s}$ ,  $\langle i_{L2}(t) \rangle_{T_s}$ ,  $\langle v_{C1}(t) \rangle_{T_s}$ , and  $\langle v_{C2}(t) \rangle_{T_s}$ , to write the above equations in terms of the averaged independent terminal currents and voltages of the switch network. By combining Eqs. (14.41) and (14.42), we obtain:

$$\langle v_{C1}(t) \rangle_{T_s} + \langle v_{C2}(t) \rangle_{T_s} = \langle v_1(t) \rangle_{T_s} + \langle v_2(t) \rangle_{T_s} \quad (14.43)$$

Since the current waveform are the same as in Fig. 14.3, Eq. (14.5) can be used here:

$$\langle i_{L1}(t) \rangle_{T_s} + \langle i_{L2}(t) \rangle_{T_s} = \frac{\langle i_1(t) \rangle_{T_s}}{d(t)} \quad (14.44)$$

Substitution of Eqs. (14.43) and (14.44) into Eq. (14.41) results in:

$$\langle v_1(t) \rangle_{T_s} = R_{on}\langle i_1(t) \rangle_{T_s} + d'(t)(\langle v_1(t) \rangle_{T_s} + \langle v_2(t) \rangle_{T_s} + V_D) \quad (14.45)$$

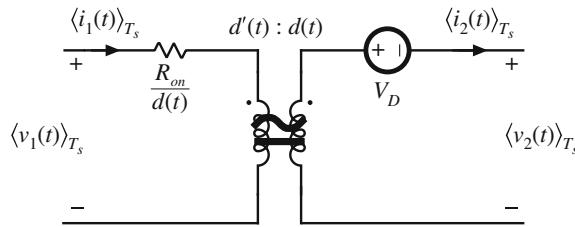
Equation (14.45) can be solved for the voltage  $\langle v_1(t) \rangle_{T_s}$ :

$$\langle v_1(t) \rangle_{T_s} = \frac{R_{on}}{d(t)}\langle i_1(t) \rangle_{T_s} + \frac{d'(t)}{d(t)}(\langle v_2(t) \rangle_{T_s} + V_D) \quad (14.46)$$

The expression for the averaged current  $\langle i_2(t) \rangle_{T_s}$  is given by Eq. (14.8) derived in Sect. 14.1.2:

$$\langle i_2(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle i_1(t) \rangle_{T_s} \quad (14.47)$$

Equations (14.46) and (14.47) constitute the averaged terminal relations of the switch network. An equivalent circuit corresponding to these relationships is shown in Fig. 14.20. The generators that depend on the transistor duty cycle  $d(t)$  are combined into an ideal transformer with the turns ratio  $d'(t):d(t)$ . This part of the model is the same as in the averaged switch model derived earlier for the switch network with ideal switches. The elements  $R_{on}/d$  and  $V_D$  model the conduction losses in the switch network. This is a large-signal, nonlinear model. If desired, this model can be perturbed and linearized in the usual manner, to obtain a small-signal ac switch model.



**Fig. 14.20** Large-signal averaged switch model for the general two-switch network of Fig. 14.17c. This model includes conduction losses due to the transistor on-resistance  $R_{on}$  and the diode forward voltage drop  $V_D$

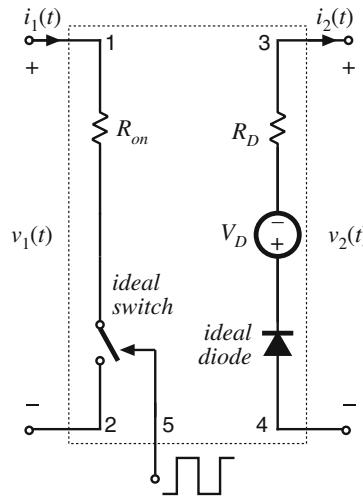
### 14.3.3 Inclusion of Switch Conduction Losses in Simulations

Let us modify the model of Fig. 14.18 to include switch conduction losses. Figure 14.21 shows simple device models that include transistor and diode conduction losses in the general two-switch network of Fig. 14.18a. The transistor is modeled as an ideal switch in series with an on-resistance  $R_{on}$ . The diode is modeled as an ideal diode in series with a forward voltage drop  $V_D$  and resistance  $R_D$ .

Construction of dc equivalent circuits to find dc conversion ratio and efficiency of converters is discussed in Chap. 3. Derivation of an averaged switch model that includes conduction losses arising from  $R_{on}$  and  $V_D$  is described in Sect. 14.3.2. Following the same averaged switch modeling approach, we can find the following relationships that describe the averaged switch model for the switch network of Fig. 14.21:

$$\langle v_1(t) \rangle_{T_s} = \left( \frac{R_{on}}{d(t)} + \frac{d'(t)R_D}{d^2(t)} \right) \langle i_1(t) \rangle_{T_s} + \frac{d'(t)}{d(t)} (\langle v_2(t) \rangle_{T_s} + V_D) \quad (14.48)$$

$$\langle i_2(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle i_1(t) \rangle_{T_s} \quad (14.49)$$



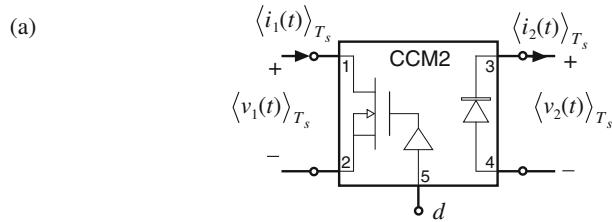
**Fig. 14.21** Switch network model that includes conduction loss elements  $R_{on}$ ,  $V_D$ , and  $R_D$

A subcircuit implementation of the averaged switch model described by Eqs. (14.48) and (14.49) is shown in Fig. 14.22. The subcircuit terminal nodes are the same as in the CCM1 subcircuit: the transistor port is between the nodes 1 and 2; the diode port is between the nodes 3 and 4; the duty ratio  $d = v(5)$  is the control input to the subcircuit at the node 5. Two controlled voltage sources in series,  $E_r$  and  $E_t$ , are used to generate the port 1 (transistor) averaged voltage according to Eq. (14.48). The controlled voltage source  $E_r$  models the voltage drop across the equivalent resistance  $R_{on}/d(t) + d'(t)R_D/d^2(t)$  in Eq. (14.48). Note that this equivalent resistance is a nonlinear function of the switch duty cycle  $d(t)$ . The controlled voltage source  $E_t$  shows how the port 1 (transistor) averaged voltage depends on the port 2 (diode) averaged voltage. The controlled current source  $G_d$  models the averaged diode current according to Eq. (14.49). The subcircuit CCM2 has three parameters ( $R_{on}$ ,  $V_D$ , and  $R_D$ ) that can be specified when the subcircuit is used in a converter circuit. The default values of the subcircuit parameters,  $R_{on} = 0$ ,  $V_D = 0$ , and  $R_D = 0$ , are defined in the .subckt line. These values correspond to the ideal case of no conduction losses.

The model of Fig. 14.22 is based on the simple device models of Fig. 14.21. It is assumed that inductor current ripples are small and that the converter operates in continuous conduction mode. Many practical converters, however, must operate in discontinuous conduction mode at low duty cycles where the diode forward voltage drop is comparable to or larger than the output voltage. In such cases, the model of Fig. 14.21, which includes  $V_D$  as a fixed voltage generator, gives incorrect, physically impossible results for polarities of converter voltages and currents, losses, and efficiency.

#### 14.3.4 Example: SEPIC DC Conversion Ratio and Efficiency

Let us consider an example of how the subcircuit CCM2 can be used to generate dc conversion ratio and efficiency curves for a CCM converter. As an example, Figure 14.23 shows a SEPIC averaged circuit model. The converter circuit can be found in Fig. 6.39a, or in Fig. 14.2. To con-

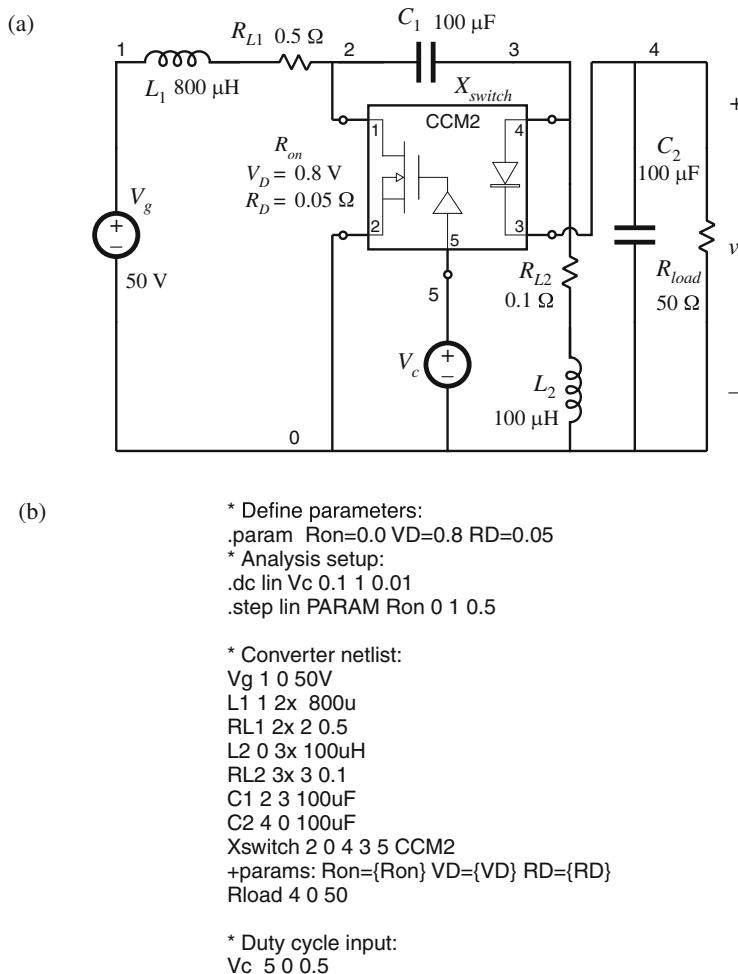


(b)

```
*****
* MODEL: CCM2
* Application: two-switch PWM converters, includes
*           conduction losses due to Ron, VD, RD
* Limitations: CCM only, no transformer
*****
* Parameters:
*   Ron = transistor on-resistance
*   VD = diode forward voltage drop
*   RD = diode on-resistance
*****
* Nodes:
*   1: transistor positive (drain for an n-channel MOS)
*   2: transistor negative (source for an n-channel MOS)
*   3: diode cathode
*   4: diode anode
*   5: duty cycle control input
*****
.subckt CCM2 1 2 3 4 5
+params: Ron=0 VD=0 RD=0
Er 1 1x value={i(Et)*(Ron+(1-v(5))*RD/v(5))/v(5)}
Et 1x 2 value={(1-v(5))*(V(3,4)+VD)/v(5)}
Gd 4 3 value={(1-v(5))*i(Et)/v(5)}
.ends
*****
```

**Fig. 14.22** Subcircuit implementation of the CCM averaged switch model that includes conduction losses: (a) circuit symbol; (b) SPICE netlist for the subcircuit

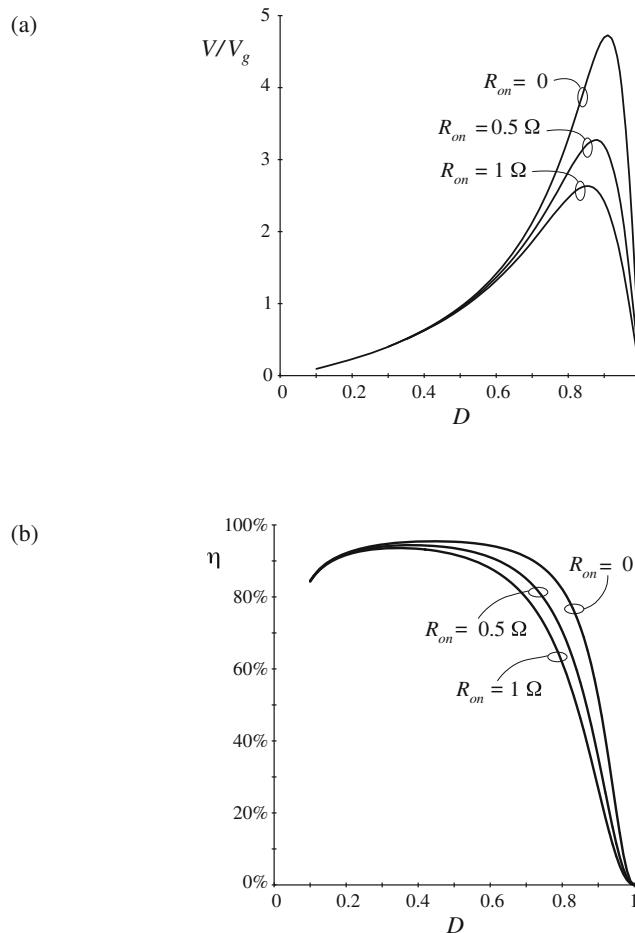
struct the averaged circuit model for simulation, the switch network is replaced by the subcircuit CCM2. In the converter netlist shown in Fig. 14.23, the  $X_{switch}$  line shows how the subcircuit is connected to other parts of the converter. The switch duty cycle is set by the voltage source  $V_c$ . All other parts of the converter circuit are simply copied to the averaged circuit model. Inductor winding resistances  $R_{L1} = 0.5 \Omega$  and  $R_{L2} = 0.1 \Omega$  are included to model copper losses of the inductors  $L_1$  and  $L_2$ , respectively. The switch conduction loss parameters are defined by the .param line in the netlist:  $R_{on} = 0$ ,  $V_D = 0.8V$ ,  $R_D = 0.05 \Omega$ . Notice how these values are passed to the subcircuit CCM2 in the  $X_{switch}$  line. In this example, all other losses in the converter are neglected. A dc sweep analysis (see the .dc line in the netlist) is set to vary the dc voltage source  $V_c$  from 0.1 V to 1 V, in 0.01 V increments, which corresponds to varying the switch duty cycle over the range from  $D = 0.1$  to  $D = 1$ . The range of duty cycles from zero to 0.1 is not covered because of the model discontinuity problem at  $D = 0$  (discussed in Sect. 14.3.1), and because the model predictions for conduction losses at low duty cycles are not valid, as discussed in



**Fig. 14.23** SEPIC simulation example: (a) schematic; (b) SPICE netlist

Sect. 14.3.3. The dc sweep analysis is repeated for values of the switch on-resistance in the range from  $R_{on} = 0 \Omega$  to  $R_{on} = 1 \Omega$  in 0.5  $\Omega$  increments (see the .step line in the netlist).

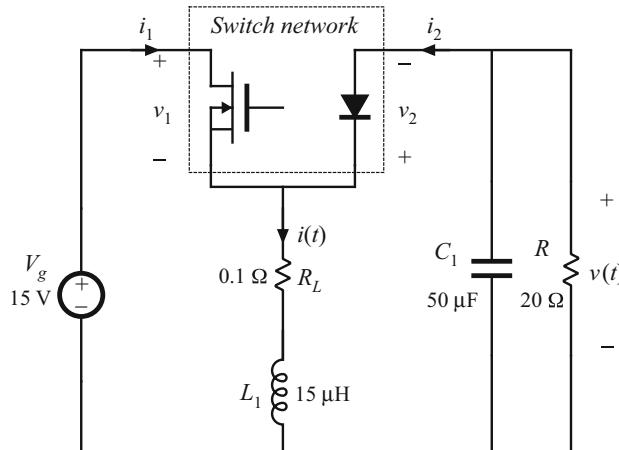
Simulation results for the dc output voltage  $V$  and the converter efficiency  $\eta$  are shown in Fig. 14.24. Several observations can be made based on the modeling approach and discussions presented in Chapter 3. At low duty cycles, efficiency drops because the diode forward voltage drop is comparable to the output voltage. At higher duty cycles, the converter currents increase, so that the conduction losses increase. Eventually, for duty cycles approaching 1, both the output voltage and the efficiency approach zero. Given a desired dc output voltage and efficiency, the plots in Fig. 14.24 can be used to select the transistor with an appropriate value of the on-resistance.



**Fig. 14.24** SEPIC simulation example: (a) dc conversion ratio; (b) efficiency

#### 14.3.5 Example: Transient Response of a Buck-Boost Converter

In addition to steady-state conversion characteristics, it is often of interest to investigate converter transient responses. For example, in voltage regulator designs, it is necessary to verify whether the output voltage remains within specified limits when the load current takes a step change. As another example, during a start-up transient when the converter is powered up, converter components can be exposed to significantly higher stresses than in steady state. It is of interest to verify that component stresses are within specifications or to make design modifications to reduce the stresses. In these examples, transient simulations can be used to test for converter responses.

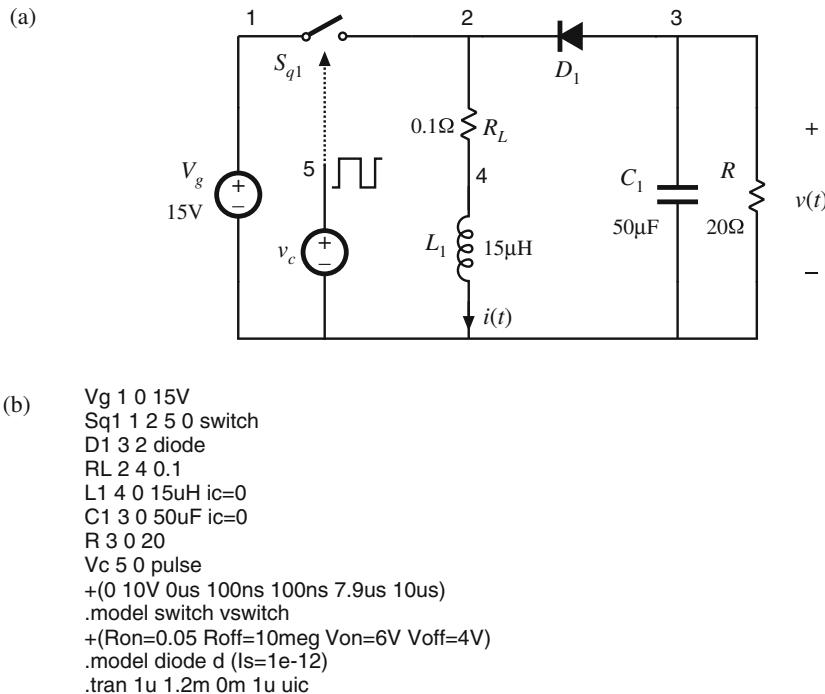


**Fig. 14.25** Buck-boost converter example

Transient simulations can be performed on the converter switching circuit model or on the converter averaged circuit model. As an example, let us apply these two approaches to investigate a start-up transient response of the buck-boost converter shown in Fig. 14.25.

Figure 14.26 shows a switching circuit model of the buck-boost converter. The inductor winding resistance  $R_L$  is included to model the inductor copper losses. The MOSFET is modeled as a voltage-controlled switch  $S_{q1}$  controlled by a pulsating voltage source  $v_c$ . The switch .model line specifies the switch on-resistance  $R_{on} = 50 \text{ m}\Omega$ , and the switch off-resistance  $R_{off} = 10 \text{ M}\Omega$ . The switch is on when the controlling voltage  $v_c$  is greater than  $V_{on} = 6 \text{ V}$ , and off when the controlling voltage  $v_c$  is less than  $V_{off} = 4 \text{ V}$ . The pulsating source  $v_c$  has the pulse amplitude equal to 10 V. The period is  $T_s = 1/f_s = 10 \mu\text{s}$ , the rise and fall times are  $t_r = t_f = 100 \text{ ns}$ , and the pulse width is  $t_p = 7.9 \mu\text{s}$ . The switch duty cycle is  $D = (t_p + 0.5(t_r + t_f))/T_s = 0.8$ . The built-in nonlinear SPICE model is used for the diode. In the diode .model statement, only the parameter  $I_s$  is specified, to set the forward voltage drop across the diode. The switch and the diode models used in this example are very simple. Conduction losses are modeled in a simple manner, and details of complex device behavior during switching transitions are neglected.

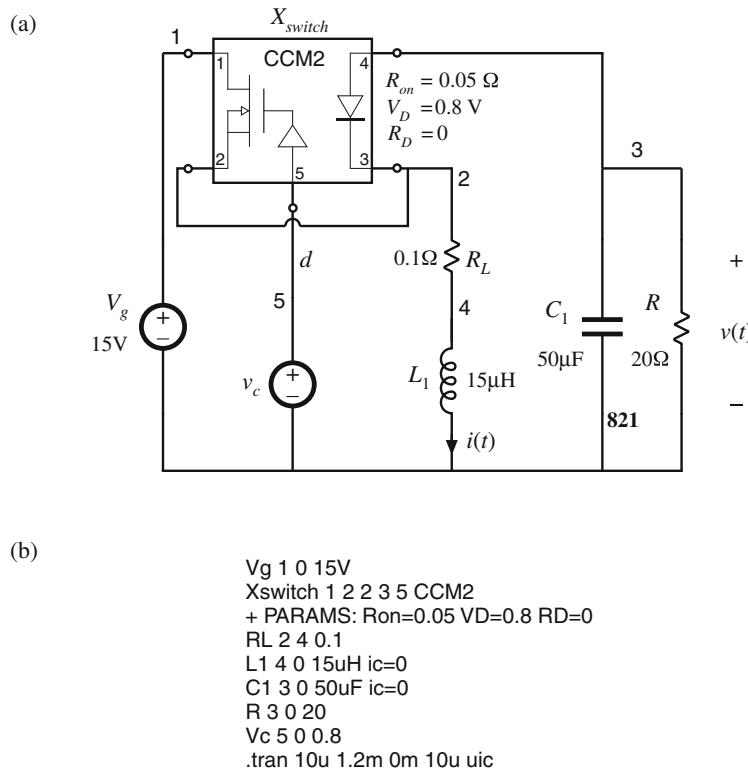
Therefore, the circuit model of Fig. 14.26 cannot be used to examine switching transitions or to predict switching losses in the converter. Nevertheless, basic switching operation is modeled, and a transient simulation can be used to find out how the converter waveforms evolve in time over many switching cycles. Transient simulation parameters are defined by the .tran line: the output time step is 1  $\mu\text{s}$ , the final simulation time is 1.2 ms, the output waveforms are generated from the start of simulation at time equal to zero, and the maximum allowed time step is 1  $\mu\text{s}$ . The uic (“use initial conditions”) option tells the simulator to start with all capacitor voltages and inductor currents equal to the specified initial values. For example,  $ic=0$  in the  $L_1$  line sets the initial inductor current to zero. In SPICE, the default initial conditions are always zero, so that  $ic=0$  statements can be omitted.



**Fig. 14.26** Buck-boost converter simulation example: (a) schematic of switching circuit model; (b) SPICE netlist

An averaged circuit model of the buck-boost converter is shown in Fig. 14.27. This circuit model is obtained by replacing the switch network in the converter of Fig. 14.25 by the CCM2 subcircuit. Notice that the circuits and the netlists of Fig. 14.26 and Fig. 14.27 are very similar. The only difference is that the switching devices in the converter circuit of Fig. 14.26 are replaced by the CCM2 subcircuit  $X_{switch}$  in Fig. 14.27. Also, the pulsating source  $v_c(t)$  in the switching circuit is replaced by a constant voltage source  $v_c$  equal to the switch duty cycle  $D = 0.8$ .

The inductor current and the capacitor voltage waveforms during the start-up transient are shown in Fig. 14.28. For comparison, the waveforms obtained by transient simulation of the switching converter circuit shown in Fig. 14.26, and by simulation of the averaged circuit model of Fig. 14.27 are shown. Switching ripples can be observed in the waveforms obtained by simulation of the switching circuit model. The converter transient response is governed by the converter natural time constants. Since these time constants are much longer than the switching period, the converter start-up transient responses in Fig. 14.28 take many switching cycles to reach the steady state. In the results obtained by simulation of the averaged circuit model, the switching ripples are removed, but the low-frequency portions of the converter transient responses, which are governed by the natural time constants of the converter network, match very closely the responses obtained by simulation of the switching circuit.

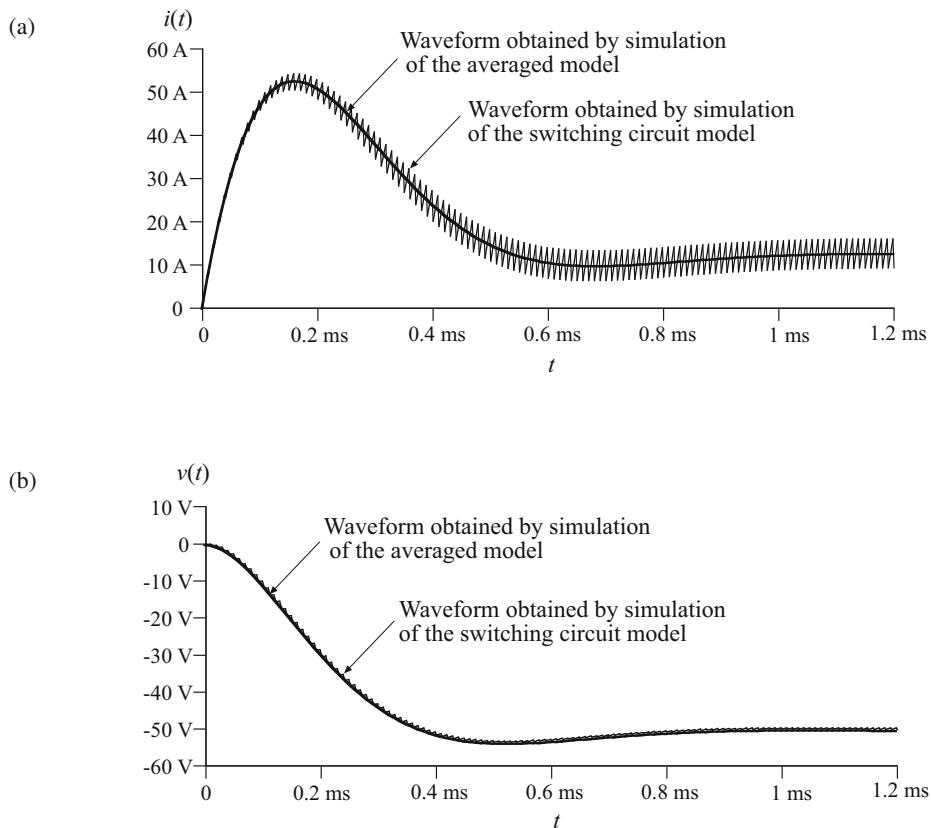


**Fig. 14.27** Buck-boost converter simulation example: (a) schematic of averaged circuit model; (b) SPICE netlist

Based on the results shown in Fig. 14.28, we can see that converter components are exposed to significantly higher current stresses during the start-up transient than during steady state operation. The problem of excessive stresses in the start-up transient is quite typical for switching power converters. Practical designs usually include a “soft-start” circuit, where the switch duty cycle is slowly increased from zero to the steady-state value to reduce start-up transient stresses.

This simulation example illustrates how an averaged circuit model can be used in place of a switching circuit model to investigate converter large-signal transient responses. An advantage of the averaged circuit model is that transient simulations can be completed much more quickly because the averaged model is time invariant, and the simulator does not spend time computing the details of the fast switching transitions. This advantage can be important in simulations of larger electronic systems that include switching power converters.

Converter averaged circuit models are nonlinear but time-invariant. This brings up another important advantage of averaged simulation models: SPICE ac simulations can be used to linearize the model numerically, and generate small-signal frequency responses of interest. The ac simulations can be easily performed over ranges or dc operating points or sets of parameter values. This is not possible with switching circuit models. Examples of small-signal ac simulations are given in Chap. 15.



**Fig. 14.28** Inductor current (a) and output voltage (b) waveforms obtained by transient simulation of the switching converter circuit shown in Fig. 14.26 and by simulation of the averaged circuit model of Fig. 14.27

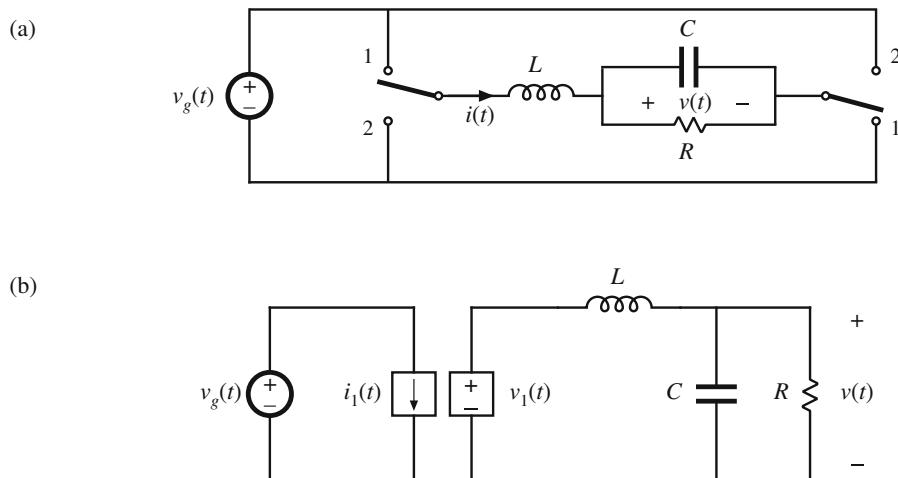
## 14.4 Summary of Key Points

1. The circuit averaging approach to converter modeling requires that the switch elements be replaced by dependent sources having waveforms identical to those of the actual switches. The converter waveforms then are averaged, and an averaged equivalent circuit model is obtained. This approach provides the theoretical basis for averaged switch modeling, in which the switch network of a converter is replaced by an averaged switch model, resulting in an averaged converter equivalent circuit.
2. Averaged switch modeling effectively replaces the switch elements of a CCM converter with a dc transformer model. A small-signal ac switch model can additionally provide an ac equivalent circuit for the converter. While these models may acquire a form that is different from those of earlier chapters, the models are equivalent and yield the same predictions of operating points and small-signal transfer functions.

3. The averaged switch approach is especially convenient for SPICE-based computer simulation. The switching elements are replaced by an averaged subcircuit. Typically the simulation runs much faster and is less prone to diverge. Models may include losses, dynamics, and be embedded in a larger system.
4. Indirect power is the portion of the converter input power that is converted to high frequency by the switch network, temporarily stored in reactive elements, converted back to dc or low frequency by the switch network, and output to the load. These processes incur ac loss that may significantly impact the converter efficiency.

## PROBLEMS

- 14.1** Use the circuit averaging to derive the dc and small-signal ac equivalent circuit of the buck converter with input filter, illustrated in Fig. 2.33. All elements are ideal.
- 14.2** Circuit averaging of the bridge inverter circuit of Fig. 14.29a.

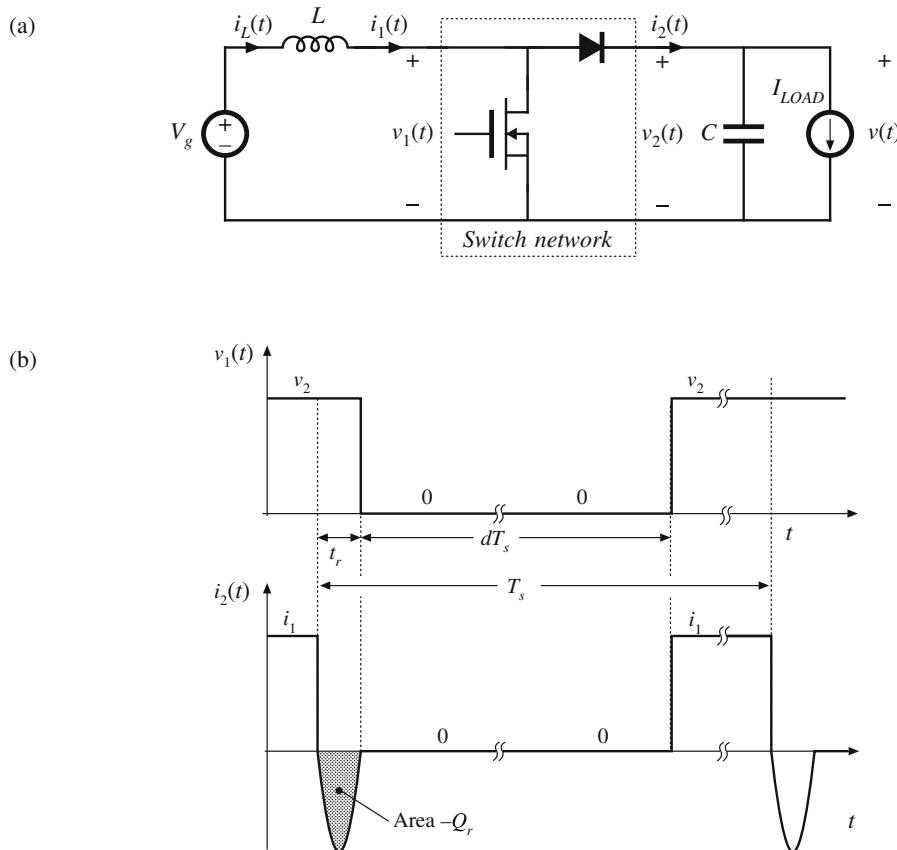


**Fig. 14.29** Bridge inverter, Problem 14.2: (a) circuit, (b) large-signal averaged model

- (a) Show that the converter of Fig. 14.29a can be written in the electrically identical form shown in Fig. 14.29b. Sketch the waveforms  $i_1(t)$  and  $v_1(t)$ .
- (b) Use the circuit averaging method to derive a large-signal averaged model for this converter.
- (c) Perturb and linearize your circuit model of part (b), to obtain a single equivalent circuit that models dc and small-signal ac signals in the bridge inverter.
- 14.3** Use the circuit averaging method to derive an equivalent circuit that models dc and small-signal ac signals in the buck-boost converter. You may assume that the converter operates in the continuous conduction mode, and that all elements are ideal.

- (a) Give a time-invariant electrically identical circuit, in which the switching elements are replaced by equivalent voltage and current sources. Define the waveforms of the sources.
- (b) Derive a large-signal averaged model for this converter.
- (c) Perturb and linearize your circuit model of part (b), to obtain a single equivalent circuit that models dc and small-signal ac signals in the buck-boost converter.
- 14.4** In a two-switch PWM converter operating in CCM, the transistor switch absorbs dc power  $P_{dc}$  and delivers ac power  $P_{ac} = P_{dc}$  to the rest of the circuit. On the other hand, the rectifier switch absorbs  $P_{ac}$  from the circuit, and delivers  $P_{dc}$ . The converter dc output power  $P_{out}$  can be written in the form
- $$P_{out} = P_{direct} + P_{indirect}$$
- where  $P_{indirect}$  equals the ac power  $P_{ac}$  processed by the switches. Reference polarities are selected so that  $P_{out} > 0$ ,  $P_{direct} > 0$ ,  $P_{indirect} > 0$ . You may assume that losses can be neglected. Derive expressions for the output power  $P_{out}$  and for the indirect power  $P_{indirect}$  as functions of  $V_g$ ,  $I_{load}$ , and  $D$ , and expressions for  $P_{indirect}/P_{out}$  and  $P_{direct}/P_{out}$  as functions of the dc conversion ratio  $M = V/V_g$  for two cases:
- Buck converter shown in Fig. 4.8.
  - Ćuk converter shown Fig. 2.20.
- 14.5** Use the averaged switch modeling technique to derive an ac equivalent circuit model for the buck-boost converter of Fig. 7.42:
- Replace the switches in Fig. 7.42 with the averaged switch model given in Fig. 14.17c.
  - Compare your result with the model given in Fig. 7.16b. Show that the two models predict the same small-signal line-to-output transfer function  $G_{vg}(s) = \hat{v}/\hat{v}_g$ .
- 14.6** Modify the CCM dc and small-signal ac averaged switch models of Fig. 14.17, to account for MOSFET on-resistance  $R_{on}$  and diode forward voltage drop  $V_D$ .
- 14.7** Use the averaged switch modeling technique to derive a dc and ac equivalent circuit model for the flyback converter of Fig. 7.19. You can neglect all losses and the transformer leakage inductances.
- Define a switch network containing the transistor  $Q_1$  and the diode  $D_1$  as in Fig. 14.4a. Derive a large-signal averaged switch model of the switch network. The model should account for the transformer turns ratio  $n$ .
  - Perturb and linearize the model you derived in part (a) to obtain the dc and ac small-signal averaged switch model. Verify that for  $n = 1$  your model reduces to the model shown in Fig. 14.4d.
  - Using the averaged switch model you derived in part (b), sketch a complete dc and small-signal ac model of the flyback converter. Solve the model for the steady-state conversion ratio  $M(D) = V/V_g$ .
  - The averaged switch models you derived in parts (a) and (b) could be used in other converters having an isolation transformer. Which ones?
- 14.8** An ideal buck converter operates with input voltage  $V_g$ , output current  $I_{load}$ , and duty cycle  $D$ . Derive expressions for the output power and for the indirect power, as functions of  $V_g$ ,  $I_{load}$ , and  $D$ .

- 14.9** Ideal buck, boost, and buck-boost converters operate with input voltage  $V_g$ , output current  $I_{load}$ , and duty cycle  $D$ . For each converter, derive expressions for the ratio of indirect power to output power  $P_{indirect}/P_{load}$ .
- 14.10** In the flyback converter of Fig. 7.19, the transistor on-resistance is  $R_{on}$ , and the diode forward voltage drop is  $V_D$ . Other losses and the transformer leakage inductances can be neglected. Derive a dc and small-signal ac averaged switch model for the switch network containing the transistor  $Q_1$  and the diode  $D_1$ . The model should account for the on-resistance  $R_{on}$ , the diode forward voltage drop  $V_D$ , and the transformer turns ratio  $n$ .
- 14.11** In the boost converter of Fig. 14.30a, the  $v_1(t)$  and  $i_2(t)$  waveforms of Fig. 14.30b are observed. During the transistor turn-on transition, a reverse current flows through the diode which removes the diode stored charge. As illustrated in Fig. 14.30b, the reverse current spike has area  $-Q_r$ , and duration  $t_r$ . The inductor winding has resistance  $R_L$ . You may neglect all losses other than the switching loss due to the diode stored charge and the conduction loss due to the inductor winding resistance.



**Fig. 14.30** Boost converter and waveforms illustrating reverse recovery of the diode. Averaged switch modeling in this converter is addressed in Problem 14.11

- (a) Derive an averaged switch model for the boost switch network in Fig. 14.30a.
- (b) Use your result of part (a) to sketch a dc equivalent circuit model for the boost converter.
- (c) The diode stored charge can be expressed as a function of the current  $I_1$  as:

$$Q_r = k_q \sqrt{I_1}$$

while the reverse recovery time  $t_r$  is approximately constant. Given  $V_g = 100 V$ ,  $D = 0.5$ ,  $f_s = 100 kHz$ ,  $k_q = 100nC/A^{1/2}$ ,  $t_r = 100 ns$ ,  $R_L = 0.1 \Omega$ , use a dc sweep simulation to plot the converter efficiency as a function of the load current  $I_{LOAD}$  in the range:

$$1A \leq I_{LOAD} \leq 10A$$



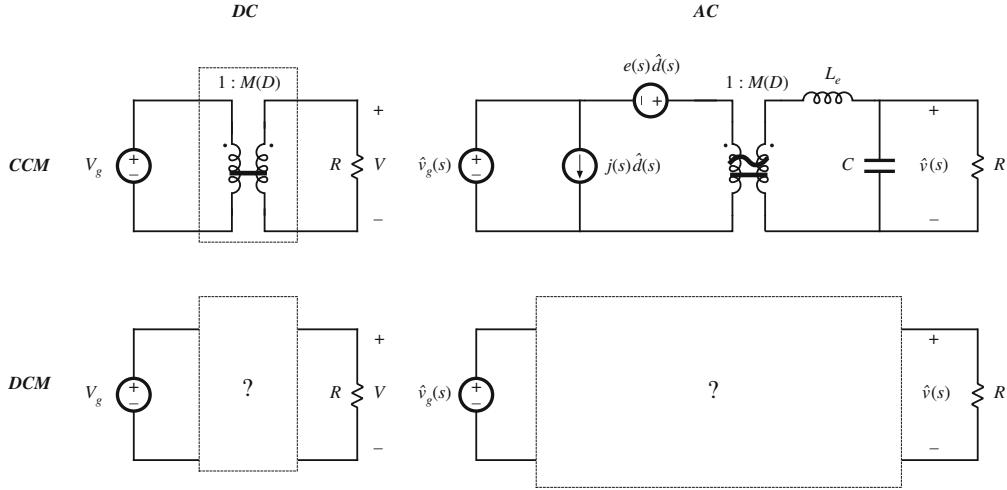
## AC and DC Equivalent Circuit Modeling of the Discontinuous Conduction Mode

So far, we have derived equivalent circuit models for dc–dc pulse-width modulation (PWM) converters operating in the continuous conduction mode. As illustrated in Fig. 15.1, the basic dc conversion property is modeled by an effective dc transformer, having a turns ratio equal to the conversion ratio  $M(D)$ . This model predicts that the converter has a voltage-source output characteristic, such that the output voltage is essentially independent of the load current or load resistance  $R$ . We have also seen how to refine this model, to predict losses and efficiency, converter dynamics, and small-signal ac transfer functions. We found that the transfer functions of the buck converter contain two low-frequency poles, owing to the converter filter inductor and capacitor. The control-to-output transfer functions of the boost and buck–boost converters additionally contain a right half-plane zero. Finally, we have seen how to utilize these results in the design of converter control systems.

What are the basic dc and small-signal ac equivalent circuits of converters operating in the discontinuous conduction mode (DCM)? It was found in Chap. 5 that, in DCM, the output voltage becomes load-dependent: the conversion ratio  $M(D, K)$  is a function of the dimensionless parameter  $K = 2L/RT_s$ , which in turn is a function of the load resistance  $R$ . So the converter no longer has a voltage-source output characteristic, and hence the dc transformer model is less appropriate.

In Sect. 15.1, a buck–boost DCM converter example is used to introduce DCM converter ac waveforms and averaged dynamics. It is shown that the moving average of the inductor voltage waveform is zero or approximately zero at all times, which is why, in practice, high-frequency inductor dynamics can usually be neglected in DCM, and DCM converters exhibit simpler, reduced-order dynamic responses compared to operation in the continuous conduction mode.

Based on the approximation that the moving average of the inductor voltage waveform is zero at all times, the averaged switch modeling approach [70–74, 126, 130, 131] is employed in Sect. 15.2 to derive equivalent circuits of the DCM switch network. It is shown that the *loss-free resistor* model [132–134] is the averaged switch model of the DCM switch network. This equivalent circuit represents the steady-state and large-signal dynamic characteristics of the DCM switch network, in a clear and simple manner. In the discontinuous conduction mode, the average transistor voltage and current obey Ohm’s law, and hence the transistor is modeled by an effective resistor  $R_e$ . The average diode voltage and current obey a power source characteristic, with power equal to the power effectively dissipated in  $R_e$ . Therefore, the diode is modeled with a *dependent power source*.



**Fig. 15.1** The objective of this chapter is the derivation of large-signal dc and small-signal ac equivalent circuit models for converters operating in the discontinuous conduction mode

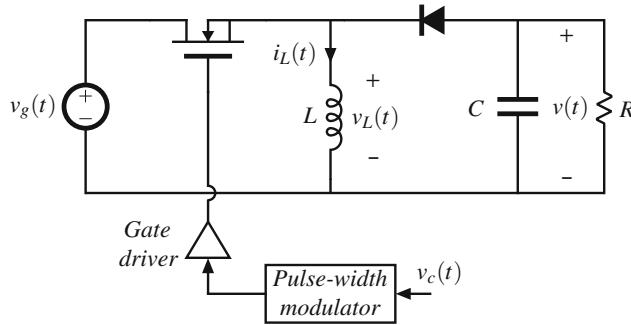
Section 15.4 addresses simulation models for converters that may operate in CCM or DCM. An average switch model that automatically switches between modes is derived, and this model is implemented in SPICE.

Since most converters operate in discontinuous conduction mode at some operating points, small-signal ac DCM models are needed, to prove that the control systems of such converters are correctly designed. In Sect. 15.3, a small-signal model of the DCM switch network is derived by linearization of the loss-free resistor model. The transfer functions of DCM converters are quite different from their respective CCM transfer functions. The basic DCM buck, boost, and buck-boost converters essentially exhibit simple single-pole transfer functions [15, 135], while high-frequency dynamics can usually be neglected. So the basic converters operating in DCM are easy to control; for this reason, converters are sometimes purposely operated in DCM for all loads. The transfer functions of higher-order converters such as the DCM Ćuk or SEPIC are considerably more complicated; but again, one pole is shifted to high frequency, where it has negligible practical effect. This chapter concludes, in Sect. 15.5, with a discussion of high-frequency dynamics of DCM converters. The more detailed analysis predicts that the high-frequency dynamics of DCM converters are related to the sampling process associated with the pulse-width modulator, and the nature of the response of the inductor current to duty-cycle perturbations [136]. This behavior can be modeled by an effective pole in the vicinity of the switching frequency.

## 15.1 Introduction to DCM Converter Dynamics

Consider the buck-boost converter of Fig. 15.2. The transistor switch duty cycle is modulated by a sinusoidal PWM input signal,

$$v_c(t) = V_c + V_m \sin \omega_m t \quad (15.1)$$



**Fig. 15.2** Buck-boost converter example. The transistor switch duty cycle is modulated by the PWM input signal  $v_c(t)$

where the modulation frequency  $f_m = \omega_m/(2\pi)$  is much smaller than the converter switching frequency  $f_s$ . Figure 15.3 shows the converter switching and averaged waveforms over a modulation period. In this example, the inductor current ripple is so large that the converter operates in DCM at all times. As shown in Fig. 15.3b, inductor current waveform  $i_L(t)$  consists of triangular pulses that start from zero and end at zero within a switching period. As expected, the moving average of the inductor current,  $\langle i_L(t) \rangle_{T_s}$ , retains low-frequency dynamics of the inductor current, including a dc component and an ac component in response to the sinusoidally modulated transistor duty cycle. Similarly, the moving average of the output voltage,  $\langle v(t) \rangle_{T_s}$ , includes a dc component  $V$ , and an ac variation resulting from the sinusoidally modulated duty cycle, while the switching ripple in  $v(t)$  is removed, as shown in Fig. 15.3c. It is of particular interest to examine the inductor voltage switching and averaged waveforms shown in Fig. 15.3d. The switching waveform  $v_L(t)$  is a pulsating waveform that follows the DCM pattern described in Chap. 5,

$$v_L(t) = \begin{cases} v_g(t) & \text{during } d_1 T_s \text{ when transistor is on and diode is off} \\ v(t) & \text{during } d_2 T_s \text{ when transistor is off and diode is on} \\ 0 & \text{during } d_3 T_s \text{ when both transistor and diode are off} \end{cases} \quad (15.2)$$

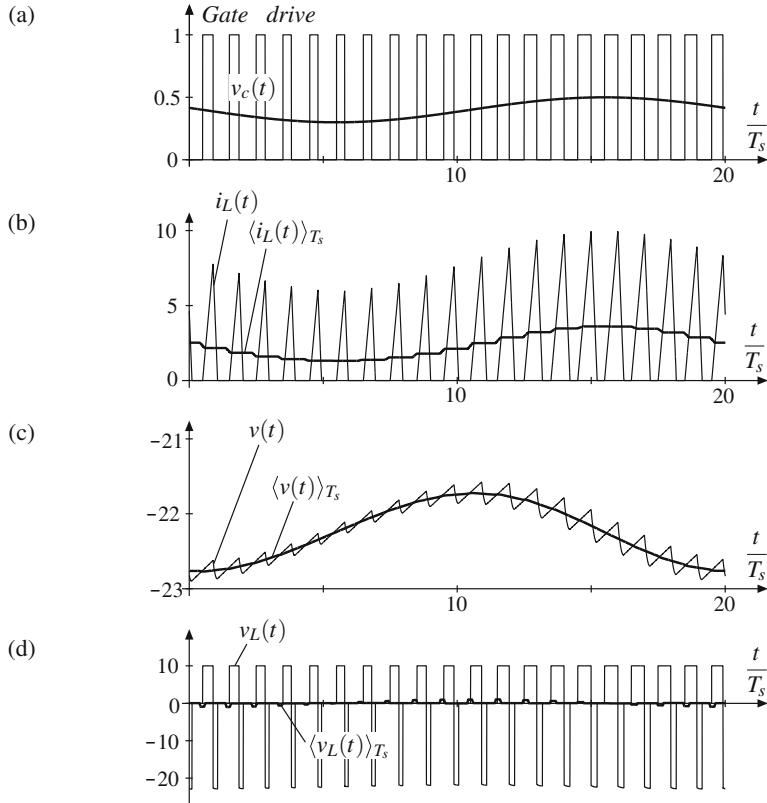
where  $d_1$  is the transistor switch duty cycle and  $d_1 + d_2 + d_3 = 1$ .

One may observe that the moving average  $\langle v(t) \rangle_{T_s}$  is either equal to zero or is close to zero at all times. To explain the DCM inductor dynamics, consider the inductor current and the averaged inductor voltage waveforms shown in Fig. 15.4 over a couple of switching periods. As a result of duty-cycle modulation, the transistor duty cycle in the second period is  $\Delta d$  longer than the duty cycle  $d_1$  in the first period. For an averaging interval centered around time  $t$ , the moving average of  $v_L(t)$  can be found as

$$\langle v_L(t) \rangle_{T_s} = \frac{1}{T_s} \int_{t-T_s/2}^{t+T_s/2} v_L(\tau) d\tau = \frac{L}{T_s} (i_L(t + T_s/2) - i_L(t - T_s/2)) \quad (15.3)$$

For the example shown in Fig. 15.4,

$$i_L(t - T_s/2) = i_L(t + T_s/2) = 0 \quad (15.4)$$



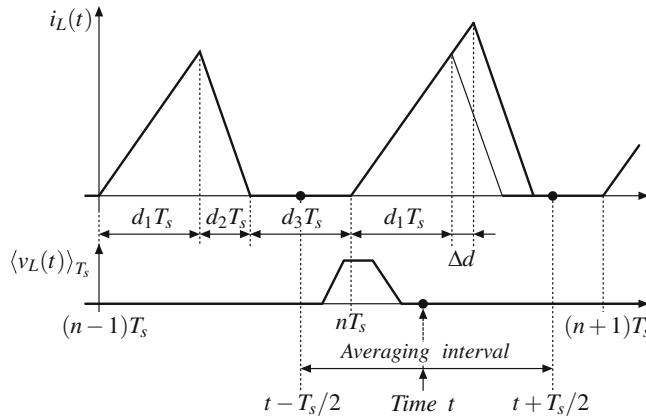
**Fig. 15.3** Switching and averaged waveforms in the buck-boost converter of Fig. 15.2. In this example, the converter parameters are  $V_g = 10$  V,  $L = 5 \mu\text{H}$ ,  $C = 22 \mu\text{F}$ ,  $f_s = 1/T_s = 100$  kHz,  $R = 30 \Omega$ , PWM gain  $1/V_M = 1 \text{ V}^{-1}$ ,  $v_c(t) = 0.4 + 0.1 \sin(\omega_m t)$ , modulation frequency  $f_m = f_s/20 = 5$  kHz

and hence

$$\langle v_L(t) \rangle_{T_s} = 0 \quad (15.5)$$

It follows from Eq. (15.3) that  $\langle v_L(t) \rangle_{T_s} = 0$  whenever  $i_L(t + T_s/2) = i_L(t - T_s/2)$ , which is always the case over portions of a switching period in DCM—even when the converter is not in equilibrium. In the examples of Figs. 15.3 or 15.4,  $\langle v_L(t) \rangle_{T_s} \neq 0$  only during time intervals of length  $d_2 T_s$  and only when duty cycle varies between successive switching periods. Referring to Fig. 15.3d, the nonzero pulses in  $\langle v_L(t) \rangle_{T_s} \neq 0$  clearly contain a small low-frequency component in response to the duty-cycle modulation. However, as discussed further in Sect. 15.5, the relatively short, relatively low amplitude nonzero pulses in  $\langle v_L(t) \rangle_{T_s}$ , which are related to sampling effects and high-frequency dynamics, do not affect the dominant, low-frequency DCM dynamics significantly. In conclusion, in DCM, we can simply assume that the inductor volt-seconds balance holds not only in equilibrium but at all times:

$$\langle v_L(t) \rangle_{T_s} = \frac{1}{T_s} \int_{t-T_s/2}^{t+T_s/2} v_L(\tau) d\tau \approx 0 \quad (15.6)$$



**Fig. 15.4** DCM inductor current  $i_L(t)$  and the moving average  $\langle v_L(t) \rangle_{T_s}$  of the inductor voltage

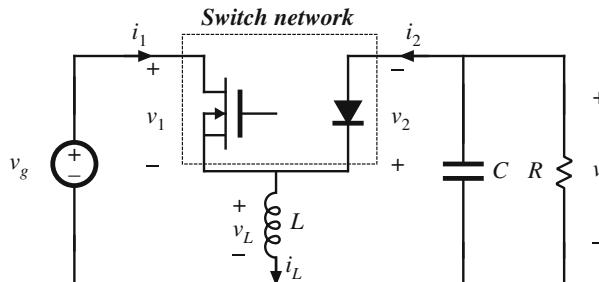
In the next section, following the averaged switch modeling approach, the approximation given by Eq. (15.6) is used to derive dc and ac models of DCM converters.

## 15.2 DCM Averaged Switch Model

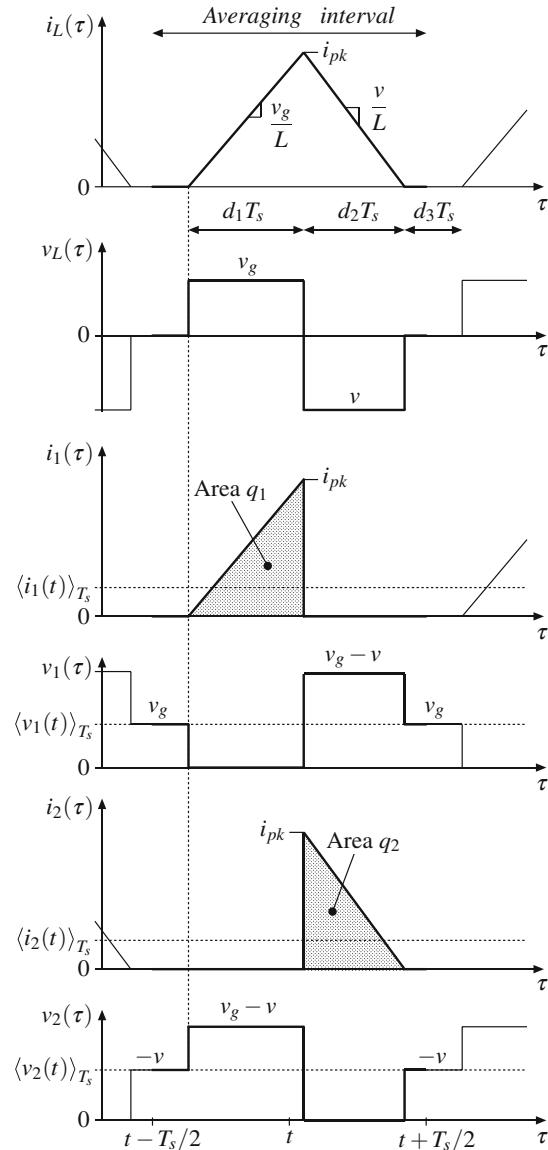
Consider the buck-boost converter of Fig. 15.5. Let us follow the averaged switch modeling approach of Sect. 14.1, to derive an equivalent circuit that models the averaged terminal waveforms of the switch network. The general two-switch network and its terminal quantities  $v_1(t)$ ,  $i_1(t)$ ,  $v_2(t)$ , and  $i_2(t)$  are defined as illustrated in Fig. 15.5, consistent with Fig. 14.4a. The inductor and switch network voltage and current waveforms are illustrated in Fig. 15.6, for DCM operation.

During the subinterval  $d_1 T_s$ , while the transistor conducts, the inductor current increases from zero with a slope of  $v_g(t)/L$ . At the end of this subinterval, the inductor current  $i_L(t)$  attains the peak value given by

$$i_{pk} = \frac{v_g}{L} d_1 T_s \quad (15.7)$$



**Fig. 15.5** Buck-boost converter example, with switch network terminal quantities identified



**Fig. 15.6** Inductor and switch network voltage and current waveforms

During the next subinterval, while the diode conducts, the inductor current decreases with a slope equal to  $v(t)/L$ . This subinterval ends when the inductor current drops to zero and the diode becomes reverse-biased. The length of this subinterval is  $d_2 T_s$ . The inductor current and the inductor voltage then remain zero for the balance  $d_3 T_s$  of the switching period.

A DCM averaged switch model can be derived with reference to the waveforms of Fig. 15.6. The averaging interval of length  $T_s$ , centered around time  $t$  is highlighted.

Following the approach of Sect. 14.1.2, let us find the average values of the switch network terminal waveforms  $v_1(t)$ ,  $v_2(t)$ ,  $i_1(t)$ , and  $i_2(t)$  in terms of the converter state variables (inductor currents and capacitor voltages), the input voltage  $v_g(t)$ , and the subinterval lengths  $d_1$  and  $d_2$ .

To find the average switch network input voltage  $\langle v_1(t) \rangle_{T_s}$ , or the average transistor voltage, it is convenient to start from a converter voltage loop equation

$$v_1 = v_g - v_L \quad (15.8)$$

Averaging applied to Eq. (15.8) yields

$$\langle v_1 \rangle_{T_s} = \langle v_g \rangle_{T_s} - \langle v_L \rangle_{T_s} \quad (15.9)$$

Taking the approximation Eq. (15.6) into account, we have

$$\langle v_1 \rangle_{T_s} = \langle v_g \rangle_{T_s} \quad (15.10)$$

For the averaging interval shown in Fig. 15.6, one may note that  $\langle v_L \rangle_{T_s} = 0$  exactly.

Similar analysis, based on the voltage loop equation  $v_2 = v_L - v$ , leads to the following expression for the average diode voltage:

$$\langle v_2 \rangle_{T_s} = \langle -v \rangle_{T_s} \quad (15.11)$$

The average switch network input current  $\langle i_1(t) \rangle_{T_s}$  is found by integrating the  $i_1(t)$  waveform of Fig. 15.6 over one switching period:

$$\langle i_1(t) \rangle_{T_s} = \frac{1}{T_s} \int_{t-T_s/2}^{t+T_s/2} i_1(t) dt = \frac{q_1}{T_s} \quad (15.12)$$

The integral  $q_1$  is equal to the area under the  $i_1(t)$  waveform during the first subinterval. This area is easily evaluated using the triangle area formula:

$$q_1 = \int_{t-T_s/2}^{t+T_s/2} i_1(t) dt = \frac{1}{2} (d_1 T_s) (i_{pk}) \quad (15.13)$$

Substitution of Eqs. (15.7), (15.13), and (15.10) into Eq. (15.12) gives

$$\langle i_1(t) \rangle_{T_s} = \frac{d_1^2 T_s}{2L} \langle v_g(t) \rangle_{T_s} = \frac{d_1^2 T_s}{2L} \langle v_1(t) \rangle_{T_s} \quad (15.14)$$

Note that  $\langle i_1(t) \rangle_{T_s}$  is not equal to  $d_1 \langle i_L(t) \rangle_{T_s}$ . Since the inductor current ripple is not small, it is necessary to sketch the actual input current waveform, including the large switching ripple, and then correctly compute the average as in Eqs. (15.12) to (15.14).

The average diode current  $\langle i_2(t) \rangle_{T_s}$  is found in a manner similar to that used above for  $\langle i_1(t) \rangle_{T_s}$ :

$$\langle i_2(t) \rangle_{T_s} = \frac{1}{T_s} \int_{t-T_s/2}^{t+T_s/2} i_2(t) dt = \frac{q_2}{T_s} \quad (15.15)$$

The integral  $q_2$  is equal to the area under the  $i_2(t)$  waveform during the  $d_2 T_s$  subinterval. This area is evaluated using the triangle area formula:

$$q_2 = \int_{t-T_s/2}^{t+T_s/2} i_2(t) dt = \frac{1}{2} (d_2 T_s) (i_{pk}) \quad (15.16)$$

Substitution of Eqs. (15.7), (15.16), and (15.10) into Eq. (15.15) leads to:

$$\langle i_2(t) \rangle_{T_s} = \frac{d_1 d_2 T_s}{2L} \langle v_g(t) \rangle_{T_s} = \frac{d_1 d_2 T_s}{2L} \langle v_1(t) \rangle_{T_s} \quad (15.17)$$

Equations (15.10), (15.11), (15.14), and (15.17) constitute the averaged terminal equations of the switch network in the DCM buck-boost converter. In these equations, it remains to express the subinterval length  $d_2$  in terms of the switch duty cycle  $d_1 = d$ , and the converter averaged waveforms. Considering the averaging interval shown in Fig. 15.6, we note that  $i_L(t - T_s/2) = i_L(t + T_s/2) = 0$ . There is no net change in inductor current, and no net volt-seconds are applied to the inductor over this averaging interval. In other words, the average inductor voltage computed over the averaging interval shown in Fig. 15.6 is zero,

$$\langle v_L(t) \rangle_{T_s} = d_1 \langle v_g(t) \rangle_{T_s} + d_2 \langle v(t) \rangle_{T_s} = 0 \quad (15.18)$$

Based on the approximation given by Eq. (15.5) we conclude that Eq. (15.18) can be used to find the length of the  $d_2 T_s$  subinterval in general, even when the converter is not in equilibrium:

$$d_2(t) = -d_1(t) \frac{\langle v_g(t) \rangle_{T_s}}{\langle v(t) \rangle_{T_s}} \quad (15.19)$$

Substitution of Eq. (15.19) into Eqs. (15.14) and (15.17) allows us to obtain simple expressions for the averaged terminal waveforms of the switch network in the discontinuous conduction mode:

$$\langle i_1(t) \rangle_{T_s} = \frac{d_1^2 T_s}{2L} \langle v_1(t) \rangle_{T_s} \quad (15.20)$$

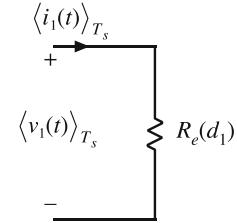
$$\langle i_2(t) \rangle_{T_s} = \frac{d_1^2 T_s}{2L} \frac{\langle v_1(t) \rangle_{T_s}^2}{\langle v_2(t) \rangle_{T_s}} \quad (15.21)$$

Let us next construct an equivalent circuit corresponding to the averaged switch network equations (15.20) and (15.21). The switch network input port is modeled by Eq. (15.20). This equation states that the average input current  $\langle i_1(t) \rangle_{T_s}$  is proportional to the applied input voltage  $\langle v_1(t) \rangle_{T_s}$ . In other words, the low-frequency components of the switch network input port obey Ohm's law:

$$\langle i_1(t) \rangle_{T_s} = \frac{\langle v_1(t) \rangle_{T_s}}{R_e(d_1)} \quad (15.22)$$

where the effective resistance  $R_e$  is

$$R_e(d_1) = \frac{2L}{d_1^2 T_s} \quad (15.23)$$



**Fig. 15.7** Equivalent circuit that models the average waveforms of the switch input (transistor) port

An equivalent circuit is illustrated in Fig. 15.7. During the  $d_1 T_s$  subinterval, the slope of the input current waveform  $i_1(t)$  is proportional to the input voltage  $\langle v_g(t) \rangle_{T_s} = \langle v_1(t) \rangle_{T_s}$ , as illustrated in Fig. 15.6. As a result, the peak current  $i_{pk}$ , the total charge  $q_1$ , and the average input current  $\langle i_1(t) \rangle_{T_s}$ , are also proportional to  $\langle v_1(t) \rangle_{T_s}$ . Of course, there is no physical resistor inside the converter. Indeed, if the converter elements are ideal, then no heat is generated inside the converter. Rather, the power apparently consumed by  $R_e$  is transferred to the switch network output port.

The switch network output (diode) port is modeled by Eq. (15.21), or

$$\langle i_2(t) \rangle_{T_s} \langle v_2(t) \rangle_{T_s} = \frac{\langle v_1(t) \rangle_{T_s}^2}{R_e(d_1)} = \langle p(t) \rangle_{T_s} \quad (15.24)$$

Note that  $\langle v_1(t) \rangle_{T_s}^2 / R_e$  is the average power  $\langle p(t) \rangle_{T_s}$  apparently consumed by the effective resistor  $R_e(d_1)$ . Equation (15.24) states that this power flows out of the switch network output port. So the switch network consumes no net power—its average input and output powers are equal.

Equation (15.24) can also be derived by consideration of the inductor stored energy. During the first subinterval, the inductor current increases from 0 to  $i_{pk}$ . In the process, the inductor stores the following energy:

$$\frac{1}{2} L i_{pk}^2 = \frac{\langle v_1 \rangle_{T_s}^2 d_1 T_s^2}{2L} = \frac{\langle v_1 \rangle_{T_s}^2}{R_e(d_1)} T_s \quad (15.25)$$

Here,  $i_{pk}$  has been expressed in terms of  $\langle v_1(t) \rangle_{T_s}$  using Eqs. (15.7) and (15.10). This energy is transferred from the source  $v_g$ , through the switch network input terminals (i.e., through the transistor), to the inductor. During the second subinterval, the inductor releases all of its stored energy through the switch network output terminals (i.e., through the diode), to the output. The average output power can therefore be expressed as the energy transferred per cycle, divided by the switching period:

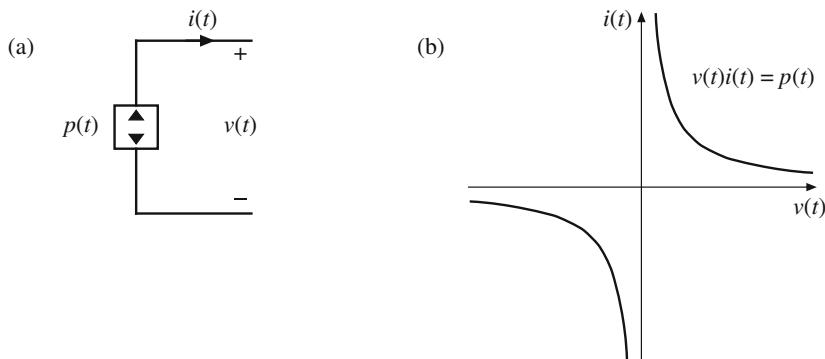
$$\langle p(t) \rangle_{T_s} = \left( \frac{\langle v_1 \rangle_{T_s}^2}{R_e(d_1)} T_s \right) \left( \frac{1}{T_s} \right) = \frac{\langle v_1 \rangle_{T_s}^2}{R_e(d_1)} \quad (15.26)$$

This power is transferred to the load, and hence

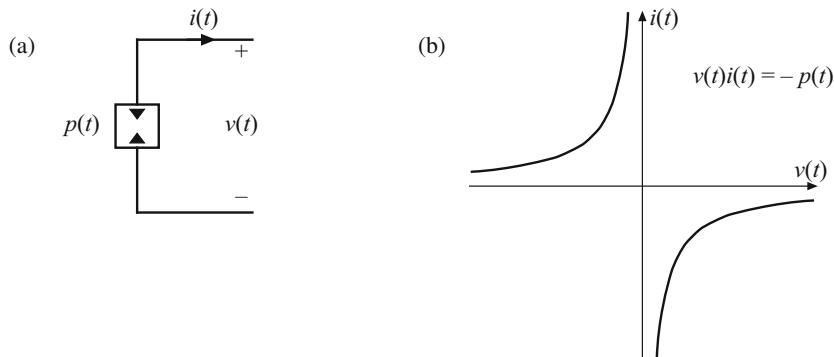
$$\langle v \rangle_{T_s} \langle i_2 \rangle_{T_s} = \langle v_2 \rangle_{T_s} \langle i_2 \rangle_{T_s} = \langle p(t) \rangle_{T_s} = \frac{\langle v_1 \rangle_{T_s}^2}{R_e(d_1)} \quad (15.27)$$

This result coincides with Eq. (15.24).

The average power  $\langle p(t) \rangle_{T_s}$  is independent of the load characteristics, and is determined solely by the effective resistance  $R_e$  and the applied switch network input terminal voltage or current. In other words, the switch network output port behaves as a source of power, equal



**Fig. 15.8** The dependent power source: (a) schematic symbol, (b)  $i$ - $v$  characteristic

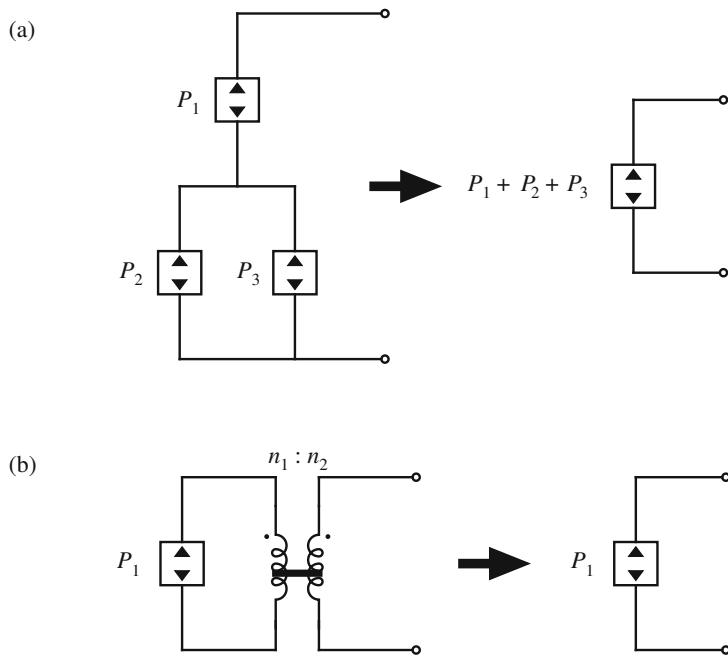


**Fig. 15.9** The dependent power sink: (a) schematic symbol, (b)  $i$ - $v$  characteristic

to the power apparently consumed by the effective resistance  $R_e$ . This behavior is represented schematically by the dependent power source symbol illustrated in Fig. 15.8. In any lossless two-port network, when the voltage and current at one port are independent of the characteristics of the external network connected to the second port, then the second port must exhibit a dependent power source characteristic [133]. This situation arises in a number of common power-processing applications, including switch networks operating in the discontinuous conduction mode.

The power source characteristic illustrated in Fig. 15.8b is symmetrical with respect to voltage and current; in consequence, the power source exhibits several unique properties. Similar to the voltage source, the ideal power source must not be short-circuited; otherwise, infinite current occurs. And similar to the current source, the ideal power source must not be open-circuited, to avoid infinite terminal voltage. The power source must be connected to a load capable of absorbing the power  $p(t)$ , and the operating point is defined by the intersection of the load and power source  $i$ - $v$  characteristics.

We can define a power sink element similarly, with reversal of the direction of power flow. The schematic symbol for this element is illustrated in Fig. 15.9, with its  $i$ - $v$  characteristic.

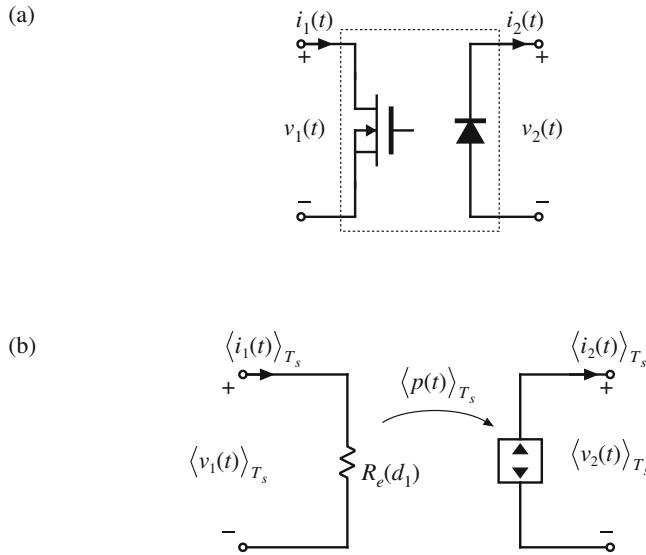


**Fig. 15.10** Circuit manipulations of power source elements: (a) combination of series- and parallel-connected power sources into a single equivalent power source, (b) invariance of the power source to reflection through an ideal transformer of arbitrary turns ratio

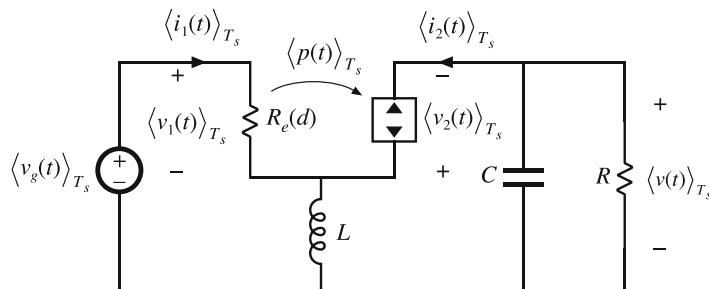
As illustrated in Fig. 15.10a, series-and parallel-connected power sources can be combined into a single power source, equal to the sum of the powers of the individual sources. Figure 15.10b illustrates how reflection of a power source through a transformer, having an arbitrary turns ratio, leaves the power source unchanged. Power sources are also invariant to duality transformations.

The averaged large-signal model of the general two-switch network in DCM is illustrated in Fig. 15.11b. The input port behaves effectively as resistance \$R\_e\$. The instantaneous power apparently consumed by \$R\_e\$ is transferred to the output port, and the output port behaves as a dependent power source. This lossless two-port network is called the *loss-free resistor* model (LFR) [132]. The loss-free resistor represents the basic power conversion properties of DCM switch networks [134]. It can be shown that the loss-free resistor models the averaged properties of DCM switch networks not only in the buck–boost converter, but also in other PWM converters.

When the switch network of the DCM buck–boost converter is replaced by the averaged model of Fig. 15.11b, the converter equivalent circuit of Fig. 15.12 is obtained. Upon setting all averaged waveforms to their quiescent values, and letting the inductor and capacitor become a short-circuit and an open-circuit, respectively, we obtain the dc model of Fig. 15.13.



**Fig. 15.11** The general two-switch network (a), and the corresponding averaged switch model in the discontinuous conduction mode (b). The average transistor waveforms obey Ohm's law, while the average diode waveforms behave as a dependent power source



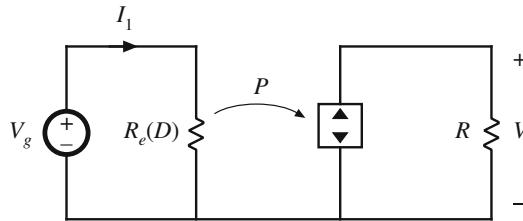
**Fig. 15.12** Replacement of the switch network of the DCM buck-boost converter with the loss-free resistor model

Systems containing power sources or loss-free resistors can usually be easily solved, by equating average source and load powers. For example, in the dc network of Fig. 15.13, the power flowing into the converter input terminals is

$$P = \frac{V_g^2}{R_e} \quad (15.28)$$

The power flowing into the load resistor is

$$P = \frac{V^2}{R} \quad (15.29)$$



**Fig. 15.13** Dc network example containing a loss-free resistor model

The loss-free resistor model states that these two powers must be equal:

$$P = \frac{V_g^2}{R_e} = \frac{V^2}{R} \quad (15.30)$$

Solution for the voltage conversion ratio  $M = V/V_g$  yields

$$\frac{V}{V_g} = \pm \sqrt{\frac{R}{R_e}} \quad (15.31)$$

Equation (15.31) is a general result, valid for any converter that can be modeled by a loss-free resistor and that drives a resistive load. Other arguments must be used to determine the polarity of  $V/V_g$ . In the buck-boost converter shown in Fig. 15.5, the diode polarity indicates that  $V/V_g$  must be negative. The steady-state value of  $R_e$  is

$$R_e(D) = \frac{2L}{D^2 T_s} \quad (15.32)$$

where  $D$  is the quiescent transistor duty cycle. Substitution of Eq. (15.32) into (15.31) leads to

$$\frac{V}{V_g} = -\sqrt{\frac{D^2 T_s R}{2L}} = -\frac{D}{\sqrt{K}} \quad (15.33)$$

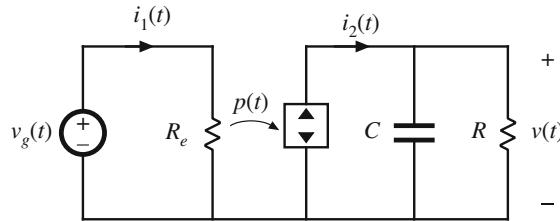
with  $K = 2L/RT_s$ . This equation coincides with the previous steady-state result given in Table 5.2.

Similar arguments apply when the waveforms contain ac components. For example, consider the network of Fig. 15.14, in which the voltages and currents are periodic functions of time. The rms values of the waveforms can be determined by simply equating the average source and load powers. The average power flowing into the converter input port is

$$P_{av} = \frac{V_{g,rms}^2}{R_e} \quad (15.34)$$

where  $P_{av}$  is the average power consumed by the effective resistance  $R_e$ . No average power is consumed by capacitor  $C$ , and hence the average power  $P_{av}$  must flow entirely into the load resistor  $R$ :

$$P_{av} = \frac{V_{rms}^2}{R} \quad (15.35)$$



**Fig. 15.14** Ac network example containing a loss-free resistor model

Upon equating Eqs. (15.34) and (15.35), we obtain

$$\frac{V_{rms}}{V_{g,rms}} = \sqrt{\frac{R}{R_e}} \quad (15.36)$$

Thus, the rms terminal voltages obey the same relationship as in the dc case.

Averaged equivalent circuits of the DCM buck, boost, and buck-boost converters, as well as the DCM Ćuk and SEPIC converters, are listed in Fig. 15.15. In each case, the averaged transistor waveforms obey Ohm's law, and are modeled by an effective resistance  $R_e$ . The averaged diode waveforms follow a power source characteristic, equal to the power effectively dissipated in  $R_e$ . For the buck, boost, and buck-boost converters,  $R_e$  is given by

$$R_e = \frac{2L}{d^2 T_s} \quad (15.37)$$

For the Ćuk and SEPIC converters,  $R_e$  is given by

$$R_e = \frac{2(L_1 \parallel L_2)}{d^2 T_s} \quad (15.38)$$

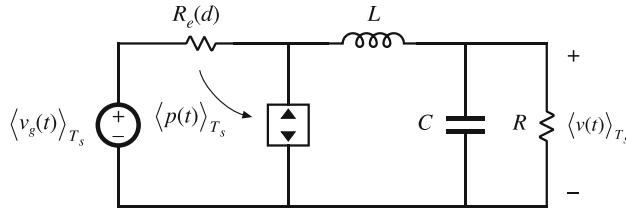
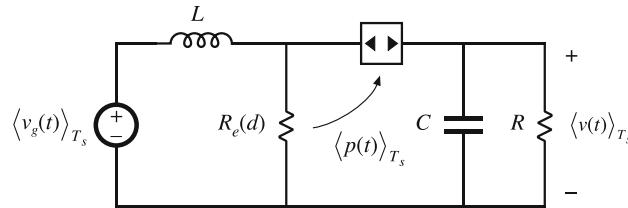
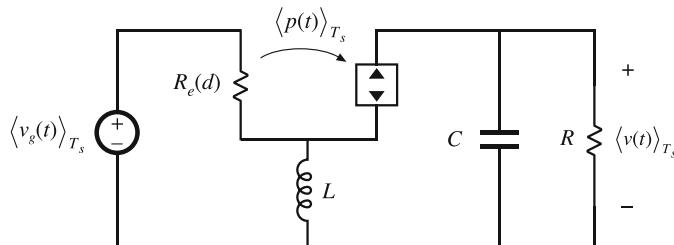
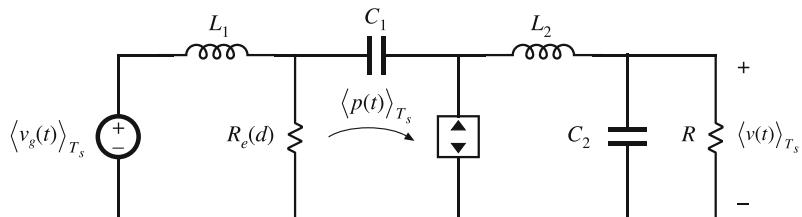
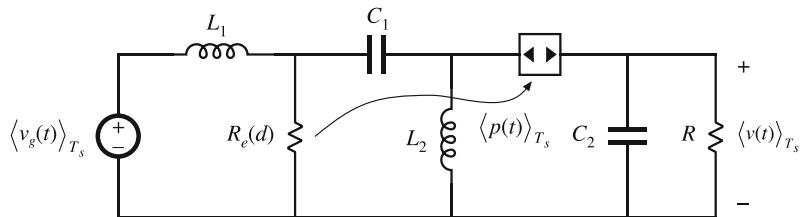
Here,  $d$  is the transistor duty cycle.

Steady-state conditions in the converters of Fig. 15.15 are found by letting the inductors and capacitors become short circuits and open circuits, respectively, and then solving the resulting dc circuits with  $d(t) = D$ . The buck-boost, Ćuk, and SEPIC then reduce to the circuit of Fig. 15.13. The buck and boost converters reduce to the circuits of Fig. 15.16. Equilibrium conversion ratios  $M = V/V_g$  of these converters are summarized in Table 15.1, as functions of  $R_e(D)$ . It can be shown that these converters operate in the discontinuous conduction mode whenever the load current  $I$  is less than the critical current  $I_{crit}$ :

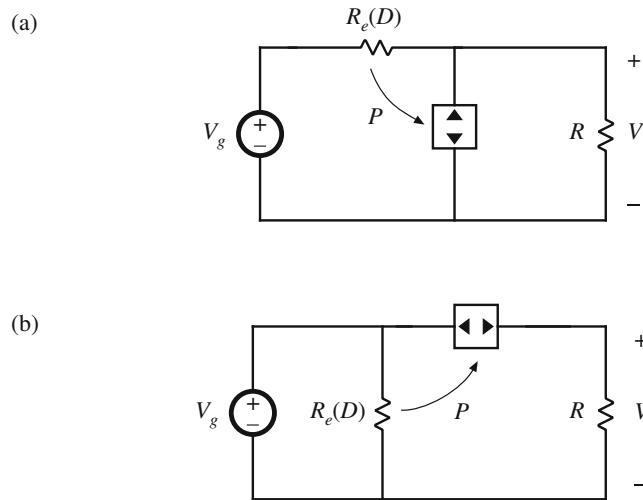
$$\begin{aligned} I > I_{crit} &\text{ for CCM} \\ I < I_{crit} &\text{ for DCM} \end{aligned} \quad (15.39)$$

For all of these converters,  $I_{crit}$  is given by

$$I_{crit} = \frac{1-D}{D} \frac{V_g}{R_e(D)} \quad (15.40)$$

**Buck****Boost****Buck-boost****Cuk****SEPIC**

**Fig. 15.15** Averaged large-signal equivalent circuits of five basic converters operating in the discontinuous conduction mode



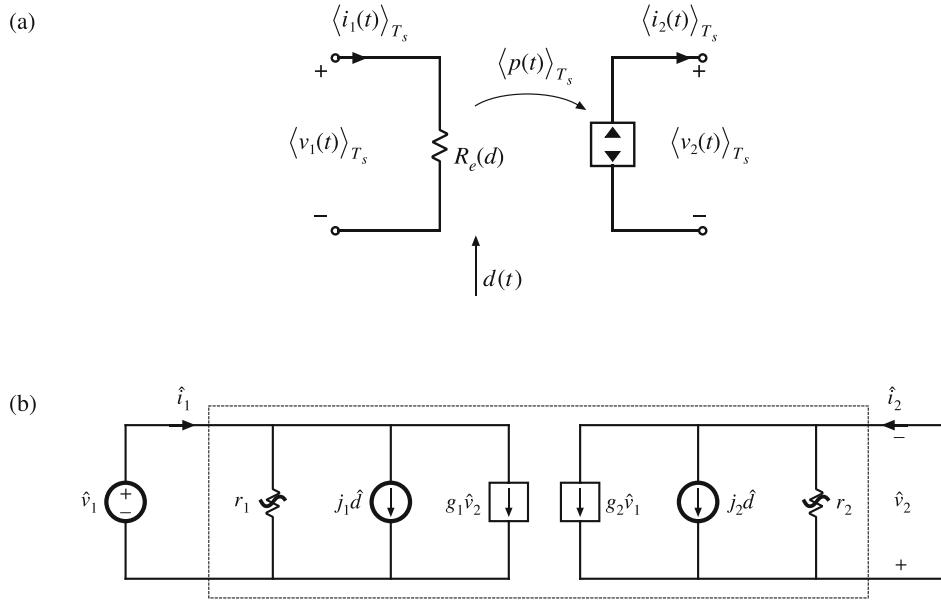
**Fig. 15.16** Dc equivalent circuits representing the buck (a) and boost (b) converters operating in DCM

**Table 15.1** CCM and DCM conversion ratios of basic converters

Converter	$M$ , CCM	$M$ , DCM
Buck	$D$	$\frac{2}{1 + \sqrt{1 + 4R_e/R}}$
Boost	$\frac{1}{1 - D}$	$\frac{1 + \sqrt{1 + 4R_e/R}}{2}$
Buck-boost, Ćuk	$\frac{-D}{1 - D}$	$-\sqrt{\frac{R}{R_e}}$
SEPIC	$\frac{D}{1 - D}$	$\sqrt{\frac{R}{R_e}}$

### 15.3 Small-Signal AC Modeling of the DCM Switch Network

The next step is construction of a small-signal equivalent circuit model for converters operating in the discontinuous conduction mode. In the large-signal ac equivalent circuits of Fig. 15.15, the averaged switch networks are nonlinear. Hence, construction of a small-signal ac model involves perturbation and linearization of the loss-free resistor network. The signals in the large-signal averaged DCM switch network model of Fig. 15.17a are perturbed about a quiescent operating point, as follows:



**Fig. 15.17** Averaged models of the general two-switch network in a converter operating in DCM: (a) large-signal model, (b) small-signal model

$$\begin{aligned}
 d(t) &= D + \hat{d}(t) \\
 \langle v_1(t) \rangle_{T_s} &= V_1 + \hat{v}_1(t) \\
 \langle i_1(t) \rangle_{T_s} &= I_1 + \hat{i}_1(t) \\
 \langle v_2(t) \rangle_{T_s} &= V_2 + \hat{v}_2(t) \\
 \langle i_2(t) \rangle_{T_s} &= I_2 + \hat{i}_2(t)
 \end{aligned} \tag{15.41}$$

Here,  $D$  is the quiescent value of the transistor duty cycle,  $V_1$  is the quiescent value of the applied average transistor voltage  $\langle v_1(t) \rangle_{T_s}$ , etc. The quantities  $\hat{d}(t)$ ,  $\hat{v}_1(t)$ , etc., are small ac variations about the respective quiescent values. It is desired to linearize the average switch network terminal equations (15.20) and (15.21).

Equations (15.20) and (15.21) express the average terminal currents  $\langle i_1(t) \rangle_{T_s}$  and  $\langle i_2(t) \rangle_{T_s}$  as functions of the transistor duty cycle  $d(t) = d_1(t)$  and the average terminal voltages  $\langle v_1(t) \rangle_{T_s}$  and  $\langle v_2(t) \rangle_{T_s}$ . Upon perturbation and linearization of these equations, we will therefore find that  $\hat{i}_1(t)$  and  $\hat{i}_2(t)$  are expressed as linear functions of  $\hat{d}(t)$ ,  $\hat{v}_1(t)$ , and  $\hat{v}_2(t)$ . So the small-signal switch network equations can be written in the following form:

$$\begin{aligned}
 \hat{i}_1 &= \frac{\hat{v}_1}{r_1} + j_1\hat{d} + g_1\hat{v}_2 \\
 \hat{i}_2 &= -\frac{\hat{v}_2}{r_2} + j_2\hat{d} + g_2\hat{v}_1
 \end{aligned} \tag{15.42}$$

These equations describe the two-port equivalent circuit of Fig. 15.17b.

The parameters  $r_1$ ,  $j_1$ , and  $g_1$  can be found by Taylor expansion of Eq. (15.20), as described in Sect. 7.2.8. The average transistor current  $\langle i_1(t) \rangle_{T_s}$ , Eq. (15.20), can be expressed in the following form:

$$\langle i_1(t) \rangle_{T_s} = \frac{\langle v_1(t) \rangle_{T_s}}{R_e(d(t))} = f_1(\langle v_1(t) \rangle_{T_s}, \langle v_2(t) \rangle_{T_s}, d(t)) \quad (15.43)$$

Let us expand this expression in a three-dimensional Taylor series, about the quiescent operating point ( $V_1$ ,  $V_2$ ,  $D$ ):

$$\begin{aligned} I_1 + \hat{i}_1(t) &= f_1(V_1, V_2, D) + \hat{v}_1(t) \left. \frac{\partial f_1(v_1, V_2, D)}{\partial v_1} \right|_{v_1=V_1} \\ &\quad + \hat{v}_2(t) \left. \frac{\partial f_1(V_1, v_2, D)}{\partial v_2} \right|_{v_2=V_2} + \hat{d}(t) \left. \frac{\partial f_1(V_1, V_2, d)}{\partial d} \right|_{d=D} \\ &\quad + \text{higher-order nonlinear terms} \end{aligned} \quad (15.44)$$

For simplicity of notation, the angle brackets denoting average values are dropped in the above equation. The dc terms on both sides of Eq. (15.44) must be equal:

$$I_1 = f_1(V_1, V_2, D) = \frac{V_1}{R_e(D)} \quad (15.45)$$

As usual, we linearize the equation by discarding the higher-order nonlinear terms. The remaining first-order linear ac terms on both sides of Eq. (15.44) are equated:

$$\hat{i}_1(t) = \hat{v}_1(t) \frac{1}{r_1} + \hat{v}_2(t) g_1 + \hat{d}(t) j_1 \quad (15.46)$$

where

$$\frac{1}{r_1} = \left. \frac{\partial f_1(v_1, V_2, D)}{\partial v_1} \right|_{v_1=V_1} = \frac{1}{R_e(D)} \quad (15.47)$$

$$g_1 = \left. \frac{\partial f_1(V_1, v_2, D)}{\partial v_2} \right|_{v_2=V_2} = 0 \quad (15.48)$$

$$\begin{aligned} j_1 &= \left. \frac{\partial f_1(V_1, V_2, d)}{\partial d} \right|_{d=D} = -\frac{V_1}{R_e^2(D)} \left. \frac{\partial R_e(d)}{\partial d} \right|_{d=D} \\ &= \frac{2V_1}{DR_e(D)} \end{aligned} \quad (15.49)$$

Thus, the small-signal input resistance  $r_1$  is equal to the effective resistance  $R_e$ , evaluated at the quiescent operating point. This term describes how variations in  $\langle v_1(t) \rangle_{T_s}$  affect  $\langle i_1(t) \rangle_{T_s}$ , via  $R_e(D)$ . The small-signal parameter  $g_1$  is equal to zero, since the average transistor current  $\langle i_1(t) \rangle_{T_s}$  is independent of the average diode voltage  $\langle v_2(t) \rangle_{T_s}$ . The small-signal gain  $j_1$  describes how duty-cycle variations, which affect the value of  $R_e(d)$ , lead to variations in  $\langle i_1(t) \rangle_{T_s}$ .

In a similar manner,  $\langle i_2(t) \rangle_{T_s}$  from Eq. (15.21) can be expressed as

$$\langle i_2(t) \rangle_{T_s} = \frac{\langle v_1(t) \rangle_{T_s}^2}{R_e(d(t)) \langle v_2(t) \rangle_{T_s}} = f_2(\langle v_1(t) \rangle_{T_s}, \langle v_2(t) \rangle_{T_s}, d(t)) \quad (15.50)$$

Expansion of the function  $f_2(v_1, v_2, d)$  in a three-dimensional Taylor series about the quiescent operating point leads to

$$\begin{aligned}
I_2 + \hat{i}_2(t) &= f_2(V_1, V_2, D) + \hat{v}_1(t) \frac{\partial f_2(V_1, V_2, D)}{\partial v_1} \Big|_{v_1=V_1} \\
&\quad + \hat{v}_2(t) \frac{\partial f_2(V_1, V_2, D)}{\partial v_2} \Big|_{v_2=V_2} + \hat{d}(t) \frac{\partial f_2(V_1, V_2, d)}{\partial d} \Big|_{d=D} \\
&\quad + \text{higher-order nonlinear terms}
\end{aligned} \tag{15.51}$$

By equating the dc terms on both sides of Eq. (15.51), we obtain

$$I_2 = f_2(V_1, V_2, D) = \frac{V_1^2}{R_e(D)V_2} \tag{15.52}$$

The higher-order nonlinear terms are discarded, leaving the following first-order linear ac terms:

$$\hat{i}_2(t) = \hat{v}_2(t) \left( -\frac{1}{r_2} \right) + \hat{v}_1(t) g_2 + \hat{d}(t) j_2 \tag{15.53}$$

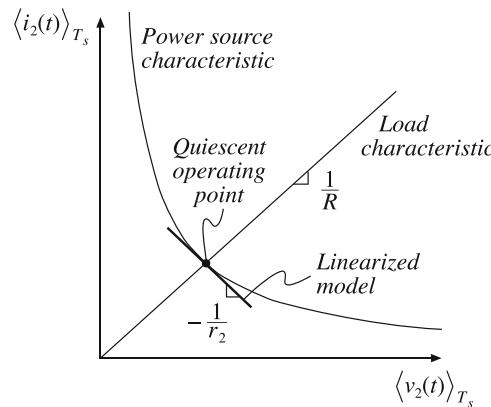
with

$$\frac{1}{r_2} = - \frac{\partial f_2(V_1, V_2, D)}{\partial v_2} \Big|_{v_2=V_2} = \frac{1}{R} = \frac{1}{M^2 R_e(D)} \tag{15.54}$$

$$g_2 = \frac{\partial f_2(V_1, V_2, D)}{\partial v_1} \Big|_{v_1=V_1} = \frac{2}{MR_e(D)} \tag{15.55}$$

$$\begin{aligned}
j_2 &= \frac{\partial f_2(V_1, V_2, d)}{\partial d} \Big|_{d=D} = - \frac{V_1^2}{R_e^2(D)V_2} \frac{\partial R_e(d)}{\partial d} \Big|_{d=D} \\
&= \frac{2V_1}{DMR_e(D)}
\end{aligned} \tag{15.56}$$

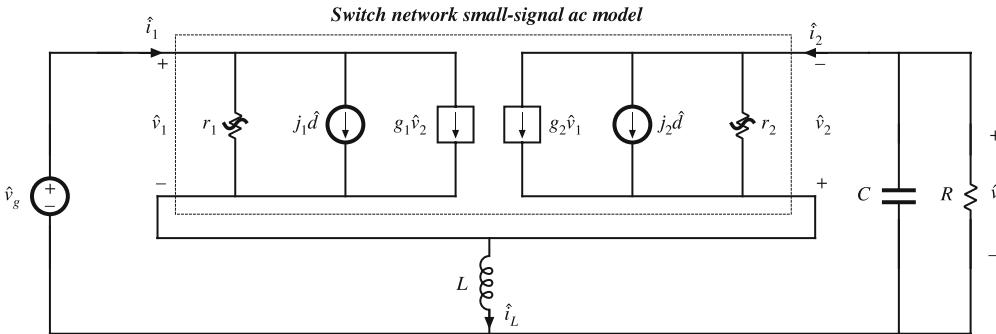
The output resistance  $r_2$  describes how variations in  $\langle v_2(t) \rangle_{T_s}$  influence  $\langle i_2(t) \rangle_{T_s}$ . As illustrated in Fig. 15.18,  $r_2$  is determined by the slope of the power source characteristic, evaluated at the quiescent operating point. For a linear resistive load,  $r_2 = R$ . For any type of load, it is true



**Fig. 15.18** The small-signal output resistance  $r_2$  is determined by the slope of the power source characteristic at the quiescent operating point

**Table 15.2** Small-signal DCM switch model parameters

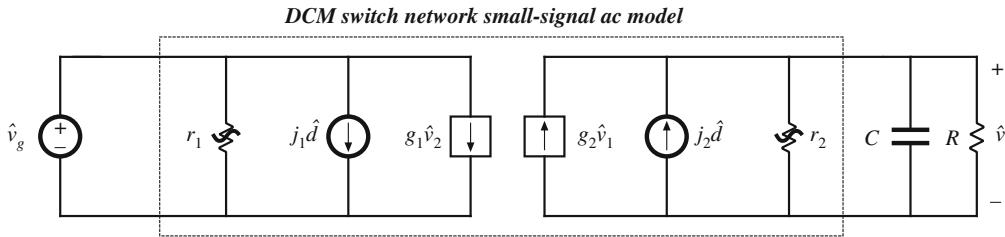
Switch network	$g_1$	$j_1$	$r_1$	$g_2$	$j_2$	$r_2$
General two-switch, Fig. 15.11a	0	$\frac{2V_1}{DR_e}$	$R_e$	$\frac{2}{MR_e}$	$\frac{2V_1}{DMR_e}$	$M^2 R_e$
Buck, Fig. 15.21a	$-\frac{1}{R_e}$	$\frac{2(1-M)V_1}{DR_e}$	$R_e$	$\frac{2-M}{MR_e}$	$\frac{2(1-M)V_1}{DMR_e}$	$M^2 R_e$
Boost, Fig. 15.21b	$-\frac{1}{(M-1)^2 R_e}$	$\frac{2MV_1}{D(M-1)R_e}$	$\frac{(M-1)^2}{M^2} R_e$	$\frac{2M-1}{(M-1)^2 R_e}$	$\frac{2V_1}{D(M-1)R_e}$	$(M-1)^2 R_e$

**Fig. 15.19** Small-signal ac model of the DCM buck-boost converter obtained by insertion of the switch network two-port small-signal model into the original converter circuit

that  $r_2 = M^2 R_e(D)$ . The parameters  $j_2$  and  $g_2$  describe how variations in the duty cycle  $d(t)$  and in the average transistor voltage  $\langle v_1(t) \rangle_{T_s}$  (which influence the average power  $\langle p(t) \rangle_{T_s}$ ) lead to variations in the average diode current  $\langle i_2(t) \rangle_{T_s}$ . Values of the small-signal parameters in the DCM switch model of Fig. 15.17b are summarized in the top row of Table 15.2.

A small-signal model of the DCM buck-boost converter is obtained by replacing the transistor and diode of the converter with the switch model of Fig. 15.17b. The result is illustrated in Fig. 15.19. This equivalent circuit can now be solved using conventional linear circuit analysis techniques, to determine the transfer functions and other small-signal quantities of interest.

The small-signal equivalent circuit models of Fig. 15.19 contain two dynamic elements: capacitor  $C$  and inductor  $L$ . Control-to-output transfer functions obtained by solving this equivalent circuit model have two poles. It has been shown [71, 74, 126, 130, 131] that one of the poles, due to the capacitor  $C$ , appears at a low frequency, while the other pole (and a RHP zero) due to the inductor  $L$ , occurs at much higher frequency, close to or above the converter switching frequency. The small-signal equivalent circuit models have been derived from the large-signal averaged switch network equations (15.20) and (15.21). These equations are based on the approximation in Eq. (15.5), which states that the average inductor voltage, and therefore its small-signal ac voltage, is zero. This contradicts predictions of the resulting small-signal model in Fig. 15.19. As a result, we expect that the models derived in this section can be used to predict low-frequency dynamics, while predictions of the high-frequency dynamics due to the



**Fig. 15.20** Low-frequency ac model obtained by neglecting inductor  $L$  dynamics. The buck, boost, or buck-boost converters can be modeled, by employing the appropriate parameters from Table 15.2

inductor  $L$  are of questionable validity. The origins, analysis, and more accurate predictions of high-frequency dynamics of DCM converters are discussed in Sect. 15.5.

A simple approximate way to determine the low-frequency small-signal transfer functions is to neglect the inductor high-frequency dynamics by simply shorting  $L$  in the equivalent circuit of Fig. 15.19. The simplified, first-order model is shown in Fig. 15.20.

The small-signal switch model can be employed to model other DCM converters, by simply replacing the transistor and diode with ports 1 and 2, respectively, of the two-port model of Fig. 15.17b. An alternative approach, which yields more convenient results in the analysis of the buck and boost converters, is to define the switch network as illustrated in Figs. 15.21a,b, respectively. These switch networks can also be modeled using the two-port small-signal equivalent circuit of Fig. 15.21c; however, new expressions for the parameters  $r_1$ ,  $j_1$ ,  $g_1$ , etc., must be derived. These expressions are again found by linearizing the equations of the averaged switch network terminal currents.

Table 15.2 lists the small-signal parameters for the buck switch network of Fig. 15.21a (middle row) and for the boost switch network of Fig. 15.21b (bottom row). Insertion of the small-signal two-port model into the DCM buck and boost converters, together with shorting  $L$  to neglect the inductor high-frequency dynamics, leads to the same equivalent circuits shown in Fig. 15.20. The model parameters are given in Table 15.2.

The control-to-output transfer function  $G_{vd}(s)$  is found by letting  $\hat{v}_g = 0$  in Fig. 15.20. Solution for  $\hat{v}$  then leads to

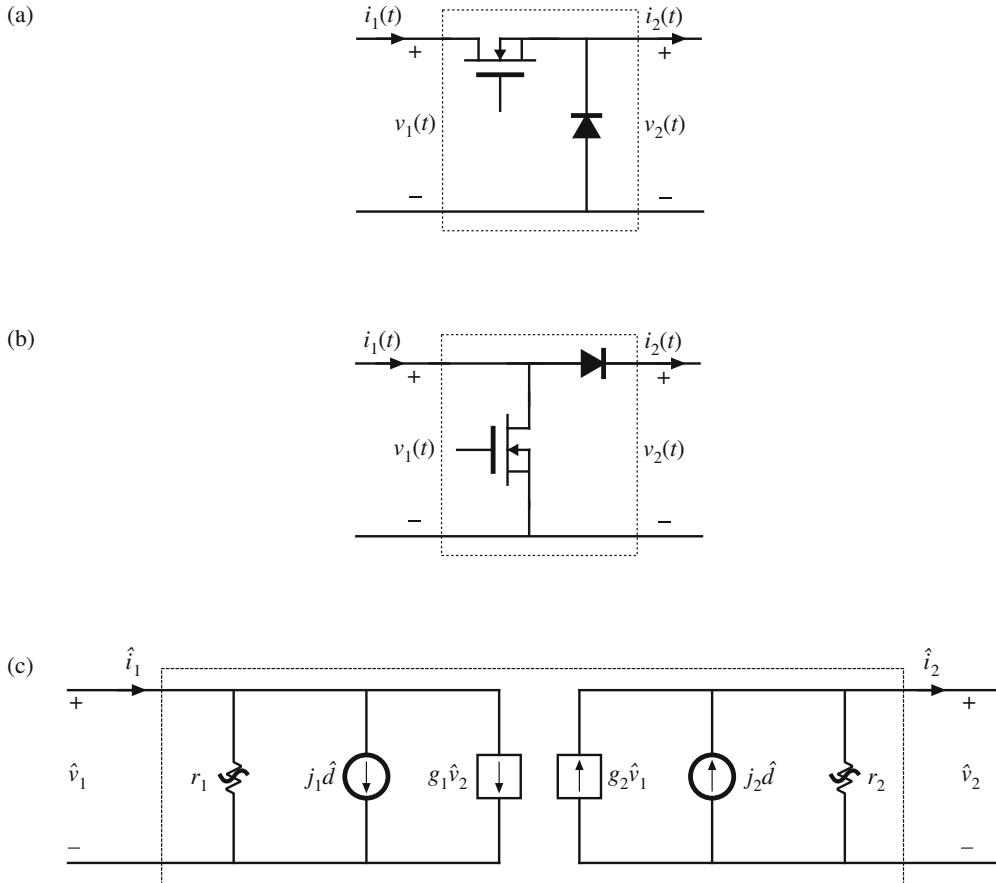
$$G_{vd}(s) = \frac{\hat{v}}{\hat{d}} \Big|_{\hat{v}_g=0} = \frac{G_{d0}}{\left(1 + \frac{s}{\omega_p}\right)} \quad (15.57)$$

with

$$\begin{aligned} G_{d0} &= j_2(R||r_2) \\ \omega_p &= \frac{1}{(R||r_2)C} \end{aligned} \quad (15.58)$$

The line-to-output transfer function  $G_{vg}(s)$  is found by letting  $\hat{d} = 0$  in Fig. 15.20. One then obtains

$$G_{vg}(s) = \frac{\hat{v}}{\hat{v}_g} \Big|_{\hat{d}=0} = \frac{G_{g0}}{\left(1 + \frac{s}{\omega_p}\right)} \quad (15.59)$$



**Fig. 15.21** A convenient way to model the switch networks of DCM buck and boost converters: (a) defined terminal quantities of the DCM buck switch network, (b) defined terminal quantities of the boost switch network, (c) two-port small-signal ac model. The model parameters are given in Table 15.2

with

$$G_{g0} = g_2(R||r_2) = M \quad (15.60)$$

Expressions for  $G_{d0}$ ,  $G_{g0}$ , and  $\omega_p$  are listed in Table 15.3, for the DCM buck, boost, and buck-boost converters with resistive loads [15, 135].

The ac modeling approach described in this section is both general and useful. The transistor and diode of a DCM converter can be simply replaced by the two-port network of Fig. 15.17b, leading to the small-signal ac model. Alternatively, the switch network can be defined as in Fig. 15.21a or b, and then modeled by the same two-port network, Fig. 15.21c. The small-signal converter model can then be solved via conventional circuit analysis techniques, to obtain the small-signal transfer functions of the converter.

**Table 15.3** Salient features of DCM converter small-signal transfer functions

Converter	$G_{d0}$	$G_{g0}$	$\omega_p$
Buck	$\frac{2V}{D} \frac{1-M}{2-M}$	$M$	$\frac{2-M}{(1-M)RC}$
Boost	$\frac{2V}{D} \frac{M-1}{2M-1}$	$M$	$\frac{2M-1}{(M-1)RC}$
Buck-boost	$\frac{V}{D}$	$M$	$\frac{2}{RC}$

### 15.3.1 Example: Control-to-Output Frequency Response of a DCM Boost Converter

As a simple numerical example, let us find the small-signal control-to-output transfer function of a DCM boost converter having the following element and parameter values:

$$\begin{aligned} R &= 12\Omega \\ L &= 5 \mu\text{H} \\ C &= 470 \mu\text{F} \\ f_s &= 100 \text{ kHz} \end{aligned} \quad (15.61)$$

The output voltage is regulated to be  $V = 36$  V. It is desired to determine  $G_{vd}(s)$  at the operating point where the load current is  $I = 3$  A and the dc input voltage is  $V_g = 24$  V.

The effective resistance  $R_e(D)$  is found by solution of the dc equivalent circuit of Fig. 15.16b. Since the load current  $I$  and the input and output voltages  $V$  and  $V_g$  are known, the power source value  $P$  is

$$P = I(V - V_g) = (3 \text{ A})(36 \text{ V} - 24 \text{ V}) = 36 \text{ W} \quad (15.62)$$

The effective resistance is therefore

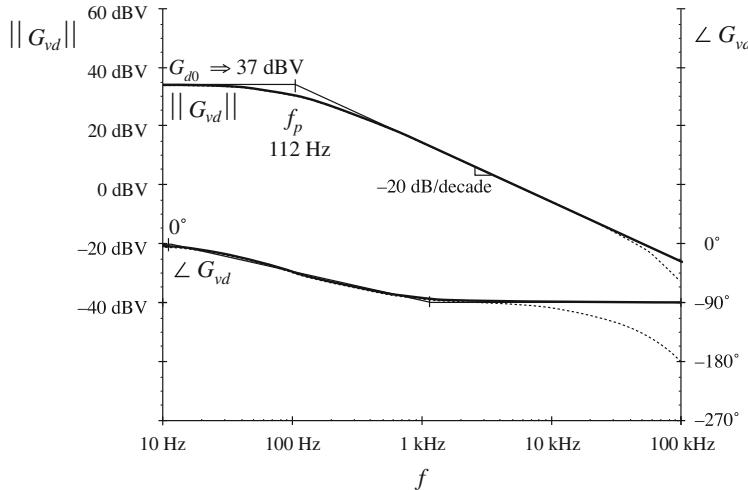
$$R_e = \frac{V_g^2}{P} = \frac{(24 \text{ V})^2}{36 \text{ W}} = 16 \Omega \quad (15.63)$$

The steady-state duty cycle  $D$  can now be found using Eq. (15.37):

$$D = \sqrt{\frac{2L}{R_e T_s}} = \sqrt{\frac{2(5 \mu\text{H})}{(16 \Omega)(10 \mu\text{s})}} = 0.25 \quad (15.64)$$

The expressions given in Table 15.3 for  $G_{d0}$  and  $\omega_p$  of the boost converter can now be evaluated:

$$\begin{aligned} G_{d0} &= \frac{2V}{D} \frac{M-1}{2M-1} = \frac{2(36 \text{ V})}{(0.25)} \frac{\left(\frac{(36 \text{ V})}{(24 \text{ V})} - 1\right)}{\left(2\frac{(36 \text{ V})}{(24 \text{ V})} - 1\right)} = 72 \text{ V} \Rightarrow 37 \text{ dBV} \\ f_p &= \frac{\omega_p}{2\pi} = \frac{2M-1}{2\pi(M-1)RC} = \frac{\left(2\frac{(36 \text{ V})}{(24 \text{ V})} - 1\right)}{2\pi\left(\frac{(36 \text{ V})}{(24 \text{ V})} - 1\right)(12 \Omega)(470 \mu\text{F})} = 112 \text{ Hz} \end{aligned} \quad (15.65)$$



**Fig. 15.22** Magnitude and phase of the control-to-output transfer function, DCM boost example. *Solid lines*: function and its asymptotes, approximate single-pole response predicted by the model of Fig. 15.20. *Dashed lines*: more accurate response that includes high-frequency inductor dynamics

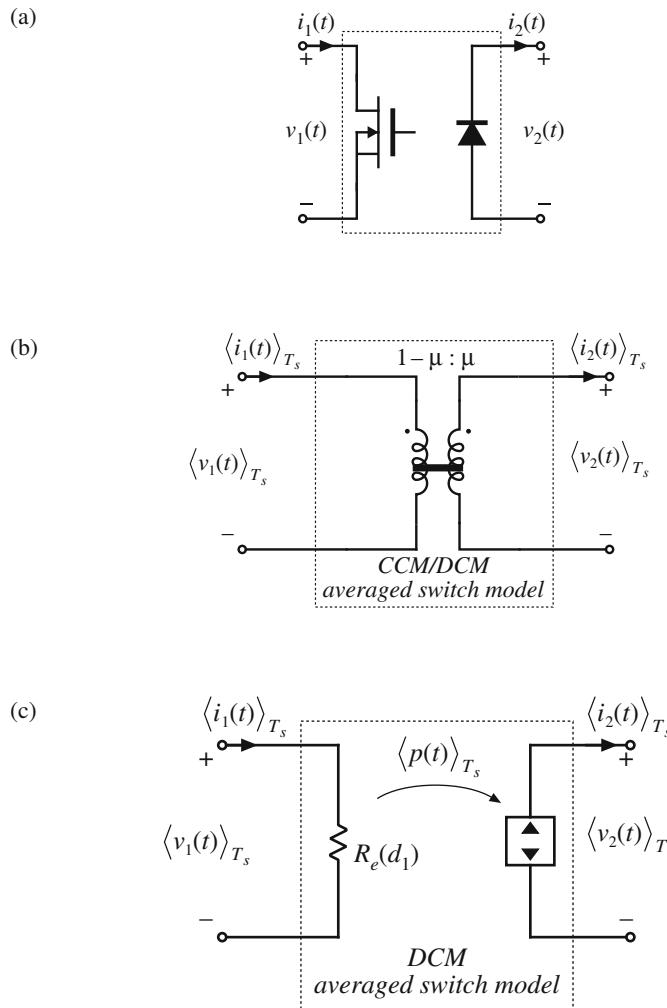
A Bode diagram of the control-to-output transfer function is constructed in Fig. 15.22. The solid lines illustrate the magnitude and phase predicted by the approximate single-pole model of Fig. 15.20. The dashed lines are the predictions of the more accurate model discussed in Sect. 15.5, which include a second pole at  $f_2 = 64$  kHz and a RHP zero at  $f_z = 127$  kHz, arising from the inductor dynamics. Since the switching frequency is 100 kHz, the accuracy of the model at these frequencies cannot be guaranteed. Nonetheless, in practice, the lagging phase asymptotes arising from the inductor dynamics can be observed beginning at  $f_2/10 = 6.4$  kHz.

## 15.4 Combined CCM/DCM Averaged Switch Simulation Model

All converters containing a diode rectifier operate in discontinuous conduction mode (DCM) if the load current is sufficiently low. In some cases, converters are purposely designed to operate in DCM. It is therefore of interest to develop averaged models suitable for simulation of converters that may operate in either CCM or DCM.

Figure 15.23 illustrates the general two-switch network, and the corresponding large-signal averaged models in CCM and DCM. The CCM averaged switch model, which is derived in Sect. 14.1, is an ideal transformer with  $d':d$  turns ratio. In DCM, the large-signal averaged switch model is a loss-free resistor, as derived in Sect. 15.2. Our objective is to construct a combined CCM/DCM averaged switch model that reduces to the model of Fig. 15.23a or to the model of Fig. 15.23c depending on the operating mode of the converter. Let us define an effective switch conversion ratio  $\mu(t)$ , so that the averaged switch model in both modes has the same form as in CCM, as shown in Fig. 15.24. If the converter operates in CCM, then the switch conversion ratio  $\mu(t)$  is equal to the switch duty cycle  $d(t)$ ,

$$\mu = d \quad (15.66)$$



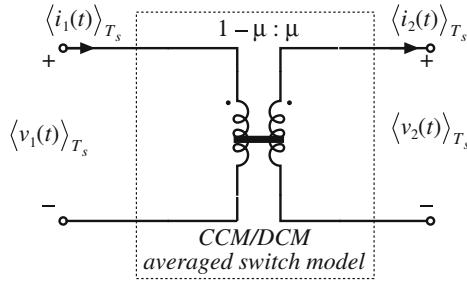
**Fig. 15.23** Summary of averaged switch modeling: (a) general two-switch network, (b) averaged switch model in CCM, and (c) averaged switch model in DCM

If the converter operates in DCM, then the effective switch conversion ratio can be computed so that the terminal characteristics of the averaged switch model of Fig. 15.24 match the terminal characteristics of the loss-free resistor model of Fig. 15.23c. Matching the port 1 characteristics gives

$$\langle v_1(t) \rangle_{T_s} = \frac{1 - \mu}{\mu} \langle v_2(t) \rangle_{T_s} = R_e \langle i_1(t) \rangle_{T_s} \quad (15.67)$$

which can be solved for the switch conversion ratio  $\mu$ ,

$$\mu = \frac{1}{1 + \frac{R_e \langle i_1(t) \rangle_{T_s}}{\langle v_2(t) \rangle_{T_s}}} \quad (15.68)$$



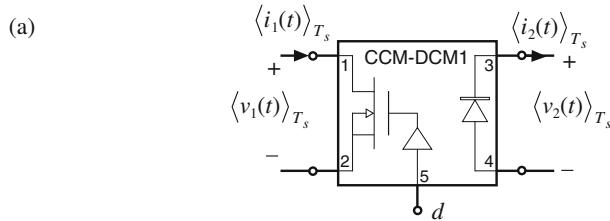
**Fig. 15.24** A general averaged switch model using the equivalent switch conversion ratio  $\mu$

It can be verified that matching the port 2 characteristics of the models in Figs. 15.23c and 15.24 gives exactly the same result for the effective switch conversion ratio in DCM.

The switch conversion ratio  $\mu(t)$  can be considered a generalization of the duty cycle  $d(t)$  of CCM switch networks. Based on this approach, models and results developed for converters in CCM can be used not only for DCM but also for other operating modes or even for other converter configurations by simply replacing the switch duty cycle  $d(t)$  with the appropriate switch conversion ratio  $\mu(t)$  [71–74]. For example, if  $M(d)$  is the conversion ratio in CCM, then  $M(\mu)$ , with  $\mu$  given by Eq. (15.68), is the conversion ratio in DCM. The switch conversion ratio in DCM depends on the averaged terminal voltage and current, as well as the switch duty cycle  $d$  through the effective resistance  $R_e = 2L/d^2T_s$ . If the converter is completely unloaded, then the average transistor current  $\langle i_1(t) \rangle_{T_s}$  is zero, and the DCM switch conversion ratio becomes  $\mu = 1$ . As a result, the dc output voltage attains the maximum possible value  $V = V_g M(1)$ . This is consistent with the results of the steady-state DCM analyses in Chap. 5 and Sect. 15.2.

To construct a combined CCM/DCM averaged switch model based on the general averaged switch model of Fig. 15.24, it is necessary to specify which of the two expressions for the switch conversion ratio to use: Eq. (15.66), which is valid in CCM, or Eq. (15.68), which is valid in DCM. At the CCM/DCM boundary, these two expressions must give the same result,  $\mu = d$ . If the load current decreases further, the converter operates in DCM, the average switch current  $\langle i_1(t) \rangle_{T_s}$  decreases, and the DCM switch conversion ratio in Eq. (15.68) becomes greater than the switch duty cycle  $d$ . We conclude that the correct value of the switch conversion ratio, which takes into account operation in CCM or DCM, is the larger of the two values computed using Eq. (15.66) and Eq. (15.68).

Figure 15.25 shows an implementation of the combined CCM/DCM model as a SPICE subcircuit CCM-DCM1. This subcircuit has the same five interface nodes as the subcircuits CCM1 and CCM2 of Sect. 14.3.1. The controlled sources  $E_t$  and  $G_d$  model the port 1 (transistor) and port 2 (diode) averaged characteristics, as shown in Fig. 15.24. The switch conversion ratio  $\mu$  is equal to the voltage  $v(u)$  at the subcircuit node  $u$ . The controlled voltage source  $E_u$  computes the switch conversion ratio as the greater of the two values obtained from Eqs. (15.66) and (15.68). The controlled current source  $G_a$ , the zero-value voltage source  $V_a$ , and the resistor  $R_a$  form an auxiliary circuit to ensure that the solution found by the simulator has the transistor and the diode currents with correct polarities,  $\langle i_1(t) \rangle_{T_s} > 0$ ,  $\langle i_2(t) \rangle_{T_s} > 0$ . The subcircuit parameters are the inductance  $L$  relevant for CCM/DCM operation, and the switching frequency  $f_s$ . The default values in the subcircuit are arbitrarily set to  $L = 100\mu\text{H}$  and  $f_s = 100\text{ kHz}$ .



(b)

```
*****
* MODEL: CCM-DCM1
* Application: two-switch PWM converters, CCM or DCM
* Limitations: ideal switches, no transformer
*****
* Parameters:
*   L = equivalent inductance for DCM
*   fs = switching frequency
*****
* Nodes:
* 1: transistor positive (drain for an n-channel MOS)
* 2: transistor negative (source for an n-channel MOS)
* 3: diode cathode
* 4: diode anode
* 5: duty cycle control input
*****
.subckt CCM-DCM1 1 2 3 4 5
+ params: L=100u fs=1E5
Et 1 2 value={(1-v(u))*v(3,4)/v(u)}
Gd 4 3 value={(1-v(u))*i(Et)/v(u)}
Ga 0 a value={MAX(i(Et),0)}
Va a b
Ra b 0 1k
Eu u 0 table {MAX(v(5),
+ v(5)*v(5)/(v(5)*v(5)+2*L*fs*i(Va)/v(3,4)))} (0 0) (1 1)
.ends
*****
```

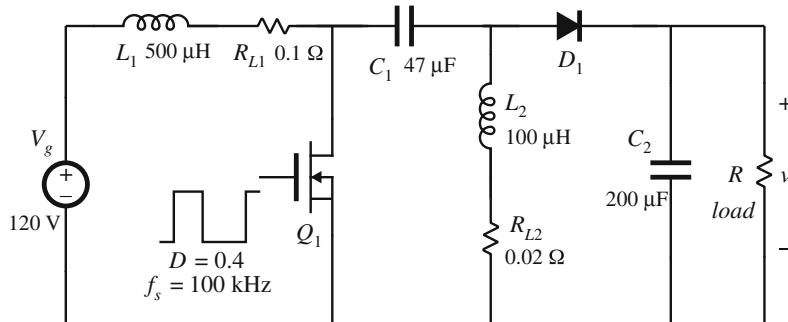
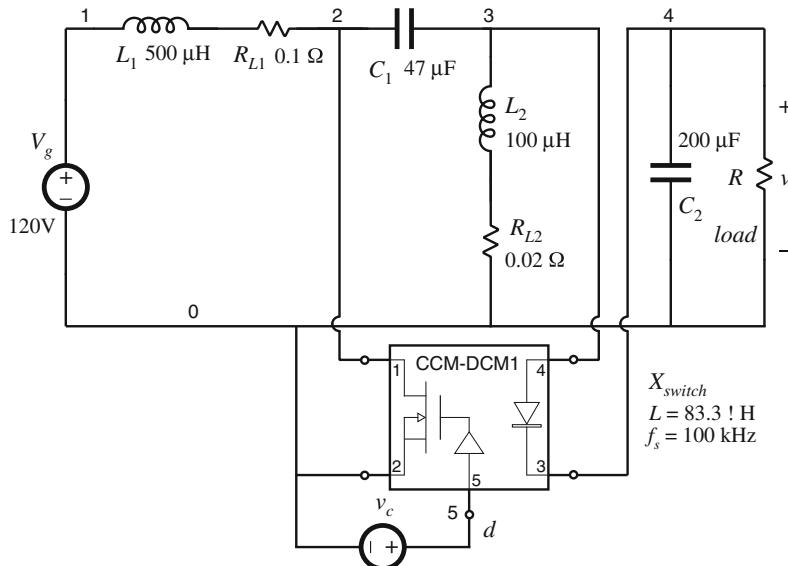
**Fig. 15.25** Implementation of the combined CCM-DCM averaged switch model: (a) schematic symbol, (b) SPICE netlist

The SPICE subcircuit CCM-DCM1 of Fig. 15.25 can be used for dc, ac, and transient simulations of PWM converters containing a transistor switch and a diode switch. This subcircuit is included in the model library *switch.lib*. It can be modified further for use in converters with isolation transformer.

#### 15.4.1 Example: CCM/DCM SEPIC Frequency Responses

As another example, consider the SEPIC of Fig. 15.26. According to Eq. (15.39), this converter operates in CCM if

$$\frac{V}{R} > \frac{1-D}{D} \frac{V_g}{R_e(D)} \quad (15.69)$$

**Fig. 15.26** SEPIC example**Fig. 15.27** SEPIC simulation example: averaged circuit model

where  $R_e(D)$  is given by Eq. (15.38). Upon neglecting losses in the converter, one finds that the CCM conversion ratio is

$$\frac{V}{V_g} \approx \frac{D}{1 - D} \quad (15.70)$$

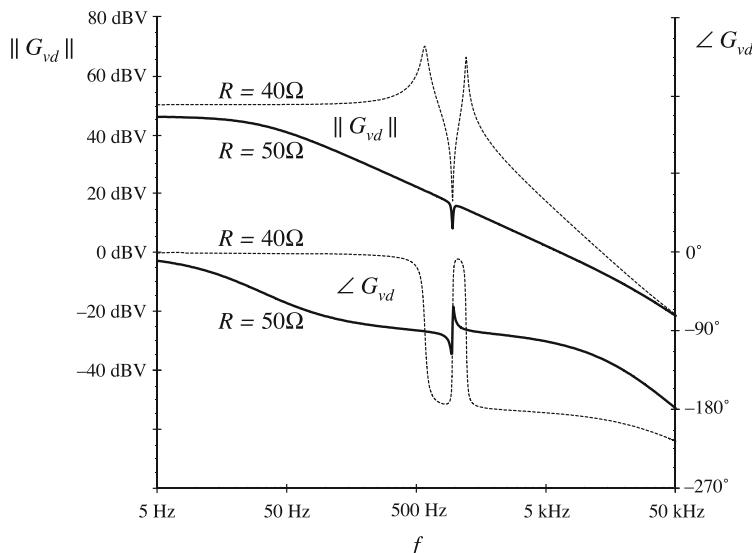
When Eqs. (15.38) and (15.70) are substituted into Eq. (15.69), the condition for operation in CCM becomes:

$$R < \frac{2(L_1 \| L_2)}{(1 - D)^2 T_s} = 46 \Omega \quad (15.71)$$

Figure 15.27 shows the averaged circuit model obtained by replacing the switch network with the CCM-DCM1 subcircuit of Fig. 15.25. A part of the circuit netlist is included in

Fig. 15.27. The connections and the parameters of the CCM-DCM1 subcircuit are defined by the  $X_{switch}$  line. In the SEPIC, the inductance parameter  $L = 83.3 \mu\text{H}$  is equal to the parallel combination of  $L_1$  and  $L_2$ . The voltage source  $v_c$  sets the quiescent value of the duty cycle to  $D = 0.4$ , and the small-signal ac value to  $\hat{d} = 1$ . Ac simulation is performed on a linearized circuit model, so that amplitudes of all small-signal ac waveforms are directly proportional to the amplitude of the ac input, regardless of the input ac amplitude value. For example, the control-to-output transfer function is  $G_{vd} = \hat{v}/\hat{d}$ , where  $\hat{v} = v(4)$  in the circuit of Fig. 15.27a. We can set the input ac amplitude to 1, so that the control-to-output transfer function  $G_{vd}$  can be measured directly as  $v(5)$ . This setup is just for convenience in finding small-signal frequency responses by simulation. For measurements of converter transfer functions in an experimental circuit (see Sect. 8.5), the actual amplitude of the small-signal ac variation  $\hat{d}$  would be set to a fraction of the quiescent duty cycle  $D$ . Parameters of the ac simulation are set by the .ac line in the netlist: the signal frequency is swept from the minimum frequency of 5 Hz to the maximum frequency of 50 kHz in 201 points per decade.

Figure 15.28 shows magnitude and phase responses of the control-to-output transfer function obtained by SPICE ac simulations for two different values of the load resistance:  $R = 40 \Omega$ , for which the converter operates in CCM, and  $R = 50 \Omega$ , for which the converter operates in DCM. For these two operating points, the quiescent (dc) voltages and currents in the circuit are nearly the same. Nevertheless, the frequency responses are qualitatively very different in the two operating modes. In CCM, the converter exhibits a fourth-order response with two pairs of high- $Q$  complex-conjugate poles and a pair of complex-conjugate zeroes. Another RHP (right half-plane) zero can be observed at frequencies approaching 50 kHz. In DCM, there is a dominant low-frequency pole followed by a pair of complex-conjugate poles and a pair of



**Fig. 15.28** Magnitude and phase responses of the control-to-output transfer function obtained by simulation of the SEPIC example, for two values of load resistance. For  $R = 50 \Omega$ , the converter operates in DCM (solid lines), and for  $R = 40 \Omega$  the converter operates in CCM (dashed lines)

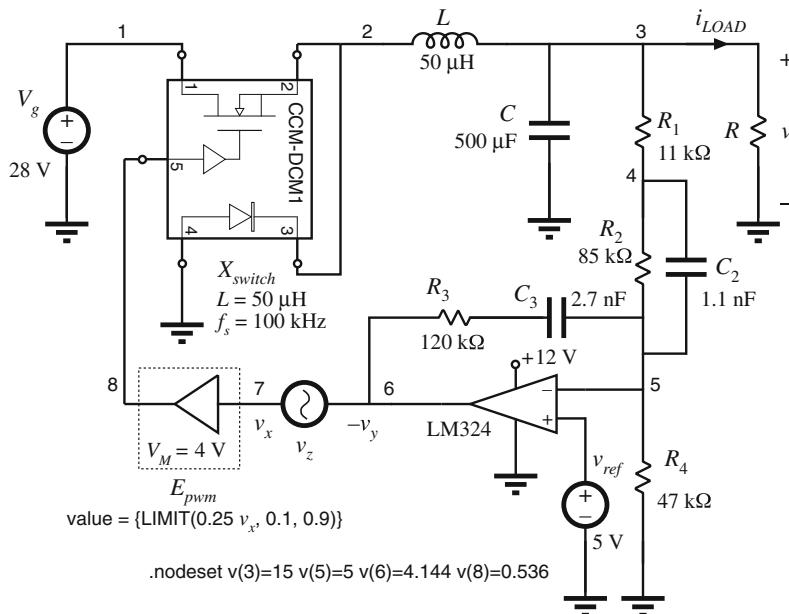
complex-conjugate zeroes. The frequencies of the complex poles and zeroes are very close in value. High-frequency dynamics contribute additional phase lag at higher frequencies.

In the design of a feedback controller around a converter that may operate in CCM or in DCM, one should take into account that the crossover frequency, the phase margin, and the closed-loop responses can be substantially different depending on the operating mode. This point is illustrated by the example of the next section.

### 15.4.2 Example: Loop Gain and Closed-Loop Responses of a Buck Voltage Regulator

A controller design for a buck converter example is discussed in Sect. 9.5.4. The converter and the block diagram of the controller are shown in Fig. 9.35. This converter system is designed to regulate the dc output voltage at  $V = 15$  V for the load current up to 5 A. Let us test this design by simulation. An averaged circuit model of a practical realization of the buck voltage regulator described in Sect. 9.5.4 is shown in Fig. 15.29. The MOSFET and the diode switch are replaced by the averaged switch model implemented as the CCM-DCM1 subcircuit. The pulse-width modulator with  $V_M = 4$  V is modeled according to the discussion in Sect. 7.3 as a dependent voltage source  $E_{pwm}$  controlled by the PWM input voltage  $v_x$ . The value of  $E_{pwm}$  is equal to  $1/V_M = 0.25$  times the PWM input voltage  $v_x$ , with a limit for the minimum value set to 0.1 V, and a limit for the maximum value set to 0.9 V. The output of the pulse-width modulator is the control duty-cycle input to the CCM-DCM1 averaged switch subcircuit. Given the specified limits for  $E_{pwm}$ , the switch duty cycle  $d(t)$  can take values in the range:

$$D_{\min} \leq d(t) \leq D_{\max} \quad (15.72)$$



**Fig. 15.29** Buck voltage regulator example

where  $D_{min} = 0.1$ , and  $D_{max} = 0.9$ . Practical PWM integrated circuits often have a limit  $D_{max} < 1$  for the maximum possible duty cycle. The voltage sensor and the compensator are implemented around an op amp LM324. With very large loop gain in the system, the steady-state error voltage is approximately zero, i.e., the dc voltages at the plus and the minus inputs of the op amp are almost the same,

$$v(5) = v_{ref} \quad (15.73)$$

As a result, the quiescent (dc) output voltage  $V$  is set by the reference voltage  $v_{ref}$  and the voltage divider comprised of  $R_1$ ,  $R_2$ ,  $R_4$ :

$$V \frac{R_4}{R_1 + R_2 + R_4} = v_{ref} = 5 \text{ V} \quad (15.74)$$

By setting the ac reference voltage  $\hat{v}_{ref}$  to zero, one can find the combined transfer function of the voltage sensor and the compensator as:

$$H(s)G_c(s) = \frac{\hat{v}_y}{\hat{v}} = \frac{R_3 + \frac{1}{sC_3}}{R_1 + R_2 \parallel \frac{1}{sC_2}} \quad (15.75)$$

This transfer function can be written in factored pole-zero form as

$$G_{cm}H \frac{\left(1 + \frac{s}{\omega_z}\right)\left(1 + \frac{\omega_L}{s}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \quad (15.76)$$

where

$$G_{cm}H = \frac{R_3}{R_1 + R_2} \quad (15.77)$$

$$f_z = \frac{\omega_z}{2\pi} = \frac{1}{2\pi R_2 C_2} \quad (15.78)$$

$$f_L = \frac{\omega_L}{2\pi} = \frac{1}{2\pi R_3 C_3} \quad (15.79)$$

$$f_p = \frac{\omega_p}{2\pi} = \frac{1}{2\pi (R_1 \parallel R_2) C_2} \quad (15.80)$$

The design described in Sect. 9.5.4 resulted in the following values for the gain and the corner frequencies:

$$G_{cm}H = 3.7(1/3) = 1.23, f_z = 1.7 \text{ kHz}, f_L = 500 \text{ Hz}, f_p = 14.5 \text{ kHz} \quad (15.81)$$

Eqs. (15.74) and (15.77) to (15.81) can be used to select the circuit parameter values. Let us (somewhat arbitrarily) choose  $C_2 = 1.1 \text{ nF}$ . Then, from Eq. (15.78), we have  $R_2 = 85 \text{ k}\Omega$ , and Eq. (15.80) yields  $R_1 = 11 \text{ k}\Omega$ . From Eq. (15.77) we obtain  $R_3 = 120 \text{ k}\Omega$ , and Eq. (15.79) gives  $C_3 = 2.7 \text{ k}\Omega$ . Finally,  $R_4 = 47 \text{ k}\Omega$  is found from Eq. (15.74). The voltage regulator design can now be tested by simulations of the circuit in Fig. 15.29.

Loop gains can be obtained by simulation using exactly the same techniques described in Sect. 9.6 for experimental measurement of loop gains [137]. Let us apply the voltage injection technique of Sect. 9.6.1. An ac voltage source  $v_z$  is injected between the compensator output and the PWM input. This is a good injection point since the output impedance of the compensator built around the op amp is small, and the PWM input impedance is very large (infinity in the circuit model of Fig. 15.29). With the ac source amplitude set (arbitrarily) to 1, and no other ac sources in the circuit, ac simulations are performed to find the loop gain as

$$T(s) = \frac{\hat{v}_y}{\hat{v}_x} = -\frac{v(6)}{v(7)} \quad (15.82)$$

To perform ac analysis, the simulator first solves for the quiescent (dc) operating point. The circuit is then linearized at this operating point, and small-signal frequency responses are computed for the specified range of signal frequencies. Solving for the quiescent operating point involves numerical solution of a system of nonlinear equations. In some cases, the numerical solution does not converge and the simulation is aborted with an error message. In particular, convergence problems often occur in circuits with feedback, especially when the loop gain at dc is very large. This is the case in the circuit of Fig. 15.29. To help convergence when the simulator is solving for the quiescent operating point, one can specify approximate or expected values of node voltages using the .nodeset line as shown in Fig. 15.29. In this case, we know by design that the quiescent output voltage is close to 15 V ( $v(3) = 15$ ), that the negative input of the op amp is very close to the reference ( $v(5) = 5$ ), and that the quiescent duty cycle is approximately  $D = V/V_g = 0.536$ , so that  $v(8) = 0.536$  V. Given these approximate node voltages, the numerical solution converges, and the following quiescent operating points are found by the simulator for two values of the load resistance  $R$ :

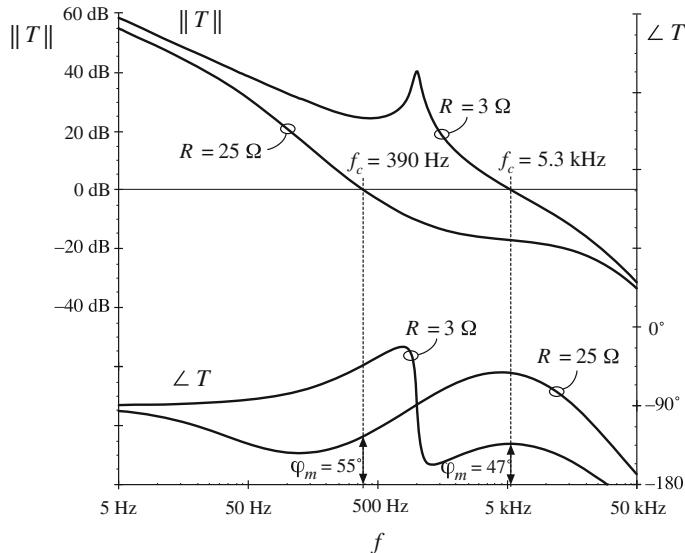
$$R = 3 \Omega, v(3) = 15.2 \text{ V}, v(5) = 5.0 \text{ V}, v(7) = 2.173 \text{ V}, v(8) = 0.543 \text{ V}, D = 0.543 \quad (15.83)$$

$$R = 25 \Omega, v(3) = 15.2 \text{ V}, v(5) = 5.0 \text{ V}, v(7) = 2.033 \text{ V}, v(8) = 0.508 \text{ V}, D = 0.508 \quad (15.84)$$

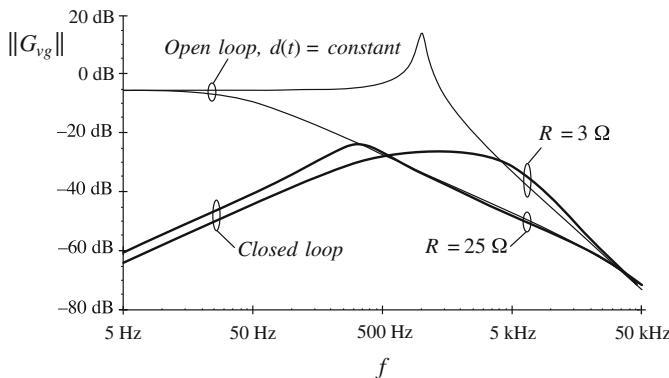
For the nominal load resistance  $R = 3 \Omega$ , the converter operates in CCM, so that  $D = V/V_g$ . For  $R = 25 \Omega$ , the same dc output voltage is obtained for a lower value of the quiescent duty cycle, which means that the converter operates in DCM.

The magnitude and phase responses of the loop gain found for the operating points given by Eqs. (15.83) and (15.84) are shown in Fig. 15.30. For  $R = 3 \Omega$ , the crossover frequency is  $f_c = 5.3$  kHz, and the phase margin is  $\phi_M = 47^\circ$ , very close to the values ( $f_c = 5$  kHz,  $\phi_M = 52^\circ$ ) that we designed for in Sect. 9.5.4. At light load, for  $R = 25 \Omega$ , the loop gain responses are considerably different because the converter operates in DCM. The crossover frequency drops to  $f_c = 390$  Hz, while the phase margin is  $\phi_M = 55^\circ$ .

The magnitude responses of the line-to-output transfer function are shown in Fig. 15.31, again for two values of the load resistance,  $R = 3 \Omega$  and  $R = 25 \Omega$ . The open-loop responses are obtained by braking the feedback loop at node 8, and setting the dc voltage at this node to the quiescent value  $D$  of the duty cycle. For  $R = 3 \Omega$ , the open-loop and closed-loop responses can be compared to the theoretical plots shown in Fig. 9.45. At 100 Hz, the closed-loop magnitude response is  $0.012 \Rightarrow -38$  dB. A 1 V, 100 Hz variation in  $v_g(t)$  would induce a 12 mV variation in the output voltage  $v(t)$ . For  $R = 25 \Omega$ , the closed-loop magnitude response is  $0.02 \Rightarrow -34$  dB,



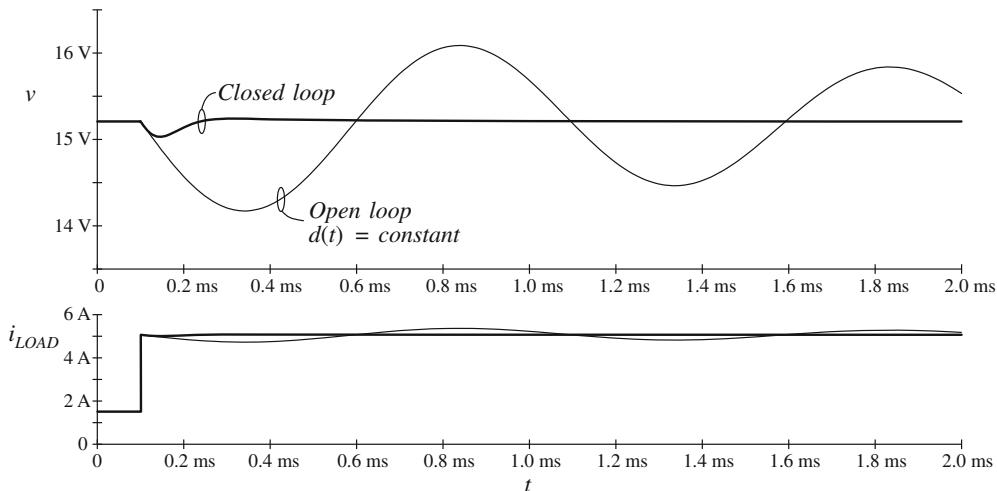
**Fig. 15.30** Loop gain in the buck voltage regulator example



**Fig. 15.31** Line-to-output response of the buck voltage regulator example

which means that the 1 V, 100 Hz variation in  $v_g(t)$  would induce a 20 mV variation in the output voltage. Notice how the regulator performance in terms of rejecting the input voltage disturbance is significantly worse at light load than at the nominal load.

A test of the transient response to a step change in load is shown in Fig. 15.32. The load current is initially equal to 1.5 A, and increases to  $i_{LOAD} = 5$  A at  $t = 0.1$  ms. When the converter is operated in open-loop at constant duty cycle, the response is governed by the natural time constants of the converter network. A large undershoot and long lightly damped oscillations can be observed in the output voltage. With the feedback loop closed, the controller dynamically adjusts the duty cycle  $d(t)$  trying to maintain the output voltage constant. The output voltage drops by about 0.2 V, and it returns to the regulated value after a short, well-damped transient.



**Fig. 15.32** Load transient response of the buck voltage regulator example

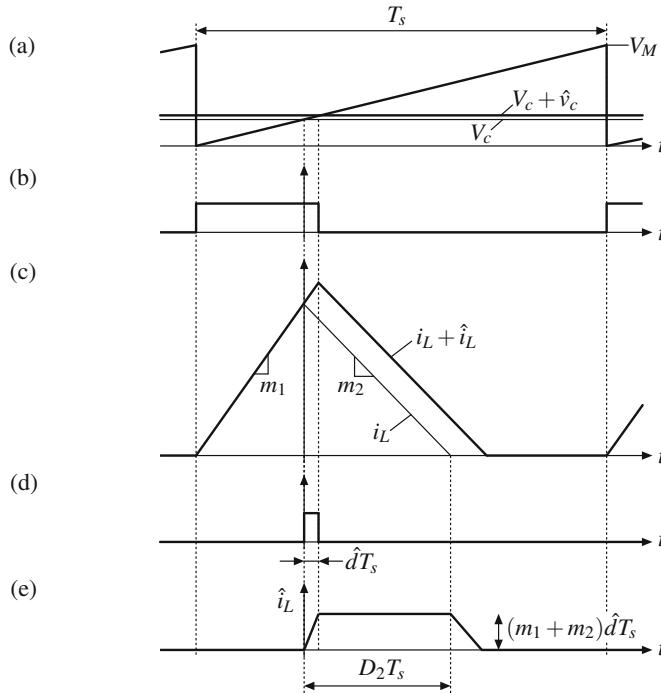
The voltage regulator example of Fig. 15.29 illustrates how the performance can vary significantly if the regulator is expected to supply a wide range of loads. In practice, further tests would also be performed to account for expected ranges of input voltages, and variations in component parameter values. Design iterations may be necessary to ensure that performance specifications are met under worst-case conditions.

## 15.5 High-Frequency Dynamics of Converters in DCM

As discussed in Sect. 15.3, transfer functions of converters operating in discontinuous conduction mode exhibit a dominant low-frequency pole. To correctly model the high-frequency dynamics of DCM converters, the approximation given by Eq. (15.5) must be removed, *i.e.*, one must account for the fact that the ac voltage across the inductor is not zero [130]. In this section, we show that the high-frequency dynamics of DCM converters are related to the sampling process associated with the pulse-width modulator and the nature of the response of the inductor current to duty-cycle perturbations [136].

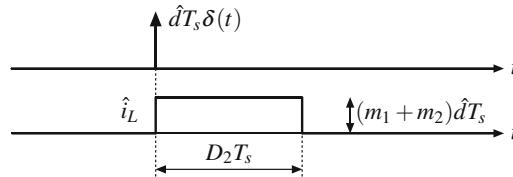
Figure 15.33 shows details of steady-state and small-signal perturbed waveforms in a DCM converter. During the switching period shown, the inductor current ramps up from zero with a slope  $m_1$ , and then ramps down to zero with a slope  $m_2$ . It is assumed that converter voltages do not change appreciably so that the slopes  $m_1$  and  $m_2$  can be considered constant.

The PWM input signal  $v_c(t)$  has a steady-state dc component  $V_c$  and a small-signal ac perturbation  $\hat{v}_c$ . During the switching period shown in Fig. 15.33, the transistor switch gate-drive waveform is extended by  $\hat{d}T_s$ , where  $\hat{d} = \hat{v}_c/V_M$  and  $V_M$  is the amplitude of the PWM ramp. Figure 15.33d shows that the perturbation in the transistor gate-drive waveform is a pulse of length  $\hat{d}T_s$ , which occurs at the modulated edge of the gate-drive waveform. As a result, a perturbation in the inductor current waveform is observed. It is important to note that the converter waveforms are unaffected by the ac perturbation  $\hat{v}_c$  until the modulated (trailing) edge of the



**Fig. 15.33** Steady-state and small-signal perturbed waveforms in a DCM converter

gate-drive signal. As shown in Fig. 15.33e, the inductor current ac perturbation is a trapezoidal pulse starting at the modulated edge of the gate-drive signal and extending over a time interval approximately equal to  $D_2 T_s$ .



**Fig. 15.34** Impulse response of the small-signal perturbed inductor current waveforms in a DCM converter

In the small-signal limit,  $\hat{d}T_s$  is very short, and the transitions in  $\hat{i}_L$  can be neglected. Hence, as illustrated in Fig. 15.34, the response from the perturbation in the gate-drive waveform to the inductor current perturbation can be viewed as a response from an impulse  $\hat{d}T_s\delta(t)$  to a pulse of amplitude  $(m_1 + m_2)\hat{d}T_s$  and length  $D_2 T_s$ . It should be noted that the unit impulse  $\delta(t)$  occurs at the modulated edge of the gate-drive waveform. The impulse represents the small-signal sampling process that occurs at the modulated edge in the pulse-width modulator.

We are now in a position to explain the nature of the high-frequency dynamics of DCM converters in frequency domain. Let us derive a control-to-inductor current transfer function  $G_{ic}(s) = \hat{i}_L/\hat{v}_c$  based on the time-domain waveforms shown in Figs. 15.33 and 15.34. In the derivations, a sampled variable  $x$  is denoted by a star,  $x^*$ .

In general, given a small-signal perturbation  $\hat{v}_c(t)$ , the corresponding duty-cycle perturbation is a sampled variable

$$\hat{d}^*(t) = \frac{\hat{v}_c(t)}{V_M} \sum_{k \rightarrow -\infty}^{k \rightarrow +\infty} \delta(t - kT_s) \quad (15.85)$$

The Laplace transform of Eq. (15.85) yields

$$\hat{d}^*(s) = \frac{1}{V_M} \frac{1}{T_s} \sum_{k \rightarrow -\infty}^{k \rightarrow +\infty} \hat{v}_c(s - jk\omega_s) \quad (15.86)$$

where  $\omega_s = 2\pi f_s$ . In time domain, the impulse response of the inductor current perturbation is shown in Fig. 15.34,

$$\hat{i}_L = (m_1 + m_2)\hat{dT}_s(h(t) - h(t - D_2 T_s)) \quad (15.87)$$

where  $h(t)$  is the unit step function. The small-signal inductor current response resembles the response of a sample-and-hold to an impulse, i.e., a translation from a sampled variable to a continuous-time variable. Given the sampled nature of the duty-cycle perturbation, and the continuous-time nature of the converter states, it is appropriate to refer to the response in Eq. (15.87) as an *equivalent hold* [77].

The Laplace transform of the impulse response in Eq. (15.87) can be used to find the transfer function of the equivalent hold for the inductor current perturbation:

$$\mathcal{L}(\hat{i}_L(t)) = (m_1 + m_2)\hat{dT}_s \frac{1 - e^{-sD_2 T_s}}{s} \quad (15.88)$$

From (15.86) and (15.88), it follows that

$$\hat{i}_L^*(s) = \frac{(m_1 + m_2)T_s}{V_M} \frac{1 - e^{-sD_2 T_s}}{s} \frac{1}{T_s} \sum_{k \rightarrow -\infty}^{k \rightarrow +\infty} \hat{v}_c(s - jk\omega_s) \quad (15.89)$$

Given the sampled-data nature of a pulse-width modulated converter, it is not surprising that the inductor current spectrum consists of an infinite sum of responses to the images of  $\hat{v}_c(s)$ . Since we are interested only in the converter responses at frequencies well below the switching frequency, a control-to-inductor current "transfer function" can be obtained by retaining only the low-frequency ( $k = 0$ ) portion of the spectrum of  $\hat{i}_L(s)$ ,

$$G_{ic}(s) = \frac{\hat{i}_L}{\hat{v}_c} = \frac{(m_1 + m_2)}{V_M} \frac{1 - e^{-sD_2 T_s}}{s} \quad (15.90)$$

Note that the transfer function (15.90) is not a standard rational function of  $s$ . Instead, the transfer function contains an  $e^{-sDT_s}$  term, which is a result of the sampling process and the equivalent hold response illustrated in Fig. 15.34. From Eq. (15.90), an approximate rational transfer function can be obtained using an approximation known as the Padé approximation [138]. The first-order Padé approximation is given by:

$$e^{-sD_2T_s} \approx \frac{1 - \frac{s}{\omega_2}}{1 + \frac{s}{\omega_2}}, \quad (15.91)$$

where

$$f_2 = \frac{\omega_2}{2\pi} = \frac{1}{\pi D_2 T_s} = \frac{1}{D_2} \frac{f_s}{\pi}. \quad (15.92)$$

Applying (15.91) to (15.90) yields an approximate control-to-inductor current transfer function, including high-frequency dynamics,

$$G_{ic}(s) \approx \frac{(m_1 + m_2)D_2 T_s}{V_M} \frac{1}{1 + \frac{s}{\omega_2}} \quad (15.93)$$

where the pole frequency is given by Eq. (15.92). This expression for the high-frequency pole is general, valid for all basic converters operating in DCM. Since  $0 < D_2 < 1$ , Eq. (15.92) implies that the high-frequency pole is always greater than approximately one third of the switching frequency. Taking the steady-state solution for  $D_2$  into account, the pole frequency can be found in terms of the conversion ratio  $M$  and the duty cycle  $D$ . For the basic converters, the results are summarized in Table 15.4. Although the derivation in this section has been focused on  $G_{ic}(s)$  only, the same high-frequency pole can be found in all other DCM converter transfer functions.

**Table 15.4** High-frequency pole in DCM converter control-to-output transfer functions

Converter	High-frequency pole $f_2$
Buck	$\frac{M}{D(1-M)} \frac{f_s}{\pi}$
Boost	$\frac{M-1}{D} \frac{f_s}{\pi}$
Buck-boost	$\frac{ M }{D} \frac{f_s}{\pi}$

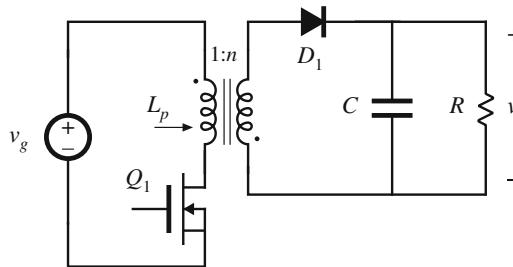
It is important to reiterate that the high-frequency pole in frequency responses is an approximation to the responses represented by the converter time-domain dynamics illustrated in Fig. 15.34. In response to a duty-cycle perturbation, the inductor current perturbation is a pulse of length  $D_2 T_s$ . The longer the equivalent hold pulse, the longer time delay is between the duty-cycle perturbation and the perturbations in converter waveforms. In frequency domain, this corresponds to additional phase lag due to a lower frequency  $f_2$  in the converter control-to-output responses. Since the equivalent hold extends over a fraction of a switching period, the resulting pole  $f_2$  is very high, and the additional phase lag can usually be ignored in practice. The behavior discussed in Sect. 8.2.3, leading to the right half-plane zero in frequency responses of boost or buck-boost CCM converters, is present in DCM converters as well. An increase in duty cycle, for example, results in the output voltage temporarily moving in the opposite direction. However, in DCM converters this opposite-direction transient is also limited to a fraction of a switching period and has essentially no impact on the design or stability of control loops around DCM converters.

## 15.6 Summary of Key Points

1. In the discontinuous conduction mode, the average transistor voltage and current are proportional, and hence obey Ohm's law. An averaged equivalent circuit can be obtained by replacing the transistor with an effective resistor  $R_e(d)$ . The average diode voltage and current obey a power source characteristic, with power equal to the power effectively dissipated by  $R_e$ . In the averaged equivalent circuit, the diode is replaced with a dependent power source.
2. The two-port lossless network consisting of an effective resistor and power source, which results from averaging the transistor and diode waveforms of DCM converters, is called a loss-free resistor. This network models the basic power-processing functions of DCM converters, much in the same way that the ideal dc transformer models the basic functions of CCM converters.
3. The large-signal averaged model can be solved under equilibrium conditions to determine the quiescent values of the converter currents and voltages. Average power arguments can often be used.
4. A small-signal ac model for the DCM switch network can be derived by perturbing and linearizing the loss-free resistor network. The result has the form of a two-port  $y$ -parameter model. The model describes the small-signal variations in the transistor and diode currents, as functions of variations in the duty cycle and in the transistor and diode ac voltage variations.
5. To simplify the ac analysis of the DCM buck and boost converters, it is convenient to define two other forms of the small-signal switch model, corresponding to the switch networks of Figs. 15.21a and 15.21b. These models are also  $y$ -parameter two-port models, but have different parameter values.
6. The inductor dynamics of the DCM buck, boost, and buck-boost converters occur at high frequency, above or just below the switching frequency. Hence, in most cases the high-frequency inductor dynamics can be ignored. In the small-signal ac model, the inductance  $L$  is set to zero, and the remaining model is solved relatively easily for the low-frequency converter dynamics. The DCM buck, boost, and buck-boost converters exhibit transfer functions containing essentially a single low-frequency dominant pole.
7. The high-frequency dynamics of DCM converters are related to the sampling process associated with the pulse-width modulator and the nature of the response of the inductor current to duty-cycle perturbations.

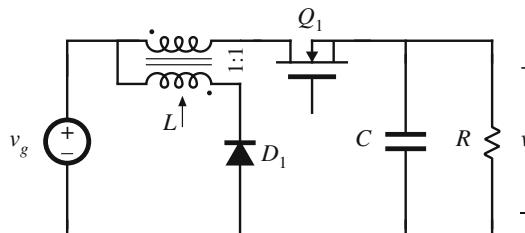
## PROBLEMS

- 15.1** Averaged switch modeling of a flyback converter. The converter of Fig. 15.35 operates in the discontinuous conduction mode. The two-winding inductor has a  $1:n$  turns ratio and negligible leakage inductance, and can be modeled as an ideal transformer in parallel with primary-side magnetizing inductance  $L_p$ .
- (a) Sketch the transistor and diode voltage and current waveforms, and derive expressions for their average values.
  - (b) Sketch an averaged model for the converter that includes a loss-free resistor network, and give an expression for  $R_e(d)$ .

**Fig. 15.35** Flyback converter, Problem 15.1

- (c) Solve your model to determine the voltage ratio  $V/V_g$  in the discontinuous conduction mode.
- (d) Over what range of load current  $I$  is your answer of part (c) valid? Express the DCM boundary in the form  $I < I_{crit}(D, R_e, V_g, n)$ .
- (e) Derive an expression for the small-signal control-to-output transfer function  $G_{vd}(s)$ . You may neglect inductor dynamics.

**15.2** Averaged switch modeling of a nonisolated Watkins–Johnson converter. The converter of Fig. 15.36 operates in the discontinuous conduction mode. The two-winding inductor has a 1:1 turns ratio and negligible leakage inductance, and can be modeled as an ideal transformer in parallel with magnetizing inductance  $L$ .

**Fig. 15.36** Watkins–Johnson converter, Problem 15.2

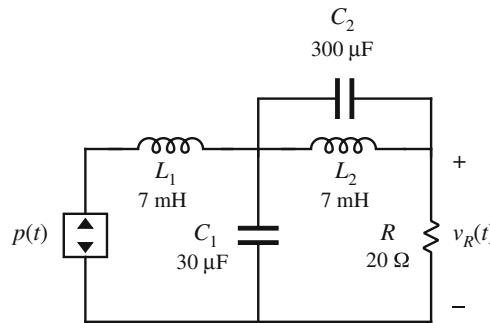
- (a) Sketch the transistor and diode voltage and current waveforms, and derive expressions for their average values.
- (b) Sketch an averaged model for the converter that includes a loss-free resistor network, and give an expression for  $R_e(d)$ .
- (c) Solve your model to determine the converter conversion ratio  $M(D) = V/V_g$  in the discontinuous conduction mode. Over what range of load currents is your expression valid?

**15.3** Sketch the steady-state output characteristics of the buck–boost converter: plot the output voltage  $V$  vs. the load current  $I$ , for several values of duty cycle  $D$ . Include both CCM and DCM operation, and clearly label the boundary between modes.

- 15.4** In the network of Fig. 15.37, the power source waveform  $p(t)$  is given by

$$p(t) = 1000 \cos^2 377t$$

The circuit operates in steady state. Determine the rms resistor voltage  $V_{R,rms}$ .



**Fig. 15.37** Network with a power source, Problem 15.4

- 15.5** Verify the expressions for  $G_{d0}$  and  $\omega_p$  given in Table 15.3.

- 15.6** A certain buck converter operates with an input voltage of  $V_g = 28$  V and an output voltage of  $V = 15$  V. The load resistance is  $R = 10\Omega$ . Other element and parameter values are  $L = 8\mu\text{H}$ ,  $C = 220\mu\text{F}$ ,  $f_s = 150\text{kHz}$ .

- (a) Determine the value of  $R_e$ .
- (b) Determine the quiescent duty cycle  $D$ .
- (c) Sketch a Bode plot of the control-to-output transfer function  $G_{vd}(s)$ . Label the values of all salient features. You may neglect inductor dynamics.

- 15.7** Using the approach of Sect. 15.5, determine the control-to-output transfer function  $G_{vd}(s)$  of a boost converter. Do not make the approximation  $L \approx 0$ .

- (a) Derive analytical expressions for the dc gain  $G_{d0}$  and the RHP zero frequency  $\omega_z$ , as functions of  $M$ ,  $R_e$ ,  $D$ ,  $V_g$ ,  $L$ ,  $C$ , and  $R$ .
- (b) With the assumption that  $C$  is sufficiently large and that  $L$  is sufficiently small, the poles of  $G_{vd}(s)$  can be factored using the low- $Q$  approximation. Do so, and express the two poles as functions of  $M$ ,  $D$ ,  $L$ ,  $C$ , and  $R$ . Show that the low-frequency pole matches the expression in Table 15.3, and that the high-frequency pole is given by the expression in Table 15.4.



## Techniques of Design-Oriented Analysis: Extra Element Theorems

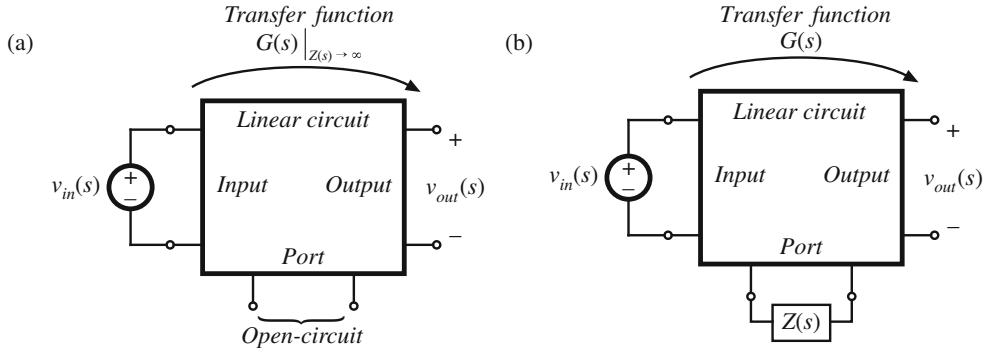
Middlebrook's *Extra Element Theorem* (EET) is a powerful technique of Design-Oriented Analysis that aids in the analysis of complex circuits and systems, with the goal of deriving tractable equations that are useful for design. As with the Feedback Theorem of Chap. 13, it is based on linear superposition and the *null double injection* analysis technique.

The *Extra Element Theorem* exposes how a known transfer function is changed by addition of a new network element. Section 16.1 contains a derivation by null double injection, and Sect. 16.2 describes several examples of its use. This theorem is the basis for the Chap. 17 analysis of converter input filters. The EET is employed in Sect. 16.2.3 to gain an understanding of how to damp the internal resonance of the SEPIC.

The *n-Extra Element Theorem* (*n-EET*) is an extension of the EET to cover the simultaneous addition of multiple elements to a circuit. A useful application of the *n-EET* is the treatment of all reactive components as extra elements: a transfer function can be written as a normalized rational fraction with little or no algebra. This powerful technique can substantially extend the engineer's ability to perform tractable paper analysis and design of complex dynamical circuits. Section 16.3 describes this technique without proof, and includes several examples.

### 16.1 Extra Element Theorem

The *Extra Element Theorem* of R. D. Middlebrook [139–141] shows how a transfer function is changed by the addition of an impedance to the network. The theorem allows one to determine the effects of this extra element on any transfer function of interest, without solving the system all over again. The Extra Element Theorem is a powerful technique of design-oriented analysis. It leads to impedance inequalities which guarantee that an element does not substantially alter a transfer function. The Extra Element Theorem is employed in Chap. 17, where it leads to a relatively simple methodology for designing input filters that do not degrade the loop gains of switching regulators. It is also employed in Sect. 22.4, to determine how the load resistance affects the properties of a resonant inverter. In this section, Middlebrook's Extra Element Theorem is derived, based on the principle of superposition. Its application is illustrated via examples.



**Fig. 16.1** How an added element changes a transfer function  $G(s)$ : (a) original conditions, before addition of new element; (b) addition of element having impedance  $Z(s)$

### 16.1.1 Basic Result

Consider the linear circuit of Fig. 16.1a. This network contains an input  $v_{in}(s)$  and an output  $v_{out}(s)$ . In addition, it contains a port whose terminals are open-circuited. It is assumed that the transfer function from  $v_{in}(s)$  to  $v_{out}(s)$  is known, and is given by

$$\frac{v_{out}(s)}{v_{in}(s)} = G(s) \Big|_{Z(s) \rightarrow \infty} \quad (16.1)$$

The Extra Element Theorem tells us how the transfer function  $G(s)$  is modified when an impedance  $Z(s)$  is connected between the terminals at the port, as in Fig. 16.1b. The result is

$$\frac{v_{out}(s)}{v_{in}(s)} = \left( G(s) \Big|_{Z(s) \rightarrow \infty} \right) \left( \frac{1 + \frac{Z_N(s)}{Z(s)}}{1 + \frac{Z_D(s)}{Z(s)}} \right) \quad (16.2)$$

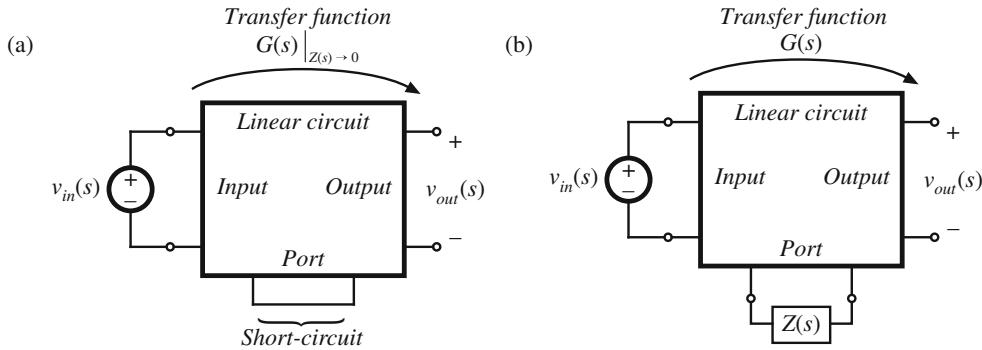
The right-hand side terms involving  $Z(s)$  account for the influence of  $Z(s)$  on  $G(s)$ , and are known as the *correction factor*.

The Extra Element Theorem also applies to the dual form illustrated in Fig. 16.2. In this form, the transfer function is initially known under the conditions that the port is short-circuited. In Fig. 16.2b, the short circuit is replaced by the impedance  $Z(s)$ . In this case, the addition of the impedance  $Z(s)$  causes the transfer function to become

$$\frac{v_{out}(s)}{v_{in}(s)} = \left( G(s) \Big|_{Z(s) \rightarrow 0} \right) \left( \frac{1 + \frac{Z(s)}{Z_N(s)}}{1 + \frac{Z(s)}{Z_D(s)}} \right) \quad (16.3)$$

The  $Z_N(s)$  and  $Z_D(s)$  terms in Eqs. (16.2) and (16.3) are identical. By equating the  $G(s)$  expressions of Eqs. (16.2) and (16.3), one can show that

$$\frac{G(s) \Big|_{Z(s) \rightarrow \infty}}{G(s) \Big|_{Z(s) \rightarrow 0}} = \frac{Z_D(s)}{Z_N(s)} \quad (16.4)$$



**Fig. 16.2** The dual form of the Extra Element Theorem, in which the extra element replaces a short circuit: (a) original conditions; (b) addition of element having impedance  $Z(s)$

This is known as the *reciprocity relationship*.

The quantities  $Z_N(s)$  and  $Z_D(s)$  can be found by measuring impedances at the port. The term  $Z_D(s)$  is the Thevenin equivalent impedance seen looking into the port, also known as the driving-point impedance. As illustrated in Fig. 16.3a, this impedance is found by setting the independent source  $v_{in}(s)$  to zero, and then measuring the impedance between the terminals of the port:

$$Z_D(s) = \frac{v(s)}{i(s)} \Big|_{v_{in}(s)=0} \quad (16.5)$$

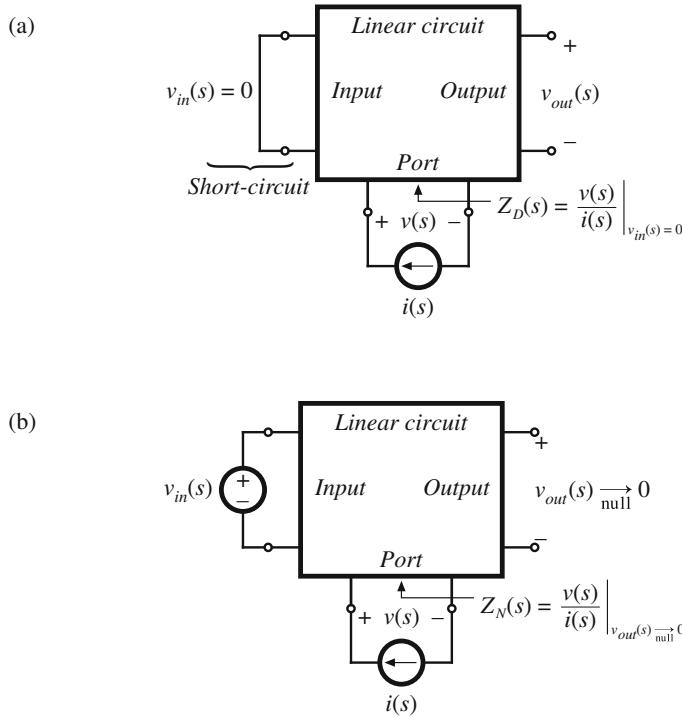
Thus,  $Z_D(s)$  is the impedance between the port terminals when the input  $v_{in}(s)$  is set to zero.

Determination of the impedance  $Z_N(s)$  is illustrated in Fig. 16.3b. The term  $Z_N(s)$  is found under the conditions that the output  $v_{out}(s)$  is *nulled* to zero. A current source  $i(s)$  is connected to the terminals of the port. In the presence of the input signal  $v_{in}(s)$ , the current  $i(s)$  is adjusted so that the output  $v_{out}(s)$  is nulled to zero. Under these conditions, the quantity  $Z_N(s)$  is given by

$$Z_N(s) = \frac{v(s)}{i(s)} \Big|_{\substack{v_{out}(s) \rightarrow 0 \\ \text{null}}} \quad (16.6)$$

Note that *nulling* the output is not the same as *shorting* the output. If one simply shorted the output, then a current would flow through the short, which would induce voltage drops and currents in other elements of the network. These voltage drops and currents are not present when the output is nulled. The null condition of Fig. 16.3b does not employ any connections to the output of the circuit. Rather, the null condition is achieved by adjustment of the independent sources  $v_{in}(s)$  and  $i(s)$  in a special way that causes the output  $v_{out}(s)$  to be zero. By superposition,  $v_{out}(s)$  can be expressed as a linear combination of  $v_{in}(s)$  and  $i(s)$ ; therefore, for a given  $v_{in}(s)$ , it is always possible to choose an  $i(s)$  that will cause  $v_{out}(s)$  to be zero. Under these null conditions,  $Z_N(s)$  is measured as the ratio of  $v(s)$  to  $i(s)$ . In practice, the circuit analysis to find  $Z_N(s)$  is simpler than analysis of  $Z_D(s)$ , because the null condition causes many of the signals within the circuit to be zero. Several examples are given in Sect. 16.2.

The input and output quantities need not be voltages, but could also be currents or other signals that can be set or nulled to zero. The next section contains a derivation of the Extra Element Theorem with a general input  $u(s)$  and output  $y(s)$ .



**Fig. 16.3** Determination of the quantities  $Z_N(s)$  and  $Z_D(s)$ : (a)  $Z_D(s)$  is the driving-point impedance at the port, and is measured with the input  $v_{in}(s)$  set to zero; (b)  $Z_N(s)$  is the impedance seen at the port under the condition that the output is nulled

### 16.1.2 Derivation

Figure 16.4a illustrates a general linear system having an input  $u(s)$  and an output  $y(s)$ . In addition, the system contains an electrical port having voltage  $v(s)$  and current  $i(s)$ , with the polarities illustrated. Initially, the port is open-circuited:  $i(s) = 0$ . The transfer function of this system, with the port open-circuited, is

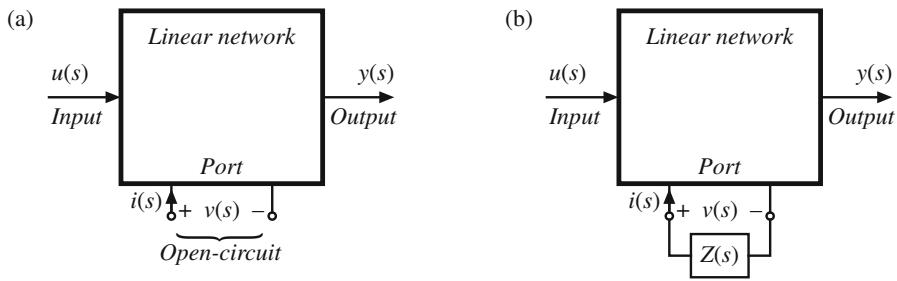
$$G_{old}(s) = \frac{y(s)}{u(s)} \Big|_{i(s)=0} \quad (16.7)$$

The objective of the Extra Element Theorem is to determine the new transfer function  $G(s)$  that is obtained when an impedance  $Z(s)$  is connected to the port:

$$G(s) = \frac{y(s)}{u(s)} \quad (16.8)$$

The situation is illustrated in Fig. 16.4b. It can be seen that the conditions at the port are now given by

$$v(s) = -i(s)Z(s) \quad (16.9)$$

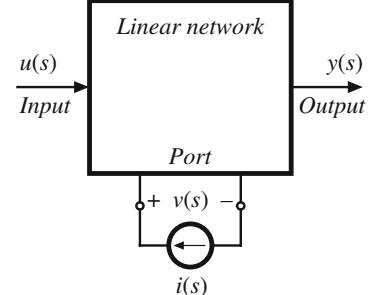


**Fig. 16.4** Modification of a linear network by addition of an extra element: (a) original system; (b) modified system, with impedance  $Z(s)$  connected at an electrical port

To express the new transfer function  $G(s)$  in Eq. (16.8) in terms of the original transfer function  $G_{old}(s)$  of Eq. (16.7), we use current injection at the port, as illustrated in Fig. 16.5. There are now two independent inputs: the input  $u(s)$  and the independent current source  $i(s)$ . The dependent quantities  $y(s)$  and  $v(s)$  can be expressed as functions of these independent inputs using the principle of superposition:

$$y(s) = G_{old}(s)u(s) + G_i(s)i(s) \quad (16.10)$$

$$v(s) = G_v(s)u(s) + Z_D(s)i(s) \quad (16.11)$$



**Fig. 16.5** Current injection at the electrical port, by addition of independent current source  $i(s)$

where

$$G_{old}(s) = \left. \frac{y(s)}{u(s)} \right|_{i(s)=0} \quad (16.12)$$

$$G_i(s) = \left. \frac{y(s)}{i(s)} \right|_{u(s)=0} \quad (16.13)$$

$$Z_D(s) = \left. \frac{v(s)}{i(s)} \right|_{u(s)=0} \quad (16.14)$$

$$G_v(s) = \left. \frac{v(s)}{u(s)} \right|_{i(s)=0} \quad (16.15)$$

are the transfer functions from the independent inputs to the respective dependent quantities  $y(s)$  and  $v(s)$ .

The transfer function  $G(s)$  can be found by elimination of  $v(s)$  and  $i(s)$  from the system of equations (16.9) to (16.11), and solution for  $y(s)$  as a function of  $u(s)$ . The result is

$$G(s) = \frac{y(s)}{u(s)} = G_{old}(s) - \frac{G_v(s)G_i(s)}{Z(s) + Z_D(s)} \quad (16.16)$$

This intermediate result expresses the new transfer function  $G(s)$  as a function of the original transfer function  $G_{old}(s)$  and the extra element  $Z(s)$ , as well as the quantities  $Z_D(s)$ ,  $G_v(s)$ , and  $G_i(s)$ .

Equation (16.14) gives a direct way to find the quantity  $Z_D(s)$ .  $Z_D(s)$  is the driving-point impedance at the port, when the input  $u(s)$  is set to zero. This quantity can be found either by conventional circuit analysis or simulation, or by laboratory measurement.

Although  $G_v(s)$  and  $G_i(s)$  could also be determined from the definitions (16.13) and (16.15), it is preferable to eliminate these quantities, and instead express  $G(s)$  as a function of the impedances at the given port. This can be accomplished via the following thought experiment. In the presence of the input  $u(s)$ , we adjust the independent current source  $i(s)$  in the special way that causes the output  $y(s)$  to be nulled to zero. The impedance  $Z_N(s)$  is defined as the ratio of  $v(s)$  to  $i(s)$  under these null conditions:

$$Z_N(s) = \left. \frac{v(s)}{i(s)} \right|_{\substack{y(s) \rightarrow 0 \\ \text{null}}} \quad (16.17)$$

The value of  $i(s)$  that achieves the null condition  $y(s) \rightarrow 0$  can be found by setting  $y(s) = 0$  in Eq. (16.10), as follows:

$$[G_{old}(s)u(s) + G_i(s)i(s)] \rightarrow 0 \quad (16.18)$$

Hence, the output  $y(s)$  is nulled when the inputs  $u(s)$  and  $i(s)$  are related as follows:

$$u(s) \Big|_{\substack{y(s) \rightarrow 0 \\ \text{null}}} = -\frac{G_i(s)}{G_{old}(s)} i(s) \Big|_{\substack{y(s) \rightarrow 0 \\ \text{null}}} \quad (16.19)$$

Under this null condition, the voltage  $v(s)$  is given by

$$\begin{aligned} v(s) \Big|_{\substack{y(s) \rightarrow 0 \\ \text{null}}} &= G_v(s)u(s) \Big|_{\substack{y(s) \rightarrow 0 \\ \text{null}}} + Z_D(s)i(s) \Big|_{\substack{y(s) \rightarrow 0 \\ \text{null}}} \\ &= \left( -\frac{G_v(s)G_i(s)}{G_{old}(s)} + Z_D(s) \right) i(s) \Big|_{\substack{y(s) \rightarrow 0 \\ \text{null}}} \end{aligned} \quad (16.20)$$

which follows from Eqs. (16.11) and (16.19). Substitution of Eq. (16.17) into Eq. (16.20) yields

$$v(s) \Big|_{\substack{y(s) \rightarrow 0 \\ \text{null}}} = Z_N(s)i(s) \Big|_{\substack{y(s) \rightarrow 0 \\ \text{null}}} = \left( -\frac{G_v(s)G_i(s)}{G_{old}(s)} + Z_D(s) \right) i(s) \Big|_{\substack{y(s) \rightarrow 0 \\ \text{null}}} \quad (16.21)$$

Hence,

$$Z_N(s) = Z_D(s) - \frac{G_v(s)G_i(s)}{G_{old}(s)} \quad (16.22)$$

Solution for the quantity  $G_v(s)G_i(s)$  yields

$$G_v(s)G_i(s) = (Z_D(s) - Z_N(s))G_{old}(s) \quad (16.23)$$

Thus, the unknown quantities  $G_v(s)$  and  $G_i(s)$  can be related to  $Z_N(s)$  and  $Z_D(s)$ , which are properties of the port at which the new impedance  $Z(s)$  will be connected, and to the original transfer function  $G_{old}(s)$ .

The final step is to substitute Eq. (16.23) into Eq. (16.16), leading to

$$G(s) = G_{old}(s) - \frac{Z_D(s) - Z_N(s)}{Z(s) + Z_D(s)}G_{old}(s) \quad (16.24)$$

This expression can be simplified as follows:

$$G(s) = G_{old}(s) \left( \frac{1 + \frac{Z_N(s)}{Z(s)}}{1 + \frac{Z_D(s)}{Z(s)}} \right) \quad (16.25)$$

or,

$$G(s) = \left( G(s) \Big|_{Z(s) \rightarrow \infty} \right) \left( \frac{1 + \frac{Z_N(s)}{Z(s)}}{1 + \frac{Z_D(s)}{Z(s)}} \right) \quad (16.26)$$

This is the desired result. It states how the transfer function  $G(s)$  is modified by addition of the extra element  $Z(s)$ . The right-most term in Eq. (16.26) is called the *correction factor*; this term gives a quantitative measure of the change in  $G(s)$  arising from the introduction of  $Z(s)$ .

Derivation of the dual result, Eq. (16.3), follows similar steps.

### 16.1.3 Discussion

The general form of the Extra Element Theorem makes it useful for designing a system such that unwanted circuit elements do not degrade the desirable system performance already obtained. For example, suppose that we already know some transfer function or similar quantity  $G(s)$ , under simplified or ideal conditions, and have designed the system such that this quantity meets specifications. We can then use the Extra Element Theorem to answer the following questions:

- What is the effect of a parasitic element  $Z(s)$  that was not included in the original analysis?
- What happens if we later decide to add some additional components having impedance  $Z(s)$  to the system?
- Can we establish some conditions on  $Z(s)$  that ensure that  $G(s)$  is not substantially changed?

A common application of the Extra Element Theorem is the determination of conditions on the extra element that guarantee that the transfer function  $G(s)$  is not significantly altered. According to Eqs. (16.2) and (16.26), this will occur when the correction factor is approximately equal to unity. The conditions are

$$\begin{aligned} \|Z(j\omega)\| &\gg \|Z_N(j\omega)\| \\ \|Z(j\omega)\| &\gg \|Z_D(j\omega)\| \end{aligned} \quad (16.27)$$

This gives a formal way to show when an impedance can be ignored: one can plot the impedances  $\|Z_N(j\omega)\|$  and  $\|Z_D(j\omega)\|$ , and compare the results with a plot of  $\|Z(j\omega)\|$ . The impedance  $Z(s)$  can be ignored over the range of frequencies where the inequalities (16.27) are satisfied.

For the dual case in which the new impedance is inserted where there was previously a short circuit, Eq. (16.3), the inequalities are reversed:

$$\begin{aligned}\|Z(j\omega)\| &\ll \|Z_N(j\omega)\| \\ \|Z(j\omega)\| &\ll \|Z_D(j\omega)\|\end{aligned}\quad (16.28)$$

This equation shows how to limit the magnitude  $\|Z(j\omega)\|$ , to avoid significantly changing the transfer function  $G(s)$ .

For quantitative design, Eqs. (16.27) and (16.28) raise an additional question: By what factor should  $\|Z(j\omega)\|$  exceed (or be less than)  $\|Z_N(j\omega)\|$  and  $\|Z_D(j\omega)\|$ , in order for the inequalities of Eq. (16.27) or (16.28) to be well satisfied? This question can be answered by plotting the magnitudes and phases of the correction factor terms, as a function of the magnitudes and phases of  $(Z/Z_N)$  and  $(Z/Z_D)$ .

Figure 16.6 shows contours of constant  $\|1 + Z/Z_N\|$ , as a function of the magnitude and phase of  $Z/Z_N$ . Figure 16.7 shows similar contours of constant  $\angle(1 + Z/Z_N)$ . It can be seen that, when  $\|Z/Z_N\|$  is less than  $-20$  dB, then the maximum deviation caused by the numerator  $(1 + Z/Z_N)$  term is less than  $\pm 1$  dB in magnitude, and less than  $\pm 7^\circ$  in phase. For  $\|Z/Z_N\|$  less than  $-10$  dB, the maximum deviation caused by the numerator  $(1 + Z/Z_N)$  term is less than  $\pm 3.5$  dB in magnitude, and less than  $\pm 20^\circ$  in phase.

Figures 16.8 and 16.9 contain contours of constant  $\|1/(1 + Z/Z_D)\|$  and  $\angle 1/(1 + Z/Z_D)$ , respectively, as a function of the magnitude and phase of  $Z/Z_D$ . These plots contain minus signs because the terms appear in the denominator of the correction factor; otherwise, they are identical to Figs. 16.6 and 16.7. Again, for  $\|Z/Z_D\|$  less than  $-20$  dB, the maximum deviation caused by the denominator  $(1 + Z/Z_D)$  term is less than  $\pm 1$  dB in magnitude, and less than  $\pm 7^\circ$  in phase. For  $\|Z/Z_D\|$  less than  $-10$  dB, the maximum deviation caused by the denominator  $(1 + Z/Z_D)$  term is less than  $\pm 3.5$  dB in magnitude, and less than  $\pm 20^\circ$  in phase.

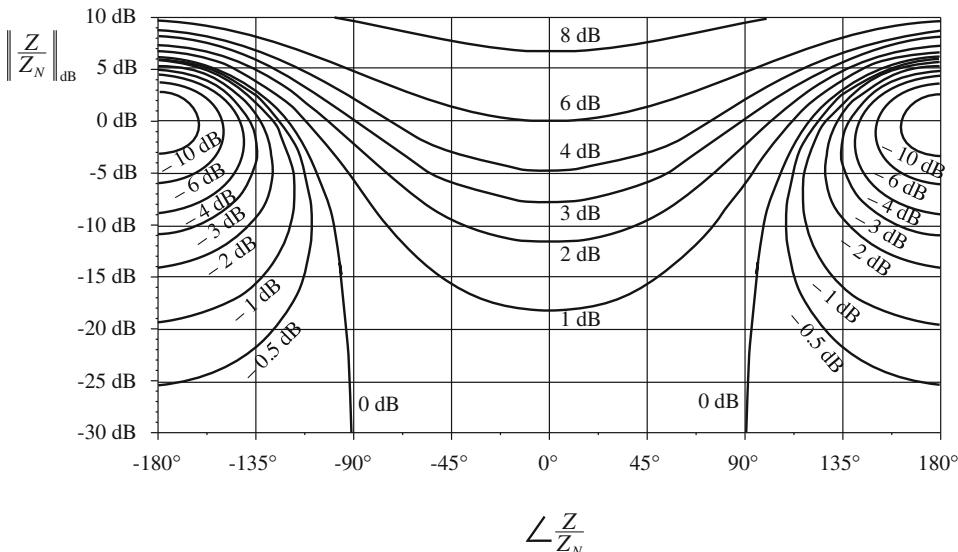
## 16.2 EET Examples

### 16.2.1 A Simple Transfer Function

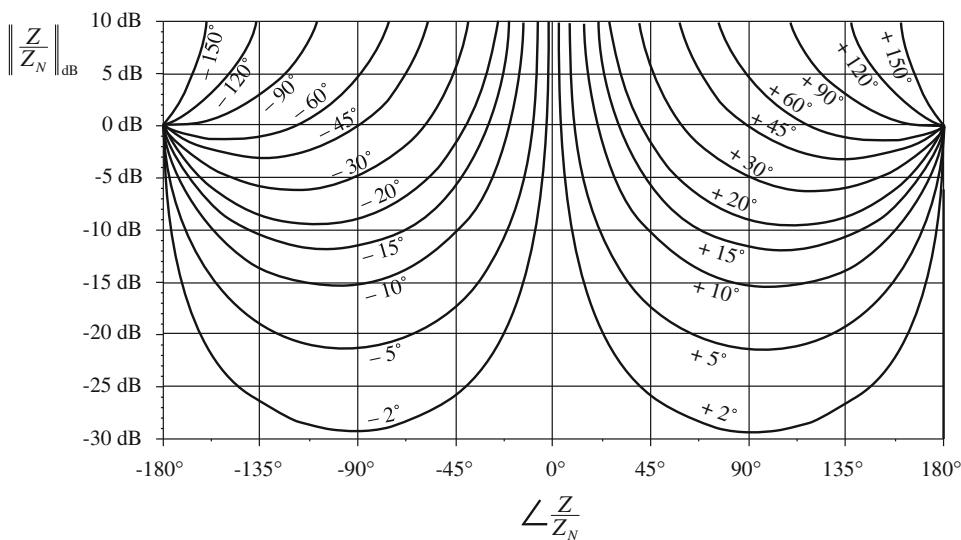
The first example illustrates how the Extra Element Theorem can be used to find a transfer function essentially by inspection. We are given the circuit illustrated in Fig. 16.10. It is desired to solve for the transfer function

$$G(s) = \frac{v_2(s)}{v_1(s)} \quad (16.29)$$

and to express this transfer function in factored pole-zero form. One way to do this is to employ the Extra Element Theorem, treating the capacitor  $C$  as an “extra” element. As illustrated in Fig. 16.11, the electrical port is taken to be at the location of the capacitor, and the “original conditions” are taken to be the case when the capacitor impedance is infinite, i.e., an open circuit. Under these original conditions, the transfer function is given by the voltage divider composed of resistors  $R_1$ ,  $R_3$ , and  $R_4$ . Hence,  $G(s)$  can be expressed as



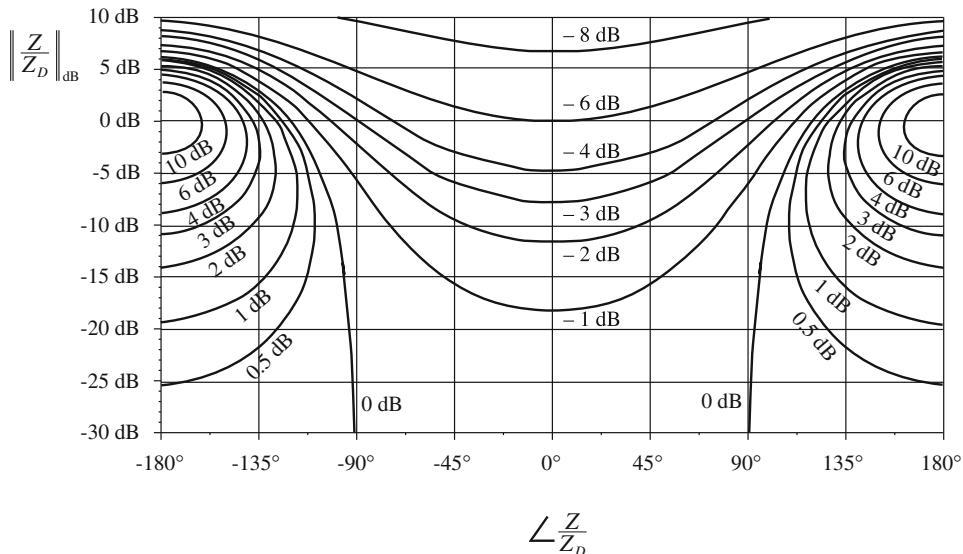
**Fig. 16.6** Contours of constant  $\|1 + Z/Z_N\|$ , as a function of the magnitude and phase of  $Z/Z_N$



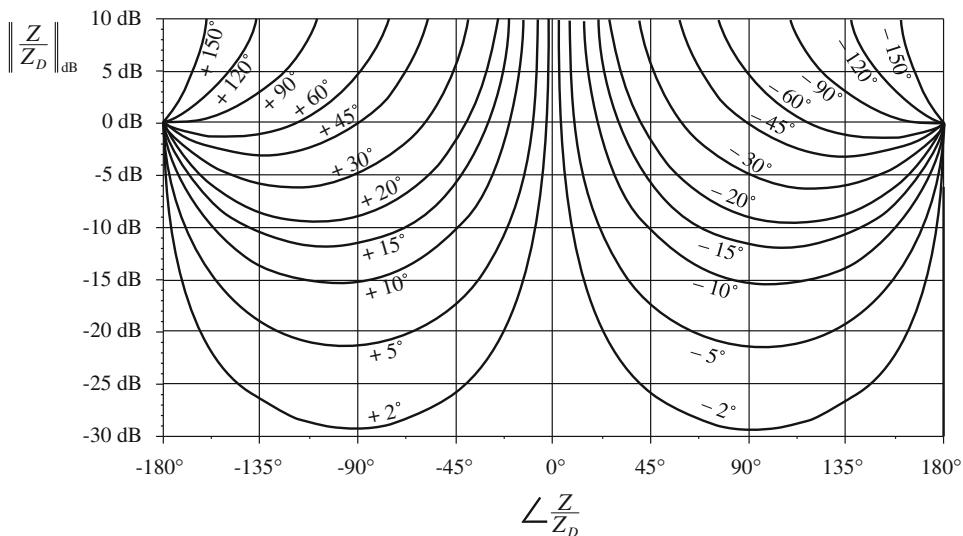
**Fig. 16.7** Contours of constant  $\angle(1 + Z/Z_N)$ , as a function of the magnitude and phase of  $Z/Z_N$

$$\frac{v_2(s)}{v_1(s)} = G(s) = \left( \frac{R_4}{R_1 + R_3 + R_4} \right) \frac{\left( 1 + \frac{Z_N}{Z} \right)}{\left( 1 + \frac{Z_D}{Z} \right)} \quad (16.30)$$

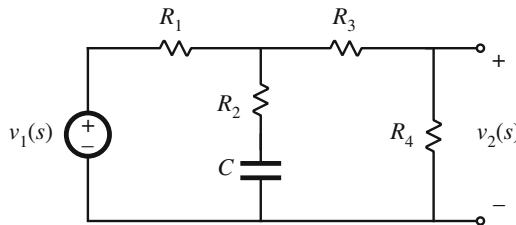
where  $Z(s)$  is the capacitor impedance  $1/sC$ .



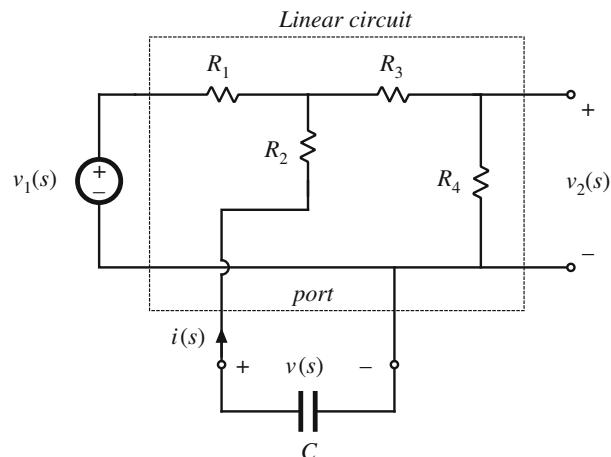
**Fig. 16.8** Contours of constant  $\|1 + Z/Z_D\|$ , as a function of the magnitude and phase of  $Z/Z_D$



**Fig. 16.9** Contours of constant  $\angle(1 + Z/Z_D)$ , as a function of the magnitude and phase of  $Z/Z_D$



**Fig. 16.10**  $R$ - $C$  circuit example of Sect. 16.2.1



**Fig. 16.11** Manipulation of the circuit of Fig. 16.10 into the form of Fig. 16.1

The impedance  $Z_D(s)$  is the Thevenin equivalent impedance seen at the port where the capacitor is connected. As illustrated in Fig. 16.12a, this impedance is found by setting the independent source  $v_1(s)$  to zero, and then determining the impedance between the port terminals. The result is

$$Z_D = R_2 + R_1\parallel(R_3 + R_4) \quad (16.31)$$

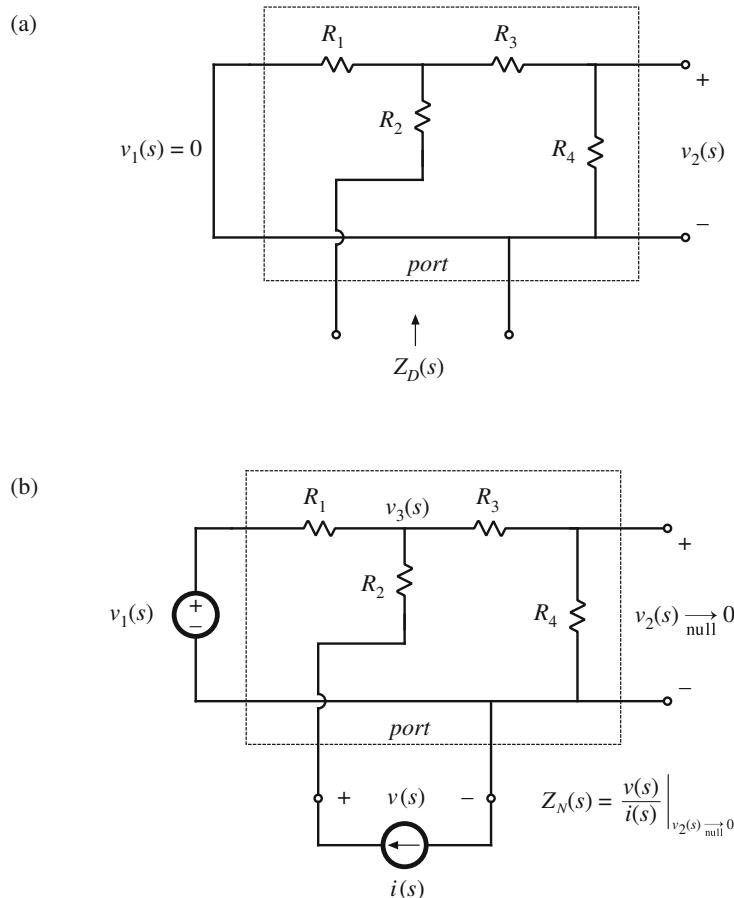
Figure 16.12b illustrates determination of the impedance  $Z_N(s)$ . A current source  $i(s)$  is connected to the port, in place of the capacitor. In the presence of the input  $v_1(s)$ , the current source  $i(s)$  is adjusted so that the output  $v_2(s)$  is nulled. Under these null conditions, the impedance  $Z_N(s)$  is found as the ratio of  $v(s)$  to  $i(s)$ .

It is easiest to find  $Z_N(s)$  by first determining the effect of the null condition on the signals in the circuit. Since  $v_2$  is nulled to zero, there is no current through the resistor  $R_4$ . Since  $R_3$  is connected in series with  $R_4$ , there is also no current through  $R_3$ , and hence no voltage across  $R_3$ . Therefore, the voltage  $v_3$  in Fig. 16.12b is equal to  $v_2$ , i.e.,

$$v_3 = v_2 \xrightarrow{\text{null}} 0 \quad (16.32)$$

Therefore, the voltage  $v$  is given by  $iR_2$ . The impedance  $Z_N$  is

$$Z_N(s) = \left. \frac{v(s)}{i(s)} \right|_{v_2 \rightarrow 0} = R_2 \quad (16.33)$$



**Fig. 16.12** Measurement of the quantities  $Z_N(s)$  and  $Z_D(s)$ : (a) determination of  $Z_D(s)$ ; (b) determination of  $Z_N(s)$

Note that, in general, the independent sources  $v_1$  and  $i$  are nonzero during the  $Z_N$  measurement. For this example, the null condition implies that the current  $i(s)$  flows entirely through the path composed of  $R_2$ ,  $R_1$ , and  $v_1$ .

The transfer function  $G(s)$  is found by substitution of Eqs. (16.31) and (16.33) into Eq. (16.30):

$$G(s) = \left( \frac{R_4}{R_1 + R_3 + R_4} \right) \frac{(1 + sCR_2)}{(1 + sC[R_2 + R_1 \parallel (R_3 + R_4)])} \quad (16.34)$$

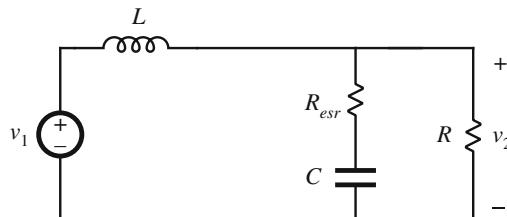
For this example, the result is obtained in standard normalized pole-zero form, because the capacitor is the only dynamic element in the circuit, and because the “original conditions,” in which the capacitor impedance tends to an open circuit, coincide with dc conditions in the circuit. A similar procedure can be applied to write the transfer function of a circuit, containing an arbitrary number of reactive elements, in normalized form via the  $n$ -Extra Element Theorem of Sect. 16.3.

### 16.2.2 An Unmodeled Element

In the simple  $R-L-C$  low-pass filter illustrated in Fig. 16.13, the capacitor dielectric loss, contact (termination) resistance, and foil resistance are modeled by a series resistance  $R_{esr}$ , known as the capacitor *equivalent series resistance* (ESR). Physical capacitors can contain significant ESR, which can degrade performance and can also lead to failure when the power loss  $I_{rms}^2 R_{esr}$  causes excessive temperature rise within the capacitor. The presence of ESR also alters the filter transfer function. In first-pass analysis of the transfer function, the ESR often is ignored (“unmodeled”); later, it may be desired to include the effects of this element in the analysis. The object of this simple example is to include the ESR in the filter transfer function, as an extra element.

The filter transfer function  $G(s)$  is defined as

$$G(s) = \frac{v_2}{v_1} \quad (16.35)$$

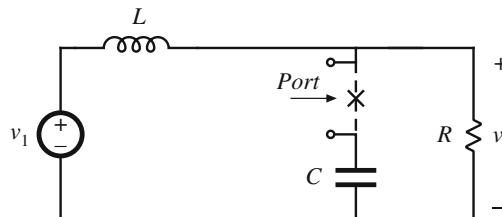


**Fig. 16.13**  $R-L-C$  filter example

For the case  $R_{esr} \rightarrow 0$ , the filter transfer function is

$$G(s) \Big|_{R_{esr} \rightarrow 0} = \frac{1}{1 + \frac{sL}{R} + s^2 LC} \quad (16.36)$$

We can therefore employ the Extra Element Theorem to determine how nonzero ESR changes  $G(s)$ . As illustrated in Fig. 16.14, we view the “original circuit” as the case where the ESR is a short circuit, and addition of the “extra element” constitutes breaking this short circuit at the port as shown.

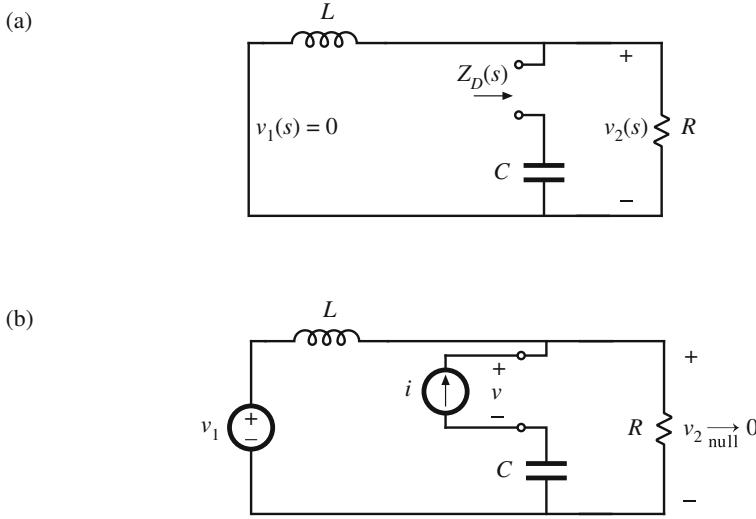


**Fig. 16.14** Treating the capacitor ESR as an extra element

In the presence of the ESR, the transfer function becomes

$$G(s) = \left( G(s) \Big|_{R_{esr} \rightarrow 0} \right) \frac{\left( 1 + \frac{Z(s)}{Z_N(s)} \right)}{\left( 1 + \frac{Z(s)}{Z_D(s)} \right)} \quad (16.37)$$

where  $Z(s)$  is equal to  $R_{esr}$ .



**Fig. 16.15** Capacitor ESR example: (a) determination of  $Z_D(s)$ ; (b) determination of  $Z_N(s)$

Figure 16.15a illustrates determination of  $Z_D(s)$ . The input source  $v_1(s)$  is set to zero, and the impedance between the terminals of the port is found. It can be seen that the impedance  $Z_D(s)$  reduces to the capacitor impedance, in series with the parallel combination of the inductor impedance and the load resistance  $R$ :

$$Z_D(s) = \frac{1}{sC} + \left( R \parallel sL \right) = \frac{1 + \frac{sL}{R} + s^2 LC}{sC \left( 1 + \frac{sL}{R} \right)} \quad (16.38)$$

Figure 16.15b illustrates determination of  $Z_N(s)$ . In the presence of the input source  $v_1(s)$ , a current  $i(s)$  is injected at the port as shown. This current is adjusted such that the output  $v_2(s)$  is nulled. Under these conditions, the quantity  $Z_N(s)$  is given by  $v(s)/i(s)$ . It can be seen that when  $v_2(s)$  is nulled, the voltage  $v(s)$  is equal to the current  $i(s)$  multiplied by the capacitor impedance  $1/sC$ . Therefore,

$$Z_N(s) = \left. \frac{v(s)}{i(s)} \right|_{v_2(s) \rightarrow 0} = \frac{1}{sC} \quad (16.39)$$

Note that, in general,  $i(s)$  will not be equal to zero during the  $Z_N(s)$  measurement. The null condition is achieved by setting the source  $i(s)$  equal to the value  $-v_1(s)/sL$ . Thus, in the presence of nonzero  $R_{esr}$ , the transfer function  $G(s)$  can be expressed as follows:

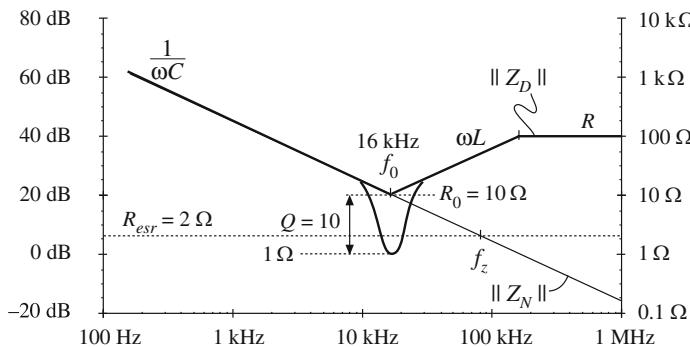
$$\begin{aligned} G(s) &= \left( G(s) \Big|_{R_{esr} \rightarrow 0} \right) \frac{\left( 1 + \frac{R_{esr}}{Z_N(s)} \right)}{\left( 1 + \frac{R_{esr}}{Z_D(s)} \right)} \\ &= \left( \frac{1}{1 + \frac{sL}{R} + s^2 LC} \right) \frac{(1 + sCR_{esr}))}{\left( 1 + \frac{R_{esr}}{Z_D(s)} \right)} \end{aligned} \quad (16.40)$$

It can be seen that the correction factor adds a zero at frequency  $\omega_z = 1/R_{esr}C$ , arising from the  $Z_N$  term. The denominator  $Z_D$  term may additionally modify the transfer function; the denominator term has negligible effect provided that

$$R_{esr} \ll \|Z_D\| \quad (16.41)$$

We can now plot the impedance inequalities (16.28) to examine how addition of  $R_{esr}$  changes  $G(s)$ . The magnitudes of  $Z_D(s)$  and  $Z_N(s)$  are constructed in Fig. 16.16 for the values  $L = 100 \mu\text{H}$ ,  $C = 1 \mu\text{F}$ ,  $R = 100 \Omega$ , and  $R_{esr} = 2 \Omega$ , using the approximate graphical construction approach of Sect. 8.3.

$Z_N$  is equal to the capacitor impedance; at low frequency,  $R_{esr} \ll \|Z_N\|$ . However, at high frequency  $\|Z_N\|$  becomes small, and it is unavoidable that  $R_{esr}$  becomes greater than  $\|Z_N\|$ . This leads to the zero at frequency  $f_z$ , as noted previously.



**Fig. 16.16** Construction of the magnitude impedance Bode plots of  $Z_N$ ,  $Z_D$ , and  $R_{esr}$

For the values given,  $\|Z_D\| \gg R_{esr}$  at all frequencies except in the vicinity of the resonant frequency  $f_0$ . In consequence, the denominator  $Z_D$  term of Eq. (16.40) is substantially equal to one, except near this resonant frequency. At the resonant frequency  $f_0$ ,  $Z_D$  is approximately equal to  $1 \Omega$ , so that the denominator  $Z_D$  term becomes equal to

$$\left(1 + \frac{R_{esr}}{Z_D(s)}\right) = \left(1 + \frac{2 \Omega}{1 \Omega}\right) = 3 \quad (16.42)$$

This effectively reduces the transfer function  $Q$ -factor from 10 to approximately  $10/3 = 3.33$ .

By multiplying out Eq. (16.40), it can be verified that the exact transfer function  $G(s)$  can be expressed as

$$G(s) = \frac{(1 + sCR_{esr})}{1 + s\left(\frac{L}{R} + R_{esr}C\right) + s^2LC\left(\frac{R + R_{esr}}{R}\right)} \quad (16.43)$$

The effect of the denominator  $Z_D$  term is to reduce the exact  $Q$ -factor from 10 to 3.37, and to reduce the resonant frequency  $f_0$  from 15.9 kHz to 15.8 kHz.

### 16.2.3 SEPIC Example

As a third example, let us consider derivation and design of the small-signal transfer functions of the SEPIC. A small-signal SEPIC model is derived using average switch modeling in Sect. 14.1.3, with the result given in Fig. 14.7 and reproduced in Fig. 16.17. Analysis of the transfer function  $G_{vd}(s)$  is tedious because of the convoluted nature of the circuit that results from averaged switch modeling. The Extra Element Theorem gives an alternate approach to solution of this circuit, leading to a simplified interpretation of the transfer functions. This approach also leads to insight into how to damp the internal resonance of this fourth-order system, so that the small-signal transfer functions are better behaved.

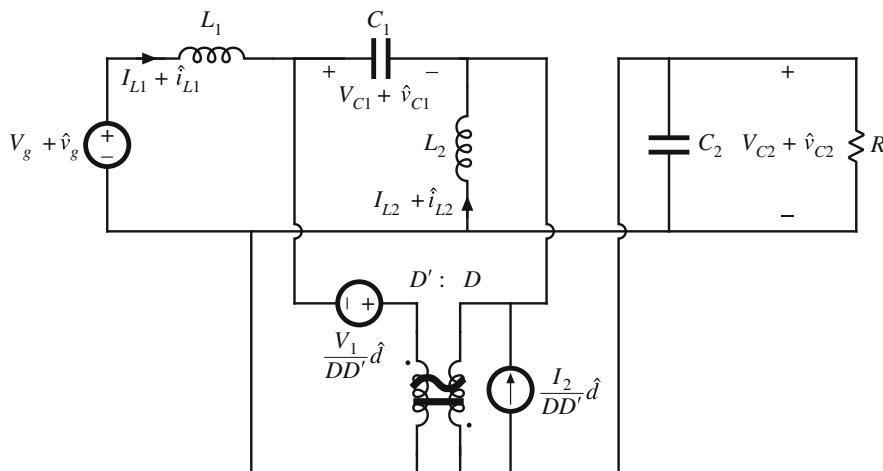
The difficulty in solution of the model of Fig. 16.17 arises from element  $C_1$ , which provides a path parallel to the DC transformer to couple the input and output sections of the model. If this element were not present, solution of the circuit would be considerably simpler. Therefore, the strategy employed in this section is to let  $C_1$  become an open circuit, and solve the much simpler model that is obtained. The Extra Element Theorem is then employed to incorporate the effects of  $C_1$  into the transfer functions such as  $G_{vd}(s)$ . We define

$$G_{vd-bb} = \left. \frac{\hat{v}}{\hat{d}} \right|_{C_1 \rightarrow 0} \quad (16.44)$$

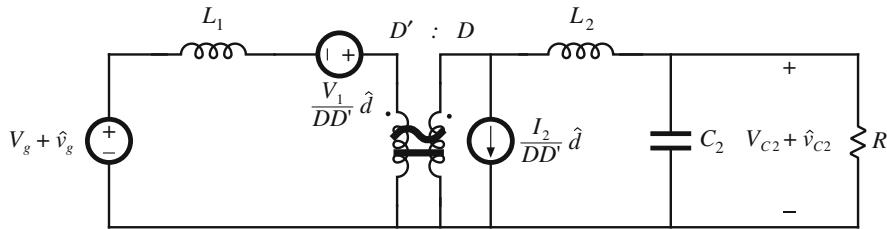
The Extra Element Theorem predicts that this transfer function can be written as follows:

$$G_{vd} = G_{vd-bb} \left( \frac{1 + \frac{Z_N}{Z}}{1 + \frac{Z_D}{Z}} \right) \quad (16.45)$$

with  $Z = 1/sC_1$ . The quantities  $Z_N$ , and  $Z_D$  are found using the Extra Element Theorem. The impedance  $Z_D$  is the driving-point impedance at the port where  $C_1$  is connected. Equations (16.44)–(16.45) state that the control-to-output transfer function of the SEPIC is equal to that of an effective buck–boost converter  $G_{vd-bb}$ , multiplied by a correction factor that accounts for the effects of  $C_1$  and its associated resonances.



**Fig. 16.17** The small-signal averaged switch model of the SEPIC, Fig. 14.7



**Fig. 16.18** When  $C_1 \rightarrow 0$ , the SEPIC model reduces to an effective buck-boost converter

When we let  $C_1$  tend to an open circuit, the SEPIC model of Fig. 16.17 can be reduced to the effective buck-boost converter model illustrated in Fig. 16.18. The transfer functions of this circuit can now be found in the usual manner, as described in Chaps. 7 and 8. The transfer function from  $\hat{d}$  to  $\hat{v}$  is found by setting the  $\hat{v}_g$  source to zero and solving for  $\hat{v}$ , with the following result:

$$G_{vd-bb}(s) = \frac{V_g}{D'^2} \frac{1 - s \frac{L_1}{R} \left( \frac{D}{D'} \right)^2}{1 + s \left( \frac{L_2 + \left( \frac{D}{D'} \right)^2 L_1}{R} \right) + s^2 C_2 \left( L_2 + \left( \frac{D}{D'} \right)^2 L_1 \right)} \quad (16.46)$$

This expression is of the form

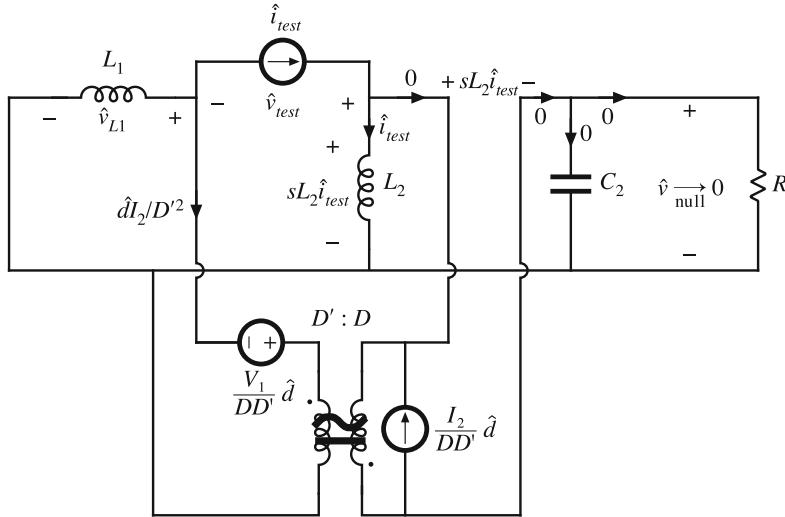
$$G_{vd-bb}(s) = G_{d0} \frac{1 - \frac{s}{\omega_z}}{1 + \frac{s}{Q_o \omega_o} + \left( \frac{s}{\omega_o} \right)^2} \quad (16.47)$$

with

$$\begin{aligned} G_{d0} &= \frac{V_g}{D'^2} \\ \omega_o &= \frac{1}{\sqrt{C_2 \left( L_2 + \left( \frac{D}{D'} \right)^2 L_1 \right)}} \\ Q_o &= R \sqrt{\frac{C_2}{L_2 + \left( \frac{D}{D'} \right)^2 L_1}} \\ \omega_z &= \frac{R}{L_1} \left( \frac{D'}{D} \right)^2 \quad (\text{RHP}) \end{aligned} \quad (16.48)$$

Thus,  $G_{vd-bb}$  contains quadratic poles and a RHP zero.

Derivation of  $Z_N$  is illustrated in Fig. 16.19. The  $\hat{v}_g$  source is set to zero. In the presence of  $\hat{d}$ , a current  $\hat{i}_{test}$  is injected into the port where  $C_1$  would be connected. The sources are adjusted to null the output  $\hat{v}$ .

**Fig. 16.19** Derivation of  $Z_N$ 

The quantity  $Z_N$  is given by

$$Z_N = \left. \frac{\hat{v}_{test}}{\hat{i}_{test}} \right|_{\hat{v} \rightarrow 0} \quad (16.49)$$

To analyze this circuit, we start with the null condition, and follow the signals towards the injection port. With the output voltage nulled  $\hat{v} \rightarrow 0$ , the current in the load resistance  $R$  and the output capacitance  $C_2$  are also nulled. This implies that the current in the transformer secondary and primary windings are determined solely by the  $\hat{d}I_2/DD'$  current source of the averaged switch model. Consequently, the primary current is  $\hat{d}I_2/D'^2$  as shown. Additionally, the injection current  $\hat{i}_{test}$  flows entirely through inductor  $L_2$ , and the voltage across  $L_2$  is equal to  $sL_2 \hat{i}_{test}$ . This voltage also appears across the transformer secondary, and can be employed to find the transformer primary voltage. This allows us to express the inductor  $L_1$  voltage as:

$$\hat{v}_{L1} = -\frac{V_1 \hat{d}}{DD'} - sL_2 \hat{i}_{test} \frac{D'}{D} \quad (16.50)$$

We can also write the loop equation

$$\hat{v}_{test} + \hat{v}_{L1} = sL_2 \hat{i}_{test} \quad (16.51)$$

Finally, we can write the node equation

$$\frac{\hat{v}_{L1}}{sL_1} + \frac{\hat{d}I_2}{D'^2} + \hat{i}_{test} = 0 \quad (16.52)$$

Elimination of  $\hat{v}_{L1}$  and  $\hat{d}$  from Eqs. 16.50, 16.51, and 16.52, and solution for  $\hat{v}_{test}/\hat{i}_{test}$ , leads to the following expression for  $Z_N$ :

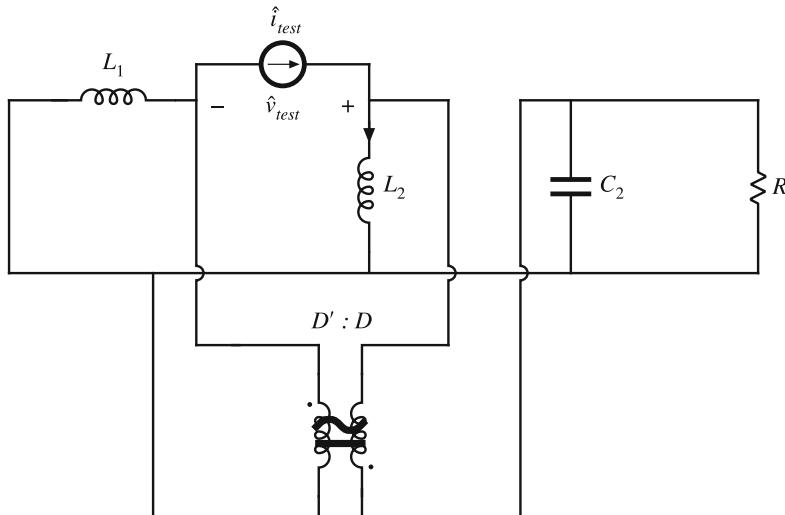
$$Z_N(s) = s(L_1 + L_2) \frac{\left(1 - s \frac{L_1||L_2}{R} \frac{D}{D'^2}\right)}{\left(1 - s \frac{D^2 L_1}{D'^2 R}\right)} \quad (16.53)$$

This equation is of the form

$$Z_N(s) = s(L_1 + L_2) \frac{\left(1 - \frac{s}{\omega_{zN}}\right)}{\left(1 - \frac{s}{\omega_z}\right)} \quad (16.54)$$

It should be noted that a null impedance such as  $Z_N$  is not a passive or driving-point impedance, and it is possible for this impedance to be negative or to contain RHP poles or zeroes. Equation (16.53) predicts that  $Z_N$  exhibits a low-frequency asymptote given by the series combination  $s(L_1 + L_2)$ , which is purely inductive and exhibits phase of  $+90^\circ$ .  $Z_N$  contains a RHP zero and a RHP pole; the RHP pole coincides with the RHP zero  $\omega_z$  of  $G_{vd-bb}$ . The high-frequency asymptote is given by  $sL_2/D$ , which also is purely inductive with  $+90^\circ$  phase.

The quantity  $Z_D$  is the driving-point impedance seen at the capacitor  $C_1$  port, with the  $\hat{v}_g$  and  $\hat{d}$  sources set to zero. As illustrated in Fig. 16.20, a test current  $\hat{i}_{test}$  is injected at the port, and the port voltage  $\hat{v}_{test}$  is measured. Since there are no null conditions associated with  $Z_D$ , this quantity generally depends on all elements, and therefore the algebra is more complex.



**Fig. 16.20** Derivation of  $Z_D$

With some analysis and careful algebra, one can show that

$$Z_D(s) = s(L_1 + L_2) \frac{\left(1 + s \frac{L_1 \| L_2}{D'^2 R} + s^2 \frac{L_1 \| L_2}{D'^2} C_2\right)}{\left(1 + s \frac{L_2 + \left(\frac{D}{D'}\right)^2 L_1}{R} + s^2 C_2 \left(L_2 + \left(\frac{D}{D'}\right)^2 L_1\right)\right)} \quad (16.55)$$

This expression is of the form

$$Z_D(s) = s(L_1 + L_2) \frac{\left(1 + \frac{s}{Q_{zD}\omega_{zD}} + \left(\frac{s}{\omega_{zD}}\right)^2\right)}{\left(1 + \frac{s}{Q_o\omega_o} + \left(\frac{s}{\omega_o}\right)^2\right)} \quad (16.56)$$

with

$$\omega_{zD} = \frac{D'}{\sqrt{(L_1 \| L_2)C_2}} \quad (16.57)$$

$$Q_{zD} = D'R \sqrt{\frac{C_2}{L_1 \| L_2}} \quad (16.58)$$

The quantities  $G_{vd-bb}$  and  $Z_D$  have identical denominator polynomials.

Thus, the low-frequency asymptote of  $Z_D$  is equal to  $s(L_1 + L_2)$ . This asymptote is purely inductive, with a phase of  $+90^\circ$ . There are mid-frequency quadratic poles and zeroes; these may cause the mid-frequency asymptotes to become resistive or capacitive. The high-frequency asymptote is

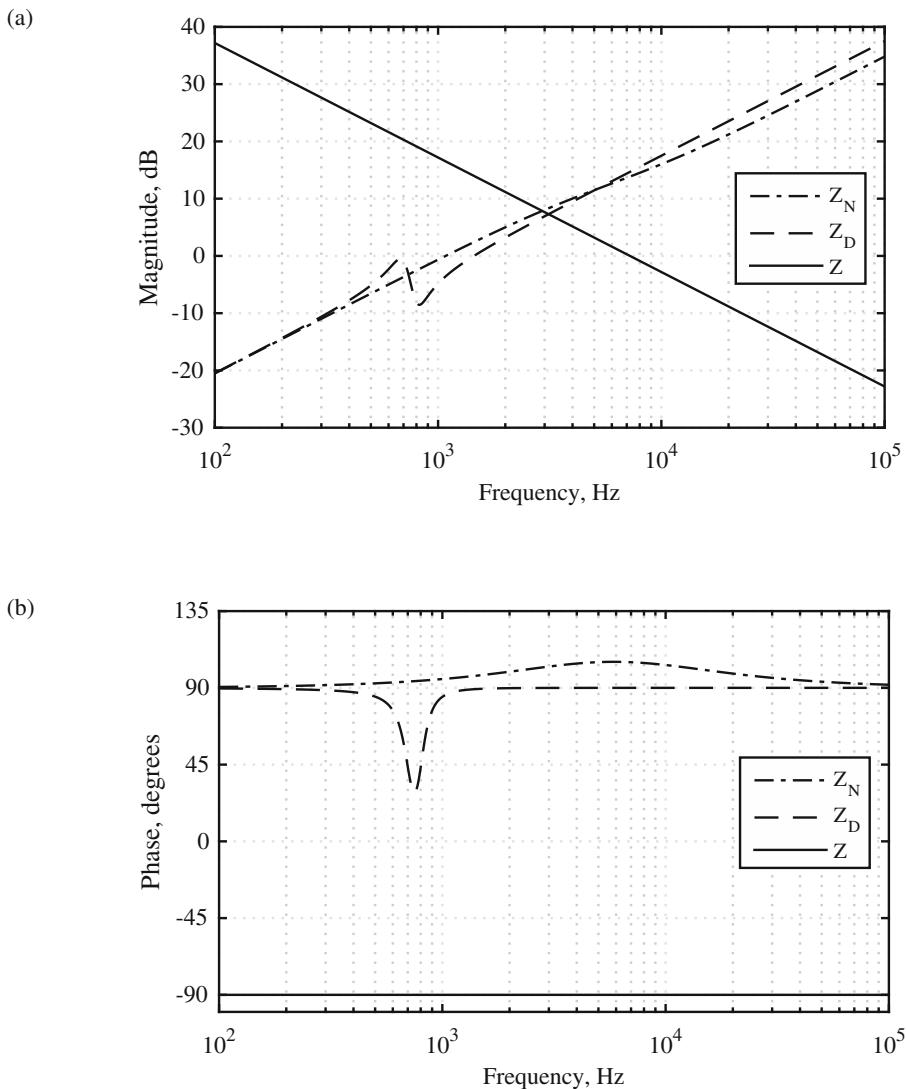
$$s(L_1 + L_2) \left(\frac{\omega_p}{\omega_z}\right)^2 = s \left(\frac{L_1}{D'^2} \parallel \frac{L_2}{D'^2}\right) \quad (16.59)$$

which again is purely inductive with phase of  $+90^\circ$ .

#### 16.2.4 Damping the SEPIC Internal Resonances

Consider a SEPIC having the following element values: input voltage  $V_g = 18$  V, output voltage  $V = 24$  V, switching frequency  $f_s = 100$  kHz, inductances  $L_1 = 100 \mu\text{H}$ ,  $L_2 = 50 \mu\text{H}$ , capacitances  $C_1 = 22 \mu\text{F}$ ,  $C_2 = 220 \mu\text{F}$ , and load resistance  $R = 5 \Omega$ . With these element values, Eq. 16.48 predicts that  $G_{vd-bb}$  contains complex poles at  $f_o = 711$  Hz with  $Q_o = 4.9$ . Additionally,  $G_{vd-bb}$  contains a RHP zero at 4.5 kHz.

The impedances  $Z_N$  (Eq. (16.53)),  $Z_D$  (Eq. (16.56)), and  $Z = 1/sC_1$  are plotted in Fig. 16.21. At frequencies below approximately 2 kHz, the capacitor  $C_1$  impedance is much greater in magnitude than either  $Z_N$  or  $Z_D$ . Hence the correction factor in Eq. (16.45) is approximately equal to 1, and the SEPIC  $G_{vd}$  is equal to the  $G_{vd-bb}$  of the effective buck-boost model. At frequencies above approximately 6 kHz, the capacitor  $C_1$  impedance is much smaller in magnitude than both  $Z_N$  and  $Z_D$ . For this case, Eq. (16.45) reduces to:



**Fig. 16.21** Magnitude and phase Bode plots of the impedances  $Z_N$ ,  $Z_D$ , and  $Z = 1/sC_1$  for the undamped SEPIC example. Dashed curves:  $Z_N$  and  $Z_D$ . Solid curves:  $Z$

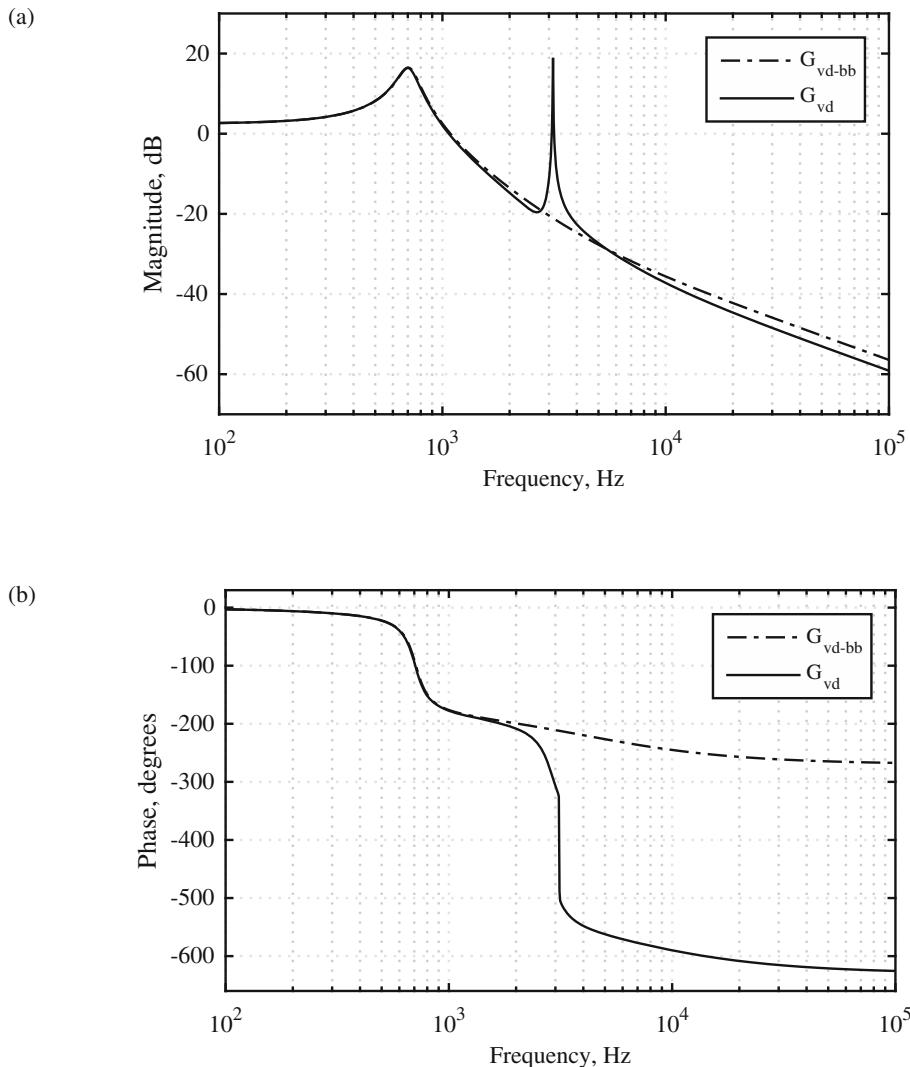
$$G_{vd} \rightarrow G_{vd-bb} \left. \frac{1 + \frac{Z_N}{Z}}{1 + \frac{Z_D}{Z}} \right|_{Z \rightarrow 0} = G_{vd-bb} \left( \frac{Z_N}{Z_D} \right) \quad (16.60)$$

Since  $Z_N$  and  $Z_D$  are both inductive above 6 kHz, the ratio  $(Z_N/Z_D)$  is constant, and hence  $G_{vd}$  is equal to  $G_{vd-bb}$  scaled by this constant.

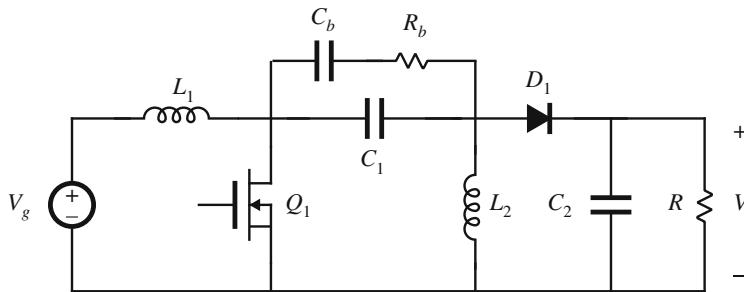
The impedance  $\|Z\|$  is equal in magnitude to  $\|Z_N\|$  or  $\|Z_D\|$  at 3 to 4 kHz. Note that the phase of the capacitor impedance  $\angle Z$  is  $-90^\circ$ , while the impedances  $Z_N$  and  $Z_D$  are essentially induc-

tive and have phases of approximately  $+90^\circ$ . Hence, at 3 to 4 kHz, the phases of  $Z/Z_N$  and  $Z/Z_D$  are approximately  $180^\circ$ , while the magnitudes are approximately equal to one. In the vicinity of these frequencies, the correction factor in Eq. (16.45) can vary substantially, according to Figs. 16.6 to 16.9. We expect the numerator and denominator terms of the correction factor to contain resonances at these frequencies.

Figure 16.22 contains a Bode plot of the control-to-output transfer functions  $G_{vd-bb}(s)$  and  $G_{vd}(s)$ . The effective buck-boost model contains resonant poles and a RHP zero, leading to



**Fig. 16.22** Magnitude and phase Bode plots of the undamped control-to-output transfer function, SEPIC example. Dashed curves: response of the effective buck-boost model  $G_{vd-bb}$ . Solid curves: response of SEPIC, including correction factor,  $G_{vd}$



**Fig. 16.23** Addition of damping network elements  $R_b$  and  $C_b$  to the SEPIC

a high-frequency phase asymptote of  $-270^\circ$ . The correction factor contributes two additional high- $Q$  poles and two RHP zeroes, in the vicinity of 3 kHz. These terms contribute an additional  $-360^\circ$  of phase at high frequencies. Consequently, it is problematic to achieve an adequate phase margin in a feedback loop having a crossover frequency above 3 kHz.

The dynamics of the SEPIC can be considerably improved by addition of a damping network to  $C_1$ , as illustrated in Fig. 16.23. This causes the “extra” impedance  $Z(s)$  to become:

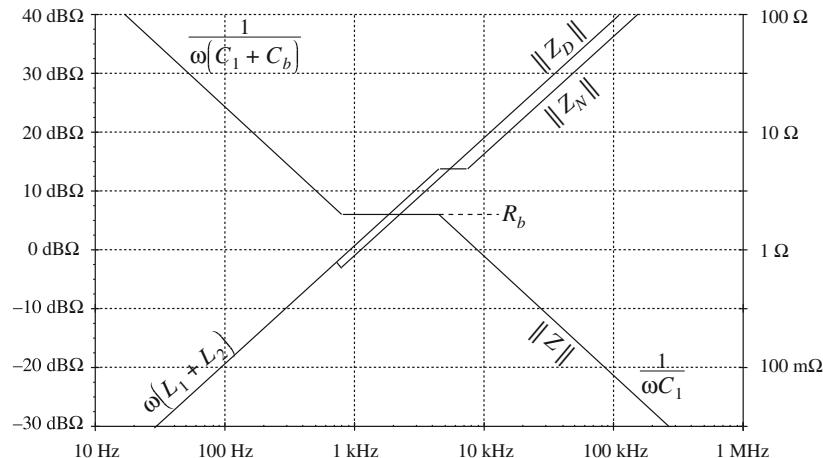
$$Z(s) = \frac{1}{sC_1} \left| \left( R_b + \frac{1}{sC_b} \right) \right| \quad (16.61)$$

The element values are chosen so that the impedance  $Z$  is dominated by the damping resistor  $R_b$  in the vicinity of the frequencies where  $\|Z\|$  is equal to  $\|Z_N\|$  or  $\|Z_D\|$ . The phase of  $Z$  tends closer to  $0^\circ$ , causing the phases of  $Z/Z_N$  and  $Z/Z_D$  to tend towards  $90^\circ$ . According to Figs. 16.6 to 16.9, the variation in the correction factor is much less extreme in this case. The damping network reduces the  $Q$ -factors of the poles and zeroes of the correction factor, and can also move its RHP zeroes into the left half-plane.

Capacitor  $C_b$  is a dc blocking capacitor that prevents a dc voltage from being applied to resistor  $R_b$ . This reduces the power loss that otherwise would be induced in  $R_b$ . The impedance of capacitor  $C_b$  should be substantially smaller than  $R_b$  at the frequencies where  $\|Z\|$  is close to  $\|Z_N\|$  or  $\|Z_D\|$ . Damping networks such as this  $R_b-C_b$  network are discussed in more detail in Chap. 17.

Figure 16.24 illustrates construction of the asymptotes of the impedances  $Z_N$  and  $Z_D$  for this example. Asymptotes for the impedance  $Z$ , including the  $R_b - C_b$  damping network designed as described above, are overlayed. Again, the damping resistor  $R_b$  dominates the impedance  $Z$  at the frequencies where  $\|Z\|$  is equal to  $\|Z_N\|$  or  $\|Z_D\|$ . The values of  $R_b$  and  $C_b$  can now be selected so that these  $Z$  asymptotes are obtained.

A Bode plot of a damped  $Z$ , using the values  $C_1 = 22\mu\text{F}$ ,  $R_b = 2\Omega$ , and  $C_b = 100\mu\text{F}$ , is illustrated in Fig. 16.25. The magnitude of  $Z$  is now equal to the magnitudes of  $Z_N$  or  $Z_D$  at frequencies in the vicinity of 2 kHz. At this frequency range, the phase of the damped  $Z$  is now approximately  $-45^\circ$ .



**Fig. 16.24** Construction of the magnitude asymptotes for  $Z_N$ ,  $Z_D$ , and the damped  $Z$

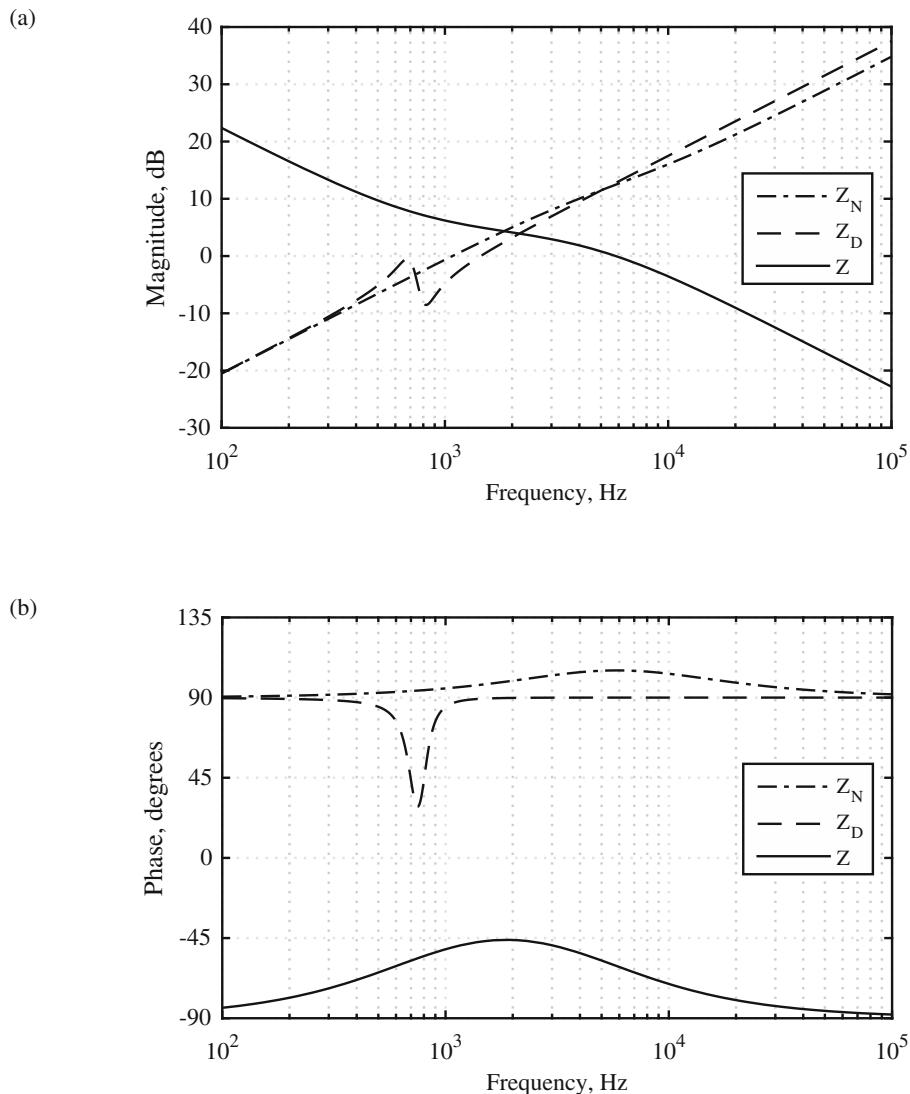
Figure 16.26 compares the resulting  $G_{vd}(s)$  with  $G_{vd-bb}(s)$ . It can be observed that the  $Q$ -factors of the correction factor poles and zeroes are substantially reduced, and the RHP zeroes have moved to the left half-plane. These poles and zeroes nearly cancel. The magnitude and phase of  $G_{vd}(s)$  now is approximately equal to that of the effective buck-boost converter model.

The SEPIC control-to-output transfer function  $G_{vd}(s)$  naturally contains four poles and three RHP zeroes. The Extra Element Theorem approach shows how this transfer function can be viewed as a simpler effective buck-boost transfer function  $G_{vd-bb}(s)$  containing two poles and one RHP zero, multiplied by a correction factor that accounts for the additional poles and zeroes. Further, the Extra Element Theorem approach provides a framework for designing a damping network that causes the correction factor poles and zeroes to approximately cancel. The resulting  $G_{vd}(s)$  is then approximately equal to the much simpler  $G_{vd-bb}(s)$ .

### 16.3 The $n$ -Extra Element Theorem

The  $n$  Extra Element Theorem ( $n$ EET) is an extension of Middlebrook's Extra Element Theorem to the case when multiple extra elements are added simultaneously to a circuit. Its major application is to write transfer functions directly as rational fractions, without need to perform loop and node analysis and algebraic manipulations. This is accomplished by treating each reactive component as an "extra" element that is added to the dc gain of the network. The method gives a physical interpretation to the coefficients of  $L$  and  $C$  in the standard normalized form of the transfer function, and it allows complex transfer functions to be derived nearly by inspection.

Use of the basic  $n$ EET to derive transfer functions is described here without proof, beginning with a simple example. Extensions involving inverted forms as special cases are also described. For a derivation and more general treatment of the  $n$ EET, the interested reader is referred to [141, 142].

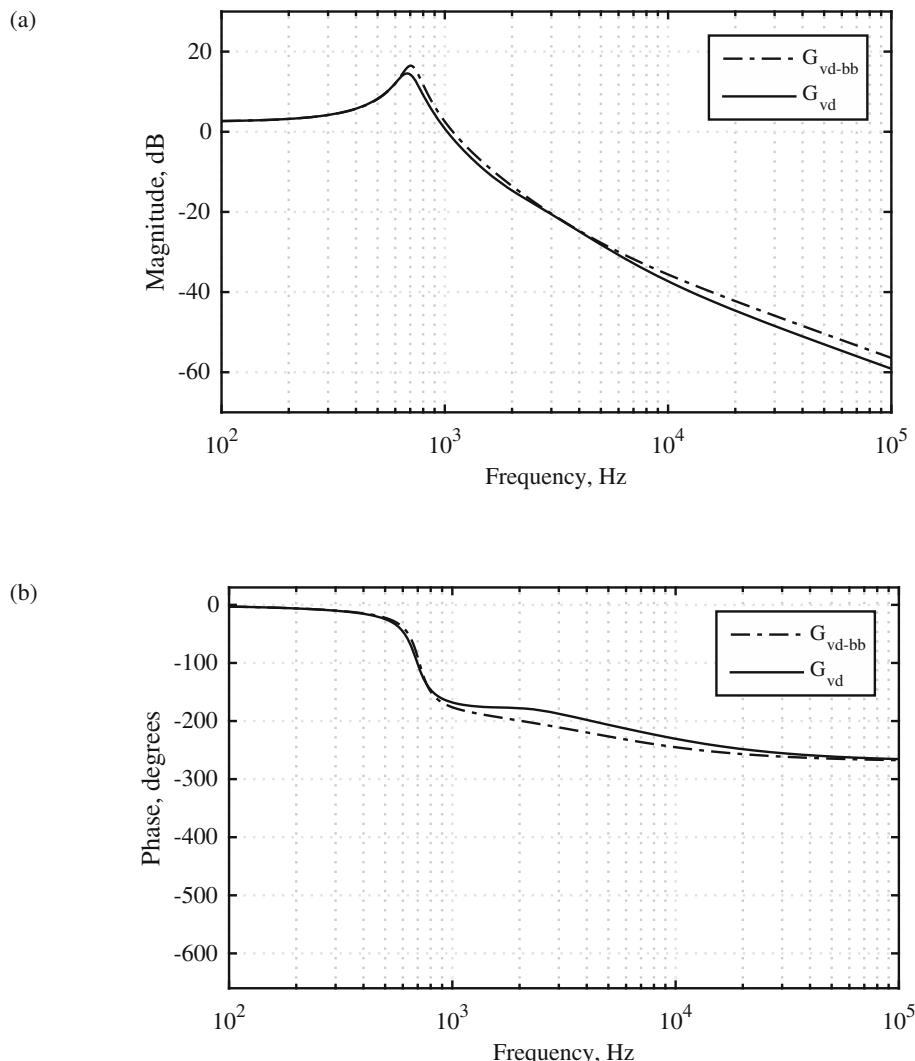


**Fig. 16.25** Magnitude and phase Bode plots of the impedances  $Z_N$ ,  $Z_D$ , and  $Z$  for the damped SEPIC example. Dashed curves:  $Z_N$  and  $Z_D$ . Solid curves:  $Z$

### 16.3.1 Introduction to the $n$ -EET

Given a linear network containing  $n$  inductors and  $m$  capacitors, it is desired to find a transfer function  $G(s) = y(s)/u(s)$ . It is assumed here that this transfer function can be written as a rational fraction referenced to a dc gain, as follows:

$$G(s) = G_{dc} \frac{1 + a_1 s + a_2 s^2 + \dots + a_{n+m} s^{n+m}}{1 + b_1 s + b_2 s^2 + \dots + b_{n+m} s^{n+m}} \quad (16.62)$$



**Fig. 16.26** Effects of R-C damping network on the control-to-output transfer function, SEPIC example. Dashed curves: response of the effective buck-boost model  $G_{vd-bb}$ . Solid curves: response of SEPIC, including correction factor,  $G_{vd}$

Special cases whose transfer functions cannot be written in this manner, such as when  $G(s)$  contains poles or zeroes at the origin, are treated in a later section. The method used here employs a generalization of the Extra Element Theorem, in which all of the inductors and capacitors are treated as “extra” elements, and are added simultaneously. The zeroes of  $G(s)$  are found with the output nulled in the presence of the input, while the poles are found with the input set to zero. The method allows the coefficients  $a_1, a_2, \dots, a_{n+m}, b_1, b_2, \dots, b_{n+m}$  to be found by evaluating the resistances seen looking into the inductor or capacitor ports under various special conditions.

Let us first define the following terminology:

*DC state*: the DC state of an inductor is a short circuit, and the DC state of a capacitor is an open circuit.

*HF state*: the high-frequency (HF) state of an inductor is an open circuit, and the HF state of a capacitor is a short circuit.

In the terminology of the Extra Element Theorem, the “original gain” of the circuit is the reference dc gain  $G_{dc} = G(0)$ , found with all dynamic elements set to their DC states. The transfer function  $s$ -coefficients depend on how the reactive elements change to their HF states, as explained below.

The general form of the coefficient of  $s^k$  has dimensions  $(\text{Hz})^{-k}$ , and is a sum of products of all combinations of terms of the form  $R_x C_i$  and  $L_j / R_y$  which contain the proper dimensions. The  $R_x$  and  $R_y$  terms are found by application of the  $n$ EET, with injection at the terminals of the corresponding reactive element. In the case of denominator coefficients, the input source  $u(s)$  is set to zero. For numerator coefficients, the transfer function output  $y(s)$  is nulled.

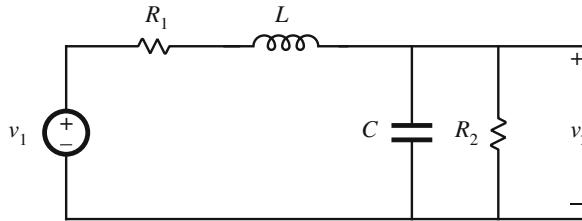


Fig. 16.27  $R$ - $L$ - $C$  circuit example

Consider the low-pass filter circuit of Fig. 16.27. It is desired to compute the transfer function  $G(s) = v_2(s)/v_1(s)$ . This transfer function contains two poles and no zeroes (why?), and can be written in the following form:

$$G(s) = G_{dc} \frac{1}{1 + b_1 s + b_2 s^2} \quad (16.63)$$

The dimensions of  $b_1$  are  $(\text{Hz})^{-1}$ . The two possible terms in  $b_1$  are

$$\frac{L}{R_a} \quad \text{and} \quad R_b C \quad (16.64)$$

The dimensions of  $b_2$  are  $(\text{Hz})^{-2}$ . The only possible term in  $b_2$  is of the form:

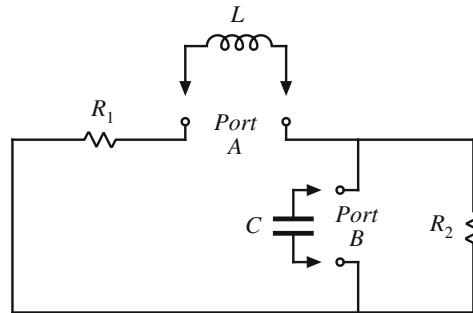
$$\left(\frac{L}{R_c}\right)(R_d C) \quad (16.65)$$

The  $n$ EET shows us how to easily find  $R_a$ ,  $R_b$ ,  $R_c$ , and  $R_d$ .

The dc gain  $G_{dc}$  is found by setting both reactive elements to their DC states, *i.e.*, the inductor is set to a short circuit and the capacitor is set to an open circuit. Under these conditions, the transfer function  $G(s)$  reduces to that of a voltage divider:

$$G_{dc} = \frac{R_2}{R_1 + R_2} \quad (16.66)$$

As with the  $Z_D$  term of the EET, the terms in the denominator polynomial are found with the input source  $v_1$  set to zero. The inductor and capacitor are treated as extra elements, and the circuit of Fig. 16.28 is obtained.



**Fig. 16.28**  $R-L-C$  circuit example: use of the  $n$ EET to find the denominator terms

Since the circuit contains two reactive elements, the denominator is a second-order polynomial that can be written in the following form:

$$\text{denominator} = 1 + s \left( \frac{L}{R_a} + R_b C \right) + s^2 \left( \frac{L}{R_c} R_d C \right) \quad (16.67)$$

The resistance  $R_a$  is the resistance seen at the inductor port (Port A), with the capacitor set to its DC state: Port B is treated as an open circuit. Under these conditions, the resistance between the terminals of Port A is the series combination of  $R_1$  and  $R_2$ :

$$R_a = R_1 + R_2 \quad (16.68)$$

In a similar manner, the resistance  $R_b$  is the resistance seen at the capacitor port (Port B) with the inductor set to its DC state: Port A is treated as a short circuit. Under these conditions, the resistance between the terminals of Port B is the parallel combination of  $R_1$  and  $R_2$ :

$$R_b = R_1 \parallel R_2 \quad (16.69)$$

For the coefficient of  $s^2$ , there are two possible approaches that in principle lead to the same result. We can choose one of the terms (either  $R_c$  or  $R_d$ ) to be the same as the corresponding  $s^1$  term. For example, let us select the term associated with the inductor port,  $R_c$ , to be the same as in the  $s^1$  coefficient:

$$R_c = R_a = R_1 + R_2 \quad (16.70)$$

Then  $R_d$  is the resistance looking into the capacitor port (Port  $B$ ), with the inductor set to its high-frequency state, or open-circuited. With Port  $A$  open-circuited, the resistance between the terminals of Port  $B$  is seen to be

$$R_d = R_2 \quad (16.71)$$

Therefore, the transfer function  $G(s)$  is

$$G(s) = \frac{R_2}{R_1 + R_2} \frac{1}{1 + s\left(\frac{L}{R_1 + R_2} + R_1\|R_2C\right) + s^2\left(LC\frac{R_2}{R_1 + R_2}\right)} \quad (16.72)$$

Thus, the coefficients in the transfer function can be found using some simple rules, without need for algebraic analysis. The reader may wish to verify the result of Eq. (16.72) via conventional analysis, and compare the amount of work required.

### 16.3.2 Procedure for DC-Referenced Functions

As illustrated in the simple example above, the denominator terms are found by setting the input  $u(s)$  to zero, and evaluating the resistance seen at the given port under specific conditions. The numerator terms are found by null double injection in the presence of the input  $u(s)$ , to null the output  $y(s)$ . For a network containing a total of  $p$  independent reactive elements, the numerator and denominator polynomials may contain terms of order up to  $s^p$ . Terms within these polynomials of order  $s^q$  could include some or all combinations of the sums of products of reactive elements taken  $q$  at a time. The numerator and denominator polynomials are of the following form:

$$\begin{aligned} & 1 + s\left(\sum_{i=1}^n \frac{L_i}{R_i} + \sum_{i=1}^m R_i C_i\right) + s^2\left(\sum \sum \frac{L_i L_j}{R_i R_{j-i}} + \sum \sum \frac{L_i}{R_i} C_j R_{j-i} + \sum \sum C_i R_i C_j R_{j-i}\right) \\ & + s^3\left(\sum \sum \sum \frac{L_i L_j L_k}{R_i R_{j-i} R_{k-i}} + \sum \sum \sum \frac{L_i L_j}{R_i R_{j-i}} C_k R_{k-i} + \sum \sum \sum \frac{L_i}{R_i} C_j R_{j-i} C_k R_{k-i}\right. \\ & \left. + \sum \sum \sum C_i R_i C_j R_{j-i} C_k R_{k-i}\right) + s^4 \dots \end{aligned} \quad (16.73)$$

The  $n$ EET tells us how to easily find the resistances  $R_i$ ,  $R_{j-i}$ , etc., in the above polynomial. In Eq. (16.73), the first subscript of each resistance (before the hyphen) denotes the port where the resistance is measured, while any additional subscripts (after the hyphen) denote ports that are set to their high-frequency states during this measurement. The order of these additional subscripts is irrelevant. The coefficients are determined using the following specific conditions:

**Coefficients of  $s^1$ :**  $R_i$  is the resistance seen at port  $i$  with all other ports set to their DC states.

**Coefficients of  $s^2$ :**  $R_i$  is the same term as in the corresponding coefficient of  $s^1$ , i.e., the resistance seen at port  $i$  with all other ports set to their DC states.  $R_{j-i}$  is the resistance seen at port  $j$ , with all other ports *except port  $i$*  set to their DC states. Port  $i$  is set to its HF state.

**Coefficients of  $s^3$ :**  $R_i$  and  $R_{j-i}$  are the same terms appearing in the coefficients of  $s^2$ .  $R_{k-i}$  is the resistance seen at port  $k$ , with all other ports *except ports  $i$  and  $j$*  set to their DC states. Ports  $i$  and  $j$  are set to their HF states.

**Higher-order terms:** the above process continues for higher-order terms. The highest-order term will be measured at one port, with all other ports set to their HF states.

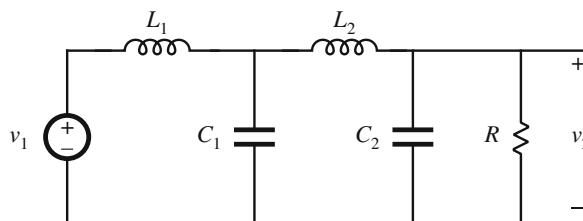
The orders of the terms in the above equation are irrelevant; for example, it can be shown by reciprocity that  $R_{i-j}R_j = R_{j-i}R_i$  (with a similar result for higher-order terms). This implies that it does not matter which reactive element is set to the high-frequency state: either one can be chosen, and the appropriate resistance terms found, leading to a consistent result. Again, each term (*e.g.*,  $R_i$ ) is found by current injection at the connections to the corresponding reactive element (*e.g.*, in place of  $L_1$ ). For denominator terms, the transfer function input is set to zero. For numerator terms, the output is nulled by adjusting the current injection at the port, in the presence of the transfer function input source. For each coefficient, it is necessary to derive only one new term; the other terms are identical to the corresponding terms in a previous lower-order coefficient.

By following the above rules, the transfer function can be written directly, without need for algebraic manipulations. Admittedly, some practice is required to become facile with these rules; nonetheless, the effort required to write exact expressions for complex circuits can be considerably reduced.

## 16.4 *n*-EET Examples

### 16.4.1 Two-Section *L*–*C* Filter

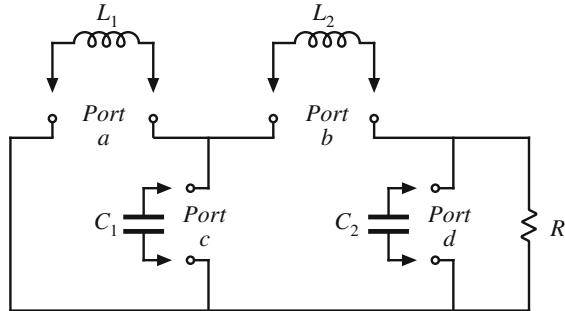
As another example of the *n*EET, consider the two-section *L*–*C* filter of Fig. 16.29. Since this circuit has four reactive elements, we expect the transfer function  $G(s) = v_2(s)/v_1(s)$  to have four poles. We also expect the high-frequency asymptote to have a –80 dB/decade slope: at high frequency each inductor tends to an open circuit and each capacitor tends to a short circuit, with each element leading to reduction of the gain of the path between the input and output of the filter. Hence, we expect that this filter circuit contains no zeroes.



**Fig. 16.29** Two-section *L*–*C* filter example

The DC gain  $G_{dc}$  is found by setting all reactive elements to their dc states; the input is then directly connected to the output, and so  $G_{dc}$  is equal to one. Thus the transfer function is of the form:

$$G(s) = \frac{1}{1 + b_1 s + b_2 s^2 + b_3 s^3 + b_4 s^4} \quad (16.74)$$

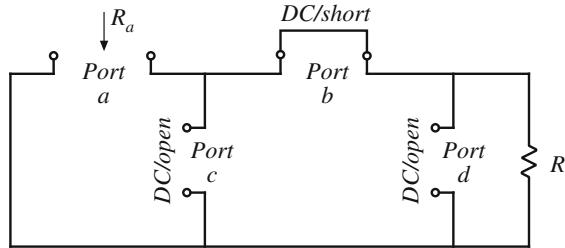


**Fig. 16.30** Two-section  $L$ - $C$  filter example: finding the denominator terms

The denominator polynomial is found when the input  $v_1(s)$  is set to zero. The circuit can then be written as in Fig. 16.30. We now apply the procedure of Sect. 16.3.2 to this circuit, finding the driving-point impedances at the ports with the other ports set to their DC or HF states as required. The results are summarized in Table 16.1.

**Table 16.1** Derivation of Denominator Terms, Two-Section  $L$ - $C$  Filter Example

Term	States of Ports / Reactive Elements				Result
	$L_1$ Port A	$L_2$ Port B	$C_1$ Port C	$C_2$ Port D	
$\frac{sL_1}{R_a}$	Measurement	DC/short	DC/open	DC/open	$R_a = R$
$\frac{sL_2}{R_b}$	DC/short	Measurement	DC/open	DC/open	$R_b = R$
$sC_1R_c$	DC/short	DC/short	Measurement	DC/open	$R_c = 0$
$sC_2R_d$	DC/short	DC/short	DC/open	Measurement	$R_d = 0$
$s^2 \frac{L_1L_2}{R_aR_{b-a}}$	HF/open	Measurement	DC/open	DC/open	$R_{b-a} = \infty$
$s^2 \frac{L_1}{R_a} C_1 R_{c-a}$	HF/open	DC/short	Measurement	DC/open	$R_{c-a} = R$
$s^2 \frac{L_1}{R_a} C_2 R_{d-a}$	HF/open	DC/short	DC/open	Measurement	$R_{d-a} = R$
$s^2 \frac{L_2}{R_b} C_1 R_{c-b}$	DC/short	HF/open	Measurement	DC/open	$R_{c-b} = 0$
$s^2 \frac{L_2}{R_b} C_2 R_{d-b}$	DC/short	HF/open	DC/open	Measurement	$R_{d-b} = R$
$s^2 C_1 R_c C_2 R_{d-c}$	DC/short	DC/short	HF/short	Measurement	$R_{d-c} = 0$
$s^3 \frac{L_1}{R_a} C_1 R_{c-a} \frac{L_2}{R_{b-ac}}$	HF/open	Measurement	HF/short	DC/open	$R_{b-ac} = R$
$s^3 \frac{L_1}{R_a} C_2 R_{d-a} \frac{L_2}{R_{b-ad}}$	HF/open	Measurement	DC/open	HF/short	$R_{b-ad} = \infty$
$s^3 \frac{L_1}{R_a} C_2 R_{d-a} C_1 R_{c-ad}$	HF/open	DC/short	Measurement	HF/short	$R_{c-ad} = 0$
$s^3 \frac{L_2}{R_b} C_2 R_{d-b} C_1 R_{c-bd}$	DC/short	HF/open	Measurement	HF/short	$R_{c-bd} = 0$
$s^4 \frac{L_1}{R_a} C_1 R_{c-a} \frac{L_2}{R_{b-ac}} C_2 R_{d-abc}$	HF/open	HF/open	HF/short	Measurement	$R_{d-abc} = R$

Fig. 16.31 Finding  $R_a$ 

For the denominator term  $sL_1/R_a$ , the coefficient  $R_a$  is the resistance between the Port  $a$  terminals, with the reactive elements of the remaining ports set to their dc states. As illustrated in Fig. 16.31, inductor  $L_2$  at Port  $b$  becomes a short circuit, while capacitors  $C_1$  and  $C_2$  at Ports  $c$  and  $d$  become open circuits. It can be seen that  $R_a$  is equal to  $R$ . The remaining  $s^1$  terms of Table 16.1 are left to the reader to verify.

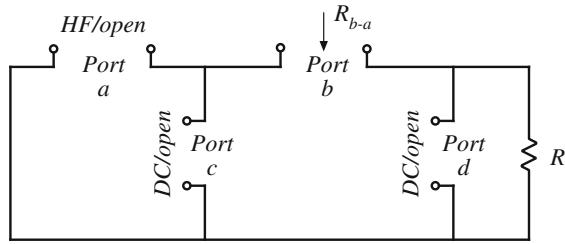
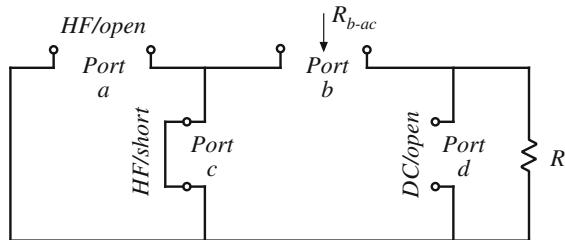
Fig. 16.32 Finding  $R_{b-a}$ 

Figure 16.32 illustrates determination of  $R_{b-a}$ , as needed in the denominator term

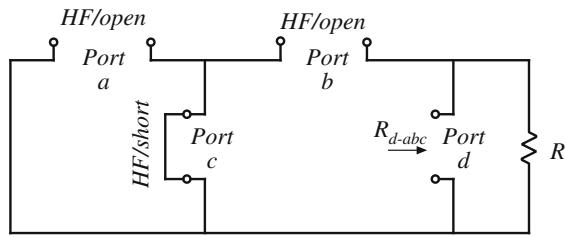
$$s^2 \left( \frac{L_1}{R_a} \right) \left( \frac{L_2}{R_{b-a}} \right) \quad (16.75)$$

The  $R_a$  term coincides with the result derived in the previous paragraph. The term  $R_{b-a}$  is the resistance between the Port  $b$  terminals, with the element  $L_1$  at Port  $a$  set to its high-frequency state (an open circuit). The remaining reactive elements  $C_1$  and  $C_2$  are set to their dc states (open circuits). It can be seen that Port  $b$  becomes an open circuit under these conditions, and hence  $R_{b-a} = \infty$ . In consequence, the denominator  $s^2$  term of Eq. (16.75) is equal to zero. The remaining  $s^2$  terms of Table 16.1 are left to the reader to verify.

Let us consider next the denominator term  $s^3 L_1 L_2 C_1 / R_x$ . One way to approach solution for this term is to apply the result of the previous paragraph to express this term as  $s^3 (L_1/R_a)(L_2/R_{b-a})(C_1 R_{c-ab})$ . However, since the result of the previous paragraph was  $R_{b-a} = \infty$ , such an approach will lead to an indeterminate result with  $R_{c-ab} = \infty$  (try it!). Instead, we should base our approach on an  $s^2$  term that is nonzero. By examination of Table 16.1, one can see that the term  $s^2 (L_1/R_a)(C_1 R_{c-a})$  is nonzero. Therefore, let us determine  $R_{b-ac}$ , as needed to express this denominator term as  $s^3 (L_1/R_a)(C_1 R_{c-a})(L_2/R_{b-ac})$ . As illustrated in Fig. 16.33, the quantity  $R_{b-ac}$  is equal to the resistance between the Port  $b$  terminals when  $L_1$  and  $C_1$  are set to their high-frequency states, and  $C_2$  remains in its dc state. It can be seen that  $R_{b-ac} = R$ . The remaining  $s^3$  terms of Table 16.1 are also left to the reader to verify.

**Fig. 16.33** Finding  $R_{b-ac}$ 

There is a single  $s^4$  term. To find this term, we should begin with a nonzero  $s^3$  term. The result of the previous paragraph is such a term. Hence, let us express the  $s^4$  term in the form  $s^4(L_1/R_a)(C_1R_{c-a})(L_2/R_{b-ac})(C_2R_{d-abc})$ . As illustrated in Fig. 16.34, the quantity  $R_{d-abc}$  is the resistance between the Port  $d$  terminals when the elements at Ports  $a$ ,  $b$ , and  $c$  are set to their high-frequency states. By examination of Fig. 16.34, it can be seen that  $R_{d-abc} = R$ .

**Fig. 16.34** Finding  $R_{d-abc}$ 

The results of Table 16.1 predict that the denominator polynomial is

$$\begin{aligned} \text{denominator} = & 1 + s \left( \frac{L_1}{R} + \frac{L_2}{R} + C_1 \cdot 0 + C_2 \cdot 0 \right) + \\ & s^2 \left( \frac{L_1}{R} \frac{L_2}{\infty} + \frac{L_1}{R} C_1 R + \frac{L_1}{R} C_2 R + \frac{L_2}{R} C_1 \cdot 0 + \frac{L_2}{R} C_2 R + C_1 \cdot 0 C_2 \cdot 0 \right) + \\ & s^3 \left( \frac{L_1}{R} C_1 R \frac{L_2}{R} + \frac{L_1}{R} \frac{L_2}{\infty} C_2 R + \frac{L_1}{R} C_2 R C_1 \cdot 0 + \frac{L_2}{R} C_2 R C_1 \cdot 0 \right) + \\ & s^4 \left( \frac{L_1}{R} \frac{L_2}{R} C_1 R C_2 R \right) \end{aligned} \quad (16.76)$$

Upon elimination of terms that evaluate to zero, the transfer function  $G(s)$  can then be written as:

$$G(s) = \frac{1}{1 + s \left( \frac{L_1 + L_2}{R} \right) + s^2 \left( L_1 (C_1 + C_2) + L_2 C_2 \right) + s^3 \left( \frac{L_1 L_2 C_1}{R} \right) + s^4 \left( L_1 L_2 C_1 C_2 \right)} \quad (16.77)$$

Thus, the coefficients in the transfer function of this somewhat complex fourth-order filter circuit are found through a sequence of simple circuit evaluations. With practice, one can perform these evaluations quickly using the schematic of Fig. 16.30. Additionally, terms derived in other ways can be checked using this approach. The *n*EET approach is particularly advantageous when circuit contains multiple resistors and more complex interconnections.

It should also be noted that, if we had not had the insight that  $G(s)$  contains no zeroes, we could have employed the procedure of Sect. 16.3.2 to compute the numerator polynomial. We would have found that the numerator terms of order  $s^1$  to  $s^4$  are zero.

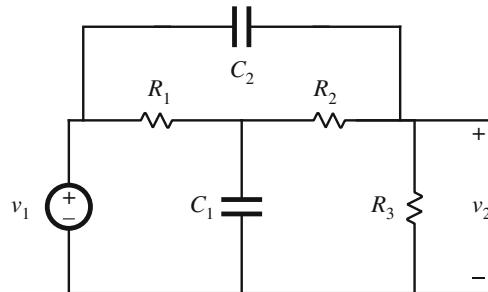
### 16.4.2 Bridge-T Filter Example

As a third example, consider the Bridge-T filter circuit of Fig. 16.35. Conventional analysis of the transfer function  $G(s) = v_2(s)/v_1(s)$  for this circuit is somewhat onerous because of element  $C_2$ . Let us derive this transfer function using the nEET.

Since there are two reactive elements, we expect  $G(s)$  to contain two poles. Additionally, we expect the high-frequency asymptote of  $G(s)$  to be equal to one because capacitor  $C_2$  tends to zero impedance at high frequency, shorting the output to the input. Therefore  $G(s)$  must contain two zeroes, so that its high-frequency magnitude asymptote has a slope of 0 dB/decade. Hence the transfer function is of the form

$$G(s) = G_{dc} \frac{1 + a_1 s + a_2 s^2}{1 + b_1 s + b_2 s^2} \quad (16.78)$$

Analysis requires application of the procedure of Sect. 16.3.2 twice. First, null double injection is employed to find the numerator polynomial under the conditions that the output  $v_2$  is nulled. A subscript  $N$  is appended to the resistance names, to distinguish these numerator terms from



**Fig. 16.35** Bridge-T filter example

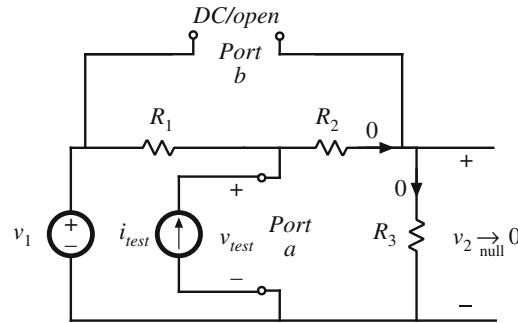
the similarly named denominator terms. Second the procedure of Sect. 16.3.2 is applied under the conditions that the input  $v_1$  is set to zero, to find the denominator polynomial. A subscript  $D$  is appended to the names of the denominator resistance terms.

First consider determination of the zeroes of  $G(s)$ . The numerator polynomial can be expressed in the form:

$$\text{numerator} = 1 + s(C_1 R_{Na} + C_2 R_{Nb}) + s^2 C_1 R_{Na-b} C_2 R_{Nb} \quad (16.79)$$

Here, capacitor  $C_1$  is connected at Port  $a$  and capacitor  $C_2$  is connected at Port  $b$ .

Figure 16.36 illustrates the determination of  $R_{Na}$ . Capacitor  $C_2$  is set to its dc state (open circuit at Port  $b$ ). In the presence of the input source  $v_1$ , a current source  $i_{test}$  is applied at Port  $a$ , and the two sources are adjusted to null the output  $v_2$ . One follows this null condition towards



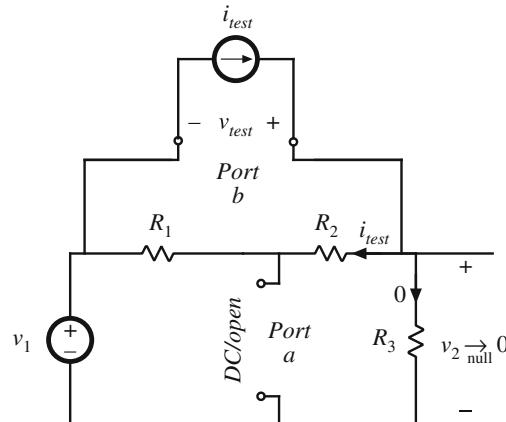
**Fig. 16.36** Determination of numerator  $R_{Na}$

the injection point to find the Port *a* voltage  $v_{test}$ . With the output voltage nulled, the current through resistor  $R_3$  is also nulled. Since there is no current through the open-circuited Port *b*, the current through resistor  $R_2$  must also be nulled. By Ohm's law, the voltage across  $R_2$  is zero, and hence the voltage  $v_{test}$  is zero. Therefore, the numerator  $R_{Na}$  is

$$R_{Na} = \left. \frac{v_{test}}{i_{test}} \right|_{v_2 \rightarrow 0} = 0 \quad (16.80)$$

The quantity  $R_{Nb}$  is found in a similar manner. In the presence of the input  $v_1$ , current injection is applied at the  $C_2$  port (Port *b*) and adjusted to null the output  $v_2$ . Capacitor  $C_1$  is set to its dc state, and hence Port *a* becomes an open circuit. This measurement is illustrated in Fig. 16.37. Since the current through resistor  $R_3$  is nulled to zero, the current  $i_{test}$  must flow through resistors  $R_2$  and  $R_1$ . Therefore the voltage  $v_{test}$  is equal to  $i_{test}(R_1 + R_2)$ , and the numerator  $R_{Nb}$  is given by:

$$R_{Nb} = \left. \frac{v_{test}}{i_{test}} \right|_{v_2 \rightarrow 0} = R_1 + R_2 \quad (16.81)$$



**Fig. 16.37** Determination of numerator  $R_{Nb}$

To find  $R_{Na-b}$ , the current  $i_{test}$  is injected at Port *a*, and capacitor  $C_2$  is set to its high-frequency state (Port *b* is shorted). The independent sources  $v_1$  and  $i_{test}$  are adjusted to null

the output  $v_2$ . This experiment is illustrated in Fig. 16.38. For this particular circuit, the shorting of Port  $b$  causes the output  $v_2$  to be equal to the input  $v_1$ , and hence the output null condition cannot be achieved unless the input voltage source  $v_1$  is zero. Under this condition, the current  $i_{test}$  flows through the parallel combination of  $R_1$  and  $R_2$ , and hence  $v_{test}$  is equal to  $i_{test}R_1\parallel R_2$ . The numerator  $R_{Na-b}$  is given by

$$R_{Na-b} = \left. \frac{v_{test}}{i_{test}} \right|_{v_2 \rightarrow 0} = R_1 \parallel R_2 \quad (16.82)$$

Upon insertion of Eqs. (16.80)–(16.82) into Eq. (16.79), one finds that the numerator polynomial is given by

$$\text{numerator} = 1 + sC_2(R_1 + R_2) + s^2C_1C_2R_1R_2 \quad (16.83)$$

Next consider determination of the poles of  $G(s)$ . The denominator polynomial can be expressed in the form:

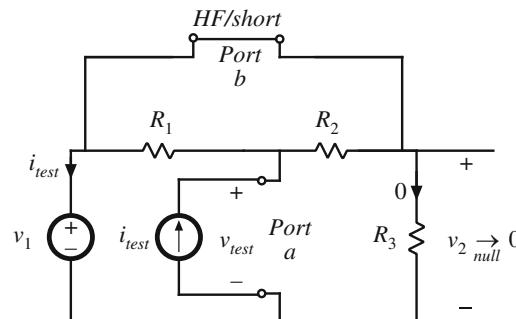
$$\text{denominator} = 1 + s(C_1R_{Da} + C_2R_{Db}) + s^2C_1R_{Da-b}C_2R_{Db} \quad (16.84)$$

The driving-point resistances  $R_{Da}$ ,  $R_{Db}$ , and  $R_{Da-b}$  are found with the input source  $v_1$  set to zero.

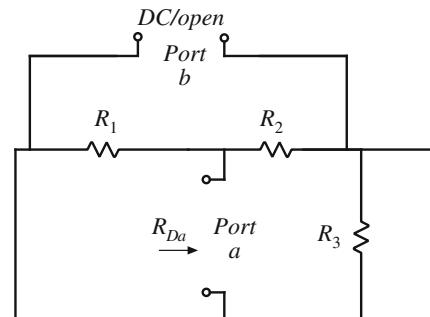
Figure 16.39 illustrates the determination of  $R_{Da}$ . Capacitor  $C_2$  is set to its dc state (open circuit at Port  $b$ ), and the input source  $v_1$  is set to zero (short circuit). The resistance between the Port  $a$  terminals is found, with the result

$$R_{Da} = R_1 \parallel (R_2 + R_3) \quad (16.85)$$

**Fig. 16.38** Determination of numerator  $R_{Na-b}$



**Fig. 16.39** Determination of denominator  $R_{Da}$

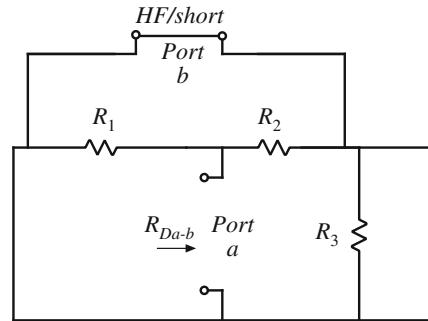


The quantity  $R_{Db}$  is found in a similar manner: it is the resistance between the Port (b) terminals with capacitor  $C_1$  set to its dc state (open circuit at Port  $a$ ) and with the input source  $v_1$  set to zero. The result is

$$R_{Db} = R_3 \parallel (R_1 + R_2) \quad (16.86)$$

Figure 16.40 illustrates the determination of  $R_{Da-b}$ . Capacitor  $C_2$  is set to its high-frequency state (short circuit at Port  $b$ ), and the input source  $v_1$  is set to zero (short circuit). The resistance between the Port  $a$  terminals is found, with the result

$$R_{Da-b} = R_1 \parallel R_2 \quad (16.87)$$



**Fig. 16.40** Determination of denominator  $R_{Da-b}$

Hence, the denominator polynomial is

$$\begin{aligned} \text{denominator} &= 1 + s \left[ C_1 \left( R_1 \parallel (R_2 + R_3) \right) + C_2 \left( R_3 \parallel (R_1 + R_2) \right) \right] + \\ &\quad s^2 \left[ C_1 C_2 \left( R_1 \parallel (R_2 + R_3) \right) \left( R_1 \parallel R_2 \right) \right] \end{aligned} \quad (16.88)$$

Finally, the dc gain  $G_{dc}$  is found by setting all reactive elements to their dc states, and then solving for the transfer function. The result is found using the voltage divider formula to obtain

$$G_{dc} = \frac{R_3}{R_1 + R_2 + R_3} \quad (16.89)$$

The complete transfer function is obtained by substitution of Eqs. (16.83), (16.88), and (16.89) into Eq. (16.78).

## 16.5 Frequency Inversion

Sometimes, the dc gain of a transfer function or other function of interest is zero or infinite; this occurs when there are poles or zeroes at the origin of the complex plane. In the power electronics field, this is nearly always the case for impedances because we do not want the dc or low-frequency ac current to flow through a lossy resistive element. This also often occurs in compensator transfer functions, where PI or PID compensators are employed.

### 16.5.1 Example: Damped Input Filter

For example, consider the output impedance  $Z(s)$  of the damped input filter circuit illustrated in Fig. 16.41. To measure this output impedance, we would set the independent source  $\hat{v}_g$  to zero, then inject a current  $\hat{i}$  and measure the induced voltage  $\hat{v}$  as shown in Fig. 16.42. The output impedance is then given by

$$Z(s) = \left. \frac{\hat{v}}{\hat{i}} \right|_{\hat{v}_g=0} \quad (16.90)$$

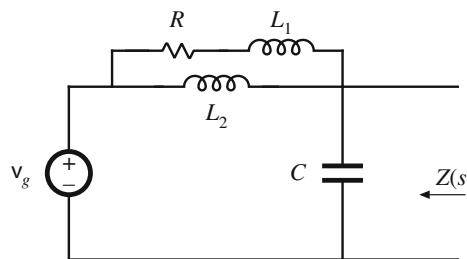
So we can view  $Z(s)$  as the transfer function from  $\hat{i}$  to  $\hat{v}$ . If we attempt to use the  $n$ -Extra Element Theorem in its basic form to express  $Z(s)$ , we find that the dc value of  $Z(s)$  is zero, so that

$$Z(s) = 0 \cdot \frac{\text{numerator polynomial}}{\text{denominator polynomial}} \quad (16.91)$$

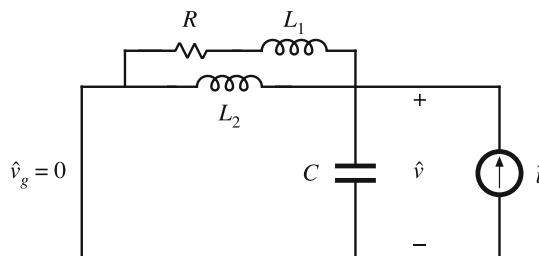
Because the reference gain is zero, this approach does not work.

Figure 16.43 illustrates graphical construction of the output impedance asymptotes, using the approach of Sect. 8.3, for some assumed element values with  $L_1 \gg L_2$ . It appears that  $Z(s)$  could be expressed with reference to the midband asymptote  $R$ , using an inverted pole at  $R/L_2$ , plus a zero at  $R/L_1$  and complex poles at  $\omega_0 = 1/\sqrt{L_1 C}$ :

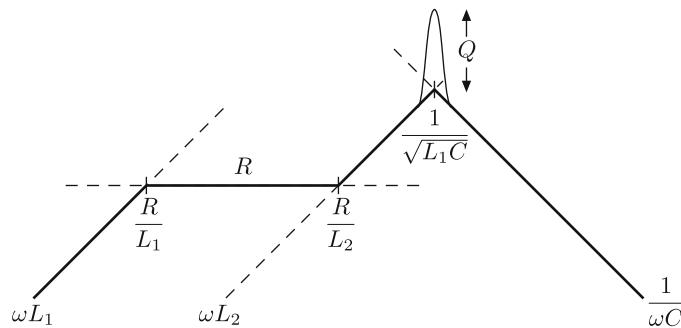
$$Z(s) \approx R \frac{\left(1 + \frac{sL_1}{R}\right)}{\left(1 + \frac{R}{sL_2}\right)\left(1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)} \quad (16.92)$$



**Fig. 16.41** A damped LC filter



**Fig. 16.42** Measurement of the output impedance  $Z(s)$  of the LC filter of Fig. 16.41



**Fig. 16.43** Graphical construction of typical output impedance asymptotes of the LC filter of Fig. 16.41

This suggests that, to find the exact expression for  $Z(s)$ , we could employ frequency inversion to express  $Z(s)$  with respect to the reference gain  $R$ .

This can be achieved with a generalization of the *nEET* to handle frequency inversion. First, we must extend the notion of the “DC state” and “HF state” of a reactive element, to the following:

*Reference state*: the reference state of a reactive element is the state (short circuit or open circuit) that causes the transfer function to be equal to the reference gain.

*Inverse state*: the inverse state of a reactive element is the opposite (open circuit or short circuit) of its reference state.

For the example of Fig. 16.42,  $Z(s)$  is equal to  $R$  when  $L_1$  is short-circuited,  $L_2$  is open-circuited, and  $C$  is open-circuited. Hence we define these as the reference states of these elements, as summarized in Table 16.2.

**Table 16.2** Reference and Inverse States of Reactive Elements, Damped  $L-C$  Filter Example

Element	Reference State	Inverse State
$L_1$	Short	Open
$L_2$	Open	Short
$C$	Open	Short

The reference states of elements  $L_1$  and  $C$  coincide with their DC states, while the reference state of  $L_2$  coincides with its HF state. We therefore treat  $L_2$  using frequency-inverted terms: where we previously employed a term of the form

$$\frac{sL_2}{R_a} \quad (16.93)$$

we now use the inverted form

$$\frac{R_a}{sL_2} \quad (16.94)$$

If the reference state of capacitor  $C$  had been its high-frequency state, then we would have replaced terms of the form

$$sCR_a \quad (16.95)$$

with the inverted form

$$\frac{1}{sCR_a} \quad (16.96)$$

We now generalize the procedure of Sect. 16.3.2, replacing DC and HF port states with reference and inverse states. The notation  $R_{N1-2}$ ,  $R_{D3-12}$ , etc., now has the meaning that additional subscripts after the hyphen denote ports that are set to their inverse states during measurement, while other ports are set to their reference states. Hence  $Z(s)$  will be expressed in the form

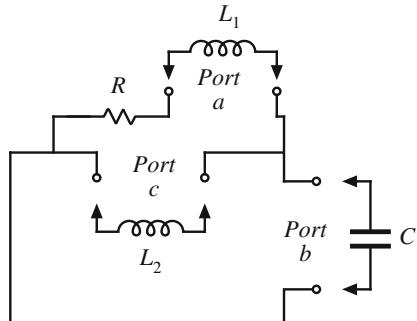
$$Z(s) = R \frac{\text{numerator}}{\text{denominator}} \quad (16.97)$$

The denominator may contain products having one, two, or all three reactive elements. For the output impedance example, we obtain:

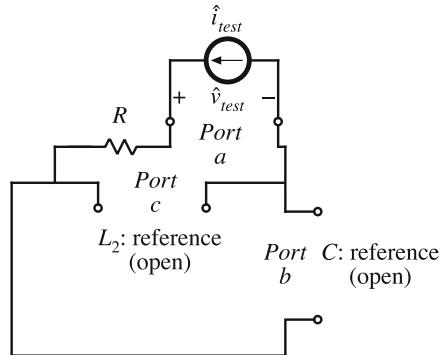
$$\begin{aligned} \text{denominator} &= 1 + \left( \frac{sL_1}{R_{Da}} + sCR_{Db} + \frac{R_{Dc}}{sL_2} \right) \\ &+ \left( sCR_{Db} \frac{sL_1}{R_{Da-b}} + sCR_{Db} \frac{R_{Dc-b}}{sL_2} + \frac{R_{Dc}}{sL_2} \frac{sL_1}{R_{Da-c}} \right) \\ &+ \left( sCR_{Db} \frac{sL_1}{R_{Da-b}} \frac{R_{Dc-ab}}{sL_2} \right) \end{aligned} \quad (16.98)$$

Through the reciprocity relationship  $R_{Di-j}R_{Dj} = R_{Dj-i}R_{Di}$ , it is possible to express the denominator in more than one way, as in earlier examples.

**Fig. 16.44** Damped  $L-C$  filter example of Fig. 16.41: finding the output impedance denominator terms. The independent sources  $\hat{v}_g$  and  $\hat{i}$  are set to zero



We now find the coefficients  $R_{Da}$  through  $R_{Dc-ab}$  in the usual way, except that “DC state” is replaced with “reference state,” and “HF state” is replaced with “inverse state.” The denominator coefficients are found with the independent sources set to zero:  $\hat{v}_g = 0$  and  $\hat{i} = 0$ , as illustrated in Fig. 16.44.



**Fig. 16.45** Damped  $L-C$  filter example of Fig. 16.41: finding  $R_{Da}$ . The resistance seen at Port a is found with the reactive elements at Ports b and c set to their reference states

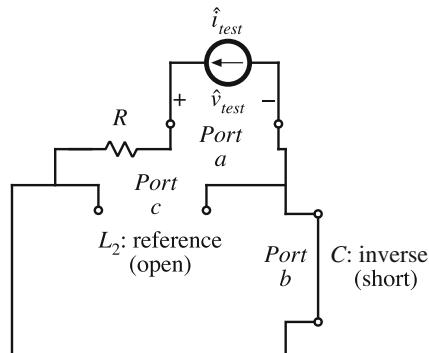
The coefficient  $R_{Da}$  is the resistance seen at the  $L_1$  port (Port a) when Port b ( $C$ ) is set to its reference (DC/open) state, and Port c ( $L_2$ ) is set to its reference (HF/open) state. From examination of Fig. 16.45 with these conditions, it can be seen that  $R_{Da} = \infty$  (open circuit).

The coefficient  $R_{Da-b}$  is the resistance seen at the  $L_1$  port (Port a) when Port b ( $C$ ) is set to its inverse (DC/open) state, and Port c ( $L_2$ ) is set to its reference (HF/open) state. From examination of Fig. 16.46 with these conditions, it can be seen that  $R_{Da-b} = R$ .

The port states and results for the seven denominator terms are listed in Table 16.3. Derivation of the remaining terms of Table 16.3 is left for the reader. The resulting denominator is

$$\text{denominator} = 1 + sCR + \frac{R}{sL_2} + sCR\frac{sL_1}{R} + \frac{R}{sL_2}\frac{sL_1}{R} \quad (16.99)$$

We will further simplify the denominator after the numerator has been found.



**Fig. 16.46** Damped  $L-C$  filter example of Fig. 16.41: finding  $R_{Da-b}$ . The resistance seen at Port a is found with the reactive element at Port b set to its inverse state (short) and Port c set to its reference state

**Table 16.3** Derivation of Denominator Terms, Damped L-C Filter Example

Term	States of Ports / Reactive Elements			Result
	$L_1$ Port a	$C$ Port b	$L_2$ Port c	
$\frac{sL_1}{R_{Da}}$	Measurement	Reference/open	Reference/open	$R_{Da} = \infty$
$sCR_{Db}$	Reference/short	Measurement	Reference/open	$R_{Db} = R$
$\frac{R_{Dc}}{sL_2}$	Reference/short	Reference/open	Measurement	$R_{Dc} = R$
$sCR_{Db} \frac{sL_1}{R_{Da-b}}$	Measurement	Inverse/short	Reference/open	$R_{Da-b} = R$
$sCR_{Db} \frac{R_{Dc-b}}{sL_2}$	Reference/short	Inverse/short	Measurement	$R_{Dc-b} = 0$
$\frac{R_{Dc}}{sL_2} \frac{sL_1}{R_{Da-c}}$	Measurement	Reference/open	Inverse/short	$R_{Da-c} = R$
$sCR_{Db} \frac{sL_1}{R_{Da-b}} \frac{R_{Dc-ab}}{sL_2}$	Inverse/open	Inverse/short	Measurement	$R_{Dc-ab} = 0$

The numerator may also contain products having one, two, or all three reactive elements. For the output impedance example, we obtain:

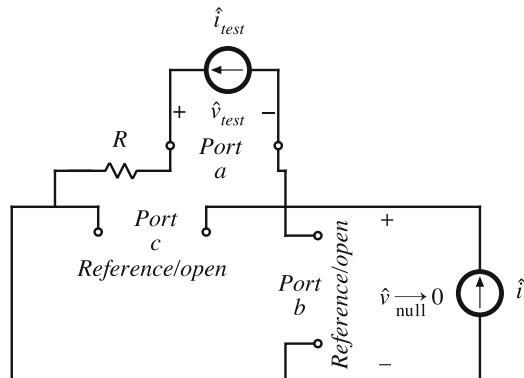
$$\begin{aligned} \text{numerator} = & 1 + \left( \frac{sL_1}{R_{Na}} + sCR_{Nb} + \frac{R_{Nc}}{sL_2} \right) \\ & + \left( \frac{sL_1}{R_{Na}} sCR_{Nb-a} + \frac{sL_1}{R_{Na}} \frac{R_{Nc-a}}{sL_2} + \frac{R_{Nc}}{sL_2} sCR_{Nb-c} \right) \\ & + \left( \frac{sL_1}{R_{Na}} \frac{R_{Nc-a}}{sL_2} sCR_{Nb-ac} \right) \end{aligned} \quad (16.100)$$

As usual, the numerator terms are found in the presence of  $\hat{i}$ , with the transfer function output ( $\hat{v}$ ) nulled to zero. Since in this example the output voltage coincides with the capacitor (Port b) voltage, we expect the capacitor terms to be zero.

We again employ the generalized definitions of reference and inverse states. In the presence of  $\hat{i}$ , we inject at the  $L_1$ ,  $C$ , or  $L_2$  port, and adjust the injection such that  $\hat{v}$  is nulled. The coefficients are the resistances seen at the injection ports under these conditions.

For example, to find  $R_{Na}$ , we inject a current at the  $L_1$  port (Port a), with  $C$  (Port b) set to its reference state (open) and  $L_2$  set to its reference state (open). The injection current is adjusted in the presence of the current  $\hat{i}$  to null  $\hat{v}$ , as illustrated in Fig. 16.47. With  $\hat{v}$  nulled to zero, it can be seen that  $\hat{v}_{test} = \hat{i}_{test} R$ , and hence  $R_{Na} = R$ .

From examination of Fig. 16.47, it can be seen that nulling the output voltage  $\hat{v}$  causes the voltages across ports  $b$  and  $c$  to be zero. Consequently, numerator terms associated with these ports are zero, and the only nonzero numerator term is  $R_{Na}$ . Determination of the numerator terms is summarized in Table 16.4.



**Fig. 16.47** Determination of numerator term  $R_{Na}$

**Table 16.4** Derivation of Numerator Terms, Damped L-C Filter Example

Term	States of Ports / Reactive Elements			Result
	$L_1$ Port a	$C$ Port b	$L_2$ Port c	
$\frac{sL_1}{R_{Na}}$	Measurement	Reference/open	Reference/open	$R_{Na} = R$
$sCR_{Nb}$	Reference/short	Measurement	Reference/open	$R_{Nb} = 0$
$\frac{R_{Nc}}{sL_2}$	Reference/short	Reference/open	Measurement	$R_{Nc} = 0$
$\frac{sL_1}{R_{Na}} sCR_{Nb-a}$	Inverse/open	Measurement	Reference/open	$R_{Nb-a} = 0$
$\frac{R_{Nc}}{sL_1} \frac{R_{Nc-a}}{sL_2}$	Inverse/open	Reference/open	Measurement	$R_{Nc-a} = 0$
$\frac{sL_2}{R_{Na}} sCR_{Nb-c}$	Reference/short	Measurement	Inverse/short	$R_{Nb-c} = 0$
$\frac{sL_2}{R_{Na}} \frac{R_{Nc-a}}{sL_2} sCR_{Nb-ac}$	Inverse/open	Measurement	Inverse/short	$R_{Nb-ac} = 0$

The resulting expression for the output impedance is

$$Z(s) = R \frac{1 + \frac{sL_1}{R}}{1 + sRC + \frac{R}{sL_2} + s^2 L_1 C + \frac{sL_1}{sL_2}} \quad (16.101)$$

If desired, we can eliminate the inverted terms by multiplying the numerator and denominator by the factor  $sL_2/R$  to obtain

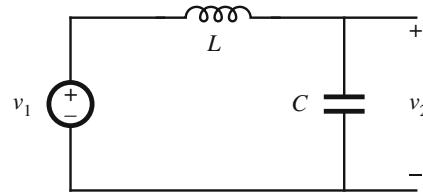
$$Z(s) = sL_2 \frac{1 + \frac{sL_1}{R}}{1 + \frac{s(L_1 + L_2)}{R} + s^2 L_2 C + \frac{s^3 L_1 L_2 C}{R}} \quad (16.102)$$

In summary, the nEET allows us to write the transfer functions of quite complex systems with a minimum of algebraic manipulations. Inverted forms can also be handled by definition of

a reference gain that occurs when the reactive elements are set to reference states. This allows us to solve the case where there are poles or zeroes at the origin.

### 16.5.2 Other Special Cases

It sometimes happens in application of the  $n$ -EET that all terms for an intermediate power of  $s$  are zero. This happens in circuits having undamped resonances. When we compute the higher-order terms, we then obtain  $(0 \cdot \infty)$  for all terms.

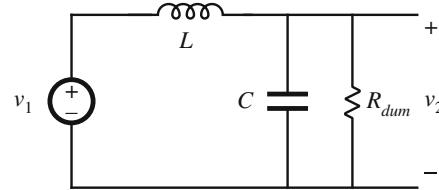


**Fig. 16.48** Undamped  $L$ - $C$  filter example

An example is the undamped  $L$ - $C$  filter illustrated in Fig. 16.48. The transfer function of this circuit is

$$G(s) = \frac{v_2}{v_1} = \frac{1}{1 + s^2 LC} \quad (16.103)$$

The  $n$ -EET encounters problems with this example because the coefficient of  $s^1$  in the denominator is zero. Hence we are unable to compute the coefficient of  $s^2$ : we obtain  $(0 \cdot \infty)$ .



**Fig. 16.49** Addition of dummy resistor  $R_{dum}$  to the undamped  $L$ - $C$  filter example

A solution is to insert a dummy resistor  $R_{dum}$  into the circuit as in Fig. 16.49; this adds a nonzero damping term. We can then proceed with the  $n$ -EET analysis as usual, to obtain the transfer function

$$G(s) = \frac{1}{1 + s \left( \frac{L}{R_{dum}} + C \cdot 0 \right) + s^2 \frac{L}{R} CR} \quad (16.104)$$

$$= \frac{1}{1 + s \frac{L}{R_{dum}} + s^2 LC} \quad (16.105)$$

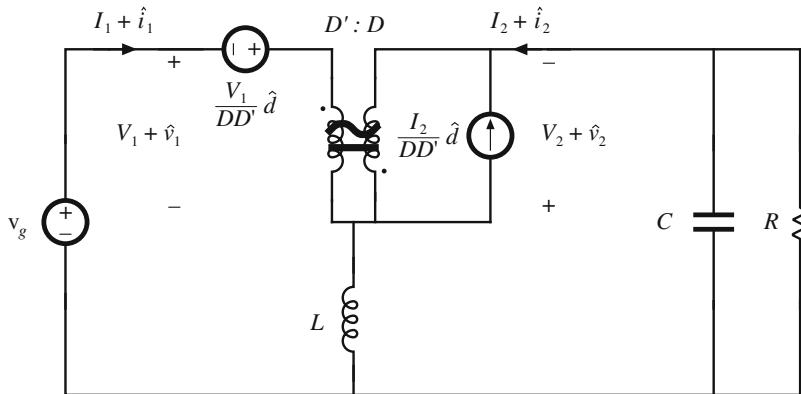
The original circuit is obtained when we let  $R_{dum} \rightarrow \infty$ . The transfer function then becomes

$$G(s) = \frac{1}{1 + s^2 LC} \quad (16.106)$$

The technique of adding dummy resistors to the circuit can allow the  $n$ -EET to be employed when degenerate cases arise.

## PROBLEMS

**16.1 Analysis of the buck-boost converter control-to-output transfer function  $G_{vd}(s)$  using the Extra Element Theorem.** Averaged switch modeling of the buck-boost converter leads to the continuous conduction mode small-signal ac model illustrated in Fig. 16.50. One approach to solving for  $G_{vd}(s)$  in this circuit is to employ the Extra Element Theorem, treating inductor  $L$  as the extra element. No credit will be given for other methods.



**Fig. 16.50** Small-signal ac model for the CCM buck-boost converter of Problem 16.1, derived by average switch modeling

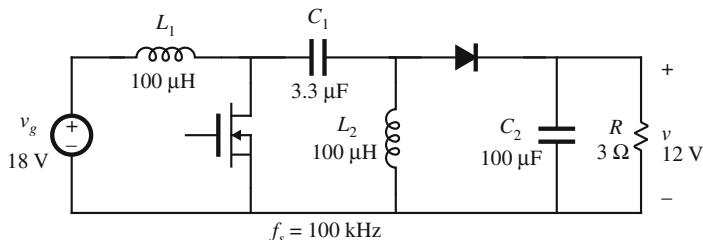
- (a) Let  $L \rightarrow$  short circuit, and determine the “original transfer function”  $G_{d0}$ .
- (b) Determine  $Z_N(s)$  and  $Z_D(s)$ , and hence derive the expression for  $G_{vd}(s)$ . Express your result in standard normalized form.

**16.2 Analysis and design of a CCM SEPIC.** A dc–dc SEPIC, along with nominal element values, is illustrated in Fig. 16.50. The object of this problem is to employ the Extra Element Theorem as discussed in Sect. 16.2.3 to gain insight into the physical origins of the salient features of the control-to-output transfer function  $G_{vd}(s)$ , and to improve its behavior by addition of a damping network. It is expected that your work will follow the analysis of Sect. 16.2.3; no credit will be given for other approaches.

- (a) Sketch the small-signal averaged switch model for this converter. Evaluate the numerical values of the quiescent conditions in your model (i.e., the steady-state duty cycle  $D$  and the switch model quantities  $I_1$ ,  $I_2$ ,  $V_1$ , and  $V_2$ ).
- (b) Using the simple approximation  $C_1 \rightarrow$  open circuit, determine the approximate control-to-output transfer function

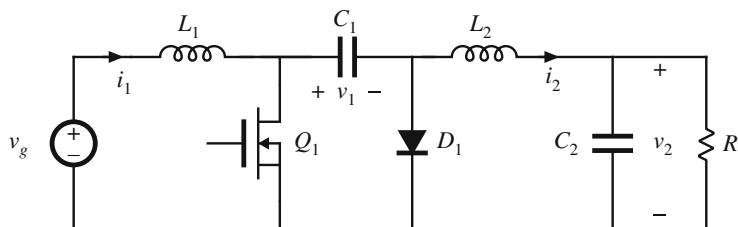
$$G_{vd-bb}(s) = \left. \frac{\hat{v}(s)}{\hat{d}(s)} \right|_{C_1 \rightarrow 0}$$

Construct the Bode plot of the magnitude and phase of this transfer function on semi-log axes, and label salient features (corner frequencies,  $Q$ -factors, dc gain) as appropriate.

**Fig. 16.51** CCM SEPIC of Problem 16.2

- (c) Construct the Bode plots of  $\|Z_N\|$  and  $\|Z_D\|$ , using semi-log axes, and label the numerical values of the salient features. Overlay the capacitor  $C_1$  impedance. Hence, estimate the frequencies of the resonant poles and zeroes in  $G_{vd}(s)$  induced by the internal resonance. Verify your analysis by simulation, using an averaged model to plot the Bode plot of the exact  $G_{vd}(s)$ .
- (d) Add an  $R_b-C_b$  damping network as discussed in Sect. 16.2.4, as follows. Choose  $C_b = 10C_1$ . Select  $R_b$  such that the resonant poles and zeroes are approximately centered on the  $R_b$  asymptote of the impedance  $Z(s)$  of Eq. (16.61). Overlay the  $\|Z(s)\|$  asymptotes on your Bode plots of  $\|Z_N\|$  and  $\|Z_D\|$ . Again use averaged simulation to plot the exact magnitude and phase of the damped  $G_{vd}(s)$ , and verify that the internal resonance is adequately damped.

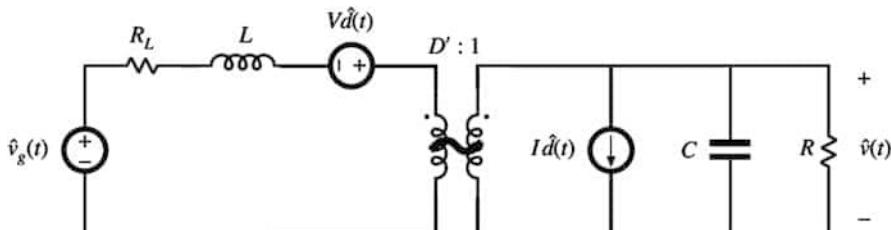
**16.3 Analysis of a CCM Ćuk Converter.** A Ćuk converter is illustrated in Fig. 16.52. The objective of this problem is to employ the Extra Element Theorem to derive an expression for the line-to-output transfer function  $G_{vg}(s)$ , with an approach that is similar to that employed in the SEPIC example of Sect. 16.2.3. Like the SEPIC, the Ćuk converter can be viewed as an effective buck-boost converter plus correction factor terms that account for an additional internal resonance.

**Fig. 16.52** Ćuk converter circuit of Problem 16.3

- (a) Construct the average switch model for this converter operating in continuous conduction mode.
- (b) If we let  $C_1 \rightarrow 0$  (open circuit) in the small-signal model, then an effective buck-boost converter is obtained. Sketch the small-signal model for this case, and find its line-to-output transfer function  $G_{vg-bb}(s)$ .

- (c) Apply the Extra Element Theorem to find  $Z_N(s)$  and  $Z_D(s)$  in the correction factor of the line-to-output transfer function.  
 (d) For some values, plot  $G_{vg}$ .

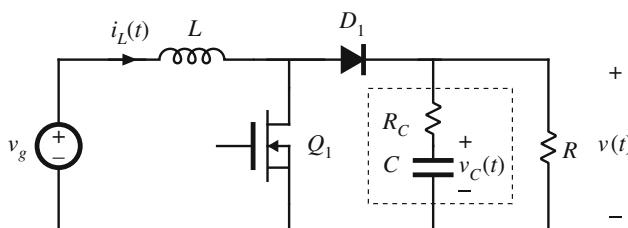
**16.4** Figure 16.53 contains a small-signal model of a boost converter that includes inductor resistance  $R_L$ .



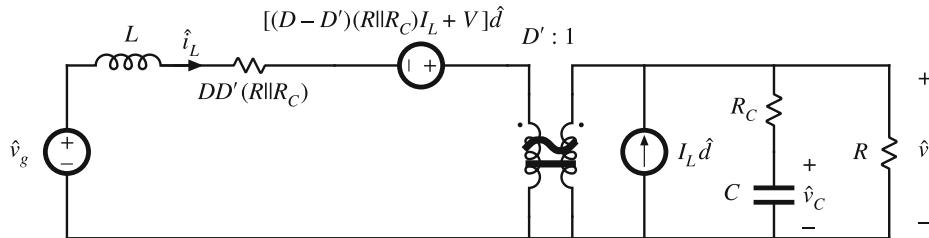
**Fig. 16.53** Large-signal dc and small-signal ac model of the CCM boost converter of Problem 16.4

- (a) Use the  $n$ -Extra Element Theorem to derive an expression for the control-to-output transfer function  $G_{vd}(s)$  predicted by this circuit model. No credit will be given for other methods.  
 (b) Can the inductor resistance  $R_L$  be used to move the right half-plane zero into the left half-plane? Explain. What is the resulting effect on the converter efficiency? Compare the resulting loss in  $R_L$  with the load power.

**16.5** A boost converter including an output capacitor equivalent series resistance  $R_C$  is illustrated in Fig. 16.54. For continuous conduction mode operation, the small-signal ac model for this converter can be derived by state-space averaging, with the result illustrated in Fig. 16.55.



**Fig. 16.54** Boost converter with capacitor ESR  $R_C$ , Problem 16.5

**Fig. 16.55** Small-signal ac model for the boost converter of Fig. 16.54

Use the *n*-Extra Element Theorem to derive an expression for the control-to-output transfer function  $G_{vd}(s)$  of this converter. No credit will be given for other methods. Be sure to explain how you derived each term. You may use the following substitutions:

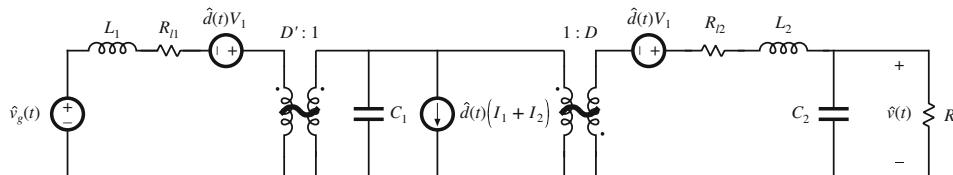
$$R_e = DD' (R||R_C)$$

$$V_e = (D - D') (R||R_C) I_L + V$$

You may express your answer in terms of the following quantities:  $R, R_C, I_L, D, D', V, R_e, V_e, L, C$ . It is not necessary to further simplify your answers.

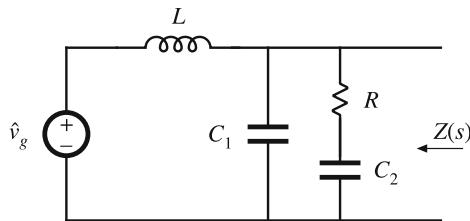
**16.6** Use the *n*-Extra Element Theorem to derive an expression for the control-to-output transfer function  $G_{vd}(s)$  predicted by the SEPIC small-signal model of Fig. 16.17.

**16.7** A small-signal ac model of the Ćuk converter operating in continuous conduction mode is illustrated in Fig. 16.56. Resistors  $R_{l1}$  and  $R_{l2}$  model the inductor copper loss.

**Fig. 16.56** Small-signal ac model of the Ćuk converter of Problem 16.7

Use the *n*-EET to determine the line-to-output transfer function  $G_{vg}(s)$ . Your result should be expressed as a rational fraction in  $s$ . No credit will be given for methods that do not employ the *n*-EET.

- 16.8** Figure 16.57 contains the schematic of a single-section input filter with an  $R$ - $C$  damping network.



**Fig. 16.57** Damped  $L$ - $C$  input filter section, Problem 16.8

Use the  $n$ -EET to write the expression for the output impedance  $Z(s)$  of this network. No credit will be given for methods that do not employ the  $n$ -EET.



## Input Filter Design

### 17.1 Introduction

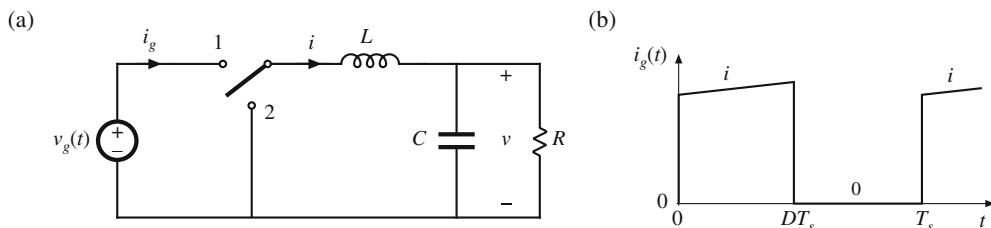
#### 17.1.1 Conducted EMI

It is nearly always required that a filter be added at the power input of a switching converter. By attenuating the switching harmonics that are present in the converter input current waveform, the input filter allows compliance with regulations that limit *conducted electromagnetic interference* (EMI). The input filter can also protect the converter and its load from transients that in the input voltage  $v_g(t)$ , thereby improving the system reliability.

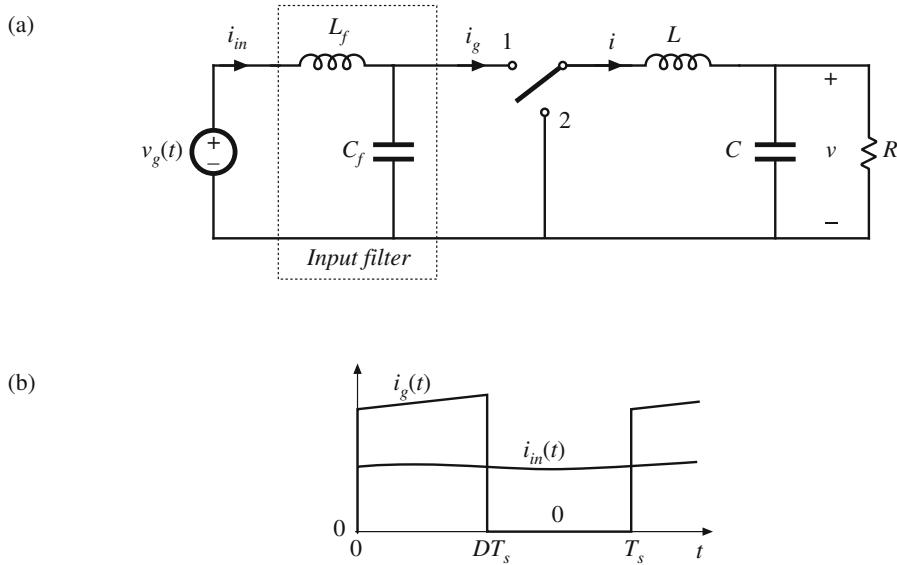
A simple buck converter example is illustrated in Fig. 17.1. The converter injects the pulsating current  $i_g(t)$  of Fig. 17.1b into the power source  $v_g(t)$ . The Fourier series of  $i_g(t)$  contains harmonics at multiples of the switching frequency  $f_s$ , as follows:

$$i_g(t) = DI + \sum_{k=1}^{\infty} \frac{2I}{k\pi} \sin(k\pi D) \cos(k\omega t) \quad (17.1)$$

In practice, the magnitudes of the higher-order harmonics can also be significantly affected by the current spike caused by diode reverse recovery, and also by the finite slopes of the switching transitions. The large high-frequency current harmonics of  $i_g(t)$  can interfere with television and radio reception, and can disrupt the operation of nearby electronic equipment. In consequence, regulations and standards exist that limit the amplitudes of the harmonic currents injected by a



**Fig. 17.1** Buck converter example: (a) circuit of power stage; (b) pulsating input current waveform



**Fig. 17.2** Addition of a simple  $L$ - $C$  low-pass filter to the power input terminals of the buck converter: (a) circuit; (b) input current waveforms

switching converter into its power source [143–150]. As an example, if the dc inductor current  $i$  of Fig. 17.2 has a magnitude of several Amperes, then the fundamental component ( $n = 1$ ) has an rms amplitude in the vicinity of one Ampere. Regulations may require attenuation of this current to a value typically in the range  $10\mu\text{A}$  to  $100\mu\text{A}$ .

To meet limits on conducted EMI, it is necessary to add an input filter to the converter. Figure 17.2 illustrates a simple single-section  $L$ - $C$  low-pass filter, added to the input of the converter of Fig. 17.1. This filter attenuates the current harmonics produced by the switching converter, and thereby smooths the current waveform drawn from the power source. If the filter has transfer function  $H(s) = i_{in}/i_g$ , then the input current Fourier series becomes

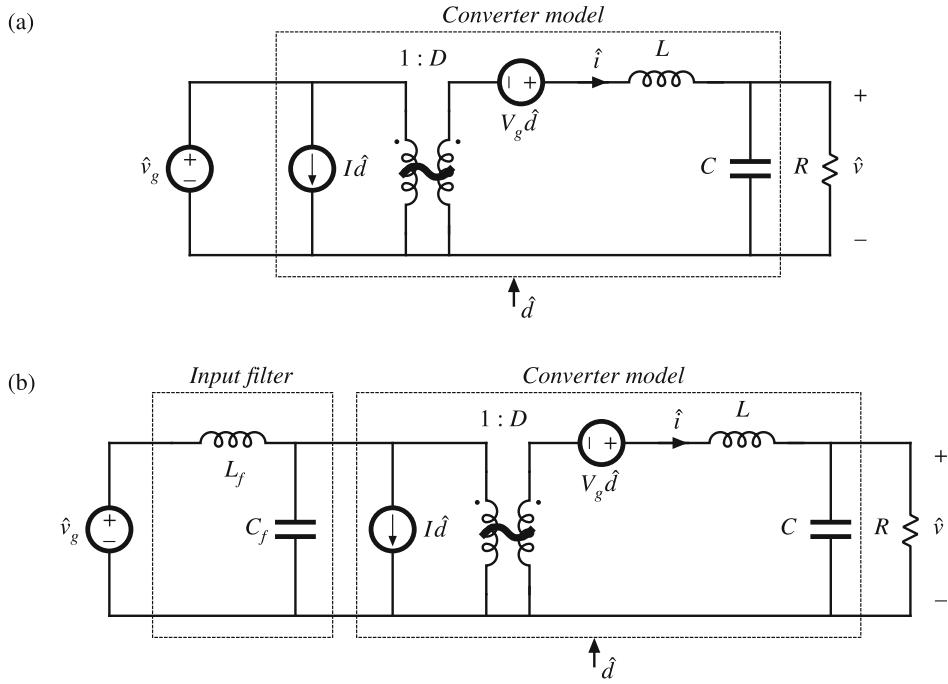
$$i_{in}(t) = H(0)DI + \sum_{k=1}^{\infty} \|H(kj\omega)\| \frac{2I}{k\pi} \sin(k\pi D) \cos(k\omega t + \angle H(kj\omega)) \quad (17.2)$$

In other words, the amplitude of each current harmonic at angular frequency  $k\omega$  is attenuated by the filter transfer function at the harmonic frequency,  $\|H(kj\omega)\|$ . Typical requirements effectively limit the current harmonics to have amplitudes less than  $100\mu\text{A}$ , and hence input filters are often required to attenuate the current amplitudes by 80 dB or more.

To improve the reliability of the system, input filters are sometimes required to operate normally when transients or periodic disturbances are applied to the power input. Such *conducted susceptibility* specifications force the designer to damp the input filter resonances, so that input disturbances do not excite excessive currents or voltages within the filter or converter.

### 17.1.2 The Input Filter Design Problem

The situation faced by the design engineer is typically as follows. A switching regulator has been designed, which meets performance specifications. The regulator was properly designed

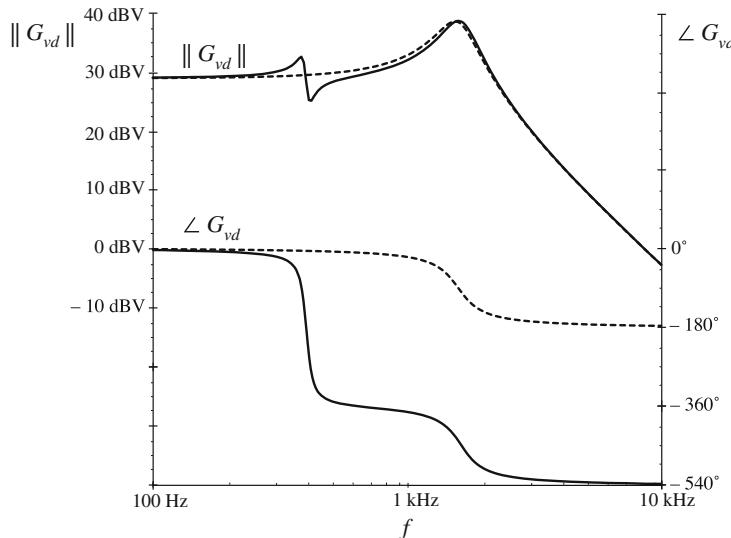


**Fig. 17.3** Small-signal equivalent circuit models of the buck converter: (a) basic converter model, (b) with addition of input filter

as discussed in Chap. 9, using a small-signal model of the converter power stage such as the equivalent circuit of Fig. 17.3a. In consequence, the transient response is well damped and sufficiently fast, with adequate phase margin at all expected operating points. The output impedance is sufficiently small over a wide frequency range. The line-to-output transfer function  $G_{vg}(s)$ , or *audiosusceptibility*, is sufficiently small, so that the output voltage remains regulated in spite of variations in  $\hat{v}_g(t)$ .

Having developed a good design that meets the above goals regarding dynamic response, the designer then addresses the problem of conducted EMI. A low-pass filter having attenuation sufficient to meet conducted EMI specifications is constructed and added to the converter input. A new problem then arises: the input filter changes the dynamics of the converter. The transient response is modified, and the control system may even become unstable. The output impedance may become large over some frequency range, possibly exhibiting resonances. The audiosusceptibility may be degraded.

The problem is that the input filter affects the dynamics of the converter, often in a manner that degrades regulator performance. For example, when a single-section  $L-C$  input filter is added to a buck converter as in Fig. 17.2a, the small-signal equivalent circuit model is modified as shown in Fig. 17.3b. The input filter elements affect all transfer functions of the converter, including the control-to-output transfer function  $G_{vd}(s)$ , the line-to-output transfer function  $G_{vg}(s)$ , and the converter output impedance  $Z_{out}(s)$ . Moreover, the influence of the input filter on these transfer functions can be quite severe.



**Fig. 17.4** Control-to-output transfer functions predicted by the equivalent circuit models of Fig. 17.3. *Dashed lines:* without input filter (Fig. 17.3a). *Solid lines:* with input filter (Fig. 17.3b)

As an illustration, let us examine how the control-to-output transfer function  $G_{vd}(s)$  of the buck converter of Fig. 17.1 is altered when a simple  $L-C$  input filter is added as in Fig. 17.2. For this example, the element values are chosen to be:  $D = 0.5$ ,  $L = 100\mu\text{H}$ ,  $C = 100\mu\text{F}$ ,  $R = 3\Omega$ ,  $L_f = 330\mu\text{H}$ ,  $C_f = 470\mu\text{F}$ . Figure 17.4 contains the Bode plot of the magnitude and phase of the control-to-output transfer function  $G_{vd}(s)$ . The dashed lines are the magnitude and phase before the input filter was added, generated by solution of the model of Fig. 17.3a. The complex poles of the converter output filter cause the phase to approach  $-180^\circ$  at high frequency. Usually, this is the model used to design the regulator feedback loop and to evaluate the phase margin (see Chap. 9). The solid lines of Fig. 17.4 show the magnitude and phase after addition of the input filter, generated by solution of the model of Fig. 17.3b. The magnitude exhibits a “glitch” at the resonant frequency of the input filter, and an additional  $-360^\circ$  of phase shift is introduced into the phase. It can be shown that  $G_{vd}(s)$  now contains an additional complex pole pair and a complex right half-plane zero pair, associated with the input filter dynamics. If the crossover frequency of the regulator feedback loop is near to or greater than the resonant frequency of the input filter, then the loop phase margin will become negative and instability will result. Such behavior is typical; consequently, input filters are notorious for destabilizing switching regulator systems.

This chapter shows how to mitigate the stability problem, by introducing damping into the input filter and by designing the input filter such that its output impedance is sufficiently small [69, 151–162]. The result of these measures is that the effect of the input filter on the control-to-output transfer function becomes negligible, and hence the converter dynamics are much better behaved. Although analysis of the fourth-order system of Fig. 17.3b is potentially quite complex, the approach used here simplifies the problem through use of impedance inequalities involving the converter input impedance and the filter output impedance [151, 152]. These inequalities are based on Middlebrook’s Extra Element Theorem of Sect. 16.1. This approach allows the engi-

neer to gain the insight needed to effectively design the input filter. Optimization of the damping networks of input filters, design of multiple-section filters, and the exact stability criterion, are also discussed.

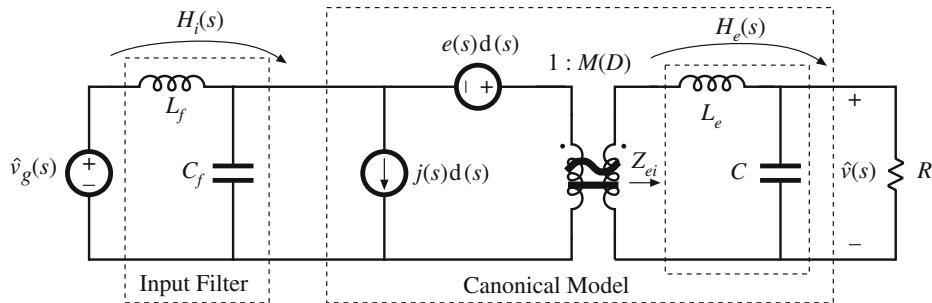
## 17.2 Effect of an Input Filter on Converter Transfer Functions

### 17.2.1 Modified Transfer Functions

The control-to-output transfer function  $G_{vd}(s)$  is defined as follows:

$$G_{vd}(s) = \left. \frac{\hat{v}(s)}{\hat{d}(s)} \right|_{\hat{v}_g(s)=0} \quad (17.3)$$

The control-to-output transfer functions of basic CCM converters with no input filters are listed in Sect. 8.2.2.



**Fig. 17.5** Addition of an input filter to the canonical model of a switching converter

Addition of an input filter to a switching regulator leads to the system illustrated in Fig. 17.5. In Fig. 17.6, the input filter is represented by its Thevenin-equivalent circuit, with  $H_i(s)$  equal to the unloaded transfer function of the filter, and  $Z_o$  equal to the output impedance of the input filter. To determine the control-to-output transfer function in the presence of the input filter, we set  $\hat{v}_g(s)$  to zero and solve for  $\hat{v}(s)/\hat{d}(s)$  according to Eq. (17.3). The input filter can then be represented simply by its output impedance  $Z_o(s)$  as illustrated in Fig. 17.7. Thus, the input filter can be treated as an extra element having impedance  $Z_o(s)$ , and the Extra Element Theorem of Chap. 16.1 can be employed to determine how addition of the input filter modifies the control-to-output transfer function. Specifically, the modified control-to-output transfer function can be expressed as follows [151]:

$$G_{vd}(s) = \left( G_{vd}(s) \Big|_{Z_o(s)=0} \right) \frac{\left( 1 + \frac{Z_o(s)}{Z_N(s)} \right)}{\left( 1 + \frac{Z_o(s)}{Z_D(s)} \right)} \quad (17.4)$$

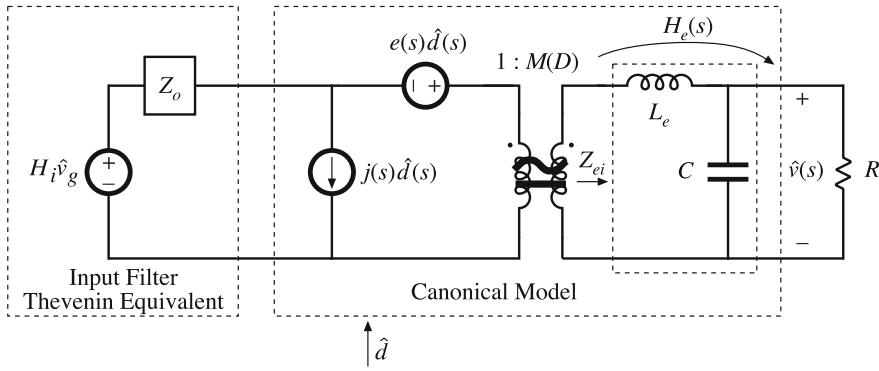
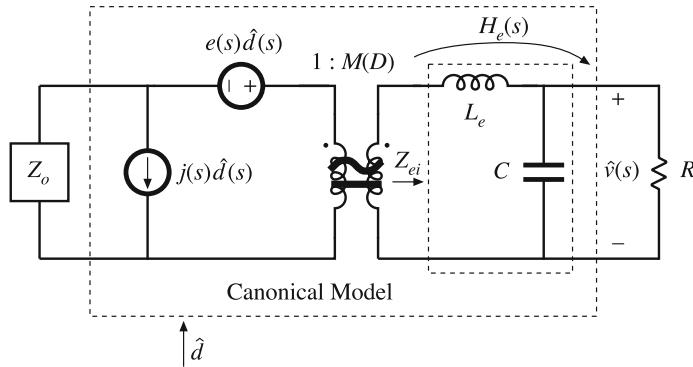


Fig. 17.6 Use of Thevenin-equivalent model for the input filter

Fig. 17.7 Finding the control-to-output transfer function  $G_{vd}(s)$ 

where

$$G_{vd}(s) \Big|_{Z_o(s)=0} \quad (17.5)$$

is the original control-to-output transfer function with no input filter.

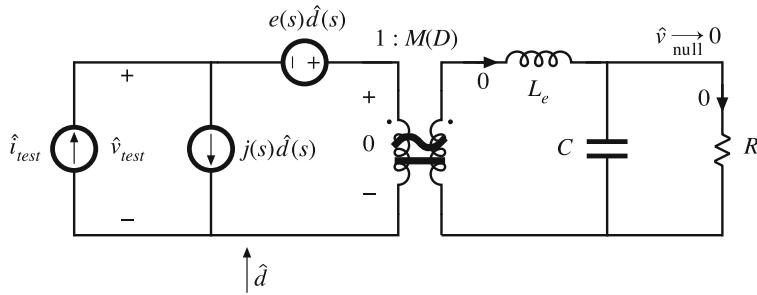
Figure 17.8 illustrates determination of  $Z_N(s)$ . In the presence of  $\hat{d}$ , a current  $\hat{i}_{test}$  is injected at the input port of the converter, and the  $\hat{d}$  and  $\hat{i}_{test}$  inputs are adjusted such that the output  $\hat{v}$  is nulled. Under these conditions, we find  $\hat{v}_{test}$  and

$$Z_N = \frac{\hat{v}_{test}}{\hat{i}_{test}} \Big|_{\hat{v} \rightarrow 0} \quad (17.6)$$

When the output  $\hat{v}$  is nulled, then no current flows through the load  $R$ , capacitor  $C$ , or inductor  $L_e$ . Hence there is no voltage across these elements, and the voltages across the transformer windings are zero. With no secondary winding current, the transformer primary winding current is zero as well. Hence we can find that

$$\hat{v}_{test} = -e(s)\hat{d} \quad (17.7)$$

$$\hat{i}_{test} = j(s)\hat{d} \quad (17.8)$$

**Fig. 17.8** Finding  $Z_N(s)$ 

Therefore,

$$Z_N = \frac{-e(s)\hat{d}}{j(s)\hat{d}} = -\frac{e(s)}{j(s)} \quad (17.9)$$

This is a general result, expressed in terms of the canonical model parameters  $e(s)$  and  $j(s)$ . The impedance  $Z_N$  is the input port impedance of the converter, under the conditions that  $\hat{d}$  and  $\hat{i}_{test}$  are varied as necessary to null the output voltage  $\hat{v}$ . Generally,  $Z_N$  is negative.

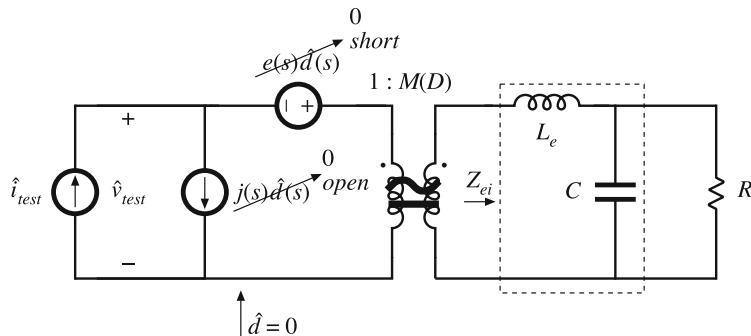
**Fig. 17.9** Finding  $Z_D(s)$ 

Figure 17.9 illustrates determination of  $Z_D(s)$ . The input  $\hat{d}$  is set to zero, and current  $\hat{i}_{test}$  is injected at the input port of the converter. The quantity  $Z_D$  is given by

$$Z_D = \left. \frac{\hat{v}_{test}}{\hat{i}_{test}} \right|_{\hat{d}=0} \quad (17.10)$$

Setting  $\hat{d}$  to zero causes the  $e(s)\hat{d}$  and  $j(s)\hat{d}$  sources to be zero. The driving-point impedance at the injection point is equal to the canonical model filter impedance  $Z_{ei}$ , reflected through the transformer turns ratio:

$$Z_D(s) = \frac{Z_{ei}(s)}{M^2} \quad (17.11)$$

This is a general result, expressed in terms of the canonical model parameters  $Z_{ei}$  and  $M$ . The impedance  $Z_D$  is the input port impedance of the converter, under open-loop conditions with  $\hat{d} = 0$ .

A similar analysis shows that the converter open-loop output impedance can be expressed in the form

$$Z_{out}(s) = \left( Z_{out}(s) \Big|_{Z_o(s)=0} \right) \frac{\left( 1 + \frac{Z_o(s)}{Z_e(s)} \right)}{\left( 1 + \frac{Z_o(s)}{Z_D(s)} \right)} \quad (17.12)$$

where

$$Z_{out}(s) \Big|_{Z_o(s)=0} \quad (17.13)$$

is the original converter output impedance with no input filter. The quantity  $Z_e(s)$  is equal to the converter input impedance  $Z_i(s)$  under the conditions that the converter output is shorted:

$$Z_e = Z_i \Big|_{\hat{v}=0} \quad (17.14)$$

The quantity  $Z_D(s)$  is again the open-loop driving-point impedance at the power input port of the open-loop converter, given by Eq. (17.11).

### 17.2.2 Discussion

Equation (17.4) relates the power stage control-to-output transfer function  $G_{vd}(s)$  to the output impedance  $Z_o(s)$  of the input filter, and also to the quantities  $Z_N(s)$  and  $Z_D(s)$  measured at the power input port of the converter. The quantity  $Z_D(s)$  coincides with the open-loop input impedance of the converter.

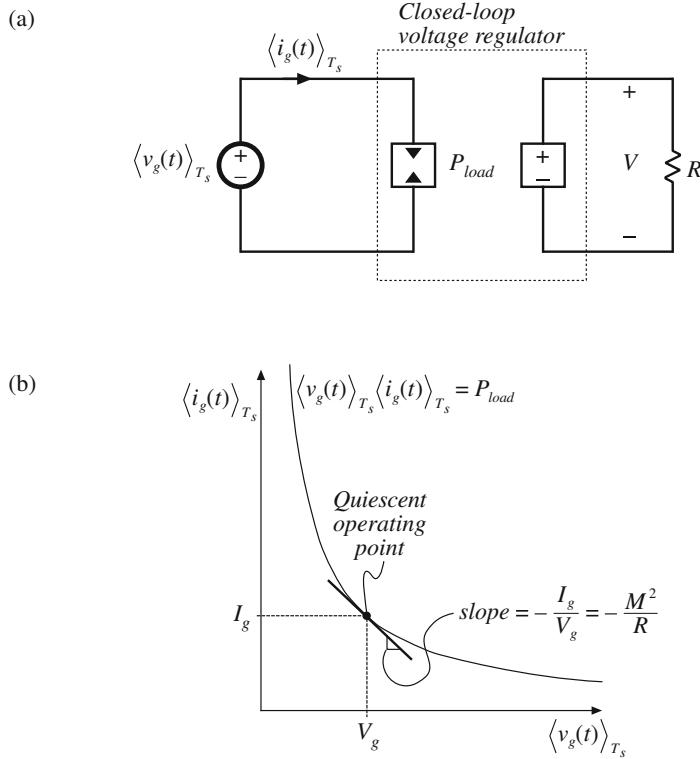
As described above, the quantity  $Z_N(s)$  is equal to the input port impedance of the converter power stage, under the conditions that  $\hat{d}(s)$  is varied as necessary to null  $\hat{v}(s)$  to zero. This is, in fact, the function performed by an ideal controller: it varies the duty cycle as necessary to maintain zero error of the output voltage. Therefore,  $Z_N(s)$  coincides with the impedance that would be measured at the converter power input terminals, if an ideal feedback loop perfectly regulated the converter output voltage. Of course, Eq. (17.4) is valid in general, regardless of whether a control system is present.

Figure 17.10 illustrates the large-signal dc behavior of a feedback loop that perfectly regulates the converter output voltage. Regardless of the applied input voltage  $v_g(t)$ , the output voltage is maintained equal to the desired value  $V$ . The load power is therefore constant, and equal to  $P_{load} = V^2/R$ . In the idealized case of a lossless converter, the power flowing into the converter input terminals will also be equal to  $P_{load}$ , regardless of the value of  $v_g(t)$ . Hence, the power input terminal of the converter obeys the equation

$$\langle v_g(t) \rangle_{T_s} \langle i_g(t) \rangle_{T_s} = P_{load} \quad (17.15)$$

This characteristic is illustrated in Fig. 17.10b, and is represented in Fig. 17.10a by the dependent power sink symbol. The properties of power sources and power sinks are discussed in detail in Chap. 15.

Figure 17.10b also illustrates linearization of the constant input power characteristic, about a quiescent operating point. The resulting line has negative slope; therefore, the incremental



**Fig. 17.10** Power input port characteristics of an ideal switching voltage regulator: (a) equivalent circuit model, including dependent power sink, (b) constant power characteristic of input port

(small signal) input resistance of the ideal voltage regulator is negative. For example, increasing the voltage  $\langle v_g(t) \rangle_{T_s}$  causes the current  $\langle i_g(t) \rangle_{T_s}$  to decrease, such that the power remains constant. This incremental resistance has the value [151, 156]:

$$-\frac{R}{M^2} \quad (17.16)$$

where  $R$  is the output load resistance, and  $M$  is the conversion ratio  $V/V_g$ . For the buck, boost, buck-boost, and other converters, the dc asymptote of  $Z_N(s)$  coincides with the negative incremental resistance given by Eq. (17.16). In a closed-loop switching regulator that regulates its output voltage well, the negative incremental resistance (17.16) is the dc asymptote of the regulator closed-loop input impedance  $Z_i(s)$ .

Loading of an  $L-C$  input filter and its output impedance  $Z_o(s)$  by the negative incremental resistance of Eq. (17.16) can lead to instability. Indeed, the  $(\hat{v}/\hat{v}_g)$  transfer function of the closed-loop regulator with input filter includes the voltage divider term

$$\frac{Z_i(s)}{Z_o(s) + Z_i(s)} \quad (17.17)$$

If the regulator input impedance  $Z_i(s)$  is well approximated by Eq. (17.16) and the input filter is an undamped  $L$ - $C$  filter, then the divider ratio (17.17) contains RHP poles.

Hence, when an undamped or lightly damped input filter is connected to the regulator input port, the input filter can interact with the negative resistance characteristic of  $Z_i(s)$  to form a *negative resistance oscillator* that can be viewed as the origin of input filter instabilities. It should be noted that the regulator closed-loop input impedance  $Z_i(s)$  is also affected by the power stage reactive elements and the loop gain, and reverts to a positive impedance at high frequencies. These additional dynamics also impact the stability of the system. A more detailed stability analysis that accounts for the dynamics of  $Z_i(s)$  is explained in Sect. 17.5.

### 17.2.3 Impedance Inequalities

Expressions for  $Z_N(s)$ ,  $Z_D(s)$ , and  $Z_e(s)$  for the basic buck, boost, and buck-boost converters are listed in Table 17.1.

Equation (17.4) reveals that addition of the input filter causes the control-to-output transfer function  $G_{vd}(s)$  to be modified by the factor

$$\frac{\left(1 + \frac{Z_o(s)}{Z_N(s)}\right)}{\left(1 + \frac{Z_o(s)}{Z_D(s)}\right)} \quad (17.18)$$

called the *correction factor*. When the following inequalities are satisfied,

$$\begin{aligned} \|Z_o\| &\ll \|Z_N\|, \text{ and} \\ \|Z_o\| &\ll \|Z_D\| \end{aligned} \quad (17.19)$$

then the correction factor has a magnitude of approximately unity, and the input filter does not substantially alter the control-to-output transfer function [151, 152]. These inequalities limit the maximum allowable output impedance of the input filter, and constitute useful filter design criteria. One can sketch the Bode plots of  $\|Z_N(j\omega)\|$  and  $\|Z_D(j\omega)\|$ , and compare with the Bode plot of  $\|Z_o(j\omega)\|$ . This allows the engineer to gain the insight necessary to design an input filter that satisfies inequalities (17.19).

**Table 17.1** Input filter design criteria for basic converters

Converter	$Z_N(s)$	$Z_D(s)$	$Z_e(s)$
Buck	$-\frac{R}{D^2}$	$\frac{R}{D^2} \frac{\left(1 + s\frac{L}{R} + s^2LC\right)}{(1 + sRC)}$	$\frac{sL}{D^2}$
Boost	$-D'^2R \left(1 - \frac{sL}{D'^2R}\right)$	$D'^2R \frac{\left(1 + s\frac{L}{D'^2R} + s^2\frac{LC}{D'^2}\right)}{(1 + sRC)}$	$sL$
Buck-boost	$-\frac{D'^2R}{D^2} \left(1 - \frac{sDL}{D'^2R}\right)$	$\frac{D'^2R}{D^2} \frac{\left(1 + s\frac{L}{D'^2R} + s^2\frac{LC}{D'^2}\right)}{(1 + sRC)}$	$\frac{sL}{D^2}$

The buck converter example of the next section illustrates how violation of inequalities (17.19) not only causes the transfer function  $G_{vd}(s)$  to be significantly changed, but also can introduce resonant poles and RHP zeroes that can seriously degrade the converter loop gain and its phase margin.

According to Eq. (17.12), the converter open-loop output impedance  $Z_{out}(s)$  is not substantially affected by the input filter when the following inequalities are satisfied:

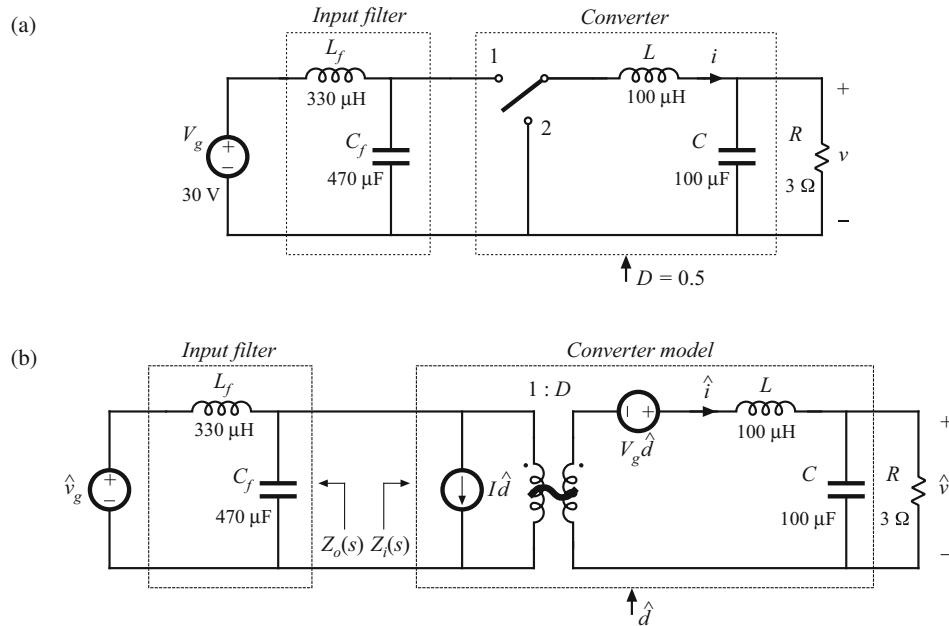
$$\begin{aligned} \|Z_o\| &\ll \|Z_e\|, \text{ and} \\ \|Z_o\| &\ll \|Z_D\| \end{aligned} \quad (17.20)$$

An input filter design that satisfies inequalities (17.19) but not (17.20) can be expected to leave the loop gain unchanged, but to modify the open-loop converter output impedance. This would lead to a modified closed-loop output impedance as well.

Similar impedance inequalities can be derived for the case of current-programmed converters [154, 155], or converters operating in the discontinuous conduction mode. Feedforward of the converter input voltage was suggested in [157]. Analysis of the effect of an input filter on a current-programmed converter is discussed in Sect. 18.4.4.

### 17.3 Buck Converter Example

Let us again consider the example of a simple buck converter with  $L-C$  input filter, as illustrated in Fig. 17.11a. Upon replacing the converter with its small-signal model, we obtain the equivalent circuit of Fig. 17.11b. Let us evaluate Eq. (17.4) for this example, to find how the input filter modifies the control-to-output transfer function of the converter.



**Fig. 17.11** Buck converter example: (a) converter circuit, (b) small-signal model

### 17.3.1 Effect of Undamped Input Filter

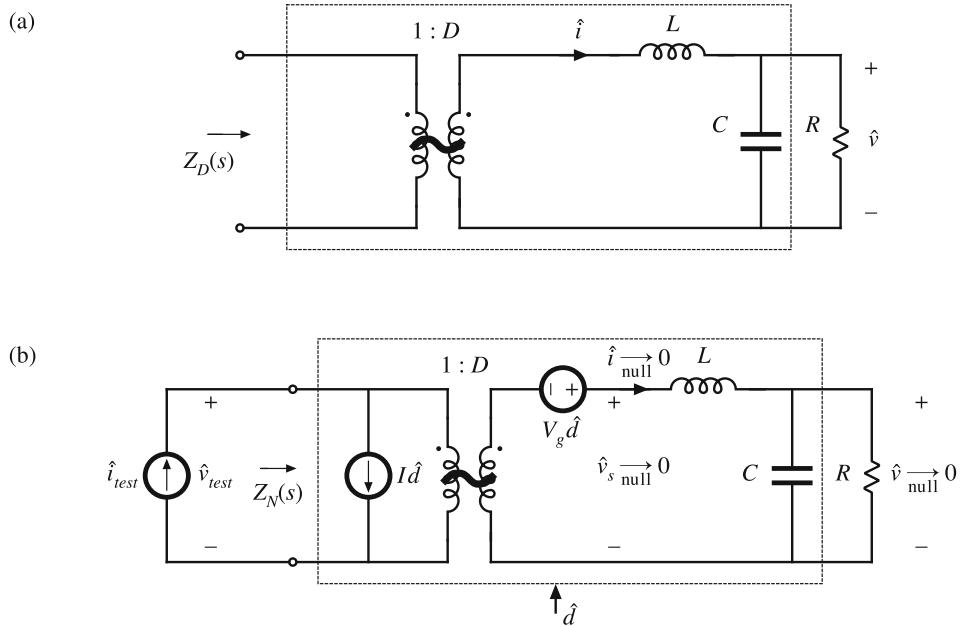
The quantities  $Z_N(s)$  and  $Z_D(s)$  can be read from Table 17.1, or can be derived from the converter model of Fig. 17.11b using Eqs. (17.6) and (17.10) as described in Sect. 17.2. Figure 17.12a illustrates determination of  $Z_D$  based on the buck converter model Fig. 17.11b. Upon setting  $\hat{d}(s)$  to zero, the converter small-signal model reduces to the circuit of Fig. 17.12a. It can be seen that  $Z_D(s)$  is equal to the input impedance of the  $R-L-C$  filter, divided by the square of the turns ratio:

$$Z_D(s) = \frac{1}{D^2} \left( sL + R \parallel \frac{1}{sC} \right) \quad (17.21)$$

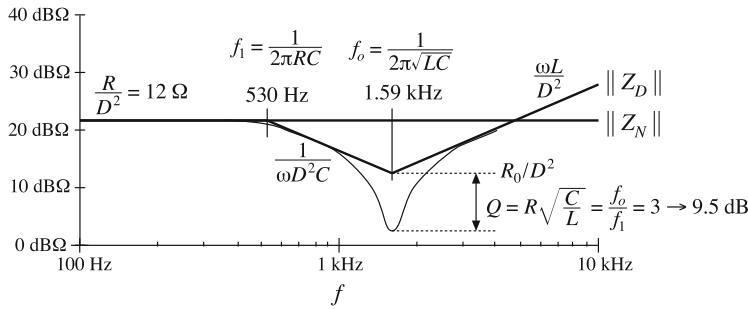
Construction of asymptotes for this impedance is treated in Sect. 8.4, with the results for the numerical values of this example given in Fig. 17.13. The load resistance dominates the impedance at low frequency, leading to a dc asymptote of  $R/D^2 = 12 \Omega$ . For the high- $Q$  case shown,  $\|Z_D(j\omega)\|$  follows the output capacitor asymptote, reflected through the square of the effective turns ratio, at intermediate frequencies. A series resonance occurs at the output filter resonant frequency  $f_0$ , given by

$$f_0 = \frac{1}{2\pi \sqrt{LC}} \quad (17.22)$$

For the element values listed in Fig. 17.11a, the resonant frequency is  $f_0 = 1.6 \text{ kHz}$ . The values of the asymptotes at the resonant frequency  $f_0$  are given by the characteristic impedance  $R_0$ , referred to the transformer primary:



**Fig. 17.12** Determination of the quantities  $Z_N(s)$  and  $Z_D(s)$  for the circuit of Fig. 17.11b; (a) determination of  $Z_D(s)$ , (b) determination of  $Z_N(s)$



**Fig. 17.13** Construction of  $\|Z_N(j\omega)\|$  and  $\|Z_D(j\omega)\|$ , buck converter example

$$\frac{R_0}{D^2} = \frac{1}{D^2} \sqrt{\frac{L}{C}} \quad (17.23)$$

For the element values given in Fig. 17.11a, this expression is equal to  $4 \Omega$ . The  $Q$ -factor is given by

$$Q = \frac{R}{R_0} = R \sqrt{\frac{C}{L}} \quad (17.24)$$

This expression yields a numerical value of  $Q = 3$ . The value of  $\|Z_D(j\omega)\|$  at the resonant frequency 1.6 kHz is therefore equal to  $(4 \Omega)/(3) = 1.33 \Omega$ . At high frequency,  $\|Z_D(j\omega)\|$  follows the reflected inductor asymptote.

Figure 17.12b illustrates determination of  $Z_N$  based on the buck converter model in Fig. 17.11b. This impedance is equal to the converter input impedance under the conditions that  $\hat{d}(s)$  is varied to maintain the output voltage  $\hat{v}(s)$  at zero. Figure 17.12b illustrates the derivation of an expression for  $Z_N(s)$ . A test current source  $\hat{i}_{test}(s)$  is injected at the converter input port. The impedance  $Z_N(s)$  can be viewed as the transfer function from  $\hat{i}_{test}(s)$  to  $\hat{v}_{test}(s)$ :

$$Z_N(s) = \left. \frac{\hat{v}_{test}(s)}{\hat{i}_{test}(s)} \right|_{\hat{v}_{test} \rightarrow 0} \quad (17.25)$$

The null condition  $\hat{v}(s) \rightarrow 0$  greatly simplifies analysis of the circuit of Fig. 17.12b. Since the voltage  $\hat{v}(s)$  is zero, the currents through the capacitor and load impedances are also zero. This further implies that the inductor current  $\hat{i}(s)$  and transformer winding currents are zero, and hence the voltage across the inductor is also zero. Finally, the voltage  $\hat{v}_s(s)$ , equal to the output voltage plus the inductor voltage, is zero.

Since the currents in the windings of the transformer model are zero, the current  $i_{test}(s)$  is equal to the independent source current  $I\hat{d}(s)$ :

$$\hat{i}_{test}(s) = I\hat{d}(s) \quad (17.26)$$

Because  $\hat{v}_s(s)$  is equal to zero, the voltage applied to the secondary of the transformer model is equal to the independent source voltage  $-V_g\hat{d}(s)$ . Upon dividing by the turns ratio  $D$ , we obtain  $\hat{v}_{test}(s)$ :

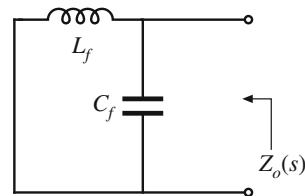
$$\hat{v}_{test}(s) = -\frac{V_g\hat{d}(s)}{D} \quad (17.27)$$

Insertion of Eqs. (17.26) and (17.27) into Eq. (17.25) leads to the following result:

$$Z_N(s) = \frac{\left(-\frac{V_g \hat{d}(s)}{D}\right)}{(I\hat{d}(s))} = -\frac{R}{D^2} \quad (17.28)$$

The steady-state relationship  $I = DV_g/R$  has been used to simplify the above result. This equation coincides with the expression listed in Table 17.1. The Bode diagram of  $\|Z_N(j\omega)\|$  is constructed in Fig. 17.13; this plot coincides with the dc asymptote of  $\|Z_D(j\omega)\|$ . The impedance  $Z_N$  is negative, and has magnitude equal to the reflected load resistance.

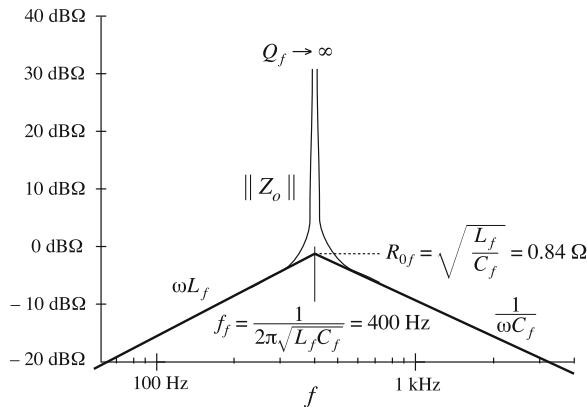
**Fig. 17.14** Determination of the filter output impedance  $Z_o(s)$



Next, let us construct the Bode diagram of the filter output impedance  $Z_o(s)$ . When the independent source  $\hat{V}_g(s)$  is set to zero, the input filter network reduces to the circuit of Fig. 17.14. It can be seen that  $Z_o(s)$  is given by the parallel combination of the inductor  $L_f$  and the capacitor  $C_f$ :

$$Z_o(s) = sL_f \parallel \frac{1}{sC_f} \quad (17.29)$$

Construction of the Bode diagram of this parallel resonant circuit is discussed in Sect. 8.3.4. As illustrated in Fig. 17.15, the magnitude  $\|Z_o(j\omega)\|$  is dominated by the inductor impedance at low frequency, and by the capacitor impedance at high frequency. The inductor and capacitor asymptotes intersect at the filter resonant frequency:



**Fig. 17.15** Magnitude plot of the output impedance of the input filter of Fig. 17.14. Since the filter is not damped, the  $Q$ -factor is very large

$$f_f = \frac{1}{2\pi\sqrt{L_f C_f}} \quad (17.30)$$

For the given values, the input filter resonant frequency is  $f_f = 400$  Hz. This filter has characteristic impedance

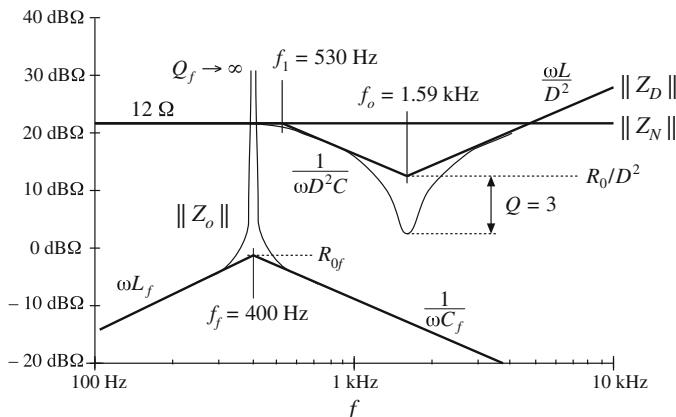
$$R_{0f} = \sqrt{\frac{L_f}{C_f}} \quad (17.31)$$

equal to  $0.84 \Omega$ . Since the input filter is undamped, its  $Q$ -factor is ideally infinite. In practice, parasitic elements such as inductor loss and capacitor equivalent series resistance limit the value of  $Q_f$ . Nonetheless, the impedance  $\|Z_o(j\omega)\|$  is very large in the vicinity of the filter resonant frequency  $f_f$ .

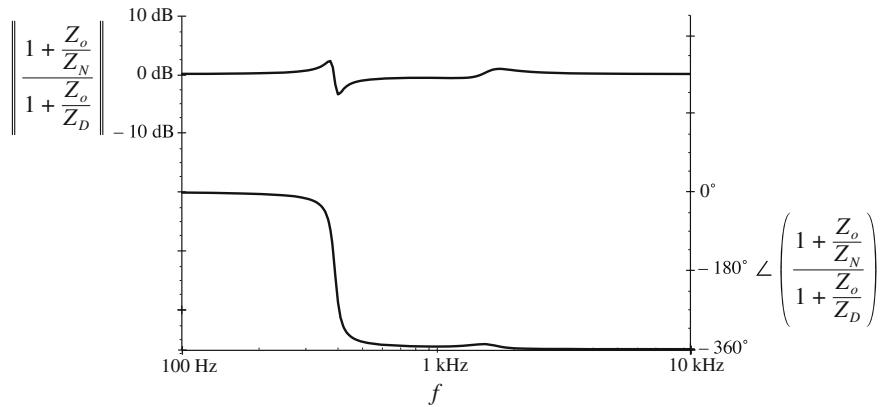
The Bode plot of the filter output impedance  $\|Z_o(j\omega)\|$  is overlaid on the  $\|Z_N(j\omega)\|$  and  $\|Z_D(j\omega)\|$  plots in Fig. 17.16, for the element values listed in Fig. 17.11a. We can now determine whether the impedance inequalities (17.19) are satisfied. Note the design-oriented nature of Fig. 17.16: since analytical expressions are given for each impedance asymptote, the designer can easily adjust the component values to satisfy Eq. (17.19). For example, the values of  $L_f$  and  $C_f$  should be chosen to ensure that the asymptotes of  $\|Z_o(j\omega)\|$  lie below the worst-case value of  $R/D^2$ , as well as the other asymptotes of  $\|Z_D(j\omega)\|$ .

It should also be apparent that it is a bad idea to choose the input and output filter resonant frequencies  $f_0$  and  $f_f$  to be equal, because it would then be more difficult to satisfy the inequalities of Eq. (17.19). Instead, the resonant frequencies  $f_0$  and  $f_f$  should be well separated in value.

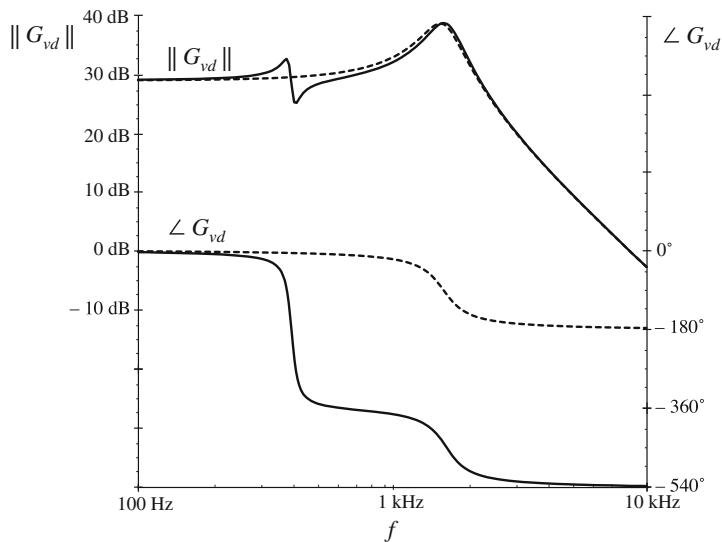
Since the input filter is undamped, it is impossible to satisfy the impedance inequalities (17.19) in the vicinity of the input filter resonant frequency  $f_f$ . Regardless of the choice of element values, the input filter changes the control-to-output transfer function  $G_{vd}(s)$  in the vicinity of frequency  $f_f$ . Figures 17.17 and 17.18 illustrate the resulting correction factor [Eq. (17.18)] and the modified control-to-output transfer function [Eq. (17.4)], respectively. At



**Fig. 17.16** Impedance design criteria  $\|Z_N(j\omega)\|$  and  $\|Z_D(j\omega)\|$  from Fig. 17.13, with the filter output impedance  $\|Z_o(j\omega)\|$  superimposed. The design criteria of Eq. (17.19) are not satisfied at the input filter resonance



**Fig. 17.17** Magnitude (upper plot) and phase (lower plot) of the correction factor, Eq. (17.18), for the buck converter example of Fig. 17.11



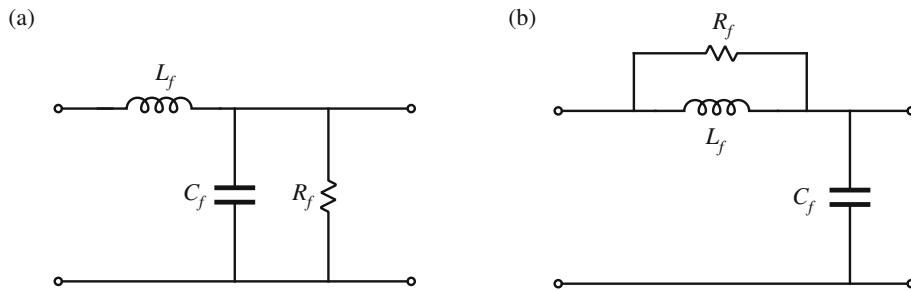
**Fig. 17.18** Effect of undamped input filter on the control-to-output transfer function of the buck converter example. *Dashed lines:* without input filter. *Solid lines:* with undamped input filter

frequencies well below the input filter resonant frequency, impedance inequalities (17.19) are well satisfied. The correction factor tends to the value \$1\angle 0^\circ\$, and the control-to-output transfer function \$G\_{vd}(s)\$ is essentially unchanged. In the vicinity of the resonant frequency \$f\_f\$, the correction factor contains a pair of complex poles, and also a pair of right half-plane complex zeroes. These cause a “glitch” in the magnitude plot of the correction factor, and they contribute \$360^\circ\$ of lag to the phase of the correction factor. The glitch and its phase lag can be seen in the Bode plot of \$G\_{vd}(s)\$. At high frequency, the correction factor tends to a value of approximately \$1\angle -360^\circ\$; consequently, the high-frequency magnitude of \$G\_{vd}\$ is unchanged. However, when the

$-360^\circ$  contributed by the correction factor is added to the  $-180^\circ$  contributed at high frequency by the two poles of the original  $G_{vd}(s)$ , a high-frequency phase asymptote of  $-540^\circ$  is obtained. If the crossover frequency of the converter feedback loop is placed near to or greater than the input filter resonant frequency  $f_f$ , then a negative phase margin is inevitable. This explains why addition of an input filter often leads to instabilities and oscillations in switching regulators.

### 17.3.2 Damping the Input Filter

Let us damp the resonance of the input filter, so that impedance inequalities (17.19) are satisfied at all frequencies.



**Fig. 17.19** Two attempts to damp the input filter: (a) addition of damping resistance  $R_f$  across  $C_f$ , (b) addition of damping resistance  $R_f$  in parallel with  $L_f$

One approach to damping the filter is to add resistor  $R_f$  in parallel with capacitor  $C_f$  as illustrated in Fig. 17.19a. The output impedance of this network is identical to the parallel resonant impedance analyzed in Sect. 8.3.4. The maximum value of the output impedance occurs at the resonant frequency  $f_f$ , and is equal in value to the resistance  $R_f$ . Hence, to satisfy impedance inequalities (17.19), we should choose  $R_f$  to be much less than the  $\|Z_N(j\omega)\|$  and  $\|Z_D(j\omega)\|$  asymptotes. The condition  $R_f \ll \|Z_N(j\omega)\|$  can be expressed as:

$$R_f \ll \frac{R}{D^2} \quad (17.32)$$

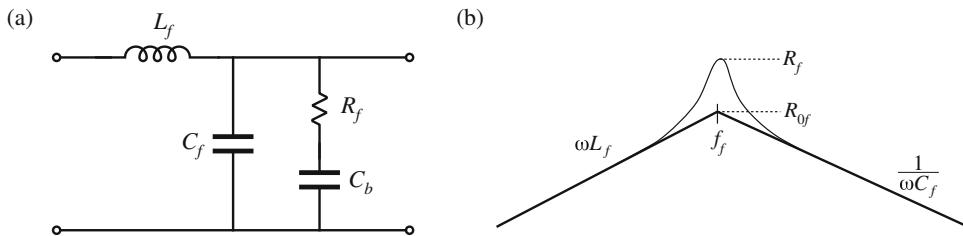
Unfortunately, this raises a new problem: the power dissipation in  $R_f$ . The dc input voltage  $V_g$  is applied across resistor  $R_f$ , and therefore  $R_f$  dissipates power equal to  $V_g^2/R_f$ . Equation (17.32) implies that this power loss is greater than the load power! Therefore, the circuit of Fig. 17.19a is not a practical solution.

One solution to the power loss problem is to place  $R_f$  in parallel with  $L_f$  as illustrated in Fig. 17.19b. The value of  $R_f$  in Fig. 17.19b is also chosen according to Eq. (17.32). Since the dc voltage across inductor  $L_f$  is zero, there is now no dc power loss in resistor  $R_f$ . The problem with this circuit is that its transfer function contains a high-frequency zero. Addition of  $R_f$  degrades the slope of the high-frequency asymptote, from  $-40$  dB/decade to  $-20$  dB/decade. The circuit of Fig. 17.19b is effectively a single-pole  $R-C$  low-pass filter, with no attenuation provided by inductor  $L_f$ .

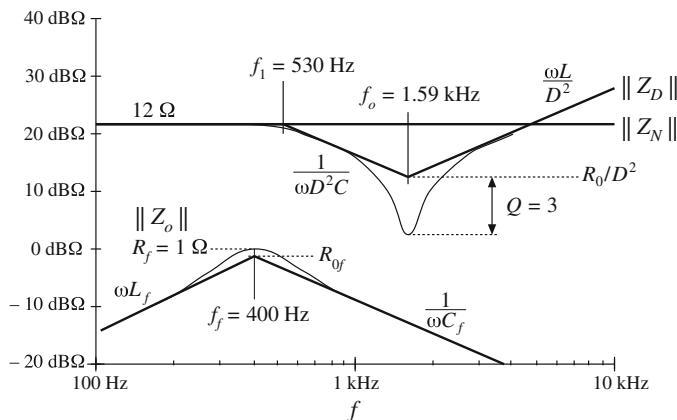
One practical solution is illustrated in Fig. 17.20 [152]. Dc blocking capacitor  $C_b$  is added in series with resistor  $R_f$ . Since no dc current can flow through resistor  $R_f$ , its dc power loss is eliminated. The value of  $C_b$  is chosen to be very large such that, at the filter resonant frequency  $f_f$ , the impedance of the  $R_f-C_b$  branch is dominated by resistor  $R_f$ . When  $C_b$  is sufficiently large, then the output impedance of this network reduces to the output impedances of the filters of Fig. 17.19. The impedance asymptotes for the case of large  $C_b$  are illustrated in Fig. 17.20b.

The low-frequency asymptotes of  $\|Z_N(j\omega)\|$  and  $\|Z_D(j\omega)\|$  in Fig. 17.13 are equal to  $R/D^2 = 12 \Omega$ . The choice  $R_f = 1 \Omega$  therefore satisfies impedance inequalities (17.19) very well. The choice  $C_b = 4700 \mu\text{F}$  leads to  $1/2\pi f_f C_b = 0.084 \Omega$ , which is much smaller than  $R_f$ . The resulting magnitude  $\|Z_o(j\omega)\|$  is compared with  $\|Z_N(j\omega)\|$  and  $\|Z_D(j\omega)\|$  in Fig. 17.21. It can be seen that the chosen values of  $R_f$  and  $C_b$  lead to adequate damping, and impedance inequalities (17.19) are now well satisfied.

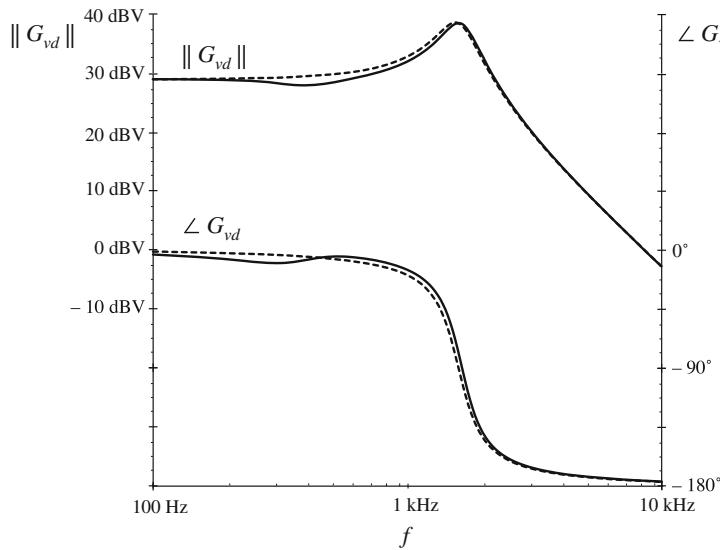
Figure 17.22 illustrates how addition of the damped input filter modifies the magnitude and phase of the control-to-output transfer function. There is now very little change in  $G_{vd}(s)$ , and we would expect that the performance of the converter feedback loop is unaffected by the input filter.



**Fig. 17.20** A practical method to damping the input filter, including damping resistance  $R_f$  and dc blocking capacitor  $C_b$ : (a) circuit, (b) output impedance asymptotes



**Fig. 17.21** Impedance design criteria  $\|Z_N(j\omega)\|$  and  $\|Z_D(j\omega)\|$  from Fig. 17.13, with the damped filter output impedance  $\|Z_o(j\omega)\|$  of Fig. 17.20 superimposed. The design criteria of Eq. (17.19) are well satisfied



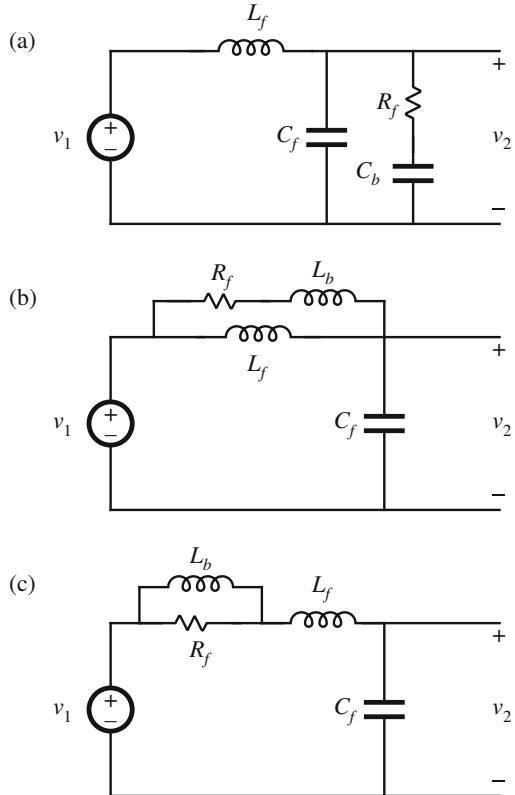
**Fig. 17.22** Effect of the damped input filter on the control-to-output transfer function of the buck converter example. *Dashed lines:* without input filter. *Solid lines:* with damped input filter

## 17.4 Design of a Damped Input Filter

As illustrated by the example of the previous section, design of an input filter requires not only that the filter impedance asymptotes satisfy impedance inequalities, but also that the filter be adequately damped. Damping of the input filter is also necessary to prevent transients and disturbances in  $v_g(t)$  from exciting filter resonances. Other design constraints include attaining the desired filter attenuation, and minimizing the size of the reactive elements. Although a large number of classical filter design techniques are well known, these techniques do not address the problems of limiting the maximum output impedance and damping filter resonances.

The value of the blocking capacitor  $C_b$  used to damp the input filter in Sect. 17.3.2 is ten times larger than the value of  $C_f$ , and hence its size and cost are of practical concern. Optimization of an input filter design therefore includes minimization of the size of the elements used in the damping networks.

Several practical approaches to damping the single-section  $L-C$  low-pass filter are illustrated in Fig. 17.23 [152, 153, 158]. Figure 17.23a contains the  $R_f-C_b$  damping branch considered in the previous section. In Fig. 17.23b, the damping resistor  $R_f$  is placed in parallel with the filter inductor  $L_f$ , and a high-frequency blocking inductor  $L_b$  is placed in series with  $R_f$ . Inductor  $L_b$  causes the filter transfer function to roll-off with a high-frequency slope of  $-40 \text{ dB/decade}$ . In Fig. 17.23c, the damping resistor  $R_f$  is placed in series with the filter inductor  $L_f$ , and the dc current is bypassed by inductor  $L_b$ . In each case, it is desired to obtain a given amount of damping (i.e., to cause the peak value of the filter output impedance to be no greater than a given value that satisfies the impedance inequalities (17.19)), while minimizing the value of  $C_b$  or  $L_b$ . This problem can be formulated in an alternate but equivalent form: for a given choice of  $C_b$  or  $L_b$ , find the value of  $R_f$  that minimizes the peak output impedance [152]. The solutions



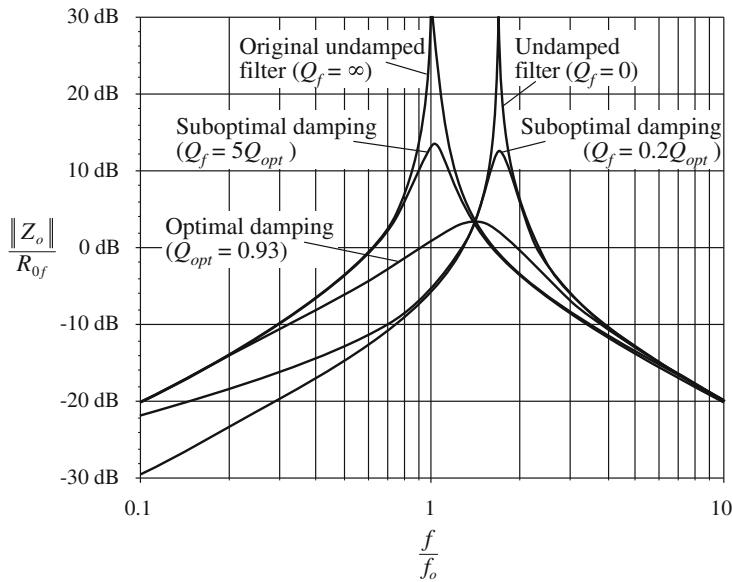
**Fig. 17.23** Several practical approaches to damping the single-section input filter: (a)  $R_f-C_b$  parallel damping, (b)  $R_f-L_b$  parallel damping, (c)  $R_f-L_b$  series damping

to this optimization problem, for the three filter networks of Fig. 17.23, are summarized in this section. In each case, the quantities  $f_f$  and  $R_{0f}$  are defined by Eqs. (17.30) and (17.31).

Consider the filter of Fig. 17.23b, with fixed values of  $L_f$ ,  $C_f$ , and  $L_b$ . Figure 17.24 contains Bode plots of the filter output impedance  $\|Z_0(j\omega)\|$  for several values of damping resistance  $R_f$ . For the limiting case  $R_f = \infty$ , the circuit reduces to the original undamped filter with infinite  $Q_f$ . In the limiting case  $R_f = 0$ , the filter is also undamped, but the resonant frequency is increased because  $L_b$  becomes connected in parallel with  $L_f$ . Between these two extremes, there must exist an optimum value of  $R_f$  that causes the peak filter output impedance to be minimized. It can be shown [152, 158] that all magnitude plots must pass through a common point, and therefore the optimum attains its peak at this point. This fact has been used to derive the design equations of optimally damped  $L$ - $C$  filter sections.

#### 17.4.1 $R_f-C_b$ Parallel Damping

Optimization of the filter network of Fig. 17.23a and Sect. 17.3.2 was described in [152]. The high-frequency attenuation of this filter is not affected by the choice of  $C_b$ , and the high-frequency asymptote is identical to that of the original undamped filter. The sole tradeoff in design of the damping elements for this filter is in the size of the blocking capacitor  $C_b$  vs. the damping achieved.



**Fig. 17.24** Comparison of output impedance curves for optimal parallel  $R_f-L_b$  damping with undamped and several suboptimal designs. For this example,  $n = L_b/L = 0.516$

For this filter, let us define the quantity  $n$  as the ratio of the blocking capacitance  $C_b$  to the filter capacitance  $C_f$ :

$$n = \frac{C_b}{C_f} \quad (17.33)$$

For the optimum design, the peak filter output impedance occurs at the frequency

$$f_m = f_f \sqrt{\frac{2}{2+n}} \quad (17.34)$$

The value of the peak output impedance for the optimum design is

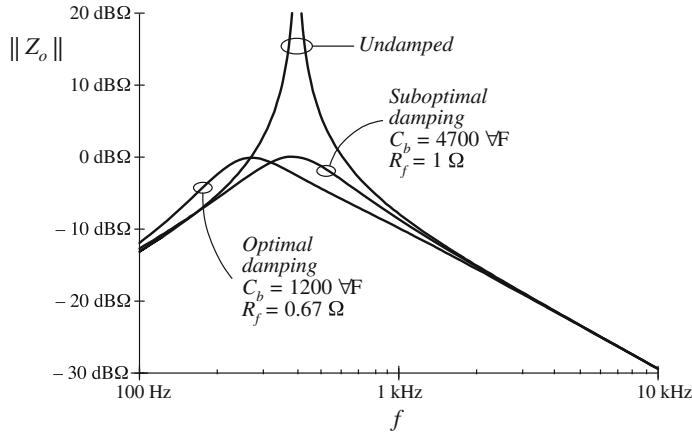
$$\|Z_o\|_{mm} = R_{0f} \frac{\sqrt{2(2+n)}}{n} \quad (17.35)$$

The value of damping resistance that leads to optimum damping is described by

$$Q_{opt} = \frac{R_f}{R_{0f}} = \sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)}} \quad (17.36)$$

The above equations allow choice of the damping values  $R_f$  and  $C_b$ .

For example, let us redesign the damping network of Sect. 17.3.2, to achieve the same peak output impedance  $\|Z_o(j\omega)\|_{mm} = 1 \Omega$ , while minimizing the value of the blocking capacitance  $C_b$ . From Sect. 17.3.2, the other parameter values are  $R_{0f} = 0.84 \Omega$ ,  $C_f = 470 \mu F$ , and  $L_f = 330 \mu H$ . First, we solve Eq. (17.35) to find the required value of  $n$ :



**Fig. 17.25** Comparison of the output impedances of the design with optimum parallel  $R_f-C_b$  damping, the suboptimal design of Sect. 17.3.2, and the original undamped filter

$$n = \frac{R_{0f}^2}{\|Z_o\|_{mm}^2} \left( 1 + \sqrt{1 + 4 \frac{\|Z_o\|_{mm}^2}{R_{0f}^2}} \right) \quad (17.37)$$

Evaluation of this expression with the given numerical values leads to  $n = 2.5$ . The blocking capacitor is therefore required to have a value of  $nC_f = 1200 \mu\text{F}$ . This is one-quarter of the value employed in Sect. 17.3.2. The value of  $R_f$  is then found by evaluation of Eq. (17.36), leading to

$$R_f = R_{0f} \sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)}} = 0.67 \Omega \quad (17.38)$$

The output impedance of this filter design is compared with the output impedances of the original undamped filter of Sect. 17.3.1, and of the suboptimal design of Sect. 17.3.2, in Fig. 17.25. It can be seen that the optimally damped filter does indeed achieve the desired peak output impedance of  $1 \Omega$ , at the slightly lower peak frequency given by Eq. (17.34).

The  $R_f-C_b$  parallel damping approach finds significant application in dc-dc converters. Since a series resistor is placed in series with  $C_b$ ,  $C_b$  can be realized using capacitor types having substantial equivalent series resistance, such as electrolytic and tantalum types. However, in some applications, the  $R_f-L_b$  approaches of the next subsections can lead to smaller designs. Also, the large blocking capacitor value may be undesirable in applications having an ac input.

#### 17.4.2 $R_f-L_b$ Parallel Damping

Figure 17.23b illustrates the placement of damping resistor  $R_f$  in parallel with inductor  $L_f$ . Inductor  $L_b$  causes the filter to exhibit a two-pole attenuation characteristic at high frequency. To allow  $R_f$  to damp the filter, inductor  $L_b$  should have an impedance magnitude that is sufficiently smaller than  $R_f$  at the filter resonant frequency  $f_f$ . Optimization of this damping network is described in [158].

With this approach, inductor  $L_b$  can be physically much smaller than  $L_f$ . Since  $R_f$  is typically much greater than the dc resistance of  $L_f$ , essentially none of the dc current flows through  $L_b$ . Furthermore,  $R_f$  could be realized as the equivalent series resistance of  $L_b$  at the filter resonant frequency  $f_f$ . Hence, this is a very simple, low-cost approach to damping the input filter.

The disadvantage of this approach is the fact that the high-frequency attenuation of the filter is degraded: the high-frequency asymptote of the filter transfer function is increased from  $1/\omega^2 L_f C_f$  to  $1/\omega^2 (L_f \| L_b) C_f$ . Furthermore, since the need for damping limits the maximum value of  $L_b$ , significant loss of high-frequency attenuation is unavoidable. To compensate, the value of  $L_f$  must be increased. Therefore, a tradeoff occurs between damping and degradation of high-frequency attenuation, as illustrated in Fig. 17.26. For example, limiting the degradation of high-frequency attenuation to 6 dB leads to an optimum peak filter output impedance  $\|Z_o\|_{mm}$  of  $\sqrt{6}$  times the original characteristic impedance  $R_{0f}$ . Additional damping leads to further degradation of the high-frequency attenuation.

The optimally damped design (i.e., the choice of  $R_f$  that minimizes the peak output impedance  $\|Z_o\|$  for a given choice of  $L_b$ ) is described by the following equations:

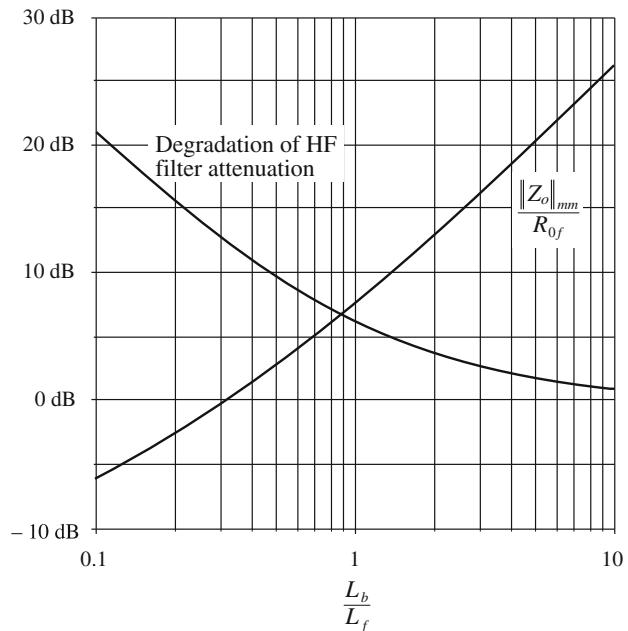
$$Q_{opt} = \frac{R_f}{R_{0f}} = \sqrt{\frac{n(3 + 4n)(1 + 2n)}{2(1 + 4n)}} \quad (17.39)$$

where

$$n = \frac{L_b}{L_f} \quad (17.40)$$

The peak filter output impedance occurs at frequency

$$f_m = f_f \sqrt{\frac{1 + 2n}{2n}} \quad (17.41)$$



**Fig. 17.26**

Performance attained via optimal design procedure, parallel  $R_f$ - $L_b$  circuit of Fig. 17.23b. Optimum peak filter output impedance  $\|Z_o\|_{mm}$  and increase of filter high-frequency gain, vs.  $n = L_b/L_f$

and has the value

$$\|Z_o\|_{mm} = R_{0f} \sqrt{2n(1 + 2n)} \quad (17.42)$$

The attenuation of the filter high-frequency asymptote is degraded by the factor

$$\frac{L_f}{L_f \|L_b\|} = 1 + \frac{1}{n} \quad (17.43)$$

So, given an undamped  $L_f-C_f$  filter having corner frequency  $f_f$ , and characteristic impedance  $R_{0f}$ , and given a requirement for the maximum allowable output impedance  $\|Z_o\|_{mm}$ , one can solve Eq. (17.42) for the required value of  $n$ . One can then determine the required numerical values of  $L_b$  and  $R_f$ .

### 17.4.3 $R_f-L_b$ Series Damping

Figure 17.23c illustrates the placement of damping resistor  $R_f$  in series with inductor  $L_f$ . Inductor  $L_b$  provides a dc bypass to avoid significant power dissipation in  $R_f$ . To allow  $R_f$  to damp the filter, inductor  $L_b$  should have an impedance magnitude that is sufficiently greater than  $R_f$  at the filter resonant frequency.

Although this circuit is theoretically equivalent to the parallel damping  $R_f-L_b$  case of Sect. 17.4.2, several differences are observed in practical designs. Both inductors must carry the full dc current, and hence both have significant size. The filter high-frequency attenuation is not affected by the choice of  $L_b$ , and the high-frequency asymptote is identical to that of the original undamped filter. The tradeoff in design of this filter does not involve high-frequency attenuation; rather, the issue is damping vs. bypass inductor size.

Design equations similar to those of the previous sections can be derived for this case. The optimum peak filter output impedance occurs at frequency

$$f_m = f_f \sqrt{\frac{2+n}{2(1+n)}} \quad (17.44)$$

and has the value

$$\|Z_o\|_{mm} = R_{0f} \frac{\sqrt{2(1+n)(2+n)}}{n} \quad (17.45)$$

The value of damping resistance that leads to optimum damping is described by

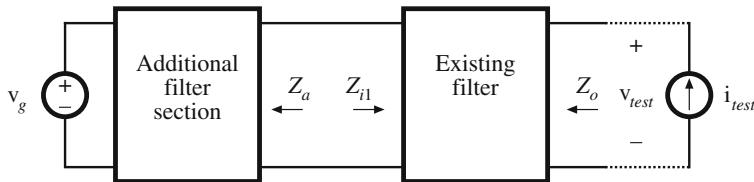
$$Q_{opt} = \frac{R_{0f}}{R_f} = \left( \frac{1+n}{n} \right) \sqrt{\frac{2(1+n)(4+n)}{(2+n)(4+3n)}} \quad (17.46)$$

For this case, the peak output impedance cannot be reduced below  $\sqrt{2}R_{0f}$  via damping. Nonetheless, it is possible to further reduce the filter output impedance by redesign of  $L_f$  and  $C_f$ , to reduce the value of  $R_{0f}$ .

#### 17.4.4 Cascading Filter Sections

A cascade connection of multiple  $L-C$  filter sections can achieve a given high-frequency attenuation with less volume and weight than a single-section  $L-C$  filter. The increased cutoff frequency of the multiple-section filter allows use of smaller inductance and capacitance values. Damping of each  $L-C$  section is usually required, which implies that damping of each section should be optimized. Unfortunately, the results of the previous sections are restricted to single-section filters. Interactions between cascaded  $L-C$  sections can lead to additional resonances and increased filter output impedance.

It is nonetheless possible to design cascaded filter sections such that interaction between  $L-C$  sections is negligible. In the approach described below, the filter output impedance is approximately equal to the output impedance of the last section, and resonances caused by interactions between stages are avoided. Although the resulting filter may not be “optimal” in any sense, insight can be gained that allows intelligent design of multiple-section filters with economical damping of each section.



**Fig. 17.27** Addition of a filter section at the input of an existing filter

Consider the addition of a filter section to the input of an existing filter, as in Fig. 17.27. Let us assume that the existing filter has been correctly designed to meet the output impedance design criteria of Eq. (17.19): under the conditions  $Z_a(s) = 0$  and  $\hat{v}_g(s) = 0$ ,  $\|Z_o\|$  is sufficiently small. It is desired to add a damped filter section that does not significantly increase  $\|Z_o\|$ .

Middlebrook’s Extra Element Theorem of Sect. 16.1 can again be invoked, to express how addition of the filter section modifies  $Z_o(s)$ :

$$Z_o(s) = \left( Z_o(s) \Big|_{Z_a(s)=0} \right) \frac{\left( 1 + \frac{Z_a(s)}{Z_{N1}(s)} \right)}{\left( 1 + \frac{Z_a(s)}{Z_{D1}(s)} \right)} \quad (17.47)$$

where

$$Z_{N1}(s) = Z_{i1}(s) \Big|_{\hat{v}_{test}(s) \rightarrow 0} \quad (17.48)$$

is the impedance at the input port of the existing filter, with its output port short-circuited. Note that, in this particular case, nulling  $\hat{v}_{test}(s)$  is the same as shorting the filter output port because the short-circuit current flows through the  $\hat{i}_{test}$  source. The quantity

$$Z_{D1}(s) = Z_{i1}(s) \Big|_{\hat{i}_{test}(s)=0} \quad (17.49)$$

is the impedance at the input port of the existing filter, with its output port open-circuited. Hence, the additional filter section does not significantly alter  $Z_o$  provided that

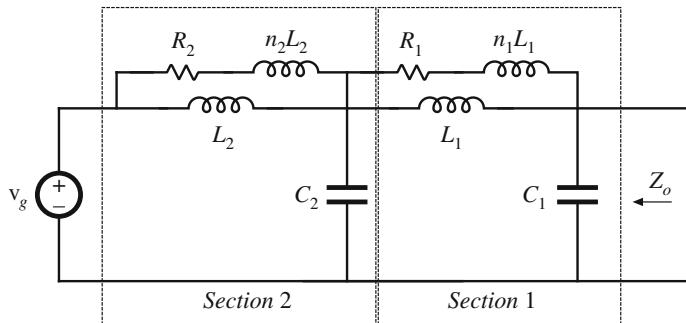
$$\begin{aligned} \|Z_a\| &\ll \|Z_{N1}\| \text{ and} \\ \|Z_a\| &\ll \|Z_{D1}\| \end{aligned} \quad (17.50)$$

Bode plots of the quantities  $Z_{N1}$  and  $Z_{D1}$  can be constructed either analytically or by computer simulation, to obtain limits of  $Z_a$ . When  $\|Z_a\|$  satisfies Eq. (17.50), then the “correction factor”  $(1 + Z_a/Z_{N1})/(1 + Z_a/Z_{D1})$  is approximately equal to 1, and the modified  $Z_o$  is approximately equal to the original  $Z_o$ .

To satisfy the design criteria (17.50), it is advantageous to select the resonant frequencies of  $Z_a$  to differ from the resonant frequencies of  $Z_{D1}$ . In other words, we should stagger-tune the filter sections. This minimizes the interactions between filter sections, and can allow use of smaller reactive element values.

#### 17.4.5 Example: Two Stage Input Filter

As an example, let us consider the design of a two-stage filter using  $R_f-L_b$  parallel damping in each section as illustrated in Fig. 17.28 [158]. It is desired to achieve the same attenuation as the single-section filters designed in Sects. 17.3.2 and 17.4.1, and to filter the input current of the same buck converter example of Fig. 17.11. These filters exhibit an attenuation of 80 dB at 250 kHz, and satisfy the design inequalities of Eq. (17.19) with the  $\|Z_N\|$  and  $\|Z_D\|$  impedances of Fig. 17.13. Hence, let us design the filter of Fig. 17.28 to attain 80 dB of attenuation at 250 kHz.



**Fig. 17.28** Two-section input filter example, employing  $R_f-L_b$  parallel damping in each section

As described in the previous section and below, it is advantageous to stagger-tune the filter sections so that interaction between filter sections is reduced. We will find that the cut-off frequency of filter section 1 should be chosen to be smaller than the cutoff frequency of section 2. In consequence, the attenuation of section 1 will be greater than that of section 2. Let us (somewhat arbitrarily) design to obtain 45 dB of attenuation from section 1, and

35 dB of attenuation from section 2 (so that the total is the specified 80 dB). Let us also select  $n_1 = n_2 = n = L_b/L_f = 0.5$  for each section; as illustrated in Fig. 17.26, this choice leads to a good compromise between damping of the filter resonance and degradation of high frequency filter attenuation. Equation (17.43) and Fig. 17.26 predict that the  $R_f-L_b$  damping network will degrade the high-frequency attenuation by a factor of  $(1+1/n) = 3$ , or 9.5 dB. Hence, the section 1 undamped resonant frequency  $f_{f1}$  should be chosen to yield  $45 \text{ dB} + 9.5 \text{ dB} = 54.5 \text{ dB} \Rightarrow 533$  of attenuation at 250 kHz. Since section 1 exhibits a two-pole ( $-40 \text{ dB/decade}$ ) roll-off at high frequencies,  $f_{f1}$  should be chosen as follows:

$$f_{f1} = \frac{(250 \text{ kHz})}{\sqrt{533}} = 10.8 \text{ kHz} \quad (17.51)$$

Note that this frequency is well above the 1.6 kHz resonant frequency  $f_0$  of the buck converter output filter. Consequently, the output impedance  $\|Z_o\|$  can be as large as  $3 \Omega$ , and still be well below the  $\|Z_N(j\omega)\|$  and  $\|Z_D(j\omega)\|$  plots of Fig. 17.13.

Solution of Eq. (17.42) for the required section 1 characteristic impedance that leads to a peak output impedance of  $3 \Omega$  with  $n = 0.5$  leads to

$$R_{0f1} = \frac{\|Z_o\|_{\text{mm}}}{\sqrt{2n(1+2n)}} = \frac{3 \Omega}{\sqrt{2(0.5)(1+2(0.5))}} = 2.12 \Omega \quad (17.52)$$

The filter inductance and capacitance values are therefore

$$\begin{aligned} L_1 &= \frac{R_{0f1}}{2\pi f_{f1}} = 31.2 \mu\text{H} \\ C_1 &= \frac{1}{2\pi f_{f1} R_{0f1}} = 6.9 \mu\text{F} \end{aligned} \quad (17.53)$$

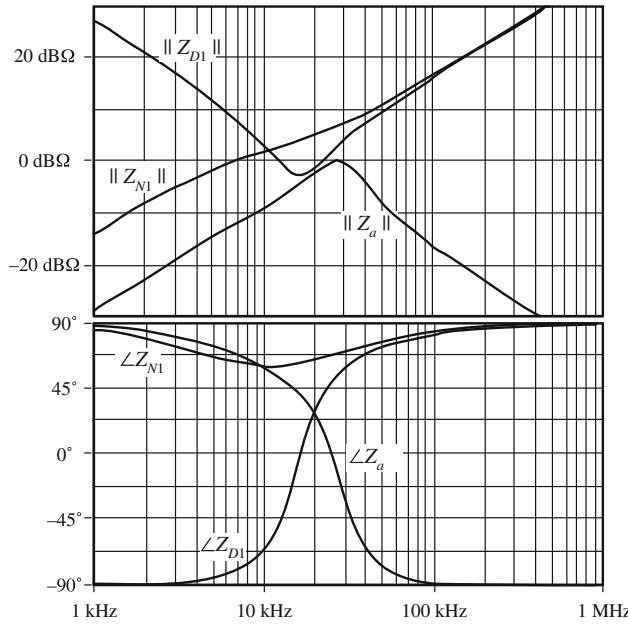
The section 1 damping network inductance is

$$n_1 L_1 = 15.6 \mu\text{H} \quad (17.54)$$

The section 1 damping resistance is found from Eq. (17.39):

$$R_1 = Q_{opt} R_{0f1} = R_{0f1} \sqrt{\frac{n(3+4n)(1+2n)}{2(1+4n)}} = 1.9 \Omega \quad (17.55)$$

The peak output impedance will occur at the frequency given by Eq. (17.41), 15.3 kHz. The quantities  $\|Z_{N1}(j\omega)\|$  and  $\|Z_{D1}(j\omega)\|$  for filter section 1 can now be constructed analytically or plotted by computer simulation.  $\|Z_{N1}(j\omega)\|$  is the section 1 input impedance  $Z_{i1}$  with the output of section 1 shorted, and is given by the parallel combination of the  $sL_1$  and the  $(R_1 + sn_1 L_1)$  branches.  $\|Z_{D1}(j\omega)\|$  is the section 1 input impedance  $Z_{i1}$  with the output of section 1 open-circuited, and is given by the series combination of  $Z_{N1}(s)$  with the capacitor impedance  $1/sC_1$ . Figure 17.29 contains plots of  $\|Z_{N1}(j\omega)\|$  and  $\|Z_{D1}(j\omega)\|$  for filter section 1, generated using Spice.



**Fig. 17.29** Bode plot of  $Z_{N1}$  and  $Z_{N2}$  for filter section 1. Also shown is the Bode plot for the output impedance  $Z_a$  of filter section 2

One way to approach design of filter section 2 is as follows. To avoid significantly modifying the overall filter output impedance  $Z_o$ , the section 2 output impedance  $\|Z_a(j\omega)\|$  must be sufficiently less than  $\|Z_{N1}(j\omega)\|$  and  $\|Z_{D1}(j\omega)\|$ . It can be seen from Fig. 17.29 that, with respect to  $\|Z_{D1}(j\omega)\|$ , this is most difficult to accomplish when the peak frequencies of sections 1 and 2 coincide. It is most difficult to satisfy the  $\|Z_{N1}(j\omega)\|$  design criterion when the peak frequency of sections 2 is lower than the peak frequency of section 1. Therefore, the best choice is to stagger-tune the filter sections, with the resonant frequency of section 1 being lower than the peak frequency of section 2. This implies that section 1 will produce more high-frequency attenuation than section 2. For this reason, we have chosen to achieve 45 dB of attenuation with section 1, and 35 dB of attenuation from section 2.

The section 2 undamped resonant frequency  $f_{f2}$  should be chosen in the same manner used in Eq. (17.51) for section 1. We have chosen to select  $n_2 = n = L_b/L_f = 0.5$  for section 2; this again means that the  $R_f-L_b$  damping network will degrade the high-frequency attenuation by a factor of  $(1 + 1/n) = 3$ , or 9.5 dB. Hence, the section 2 undamped resonant frequency  $f_{f2}$  should be chosen to yield  $35 \text{ dB} + 9.5 \text{ dB} = 44.5 \text{ dB} \Rightarrow 169$  of attenuation at 250 kHz. Since section 2 exhibits a two-pole (-40 dB/decade) roll-off at high frequencies,  $f_{f2}$  should be chosen as follows:

$$f_{f2} = \frac{(250 \text{ kHz})}{\sqrt{169}} = 19.25 \text{ kHz} \quad (17.56)$$

The output impedance of section 2 will peak at the frequency 27.2 kHz, as given by Eq. (17.41). Hence, the peak frequencies of sections 1 and 2 differ by almost a factor of 2.

Figure 17.29 shows that, at 27.2 kHz,  $\|Z_{D1}(j\omega)\|$  has a magnitude of roughly 3 dBΩ, and that  $\|Z_{N1}(j\omega)\|$  is approximately 7 dBΩ. Hence, let us design section 2 to have a peak output impedance of 0 dBΩ  $\Rightarrow 1 \Omega$ . Solution of Eq. (17.42) for the required section 2 characteristic impedance leads to

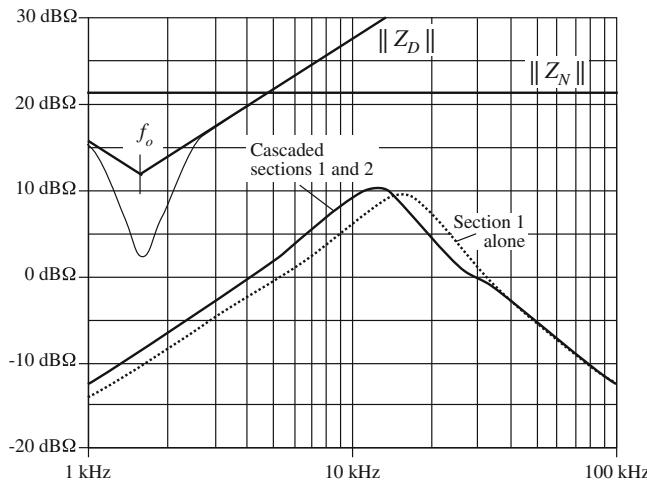
$$R_{0f2} = \frac{\|Z_a\|_{mm}}{\sqrt{2n(1+2n)}} = \frac{1 \Omega}{\sqrt{2(0.5)(1+2(0.5))}} = 0.71 \Omega \quad (17.57)$$

The section 2 element values are therefore

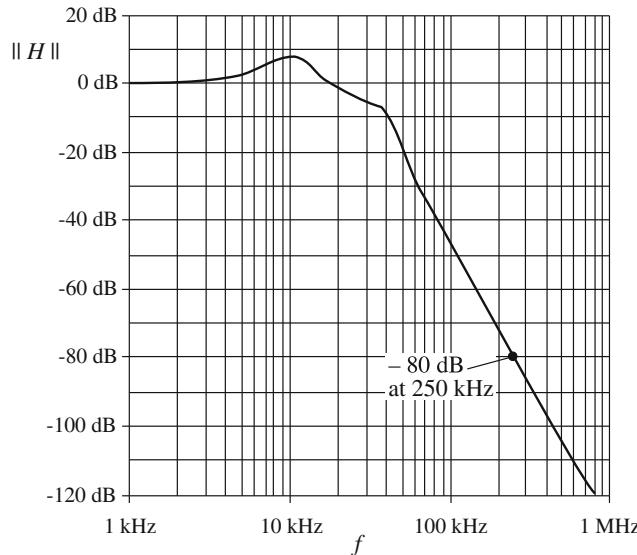
$$\begin{aligned} L_2 &= \frac{R_{0f2}}{2\pi f_{f2}} = 5.8 \mu\text{H} \\ C_2 &= \frac{1}{2\pi f_{f2} R_{0f2}} = 11.7 \mu\text{F} \\ n_2 L_2 &= 2.9 \mu\text{H} \\ R_2 &= Q_{opt} R_{0f2} = R_{0f2} \sqrt{\frac{n(3+4n)(1+2n)}{2(1+4n)}} = 0.65 \Omega \end{aligned} \quad (17.58)$$

A Bode plot of the resulting  $Z_a$  is overlaid on Fig. 17.29. It can be seen that  $\|Z_a(j\omega)\|$  is less than, but very close to,  $\|Z_{D1}(j\omega)\|$  between the peak frequencies of 15 kHz and 27 kHz. The impedance inequalities (17.50) are satisfied somewhat better below 15 kHz, and are satisfied very well at high frequency.

The resulting filter output impedance  $\|Z_o(j\omega)\|$  is plotted in Fig. 17.30, for section 1 alone and for the complete cascaded two-section filter. It can be seen that the peak output impedance



**Fig. 17.30** Comparison of the impedance design criteria  $\|Z_N(j\omega)\|$  and  $\|Z_D(j\omega)\|$ , Eq. (17.19), with the filter output impedance  $\|Z_o(j\omega)\|$ . Solid line:  $\|Z_o(j\omega)\|$  of cascaded design. Dashed line:  $\|Z_o(j\omega)\|$  of section 1 alone



**Fig. 17.31** Input filter transfer function, cascaded two-section design

is approximately  $10 \text{ dB}\Omega$ , or roughly  $3 \Omega$ . The impedance design criteria (17.19) are also shown, and it can be seen that the filter meets these design criteria. Note the absence of resonances in  $\|Z_o(j\omega)\|$ .

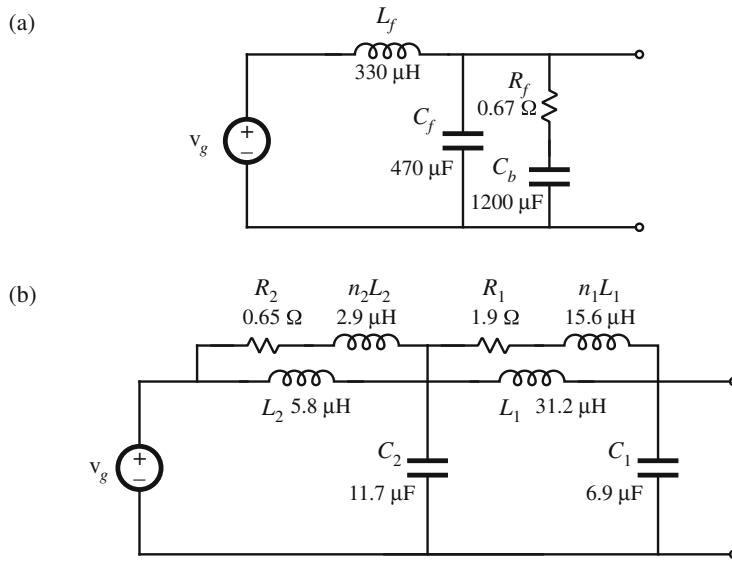
The effect of stage 2 on  $\|Z_o(j\omega)\|$  is very small above 40 kHz (where inequalities (17.50) are very well satisfied), and has moderate-to-small effect at lower frequencies. It is interesting that, above approximately 12 kHz, the addition of stage 2 actually *decreases*  $\|Z_o(j\omega)\|$ . The reason for this can be seen from Fig. 16.8: when the phase difference between  $\angle Z_a(j\omega)$  and  $\angle Z_{D1}(j\omega)$  is not too large ( $\leq 90^\circ$ ), then the  $1/(1 + Z_a/Z_{D1})$  term decreases the magnitude of the resulting  $\|Z_o(j\omega)\|$ . As can be seen from the phase plot of Fig. 17.29, this is indeed what happens. So allowing  $\|Z_a(j\omega)\|$  to be similar in magnitude to  $\|Z_{D1}(j\omega)\|$  above 12 kHz was an acceptable design choice.

The resulting filter transfer function is illustrated in Fig. 17.31. It can be seen that it does indeed attain the goal of 80 dB attenuation at 250 kHz.

Figure 17.32 compares the single-stage design of Sect. 17.4.1 to the two-stage design of this section. Both designs attain 80 dB attenuation at 250 kHz, and both designs meet the impedance design criteria of Eq. (17.19). However, the single-stage approach requires much larger filter elements.

## 17.5 Stability Criteria

In the previous sections, Middlebrook's Extra Element Theorem has been employed to gain insight into how the addition of an input filter changes the transfer functions of a converter. Impedance inequalities such as those discussed in Sect. 17.2.3 yield insight into how to shape the filter output impedance so that addition of the input filter does not substantially change the converter transfer functions  $G_{vd}(s)$ ,  $G_{vg}(s)$ , and  $Z_{out}(s)$ . Hence we expect that addition of an



**Fig. 17.32** Comparison of single-section (a) and two-section (b) input filter designs. Both designs meet the design criteria (17.19), and both exhibit 80 dB of attenuation at 250 kHz

input filter meeting the impedance inequalities will not change the stability of a well-designed switching regulator. In this sense, the impedance inequalities can be viewed as design criteria that may be conservative.

By themselves, the impedance inequalities of Sect. 17.2.3 do not define the stability boundary of a closed-loop system, because these inequalities do not depend on the actual loop gain  $T(s)$ . So far, we have applied the Extra Element Theorem only to the open-loop transfer functions such as  $G_{vd}(s)$ . To determine the stability of a closed-loop switching regulator with input filter, we need to further investigate how alteration of the transfer functions of the converter power stage affects the stability and phase margin of the loop gain  $T(s)$ .

One straightforward approach is to plot the modified loop gain including the modified  $G_{vd}(s)$  of Eq. (17.4), and then apply the usual stability tests such as the phase margin test to the result. The modified  $G_{vg}(s)$  and  $Z_{out}(s)$  can be plotted as well, to check whether these quantities continue to meet the design goals. This approach is discussed in Sect. 17.5.1.

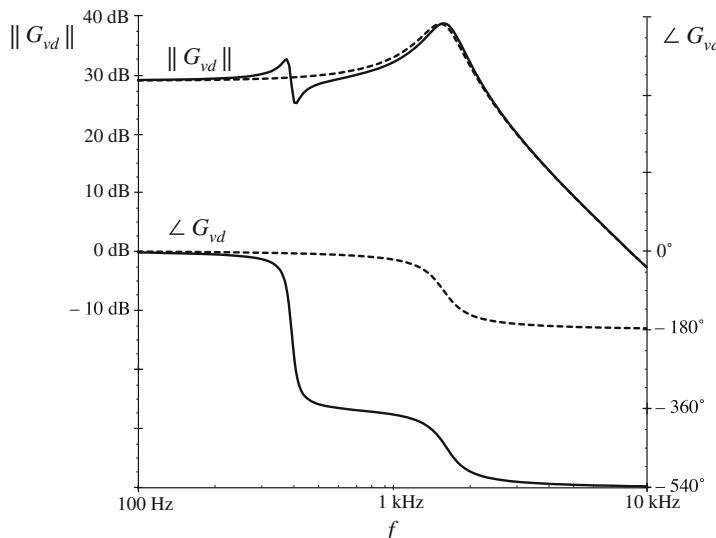
A second approach is based on comparison of the input filter source impedance  $Z_o(s)$  with the converter closed-loop input impedance  $Z_i(s)$  [151]. This approach expresses the stability boundary directly in terms of  $Z_o(s)$ . The loading of the input filter by  $Z_i(s)$  leads to a voltage divider term

$$\frac{Z_i}{Z_i + Z_o} \quad (17.59)$$

that can contain RHP poles, and is the origin of the stability problem. Section 17.5.2 contains a derivation and an example. The approaches of Sects. 17.5.1 and 17.5.2 give identical predictions of the stability boundary.

### 17.5.1 Modified Phase Margin

Let us consider again the buck converter example of Sect. 17.3. The effect of the addition of an undamped  $L-C$  input filter on the control-to-output transfer function  $G_{vd}(s)$  is illustrated in Fig. 17.18, repeated in Fig. 17.33. It can be seen that  $G_{vd}$  is substantially unchanged below the input filter resonance at 400 Hz, but  $G_{vd}$  contains an additional  $360^\circ$  of phase lag above 400 Hz. The undamped input filter violates the inequalities of Eq. (17.19) in the vicinity of 400 Hz.

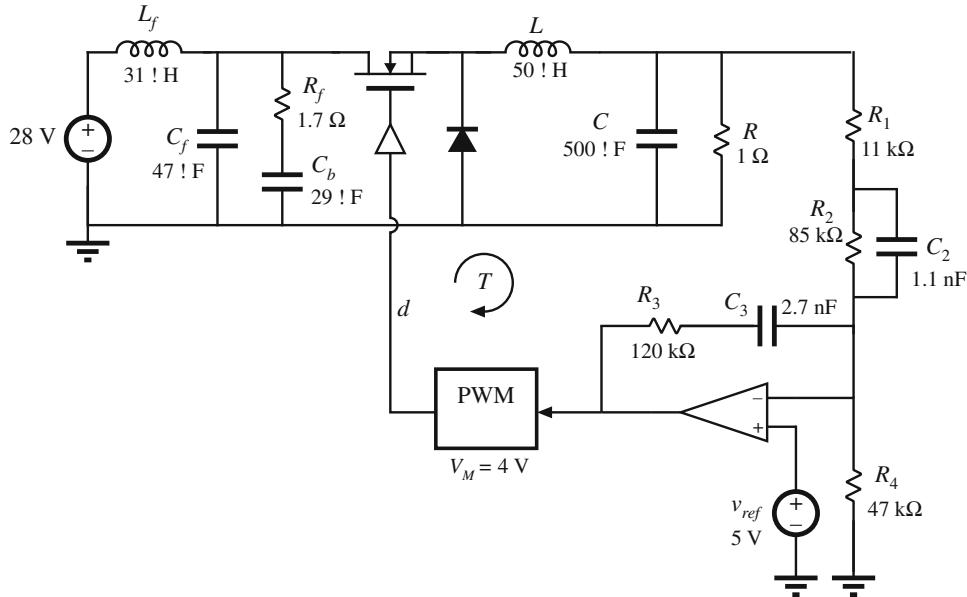


**Fig. 17.33** Effect of undamped input filter on the control-to-output transfer function  $G_{vd}(s)$  of the buck converter example. *Dashed lines:* without input filter. *Solid lines:* with undamped input filter

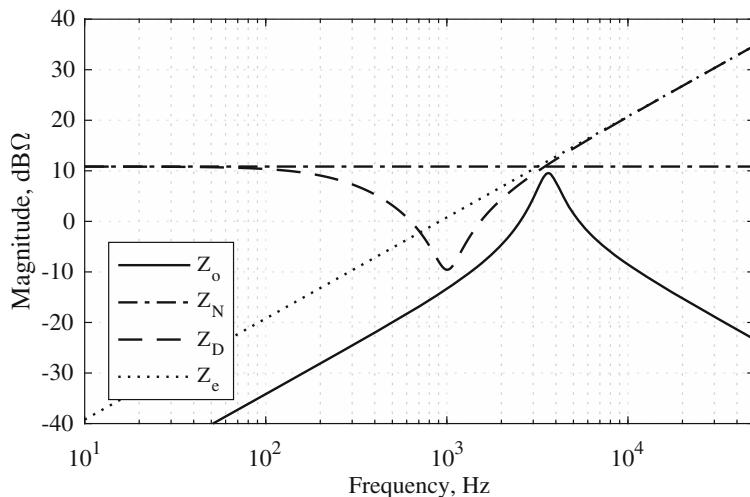
If this converter and input filter are employed in a closed-loop regulator system having a loop crossover frequency  $f_c$  well below the input filter resonance at 400 Hz, then the phase margin of the loop gain  $T(s)$  will be essentially unchanged by the input filter and the loop will be stable. Violation of the impedance inequalities is irrelevant because the violation occurs outside the bandwidth of the loop. Conversely, if the loop crossover frequency  $f_c$  is near to or greater than 400 Hz, then addition of the undamped input filter will decrease the phase margin of the loop gain  $T(s)$  by as much as  $-360^\circ$ , which would lead to a negative phase margin and instability.

Hence, one approach to determination of the stability boundary is to employ the modified  $G_{vd}(s)$  to plot the modified loop gain and find its phase margin. As an example, let us consider the closed-loop buck regulator with PID compensator designed in Sect. 9.5.4. Figure 17.34 illustrates this closed-loop system, with an added single-section input filter and  $R_f-C_b$  damping network.

Figure 17.35 contains a plot of the magnitude of the input filter source (output) impedance  $Z_o$ , along with the impedances  $Z_N$ ,  $Z_D$ , and  $Z_e$  from Table 17.1, using the numerical values specified in Fig. 17.34. It can be observed that  $\|Z_o\|$  is indeed less than  $\|Z_N\|$ ,  $\|Z_D\|$ , and  $\|Z_e\|$  at



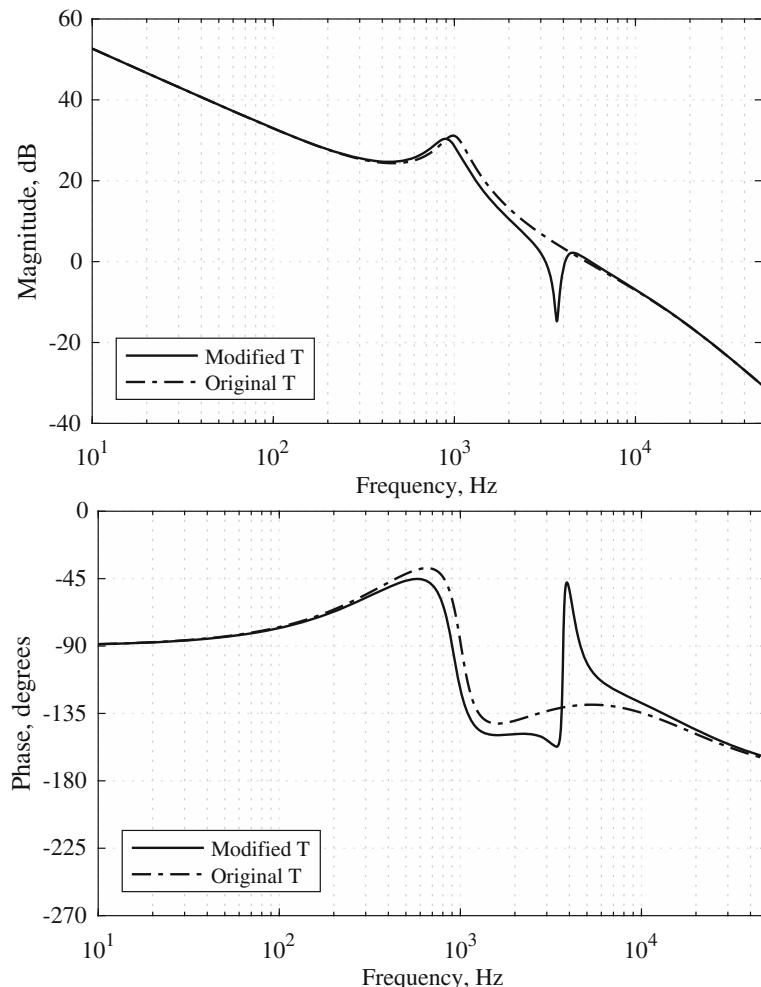
**Fig. 17.34** Closed-loop buck regulator with PID compensator, Sect. 9.5.4, with a damped input filter



**Fig. 17.35** Impedance inequalities for the regulator of Fig. 17.34

all frequencies, although the impedances are close in magnitude in the vicinity of the resonances of the input filter (approximately 4 kHz) and the converter output filter (1 kHz).

The original and modified loop gains are plotted in Fig. 17.36. It can be observed that the effect of the input filter on the loop gain is moderate, and the loop continues to be stable. Nonetheless, changes are observed at frequencies where  $\|Z_o\|$  approaches  $\|Z_N\|$  or  $\|Z_D\|$ . At or above the 1

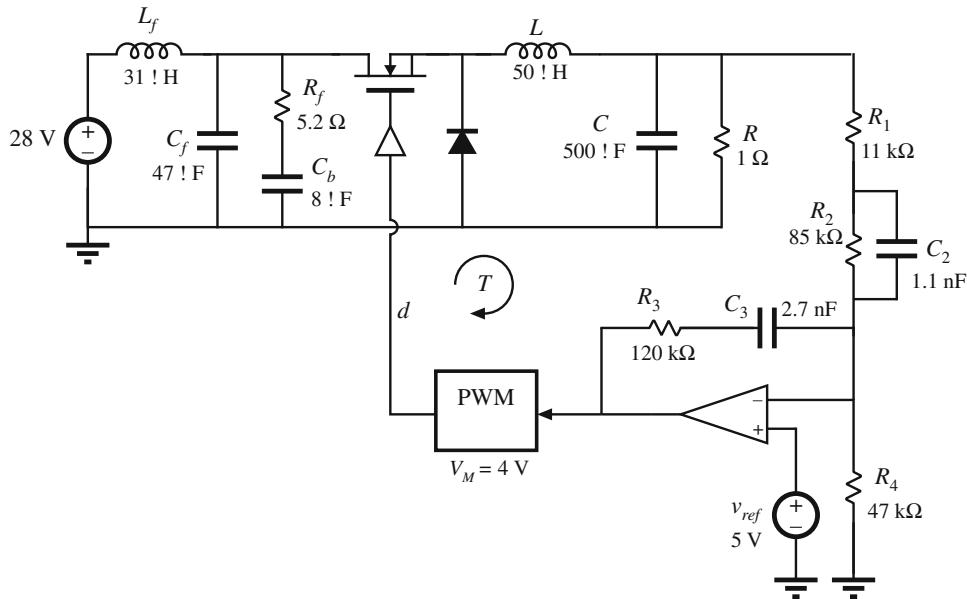


**Fig. 17.36** Modification of the loop gain magnitude and phase by the input filter, for the buck regulator of Fig. 17.34

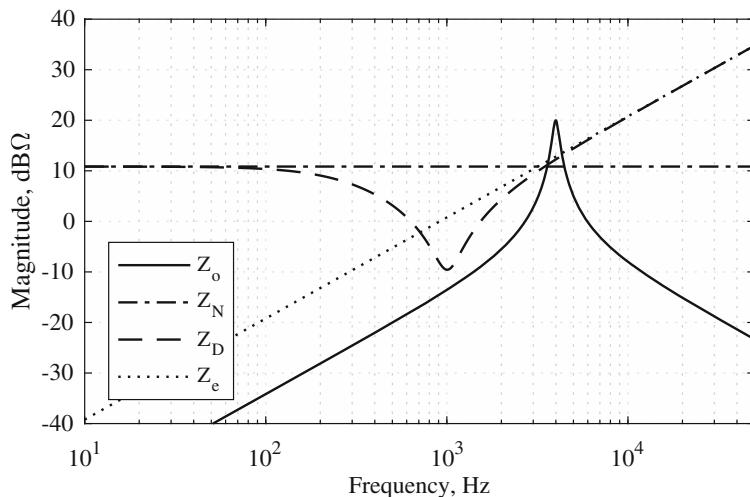
kHz resonant frequency of the buck output filter, the magnitude and phase of the loop gain  $T(s)$  are somewhat reduced. Resonant (LHP) zeroes are introduced into  $T(s)$  at the approximately 4 kHz resonance of the input filter, which cause the loop to exhibit three crossover frequencies. The loop also contains a pair of damped poles near 4 kHz. The phase margin is reduced, but is still positive, and the loop continues to be stable.

Again, it should be noted that  $\|Z_o\| < \|Z_N\|$  is not the stability condition, but rather stability is deduced from the loop gain plot.

Figure 17.37 illustrates modification of the input filter damping network, such that the peak  $\|Z_o\|$  is increased. The impedance magnitudes for this case are plotted in Fig. 17.38. It can be seen that the input filter  $\|Z_o\|$  now significantly exceeds  $\|Z_N\|$  and  $\|Z_D\|$  at the input filter resonant

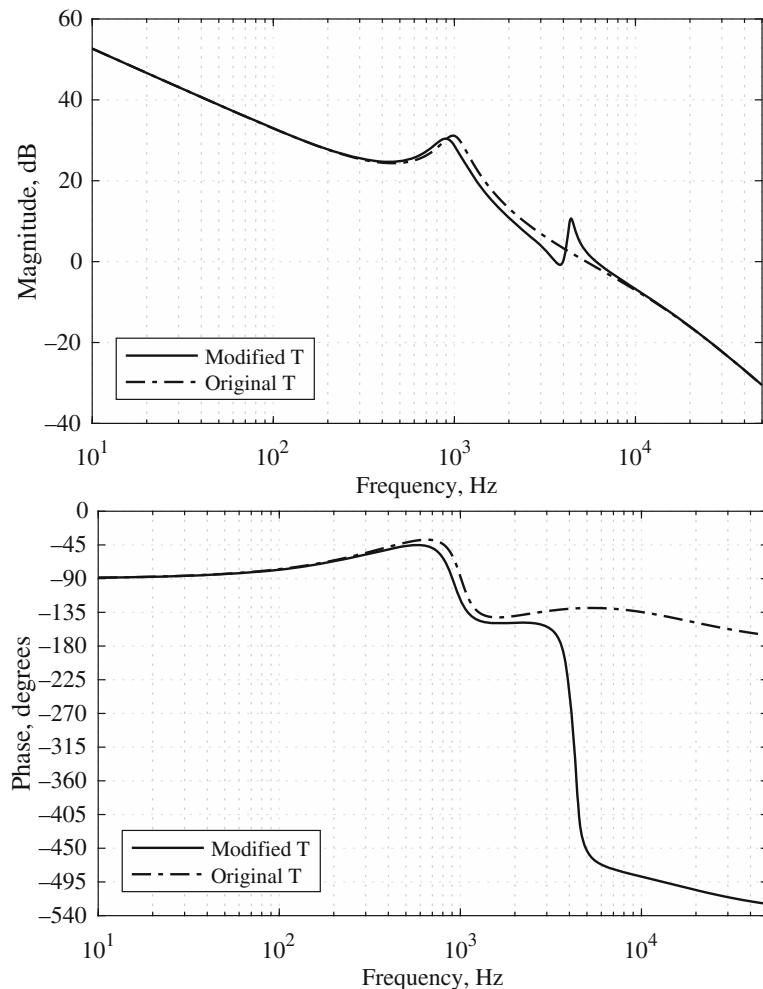


**Fig. 17.37** Modification of the input filter of Fig. 17.34 to reduce its damping



**Fig. 17.38** Impedance inequalities for the regulator of Fig. 17.37

frequency of 4 kHz. The resulting loop gain magnitude and phase is plotted in Fig. 17.39. The correction factor in Eq. (17.4) introduces resonant RHP zeroes and resonant poles into  $T(s)$ , at the input filter resonant frequency. This adds an additional  $360^\circ$  of phase lag at frequencies above 4 kHz. At the loop crossover frequency of 7 kHz, the phase margin is negative. Hence, the converter feedback loop is unstable.



**Fig. 17.39** Modification of the loop gain magnitude and phase by the input filter, for the buck regulator of Fig. 17.37

In summary, the impedance inequalities of Sect. 17.2.3 provide conditions that guarantee that the loop gain and other important quantities are unchanged by addition of an input filter. The actual stability boundary is determined by plotting the modified loop gain, and then applying the usual stability tests such as the phase margin test. In the examples of this section, the correction factor (Eq. (17.18)) leads to decrease of the magnitude and phase of the loop gain in the vicinity of the crossover frequency. In the example in which damping of the input filter was inadequate, this led to a negative phase margin and instability.

### 17.5.2 Closed-Loop Input Impedance

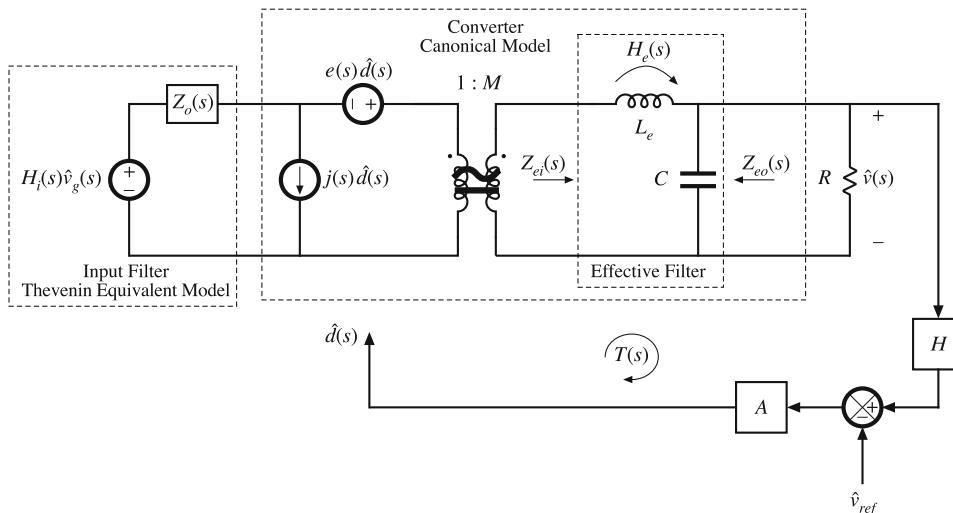
Another useful approach for determination of the exact stability boundary is based on the loading of the input filter by the closed-loop converter input impedance  $Z_i(s)$ . This loading leads to a voltage divider term

$$\frac{Z_i(s)}{Z_i(s) + Z_o(s)} = \frac{1}{1 + \frac{Z_o(s)}{Z_i(s)}} \quad (17.60)$$

that introduces new poles into the closed-loop transfer functions of the system [151]. It is possible that these new poles lie in the right half-plane, and this can be viewed as the mechanism by which addition of an input filter destabilizes the regulator. In this section, the Extra Element Theorem is employed to derive how the input filter adds the additional term (17.60) to a closed-loop transfer function of the system; the closed-loop audiosusceptibility  $\hat{v}/\hat{v}_g$  is used as an example but all closed-loop transfer functions of the network contain the same poles. Second, the Feedback Theorem is employed to find an expression for the closed-loop input impedance  $Z_i(s)$ . Finally, the stability of Eq. (17.60) is examined by treating  $T_m(s) = Z_o(s)/Z_i(s)$  as a minor loop gain whose stability can be determined using conventional techniques such as the Nyquist stability theorem and the phase margin test.

#### Effect of input filter on closed-loop transfer functions

Figure 17.40 illustrates the small-signal model of a system composed of a CCM switching converter, its feedback system, and an input filter. A Thevenin-equivalent circuit models the output port of the input filter, having output impedance  $Z_o(s)$ . The transfer function of the unloaded input filter is  $H_i(s)$ , and the voltage applied to the input port of the input filter is  $\hat{v}_g(s)$ . The converter power stage is modeled using the canonical model of Sect. 7.4. The compensator and PWM transfer functions are combined into gain block  $A(s)$ .



**Fig. 17.40** Small-signal model of a closed-loop converter system with input filter

In the case of no input filter,  $Z_o(s) = 0$  and  $H_i(s) = 1$ . Under these conditions, the “original” closed-loop transfer functions can be found using the Feedback Theorem, in a manner similar to that employed in Sect. 13.4. The “original” loop gain is found to be

$$T(s) = A(s)e(s)MH_e(s)H(s) \quad (17.61)$$

The “original” audiosusceptibility is

$$G_{vg}(s) = \frac{MH_e(s)}{1 + T(s)} \quad (17.62)$$

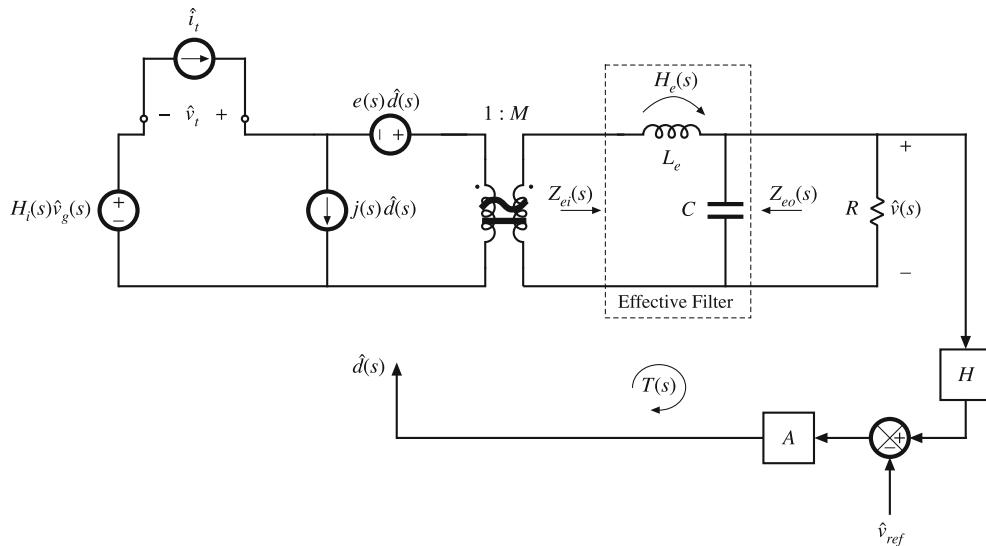
This coincides with the result of Eq. (13.103). In the presence of the input filter, the Extra Element Theorem predicts that the audiosusceptibility becomes

$$G'_{vg}(s) = H_i(s)G_{vg}(s) \frac{1 + \frac{Z_o}{Z_{Ng}}}{1 + \frac{Z_o}{Z_{Dg}}} \quad (17.63)$$

Figure 17.41 illustrates use of the Extra Element Theorem to find the modified audiosusceptibility  $G'_{vg}(s)$ . The Thevenin impedance  $Z_o(s)$  is treated as the extra element, and current  $\hat{i}_t$  is injected at the  $Z_o$  port.

The impedance  $Z_{Ng}$  is the impedance seen at the injection port, when  $\hat{i}_t$  and  $\hat{v}_{in}$  are adjusted such that the output voltage  $\hat{v}$  is nulled. The reference variation  $\hat{v}_{ref}$  is also set to zero:

$$Z_{Ng} = \left. \frac{\hat{v}_t}{\hat{i}_t} \right|_{\begin{subarray}{l} \hat{v} \rightarrow 0 \\ \hat{v}_{ref} = 0 \end{subarray}} \quad (17.64)$$



**Fig. 17.41** Use of the Extra Element Theorem to find the modified  $G'_{vg}(s)$

When  $\hat{v}$  is nulled, with  $\hat{v}_{ref}$  set to zero, the duty-cycle variation  $\hat{d}$  also becomes zero. Hence, the  $e(s)\hat{d}$  and  $j(s)\hat{d}$  sources are zero. Additionally, the null condition of  $\hat{v}$  causes zero-current variation in the load and in the  $C$  and  $L_e$  elements, so that there is no voltage across the transformer windings and no current through the transformer windings. Hence the null condition implies that  $\hat{i}_t = 0$  and  $\hat{v}_t = -H_i\hat{v}_{in}$ . Therefore  $Z_{Ng}$  is

$$Z_{Ng} = \frac{-H_i\hat{v}_{in}}{0} = \infty \quad (17.65)$$

$Z_{Ng}$  is an open circuit, and the numerator term of the correction factor (17.63) equals  $(1+0) = 1$ .

The impedance  $Z_{Dg}$  is the impedance seen at the injection port, when  $\hat{v}_{in}$  and  $\hat{v}_{ref}$  are set to zero:

$$Z_{Dg} = \left. \frac{\hat{v}_t}{\hat{i}_t} \right|_{\begin{subarray}{l} \hat{v}_{in}=0 \\ \hat{v}_{ref}=0 \end{subarray}} \quad (17.66)$$

The quantity  $Z_{Dg}$  is seen to be the closed-loop input impedance  $Z_i$  of the regulator. Hence, the closed-loop audiosusceptibility in Eq. (17.63) is

$$G'_{vg}(s) = H_i(s)G_{vg}(s) \frac{1}{\left(1 + \frac{Z_o}{Z_i}\right)} \quad (17.67)$$

A similar analysis can show that the modified closed-loop output impedance contains the same correction factor denominator term [151].

How can addition of an input filter to a stable closed-loop regulator lead to instability, *i.e.*, closed-loop transfer function poles in the right half of the complex plane? In Eq. (17.67), the quantity  $G_{vg}(s)$  is the closed-loop audiosusceptibility of the original regulator; we assume that the original regulator was correctly designed so that  $G_{vg}(s)$  is stable and contains no right half-plane poles. The quantity  $H_i$  is the unloaded transfer function of the filter, which we also assume contains no right half-plane poles since the filter is a passive network. Hence the only term that can lead to instability is the denominator correction factor term

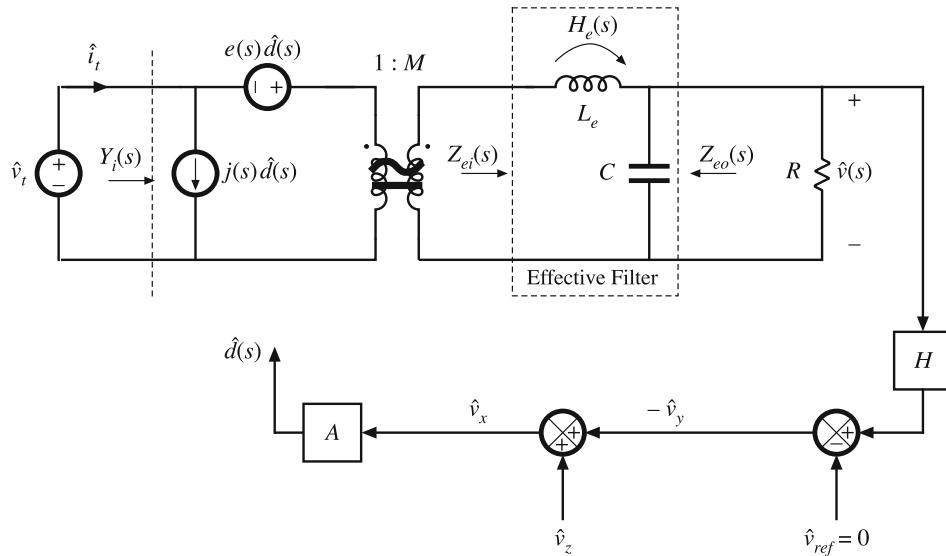
$$\frac{1}{\left(1 + \frac{Z_o}{Z_i}\right)} = \frac{1}{(1 + T_m)} \quad (17.68)$$

The term in Eq. (17.68) is the origin of potential instability caused by addition of the input filter. The denominator correction factor term assumes the same mathematical form as a closed-loop transfer function, effectively with “minor loop gain”  $T_m = Z_o/Z_i$ , and it is possible for the  $(1+T_m)$  term to contain right half-plane roots. Hence the usual stability tests such as the Nyquist stability criterion or phase margin tests can be applied to  $T_m$ .

### Finding the closed-loop input admittance $Y_i = 1/Z_{Dg}$

We can apply the Feedback Theorem of Chap. 13 as illustrated in Fig. 17.42. A test source  $\hat{v}_t$  is injected at the power input port of the small-signal model, and the converter input current  $\hat{i}_t$  is measured. The input admittance is the transfer function from  $\hat{v}_t$  to  $\hat{i}_t$ :

$$Y_i = \frac{\hat{i}_t}{\hat{v}_t} \quad (17.69)$$



**Fig. 17.42** Use of the Feedback Theorem to find the closed-loop input admittance  $Y_i = 1/Z_{Dg}$

To determine the closed-loop  $Y_i$ , source  $\hat{v}_z$  is injected after the summing node, and the Feedback Theorem is applied to express  $Y_i$  as

$$Y_i = Y_{i\infty} \frac{T}{1+T} + Y_{i0} \frac{1}{1+T} \quad (17.70)$$

The gain  $Y_{i\infty}$  is given by

$$Y_{i\infty}(s) = \left. \frac{\hat{i}_t(s)}{\hat{v}_t(s)} \right|_{\begin{subarray}{l} \hat{v}_{ref}=0 \\ \hat{v}_y \rightarrow 0 \end{subarray}} \quad (17.71)$$

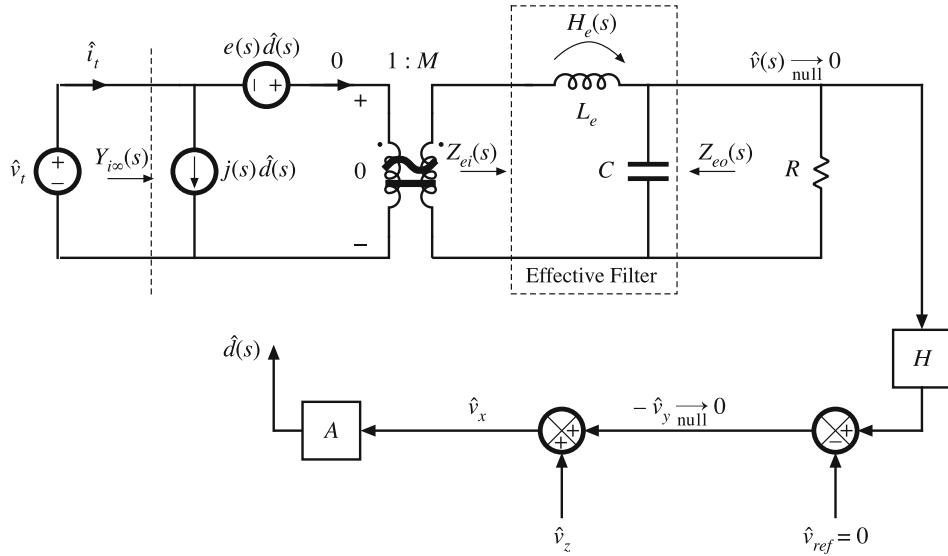
The loop reference variation  $\hat{v}_{ref}$  is set to zero. In the presence of the test source  $\hat{v}_t$ , the signal  $\hat{v}_z$  is adjusted to null  $\hat{v}_y$ . Figure 17.43 illustrates solution of the model under these conditions.

With the reference  $\hat{v}_{ref}$  set to zero, the nulling of  $\hat{v}_y$  implies that the output voltage  $\hat{v}$  is also nulled. Hence the current through the load resistance  $R$  is nulled. Hence the currents in the effective filter elements are nulled, and there must be zero voltage across the transformer secondary. This implies that there is zero voltage across the transformer primary, and zero current through the  $e(s)\hat{d}$  source. So under the null conditions, the test voltage must be  $\hat{v}_t = -e(s)\hat{d}$ , and the test current must be  $\hat{i}_t = j(s)\hat{d}$ . This leads to the result

$$Y_{i\infty} = \frac{j(s)\hat{d}}{-e(s)\hat{d}} = -\frac{j(s)}{e(s)} \quad (17.72)$$

For the buck converter, this expression reduces to

$$Y_{i\infty} = -\frac{M^2}{R} \quad (17.73)$$



**Fig. 17.43** Determination of  $Y_{i\infty}$

At frequencies where the loop gain  $T$  is large in magnitude, the converter closed-loop incremental input admittance  $Y_i$  is negative. The quantity  $1/Y_{i\infty}$  coincides with the  $Z_N$  listed in Table 17.1; when the loop gain is large then the converter closed-loop input impedance follows  $Z_N$ .

The gain  $Y_{i0}$  is given by

$$Y_{i0}(s) = \left. \frac{\hat{i}_t(s)}{\hat{v}_t(s)} \right|_{\begin{subarray}{l} \hat{v}_{ref}=0 \\ \hat{v}_x \rightarrow 0 \\ \hat{v}_y \rightarrow 0 \end{subarray}} \quad (17.74)$$

The loop reference variation  $\hat{v}_{ref}$  is set to zero. In the presence of the test source  $\hat{v}_t$ , the signal  $\hat{v}_z$  is adjusted such that  $\hat{v}_x$  is nulled. Figure 17.44 illustrates solution of the model under these conditions.

With  $\hat{v}_x$  equal to zero, the duty-cycle variation  $\hat{d}$  is zero. Hence the canonical model sources  $e(s)\hat{d}$  and  $j(s)\hat{d}$  become zero. The converter input admittance  $Y_{i0}$  is then the effective filter input admittance  $1/Z_{ei}(s)$ , reflected through the transformer turns ratio  $M^2$ :

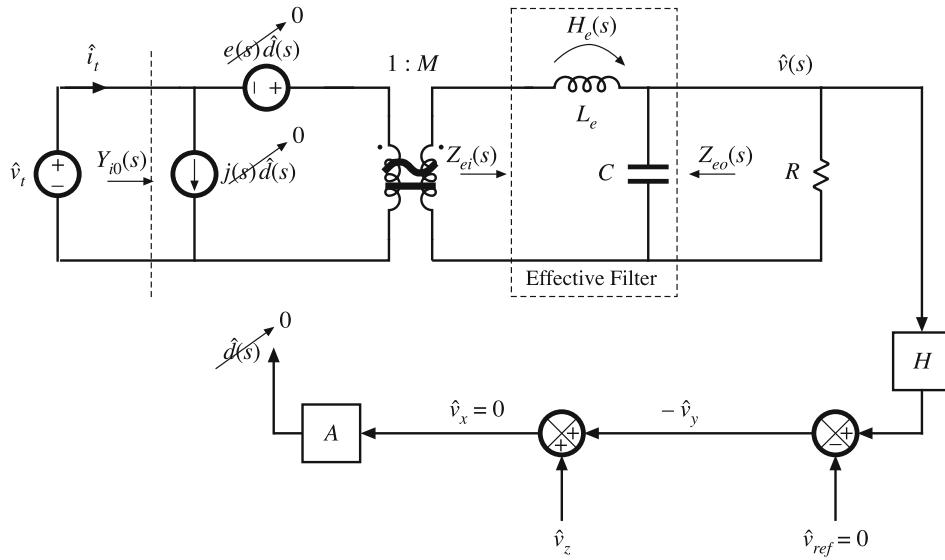
$$Y_{i0}(s) = \frac{M^2}{Z_{ei}(s)} \quad (17.75)$$

At frequencies where the loop gain  $T$  is small in magnitude, then the converter closed-loop incremental input admittance  $Y_i$  follows the open-loop value  $M^2/Z_{ei}$ . This quantity is a passive admittance, having phase in the range  $-90^\circ \leq \angle Y_i \leq +90^\circ$ . The quantity  $1/Y_{i0}$  coincides with the  $Z_D$  listed in Table 17.1; when the loop gain is small then the converter closed-loop input impedance follows  $Z_D$ .

The loop gain  $T(s)$  of Eq. (17.70) is given by

$$T(s) = \left. \frac{\hat{v}_y(s)}{\hat{v}_x(s)} \right|_{\begin{subarray}{l} \hat{v}_{ref}=0 \\ \hat{v}_t=0 \end{subarray}} \quad (17.76)$$

This is the loop gain of the original closed-loop regulator, before addition of the input filter.

Fig. 17.44 Determination of  $Y_{i0}$ 

### Construction of $Z_i$

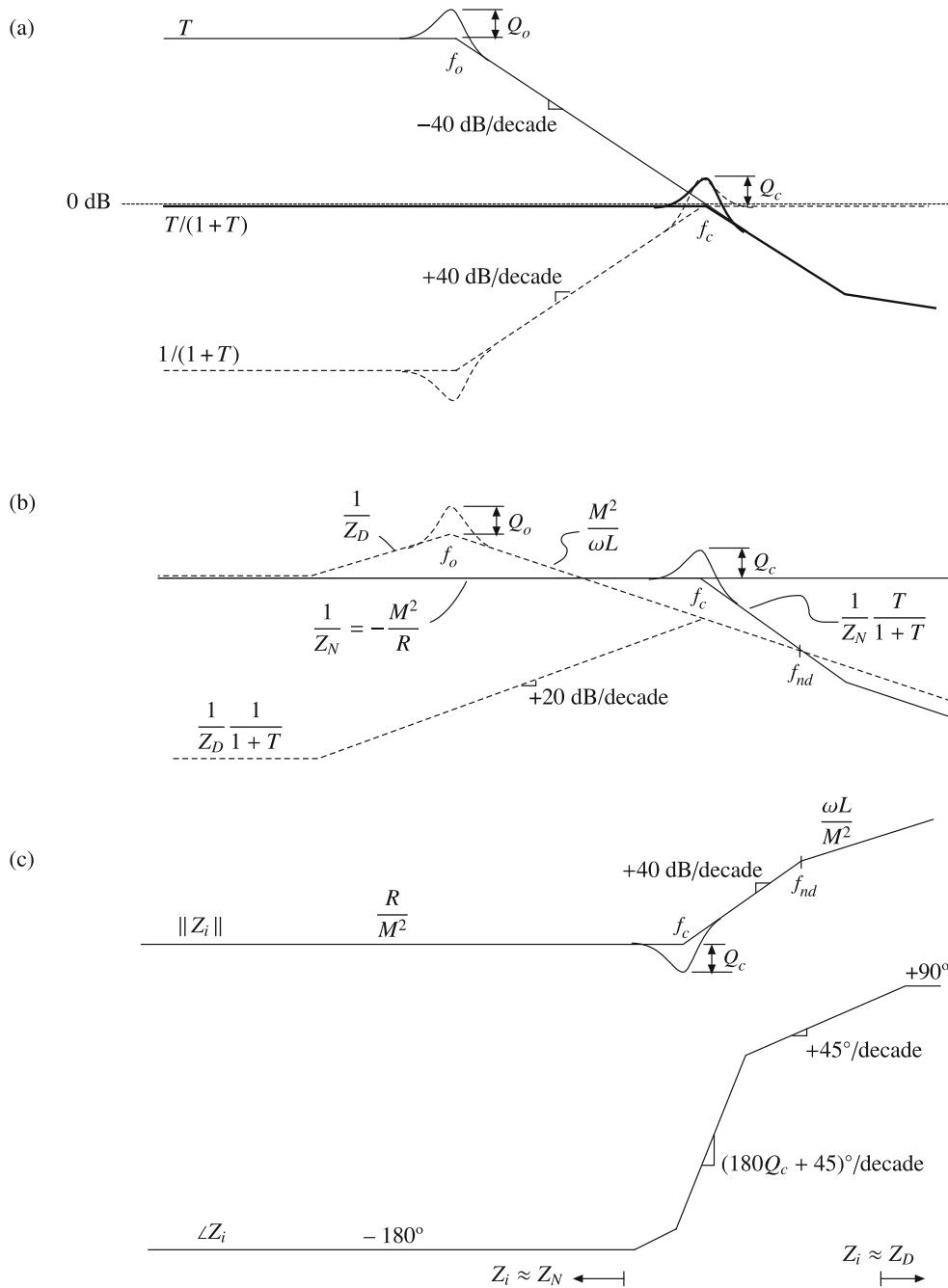
Construction of the closed-loop input impedance  $Z_i = 1/Y_i$  based on the results of Eqs. (17.70), (17.73), and (17.75). Graphical construction of  $Z_i$  is illustrated in Fig. 17.45 for a simple buck converter example. Figure 17.45a contains magnitude asymptotes of  $T$ ,  $T/(1+T)$ , and  $1/(1+T)$ , constructed as described in Sect. 9.3. The loop gain for this simple example includes the resonant poles of the converter  $L-C$  filter at frequency  $f_o$ , plus a high-frequency zero. The loop crossover frequency is  $f_c$ , and the phase margin of  $T$  leads to peaking with closed-loop  $Q$ -factor  $Q_c$  as described in Sect. 9.4.3.

Figure 17.45b illustrates construction of the admittance terms of Eq. (17.70). The  $Z_N$  and  $Z_D$  terms of Table 17.1 are inverted to obtain their admittances, and then are multiplied by the  $T/(1+T)$  and  $1/(1+T)$  plots of Fig. 17.45a. Figure 17.45c contains plots of the magnitude and phase of the converter closed-loop input impedance  $Z_i$ , derived from Fig. 17.45b according to Eq. (17.70).

At frequencies well below the original loop crossover frequency  $f_c$  where the loop gain  $T$  is large in magnitude, then  $T/(1+T) \approx 1$  and  $1/(1+T)$  is small. Hence,  $Y_i \approx Y_{i\infty}$  and  $Z_i \approx Z_N$ . As illustrated in Fig. 17.45c,  $Z_i$  follows  $-R/M^2$  and has phase  $-180^\circ$  at low frequency.

At frequencies well above  $f_c$  where  $\|T\| \ll 1$ , then  $\|T/(1+T)\| \ll 1$  and  $\|1/(1+T)\| \approx 1$ . Hence  $Y_i \approx Y_{i0}$  and the closed-loop input impedance  $Z_i$  follows  $Z_D$ . For the example asymptotes of Fig. 17.45,  $Z_i$  follows the inductor asymptote  $sL/M^2$  at high frequency, with a phase of  $+90^\circ$ .

In the vicinity of the original loop crossover frequency  $f_c$ , the impedance  $Z_i$  transitions between  $Z_N$  and  $Z_D$ . In general, the  $Z_N$  and  $Z_D$  asymptotes can differ at the loop crossover frequency, and hence this transition will contain new asymptotes that are not present in  $Z_N$  and  $Z_D$  alone. Depending on the phase margin of the original loop gain  $T$ , the  $T/(1+T)$  and  $1/(1+T)$  terms of Eq. (17.70) may contain resonant poles and peaking in the vicinity of  $f_c$ . This leads to



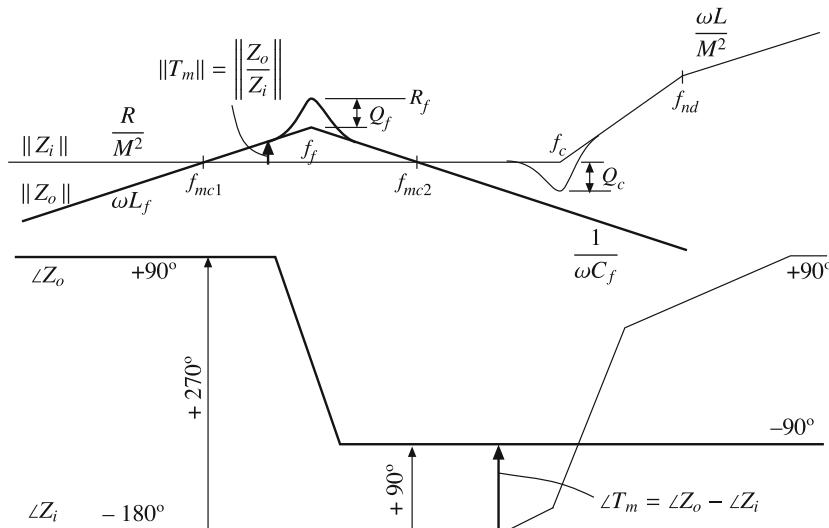
**Fig. 17.45** Steps in the construction of the asymptotes of the closed-loop converter input impedance  $Z_i(s)$ : (a) converter loop gain  $T$  and the closed-loop quantities  $T/(1+T)$  and  $1/(1+T)$ ; (b) the admittance terms of Eq. (17.70); (c) the resulting magnitude and phase asymptotes of  $Z_i(s)$

resonant zeroes in  $Z_i = 1/Y_i$ ; therefore it is possible that  $\|Z_i\|$  is smaller than  $\|Z_N\|$  and  $\|Z_D\|$  in the vicinity of  $f_c$ . Additionally,  $Z_i$  contains a RHP pole at frequency  $f_{nd}$ ; at frequencies greater than  $f_{nd}$ , the negative sign of  $Z_N$  is cancelled by the negative sign of the RHP pole, and  $Z_i$  reverts to a passive open-loop impedance. It should be noted that the RHP pole of  $Z_i$  does not directly lead to instability: when the converter is driven by a voltage source  $v_g$ , the current is given by the transfer function  $i_g = v_g/Z_i$ . This transfer function contains a RHP zero at  $f_{nd}$ , and exhibits no RHP poles.

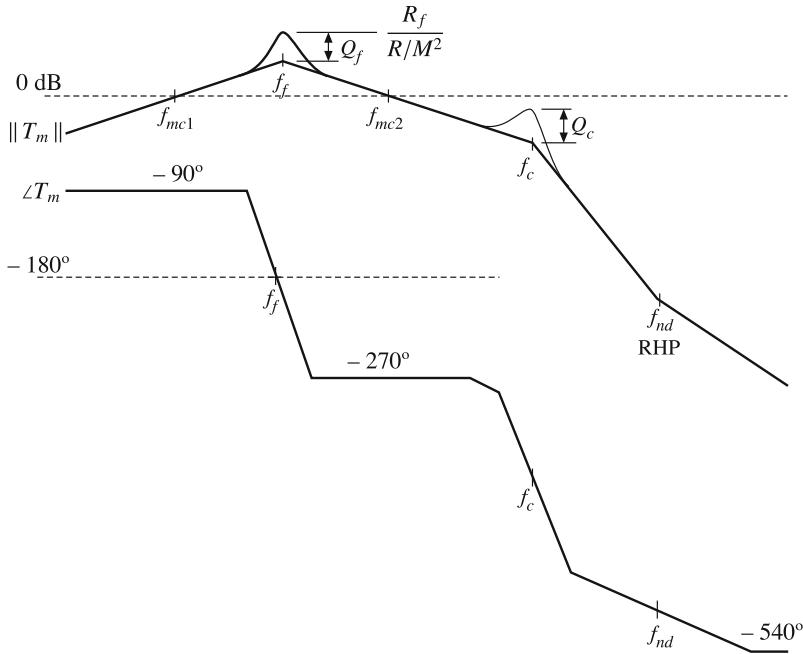
### Determination of stability

Next, we can construct the minor loop gain  $T_m = Z_o/Z_i$  of Eq. (17.68). In Fig. 17.46, an input filter impedance  $Z_o$  is overlayed on the  $Z_i$  impedance of Fig. 17.45c. As illustrated in Fig. 17.46, the magnitude of  $T_m$  can be found by subtracting the magnitude  $\|Z_i\|_{\text{dB}}$  from  $\|Z_o\|_{\text{dB}}$ . At the frequency or frequencies where  $\|Z_i\| = \|Z_o\|$ , the minor loop gain  $T_m$  exhibits a crossover frequency. The phase of  $T_m$  at a given frequency also can be found by subtracting:  $\angle T_m = \angle Z_o - \angle Z_i$ .

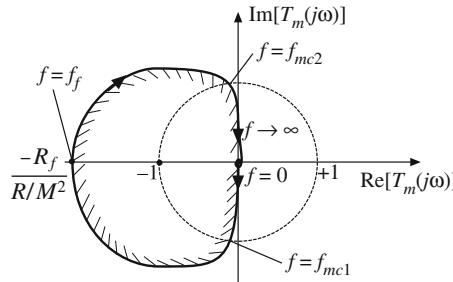
The Bode plot of the minor loop gain  $T_m$  is constructed in Fig. 17.47, based on the impedance asymptotes of Fig. 17.46. To conform with the conventional appearance of loop gain phase, the phase asymptotes of  $T_m$  have been shifted by  $-360^\circ$ ; this corresponds to multiplying  $T_m$  by  $e^{-j360^\circ} = 1$ , and does not change the result. For the specific case sketched in Fig. 17.46, the input filter impedance  $\|Z_o\|$  is greater than the converter closed-loop input impedance  $\|Z_i\|$  over the frequency range from  $f_{mc1}$  to  $f_{mc2}$ . As illustrated in Fig. 17.47, the minor loop gain  $T_m$  exhibits crossover frequencies at  $f_{mc1}$  and  $f_{mc2}$ , and reaches a peak magnitude of  $R_f M^2/R$  at the filter resonant frequency  $f_f$ . The phase of  $T_m$  at frequency  $f_{mc1}$  is approximately  $-90^\circ$ , corresponding to a phase margin of  $+90^\circ$ . The phase of  $T_m$  is approximately  $-270^\circ$  at  $f_{mc2}$ , cor-



**Fig. 17.46** Superimposing the input filter impedance  $Z_o$  on the converter closed-loop input impedance asymptotes  $Z_i$  to determine the minor loop gain  $T_m$



**Fig. 17.47** Bode plot of minor loop gain  $T_m$  for the example of Fig. 17.46



**Fig. 17.48** Nyquist plot of minor loop gain  $T_m$  for the example of Fig. 17.46. Crosshatching denotes the region to the right of the contour; the  $-1$  point is enclosed

responding to a phase margin of  $-90^\circ$ . The minor loop gain  $T_m$  contains resonant poles at the original loop crossover frequency  $f_c$  and a right half-plane zero at frequency  $f_{nd}$ .

With multiple crossover frequencies, determination of stability should be resolved by use of the Nyquist plot. The positive-frequency portion of the Nyquist plot of the minor loop gain  $T_m(s)$  is illustrated in Fig. 17.48. The minor loop gain has magnitude zero at dc. As frequency increases,  $T_m$  increases in magnitude with approximate phase  $-90^\circ$ , until it reaches unity magnitude at  $f = f_{mc1}$ . In the vicinity of  $f = f_f$ ,  $T_m$  has magnitude greater than 1, with phase decreasing from  $-90^\circ$  towards  $-270^\circ$ . At frequencies greater than  $f_{mc2}$ ,  $T_m$  exhibits magnitude less than 1. It can be seen that the  $-1$  point is encircled once by the positive-frequency portion

of the Nyquist plot sketched in Fig. 17.48. The negative-frequency portion of the Nyquist plot, which is the complex conjugate (not shown in Fig. 17.48), also encircles the  $-1$  point once. Consequently, the closed-loop term

$$\frac{1}{1 + T_m} = \frac{Z_i}{Z_o + Z_i} \quad (17.77)$$

contains two right half-plane poles, and is unstable. The regulator closed-loop transfer functions such as Eq. (17.67) will also exhibit these two right half-plane poles.

It can be observed from Fig. 17.48 that the encirclements of the  $-1$  point could be eliminated by reducing the magnitude of the quantity  $R_f/(R/M^2)$  to be less than unity. Then the Nyquist plot no longer would encircle the  $-1$  point, and the minor loop  $T_m$  would no longer introduce RHP poles. This coincides with the earlier conclusion that adequate damping of the input filter can stabilize the system.

### 17.5.3 Discussion

Section 17.5 describes two distinct approaches to derivation of the exact stability boundary of a switching regulator with addition of an input filter. In Sect. 17.5.1, the Extra Element Theorem is employed to determine the modified loop gain  $T'(s)$ . The usual gain and phase margin tests can then be employed to ascertain the stability of the modified regulator system. By contrast, the approach of Sect. 17.5.2 employs the Feedback Theorem to find the new closed-loop poles induced by addition of the input filter. These poles are ascribed to a voltage divider term that accounts for the loading of the input filter impedance  $Z_o(s)$  by the closed-loop converter input impedance  $Z_i(s)$ . This voltage divider term can be viewed as having an effective minor loop gain  $T_m(s) = Z_o(s)/Z_i(s)$ , whose stability can be ascertained using the usual techniques including phase and gain margins and the Nyquist stability tests.

Thus, we have two distinct approaches to determination of the stability boundary of the regulator when modified by addition of an input filter. It can be verified that identical closed-loop poles and characteristic equations are predicted by the two approaches. Hence, provided that the original unmodified system is stable, the two approaches predict identical stability boundaries.

Finally, it should be emphasized that Sects. 17.1 to 17.4 are concerned with design of an input filter that does not disrupt the important transfer functions of the closed-loop regulator, while Sect. 17.5 is concerned with determination of the formal stability boundary. While these are very different goals, it is revealing that all approaches rely on the impedances  $Z_N$  and  $Z_D$  of Table 17.1, albeit in different ways. Ultimately, the impedance inequalities of Eq. (17.19) are the governing design criteria, with the issue only being how conservative should the design be. The engineer can employ modern tools to plot the relevant equations of all sections and produce an informed and optimized design.

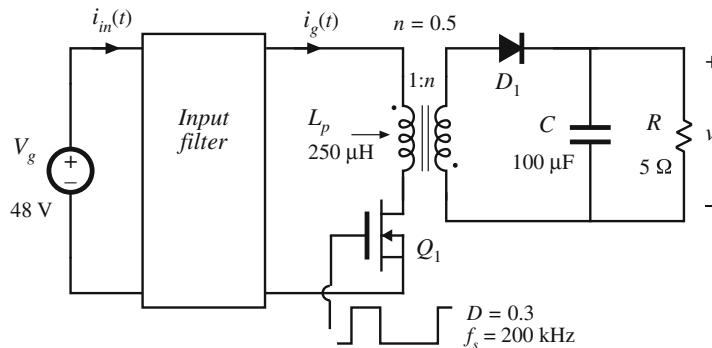
## 17.6 Summary of Key Points

1. Switching converters usually require input filters, to reduce conducted electromagnetic interference and possibly also to meet requirements concerning conducted susceptibility.
2. Addition of an input filter to a converter alters the control-to-output and other transfer functions of the converter. Design of the converter control system must account for the effects of the input filter.

3. If the input filter is not damped, then it typically introduces complex poles and RHP zeroes into the converter control-to-output transfer function, at the resonant frequencies of the input filter. If these resonant frequencies are lower than the crossover frequency of the controller loop gain, then the phase margin will become negative and the regulator will be unstable.
4. The input filter can be designed so that it does not significantly change the converter control-to-output and other transfer functions. Impedance inequalities (17.19) give simple design criteria that guarantee this. To meet these design criteria, the resonances of the input filter must be sufficiently damped.
5. Optimization of the damping networks of single-section filters can yield significant savings in filter element size. Equations for optimizing three different filter sections are listed.
6. Substantial savings in filter element size can be realized via cascading filter sections. The design of noninteracting cascaded filter sections can be achieved by an approach similar to the original input filter design method. Impedance inequalities (17.50) give design criteria that guarantee that interactions are not substantial.
7. Another useful approach for determination of the exact stability boundary is based on the loading of the input filter, whose output impedance is  $Z_o(s)$ , by the closed-loop converter input impedance  $Z_i(s)$ . The stability is examined by treating  $T_m(s) = Z_o(s)/Z_i(s)$  as a minor loop gain using conventional techniques such as the Nyquist stability theorem and the phase margin test.

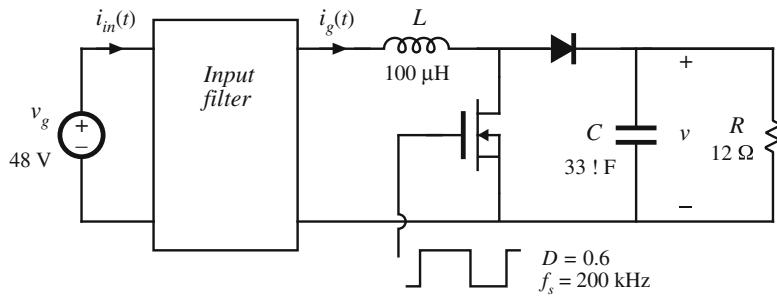
## PROBLEMS

- 17.1** It is required to design an input filter for the flyback converter of Fig. 17.49. The maximum allowed amplitude of switching harmonics of  $i_{in}(t)$  is  $10 \mu\text{A}$  rms. Calculate the required attenuation of the filter at the switching frequency.



**Fig. 17.49** Flyback converter, Problems 17.1, 17.4, 17.6, 17.8, and 17.10

- 17.2** In the boost converter of Fig. 17.50, the input filter is designed so that the maximum amplitude of switching harmonics of  $i_{in}(t)$  is not greater than  $10 \mu\text{A}$  rms. Find the required attenuation of the filter at the switching frequency.



**Fig. 17.50** Boost converter, Problems 17.2, 17.5, 17.7, and 17.9

**17.3** Derive the expressions for  $Z_N$  and  $Z_D$  in Table 17.1.

**17.4** The input filter for the flyback converter of Fig. 17.49 is designed using a single  $L_f-C_f$  section. The filter is damped using a resistor  $R_f$  in series with a very large blocking capacitor  $C_b$ .

- (a) Sketch a small-signal model of the flyback converter. Derive expressions for  $Z_N(s)$  and  $Z_D(s)$  using your model. Sketch the magnitude Bode plots of  $Z_N$  and  $Z_D$ , and label all salient features.
- (b) Design the input filter, i.e., select the values of  $L_f$ ,  $C_f$ , and  $R_f$ , so that: (i) the filter attenuation at the switching frequency is at least 100 dB, and (ii) the magnitude of the filter output impedance  $Z_o(s)$  satisfies the conditions  $\|Z_o(j\omega)\| < 0.3 \|Z_D(j\omega)\|$  and  $\|Z_o(j\omega)\| < 0.3 \|Z_N(j\omega)\|$ , for all frequencies.
- (c) Use Spice simulations to verify that the filter designed in part (b) meets the specifications.
- (d) Using Spice simulations, plot the converter control-to-output magnitude and phase responses without the input filter, and with the filter designed in part (b). Comment on the changes introduced by the filter.

**17.5** It is required to design the input filter for the boost converter of Fig. 17.50 using a single  $L_f-C_f$  section. The filter is damped using a resistor  $R_f$  in series with a very large blocking capacitor  $C_b$ .

- (a) Sketch the magnitude Bode plots of  $Z_N(s)$  and  $Z_D(s)$  for the boost converter, and label all salient features.
- (b) Design the input filter, i.e., select the values of  $L_f$ ,  $C_f$ , and  $R_f$ , so that: (i) the filter attenuation at the switching frequency is at least 80 dB, and (ii) the magnitude of the filter output impedance  $Z_o(s)$  satisfies the conditions  $\|Z_o(j\omega)\| < 0.2 \|Z_D(j\omega)\|$ ,  $\|Z_o(\omega)\| < 0.2 \|Z_N(\omega)\|$ , for all frequencies.
- (c) Use Spice simulations to verify that the filter designed in part (b) meets the specifications.
- (d) Using Spice simulations, plot the converter control-to-output magnitude and phase responses without the input filter, and with the filter designed in part (b). Comment on the changes in the control-to-output responses introduced by the filter.

**17.6** Repeat the filter design of Problem 17.4 using the optimum filter damping approach described in Sect. 17.4.1. Find the values of  $L_f$ ,  $C_f$ ,  $R_f$ , and  $C_b$ .

- 17.7** Repeat the filter design of Problem 17.5 using the optimum filter damping approach of Sect. 17.4.1. Find the values of  $L_f$ ,  $C_f$ ,  $R_f$ , and  $C_b$ .
- 17.8** Repeat the filter design of Problem 17.4 using the optimum  $R_f-L_b$  parallel damping approach described in Sect. 17.4.2. Find the values of  $L_f$ ,  $C_f$ ,  $R_f$ , and  $L_b$ .
- 17.9** Repeat the filter design of Problem 17.5 using the optimum  $R_f-L_b$  parallel damping approach described in Sect. 17.4.2. Find the values of  $L_f$ ,  $C_f$ ,  $R_f$ , and  $L_b$ .
- 17.10** It is required to design the input filter for the flyback converter of Fig. 17.32 using two filter sections. Each filter section is damped using a resistor in series with a blocking capacitor.
- Design the input filter, *i.e.*, select values of all circuit parameters, so that (i) the filter attenuation at the switching frequency is at least 100 dB, and (ii) the magnitude of the filter output impedance  $Z_o(s)$  satisfies the conditions  $\|Z_o(j\omega)\| < 0.3 \|Z_D(j\omega)\|$  and  $\|Z_o(j\omega)\| < 0.3 \|Z_N(\omega)\|$ , for all frequencies.
  - Use Spice simulations to verify that the filter designed in part (a) meets the specifications.
  - Using Spice simulations, plot the converter control-to-output magnitude and phase responses without the input filter, and with the filter designed in part (b). Comment on the changes introduced by the filter.
- 17.11** Consider the boost voltage regulator of Problem 9.3. It is required to design an input filter for this voltage regulator. The filter should have a single  $L_f-C_f$  section with optimum damping using a resistor  $R_f$  in series with a capacitor  $C_b$ .
- Design the input filter, *i.e.*, select values of all circuit parameters, so that (i) the filter attenuation at the switching frequency  $f_s = 200$  kHz is equal to at least 80 dB, and (ii) the magnitude of the filter output impedance  $Z_o(s)$  satisfies the conditions  $\|Z_o(j\omega)\| \leq 0.4 \|Z_D(j\omega)\|$  and  $\|Z_o(j\omega)\| \leq 0.4 \|Z_N(\omega)\|$ , for all frequencies.
  - Determine the closed-loop input impedance  $Z_i(s)$  of the regulator in Problem 9.3. Examine stability of the closed-loop system by analysis of the minor loop gain  $T_m(s) = Z_o(s)/Z_i(s)$ , where  $Z_o(s)$  is the output impedance of the input filter designed in part (a).



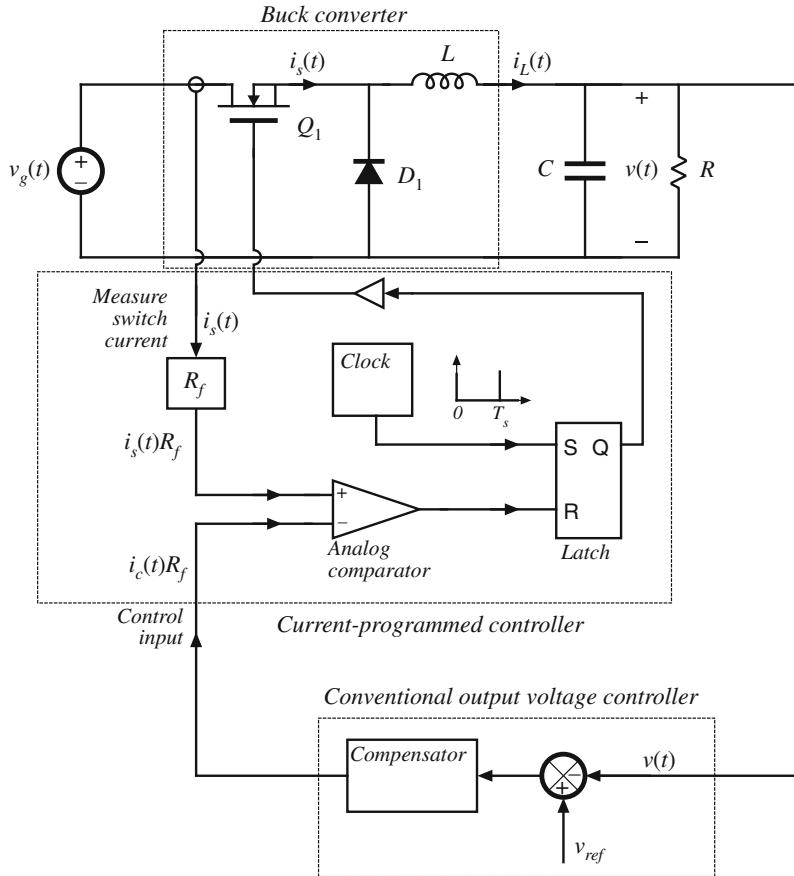
## Current-Programmed Control

So far, we have discussed duty ratio control of PWM converters, in which the converter output is controlled by direct choice of the duty ratio  $d(t)$ . We have therefore developed expressions and small-signal transfer functions that relate the converter waveforms and output voltage to the duty ratio. This direct duty ratio control is sometimes called *voltage mode control*, because the equilibrium output voltage is approximately proportional to the duty cycle in CCM.

Another control scheme which finds wide application is current programmed control [67, 69, 107, 163–175], in which the converter is controlled by choice of the transistor switch current peak( $i_s(t)$ ). The control input signal is a current  $i_c(t)$ , and a simple control network switches the transistor on and off such that the peak transistor current follows  $i_c(t)$ . The transistor duty cycle  $d(t)$  is not directly controlled, but depends on  $i_c(t)$  as well as on the converter inductor currents, capacitor voltages, and power input voltage. Converters controlled via current programming are said to operate in the *current-programmed mode* (CPM), also known as *peak current mode* (PCM) control.

The block diagram of a simple current-programmed controller is illustrated in Fig. 18.1. Control signal  $i_c(t)$  and switch current  $i_s(t)$  waveforms are given in Fig. 18.2. A clock pulse at the Set input of a latch initiates the switching period, causing the latch output  $Q$  to be high and turning on the transistor switch. While the transistor conducts, its current  $i_s(t)$  is equal to the inductor current  $i_L(t)$ ; this current increases with some positive slope  $m_1$  that depends on the value of inductance and the converter voltages. In more complicated converters,  $i_s(t)$  may follow the sum of several inductor currents. Eventually, the switch current  $i_s(t)$  becomes equal to the control signal  $i_c(t)$ . At this point, the controller turns the transistor switch off, and the inductor current decreases for the remainder of the switching period. The controller measures the switch current  $i_s(t)$  with some current sensor circuit, and compares  $i_s(t)$  to  $i_c(t)$  using an analog comparator. In practice, voltages proportional to  $i_s(t)$  and  $i_c(t)$  are compared, with constant of proportionality  $R_f$ . When  $i_s(t) \geq i_c(t)$ , the comparator resets the latch, turning the transistor off for the remainder of the switching period.

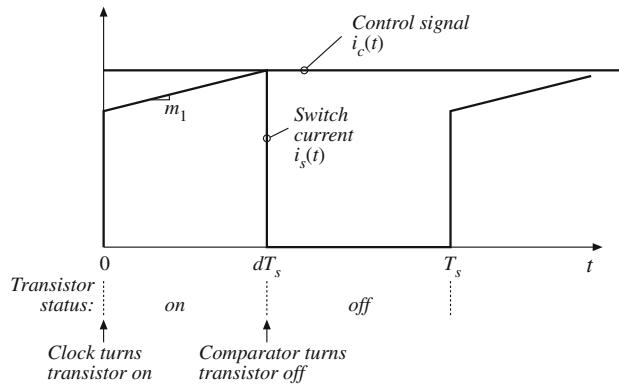
As usual, a feedback loop can be constructed for regulation of the output voltage. The output voltage  $v(t)$  is compared to a reference voltage  $v_{ref}$ , to generate an error signal. This error signal is applied to the input of a compensation network, and the output of the compensator drives the control signal  $i_c(t)R_f$ . To design such a feedback system, we need to model how variations in the control signal  $i_c(t)$  and in the line input voltage  $v_g(t)$  affect the output voltage  $v(t)$ .



**Fig. 18.1** Current-programmed control of a buck converter. The peak transistor current replaces the duty cycle as the control input

An advantage of the current-programmed mode is its simpler dynamics. To first order, the small-signal control-to-output transfer function  $\hat{v}(s)/\hat{i}_c(s)$  contains one less pole than  $\hat{v}(s)/\hat{d}(s)$ . Actually, the pole is moved to a high frequency, near the converter switching frequency. Nonetheless, simple robust wide-bandwidth output voltage control can usually be obtained, without the use of compensator lead networks. It is true that the current-programmed controller requires a circuit for measurement of the switch current  $i_s(t)$ ; however, in practice such a circuit is also required in duty ratio controlled systems, for protection of the transistor against excessive currents during transients and fault conditions. Current-programmed control makes use of the available current sensor information during normal operation of the converter, to obtain simpler system dynamics. Transistor failures due to excessive switch current can then be prevented simply by limiting the maximum value of the control signal  $i_c(t)$ . This ensures that the transistor will turn off whenever the switch current becomes too large, on a cycle-by-cycle basis.

An added benefit of current programming is the reduction or elimination of transformer saturation problems in full-bridge or push-pull isolated converters. In these converters, small



**Fig. 18.2** Switch current  $i_s(t)$  and control input  $i_c(t)$  waveforms, for the current-programmed system of Fig. 18.1

voltage imbalances induce a dc bias in the transformer magnetizing current; if sufficiently large, this dc bias can saturate the transformer. The dc current bias increases or decreases the transistor switch currents. In response, the current programmed controller alters the transistor duty cycles, such that transformer volt-second balance tends to be maintained. Current-programmed full-bridge isolated buck converters should be operated without a capacitor in series with the transformer primary winding; this capacitor tends to destabilize the system. For the same reason, current-programmed control of half-bridge isolated buck converters is generally avoided. Commercial integrated circuits that implement current-programmed control are widely available, and operation of converters in the current-programmed mode is quite popular.

A disadvantage of current-programmed control is its susceptibility to noise in the  $i_s(t)$  or  $i_c(t)$  signals. This noise can prematurely reset the latch, disrupting operation of the controller. To remove the turn-on current spike caused by the diode stored charge, a small amount of filtering of the sensed switch current waveform is usually applied. Furthermore, CPM controllers often include a short blanking interval at the beginning of a switching cycle. During the blanking interval, resetting of the latch is disabled, which prevents spurious transistor turn off. It should be noted, however, that the blanking interval imposes a lower limit on the attainable duty cycle.

This chapter is devoted to analysis, modeling and design of converters operating in current-programmed mode. In Sect. 18.1, the system small-signal transfer functions are derived using a simple first-order model. The averaged terminal waveforms of the switch network can be described by a simple current source, in conjunction with a power source element. Perturbation and linearization steps lead to a simple small-signal model.

In Sect. 18.2, stability of the current-programmed controller and its inner switch-current-sensing loop is examined. It is found that this controller is unstable whenever converter steady-state duty cycle  $D$  is greater than 0.5. The current programmed controller can be stabilized by addition of an artificial ramp signal to the sensed switch current waveform. Furthermore, addition of the artificial ramp, also known as *slope compensation*, improves noise immunity of the controller.

Although the first-order model of Sect. 18.1 yields a great deal of insight into the control-to-output transfer function and converter output impedance, it does not accurately predict the line-to-output transfer function  $G_{vg}(s)$  of current-programmed buck converters. Furthermore, the simple model does not take into account the effects of the inductor current ripple or the artificial ramp. Hence, a more accurate averaged model is developed in Sect. 18.3, and CPM transfer functions are derived in Sect. 18.4. Based on the more accurate averaged model, simulation of current-programmed converters is addressed in Sect. 18.5. Design of the voltage feedback

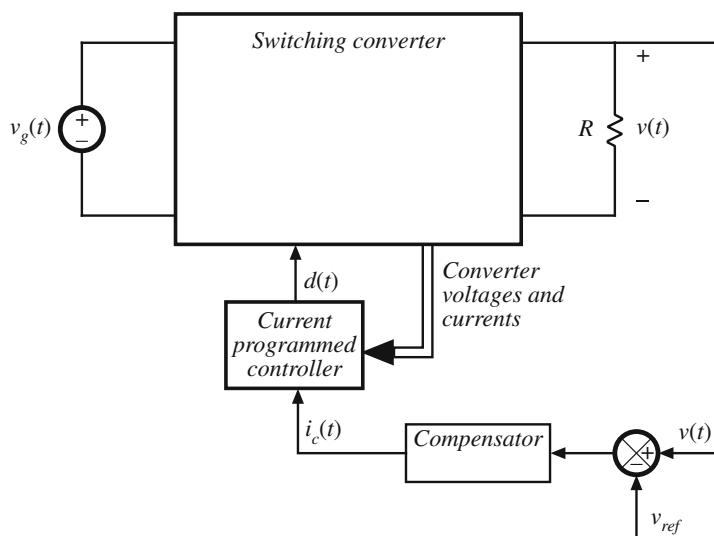
loop is discussed in Sect. 18.6. High-frequency responses of current-programmed converters in continuous conduction mode are further examined in Sect. 18.7 using sampled-data modeling techniques. Finally, Sect. 18.8 extends the modeling of current-programmed converters to the discontinuous conduction mode.

Another approach to current programming, known as *average current mode* (ACM) control, consists of constructing a feedback loop for regulation of an average converter current. This approach is discussed in Sect. 18.9. An advantage of average current-mode control is that it enables direct control over the converter input or output current, which is required in some applications, including battery chargers, drivers for light emitting diodes, as well as ac grid-tied rectifiers and inverters. Furthermore, ACM controllers have improved noise immunity, and do not necessarily require slope compensation for stable operation over wide range of duty cycles.

## 18.1 A Simple First-Order Model

Once the current-programmed controller has been constructed, it is desired to design a feedback loop for regulation of the output voltage. As usual, this voltage feedback loop must be designed to meet specifications regarding line disturbance rejection, transient response, output impedance, etc. A block diagram of a typical system is illustrated in Fig. 18.3, containing an inner current-programmed controller, with an outer voltage feedback loop.

To design the outer voltage feedback loop, an ac equivalent circuit model of the switching converter operating in the current-programmed mode is needed. In Chap. 7, averaging was employed to develop small-signal ac equivalent circuit models for converters operating with duty ratio control. These models predict the circuit behavior in terms of variations  $\hat{d}$  in the duty cycle. If we could find the relationship between the control signal  $i_c(t)$  and the duty cycle  $d(t)$  for the current-programmed controller, then we could adapt the models of Chap. 7, to apply to the



**Fig. 18.3** Block diagram of a converter system incorporating current-programmed control

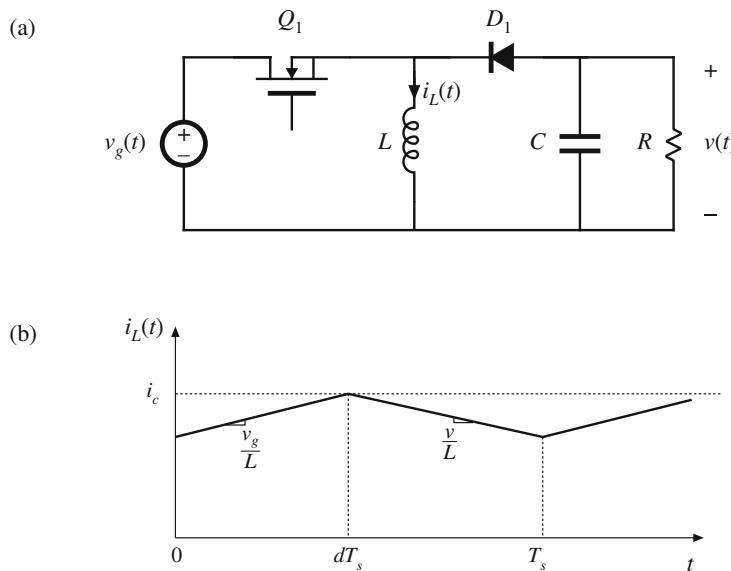
current-programmed mode as well. In general, the duty cycle depends not only on  $i_c(t)$ , but also on the converter voltages and currents; hence, the current-programmed controller incorporates multiple effective feedback loops as indicated in Fig. 18.3.

In this section, the averaging approach is extended, as described above, to treat current-programmed converters. A simple first-order approximation is employed, in which it is assumed that the current programmed controller operates ideally, and hence causes the average inductor current  $\langle i_L(t) \rangle_{T_s}$  to be identical to the control  $i_c(t)$ . This approximation is justified whenever the inductor current ripple and artificial ramp (discussed in Sect. 18.2) have negligible magnitudes. The inductor current then is no longer an independent state of the system, and no longer contributes a pole to the converter small-signal transfer functions.

This first-order model is derived in Sect. 18.1.1, using a simple algebraic approach. In Sect. 18.1.2, a simple physical interpretation is obtained via the averaged switch modeling technique. A more accurate, but more complicated, model is described in Sect. 18.3.

### 18.1.1 Simple Model via Algebraic Approach: Buck–Boost Example

The power stage of a simple buck–boost converter operating in the continuous conduction mode is illustrated in Fig. 18.4a, and its inductor current waveform is given in Fig. 18.4b. The small-signal averaged equations for this converter, under duty-cycle control, were derived in Sect. 7.2. The result, Eq. (7.44), is reproduced below:



**Fig. 18.4** Buck–boost converter example: (a) power stage, (b) inductor current waveform

$$\begin{aligned} L \frac{d\hat{i}_L(t)}{dt} &= D\hat{v}_g(t) + D'\hat{v}(t) + (V_g - V)\hat{d}(t) \\ C \frac{d\hat{v}(t)}{dt} &= -D'\hat{i}_L - \frac{\hat{v}(t)}{R} + I_L\hat{d}(t) \\ \hat{i}_g(t) &= D\hat{i}_L + I_L\hat{d}(t) \end{aligned} \quad (18.1)$$

The Laplace transforms of these equations, with initial conditions set to zero, are

$$\begin{aligned} sL\hat{i}_L(s) &= D\hat{v}_g(s) + D'\hat{v}(s) + (V_g - V)\hat{d}(s) \\ sC\hat{v}(s) &= -D'\hat{i}_L(s) - \frac{\hat{v}(s)}{R} + I_L\hat{d}(s) \\ \hat{i}_g(s) &= D\hat{i}_L(s) + I_L\hat{d}(s) \end{aligned} \quad (18.2)$$

We now make the assumption that the inductor current  $\hat{i}_L(s)$  is identical to the programmed control current  $\hat{i}_c(s)$ . This is valid to the extent that the controller is stable, and that the magnitudes of the inductor current ripple and artificial ramp waveform are sufficiently small:

$$\hat{i}_L(s) \approx \hat{i}_c(s) \quad (18.3)$$

This approximation, in conjunction with the inductor current equation of (18.2), can now be used to find the relationship between the control current  $\hat{i}_c(s)$  and the duty cycle  $\hat{d}(s)$ , as follows:

$$sL\hat{i}_c(s) \approx D\hat{v}_g(s) + D'\hat{v}(s) + (V_g - V)\hat{d}(s) \quad (18.4)$$

Solution for  $\hat{d}(s)$  yields

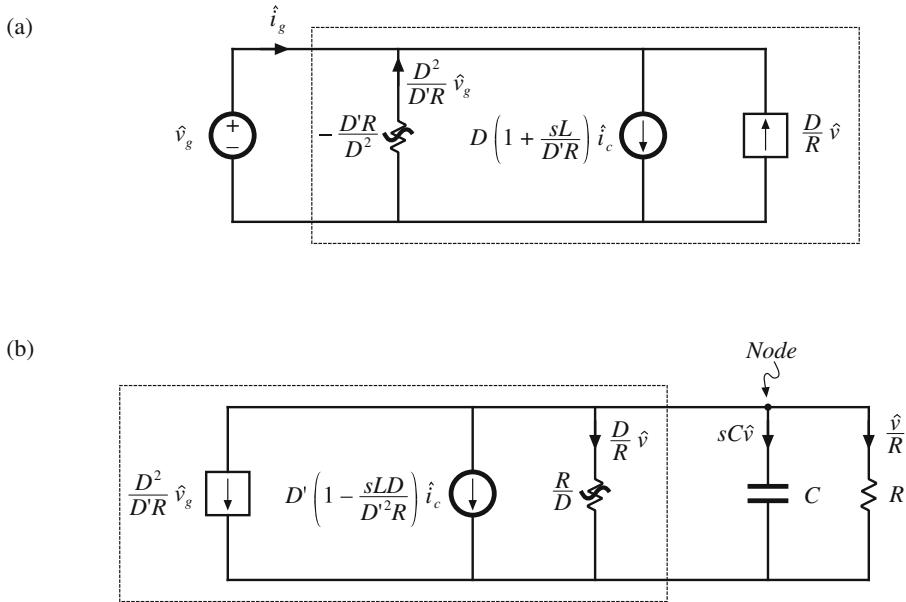
$$\hat{d}(s) = \frac{sL\hat{i}_c(s) - D\hat{v}_g(s) - D'\hat{v}(s)}{(V_g - V)} \quad (18.5)$$

This small-signal expression describes how the current-programmed controller varies the duty cycle, in response to a given control input variation  $\hat{i}_c(s)$ . It can be seen that  $\hat{d}(s)$  depends not only on  $\hat{i}_c(s)$ , but also on the converter output voltage and input voltage variations. Equation (18.5) can now be substituted into the second and third lines of Eq. (18.2), thereby eliminating  $\hat{d}(s)$ . One obtains

$$\begin{aligned} sC\hat{v}(s) &= -D'\hat{i}_c(s) - \frac{\hat{v}(s)}{R} + I_L \frac{sL\hat{i}_c(s) - D\hat{v}_g(s) - D'\hat{v}(s)}{(V_g - V)} \\ \hat{i}_g(s) &= D\hat{i}_c(s) + I_L \frac{sL\hat{i}_c(s) - D\hat{v}_g(s) - D'\hat{v}(s)}{(V_g - V)} \end{aligned} \quad (18.6)$$

These equations can be simplified by collecting terms, and by use of the steady-state relationships

$$\begin{aligned} V &= -\frac{D}{D'}V_g \\ I_L &= -\frac{V}{D'R} = \frac{D}{D'^2R}V_g \end{aligned} \quad (18.7)$$



**Fig. 18.5** Construction of CPM CCM buck-boost converter equivalent circuit: (a) input port model, corresponding to Eq. (18.9); (b) output port model, corresponding to Eq. (18.8)

Equation (18.6) then becomes

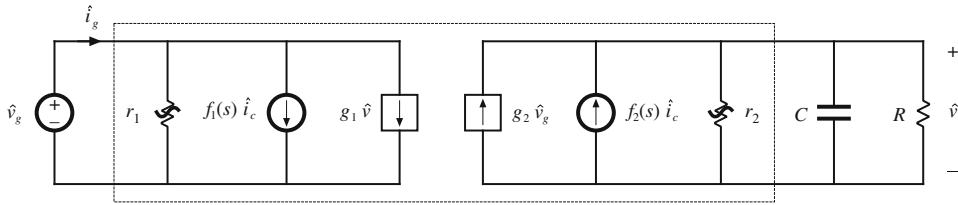
$$sC\hat{v}(s) = \left(\frac{sLD}{D'R} - D'\right)\hat{i}_c(s) - \left(\frac{D}{R} + \frac{1}{R}\right)\hat{v}(s) - \left(\frac{D^2}{D'R}\right)\hat{v}_g(s) \quad (18.8)$$

$$\hat{i}_g(s) = \left(\frac{sLD}{D'R} + D\right)\hat{i}_c(s) - \left(\frac{D}{R}\right)\hat{v}(s) - \left(\frac{D^2}{D'R}\right)\hat{v}_g(s) \quad (18.9)$$

These are the basic ac small-signal equations for the simplified first-order model of the current-programmed buck-boost converter. These equations can now be used to construct small-signal ac circuit models that represent the behavior of the converter input and output ports. In Eq. (18.8), the quantity  $sC\hat{v}(s)$  is the output capacitor current. The  $\hat{i}_c(s)$  term is represented in Fig. 18.5b by an independent current source, while the  $\hat{v}_g(s)$  term is represented by a dependent current source.  $\hat{v}(s)/R$  is the current through the load resistor, and  $\hat{v}(s)D/R$  is the current through an effective ac resistor of value  $R/D$ .

Equation (18.9) describes the current  $\hat{i}_g(s)$  drawn by the converter input port, out of the source  $\hat{v}_g(s)$ . The  $\hat{i}_c(s)$  term is again represented in Fig. 18.5a by an independent current source, and the  $\hat{v}(s)$  term is represented by a dependent current source. The quantity  $-\hat{v}_g(s)D^2/D'R$  is modeled by an effective ac resistor having the negative value  $-D'R/D^2$ .

Figures 18.5a,b can now be combined into the small-signal two-port model of Fig. 18.6. The current-programmed buck and boost converters can also be modeled by a two-port equivalent circuit, of the same form. Table 18.1 lists the model parameters for the basic buck, boost, and buck-boost converters.



**Fig. 18.6** Two-port small-signal equivalent circuit used to model the current-programmed CCM buck, boost, and buck-boost converters

**Table 18.1** Current-programmed mode small-signal equivalent circuit parameters, simple model

Converter	$g_1$	$f_1$	$r_1$	$g_2$	$f_2$	$r_2$
Buck	$\frac{D}{R}$	$D\left(1 + \frac{sL}{R}\right)$	$-\frac{R}{D^2}$	0	1	$\infty$
Boost	0	1	$\infty$	$\frac{1}{D'R}$	$D'\left(1 - \frac{sL}{D^2R}\right)$	$R$
Buck-boost	$-\frac{D}{R}$	$D\left(1 + \frac{sL}{D'R}\right)$	$-\frac{D'R}{D^2}$	$-\frac{D^2}{D'R}$	$-D'\left(1 - \frac{sDL}{D^2R}\right)$	$\frac{R}{D}$

The two-port equivalent circuit can now be solved, to find the converter transfer functions and output impedance. The control-to-output transfer function is found by setting  $\hat{v}_g$  to zero. Solution for the output voltage then leads to the transfer function  $G_{vc}(s)$ :

$$G_{vc}(s) = \left. \frac{\hat{v}(s)}{\hat{i}_c(s)} \right|_{\hat{v}_g=0} = f_2 \left( r_2 \| R \| \frac{1}{sC} \right) \quad (18.10)$$

Substitution of the model parameters for the buck-boost converter yields

$$G_{vc}(s) = -R \frac{D'}{1+D} \frac{\left(1 - s \frac{DL}{D^2R}\right)}{\left(1 + s \frac{RC}{1+D}\right)} \quad (18.11)$$

It can be seen that this transfer function contains only one pole; the pole due to the inductor has been lost. The dc gain is now directly dependent on the load resistance  $R$ . In addition, the transfer function contains a right half-plane zero whose corner frequency is unchanged from the duty-cycle-controlled case. In general, introduction of current programming alters the transfer function poles and dc gain, but not the zeroes.

The line-to-output transfer function  $G_{vg}(s)$  is found by setting the control input  $\hat{i}_c$  to zero, and then solving for the output voltage. The result is

$$G_{vg}(s) = \left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\hat{i}_c=0} = g_2 \left( r_2 \| R \| \frac{1}{sC} \right) \quad (18.12)$$

Substitution of the parameters for the buck-boost converter leads to

$$G_{vg}(s) = -\frac{D^2}{1-D^2} \frac{1}{\left(1+s\frac{RC}{1+D}\right)} \quad (18.13)$$

Again, the inductor pole is lost. The output impedance is

$$Z_{out}(s) = r_2 \| R \| \frac{1}{sC} \quad (18.14)$$

For the buck-boost converter, one obtains

$$Z_{out}(s) = \frac{R}{1+D} \frac{1}{\left(1+s\frac{RC}{1+D}\right)} \quad (18.15)$$

### 18.1.2 Averaged Switch Modeling

Additional physical insight into the properties of current programmed converters can be obtained by use of the averaged switch modeling approach developed in Sect. 14.1. Consider the buck converter of Fig. 18.7. We can define the terminal voltages and currents of the switch network as shown. When the buck converter operates in the continuous conduction mode, the switch network average terminal waveforms are related as follows:

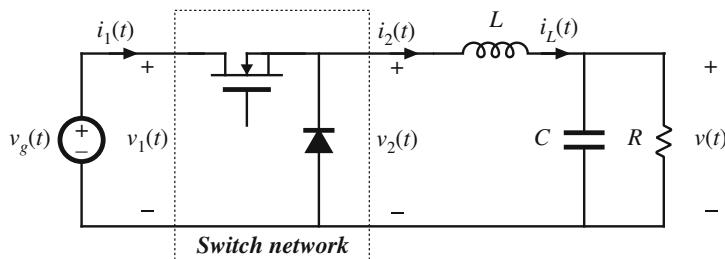
$$\begin{aligned} \langle v_2(t) \rangle_{T_s} &= d(t) \langle v_1(t) \rangle_{T_s} \\ \langle i_1(t) \rangle_{T_s} &= d(t) \langle i_2(t) \rangle_{T_s} \end{aligned} \quad (18.16)$$

We again invoke the approximation in which the inductor current exactly follows the control current. In terms of the switch network terminal current  $i_2$ , we can therefore write

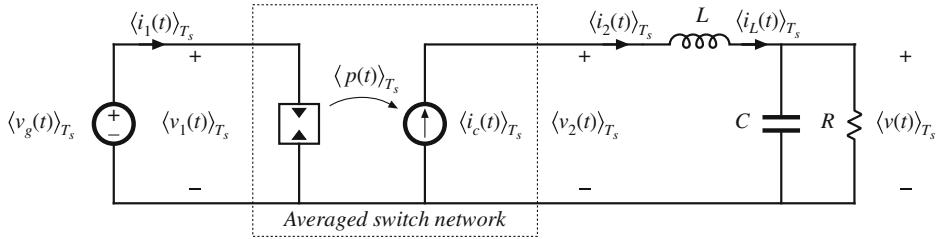
$$\langle i_2(t) \rangle_{T_s} \approx \langle i_c(t) \rangle_{T_s} \quad (18.17)$$

The duty cycle  $d(t)$  can now be eliminated from Eq. (18.16), as follows:

$$\langle i_1(t) \rangle_{T_s} = d(t) \langle i_c(t) \rangle_{T_s} = \frac{\langle v_2(t) \rangle_{T_s}}{\langle v_1(t) \rangle_{T_s}} \langle i_c(t) \rangle_{T_s} \quad (18.18)$$



**Fig. 18.7** Averaged switch modeling of a current-programmed converter: CCM buck example



**Fig. 18.8** Averaged switch model of CPM buck converter

This equation can be written in the alternative form

$$\langle i_1(t) \rangle_{T_s} \langle v_1(t) \rangle_{T_s} = \langle i_c(t) \rangle_{T_s} \langle v_2(t) \rangle_{T_s} = \langle p(t) \rangle_{T_s} \quad (18.19)$$

Equations (18.17) and (18.19) are the desired result, which describes the average terminal relations of the CCM current-programmed buck switch network. Equation (18.17) states that the average terminal current  $\langle i_2(t) \rangle_{T_s}$  is equal to the control current  $\langle i_c(t) \rangle_{T_s}$ . Equation (18.19) states that the input port of the switch network consumes average power  $\langle p(t) \rangle_{T_s}$  equal to the average power flowing out of the switch output port. The averaged equivalent circuit of Fig. 18.8 is obtained.

Figure 18.8 describes the behavior of the current programmed buck converter switch network, in a simple and straightforward manner. The switch network output port behaves as a current source of value  $\langle i_c(t) \rangle_{T_s}$ . The input port follows a power sink characteristic, drawing power from the source  $v_g$  equal to the power supplied by the  $i_c$  current source. Properties of the power source and power sink elements are described in Chaps. 15 and 21.

Similar arguments lead to the averaged switch models of the current programmed boost and buck-boost converters, illustrated in Fig. 18.9. In both cases, the switch network averaged terminal waveforms can be represented by a current source of value  $\langle i_c(t) \rangle_{T_s}$ , in conjunction with a dependent power source or power sink.

A small-signal ac model of the current-programmed buck converter can now be constructed by perturbation and linearization of the switch network averaged terminal waveforms. Let

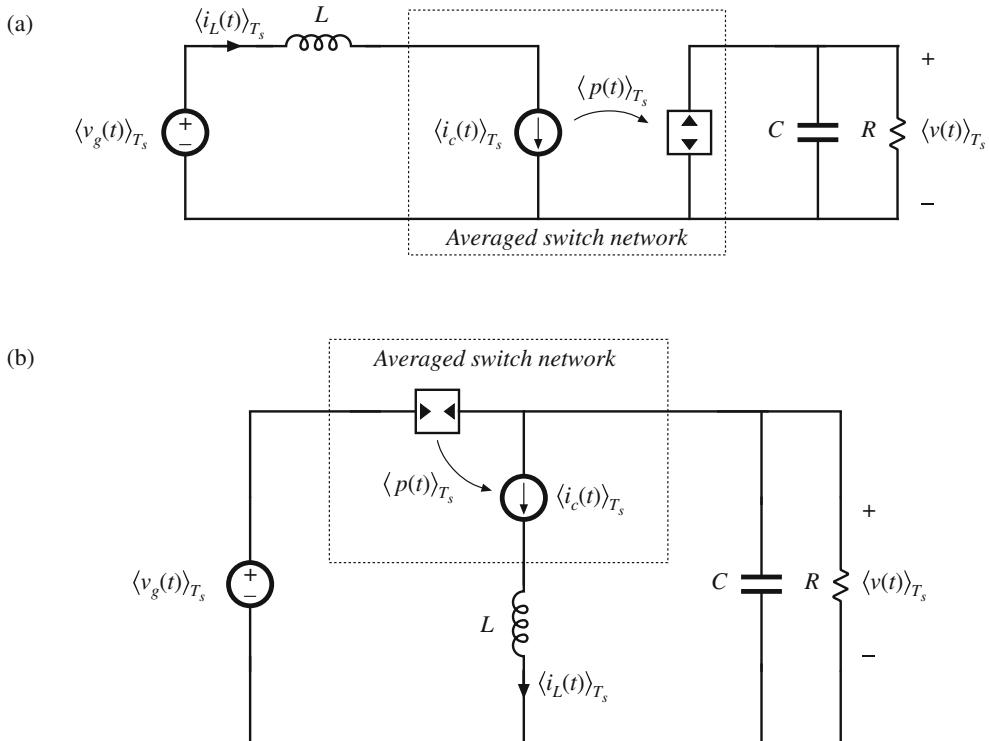
$$\begin{aligned} \langle v_1(t) \rangle_{T_s} &= V_1 + \hat{v}_1(t) \\ \langle i_1(t) \rangle_{T_s} &= I_1 + \hat{i}_1(t) \\ \langle v_2(t) \rangle_{T_s} &= V_2 + \hat{v}_2(t) \\ \langle i_2(t) \rangle_{T_s} &= I_2 + \hat{i}_2(t) \\ \langle i_c(t) \rangle_{T_s} &= I_c + \hat{i}_c(t) \end{aligned} \quad (18.20)$$

Perturbation and linearization of the  $\langle i_c(t) \rangle_{T_s}$  current source of Fig. 18.8 simply leads to a current source of value  $\hat{i}_c(t)$ . Perturbation of the power source characteristic, Eq. (18.19), leads to

$$(V_1 + \hat{v}_1(t))(I_1 + \hat{i}_1(t)) = (I_c + \hat{i}_c(t))(V_2 + \hat{v}_2(t)) \quad (18.21)$$

Upon equating the dc terms on both sides of this equation, we obtain

$$V_1 I_1 = I_c V_2 \Rightarrow I_1 = D I_c \quad (18.22)$$



**Fig. 18.9** Averaged models of CPM boost (a) and CPM buck-boost (b) converters, derived via averaged switch modeling

The linear small-signal ac terms of Eq. (18.21) are

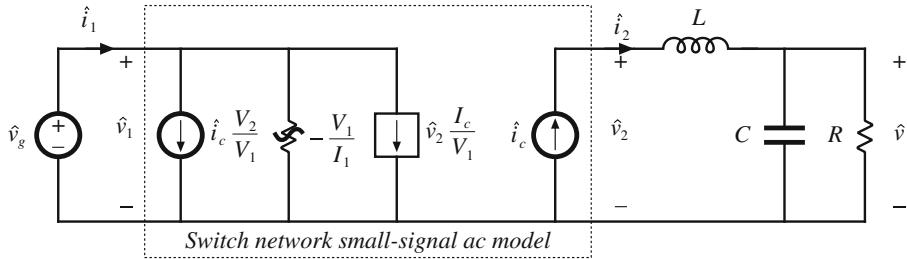
$$\hat{v}_1(t)I_1 + V_1\hat{i}_1(t) = \hat{i}_c(t)V_2 + I_c\hat{v}_2(t) \quad (18.23)$$

Solution for the small-signal switch network input current  $\hat{i}_1(t)$  yields

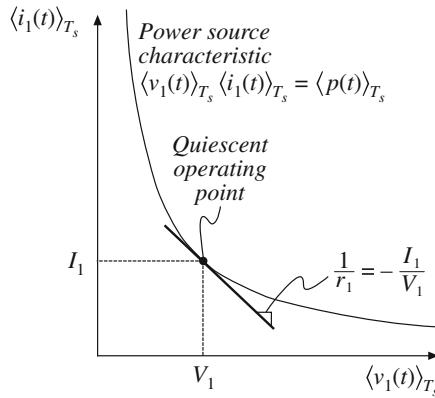
$$\hat{i}_1(t) = \hat{i}_c(t)\frac{V_2}{V_1} + \hat{v}_2(t)\frac{I_c}{V_1} - \hat{v}_1(t)\frac{I_1}{V_1} \quad (18.24)$$

The small-signal ac model of Fig. 18.10 can now be constructed. The switch network output port is again a current source, of value  $\hat{i}_c(t)$ . The switch network input port model is obtained by linearization of the power sink characteristic, as given by Eq. (18.24). The input port current  $\hat{i}_1(t)$  is composed of three terms. The  $\hat{i}_c(t)$  term is modeled by an independent current source, the  $\hat{v}_2(t)$  term is modeled by a dependent current source, and the  $\hat{v}_1(t)$  term is modeled by an effective ac resistor having the negative value  $-V_1/I_1$ . As illustrated in Fig. 18.11, this incremental resistance is determined by the slope of the power sink input port characteristic, evaluated at the quiescent operating point. The power sink leads to a negative incremental resistance because an increase in  $\langle v_1(t) \rangle_{T_s}$  causes a decrease in  $\langle i_1(t) \rangle_{T_s}$ , such that constant  $\langle p(t) \rangle_{T_s}$  is maintained.

The equivalent circuit of Fig. 18.10 can now be simplified by use of the dc relations  $V_2 = DV_1$ ,  $I_2 = V_2/R$ ,  $I_1 = DI_2$ ,  $I_2 = I_c$ . Equation (18.24) then becomes



**Fig. 18.10** Small-signal model of the CCM CPM buck converter, derived by perturbation and linearization of the switch network of Fig. 18.8



**Fig. 18.11** Origin of the input port negative incremental resistance  $r_1$ : the slope of the power sink characteristic, evaluated at the quiescent operating point

$$\hat{i}_1(t) = D\hat{i}_c(t) + \frac{D}{R}\hat{v}_2(t) - \frac{D^2}{R}\hat{v}_1(t) \quad (18.25)$$

Finally, we can eliminate the quantities  $\hat{v}_1$  and  $\hat{v}_2$  in favor of the converter terminal voltages  $\hat{v}_g$  and  $\hat{v}_2$  as follows. The quantity  $\hat{v}_1$  is simply equal to  $\hat{v}_g$ . The quantity  $\hat{v}_2$  is equal to the output voltage  $\hat{v}$  plus the voltage across the inductor,  $sL\hat{i}_c(s)$ . Hence,

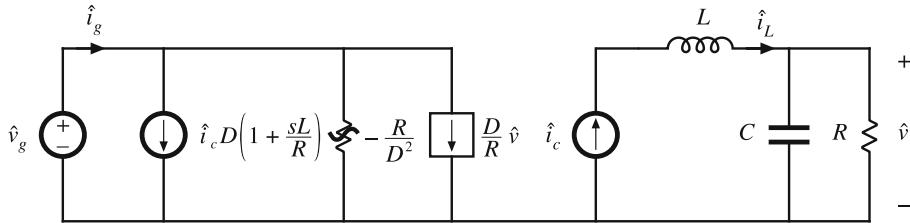
$$\hat{v}_2(s) = \hat{v}(s) + sL\hat{i}_c(s) \quad (18.26)$$

With these substitutions, Eq. (18.25) becomes

$$\hat{i}_1(s) = D\left(1 + s\frac{L}{R}\right)\hat{i}_c(s) + \frac{D}{R}\hat{v}(s) - \frac{D^2}{R}\hat{v}_g(s) \quad (18.27)$$

The equivalent circuit of Fig. 18.12 is now obtained. It can be verified that this equivalent circuit coincides with the model of Fig. 18.6 and the buck converter parameters of Table 18.1.

The approximate small-signal properties of the current-programmed buck converter can now be explained. Since the inductor is in series with the current source  $\hat{i}_c$ , the inductor does not contribute to the control-to-output transfer function. The control-to-output transfer function is determined simply by the relation



**Fig. 18.12** Simplification of the CPM buck converter model of Fig. 18.10, with dependent power source expressed in terms of the output voltage variations

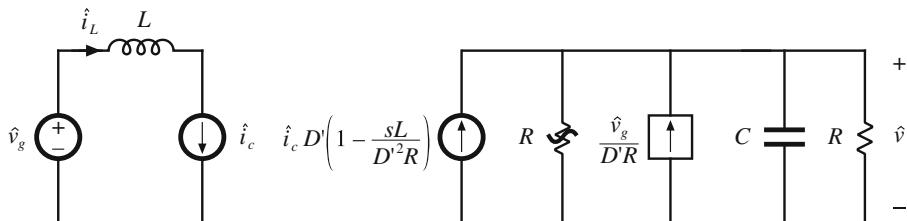
$$G_{vc}(s) = \left. \frac{\hat{v}(s)}{\hat{i}_c(s)} \right|_{\hat{v}_g=0} = \left( R \parallel \frac{1}{sC} \right) \quad (18.28)$$

So current programming transforms the output characteristic of the buck converter into a current source. The power sink input characteristic of the current-programmed buck converter leads to a negative incremental input resistance, as described above. Finally, Fig. 18.12 predicts that the buck converter line-to-output transfer function is zero:

$$G_{vg}(s) = \left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\hat{i}_c=0} = 0 \quad (18.29)$$

Disturbances in  $v_g$  do not influence the output voltage, since the inductor current depends only on  $i_c$ . The current-programmed controller adjusts the duty cycle as necessary to maintain constant inductor current, regardless of variations in  $v_g$ . The more accurate models of Sect. 18.3 predict that  $G_{vg}(s)$  is not zero, but is nonetheless small in magnitude.

Similar arguments lead to the boost converter small-signal equivalent circuit of Fig. 18.13. Derivation of this equivalent circuit is left as a homework problem. In the case of the boost converter, the switch network input port behaves as a current source, of value  $i_c$ , while the output port is a dependent power source, equal to the power apparently consumed by the current source  $i_c$ . In the small-signal model, the current source  $\hat{i}_c$  appears in series with the inductor  $L$ , and hence the converter transfer functions cannot contain poles arising from the inductor. The switch network power source output characteristic leads to an ac resistance of value  $r_2 = R$ . The line-to-output transfer function  $G_{vg}(s)$  is nonzero in the boost converter, since the magnitude of



**Fig. 18.13** Small-signal model of the CCM CPM boost converter, derived via averaged switch modeling and the approximation  $i_L \approx i_c$

the power source depends directly on the value of  $v_g$ . The control-to-output transfer function  $G_{vc}(s)$  contains a right half-plane zero, identical to the right half-plane zero of the duty-cycle-controlled boost converter.

## 18.2 Oscillation for $D > 0.5$

The current-programmed controller of Fig. 18.1 is unstable whenever the steady-state duty cycle is greater than 0.5. To avoid this stability problem, the controller is usually modified by addition of an artificial ramp to the sensed switch current waveform. In this section, the stability of the current programmed controller is analyzed. The effects of the addition of the artificial ramp are explained, using a simple first-order discrete-time analysis. Effects of the artificial ramp on controller noise susceptibility are also discussed.

Figure 18.14 illustrates a generic inductor current waveform of a switching converter operating in the continuous conduction mode. The inductor current changes with a slope  $m_1$  during the first subinterval, and a slope  $-m_2$  during the second subinterval. For the basic nonisolated converters, the slopes  $m_1$  and  $-m_2$  are given by

Buck converter

$$m_1 = \frac{v_g - v}{L} - m_2 = -\frac{v}{L}$$

Boost converter

$$m_1 = \frac{v_g}{L} - m_2 = \frac{v_g - v}{L} \quad (18.30)$$

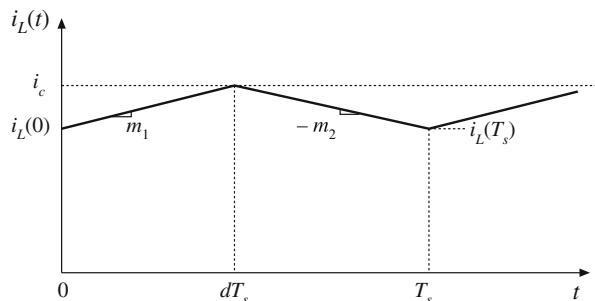
Buck-boost converter

$$m_1 = \frac{v_g}{L} - m_2 = \frac{v}{L}$$

With knowledge of the slopes  $m_1$  and  $-m_2$ , we can determine the general relationships between  $i_L(0)$ ,  $i_c$ ,  $i_L(T_s)$ , and  $dT_s$ .

During the first subinterval, the inductor current  $i_L(t)$  increases with slope  $m_1$ , until  $i_L(t)$  reaches the control signal  $i_c$ . Hence,

$$i_L(dT_s) = i_c = i_L(0) + m_1 dT_s \quad (18.31)$$



**Fig. 18.14** Inductor current waveform of a current-programmed converter operating in the continuous conduction mode

Solution for the duty cycle  $d$  leads to

$$d = \frac{i_c - i_L(0)}{m_1 T_s} \quad (18.32)$$

In a similar manner, for the second subinterval we can write

$$\begin{aligned} i_L(T_s) &= i_L(dT_s) - m_2 d' T_s \\ &= i_L(0) + m_1 d T_s - m_2 d' T_s \end{aligned} \quad (18.33)$$

In steady-state,  $i_L(0) = i_L(T_s)$ ,  $d = D$ ,  $m_1 = M_1$ , and  $m_2 = M_2$ . Insertion of these relationships into Eq. (18.33) yields

$$0 = M_1 D T_s - M_2 D' T_s \quad (18.34)$$

Or,

$$\frac{M_2}{M_1} = \frac{D}{D'} \quad (18.35)$$

Steady-state Eq. (18.35) coincides with the requirement for steady-state volt-second balance on the inductor.

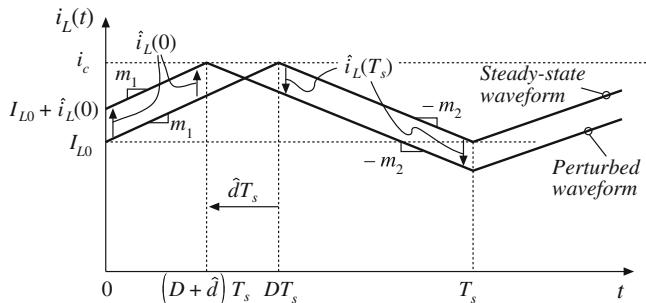
Consider now a small perturbation in  $i_L(0)$ :

$$i_L(0) = I_{L0} + \hat{i}_L(0) \quad (18.36)$$

$I_{L0}$  is a steady-state value of  $i_L(0)$ , which satisfies Eqs. (18.33) and (18.34), while  $\hat{i}_L(0)$  is a small perturbation such that

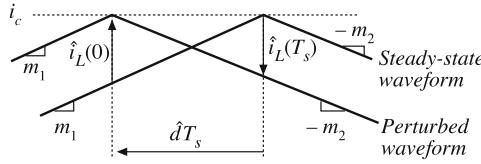
$$|\hat{i}_L(0)| \ll |I_{L0}| \quad (18.37)$$

It is desired to assess the stability of the current-programmed controller, by determining whether this small perturbation eventually decays to zero. To do so, let us solve for the perturbation after  $n$  switching periods,  $\hat{i}_L(nT_s)$ , and determine whether  $\hat{i}_L(nT_s)$  tends to zero for large  $n$ .



**Fig. 18.15** Effect of initial perturbation  $\hat{i}_L(0)$  on inductor current waveform

The steady-state and perturbed inductor current waveforms are illustrated in Fig. 18.15. For clarity, the size of the inductor current perturbation  $\hat{i}_L(0)$  is exaggerated. It is assumed that the converter operates near steady-state, such that the slopes  $m_1$  and  $m_2$  are essentially unchanged. Figure 18.15 is drawn for a positive  $\hat{i}_L(0)$ ; the quantity  $\hat{dT}_s$  is then negative. Since the slopes of



**Fig. 18.16** Expanded view of the steady-state and perturbed inductor current waveforms, near the peak of  $i_L(t)$

the steady-state and perturbed waveforms are essentially equal over the interval  $0 < t < (D + \hat{d})T_s$ , the difference between the waveforms is equal to  $\hat{i}_L(0)$  for this entire interval. Likewise, the difference between the two waveforms is a constant  $\hat{i}_L(T_s)$  over the interval  $DT_s < t < T_s$ , since both waveforms then have the slope  $-m_2$ . Note that  $\hat{i}_L(T_s)$  is a negative quantity, as sketched in Fig. 18.15. Hence, we can solve for  $\hat{i}_L(T_s)$  in terms of  $\hat{i}_L(0)$ , by considering only the interval  $(D + \hat{d})T_s < t < DT_s$  as illustrated in Fig. 18.16.

From Fig. 18.16, we can use the steady-state waveform to express  $\hat{i}_L(0)$  as the slope  $m_1$ , multiplied by the interval length  $-\hat{d}T_s$ . Hence,

$$\hat{i}_L(0) = -m_1\hat{d}T_s \quad (18.38)$$

Likewise, we can use the perturbed waveform to express  $\hat{i}_L(T_s)$  as the slope  $-m_2$ , multiplied by the interval length  $-\hat{d}T_s$ :

$$\hat{i}_L(T_s) = m_2\hat{d}T_s \quad (18.39)$$

Elimination of the intermediate variable  $\hat{d}$  from Eqs. (18.38) and (18.39) leads to

$$\hat{i}_L(T_s) = \hat{i}_L(0) \left( -\frac{m_2}{m_1} \right) \quad (18.40)$$

If the converter operating point is sufficiently close to the quiescent operating point, then  $m_2/m_1$  is given approximately by Eq. (18.35). Equation (18.40) then becomes

$$\hat{i}_L(T_s) = \hat{i}_L(0) \left( -\frac{D}{D'} \right) \quad (18.41)$$

A similar analysis can be performed during the next switching period, to show that

$$\hat{i}_L(2T_s) = \hat{i}_L(T_s) \left( -\frac{D}{D'} \right) = \hat{i}_L(0) \left( -\frac{D}{D'} \right)^2 \quad (18.42)$$

After  $n$  switching periods, the perturbation becomes

$$\hat{i}_L(nT_s) = \hat{i}_L((n-1)T_s) \left( -\frac{D}{D'} \right) = \hat{i}_L(0) \left( -\frac{D}{D'} \right)^n \quad (18.43)$$

Note that, as  $n$  tends to infinity, the perturbation  $\hat{i}_L(nT_s)$  tends to zero provided that the characteristic value  $-D/D'$  has magnitude less than one. Conversely, the perturbation  $\hat{i}_L(nT_s)$  becomes large in magnitude when the characteristic value  $\alpha = -D/D'$  has magnitude greater than one:

$$|\hat{i}_L(nT_s)| \rightarrow \begin{cases} 0 & \text{when } -\frac{D}{D'} < 1 \\ \infty & \text{when } -\frac{D}{D'} > 1 \end{cases} \quad (18.44)$$

Therefore, for stable operation of the current-programmed controller, we need  $|\alpha| = D/D' < 1$ , or

$$D < 0.5 \quad (18.45)$$

As an example, consider the operation of the boost converter with the steady-state terminal voltages  $V_g = 20$  V,  $V = 50$  V. Since  $V/V_g = 1/D'$ , the boost converter should operate with  $D = 0.6$ . We therefore expect the current-programmed controller to be unstable. The characteristic value will be

$$\alpha = -\frac{D}{D'} = \left(-\frac{0.6}{0.4}\right) = -1.5 \quad (18.46)$$

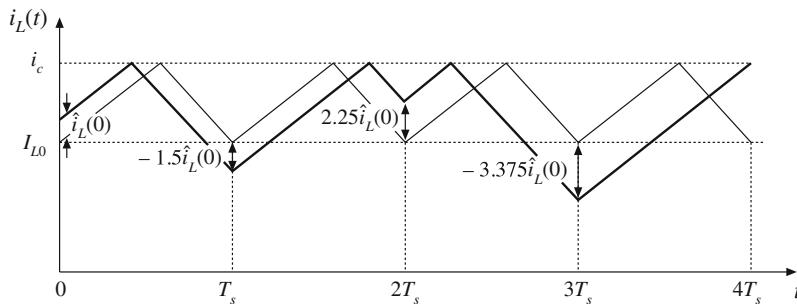
As given by Eq. (18.43), a perturbation in the inductor current will increase by a factor of  $-1.5$  over every switching period. As illustrated in Fig. 18.17, the perturbation grows to  $-1.5\hat{i}_L(0)$  after one switching period, to  $+2.25\hat{i}_L(0)$  after two switching periods, and to  $-3.375\hat{i}_L(0)$  after three switching periods. For the particular initial conditions illustrated in Fig. 18.17, this growing oscillation saturates the Current-programmed controller after three switching periods. The transistor remains on for the entire duration of the fourth switching period. The inductor current and controller waveforms may eventually become oscillatory and periodic in nature, with period equal to an integral number of switching periods. Alternatively, the waveforms may become chaotic. In either event, the controller does not operate as intended.

Figure 18.18 illustrates the inductor current waveforms when the output voltage is decreased to  $V = 30$  V. The boost converter then operates with  $D = 1/3$ , and the characteristic value becomes

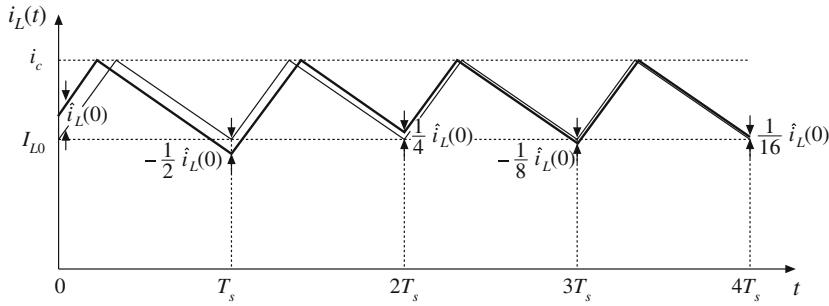
$$\alpha = -\frac{D}{D'} = \left(-\frac{1/3}{2/3}\right) = -0.5 \quad (18.47)$$

Perturbations now decrease in magnitude by a factor of 0.5 over each switching period. A disturbance in the inductor current becomes small in magnitude after a few switching periods.

The instability for  $D > 0.5$  is a well-known problem of current programmed control, and is not dependent on the converter topology. The controller can be rendered stable for all duty cycles by addition of an artificial ramp to the sensed switch current waveform, as illustrated



**Fig. 18.17** Unstable oscillation for  $D = 0.6$



**Fig. 18.18** A stable transient with  $D = \frac{1}{3}$

in Fig. 18.19. This artificial ramp has the qualitative effect of reducing the gain of the inner switch-current-sensing discrete feedback loop. The artificial ramp has slope  $m_a$  as shown. The controller now switches the transistor off when

$$i_a(dT_s) + i_L(dT_s) = i_c \quad (18.48)$$

where  $i_a(t)$  is the artificial ramp waveform. Therefore, the transistor is switched off when the inductor current  $i_L(t)$  is given by

$$i_L(dT_s) = i_c - i_a(dT_s) \quad (18.49)$$

Figure 18.20 illustrates the analog comparison of the inductor current waveform  $i_L(t)$  with the quantity  $[i_c - i_a(t)]$ .

We can again determine the stability of the current-programmed controller by analyzing the change in a perturbation of the inductor current waveform over a complete switching period. Figure 18.21 illustrates steady-state and perturbed inductor current waveforms, in the presence of the artificial ramp. Again, the magnitude of the perturbation  $\hat{i}_L(0)$  is exaggerated. The perturbed waveform is sketched for a positive value of  $\hat{i}_L(0)$ ; this causes  $\hat{d}$ , and usually also  $\hat{i}_L(T_s)$ , to be negative. If the perturbed waveforms are sufficiently close to the quiescent operating point, then the slopes  $m_1$  and  $m_2$  are essentially unchanged, and the relationship between  $\hat{i}_L(0)$  and  $\hat{i}_L(T_s)$  can be determined solely by consideration of the interval  $(D + \hat{d})T_s < t < DT_s$ . The perturbations  $\hat{i}_L(0)$  and  $\hat{i}_L(T_s)$  are expressed in terms of the slopes  $m_1$ ,  $m_2$ , and  $m_a$ , and the interval length  $-\hat{d}T_s$ , as follows:

$$\hat{i}_L(0) = -\hat{d}T_s(m_1 + m_a) \quad (18.50)$$

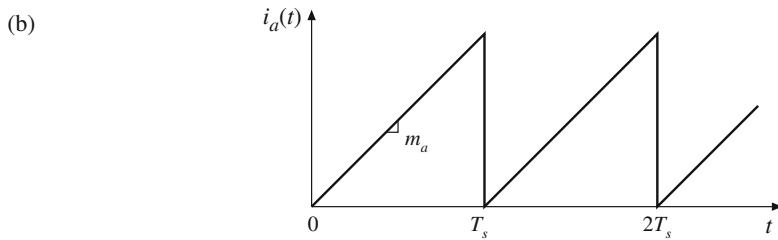
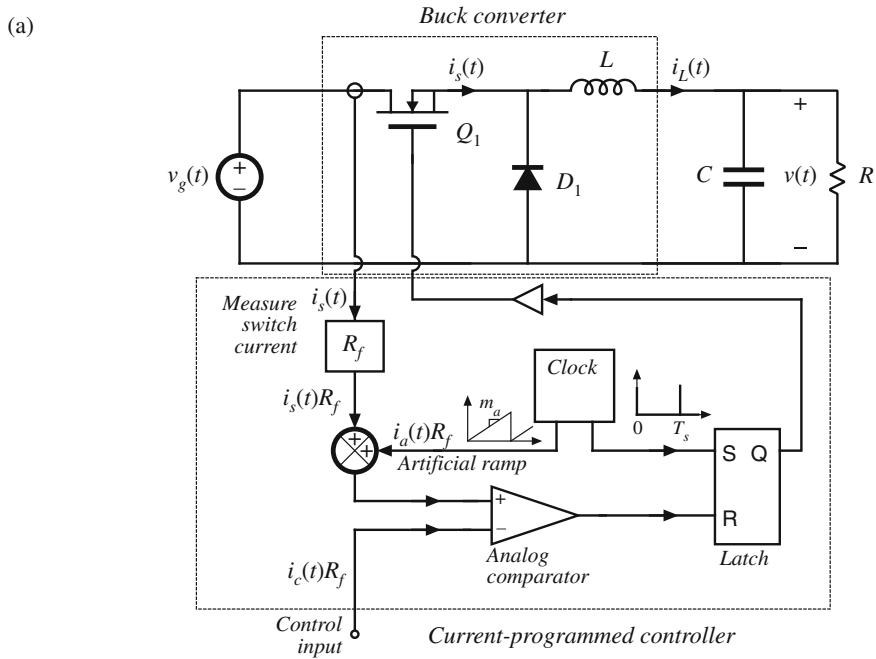
$$\hat{i}_L(T_s) = -\hat{d}T_s(m_a - m_2) \quad (18.51)$$

Elimination of  $\hat{d}$  yields

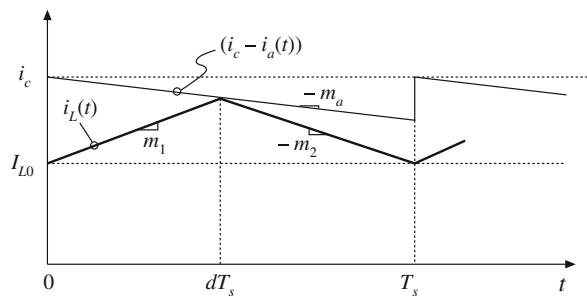
$$\hat{i}_L(T_s) = \hat{i}_L(0) \left( -\frac{m_2 - m_a}{m_1 + m_a} \right) \quad (18.52)$$

A similar analysis can be applied to the  $n^{th}$  switching period, leading to

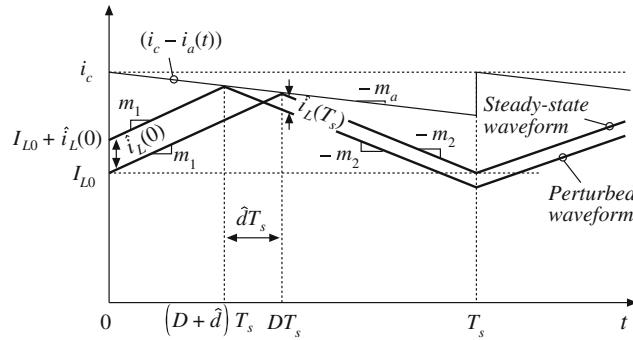
$$\hat{i}_L(nT_s) = \hat{i}_L((n-1)T_s) \left( -\frac{m_2 - m_a}{m_1 + m_a} \right) = \hat{i}_L(0) \left( -\frac{m_2 - m_a}{m_1 + m_a} \right)^n = \hat{i}_L(0)\alpha^n \quad (18.53)$$



**Fig. 18.19** Stabilization of the current-programmed controller by addition of an artificial ramp to the measured switch current waveform: (a) block diagram, (b) artificial ramp waveform



**Fig. 18.20** Addition of artificial ramp: the transistor is now switched off when  $i_L(t) = i_c - i_a(t)$



**Fig. 18.21** Steady-state and perturbed inductor current waveforms, in the presence of an artificial ramp

The evolution of inductor current perturbations is now determined by the characteristic value

$$\alpha = -\frac{m_2 - m_a}{m_1 + m_a} \quad (18.54)$$

For large  $n$ , the perturbation magnitude tends to

$$|\hat{i}_L(nT_s)| \rightarrow \begin{cases} 0 & \text{when } |\alpha| < 1 \\ \infty & \text{when } |\alpha| > 1 \end{cases} \quad (18.55)$$

Therefore, for stability of the current-programmed controller, we need to choose the slope of the artificial ramp  $m_a$  such that the characteristic value  $\alpha$  has magnitude less than one. The artificial ramp gives us an additional degree of freedom, which we can use to stabilize the system for duty cycles greater than 0.5. Note that increasing the value of  $m_a$  causes the numerator of Eq. (18.54) to decrease, while the denominator increases. Therefore, the characteristic value  $\alpha$  attains magnitude less than one for sufficiently large  $m_a$ .

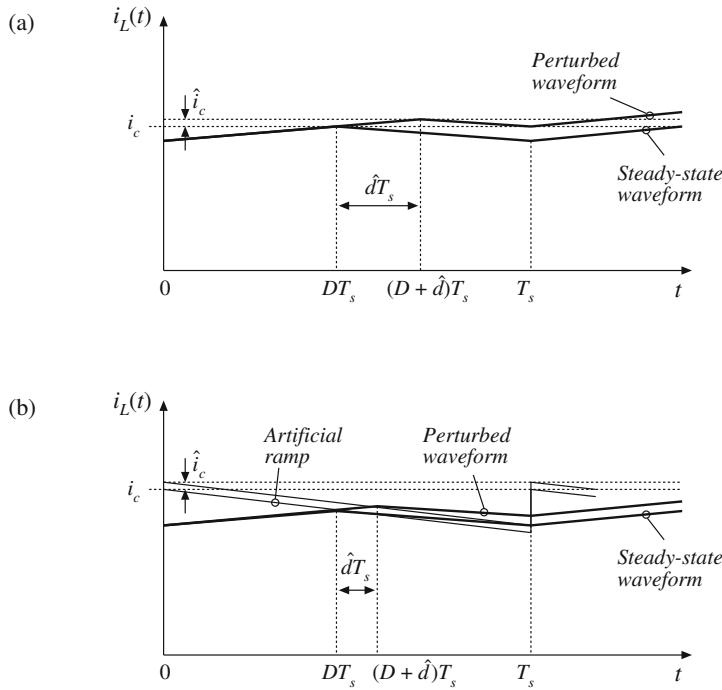
In the conventional voltage regulator application, the output voltage  $v(t)$  is well regulated by the converter control system, while the input voltage  $v_g(t)$  is unknown. Equation (18.30) then predicts that the value of the slope  $m_2$  is constant and known with a high degree of accuracy, for the buck and buck-boost converters. Therefore, let us use Eq. (18.35) to eliminate the slope  $m_1$  from Eq. (18.54), and thereby express the characteristic value  $\alpha$  as a function of the known slope  $m_2$  and the steady-state duty cycle  $D$ :

$$\alpha = -\frac{1 - \frac{m_a}{m_2}}{\frac{D'}{D} + \frac{m_a}{m_2}} \quad (18.56)$$

One common choice of artificial ramp slope is

$$m_a = \frac{1}{2}m_2 \quad (18.57)$$

It can be verified, by substitution of Eq. (18.57) into (18.56), that this choice leads to  $\alpha = -1$  at  $D = 1$ , and to  $|\alpha| < 1$  for  $0 \leq D < 1$ . This is the minimum value of  $m_a$  that leads to stability for all duty cycles. We will see in Sect. 18.3 that this choice of  $m_a$  has the added benefit of causing the ideal line-to-output transfer function  $G_{vg}(s)$  of the buck converter to become zero.



**Fig. 18.22** When noise perturbs a controller signal such as  $i_c$ , the duty cycle is perturbed: (a) with no artificial ramp and small inductor current ripple, the perturbation  $\hat{d}$  is large; (b) an artificial ramp reduces the controller gain, thereby reducing the perturbation  $\hat{d}$

Another common choice of  $m_a$  is

$$m_a = m_2 \quad (18.58)$$

This causes the characteristic value  $\alpha$  to become zero for all  $D$ . As a result,  $\hat{i}_L(T_s)$  is zero for any  $\hat{i}_L(0)$  that does not saturate the controller. The system removes any error after one switching period  $T_s$ . This behavior is known as *deadbeat control*, or *finite settling time*.

It should be noted that the above stability analysis employs a quasi-static approximation, in which the slopes  $m_1$  and  $m_2$  of the perturbed inductor current waveforms are assumed to be identical to the steady-state case. In the most general case, the stability and transient response of a complete system employing current-programmed control must be assessed using a system-wide discrete-time or sampled-data analysis. Nonetheless, in practice the above arguments are found to be sufficient for selection of the artificial ramp slope  $m_a$ .

Current-programmed controller circuits exhibit significant sensitivity to noise. The reason for this is illustrated in Fig. 18.22a, in which the control signal  $i_c(t)$  is perturbed by a small amount of noise represented by  $\hat{i}_c$ . It can be seen that, when there is no artificial ramp and when the inductor current ripple is small, then a small perturbation in  $i_c$  leads to a large perturbation in the duty cycle: the controller has high gain. When noise is present in the controller circuit, then significant jitter in the duty-cycle waveforms may be observed. A solution is to reduce the gain of the controller by introduction of an artificial ramp. As illustrated in Fig. 18.22b, the

same perturbation in  $i_c$  now leads to a reduced variation in the duty cycle. When the layout and grounding of the controller circuit introduce significant noise into the duty-cycle waveform, it may be necessary to add an artificial ramp whose amplitude is substantially greater than the inductor current ripple.

## 18.3 A More Accurate Model

The simple models discussed in the Sect. 18.1 yield much insight into the low-frequency behavior of current-programmed converters. Unfortunately, they do not always describe everything that we need to know. For example, the simple model of the buck converter predicts that the line-to-output transfer function  $G_{vg}(s)$  is zero. While it is true that this transfer function is usually small in magnitude, the transfer function is not equal to zero. To predict the effect of input voltage disturbances on the output voltage, we need to compute the actual  $G_{vg}(s)$ . Furthermore, the simple model does not take into account the effects of inductor current ripple or artificial ramp slope on the average value of the inductor current.

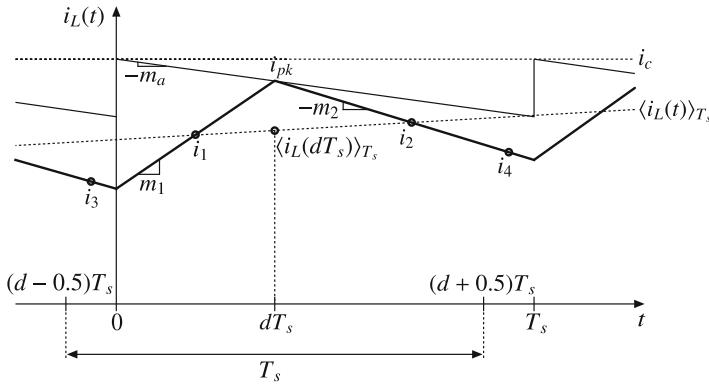
In this section, a more accurate analysis is performed, which does not rely on the approximation  $\langle i_L(t) \rangle_{T_s} \approx i_c(t)$ . The analytical approach of [167, 168] is combined with the controller model of [169]. A functional block diagram of the current programmed controller is constructed, which accounts for the presence of the artificial ramp and for the inductor current ripple. This block diagram is appended to the averaged converter models derived in Chap. 7, leading to a complete converter CPM model. Models for the CPM buck, boost, and buck-boost converters are listed, and the buck converter model is analyzed in detail.

### 18.3.1 Current Programmed Controller Model

Rather than using the approximation  $\langle i_L(t) \rangle_{T_s} = \langle i_c(t) \rangle_{T_s}$ , let us derive a more accurate expression relating the average inductor current  $\langle i_L(t) \rangle_{T_s}$  to the control input  $i_c(t)$ . Application of the moving average (7.3) to  $i_L(t)$ ,

$$\langle i_L(t) \rangle_{T_s} = \frac{1}{T_s} \int_{t-T_s/2}^{t+T_s/2} i_L(\tau) d\tau \quad (18.59)$$

is illustrated in Fig. 18.23 under transient conditions, in which  $i_L(0)$  is not equal to  $i_L(T_s)$ . It can be seen that the peak value  $i_{pk}$  of  $i_L(t)$  differs from  $i_c(t)$ , by the magnitude of the artificial ramp waveform at time  $t = dT_s$ , that is, by  $m_a dT_s$ . Furthermore, the peak and the average values of the inductor current waveform differ because of the inductor current ripple. As a result, a relationship between the average inductor current  $\langle i_L(t) \rangle_{T_s}$  and the control input  $i_c(t)$  must involve the slope  $m_a$  of the artificial ramp, the time interval  $dT_s$ , as well as the inductor current slopes  $m_1$  and  $m_2$ . A difficulty arises because this relationship depends on time  $t$  in (18.59), *i.e.*, on the position of the averaging window of length  $T_s$ . This is in contrast to the averaging applied in Chap. 7 to continuous conduction mode waveforms with duty cycle  $d$  being an independent control input, where we found that the same results are obtained regardless of the position of the averaging window within a switching period. In current-programmed control, however, duty cycle  $d$  is not an independent control input, but is instead determined by the value of the control input  $i_c(t)$  at  $dT_s$ . Just as in the pulse-width modulator discussed in Sect. 7.3, *sampling* of the control input occurs at the modulated edge of the switch control signal, at  $dT_s$ . Indeed, as shown



**Fig. 18.23** Accurate determination of the relationship between the average inductor current  $\langle i_L(t) \rangle_{T_s}$  and  $i_c$

in Fig. 18.23, it is the value of  $i_c(dT_s)$  that determines the duty cycle  $d$  in the switching period shown. Hence, the proper relationship between  $\langle i_L(t) \rangle_{T_s}$  and  $i_c(t)$  is determined by finding the average inductor current in (18.59) at the modulator sampling time  $t = dT_s$ ,

$$\langle i_L \rangle_{T_s} = \langle i_L(dT_s) \rangle_{T_s} = \frac{1}{T_s} \int_{(d-0.5)T_s}^{(d+0.5)T_s} i_L(\tau) d\tau \quad (18.60)$$

The averaging window in Eq. (18.60) is shown in Fig. 18.23 for the case  $d < 0.5$ . Averaging can be performed by splitting the averaging window into three subintervals: from  $(d - 0.5)T_s$  to 0, from 0 to  $dT_s$ , and from  $dT_s$  to  $(d + 0.5)T_s$ . Integration can be simplified by adding the areas of the three trapezoids having mid-point heights equal to  $i_3$ ,  $i_1$ ,  $i_2$ , respectively, and subtracting the area of the trapezoid having the mid-point height of  $i_4$  and with the base extending from  $(d + 0.5)T_s$  to  $T_s$ ,

$$i_L(dT_s) \rangle_{T_s} = (0.5 - d)i_3 + di_1 + d'i_2 - (0.5 - d)i_4 \quad (18.61)$$

$$i_L(dT_s) \rangle_{T_s} = di_1 + d'i_2 - (0.5 - d)(i_4 - i_3) \quad (18.62)$$

Equation (18.62) can be simplified by noting that the time interval between the midpoints  $i_4$  and  $i_3$  is  $T_s$ , while the time interval between the midpoints  $i_1$  and  $i_2$  is  $T_s/2$ . Since the slope between the midpoint values is the same,  $i_4 - i_3 = 2(i_2 - i_1)$ . As a result, Eq. (18.62) becomes

$$\begin{aligned} \langle i_L \rangle_{T_s} &= di_1 + d'i_2 - 2(0.5 - d)(i_2 - i_1) \\ &= d'i_1 + di_2 \end{aligned} \quad (18.63)$$

The literature includes a number of different approaches to CPM modeling, most notably [165, 169, 171, 172]; an important difference between these is in how they average the inductor current [175]. The above relationship, originally derived in [107], differs from various alternative expressions reported in literature. If, for example, the averaging window is centered at  $t = T_s/2$ , extending between 0 and  $T_s$ , a different relationship  $\langle i_L \rangle_{T_s} = di_1 + d'i_2$  is obtained [169]. In equilibrium,  $i_1 = i_2$ , and this alternative expression becomes equivalent to Eq. (18.63). Similarly, predictions of low-frequency dynamics are essentially the same. However, small but

conceptually important differences are found in predictions of high-frequency dynamics. As discussed further in Sect. 18.7, Eq. (18.63), which is based on correctly positioning the averaging window, leads to a small-signal averaged ac model validated by exact sampled-data analysis. The above result is consistent with the averaging definition of Eq. (7.3).

From Fig. 18.23, it follows that the midpoint currents in Eq. (18.63) can be found as

$$i_1 = i_{pk} - \frac{m_1}{2}dT_s \quad (18.64)$$

$$i_2 = i_{pk} - \frac{m_2}{2}d'T_s \quad (18.65)$$

where

$$i_{pk} = i_c - m_a dT_s \quad (18.66)$$

Substitution of Eqs. (18.64), (18.65), and (18.66) into Eq. (18.63) yields the desired large-signal relationship between  $\langle i_L \rangle_{T_s}$  and  $i_c$ :

$$\langle i_L \rangle_{T_s} = i_c - m_a dT_s - \frac{m_1 + m_2}{2} dd' T_s \quad (18.67)$$

This equation exposes how the inductor current ripple and the artificial ramp can cause the average inductor current  $\langle i_L \rangle_{T_s}$  to differ from the control input  $i_c$ .

### 18.3.2 Small-Signal Averaged Model

A small-signal current-programmed controller model is found by perturbation and linearization of Eq. (18.67). Let

$$\begin{aligned} \langle i_L \rangle_{T_s} &= I_L + \hat{i}_L(t) \\ \langle i_c \rangle_{T_s} &= i_c = I_c + \hat{i}_c(t) \\ d(t) &= D + \hat{d}(t) \\ m_1 &= M_1 + \hat{m}_1(t) \\ m_2 &= M_2 + \hat{m}_2(t) \end{aligned} \quad (18.68)$$

Note that it is necessary to perturb the slopes  $m_1$  and  $m_2$ , since the inductor current slope depends on the converter voltages according to Eq. (18.30). For the basic buck, boost, and buck-boost converters, the slope variations are given by

$$\begin{aligned} &\text{Buck converter} \\ \hat{m}_1 &= \frac{\hat{v}_g - \hat{v}}{L} \quad \hat{m}_2 = \frac{\hat{v}}{L} \\ &\text{Boost converter} \\ \hat{m}_1 &= \frac{\hat{v}_g}{L} \quad \hat{m}_2 = \frac{\hat{v} - \hat{v}_g}{L} \\ &\text{Buck-boost converter} \\ \hat{m}_1 &= \frac{\hat{v}_g}{L} \quad \hat{m}_2 = -\frac{\hat{v}}{L} \end{aligned} \quad (18.69)$$

It is assumed that  $m_a$  does not vary:  $m_a = M_a$ . The usual steps of ac perturbation and linearization, including substitution of Eq. (18.68) into Eq. (18.67), cancellation of dc terms, and retention of the first-order ac terms, leads to:

$$\hat{i}_L(t) = \hat{i}_c(t) - \left( M_a + \frac{M_1 + M_2}{2} (1 - 2D) \right) T_s \hat{d}(t) - \frac{DD'T_s}{2} (\hat{m}_1(t) + \hat{m}_2(t)) \quad (18.70)$$

With use of the equilibrium relationship  $DM_1 = D'M_2$ , Eq. (18.70) can be further simplified:

$$\hat{i}_L(t) = \hat{i}_c(t) - \left( M_a + \frac{M_1 - M_2}{2} \right) T_s \hat{d}(t) - \frac{DD'T_s}{2} \hat{m}_1(t) - \frac{DD'T_s}{2} \hat{m}_2(t) \quad (18.71)$$

Finally, solution for  $\hat{d}(t)$  yields

$$\hat{d}(t) = \frac{1}{\left( M_a + \frac{M_1 - M_2}{2} \right) T_s} \left[ \hat{i}_c(t) - \hat{i}_L(t) - \frac{DD'T_s}{2} \hat{m}_1(t) - \frac{DD'T_s}{2} \hat{m}_2(t) \right] \quad (18.72)$$

This is the small-signal relationship that the current-programmed controller follows, to determine  $\hat{d}(t)$  as a function of  $\hat{i}_c(t)$ ,  $\hat{i}_L(t)$ ,  $\hat{m}_1(t)$ , and  $\hat{m}_2(t)$ . Since the quantities  $\hat{m}_1(t)$  and  $\hat{m}_2(t)$  depend on  $\hat{v}_g(t)$  and  $\hat{v}(t)$ , according to Eq. (18.69), we can express Eq. (18.72) in the following form:

$$\hat{d}(t) = F_m \left[ \hat{i}_c(t) - \hat{i}_L(t) - F_g \hat{v}_g(t) - F_v \hat{v}(t) \right] \quad (18.73)$$

where

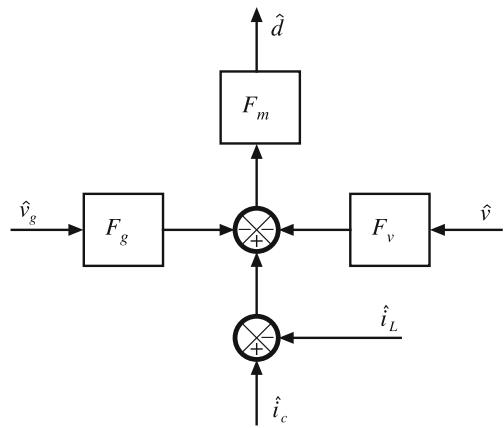
$$F_m = \frac{1}{\left( M_a + \frac{M_1 - M_2}{2} \right) T_s} \quad (18.74)$$

Expressions for the gains  $F_g$  and  $F_v$ , for the basic buck, boost, and buck-boost converters, are listed in Table 18.2. A functional block diagram of the current-programmed controller small-signal model, corresponding to Eq. (18.73), is constructed in Fig. 18.24.

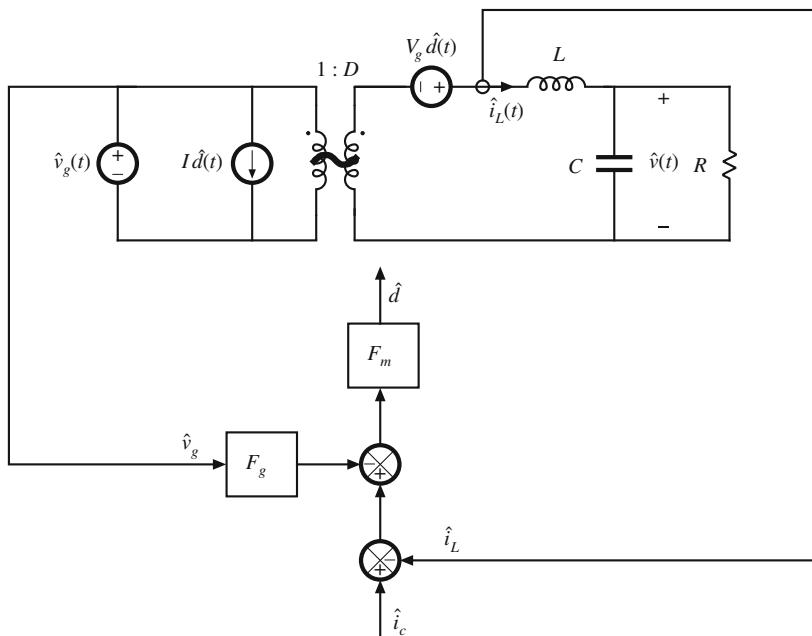
Current-programmed converter models can now be obtained, by combining the controller block diagram of Fig. 18.24 with the averaged converter models derived in Chap. 7. Figures 18.25, 18.26, and 18.27 illustrate the CPM converter models obtained by combination of Fig. 18.24 with, respectively, the buck, boost, and buck-boost models of Fig. 7.18. The current programmed controller contains effective feedback of the inductor current  $\hat{i}_L(t)$  and the output voltage  $\hat{v}(t)$ , as well as effective feedforward of the input voltage  $\hat{v}_g(t)$ .

**Table 18.2** Current-programmed controller gains for basic converters

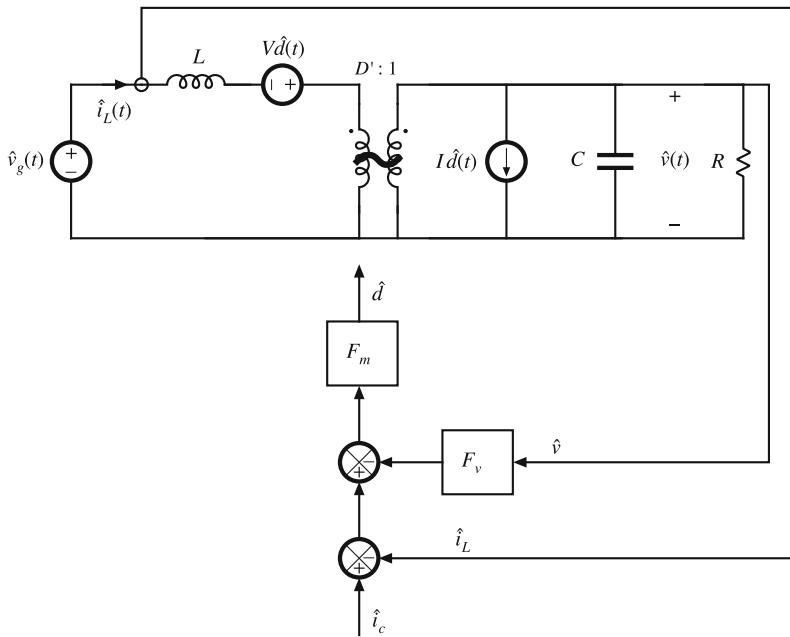
Converter	$F_g$	$F_v$
Buck	$\frac{DD'T_s}{2L}$	0
Boost	0	$\frac{DD'T_s}{2L}$
Buck-boost	$\frac{DD'T_s}{2L}$	$-\frac{DD'T_s}{2L}$



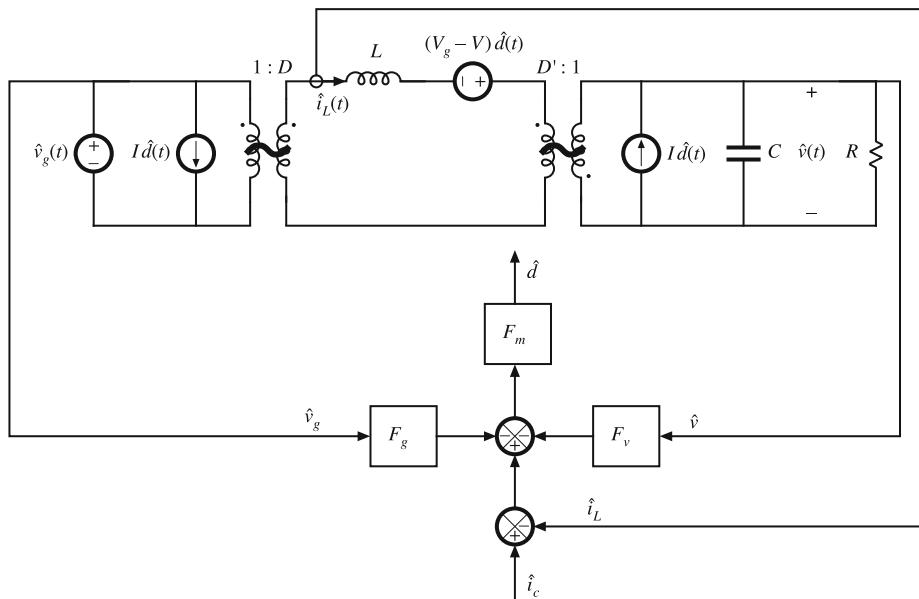
**Fig. 18.24** Functional block diagram of the current-programmed controller



**Fig. 18.25** More accurate model of a current-programmed buck converter



**Fig. 18.26** More accurate model of a current-programmed boost converter



**Fig. 18.27** More accurate model of a current-programmed buck-boost converter

## 18.4 Current-Programmed Transfer Functions

Next, let us solve the models of Sect. 18.3, to determine more accurate expressions for the control-to-output and line-to-output transfer functions of current-programmed buck, boost, and buck-boost converters. As discussed in Chap. 8, the converter output voltage  $\hat{v}$  can be expressed as a function of the duty-cycle  $\hat{d}$  and input voltage  $\hat{v}_g$  variations, using the transfer functions  $G_{vd}(s)$  and  $G_{vg}(s)$ :

$$\hat{v}(s) = G_{vd}(s)\hat{d}(s) + G_{vg}(s)\hat{v}_g(s) \quad (18.75)$$

In a similar manner, the inductor current variation  $\hat{i}$  can be expressed as a function of the duty-cycle  $\hat{d}$  and input voltage  $\hat{v}_g$  variations, by defining the transfer functions  $G_{id}(s)$  and  $G_{ig}(s)$ :

$$\hat{i}_L(s) = G_{id}(s)\hat{d}(s) + G_{ig}(s)\hat{v}_g(s) \quad (18.76)$$

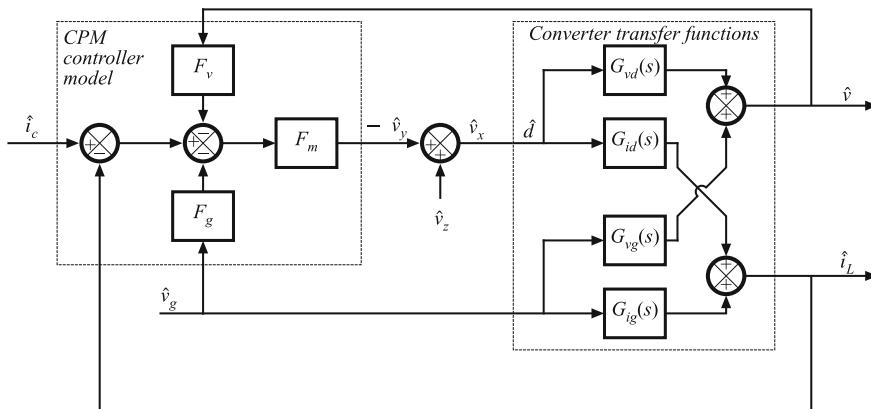
where the transfer functions  $G_{id}(s)$  and  $G_{ig}(s)$  are given by

$$\begin{aligned} G_{id}(s) &= \left. \frac{\hat{i}_L(s)}{\hat{d}(s)} \right|_{\hat{v}_g(s)=0} \\ G_{ig}(s) &= \left. \frac{\hat{i}_L(s)}{\hat{v}_g(s)} \right|_{\hat{d}(s)=0} \end{aligned} \quad (18.77)$$

Figure 18.28 illustrates replacement of the converter circuit models of Figs. 18.25, 18.26, and 18.27 with block diagrams that correspond to Eqs. (18.75) and (18.76). Furthermore, an injection source  $\hat{v}_z$  is inserted between the output of the CPM controller and the duty-cycle input to allow finding the system transfer functions using the Feedback Theorem of Chap. 13.

The control-to-output  $G_{vc}(s)$  and line-to-output  $G_{vg\_cpm}(s)$  transfer functions can now be found, by application of the Feedback Theorem to the block diagram of Fig. 18.28. The closed-loop control-to-output transfer function is given by

$$G_{vc}(s) = \left. \frac{\hat{v}}{\hat{i}_c} \right|_{\substack{\hat{v}_z=0 \\ \hat{v}_g=0}} = G_{\infty vc} \frac{T_i}{1+T_i} + G_{0vc} \frac{1}{1+T_i} \quad (18.78)$$



**Fig. 18.28** Block diagram that models the current-programmed converters of Figs. 18.25, 18.26, and 18.27

where

$$T_i(s) = \left. \frac{\hat{v}_y}{\hat{v}_x} \right|_{\begin{subarray}{l} \hat{i}_c=0 \\ \hat{v}_g=0 \end{subarray}} = F_m (G_{id} + F_v G_{vd}) \quad (18.79)$$

is the loop gain transfer function. Note that the feedback loop comprises two paths, one through  $G_{id}$  and another through  $G_{vd}$  and  $F_v$  blocks, both paths including the CPM modulator gain  $F_m$ . The feedback loop through  $G_{id}$  can conceptually be considered the main feedback loop in a current-programmed controller, while the feedback loop through  $G_{vd}$  and  $F_v$  reflects the effects of the output voltage on the current ripple, and hence on the average inductor current. In a CPM buck converter,  $F_v = 0$ , which means that only the main feedback loop exists.

The closed-loop control-to-output ideal forward gain  $G_{\infty vc}$  is found with  $\hat{v}_g = 0$  and with  $\hat{v}_y$  nulled:

$$G_{\infty vc}(s) = \left. \frac{\hat{v}}{\hat{i}_c} \right|_{\begin{subarray}{l} \hat{v}_g=0 \\ \hat{v}_y \rightarrow 0 \end{subarray}} \quad (18.80)$$

Nulling  $\hat{v}_y$  implies

$$\hat{i}_c - \hat{i}_L - F_v \hat{v} \rightarrow 0 \quad (18.81)$$

Given that  $G_{vd}\hat{v}_x = \hat{v}$  and  $G_{id}\hat{v}_x = \hat{i}_L$ , we have

$$\hat{i}_L = \frac{G_{id}}{G_{vd}} \hat{v} \quad (18.82)$$

Substituting Eq. (18.82) into Eq. (18.81), we have

$$\hat{i}_c - \frac{G_{id}}{G_{vd}} \hat{v} - F_v \hat{v} \rightarrow 0 \quad (18.83)$$

which yields an expression for the ideal forward gain

$$G_{\infty vc}(s) = \left. \frac{\hat{v}}{\hat{i}_c} \right|_{\begin{subarray}{l} \hat{v}_g=0 \\ \hat{v}_y \rightarrow 0 \end{subarray}} = \frac{G_{vd}}{G_{id} + F_v G_{vd}} = \frac{F_m G_{vd}}{T_i} \quad (18.84)$$

Finally, the direct forward transmission through the feedback path is found with  $\hat{v}_g = 0$  and with  $\hat{v}_x$  nulled. By inspection,

$$G_{0vc} = 0 \quad (18.85)$$

Substituting Eqs. (18.79), (18.84), and (18.85) into Eq. (18.78) leads to the desired result:

$$G_{vc}(s) = \frac{F_m G_{vd}}{1 + T_i} = \frac{F_m G_{vd}}{1 + F_m(G_{id} + F_v G_{vd})} \quad (18.86)$$

Similarly, line-to-output transfer function can be found by application of the Feedback Theorem to the block diagram in Fig. 18.28 with  $\hat{i}_c = 0$ ,

$$G_{vg-cpm}(s) = \left. \frac{\hat{v}}{\hat{v}_g} \right|_{\begin{subarray}{l} \hat{v}_z=0 \\ \hat{i}_c=0 \end{subarray}} = G_{\infty vg-cpm} \frac{T_i}{1 + T_i} + G_{0vg-cpm} \frac{1}{1 + T_i} \quad (18.87)$$

where

$$G_{\infty vg-cpm}(s) = \left. \frac{\hat{v}}{\hat{v}_g} \right|_{\begin{subarray}{l} \hat{i}_c=0 \\ \hat{v}_y \rightarrow 0 \end{subarray}} = \frac{-F_m F_g G_{vd} + F_m (G_{vg} G_{id} - G_{ig} G_{vd})}{T_i} \quad (18.88)$$

$$G_{0vg-cpm}(s) = \left. \frac{\hat{v}}{\hat{v}_g} \right|_{\begin{subarray}{l} \hat{i}_c=0 \\ \hat{v}_x \rightarrow 0 \end{subarray}} = G_{vg} \quad (18.89)$$

The current-programmed line-to-output transfer function is obtained by substitution of Eqs. (18.79), (18.88) and (18.89) into Eq. (18.87):

$$G_{vg-cpm}(s) = \left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\hat{i}_c(s)=0} = \frac{G_{vg} - F_m F_g G_{vd} + F_m (G_{vg} G_{id} - G_{ig} G_{vd})}{1 + F_m (G_{id} + F_v G_{vd})} \quad (18.90)$$

Equations (18.86) and (18.90) are general expressions for the important transfer functions of single-inductor current-programmed converters operating in the continuous conduction mode.

### 18.4.1 Discussion

The controller model of Eq. (18.73) and Fig. 18.24 accounts for the differences between  $i_L$  and  $i_c$  that arise by two mechanisms: the inductor current ripple and the artificial ramp. The inductor current ripple causes the peak and average values of the inductor current to differ; this leads to a deviation between the average inductor current and  $i_c$ . Since the magnitude of the inductor current ripple is a function of the converter input and capacitor voltages, this mechanism introduces  $\hat{v}_g$  and  $\hat{v}$  dependencies into the controller small-signal block diagram. Thus, the  $F_g$  and  $F_v$  gain blocks of Fig. 18.24 model the small-signal effects of the inductor current ripple. For operation deep in continuous conduction mode ( $2L/RT_s \gg 1$ ), the inductor current ripple is small. The  $F_g$  and  $F_v$  gain blocks can then be ignored, and the inductor current ripple has negligible effect on the current-programmed controller gain.

The artificial ramp also causes the average inductor current to differ from  $i_c$ . This is modeled by the gain block  $F_m$ . With no artificial ramp,  $M_a = 0$ , Eq. (18.74) implies that the modulator gain  $F_m$  tends to infinity if  $M_1 = M_2$ , which corresponds to operation at  $D = 0.5$ . If  $M_2 > M_1$  ( $D > 0.5$ ),  $F_m$  becomes negative, which implies positive feedback in the current control loop. The nature of instability and oscillations for  $D > 0.5$ , as well as the need for the artificial ramp, have been addressed in Sect. 18.2 using discrete-time techniques. According to Eqs. (18.56) and (18.57) an artificial ramp with  $M_a \geq M_2/2$  results in a stable current-programmed controller for any  $D$ ,  $0 \leq D < 1$ . One may verify that this artificial ramp slope  $M_a \geq M_2/2$  also results in a finite, positive value for the modulator gain  $F_m$  for any  $D$ .

Consider operation at  $D < 0.5$  with no artificial ramp,  $M_a = 0$ . The current-programmed modulator gain  $F_m$  is very large if  $M_1$  and  $M_2$  are very small, i.e., if the inductor current ripple can be neglected. The current-programmed control systems of Figs. 18.25, 18.26, and 18.27 then effectively have very large loop gain  $T_i$ , so that the signal at the input to the  $F_m$  block ( $\hat{d}/F_m$ ) tends to zero. The block diagram then predicts that

$$\frac{\hat{d}}{F_m} = 0 = \hat{i}_c - \hat{i}_L - F_g \hat{v}_g - F_v \hat{v} \quad (18.91)$$

In the case of negligible inductor current ripple ( $F_g \rightarrow 0$  and  $F_v \rightarrow 0$ ), this equation further reduces to

$$0 = \hat{i}_c - \hat{i}_L \quad (18.92)$$

which coincides with the simple approximation employed in Sect. 18.1. Hence, the transfer functions predicted in this section reduce to the results of Sect. 18.1 in case of no artificial ramp and negligible inductor current ripple. In the limit when  $F_m \rightarrow \infty$ ,  $F_g \rightarrow 0$ , and  $F_v \rightarrow 0$ , the control-to-output transfer function (18.86) reduces to

$$\lim_{\substack{F_m \rightarrow \infty \\ F_g \rightarrow 0 \\ F_v \rightarrow 0}} G_{vc}(s) = \frac{G_{vd}}{G_{id}} \quad (18.93)$$

and the line-to-output transfer function (18.90) reduces to

$$\lim_{\substack{F_m \rightarrow \infty \\ F_g \rightarrow 0 \\ F_v \rightarrow 0}} G_{vg-cpm}(s) = \frac{G_{vg}G_{id} - G_{ig}G_{vd}}{G_{id}} \quad (18.94)$$

It can be verified that Eqs. (18.93) and (18.94) are equivalent to the transfer functions derived in Sect. 18.1.

When an artificial ramp is present, then the CPM modulator gain  $F_m$  is reduced. The current-programmed controller no longer perfectly regulates the inductor current  $i_L$ , and the terms on the right-hand side of Eq. (18.91) do not add to zero. In the extreme case of a very large artificial ramp (large  $M_a$  and hence small  $F_m$ ), the current-programmed controller degenerates to duty-cycle control. The artificial ramp and analog comparator of Fig. 18.19 then function as a pulse-width modulator similar to Fig. 7.29, with small-signal gain  $F_m$ . For small  $F_m$ , the control-to-output transfer function (18.86) reduces to

$$\lim_{\text{small } F_m} G_{vc}(s) = F_m G_{vd}(s) \quad (18.95)$$

which coincides with conventional duty-cycle control. Likewise, Eq. (18.90) reduces to

$$\lim_{\text{small } F_m} G_{vg-cpm}(s) = G_{vg} \quad (18.96)$$

which is the line-to-output transfer function for conventional duty cycle control.

### 18.4.2 Current-Programmed Transfer Functions of the CCM Buck Converter

The control-to-output transfer function  $G_{vd}(s)$  and line-to-output transfer function  $G_{vg}(s)$  of the CCM buck converter with duty-cycle control are tabulated in Chap. 8, by analysis of the equivalent circuit model in Fig. 7.18a. The results are

$$G_{vd}(s) = \frac{V}{D} \frac{1}{den(s)} \quad (18.97)$$

$$G_{vg}(s) = D \frac{1}{den(s)} \quad (18.98)$$

where the denominator polynomial is

$$\text{den}(s) = 1 + s \frac{L}{R} + s^2 LC \quad (18.99)$$

The inductor current transfer functions  $G_{id}(s)$  and  $G_{ig}(s)$  defined by Eqs. (18.76) and (18.77) are also found by solution of the equivalent circuit model in Fig. 7.18a, with the following results:

$$G_{id}(s) = \frac{V}{DR} \frac{(1 + sRC)}{\text{den}(s)} \quad (18.100)$$

$$G_{ig}(s) = \frac{D}{R} \frac{(1 + sRC)}{\text{den}(s)} \quad (18.101)$$

where  $\text{den}(s)$  is again given by Eq. (18.99).

With no artificial ramp and negligible ripple, the control-to-output transfer function reduces to the ideal expression (18.93). Substitution of Eqs. (18.97) and (18.100) yields

$$\lim_{\substack{F_m \rightarrow \infty \\ F_g \rightarrow 0 \\ F_v \rightarrow 0}} G_{vc}(s) = \frac{G_{vd}(s)}{G_{id}(s)} = \frac{R}{1 + sRC} \quad (18.102)$$

Under the same conditions, the line-to-output transfer function reduces to the ideal expression (18.94). Substitution of Eqs. (18.97) to (18.101) leads to

$$\lim_{\substack{F_m \rightarrow \infty \\ F_g \rightarrow 0 \\ F_v \rightarrow 0}} G_{vg-cpm}(s) = \frac{G_{vg}(s)G_{id}(s) - G_{vd}(s)G_{ig}(s)}{G_{id}(s)} = 0 \quad (18.103)$$

Equations (18.102) and (18.103) coincide with the expressions derived in Sect. 18.1 for the CCM buck converter.

For arbitrary  $F_m$ ,  $F_v$ , and  $F_g$ , the control-to-output transfer function is given by Eq. (18.86). According to Table 18.2,  $F_v = 0$  for the buck converter. Substitution of Eqs. (18.97) to (18.101) into Eq. (18.86) yields

$$G_{vc}(s) = \frac{F_m G_{vd}}{1 + F_m G_{id}} = \frac{F_m \left( \frac{V}{DR} \frac{1}{\text{den}(s)} \right)}{1 + F_m \left( \frac{V}{DR} \frac{1 + sRC}{\text{den}(s)} \right)} \quad (18.104)$$

Simplification leads to

$$G_{vc}(s) = \frac{F_m \frac{V}{D}}{\text{den}(s) + \frac{F_m V}{DR} (1 + sRC)} \quad (18.105)$$

Finally, the control-to-output transfer function can be written in the following normalized form:

$$G_{vc}(s) = \frac{G_{c0}}{1 + \frac{s}{Q_c \omega_c} + \left( \frac{s}{\omega_c} \right)^2} \quad (18.106)$$

where

$$G_{c0} = \frac{V}{D} \frac{F_m}{1 + \frac{F_m V}{DR}} \quad (18.107)$$

$$\omega_c = \frac{1}{\sqrt{LC}} \sqrt{1 + \frac{F_m V}{DR}} \quad (18.108)$$

$$Q_c = R \sqrt{\frac{C}{L}} \frac{\sqrt{1 + \frac{F_m V}{DR}}}{1 + \frac{RCF_m V}{DL}} \quad (18.109)$$

In the above equations, the salient features  $G_{c0}$ ,  $\omega_c$ , and  $Q_c$  are expressed as the duty ratio-control value, multiplied by a factor that accounts for the effects of current-programmed control.

It can be seen from Eq. (18.109) that current programming tends to reduce the  $Q$ -factor of the poles. For large  $F_m$ ,  $Q_c$  varies as  $F_m^{-1/2}$ ; consequently, the poles become real and well-separated in magnitude. The low- $Q$  approximation of Sect. 8.1.7 then predicts that the low-frequency pole  $\omega_{p1}$  becomes

$$\omega_{p1} = Q_c \omega_c = \frac{R}{L} \frac{1 + \frac{F_m V}{DR}}{1 + \frac{RCF_m V}{DL}} \quad (18.110)$$

For large  $F_m$ , the pole frequency can be further approximated as

$$f_{p1} \approx \frac{1}{2\pi} \frac{1}{RC} \quad (18.111)$$

which coincides with the low-frequency pole predicted by the simple model of Sect. 18.1. The low- $Q$  approximation also predicts that the high-frequency pole  $\omega_{hf}$  becomes

$$\omega_{hf} \approx \frac{\omega_c}{Q_c} = \frac{1}{RC} \left( 1 + \frac{RCF_m V}{DL} \right) \quad (18.112)$$

For large  $F_m$ , the pole frequency  $f_{hf}$  can be further approximated as

$$f_{hf} \approx \frac{1}{2\pi} \frac{F_m V}{DL} \quad (18.113)$$

Using  $F_m$  from Eq. (18.74),  $V/L = M_2$ , and  $M_1 D = M_2 D'$ ,  $f_{hf}$  can be expressed as

$$f_{hf} = \frac{f_s}{\pi} \frac{M_1 + M_2}{2M_a + M_1 - M_2} = \frac{f_s}{\pi} \frac{1}{1 + 2D \left( \frac{M_a}{M_2} - 1 \right)} \quad (18.114)$$

It follows that the high-frequency pole is typically predicted to lie near to or even greater than the switching frequency  $f_s$ , well above the range of frequencies where the averaged model based on the continuous-time averaged analysis employed here can be considered valid. It should be pointed out that the converter switching and modulator sampling processes lead to discrete-time phenomena that affect the high-frequency behavior of the converter, as discussed further in Sect. 18.7.

For arbitrary  $F_m$ ,  $F_v$ , and  $F_g$ , the current-programmed line-to-output transfer function  $G_{vg-cpm}(s)$  is given by Eq. (18.90). In the case of the buck converter, the quantity  $(G_{vg}G_{id} - G_{vd}G_{ig})$  is equal to zero. Furthermore,  $F_v = 0$ . Hence, Eq. (18.90) becomes

$$G_{vg-cpm}(s) = \frac{G_{vg} - F_m F_g G_{vd}}{1 + F_m G_{id}} \quad (18.115)$$

Substitution of Eqs. (18.97) to (18.101) into Eq. (18.115) yields

$$G_{vg-cpm}(s) = \frac{\frac{D}{den(s)} - F_m F_g \frac{V}{D} \frac{1}{den(s)}}{1 + F_m \left( \frac{V}{DR} \frac{1 + sRC}{den(s)} \right)} \quad (18.116)$$

Simplification leads to

$$G_{vg-cpm}(s) = \frac{\left( D - F_m F_g \frac{V}{D} \right)}{den(s) + \frac{F_m V}{DR} (1 + sRC)} \quad (18.117)$$

Finally, the current-programmed line-to-output transfer function can be written in the following normalized form:

$$G_{vg-cpm}(s) = \frac{G_{g0}}{1 + \frac{s}{Q_c \omega_c} + \left( \frac{s}{\omega_c} \right)^2} \quad (18.118)$$

where

$$G_{g0} = D \frac{1 - \frac{F_m F_g V}{D^2}}{1 + \frac{F_m V}{DR}} = D \frac{\frac{2M_a - M_2}{2M_a + M_1 - M_2}}{1 + \frac{F_m V}{DR}} \quad (18.119)$$

The quantities  $Q_c$  and  $\omega_c$  are given by Eqs. (18.108) and (18.109).

Equation (18.119) shows how current programming reduces the dc gain of the buck converter line-to-output transfer function. For duty-cycle control ( $F_m \rightarrow 0$ ),  $G_{g0}$  is equal to  $D$ . Nonzero values of  $F_m$  reduce the numerator and increase the denominator of Eq. (18.119), which tends to reduce  $G_{g0}$ . In the ideal case ( $F_m \rightarrow \infty$ ), we have already seen that  $G_{g0}$  becomes zero. Equation (18.119) reveals that nonideal current-programmed buck converters can also exhibit zero  $G_{g0}$ , if the artificial ramp slope  $M_a$  is chosen equal to  $M_2/2$ . The current-programmed controller then prevents input line voltage variations from reaching the output. The mechanism that leads to this result is the effective feedforward of  $v_g$ , inherent in the current-programmed controller via the  $F_g \hat{v}_g$  term in Eq. (18.73). It can be seen from Fig. 18.28 that, when  $F_g F_m G_{vd}(s) = G_{vg}(s)$ , then the feedforward path from  $\hat{v}_g$  through  $F_g$  induces variations in the output  $\hat{v}$  that exactly cancel the  $\hat{v}_g$ -induced variations in the direct forward path of the converter through  $G_{vg}(s)$ . This cancellation occurs in the buck converter when  $M_a = 0.5M_2$ .

### 18.4.3 Results for Basic Converters

The transfer functions of the basic buck, boost, and buck-boost converters with current-programmed control are summarized in Tables 18.3, 18.4, 18.5. Control-to-output and line-to-output transfer functions for both the simple model of Sect. 18.1 and the more accurate model

**Table 18.3** Summary of results for the CPM buck converter

Simple model	Duty-cycle controlled transfer functions	
$\hat{\frac{v}{i_c}} = \frac{R}{1 + sRC}$	$G_{vd}(s) = \frac{V}{D} \frac{1}{den(s)}$	$G_{id}(s) = \frac{V}{DR} \frac{1 + sRC}{den(s)}$
$\hat{\frac{v}{v_g}} = 0$	$G_{vg}(s) = D \frac{1}{den(s)}$	$G_{ig}(s) = \frac{D}{R} \frac{1 + sRC}{den(s)}$
$den(s) = 1 + s \frac{L}{R} + s^2 LC$		
More accurate model		
$\hat{\frac{v}{i_c}} = G_{vc}(s) = G_{c0} \frac{1}{1 + \frac{s}{Q_c \omega_c} + \left(\frac{s}{\omega_c}\right)^2}$	$G_{c0} = \frac{V}{D} \frac{F_m}{\left(1 + \frac{F_m V}{DR}\right)}$	
$\omega_c = \frac{1}{\sqrt{LC}} \sqrt{1 + \frac{F_m V}{DR}}$	$Q_c = R \sqrt{\frac{C}{L} \frac{\sqrt{1 + \frac{F_m V}{DR}}}{\left(1 + \frac{RC F_m V}{DL}\right)}}$	
$\hat{\frac{v}{v_g}} = G_{vg-cpm}(s) = G_{g0} \frac{1}{1 + \frac{s}{Q_c \omega_c} + \left(\frac{s}{\omega_c}\right)^2}$	$G_{g0} = D \frac{\left(1 - \frac{F_m F_g V}{D^2}\right)}{\left(1 + \frac{F_m V}{DR}\right)}$	

**Table 18.4** Summary of results for the CPM boost converter

Simple model	Duty-cycle controlled transfer functions	
$\hat{\frac{v}{i_c}} = \frac{D'R}{2} \frac{\left(1 - s \frac{L}{D'^2 R}\right)}{\left(1 + s \frac{RC}{2}\right)}$	$G_{vd}(s) = \frac{V}{D'} \frac{\left(1 - s \frac{L}{D'^2 R}\right)}{den(s)}$	$G_{id}(s) = \frac{2V}{D'^2 R} \frac{\left(1 + s \frac{RC}{2}\right)}{den(s)}$
$\hat{\frac{v}{v_g}} = \frac{1}{2D'} \frac{1}{\left(1 + s \frac{RC}{2}\right)}$	$G_{vg}(s) = \frac{1}{D'} \frac{1}{den(s)}$	$G_{ig}(s) = \frac{1}{D'^2 R} \frac{\left(1 + sRC\right)}{den(s)}$
$den(s) = 1 + s \frac{L}{D'^2 R} + s^2 \frac{LC}{D'^2}$		
More accurate model		
$\hat{\frac{v}{i_c}} = G_{vc}(s) = G_{c0} \frac{\left(1 - s \frac{L}{D'^2 R}\right)}{1 + \frac{s}{Q_c \omega_c} + \left(\frac{s}{\omega_c}\right)^2}$	$G_{c0} = \frac{V}{D'} \frac{F_m}{\left(1 + \frac{2F_m V}{D'^2 R} + \frac{F_m F_v V}{D'}\right)}$	
$\omega_c = \frac{D'}{\sqrt{LC}} \sqrt{1 + \frac{2F_m V}{D'^2 R} + \frac{F_m F_v V}{D'}}$	$Q_c = D'R \sqrt{\frac{C}{L} \frac{\sqrt{1 + \frac{2F_m V}{D'^2 R} + \frac{F_m F_v V}{D'}}}{\left(1 + RC \frac{F_m V}{L} - \frac{F_m F_v V}{D'}\right)}}$	
$\hat{\frac{v}{v_g}} = G_{vg-cpm}(s) = G_{g0} \frac{1}{1 + \frac{s}{Q_c \omega_c} + \left(\frac{s}{\omega_c}\right)^2}$	$G_{g0} = \frac{1}{D'} \frac{\left(1 + \frac{F_m V}{D'^2 R}\right)}{\left(1 + \frac{2F_m V}{D'^2 R} + \frac{F_m F_v V}{D'}\right)}$	

**Table 18.5** Summary of results for the CPM buck-boost converter

Simple model	Duty-cycle controlled transfer functions		
$\hat{v}_i = -\frac{D'R}{(1+D)} \frac{\left(1-s\frac{DL}{D'^2R}\right)}{\left(1+s\frac{RC}{1+D}\right)}$	$G_{vd}(s) = -\frac{ V }{DD'} \frac{\left(1-s\frac{DL}{D'^2R}\right)}{den(s)}$	$G_{id}(s) = \frac{ V (1+D)}{DD'^2R} \frac{\left(1+s\frac{RC}{(1+D)}\right)}{den(s)}$	
$\hat{v}_g = -\frac{D^2}{1-D^2} \frac{1}{\left(1+s\frac{RC}{1+D}\right)}$	$G_{vg}(s) = -\frac{D}{D'} \frac{1}{den(s)}$	$G_{ig}(s) = \frac{D}{D'^2R} \frac{(1+sRC)}{den(s)}$	
$den(s) = 1 + s\frac{L}{D'^2R} + s^2\frac{LC}{D'^2}$			
More accurate model			
$\hat{v}_i = G_{vc}(s) = G_{c0} \frac{\left(1-s\frac{DL}{D'^2R}\right)}{1 + \frac{s}{Q_c \omega_c} + \left(\frac{s}{\omega_c}\right)^2}$	$G_{c0} = -\frac{ V }{DD'} \frac{F_m}{\left(1 + \frac{F_m V (1+D)}{DD'^2R} - \frac{F_m F_v  V }{DD'}\right)}$	$Q_c = D'R \sqrt{\frac{C}{L}} \frac{\sqrt{1 + \frac{F_m V (1+D)}{DD'^2R} - \frac{F_m F_v  V }{DD'}}}{\left(1 + \frac{F_m V RC}{DL} + \frac{F_m F_v  V }{D'}\right)}$	
$\omega_c = \frac{D'}{\sqrt{LC}} \sqrt{1 + \frac{F_m V (1+D)}{DD'^2R} - \frac{F_m F_v  V }{DD'}}$	$G_{g0} = -\frac{D}{D'} \frac{\left(1 + \frac{F_m V }{D'^2R} - \frac{F_m F_g  V }{D^2}\right)}{\left(1 + \frac{F_m V (1+D)}{DD'^2R} - \frac{F_m F_v  V }{DD'}\right)}$	$\omega_{gz} = \frac{DD'^2R}{ V LF_m F_g} \left(1 + \frac{F_m V }{D'^2R} - \frac{F_m F_g  V }{D^2}\right)$	
$\hat{v}_g = G_{vg-cpm}(s) = G_{g0} \frac{\left(1 + \frac{s}{\omega_{gz}}\right)}{1 + \frac{s}{Q_c \omega_c} + \left(\frac{s}{\omega_c}\right)^2}$			

derived in this section are listed. For completeness, the transfer functions for duty-cycle control are included. In each case, the salient features are expressed as the corresponding quantity with duty-cycle control, multiplied by a factor that accounts for current-programmed control.

The two poles of the line-to-output transfer functions  $G_{vg-cpm}$  and control-to-output transfer functions  $G_{vc}$  of all three converters typically exhibit low  $Q$ -factors in CPM. The low- $Q$  approximation can be applied, as in Eqs. (18.110) to (18.113), to find the low-frequency pole. The line-to-output transfer functions of the boost and buck-boost converters exhibit two poles and one zero, with substantial dc gain.

#### 18.4.4 Addition of an Input Filter to a Current-Programmed Converter

Addition of an input filter to a duty-cycle controlled converter is discussed in Chap. 17, where it is found that effects of input filter on converter transfer functions can be evaluated using the Extra Element Theorem of Chap. 16. In particular, Eq. (17.4) shows how the control-to-output transfer function  $G_{vd}$  is modified by a correction factor, which depends on the impedance ratios  $Z_o/Z_N$  and  $Z_o/Z_D$ , where  $Z_o(s)$  is the filter output impedance,  $Z_D(s)$  is the converter driving-point input impedance, and  $Z_N(s)$  is the converter input impedance determined under the condition that the output voltage is nulled. The input filter design approach of Chap. 17 is based

on meeting the impedance inequalities of Sect. 17.2.3 so that the input filter does not substantially alter the control-to-output transfer function. The same approach can be applied to current-programmed converters.

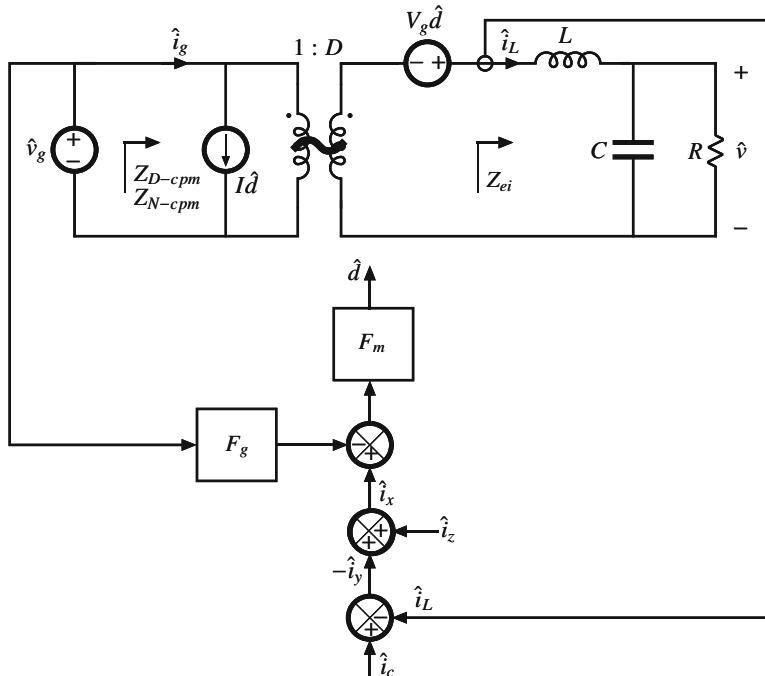
In the presence of an input filter, the CPM control-to-output transfer function is given by

$$G_{vc}(s) = \frac{\hat{v}}{\hat{i}_c} = \left( G_{vc}(s) \Big|_{Z_o(s)=0} \right) \frac{\left( 1 + \frac{Z_o(s)}{Z_{N-cpm}(s)} \right)}{\left( 1 + \frac{Z_o(s)}{Z_{D-cpm}(s)} \right)} \quad (18.120)$$

where

$$G_{vc}(s) \Big|_{Z_o(s)=0} \quad (18.121)$$

is the CPM control-to-output transfer function without the input filter, while  $Z_{N-cpm}$  and  $Z_{D-cpm}$  are input impedances of the current-programmed converter found under two different conditions prescribed by the Extra Element Theorem. The CPM input impedances  $Z_{i-cpm}$  can be found using the converter models shown in Figs. 18.25, 18.26, and 18.27. As an example, small-signal model of a current-programmed buck converter of Fig. 18.25 is shown in Fig. 18.29. The model includes three independent sources: control input  $\hat{i}_c$ , input voltage  $\hat{v}_g$ , and an additional injection source  $\hat{i}_z$ , which will facilitate determining  $Z_{D-cpm}(s)$  using the Feedback Theorem of Chap. 13.



**Fig. 18.29** Small-signal averaged model suitable for finding input impedances in the current-programmed buck converter

To determine  $Z_{N-cpm}$ , the additional injection source is set to zero,  $\hat{i}_z = 0$ . In the presence of  $\hat{i}_c$  and  $\hat{v}_g$ , the output  $\hat{v}$  is nulled. Under these conditions, we find

$$\frac{1}{Z_{N-cpm}(s)} = \left. \frac{\hat{i}_g}{\hat{v}_g} \right|_{\substack{\hat{v} \rightarrow 0 \\ \text{null}}} \quad (18.122)$$

Nulling the output implies nulling the inductor current, which means that  $D\hat{v}_g + V_g\hat{d}$  must equal zero. As a result, we have

$$\hat{d} = -\frac{D}{V_g}\hat{v}_g \quad (18.123)$$

Under the nulling condition, the input current is

$$\left. \hat{i}_g \right|_{\substack{\hat{v} \rightarrow 0 \\ \text{null}}} = I\hat{d} \quad (18.124)$$

Substitution of Eq. (18.123) into Eq. (18.124) yields

$$\frac{1}{Z_{N-cpm}(s)} = \left. \frac{\hat{i}_g}{\hat{v}_g} \right|_{\substack{\hat{v} \rightarrow 0 \\ \text{null}}} = -\frac{D^2}{R} = \frac{1}{Z_N(s)} \quad (18.125)$$

or  $Z_{N-cpm} = -R/D^2$ . The result for  $Z_{N-cpm}$  is exactly the same as the result given by Eq. (17.28) for  $Z_N$  in duty-cycle controlled buck converters. This is not surprising since the nulling condition  $\hat{v} \rightarrow 0$  results in exactly the same converter circuit conditions regardless of the nature of the control input.

To determine  $Z_{D-cpm}$ ,  $\hat{i}_z = 0$  and the independent control input is set to zero,  $\hat{i}_c = 0$ . The converter input admittance, i.e., the inverse of  $Z_{D-cpm}$ , is defined as follows:

$$\frac{1}{Z_{D-cpm}(s)} = \left. \frac{\hat{i}_g}{\hat{v}_g} \right|_{\hat{i}_c=0} \quad (18.126)$$

From the model shown in Fig. 18.29, this transfer function can be found in any number of ways. In contrast to duty-cycle converters, where  $Z_D$  is the converter open-loop input impedance,  $Z_{D-cpm}$  is the input impedance of a current-programmed converter, which includes feedback and feedforward paths. It is therefore convenient to approach finding  $Z_{D-cpm}$  using the Feedback Theorem:

$$\frac{1}{Z_{D-cpm}(s)} = \frac{1}{Z_{\infty D-cpm}(s)} \frac{T_i}{1+T_i} + \frac{1}{Z_{0D-cpm}(s)} \frac{1}{1+T_i} \quad (18.127)$$

where  $T_i(s)$  is the current-programmed loop gain

$$T_i(s) = \left. \frac{\hat{i}_y}{\hat{i}_x} \right|_{\hat{v}_g=0} = F_m G_{id}(s) \quad (18.128)$$

Note that the injection source  $\hat{i}_z$  has been added to the model of Fig. 18.29 specifically for the purpose of finding  $Z_{D-cpm}$  using the Feedback Theorem. The ideal input admittance can be found by nulling  $\hat{i}_y$  in the presence of  $\hat{i}_z$  and  $\hat{v}_g$ . Since  $\hat{i}_c = 0$ , nulling  $\hat{i}_y$  is equivalent to nulling  $\hat{i}_L$ . Hence, the input admittance under the nulling condition is given by

$$\frac{1}{Z_{\infty D-cpm}(s)} = \left. \frac{\hat{i}_g}{\hat{v}_g} \right|_{\hat{i}_y \rightarrow 0} = -\frac{D^2}{R} \quad (18.129)$$

It follows that  $Z_{\infty D-cpm}(s) = -R/D^2$ , which is the same as the result found for  $Z_{N-cpm}$ . The admittance  $1/Z_{0D-cpm}(s)$  is found under the condition that  $\hat{i}_x$  is nulled in the presence of  $\hat{v}_g$  and  $\hat{i}_z$ . Solving the circuit model in Fig. 18.29 results in

$$\frac{1}{Z_{0D-cpm}(s)} = \left. \frac{\hat{i}_g}{\hat{v}_g} \right|_{\hat{i}_x \rightarrow 0} = \frac{D^2 - F_m F_g D V_g}{Z_{ei}} - \frac{F_m F_g D V_g}{R} \quad (18.130)$$

Substitution of Eqs. (18.128), (18.129), and (18.130) into Eq. (18.127) yields an expression for the CPM input impedance  $Z_{D-cpm}$ . Following the discussion in Sect. 18.4.1, let us examine how  $Z_{D-cpm}$  depends on the converter parameters and the artificial ramp slope  $M_a$ . Consider first operation at  $D < 0.5$  with no artificial ramp,  $M_a = 0$ . If inductance  $L$  is relatively large,  $M_1$  and  $M_2$  are small, and therefore CPM gain is very large. A large  $L$  implies that the inductor current ripple is small, and that  $F_g \approx 0$ . Large  $F_m$  implies that  $T_i$  is large and Eq. (18.127) simplifies to:

$$\lim_{\substack{F_m \rightarrow \infty \\ F_g \rightarrow 0}} \frac{1}{Z_{D-cpm}(s)} = -\frac{D^2}{R} \quad (18.131)$$

Next, consider the case when the artificial ramp slope equals  $M_a = M_2/2$ , the minimum value necessary to ensure stability of the CPM controlled for any duty cycle  $D$ . It can be shown that

$$F_m F_g D V_g \Big|_{M_a=M_2/2} = D^2 \quad (18.132)$$

so that Eq. (18.127) becomes

$$\frac{1}{Z_{D-cpm}(s)} \Big|_{M_a=M_2/2} = -\frac{D^2}{R} \quad (18.133)$$

Therefore, for  $M_a = M_2/2$ , both  $Z_{N-cpm}$  and  $Z_{D-cpm}$  are equal to  $-R/D^2$ . For practical values of the artificial ramp slope  $M_a$ ,  $Z_{D-cpm} \approx Z_{N-cpm} = -R/D^2$ .

Finally, consider the case when the artificial ramp slope  $M_a$  is large, so that  $F_m$  and therefore  $T_i$  are small. Equation (18.127) then reduces to

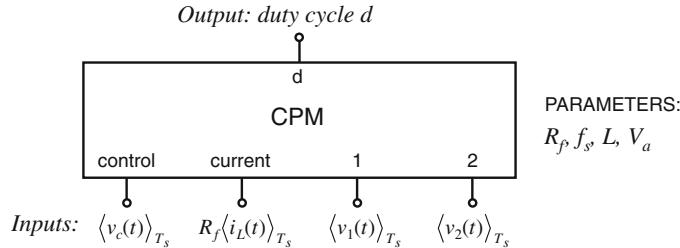
$$\lim_{F_m \rightarrow 0} \frac{1}{Z_{D-cpm}(s)} = -\frac{D^2}{Z_{ei}} \quad (18.134)$$

which means that for large  $M_a$  the CPM input impedance  $Z_{D-cpm}$  approaches the open-loop input impedance  $Z_D$  in Eq. (17.21) for a duty-cycle controlled converter.

Once  $Z_{N-cpm}$  and  $Z_{D-cpm}$  are determined, input filter design for a current-programmed controller follows the approach described in Chap. 17.

## 18.5 Simulation of CPM Controlled Converters

In the current-programmed mode (CPM), the transistor switching is controlled so that the peak transistor current follows a control signal. The transistor duty cycle  $d(t)$  is not directly controlled, but depends on the CPM control input as well as on other converter voltages and currents.

**Fig. 18.30** Current-programmed mode (CPM) subcircuit

In this section, large-signal averaged relationships in CPM are written in a form suitable for implementation as a subcircuit for simulation. The desired form of the CPM averaged subcircuit model is shown in Fig. 18.30. The inputs to the subcircuit are the average control input,

$$\langle v_c(t) \rangle_{T_s} = R_f \langle i_c(t) \rangle_{T_s} \quad (18.135)$$

the sensed average inductor current  $R_f \langle i_L(t) \rangle_{T_s}$ , the average voltage  $\langle v_1(t) \rangle_{T_s}$  applied across the inductor during the interval when the transistor is on, and the average voltage  $\langle v_2(t) \rangle_{T_s}$  applied across the inductor during the interval when the rectifier is on. The model parameters include the equivalent current-sense resistance  $R_f$ , switching frequency  $f_s$ , inductance  $L$ , and the amplitude  $V_a$  of the artificial ramp,

$$V_a = m_a T_s R_f \quad (18.136)$$

given an artificial ramp having slope  $-m_a$  added to the control input. In the subinterval when the transistor is on, the inductor current increases with slope  $m_1$  given by

$$m_1 = \frac{\langle v_1(t) \rangle_{T_s}}{L} \quad (18.137)$$

It is assumed that voltage ripples are small so that the voltage  $v_1(t)$  across the inductor is approximately equal to the averaged value  $\langle v_1(t) \rangle_{T_s}$ . The length of this subinterval is  $d(t)T_s$ . In the second subinterval, when the transistor is off and the rectifier is on, the inductor current decreases with a negative slope  $-m_2$ . Under the assumption that voltage ripples are small, the slope  $m_2$  is given by

$$m_2 = \frac{\langle v_2(t) \rangle_{T_s}}{L} \quad (18.138)$$

The CPM model output is the duty cycle  $d$ . With the inputs and the output shown in Fig. 18.30, the CPM subcircuit can be used in combination with any of the averaged switch subcircuit models developed in Sect. 14.3 to construct an averaged simulation model for a current-programmed converter. The CPM subcircuit model is developed first in Sect. 18.5.1 for the case when the converter operates in continuous conduction mode, and is then extended to include DCM operation in Sect. 18.5.2.

### 18.5.1 Simulation Model for CPM Controlled Converters in CCM

Assuming operation in continuous conduction mode, the large-signal relationship between the average inductor current  $\langle i_L \rangle_{T_s}$  and the control signal  $i_c$  is given by Eq. (18.67),

$$\langle i_L \rangle_{T_s} = i_c - m_a d T_s - \frac{m_1 + m_2}{2} d d' T_s \quad (18.139)$$

Next, the switch duty cycle is found by solving Eq. (18.139). There are many different ways the switch duty cycle can be expressed in terms of other quantities; although mathematically equivalent, these different forms of solving for  $d$  may result in different convergence performance of the numerical solver in the simulator. One approach is to express  $d$  as

$$d = \frac{i_c - \langle i_L(t) \rangle_{T_s}}{\frac{m_1 + m_2}{2} d' T_s + m_a T_s} \quad (18.140)$$

Using Eqs. (18.135), (18.136), (18.137), and (18.138), Eq. (18.140) can be written in the form

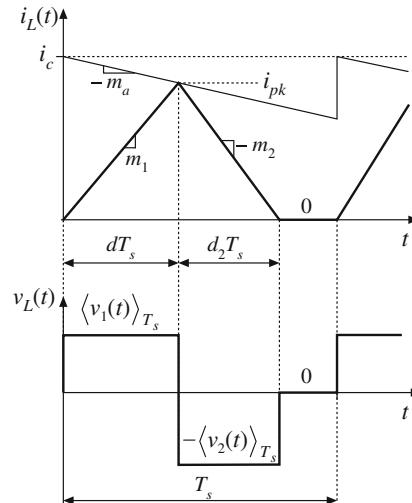
$$d = \frac{2(\langle v_c(t) \rangle_{T_s} - R_f \langle i_L(t) \rangle_{T_s})}{R_f (\langle v_1(t) \rangle_{T_s} + \langle v_2(t) \rangle_{T_s}) d' + 2V_a} \quad (18.141)$$

This implicit expression (notice that  $d$  is on both sides of the equation) is suitable for implementation in a SPICE subcircuit model, which is named CPM-CCM. The numerical solver in the simulator is capable of computing the switch duty cycle  $d$  based on Eq. (18.141).

### 18.5.2 Combined CCM/DCM Simulation Model

Typical inductor current and voltage waveforms of CPM converters operating in discontinuous conduction mode are shown in Fig. 18.31. The length of the second subinterval is  $d_2(t)T_s$ . In CCM, the second subinterval lasts until the end of the switching cycle,

$$d_2 = 1 - d \quad (18.142)$$



**Fig. 18.31** Current-programmed mode waveforms in discontinuous conduction mode

In DCM, the current drops to zero before the end of the switching period. The length of the second subinterval can be computed from:

$$d_2 = \frac{i_{pk}}{m_2 T_s} \quad (18.143)$$

If the converter operates in DCM,  $d_2$  computed from Eq. (18.143) is smaller than  $1 - d$ . If the converter operates in CCM,  $1 - d$  is smaller than  $d_2$  computed from Eq. (18.143). In general, the length of the second subinterval can be found as the smaller of the two values computed using Eqs. (18.142) and (18.143).

In the subcircuit implementation, the length of the second subinterval can therefore be computed as the smaller of the values given by Eqs. (18.142) and (18.143):

$$d_2 = \min\left(1 - d, \frac{i_{pk}}{m_2 T_s}\right) \quad (18.144)$$

By use of  $d_2$  from Eq. (18.144), Eq. (18.141) can be extended to allow for CCM or DCM operation of a current-programmed converter as follows:

$$d = \frac{2(\langle v_c(t) \rangle_{T_s} (d + d_2) - R_f \langle i_L(t) \rangle_{T_s})}{\frac{R_f}{L_{f_s}} (\langle v_1(t) \rangle_{T_s} + \langle v_2(t) \rangle_{T_s}) d_2 (d + d_2) + 2V_a (d + d_2)} \quad (18.145)$$

This relationship is valid for both CCM and DCM provided that the second subinterval length  $d_2$  is computed according to Eq. (18.144). Expression (18.145) is used in the implementation of the combined CCM/DCM subcircuit CPM.

### 18.5.3 Simulation Example: Frequency Responses of a Buck Converter with Current-Programmed Control

To illustrate an application of the CPM subcircuit, let us consider the example buck converter circuit model of Fig. 18.32. To construct this averaged circuit model in SPICE, the switches are replaced by the CCM-DCM1 averaged switch subcircuit. The control input to the CPM subcircuit is the independent voltage source  $v_c$ . Three dependent voltage sources are used to generate other inputs to the CPM subcircuit. The controlled voltage source  $E_i$  is proportional to the inductor current  $i_L$ . The controlled voltage source  $E_1$  is equal to  $v(1) - v(3)$ , which is equal to the voltage  $\langle v_1(t) \rangle_{T_s}$  applied across the inductor during the first subinterval when the transistor is on and the diode is off. The controlled voltage source  $E_2$  is equal to  $v(3)$ , which is equal to the voltage  $\langle v_2(t) \rangle_{T_s}$  applied across the inductor during the second subinterval when the transistor is off and the diode is on.

SPICE ac simulations are performed at the quiescent operating point obtained for the dc value of the control input equal to  $V_c = 1.4$  V. At the quiescent operating point, the switch duty cycle is  $D = 0.676$ , the dc output voltage is  $V = 8.1$  V, and the dc component of the inductor current is  $I_L = 0.81$  A. The converter operates in CCM.

Magnitude and phase responses of the control-to-output transfer functions  $G_{vc}(s) = \hat{v}/\hat{v}_c$  and  $G_{vd}(s) = \hat{v}/\hat{d}$  are shown in Fig. 18.33. The duty-cycle to output voltage transfer function  $G_{vd}(s)$  exhibits the familiar second-order high-Q response. Peaking in the magnitude response and a steep change in phase from  $0^\circ$  to  $-180^\circ$  occur around the center frequency of

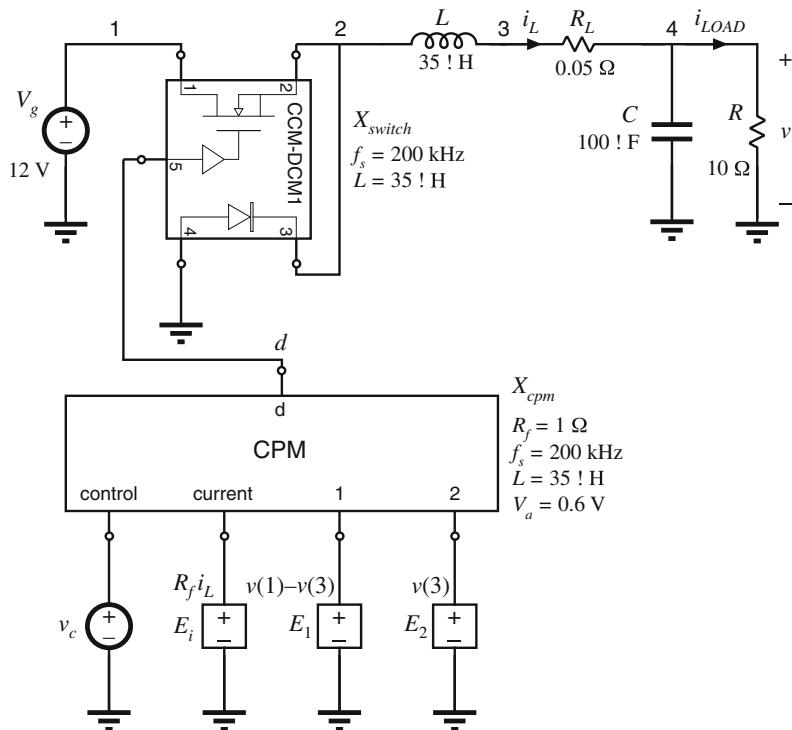


Fig. 18.32 CPM buck converter example: averaged circuit model

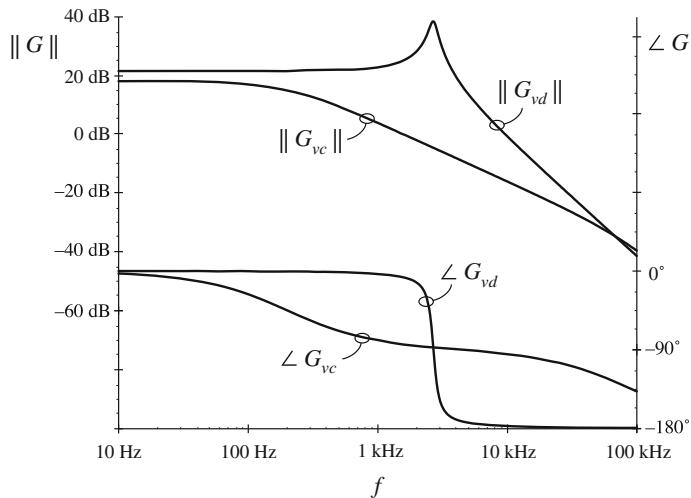
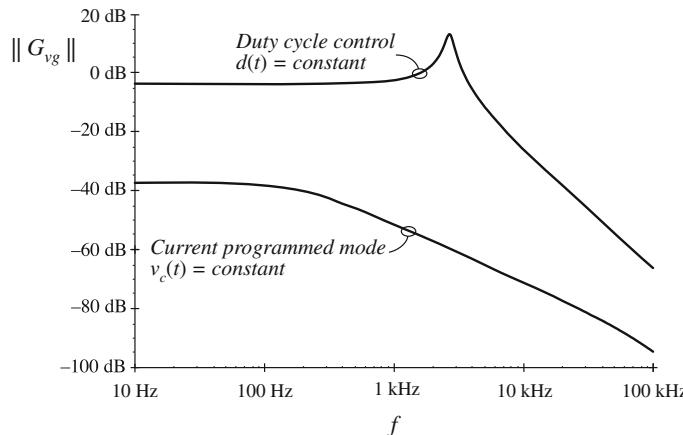


Fig. 18.33 Comparison of CPM control with duty-cycle control, for the control-to-output frequency response of the buck converter example



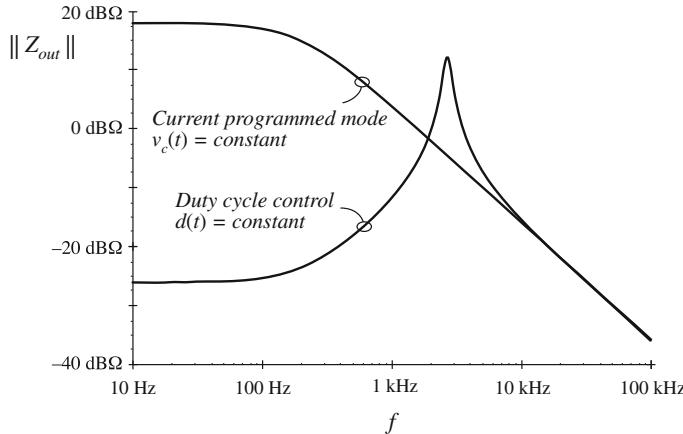
**Fig. 18.34** Comparison of CPM control with duty-cycle control, for the line-to-output frequency response of the buck converter example

the pair of complex-conjugate poles. In contrast, the CPM control-to-output response has a dominant low-frequency pole. The phase lag is around  $-90^\circ$  in a wide range of frequencies. A high-frequency pole contributes to additional phase lag at higher frequencies. The frequency responses of Fig. 18.33 illustrate an advantage of CPM control over duty-cycle control. Because of the control-to-output frequency response dominated by the single low-frequency pole, it can be much easier to close a wide-bandwidth outer voltage feedback loop around the CPM controlled power converter than around a converter where the duty cycle is the control input. Proportional-plus-integral (*PI*) controllers are commonly used in current-programmed regulators.

Another advantage of CPM control is in rejection of input voltage disturbances. Line-to-output frequency responses for duty-cycle control and CPM control in the buck example are compared in Fig. 18.34. The line-to-output transfer function  $G_{vg}(s)$  for duty-cycle control is characterized by a dc asymptote approximately equal to the duty cycle  $D = 0.676$ . Resonant poles occur at the corner frequency of the  $L-C$  filter. The line-to-output transfer function  $G_{vg-cpm}(s)$  with current-programmed control is significantly reduced, and exhibits more than 30 dB of additional attenuation over the frequencies of interest. It should again be noted that the transfer function  $G_{vg-cpm}(s)$  in Fig. 18.34 cannot be predicted by the simple models of Sect. 18.1; the more accurate model of Sect. 18.3 must be employed.

It is also interesting to compare the output impedance of the converter with duty-cycle control versus CPM control. The results are shown in Fig. 18.35. The output impedance plotted in the figure includes the load resistance of  $10 \Omega$ . For duty-cycle control, the dc asymptote of the output impedance is dominated by the inductor winding resistance of  $0.05 \Omega$ . The inductor becomes significant in the vicinity of 200 Hz. At the resonant frequency of the output  $LC$  filter, significant peaking in the output impedance of the duty-cycle controlled converter can be observed. At higher frequencies, the output impedance is dominated by the impedance of the filter capacitor, which decreases with frequency.

In the current-programmed converter, the low-frequency impedance is high. It is equal to the parallel combination of the load resistance and the CPM output resistance. Because of the lossless damping introduced by CPM control, the series inductor does not affect the output



**Fig. 18.35** Comparison of CPM control with duty-cycle control, for the output impedance of the buck converter example

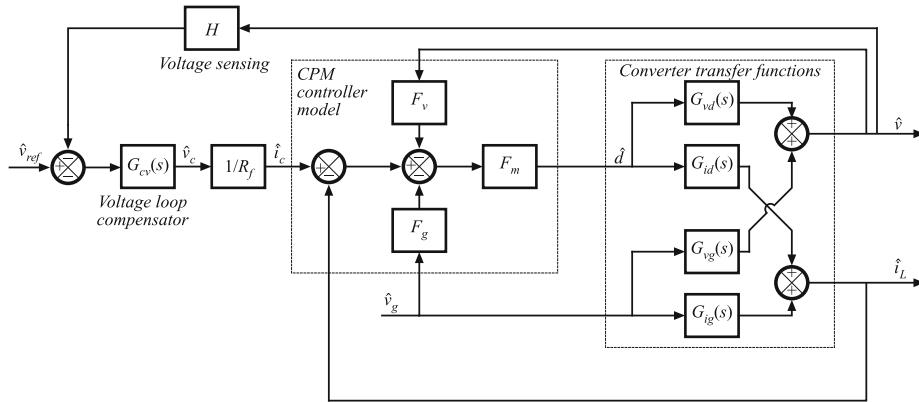
impedance. The simple model of Sect. 18.1 predicts that the inductor branch of the circuit is driven by a current source; this effectively removes the influence of the inductor on the output impedance. The plot of Fig. 18.35 was generated using the more accurate; nonetheless, the output impedance is accurately predicted by the simple model. It can be seen that current programming substantially increases the converter output impedance at low frequencies. At high frequencies the output impedances of the duty-cycle and CPM controlled converters have the same asymptotes.

## 18.6 Voltage Feedback Loop Around a Current-Programmed Converter

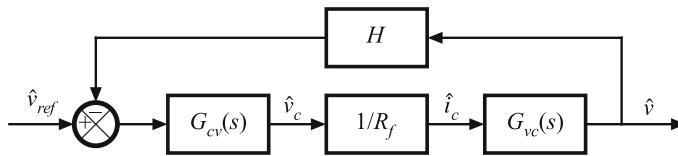
As shown in Figs. 18.1 and 18.3 a converter system incorporating current-programmed control often includes an outer voltage feedback loop, the purpose of which is to regulate the converter output voltage. As discussed in Chap. 9, voltage is sensed and compared to a reference. The error signal is processed by a voltage loop compensator, which outputs a control signal. In duty-cycle controlled converters of Chap. 9, the control signal is the input to a pulse-width modulator, which produces a switch control signal with duty ratio proportional to the PWM control input. In CPM controlled converters, the control signal generated by the voltage loop compensator is the control input  $v_c = R_f i_c$  for the CPM controller.

### 18.6.1 System Model

A complete system model, including the outer voltage loop, is shown in Fig. 18.36. The model is very similar to the system model in Fig. 9.2 except that the pulse-width modulator model is replaced by the CPM controller model. For the purpose of designing the voltage loop compensator  $G_{cv}(s)$ , it is convenient to make use of the closed-loop transfer function  $G_{vc}(s) = \hat{v}/\hat{i}_c$  of the CPM controlled converter. A block diagram of the voltage feedback loop is shown in Fig. 18.37.



**Fig. 18.36** Block diagram that models a CPM controlled converter with an outer voltage feedback loop



**Fig. 18.37** Model of the outer voltage feedback loop

The design of  $G_{cv}(s)$  amounts to employing the techniques of Chap. 9 to shape the voltage loop gain

$$T_v = HG_{cv}(s) \frac{1}{R_f} G_{vc}(s) \quad (18.146)$$

so that target crossover frequency  $f_{cv}$  stability margins are attained.

With the voltage feedback loop closed around a current-programmed converter, the closed-loop input impedance  $Z_i$  can be found using the results of Sect. 18.4.4 by application of the Feedback Theorem. As discussed in Sect. 17.5.2, the closed-loop input admittance  $Y_i = 1/Z_i$  can be found from:

$$Y_i = \frac{1}{Z_i} = \frac{1}{Z_{N-cpm}} \frac{T_v}{1 + T_v} + \frac{1}{Z_{D-cpm}} \frac{1}{1 + T_v} \quad (18.147)$$

where expressions for  $Z_{N-cpm}$  and  $Z_{D-cpm}$  are given in Sect. 18.4.4. Following the discussion in Sect. 17.5.2, the result for the closed-loop input impedance can be used to evaluate the system stability when the CPM converter with voltage feedback loop includes an input filter or, more generally, when it is supplied from a source with a nonzero output impedance.

### 18.6.2 Design Example

To illustrate an outer voltage feedback loop design, consider the CPM controlled buck converter shown in Fig. 18.32, with the voltage loop added as shown in Fig. 18.1. The system small-signal model is shown in Fig. 18.36. In this example, the reference voltage is  $V_{ref} = 3$  V, and the

voltage sensing gain is set to  $H = 0.375$ , so that the output dc voltage is ideally regulated at  $V = V_{ref}/H = 8$  V. The quiescent operating point and the small-signal model parameters are approximately the same as in the CPM buck converter considered in Sect. 18.5.3:  $D = 0.67$ ,  $I_L = V/R = 0.8$  A,  $M_a/M_2 = 0.525$ ,  $F_m = 3.2$  A $^{-1}$ ,  $F_g = 0.016$   $\Omega^{-1}$ ,  $F_v = 0$ . Table 18.3 includes an expression for the closed-loop control-to-output voltage transfer function  $G_{vc}(s)$  predicted by the more accurate CPM model,

$$G_{vc}(s) = G_{c0} \frac{1}{1 + \frac{s}{Q_c \omega_c} + \left(\frac{s}{\omega_c}\right)^2} \approx G_{c0} \frac{1}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{hf}}\right)} \quad (18.148)$$

$$G_{c0} = \frac{V}{D} \frac{F_m}{\left(1 + \frac{F_m V}{DR}\right)} = 7.92 \text{ } \Omega \rightarrow 18 \text{ dB}\Omega$$

$$f_c = \frac{1}{2\pi\sqrt{LC}} \sqrt{1 + \frac{F_m V}{DR}} = 5.9 \text{ kHz}$$

$$Q_c = R \sqrt{\frac{C}{L}} \frac{\sqrt{1 + \frac{F_m V}{DR}}}{\left(1 + \frac{RCF_m V}{DL}\right)} = 0.034$$

$$f_{p1} = Q_c f_c = 201 \text{ Hz}$$

$$f_{hf} = f_c/Q_c = 174 \text{ kHz}$$

As shown in Fig. 18.33,  $G_{vc}(s)$  exhibits a single-pole response over a wide range of frequencies, so that it is relatively easy to design a wide-bandwidth voltage feedback loop with high crossover frequency  $f_{cv}$  using a simple proportional-integral (PI) compensator,

$$G_{cv}(s) = G_{cm} \left(1 + \frac{\omega_{zv}}{s}\right) \quad (18.149)$$

A sketch of the magnitude response of the voltage loop gain  $T_v$  of Eq. (18.146), with a PI compensator of Eq. (18.149), is shown in Fig. 18.38. Assuming  $f_{zv} < f_{cv} < f_{hf}$ , the magnitude asymptote has  $-20$  dB/dec slope around the crossover frequency,

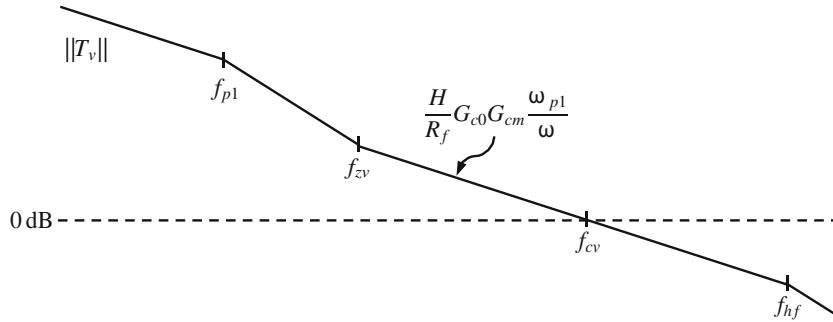
$$\|T_v\| \rightarrow \frac{H}{R_f} G_{co} G_{cm} \frac{\omega_{p1}}{\omega} \quad (18.150)$$

From Eq. (18.150) it follows that the gain  $G_{cm}$  can be selected to obtain the desired crossover frequency  $f_{cv}$ ,

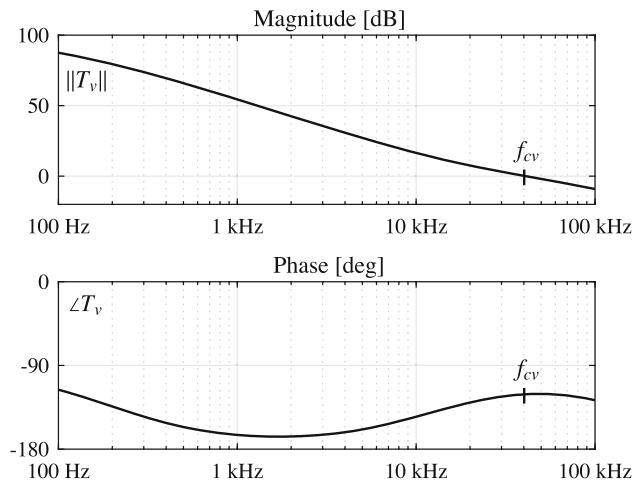
$$G_{cm} = \frac{R_f}{H G_{co}} \frac{f_{cv}}{f_{p1}} \quad (18.151)$$

To achieve wide-bandwidth voltage regulation let us choose  $f_{cv} = 40$  kHz =  $f_s/5$ . Equation (18.151) yields  $G_{cm} = 67.1$ . The phase margin  $\varphi_v$  can be evaluated based on the phase contributions of the poles and zeroes shown in Fig. 18.38. Taking into account that  $f_{p1} \ll f_{cv}$ , we have

$$\varphi_v = 180^\circ + \angle T_v(j\omega) = 180^\circ - 90^\circ - 90^\circ + \tan^{-1} \frac{f_{cv}}{f_{zv}} - \tan^{-1} \frac{f_{cv}}{f_{hf}} \quad (18.152)$$



**Fig. 18.38** Sketch of the magnitude response of the loop gain  $T_v$  using a PI compensator  $G_{cv}(s)$



**Fig. 18.39** Loop gain  $T_v$  in the design example of Sect. 18.6.2

For these values,  $\tan^{-1}(f_{cv}/f_{hf}) = 13^\circ$ . Equation (18.152) can be used to select  $f_{zv}$  to achieve a desired phase margin. For example, the choice  $f_{zv} = f_{cv}/3$  yields

$$\varphi_v = \tan^{-1} \frac{f_{cv}}{f_{zv}} - \tan^{-1} \frac{f_{cv}}{f_{hf}} = 72^\circ - 13^\circ = 59^\circ \quad (18.153)$$

Inclusion of this PI compensator  $G_{cv}(s)$  results in the voltage loop gain  $T_v$  shown in Fig. 18.39.

## 18.7 High-Frequency Dynamics of Current-Programmed Converters

The simple model of Sect. 18.2 predicts that the inductor current  $i_L$  is directly controlled by the current command  $i_c$ , which implies small-signal control-to-current transfer function equal to unity at all frequencies,

$$G_{ic}(s) = \frac{\hat{i}_L}{\hat{i}_c} \approx 1 \quad (18.154)$$

Let us compare this simple result with high-frequency predictions of the more accurate averaged small-signal model of Sect. 18.3. At high frequencies, small-signal perturbations of capacitor voltages become negligibly small. As a result,  $\hat{m}_1 \approx 0$ ,  $\hat{m}_2 \approx 0$ , and inductor current slopes  $m_1$  and  $m_2$  can be considered constant, equal to the unperturbed dc values  $M_1$  and  $M_2$ , respectively. At high frequencies, the small-signal duty-cycle perturbation in Eq. (18.73) becomes

$$\hat{d}(t) \approx F_m [\hat{i}_c(t) - \hat{i}_L(t)] \quad (18.155)$$

In a two-switch, single-inductor PWM converter, neglecting voltage perturbations, the duty-cycle to inductor current transfer function can be written as

$$G_{id} = \frac{\hat{i}_L}{\hat{d}} \approx \frac{M_1 + M_2}{s} \quad (18.156)$$

Combining Eqs. (18.156) and (18.155), the more accurate model of Sect. 18.3 yields the following prediction for the control-to-current transfer function at high frequencies

$$G_{ic}(s) = \frac{\hat{i}_L}{\hat{i}_c} \approx \frac{1}{1 + \frac{s}{\omega_{hf}}} \quad (18.157)$$

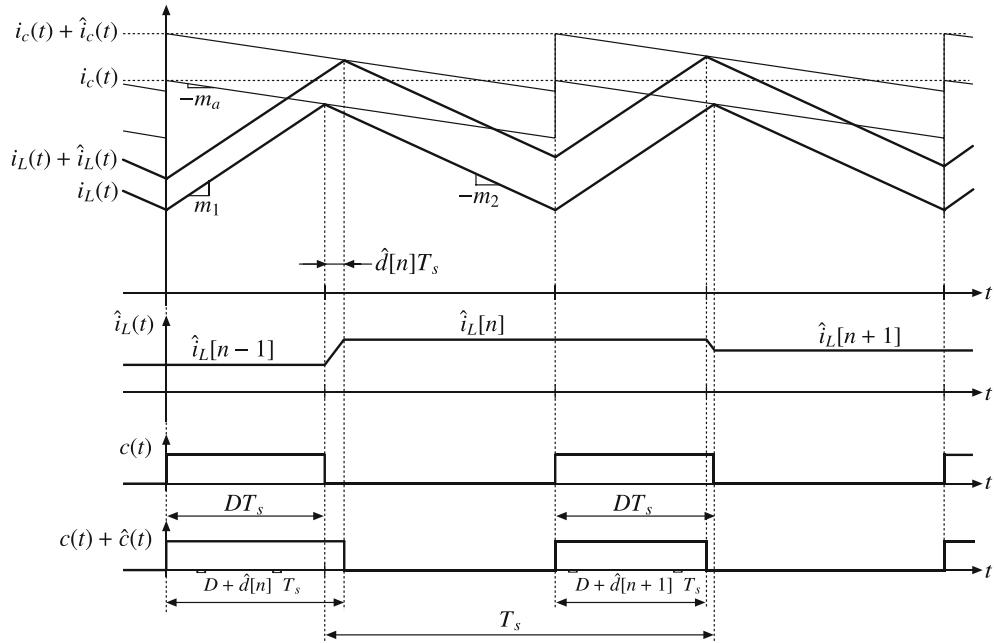
where

$$f_{hf} = \frac{1}{2\pi} F_m (M_1 + M_2) = \frac{M_1 + M_2}{2M_a + M_1 - M_2} \frac{f_s}{\pi} \quad (18.158)$$

Note that exactly the same result for the high-frequency pole was found in Eq. (18.114). Neither the simple model, which neglects inductor dynamics, nor the more accurate model, which implies a single-pole response at high frequencies, predicts instability or the need for the artificial ramp discussed in Sect. 18.2. This is because the averaged small-signal models do not take into account converter switching and modulator sampling processes, which lead to various discrete-time phenomena in a current-programmed converter. The purpose of this section is to examine high-frequency dynamics of CPM controlled converters using sampled-data modeling techniques, and to compare predictions of the sampled-data model to the predictions of the averaged small-signal models.

### 18.7.1 Sampled-Data Model

Figure 18.40 shows waveforms in a current-programmed converter in response to a perturbation  $\hat{i}_c$  in the control current  $i_c$ , with an initial perturbation in the inductor current  $i_L(t)$  denoted as  $\hat{i}_L[n-1]$ . At  $t = DT_s$ , in response to the  $\hat{i}_c$  and  $\hat{i}_L[n-1]$  perturbations, the duty cycle  $D$  is perturbed by  $\hat{d}[n]$  and the inductor current perturbation assumes a new value  $\hat{i}_L[n]$  over the next switching period  $T_s$ . Derivation of a sampled-data “transfer function”  $G_{ic} = \hat{i}_L/\hat{i}_c$  follows the approach described in [77], which includes taking into account sampling  $\hat{i}_c(t)$  to obtain discrete-time samples  $\hat{i}_c[n]$ , derivation of a discrete-time relationship between  $\hat{i}_c[n]$  and  $\hat{i}_L[n]$ , and finding an *equivalent hold* transfer function that models the process in which continuous-time inductor current perturbation  $\hat{i}_L(t)$  is obtained from the samples  $\hat{i}_L[n]$ .



**Fig. 18.40** Steady-state and perturbed waveforms in a current-programmed converter

First, we note that the Laplace transform of the samples of  $\hat{i}_c(t)$  equals

$$\frac{1}{T_s} \sum_{k \rightarrow -\infty}^{k \rightarrow +\infty} \hat{i}_c(s - jk\omega_s) \quad (18.159)$$

where  $\hat{i}_c(s)$  is the Laplace transform of the continuous-time control current  $\hat{i}_c(t)$ .

Next, we proceed to derive a discrete-time relationship between  $\hat{i}_c[n]$  and  $\hat{i}_L[n]$ . Waveform details around the sampling instant  $t = DT_s$  are shown in Fig. 18.41. From the geometry of the waveforms, the next perturbation in the inductor current  $\hat{i}_L[n]$  can be found in terms of the previous perturbation  $\hat{i}_L[n - 1]$ , the duty-cycle perturbation  $\hat{d}[n]$  and the inductor current slopes  $m_1$  and  $m_2$ ,

$$\hat{i}_L[n] = \hat{i}_L[n - 1] + (m_1 + m_2)\hat{d}[n]T_s \quad (18.160)$$

Similarly,  $\hat{i}_c[n]$  can be related to  $\hat{i}_L[n - 1]$ ,  $\hat{d}[n]$ ,  $m_1$  and  $m_a$ ,

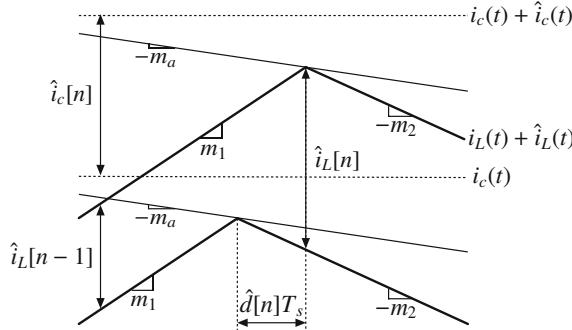
$$\hat{i}_c[n] = \hat{i}_L[n - 1] + (m_1 + m_a)\hat{d}[n]T_s \quad (18.161)$$

Eliminating  $\hat{d}[n]$  from Eqs. (18.160) and (18.161) yields a discrete-time relationship between  $\hat{i}_c[n]$  and  $\hat{i}_L[n]$ ,

$$\hat{i}_L[n] = \alpha \hat{i}_L[n - 1] + (1 - \alpha) \hat{i}_c[n] \quad (18.162)$$

where the coefficient  $\alpha$  depends on the inductor current and artificial ramp slopes,

$$\alpha = -\frac{m_2 - m_a}{m_1 + m_a} \quad (18.163)$$



**Fig. 18.41** Details of the steady-state and perturbed inductor current waveforms around the sampling instant  $t = DT_s$

which is the same as Eq. (18.54) used in the stability analysis of Sect. 18.2.

Application of the  $\mathcal{Z}$  transform [176] to Eq. (18.162) results in

$$\hat{i}_L(z) = \alpha \hat{i}_L(z) z^{-1} + (1 - \alpha) \hat{i}_c(z) \quad (18.164)$$

which yields the discrete-time  $\mathcal{Z}$ -domain transfer function

$$G_{ic}(z) = \frac{\hat{i}_L(z)}{\hat{i}_c(z)} = \frac{1 - \alpha}{1 - \alpha z^{-1}} \quad (18.165)$$

A discrete-time system is stable if all poles lie inside the unit circle in the complex  $z$  plane. Given that the transfer function  $G_{ic}(z)$  has a pole at  $z = \alpha$ , the stability condition becomes

$$|\alpha| < 1 \quad (18.166)$$

which is the same as the stability condition given by Eq. (18.55).

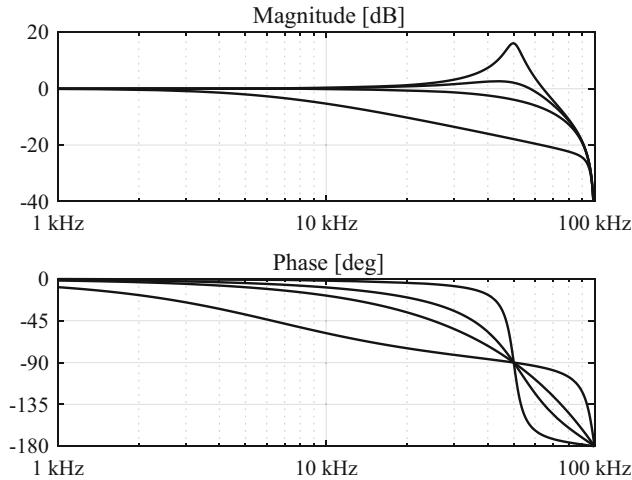
As shown in Fig. 18.40, in response to a discrete-time perturbation  $\hat{i}_L[n]$ , the continuous-time inductor current perturbation  $\hat{i}_L(t)$  is a pulse of amplitude  $\hat{i}_L[n]$  and length  $T_s$ . The transfer function of the corresponding equivalent hold is therefore equal to the transfer function of the zero-order hold [176],

$$\frac{1 - e^{-sT_s}}{s} \quad (18.167)$$

We now can combine Eqs. (18.165) and (18.167) to derive an expression for the sampled-data “transfer function”

$$G_{ic}(s) = \frac{\hat{i}_L}{\hat{i}_c} = \frac{1 - \alpha}{1 - \alpha e^{-sT_s}} \frac{1 - e^{-sT_s}}{sT_s} \quad (18.168)$$

The first part of the expression is obtained from Eq. (18.165) by replacing  $z^{-1}$  with  $e^{-sT_s}$ , which follows from the fact that a factor  $z^{-1}$  corresponds to delaying a signal by  $T_s$ , while the Laplace transform of a signal delayed by  $T_s$  equals  $e^{-sT_s}$  times the Laplace transform of the signal. The second part of the expression is the transfer function of the equivalent hold in Eq. (18.167), while  $T_s$  in the denominator is due to sampling and retaining only the low-frequency ( $k = 0$ ) portion of the spectrum of the sampled control input  $\hat{i}_c(t)$  in Eq. (18.159).



**Fig. 18.42** High-frequency magnitude and phase responses of  $G_{ic}$  based on the sampled-data model for four values of the artificial ramp slope,  $M_a/M_2 = 0.1, 0.5, 1$  and  $5$

To illustrate magnitude and phase responses of the sampled-data  $G_{ic}(s)$  in Eq. (18.168), consider a buck converter example operating at  $f_s = 100$  kHz and  $D = 0.5$ . The input dc voltage is  $V_g = 10$  V, the output voltage is  $V = DV_g = 5$  V, and inductance is  $L = 5$   $\mu$ H. Values of the output filter capacitance and load do not affect high-frequency control-to-inductor current responses. The inductor current slopes are  $M_1 = (V_g - V)/L = 1$  A/ $\mu$ s, and  $M_2 = V/L = 1$  A/ $\mu$ s. Since  $D = 0.5$ , the CPM controlled converter is stable for any  $M_a > 0$ . Magnitude and phase responses of the sampled-data  $G_{ic}(s)$  are evaluated by replacing  $s \rightarrow j\omega$  in Eq. (18.168), and the results are shown in Fig. 18.42 for four different values of the artificial ramp slope,  $M_a/M_2 = 0.1, 0.5, 1$ , and  $5$ . In all cases, the magnitude responses start from 0 dB and phase responses start from  $0^\circ$ , matching the responses expected based on the simple averaged small-signal model. For  $M_a/M_2 = 0.1$ ,  $\alpha = -0.82$ , and the sampled-data frequency response exhibits peaking in the magnitude response and a sharp decline in the phase response from  $0^\circ$  to  $-180^\circ$  around  $f_s/2 = 50$  kHz. For  $M_a = 0$ , which corresponds to the period-doubling stability boundary, one may verify that the magnitude response goes to  $\infty$  at  $f_s/2$ . The peaking in the magnitude response diminishes with increasing values of the artificial ramp slope. For very large  $M_a/M_2$ , such as  $M_a/M_2 = 5$  in Fig. 18.42, the magnitude response starts to roll off at a lower frequency, implying an effectively reduced current control bandwidth.

### 18.7.2 First-Order Approximation

It can be verified that the predictions of the sampled-data model of Eq. (18.168) match experimentally measured frequency responses very well. However, the “transfer function” of Eq. (18.168) is not a standard rational transfer function in  $s$ , and it does not offer an intuitive design-oriented interpretation. It is therefore of interest to consider a rational transfer function approximation of  $G_{ic}(s)$  in Eq. (18.168). Consider the first-order Padé approximation [138] of the term  $e^{-sT_s}$ ,

$$e^{-sT_s} \approx \frac{1 - \frac{s}{\omega_s/\pi}}{1 + \frac{s}{\omega_s/\pi}} \quad (18.169)$$

Note that the approximation includes a RHP zero and a pole at the same frequency  $f_s/\pi$ . The magnitude response of the approximation is equal to 1 (0 dB) at all frequencies, exactly matching the magnitude response of  $e^{-j\omega T_s}$  at all frequencies. Substituting Eq. (18.169) into Eq. (18.168) yields a first-order rational transfer function approximation

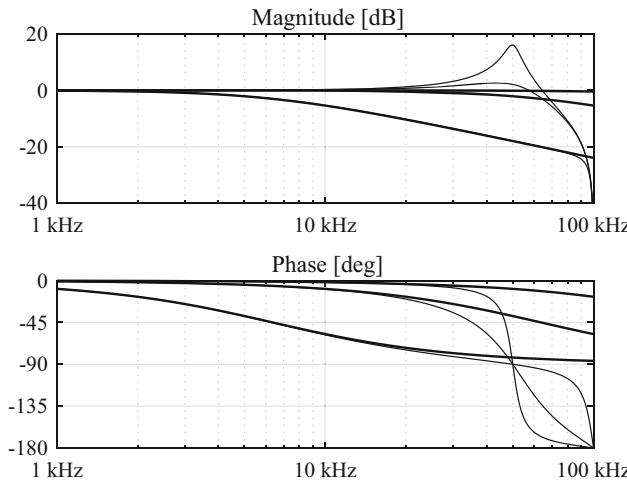
$$G_{ic}(s) \approx \frac{1}{1 + \frac{s}{\omega_{hf}}} \quad (18.170)$$

where

$$f_{hf} = \frac{1 - \alpha f_s}{1 + \alpha \pi} = \frac{M_1 + M_2}{2M_a + M_1 - M_2} \frac{f_s}{\pi} \quad (18.171)$$

which is *identical* to the frequency response  $G_{ic}(s)$  predicted by the more accurate averaged small-signal model given by Eq. (18.157). It follows that the more accurate averaged small-signal model of Sect. 18.3 is equivalent to the first-order approximation of the sampled-data model.

Figure 18.43 compares the magnitude and phase responses of the sampled-data model in Eq. (18.168) to the magnitude and phase responses of the first-order approximation in Eq. (18.170) or, equivalently, Eq. (18.157), for the same buck converter example considered in Fig. 18.42, and for three values of the artificial ramp slope,  $M_a/M_2 = 0.1, 0.5$ , and  $5$ . For  $M_a/M_2 = 0.1$ , the first-order approximation predicts a pole at  $3.2f_s$ , which is a very poor approximation to the sampled-data model predictions. The high-frequency predictions of the first-order



**Fig. 18.43** Comparison of high-frequency  $G_{ic}$  responses based on the sampled-data model and its first-order approximation for three different values of the artificial ramp slope,  $M_a/M_2 = 0.1, 0.5$ , and  $5$ . The first-order approximation responses are identical to the predictions of the more accurate CPM model

approximation improve with increasing slope of the artificial ramp. For  $M_a = 0.5M_2$ , which is a practical choice that guarantees stability for any duty cycle  $D$ , the example of Fig. 18.43 illustrates a very good match up to around  $f_s/5$ . For large  $M_a/M_2$ , such as  $M_a/M_2 = 5$ , the magnitude and phase responses of the first-order approximation or, equivalently, the more accurate averaged small-signal model, are in very good agreement with the sampled-data model at essentially all frequencies of interest.

### 18.7.3 Second-Order Approximation

As discussed in the previous subsection, the first-order approximation does not predict CPM instability and it does not offer accurate predictions of high-frequency responses in cases when a current-programmed converter operates close to the stability boundary. In this section, we show how a second-order rational transfer function approximation offers a way to accurately incorporate sampled-data effects. The second-order Padé approximation [138] of the term  $e^{-sT_s}$  is given by

$$e^{-sT_s} \approx \frac{1 - \frac{\pi}{2} \frac{s}{\omega_s/2} + \left(\frac{s}{\omega_s/2}\right)^2}{1 + \frac{\pi}{2} \frac{s}{\omega_s/2} + \left(\frac{s}{\omega_s/2}\right)^2} \quad (18.172)$$

The second-order approximation includes a pair of RHP zeroes and a pair of poles having the same  $Q$  factor and the same center frequency  $f_s/2$ . As in the case of the first-order approximation, the magnitude response of the approximation is 1 (0 dB) at all frequencies. Substituting Eq. (18.172) into Eq. (18.168), yields a second-order rational transfer function approximation

$$G_{ic}(s) \approx \frac{1}{1 + \frac{\pi}{2} \frac{1+\alpha}{1-\alpha} \frac{s}{\omega_s/2} + \left(\frac{s}{\omega_s/2}\right)^2} \quad (18.173)$$

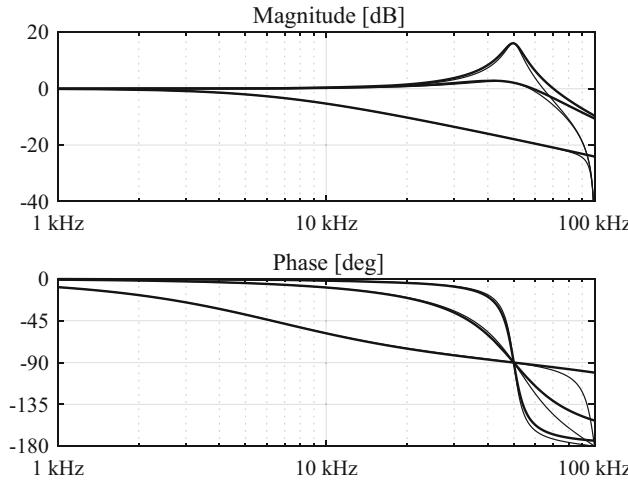
or

$$G_{ic}(s) \approx \frac{1}{1 + \frac{1}{Q_{hf}} \frac{s}{\omega_s/2} + \left(\frac{s}{\omega_s/2}\right)^2} \quad (18.174)$$

where the  $Q$ -factor of the pair of poles in  $G_{ic}(s)$  is

$$Q_{hf} = \frac{2}{\pi} \frac{1-\alpha}{1+\alpha} = \frac{2}{\pi} \frac{M_1 + M_2}{2M_a + M_1 - M_2} = \frac{2}{\pi} \frac{1}{1 - 2D + 2D \frac{M_a}{M_2}} \quad (18.175)$$

and the center frequency is at  $f_s/2$ . At the stability boundary,  $\alpha = -1$  and  $Q_{hf} \rightarrow \infty$ , which means that the second-order approximation given by Eq. (18.173) is capable of correctly predicting CPM instability. For the same buck converter example considered in Figs. 18.42 and 18.43, Fig. 18.44 shows a comparison of the magnitude and phase responses of the second-order approximation given by Eq. (18.173) and the sampled-data model given by Eq. (18.168) for three values of the artificial ramp slope,  $M_a/M_2 = 0.1, 0.5$ , and  $5$ . The second-order approximation matches predictions of the sampled-data model very well at all frequencies of interest, and for all values of the artificial ramp slope.



**Fig. 18.44** Comparison of high-frequency  $G_{ic}$  responses based on the sampled-data model and its second-order approximation for three different values of the artificial ramp slope,  $M_a/M_2 = 0.1, 0.5$ , and 5

The more accurate averaged small-signal model of Sect. 18.3, which is equivalent to the first-order approximation of the sampled-data model, can be extended to match predictions of the second-order approximation. As shown in [107], one approach to extending the more accurate model consists of replacing the modulator gain  $F_m$  in Fig. 18.24 with a single-pole response

$$\frac{F_m}{1 + \frac{s}{\omega_x}} \quad (18.176)$$

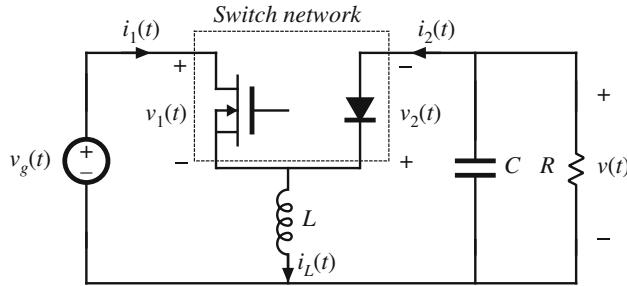
where  $F_m$  given by Eq. (18.74) remains the same as before, while the additional modulator pole frequency equals

$$f_x = \frac{\pi}{4} \left( 1 - 2D + 2D \frac{M_a}{M_2} \right) f_s \quad (18.177)$$

It can be shown that inclusion of the pole at  $f_x$  results in high-frequency responses consistent with the second-order approximation of the sampled-data model. With this extension, the more accurate averaged small-signal model is capable of predicting CPM instability and of providing accurate predictions of CPM frequency responses at all frequencies of interest, and for all values of the artificial ramp slope  $M_a$ . In practice, assuming an artificial ramp with a sufficiently large slope  $M_a$  is applied, the analytical and simulation models developed in Sects. 18.3 and 18.5 can be considered sufficiently accurate.

## 18.8 Discontinuous Conduction Mode

A model of current-programmed converters operating in the discontinuous conduction mode is incorporated in the averaged simulation model described in Sect. 18.5.2. In this section, an analytical model for current-programmed DCM converters is derived using the averaged switch



**Fig. 18.45** Current-programmed DCM buck-boost converter example

modeling approach of Sect. 15.2. It is found that the average transistor voltage and current follow a power sink characteristic, while the average diode voltage and current obey a power source characteristic. Perturbation and linearization of these characteristics leads to a small-signal equivalent circuit that models CPM DCM converters. The basic DCM CPM buck, boost, and buck-boost converters essentially exhibit single-pole transfer functions: the second pole and the right half-plane zero appear at frequencies near to or greater than the switching frequency, owing to the small value of  $L$  in DCM.

A DCM CPM buck-boost converter example is analyzed here. However, Eqs. (18.178) to (18.195) are written in general form, and apply equally well to DCM CPM buck and boost converters. The schematic of a buck-boost converter is illustrated in Fig. 18.45. The terminal waveforms of the switch network are defined as shown:  $v_1(t)$  and  $i_1(t)$  are the transistor waveforms, while  $v_2(t)$  and  $i_2(t)$  are the diode waveforms. Figure 18.46 illustrates typical DCM waveforms, for current-programmed control with an artificial ramp having slope  $-m_a$ . The inductor current is zero at the beginning of each switching period. By solution of the transistor conduction subinterval, the programmed current  $i_{pk}$  can be related to the transistor duty cycle  $d_1$  by

$$\begin{aligned} i_c &= i_{pk} + m_a d_1 T_s \\ &= (m_1 + m_a) d_1 T_s \end{aligned} \quad (18.178)$$

Solution for  $d_1$  leads to

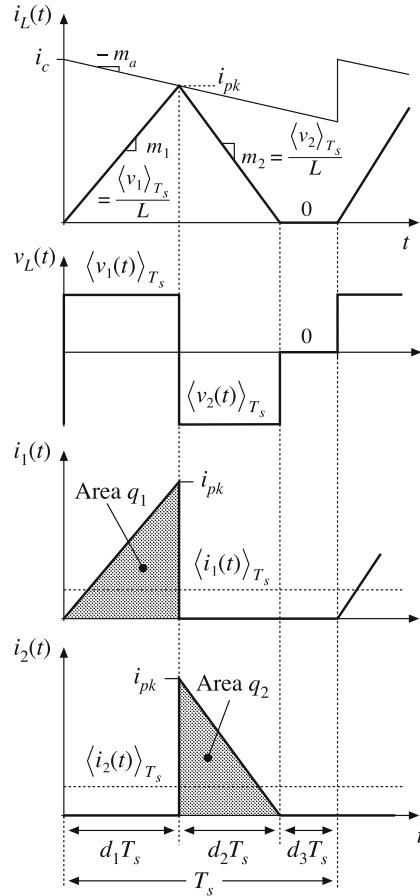
$$d_1(t) = \frac{i_c(t)}{(m_1 + m_a) T_s} \quad (18.179)$$

The average transistor current is found by integrating the  $i_1(t)$  waveform of Fig. 18.46 over one switching period:

$$\langle i_1(t) \rangle_{T_s} = \frac{1}{T_s} \int_0^{T_s} i_1(\tau) d\tau = \frac{q_1}{T_s} \quad (18.180)$$

The total area  $q_1$  is equal to one-half of the peak current  $i_{pk}$ , multiplied by the subinterval length  $d_1 T_s$ . Hence,

$$\langle i_1(t) \rangle_{T_s} = \frac{1}{2} i_{pk} d_1 T_s \quad (18.181)$$



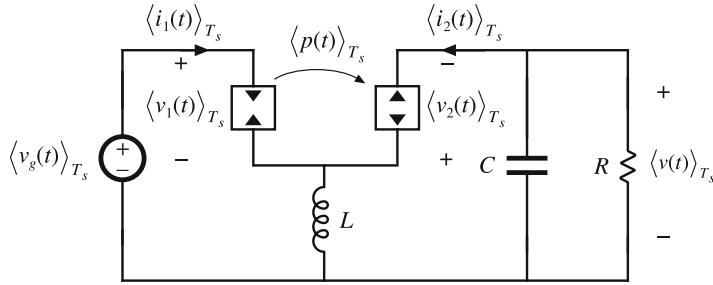
**Fig. 18.46** Waveforms, CPM DCM buck–boost example

Elimination of  $i_{pk}$  and  $d_1$ , to express the average transistor current as a function of  $i_c$ , leads to

$$\langle i_1(t) \rangle_{T_s} = \frac{\frac{1}{2} L i_c^2 f_s}{\langle v_1(t) \rangle_{T_s} \left(1 + \frac{m_a}{m_1}\right)^2} \quad (18.182)$$

Finally, Eq. (18.182) can be rearranged to obtain the averaged switch network input port relationship:

$$\langle i_1(t) \rangle_{T_s} \langle v_1(t) \rangle_{T_s} = \frac{\frac{1}{2} L i_c^2 f_s}{\left(1 + \frac{m_a}{m_1}\right)^2} = \langle p(t) \rangle_{T_s} \quad (18.183)$$



**Fig. 18.47** CPM DCM buck-boost converter model, derived via averaged switch modeling

Thus, the average transistor waveforms obey a power sink characteristic. When  $m_a = 0$ , then the average power  $\langle p(t) \rangle_{T_s}$  is a function only of  $L$ ,  $i_c$ , and  $f_s$ . The presence of the artificial ramp causes  $\langle p(t) \rangle_{T_s}$  to additionally depend on the converter voltages, via  $m_1$ .

The power sink characteristic can also be explained via inductor energy arguments. During the first subinterval, the inductor current increases from 0 to  $i_{pk}$ . In the process, the inductor stores the following energy:

$$W = \frac{1}{2} L i_{pk}^2 \quad (18.184)$$

The energy  $W$  is transferred from the power input  $v_g$ , through the switch network input port, to the inductor, once per switching period. This energy transfer process accounts for the power flow

$$\langle p(t) \rangle_{T_s} = W f_s = \frac{1}{2} L i_{pk}^2 f_s \quad (18.185)$$

The switch network input port, that is, the transistor terminals, can therefore be modeled by a power sink element, as in Fig. 18.47.

The average switch network output port current, that is, the average diode current, is

$$\langle i_2(t) \rangle_{T_s} = \frac{1}{T_s} \int_0^{T_s} i_2(\tau) d\tau = \frac{q_2}{T_s} \quad (18.186)$$

By inspection of Fig. 18.46, the area  $q_2$  is given by

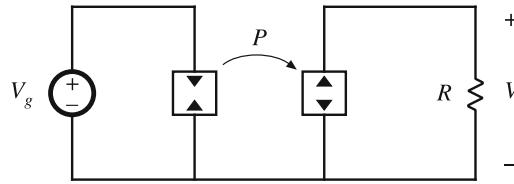
$$q_2 = \frac{1}{2} i_{pk} d_2 T_s \quad (18.187)$$

The duty cycle  $d_2$  is determined by the time required for the inductor current to return to zero, during the second subinterval. By arguments similar to those used to derive Eq. (15.19), the duty cycle  $d_2$  can be found as follows:

$$d_2(t) = d_1(t) \frac{\langle v_1(t) \rangle_{T_s}}{\langle v_2(t) \rangle_{T_s}} \quad (18.188)$$

Substitution of Eqs. (18.188), (18.187), and (18.185) into Eq. (18.186) yields

$$\langle i_2(t) \rangle_{T_s} = \frac{\langle p(t) \rangle_{T_s}}{\langle v_2(t) \rangle_{T_s}} \quad (18.189)$$



**Fig. 18.48** Steady-state model of the CPM DCM buck-boost converter

The output port of the averaged switch network is therefore described by the relationship

$$\langle i_2(t) \rangle_{T_s} \langle v_2(t) \rangle_{T_s} = \frac{\frac{1}{2} L I_c^2(t) f_s}{\left(1 + \frac{m_a}{m_1}\right)^2} = \langle p(t) \rangle_{T_s} \quad (18.190)$$

In the averaged model, the diode can be replaced by a power source of value  $\langle p(t) \rangle_{T_s}$ , equal to the power apparently consumed at the switch network input port. During the second subinterval, the inductor releases all of its stored energy through the diode, to the converter output. This results in an average power flow of value  $\langle p(t) \rangle_{T_s}$ .

A CPM DCM buck-boost averaged model is therefore as given in Fig. 18.47. In this model, the transistor is simply replaced by a power sink of value  $\langle p(t) \rangle_{T_s}$ , while the diode is replaced by a power source also of value  $\langle p(t) \rangle_{T_s}$ .

The steady-state equivalent circuit model of the CPM DCM buck-boost converter is obtained by letting the inductor and capacitor tend to short- and open-circuits, respectively. The model of Fig. 18.48 is obtained. The steady-state output voltage  $V$  can now be determined by equating the dc load power to the converter average power  $\langle p(t) \rangle_{T_s}$ . For a resistive load, one obtains

$$\frac{V^2}{R} = P \quad (18.191)$$

where the steady-state value of  $\langle p(t) \rangle_{T_s}$  is given by

$$P = \frac{\frac{1}{2} L I_c^2(t) f_s}{\left(1 + \frac{M_a}{M_1}\right)^2} \quad (18.192)$$

and where  $I_c$  is the steady-state value of the control input  $i_c(t)$ . Solution for  $V$  yields the following result

$$V = \sqrt{PR} = I_c \sqrt{\frac{RLf_s}{2\left(1 + \frac{M_a}{M_1}\right)^2}} \quad (18.193)$$

for the case of a resistive load.

Averaged models of the DCM CPM buck, boost, and other converters can be found in a similar manner. In each case, the average transistor waveforms are shown to follow a power sink characteristic, while the average diode waveforms follow a power source characteristic. The resulting equivalent circuits of the CPM DCM buck and boost converters are illustrated in Fig. 18.49. In each case, the average power is given by

$$\langle p(t) \rangle_{T_s} = \frac{\frac{1}{2} L_i^2(t) f_s}{\left(1 + \frac{m_a}{m_1}\right)^2} \quad (18.194)$$

with  $m_1$  defined as in Eq. (18.30).

Steady-state characteristics of the DCM CPM buck, boost, and buck-boost converters are summarized in Table 18.6. In each case, the dc load power is  $P_{load} = VI$  and  $P$  is given by Eq. (18.192). The conditions for operation of a current-programmed converter in the discontinuous conduction mode can be expressed as follows:

$$\begin{aligned} |I| &> |I_{crit}| && \text{for CCM} \\ |I| &< |I_{crit}| && \text{for DCM} \end{aligned} \quad (18.195)$$

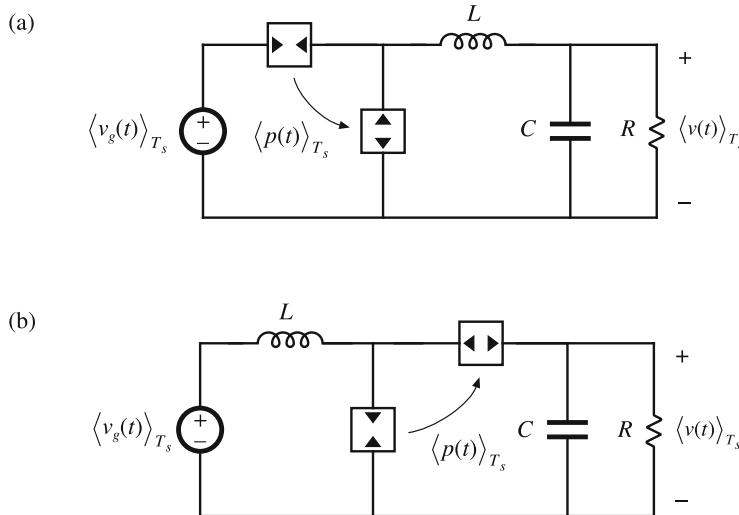
where  $I$  is the dc load current. The critical load current at the CCM-DCM boundary,  $I_{crit}$ , is expressed as a function of  $I_c$  and the voltage conversion ratio  $M = V/V_g$  in Table 18.6.

**Table 18.6** Steady-state DCM current-programmed characteristics of basic converters

Converter	$M$	$I_{crit}$	Stability range when $m_a = 0$
Buck	$\frac{P_{load} - P}{P_{load}}$	$\frac{1}{2}(I_c - Mm_a T_s)$	$0 \leq M < \frac{2}{3}$
Boost	$\frac{P_{load}}{P_{load} - P}$	$\frac{\left(I_c - \frac{M-1}{M}m_a T_s\right)}{2M}$	$0 \leq D \leq 1$
Buck-boost	Depends on load characteristic: $P_{load} = P$	$\frac{\left(I_c - \frac{M}{M-1}m_a T_s\right)}{2(M-1)}$	$0 \leq D \leq 1$

In the discontinuous conduction mode, the inductor current is zero at the beginning and end of each switching period. As a result, the current-programmed controller does not exhibit the type of instability described in Sect. 18.2. The current programmed controllers of DCM boost and buck-boost converters are stable for all duty cycles with no artificial ramp. However, the CPM DCM buck converter exhibits a different type of low-frequency instability when  $M > 2/3$  and  $m_a = 0$  that arises because the dc output characteristic is nonlinear and can exhibit two equilibrium points when the converter drives a resistive load. The stability range can be extended to  $0 \leq D \leq 1$  by addition of an artificial ramp having slope  $m_a > 0.086m_2$ , or by addition of output voltage feedback.

Small-signal models of DCM CPM converters can be derived by perturbation and linearization of the averaged models of Figs. 18.47 and 18.49. The results are given in Fig. 18.50. Parameters of the small-signal models are listed in Tables 18.7 and 18.8.



**Fig. 18.49** Averaged models of current-programmed DCM converters: (a) buck, (b) boost

The CPM DCM small-signal models of Fig. 18.50 are quite similar to the respective small-signal models of DCM duty ratio controlled converters illustrated in Figs. 15.19 and 15.21. The sole differences are the parameter expressions of Tables 18.7 and 18.8. Transfer functions can be determined in a similar manner. In particular, a simple approximate way to determine the low-frequency small-signal transfer functions of the CPM DCM buck, boost, and buck-boost converters is to simply let the inductance  $L$  tend to zero in the equivalent circuits of Fig. 18.50. This approximation is justified for frequencies sufficiently less than the converter switching frequency, because in the discontinuous conduction mode the value of  $L$  is small, and hence the pole and any RHP zero associated with  $L$  occur at frequencies near to or greater than the switching frequency. For all three converters, the equivalent circuit of Fig. 18.51 is obtained.

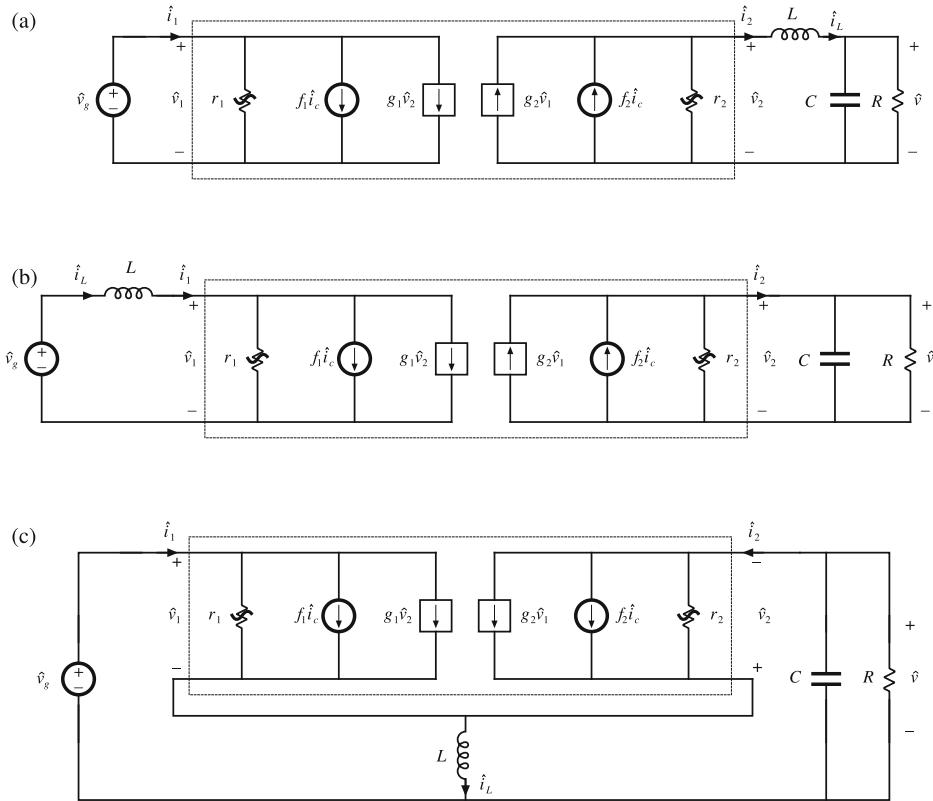
Figure 18.51 predicts that the control-to-output transfer function  $G_{vc}(s)$  is

$$G_{vc}(s) = \left. \frac{\hat{v}}{\hat{i}_c} \right|_{\hat{v}_g=0} = \frac{G_{c0}}{1 + \frac{s}{\omega_p}} \quad (18.196)$$

with

$$G_{c0} = f_2(R||r_2)$$

$$\omega_p = \frac{1}{(R||r_2)C}$$



**Fig. 18.50** Small-signal models of DCM CPM converters, derived by perturbation and linearization of Figs. 18.47 and 18.49: (a) buck, (b) boost, (c) buck-boost

The line-to-output transfer function is predicted to be

$$G_{vg}(s) = \left. \frac{\hat{v}}{\hat{v}_g} \right|_{\hat{i}_c=0} = \frac{G_{g0}}{1 + \frac{s}{\omega_p}} \quad (18.197)$$

with

$$G_{g0} = g_2(R \parallel r_2)$$

If desired, more accurate expressions which account for inductor dynamics can be derived by solution of the models of Fig. 18.50.

## 18.9 Average Current-Mode Control

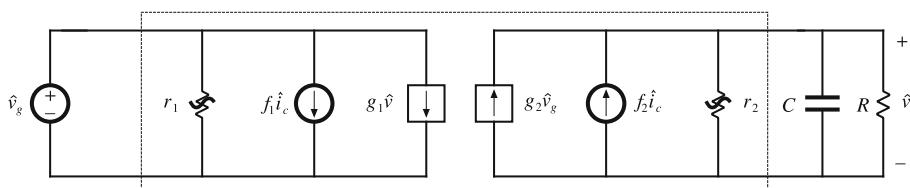
Average current-mode (ACM) control is another popular current programming technique [177, 178]. A block diagram of an average current-mode controlled converter is shown in Fig. 18.52. A sensed current signal  $R_f i$  is compared to a control signal  $v_c = R_f i_c$ , where  $R_f$  is the equivalent

**Table 18.7** Current-programmed DCM small-signal equivalent circuit parameters: input port

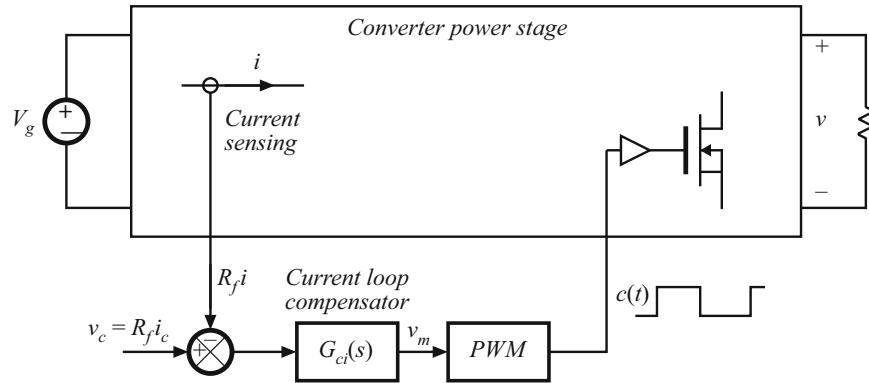
Converter	$g_1$	$f_1$	$r_1$
Buck	$\frac{1}{R} \left( \frac{M^2}{1-M} \right) \frac{\left(1 - \frac{m_a}{m_1}\right)}{\left(1 + \frac{m_a}{m_1}\right)}$	$2 \frac{I_t}{I_c}$	$-R \left( \frac{1-M}{M^2} \right) \frac{\left(1 + \frac{m_a}{m_1}\right)}{\left(1 - \frac{m_a}{m_1}\right)}$
Boost	$-\frac{1}{R} \left( \frac{M}{M-1} \right)$	$2 \frac{I}{I_c}$	$\frac{R}{M^2 \left( \frac{2-M}{M-1} + \frac{2m_a/m_1}{1+m_a/m_1} \right)}$
Buck-boost	0	$2 \frac{I_1}{I_c}$	$\frac{-R \left(1 + \frac{m_a}{m_1}\right)}{M^2 \left(1 - \frac{m_a}{m_1}\right)}$

**Table 18.8** Current-programmed DCM small-signal equivalent circuit parameters: output port

Converter	$g_2$	$f_2$	$r_2$
Buck	$\frac{1}{R} \left( \frac{M}{1-M} \right) \frac{\left(\frac{m_a}{m_1}(2-M)-M\right)}{\left(1+\frac{m_a}{m_1}\right)}$	$2 \frac{I}{I_c}$	$R \frac{(1-M)\left(1+\frac{m_a}{m_1}\right)}{\left(1-2M+\frac{m_a}{m_1}\right)}$
Boost	$\frac{1}{R} \left( \frac{M}{M-1} \right)$	$2 \frac{I_2}{I_c}$	$R \left( \frac{M-1}{M} \right)$
Buck-boost	$\frac{2M}{R} \frac{\left(\frac{m_a}{m_1}\right)}{\left(1+\frac{m_a}{m_1}\right)}$	$2 \frac{I_2}{I_c}$	$R$

**Fig. 18.51** Simplified small-signal model obtained by letting  $L$  become zero in Fig. 18.50a,b, or c

current sensing resistance. The error signal is processed by a current loop compensator  $G_{ci}(s)$ , which generates the control input  $v_m$  for a pulse-width modulator. In response, the PWM produces a switch control signal  $c(t)$  with duty cycle  $d$  proportional to the PWM control input  $v_m$ . One may note that the current control loop shown in Fig. 18.52 follows the same basic approach discussed in Chap. 9, except that the control objective is to regulate a converter current instead



**Fig. 18.52** Average current-mode controlled converter

of a converter voltage. Since current sensing and current loop compensator often incorporate low-pass filtering functions, the current control loop effectively regulates the average current  $\langle i(t) \rangle_{T_s}$ . Ideally,

$$\langle i(t) \rangle_{T_s} = \frac{1}{R_f} \langle v_c(t) \rangle_{T_s} \quad (18.198)$$

Average current-mode control finds significant application in PWM rectifiers and inverters; the rectifier application is discussed further in Sect. 21.3.1.

### 18.9.1 System Model and Transfer Functions

To design the current loop compensator  $G_{ci}(s)$ , it is convenient to represent the system small-signal model in a block diagram form, as shown in Fig. 18.53. The converter duty-cycle control transfer functions are based on the averaged converter models developed in Chap. 7. For the basic converters, these transfer functions are summarized in Tables 18.3, 18.4, 18.5. Applying the Feedback Theorem to the model in Fig. 18.53 yields an expression for the small-signal closed-loop response of the current  $\hat{i}$ ,

$$\hat{i} = \frac{1}{R_f} \frac{T_i}{1 + T_i} \hat{v}_c + G_{ig} \frac{1}{1 + T_i} \hat{v}_g \quad (18.199)$$

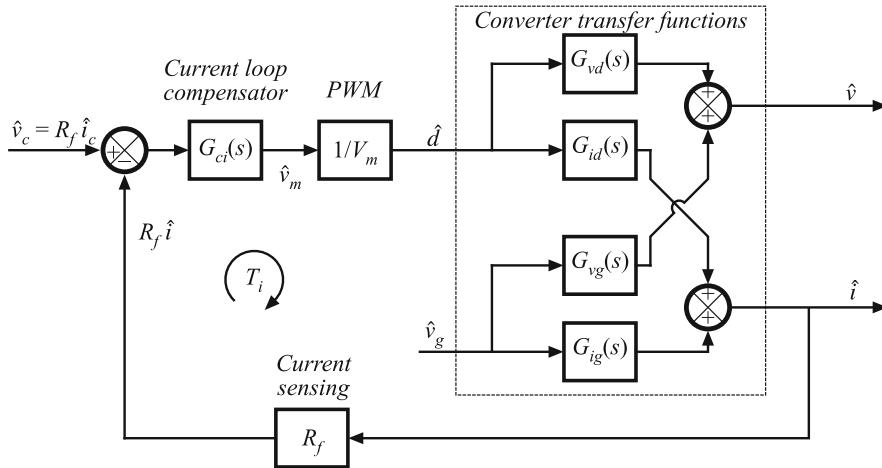
where the current loop gain  $T_i(s)$  is

$$T_i = R_f G_{ci} \frac{1}{V_M} G_{id} \quad (18.200)$$

The closed-loop control-to-current transfer function is

$$G_{ic}(s) = \left. \frac{\hat{i}}{\hat{v}_c} \right|_{\hat{v}_g=0} = \frac{1}{R_f} \frac{T_i}{1 + T_i} = G_{ic\infty} \frac{T_i}{1 + T_i} \quad (18.201)$$

where  $G_{ic\infty} = 1/R_f$  is the ideal closed-loop response of the average current control loop. One may note that the ideal closed-loop response of the average current control loop is identical



**Fig. 18.53** Block diagram that models the average current-mode control loop in Fig. 18.52

to the response predicted by the simple model of the current-programmed control discussed in Sect. 18.1. Designing the current loop compensator  $G_{ci}(s)$  amounts to shaping the current loop gain  $T_i$  to achieve a desired crossover frequency  $f_{ci}$  and stability margins, following the approaches discussed in Chap. 9.

Compared to CPM control (peak current mode) discussed in Sects. 18.8–18.8, average current-mode control has several advantages. First, direct control over the average current is required in some applications such as battery chargers, drivers for light emitting diodes, low-harmonic rectifiers, and grid-tied inverters. Furthermore, low-pass filtering associated with current sensing and  $G_{ci}$  implies reduced sensitivity to noise and switching disturbances. Stable operation can be achieved at any duty ratio without the need for slope compensation by addition of an artificial ramp. Limiting the current control signal  $v_c$  provides a limitation on the average but not the peak current. As a result, just as in duty-cycle controlled converters, additional circuitry is usually required to achieve cycle-by-cycle protection against excessive peak currents during transients or fault conditions in ACM controlled converters.

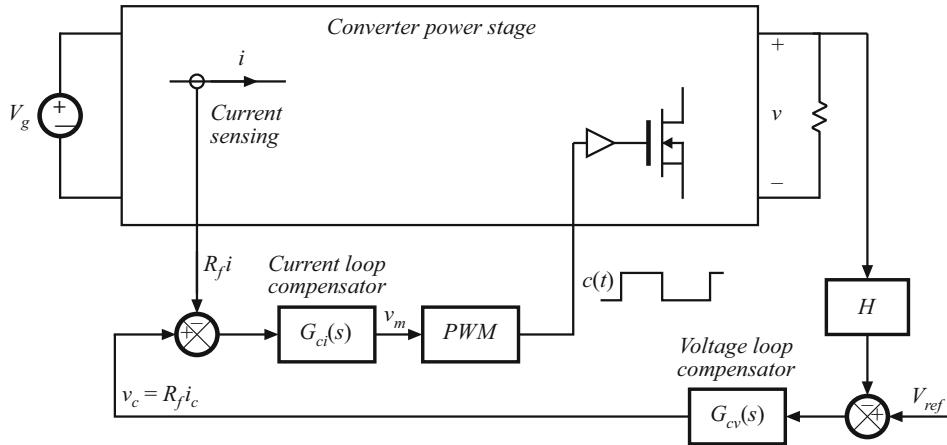
In many applications, an outer voltage control loop is closed around an ACM controlled converter, as shown in Fig. 18.54. In the outer voltage loop, a sensed output voltage  $Hv$  is compared to a reference  $V_{ref}$ . The error signal is processed by a voltage loop compensator  $G_{cv}$  to produce the control signal  $v_c$ , which serves as the reference for the current control loop. A small-signal model of the system in Fig. 18.54 is shown in Fig. 18.55.

Application of the Feedback Theorem to the inner current control loop yields the following expression for the small-signal output voltage as a function of perturbations in  $v_c$  and  $v_g$ ,

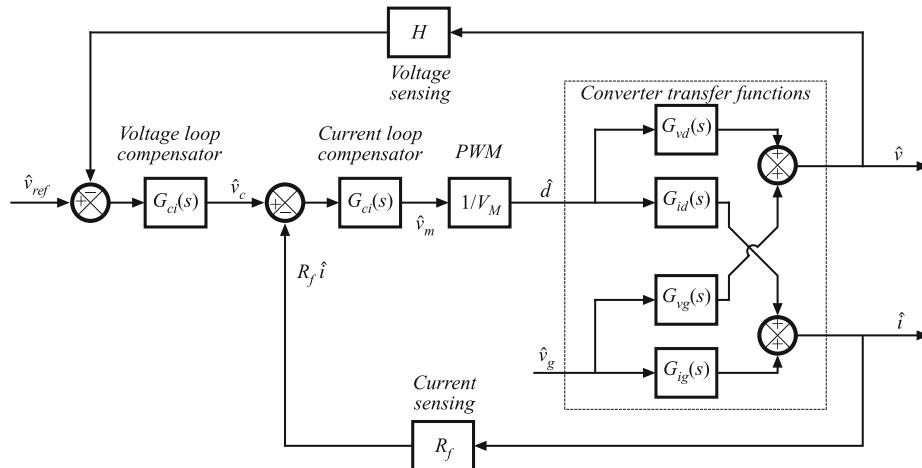
$$\hat{v} = \left( G_{ci} \frac{1}{V_M} G_{vd} \frac{1}{1 + T_i} \right) \hat{v}_c + \left( G_{vg}(s) - \frac{G_{ig}}{G_{id}} G_{vd} \frac{T_i}{1 + T_i} \right) \hat{v}_g \quad (18.202)$$

With the inner current control loop closed, the control-to-output voltage transfer function  $G_{vc}(s)$  is given by

$$G_{vc}(s) = \left. \frac{\hat{v}}{\hat{v}_c} \right|_{\hat{v}_g=0} = G_{ci} \frac{1}{V_M} G_{vd} \frac{1}{1 + T_i} = \frac{1}{R_f} \frac{G_{vd}}{G_{id}} \frac{T_i}{1 + T_i} \quad (18.203)$$



**Fig. 18.54** Output voltage control loop closed around an average current-mode controlled converter



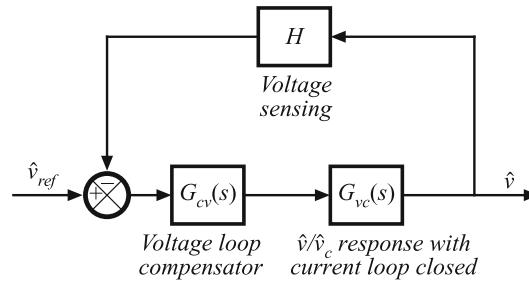
**Fig. 18.55** Block diagram that models the average current-mode controlled converter with an outer voltage control loop as shown in Fig. 18.54

For the purposes of designing the voltage loop compensator, the system block diagram of Fig. 18.55 can now be simplified as shown in Fig. 18.56. The voltage loop compensator design amounts to shaping the voltage loop gain

$$T_v = HG_{cv}G_{vc} \quad (18.204)$$

to achieve a desired crossover frequency and stability margins using the techniques discussed in Chap. 9.

It should be noted that the design of the two-loop system of Fig. 18.56 can be approached in a number of different ways. In the approach described above the inner current loop is designed



**Fig. 18.56** Block diagram that models the outer voltage control loop around an average current-mode controlled converter

first, based on the current loop gain  $T_i$ . Next, with the inner current loop closed, the control to voltage transfer function  $G_{vc}(s)$  is found from Eq. (18.203), and the voltage loop compensator is designed based on the outer voltage loop gain  $T_v$ , given by Eq. (18.204). This inner-loop first, outer-loop second design approach is illustrated by an example in the next section.

### 18.9.2 Design Example: ACM Controlled Boost Converter

An average current-mode controlled boost converter is shown in Fig. 18.57. The current and voltage control loops follow the block diagram of Fig. 18.54: average inductor current is regulated in the inner current control loop, and output voltage is regulated in the outer voltage control loop. The converter operates from  $V_g = 170$  V, and delivers  $P_{out} = 2$  kW of power at  $V = 400$  V. The switching frequency is  $f_s = 100$  kHz, the amplitude of the PWM saw-tooth ramp is  $V_M = 4$  V, and the equivalent current sensing resistance is  $R_f = 0.25$  Ω. The voltage reference is  $V_{ref} = 3$  V, and the voltage sensing gain is  $H = V_{ref}/V = 0.0075$ . In this example, the objectives are to design a current loop compensator  $G_{ci}$  to attain a crossover frequency of  $f_{ci} = 10$  kHz, or one tenth of the switching frequency, and then to design a voltage loop compensator  $G_{cv}$  so that a crossover frequency of  $f_{cv} = 1$  kHz is obtained in the outer voltage control loop. Converter losses can be neglected.

At the quiescent dc operating point,

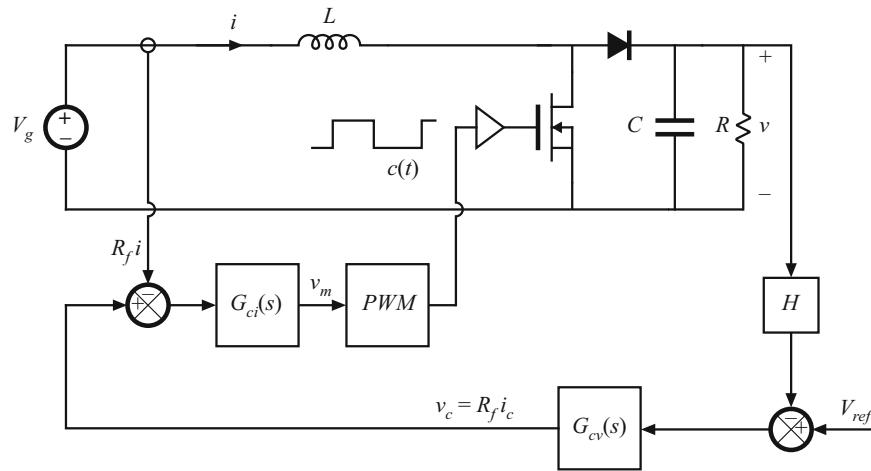
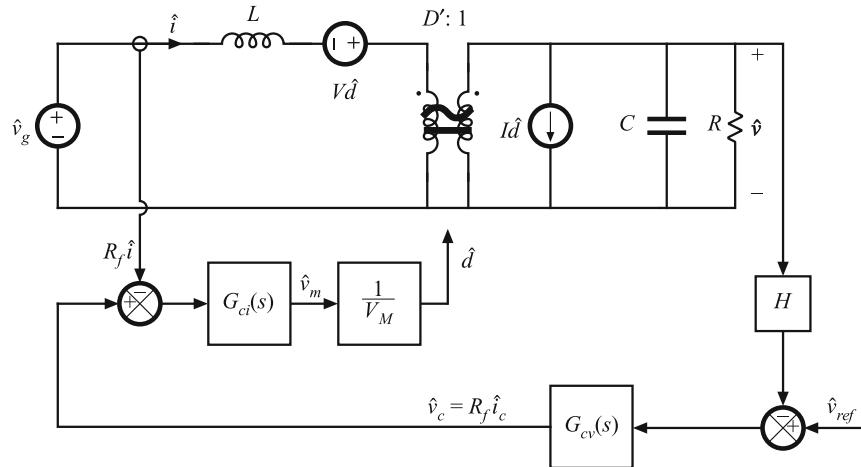
$$D = 1 - \frac{V_g}{V} = 0.575$$

$$I_g = I = \frac{P_{out}}{V_g} = 11.8 \text{ A}$$

$$V_c = R_f I = 2.94 \text{ V}$$

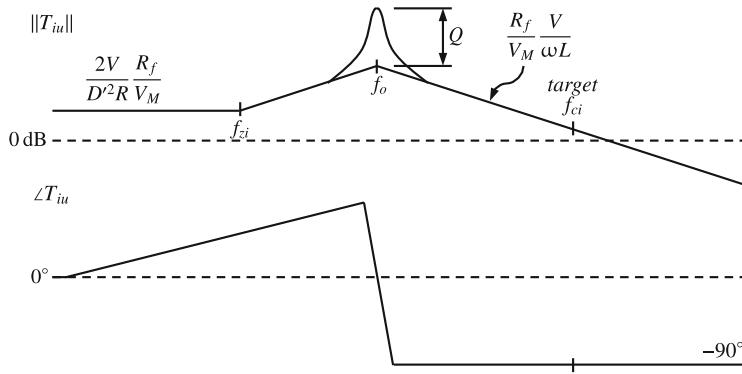
A small-signal model of the ACM controlled boost converter is shown in Fig. 18.58. From Eq. (18.200), the uncompensated current loop gain  $T_{iu}$ , with unity gain compensator  $G_{ci} = 1$ , is

$$T_{iu} = \frac{R_f}{V_M} G_{id}(s) \quad (18.205)$$

**Fig. 18.57** Average current-mode controlled boost converter**Fig. 18.58** Small-signal model of the average current-mode controlled boost converter of Fig. 18.57

where the converter duty-cycle to inductor current transfer function  $G_{id}(s)$  is given by

$$G_{id}(s) = \left. \frac{\hat{i}}{\hat{d}} \right|_{\hat{v}_g=0} = G_{id0} \frac{1 + \frac{s}{\omega_{zi}}}{1 + \frac{1}{Q} \frac{s}{\omega_o} + \left( \frac{s}{\omega_o} \right)^2} \quad (18.206)$$



**Fig. 18.59** Uncompensated loop gain for the current-mode controlled boost converter of Fig. 18.57

$$G_{id0} = \frac{2V}{D'^2 R} = 55.4 \text{ A} \rightarrow 34.9 \text{ dB A}$$

$$f_{zi} = \frac{1}{\pi RC} = 121 \text{ Hz}$$

$$f_o = \frac{D'}{2\pi\sqrt{LC}} = 745 \text{ Hz}$$

$$Q = D'R\sqrt{\frac{C}{L}} = 12.4 \rightarrow 21.8 \text{ dB}$$

The uncompensated current loop gain is sketched in Fig. 18.59. The low-frequency gain equals

$$T_{iu0} = \frac{R_f}{V_M} G_{id0} = 3.46 \rightarrow 10.8 \text{ dB} \quad (18.207)$$

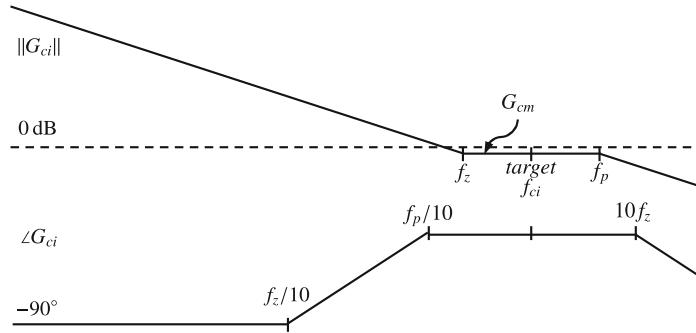
Around the target crossover frequency  $f_{ci} = 10 \text{ kHz}$ , the magnitude of  $T_{iu}$  rolls off at  $-20 \text{ dB/dec}$ ,

$$\|T_{iu}\| \rightarrow T_{iu0} \frac{\omega_o^2}{\omega_{zi}\omega} = \frac{R_f}{L\omega} \frac{V}{V_M} \quad (18.208)$$

while the corresponding phase response asymptote equals  $-90^\circ$ . A simple gain (proportional (P) compensator) would therefore be sufficient to achieve the desired crossover frequency with adequate phase margin. As discussed in Sect. 9.5.2, a lag (PI) compensator offers a way to increase the low-frequency loop gain and to achieve perfect dc regulation of the average inductor current. Furthermore, a pole is typically added in the current loop compensator transfer function in order to attenuate high-frequency switching ripple, and low-pass filter the sensed current signal. A typical ACM current loop compensator transfer function is therefore given by

$$G_{ci}(s) = G_{cm} \frac{1 + \frac{\omega_z}{s}}{1 + \frac{s}{\omega_p}} \quad (18.209)$$

and the compensator response is sketched in Fig. 18.60.



**Fig. 18.60** Magnitude and phase responses of the current loop compensator

The compensator zero is placed below the target crossover frequency ( $f_z < f_{ci}$ ), while the pole is placed above the crossover frequency ( $f_p > f_{ci}$ ). Using Eq. (18.208), gain  $G_{cm}$  is selected so that the loop gain magnitude equals 1 (0 dB) at the target crossover frequency  $f_{ci}$ ,

$$G_{cm} \frac{R_f}{L\omega_{ci}} \frac{V}{V_M} = 1 \quad (18.210)$$

Hence,

$$G_{cm} = \frac{L\omega_{ci}}{R_f} \frac{V_M}{V} = 0.63 \quad (18.211)$$

The phase margin can be found by adding contributions of the pole at zero of the PI compensator ( $-90^\circ$ ), the quadratic pole and zero in  $G_{id}$  (approximately  $-90^\circ$ ), as well as the compensator zero at  $f_z$  and the pole at  $f_p$ ,

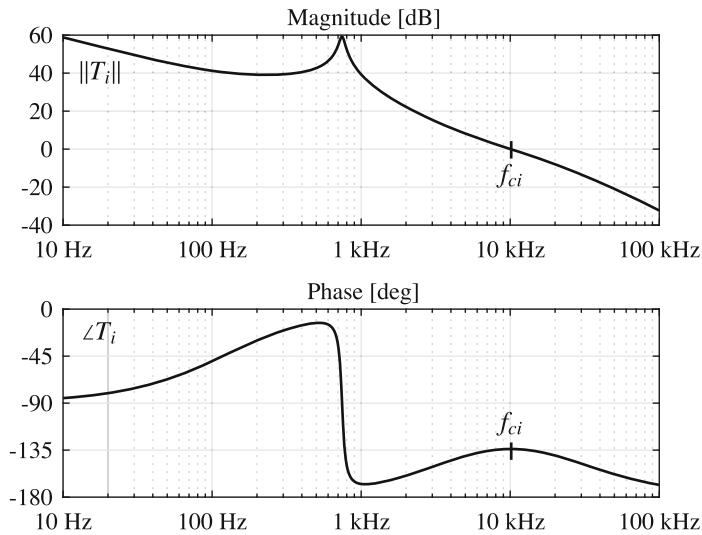
$$\varphi_m = 180^\circ + \angle T_i(j\omega_{ci}) = 180^\circ - 90^\circ - 90^\circ + \tan^{-1} \left( \frac{f_{ci}}{f_z} \right) - \tan^{-1} \left( \frac{f_{ci}}{f_p} \right) \quad (18.212)$$

A lower  $f_z$  contributes to a higher phase margin at the expense of reduced loop gain magnitude at frequencies below  $f_{ci}$ . A higher  $f_p$  contributes to a higher phase margin at the expense of reduced attenuation of the switching ripple by the compensator. Choosing, somewhat arbitrarily,  $f_z = f_{ci}/2.5 = 4$  kHz and  $f_p = 2.5f_{ci} = 25$  kHz, results in the phase margin of

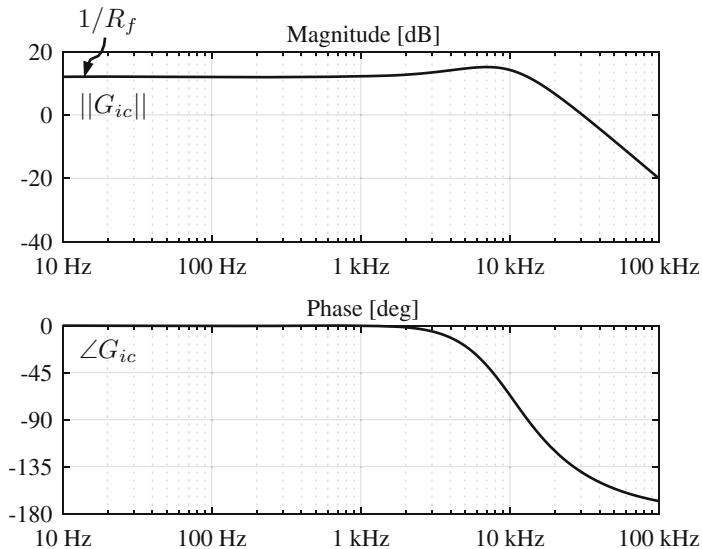
$$\varphi_m = 68^\circ - 22^\circ = 46^\circ \quad (18.213)$$

Magnitude and phase responses of the compensated current loop gain are shown in Fig. 18.61, confirming that the compensator in Eq. (18.209) with  $G_{cm} = 0.63$ ,  $f_z = 4$  kHz, and  $f_p = 25$  kHz meets the design objectives.

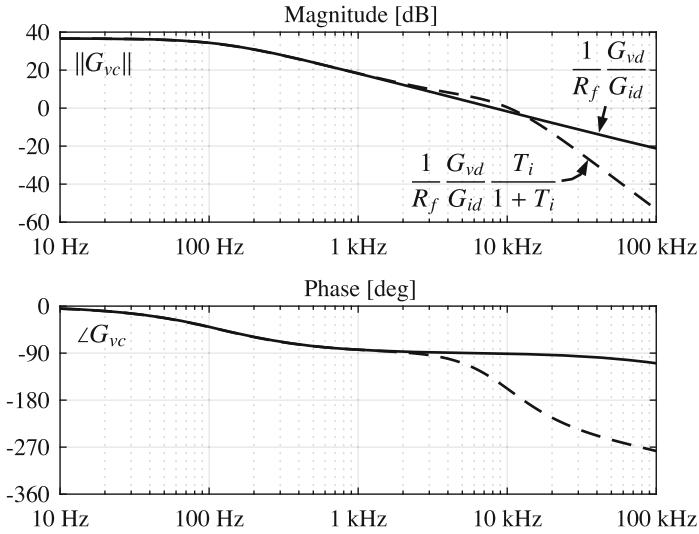
The closed-loop control-to-current transfer function  $G_{ic}$  found using Eq. (18.201) has magnitude and phase responses shown in Fig. 18.62. At low frequencies, the closed-loop response follows the ideal gain  $G_{ic\infty} = 1/R_f$ . Given  $\varphi_m = 46^\circ$ , the closed-loop transfer function exhibits a peaked response at frequencies near the crossover frequency  $f_{ci}$ , which is consistent with the discussion in Sect. 9.4.3.



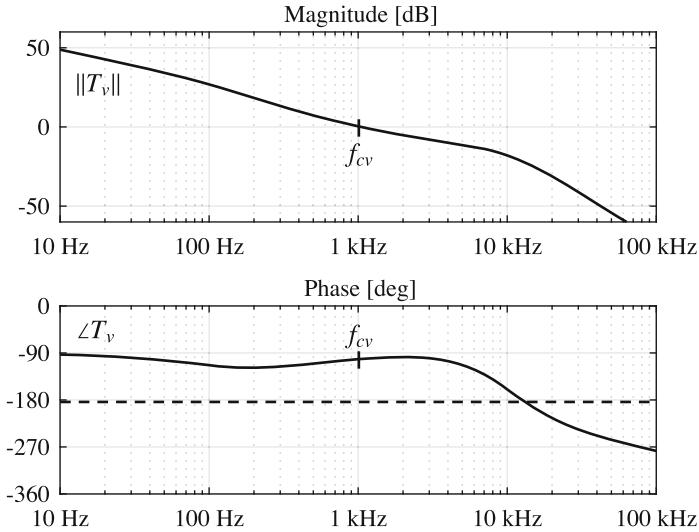
**Fig. 18.61** Compensated loop gain for the average current-mode controlled boost converter of Fig. 18.57



**Fig. 18.62** Closed-loop control-to-current response in the average current-mode controlled boost converter of Fig. 18.57



**Fig. 18.63** Closed-loop control-to-output voltage response in the average current-mode controlled boost converter of Fig. 18.57



**Fig. 18.64** Loop gain in the voltage control loop around the average current-mode controlled boost converter of Fig. 18.57

The next step is to design a voltage loop compensator  $G_{cv}$  to attain a crossover of  $f_{cv}$  in the outer voltage control loop. The design is based on the block diagram of Fig. 18.54, where  $G_{vc}$  is the closed-loop control-to-output voltage transfer function found from Eq. (18.203) and shown in Fig. 18.63. At frequencies well below the current loop crossover  $f_{ci}$ ,  $G_{vc}$  can be approximated

as

$$G_{vc} \approx \frac{1}{R_f} \frac{G_{vd}}{G_{id}} = \frac{D'R}{2R_f} \frac{1 - \frac{s}{\omega_{z,RHP}}}{1 + \frac{s}{\omega_{zi}}} \quad (18.214)$$

$$f_{z,RHP} = \frac{D'^2 R}{2\pi L} = 9.2 \text{ kHz}$$

$$f_{zi} = \frac{1}{\pi R C} = 121 \text{ Hz}$$

The magnitude and phase responses of the complete  $G_{vc}$  from Eq. (18.203) and the approximate  $G_{vc}$  from Eq. (18.214) are shown in Fig. 18.63. In cases when  $f_{cv} \ll f_{ci}$ , i.e., when the voltage loop is designed conservatively, the design of the voltage loop compensator  $G_{cv}$  can be based on the approximate  $G_{vc}$  from Eq. (18.214). Since  $G_{vc}$  has a dominant pole at  $f_{zi}$  and behaves as a single-pole transfer function around the target voltage loop crossover of  $f_{cv} = 1 \text{ kHz}$ , it is sufficient to consider a simple PI compensator

$$G_{cv}(s) = G_{vm} \left( 1 + \frac{\omega_{zv}}{s} \right) \quad (18.215)$$

where  $G_{vm}$  can be found from Eq. (18.204) to attain the desired crossover frequency  $f_{cv}$ ,

$$G_{vm} = \frac{2\pi f_{cv} CR_f}{D'H} = 16.4 \quad (18.216)$$

and  $f_{zv}$  can be selected to achieve a tradeoff between phase margin and the magnitude of  $T_v$  at frequencies below  $f_{cv}$ . Selecting

$$f_{zv} = \frac{f_{cv}}{3} = 333 \text{ Hz} \quad (18.217)$$

results in the voltage loop phase margin of

$$\varphi_{mv} \approx 180^\circ - 90^\circ - 90^\circ + \tan^{-1} \frac{f_{cv}}{f_{zv}} = 72^\circ \quad (18.218)$$

The resulting voltage loop gain is shown in Fig. 18.64.

The two-step design process illustrated by the example above is relatively simple: the inner current loop is designed first, followed by the voltage loop design. In both loops around ACM controlled converters, simple PI compensators are typically sufficient to achieve desired regulation bandwidths with adequate stability margins. In the ACM controlled boost design example, we followed a conservative approach where the outer voltage loop crossover frequency  $f_{cv}$  is set to be well below the current loop crossover frequency  $f_{ci}$ . This approach, while commonly applied in practice, is not necessarily the only available option. Depending on application and regulation bandwidth requirements, other approaches can be pursued in two-loop systems.

## 18.10 Summary of Key Points

1. In current-programmed control, the peak switch current  $i_s(t)$  follows the control input  $i_c(t)$ . This widely used control scheme has the advantage of a simpler control-to-output transfer function. The line-to-output transfer functions of current-programmed buck converters are also reduced.
2. The basic current-programmed controller is unstable when  $D > 0.5$ , regardless of the converter topology. The controller can be stabilized by addition of an artificial ramp having slope  $m_a$ . When  $m_a > 0.5m_2$ , then the controller is stable for all duty cycles.
3. The behavior of current-programmed converters can be modeled in a simple and intuitive manner by the first-order approximation  $\langle i_L(t) \rangle_{T_s} \approx i_c(t)$ . The averaged terminal waveforms of the switch network can then be modeled simply by a current source of value  $i_c$ , in conjunction with a power sink or power source element. Perturbation and linearization of these elements leads to the small-signal model. Alternatively, the small-signal converter equations derived in Chap. 7 can be adapted to cover the current-programmed mode, using the simple approximation  $i_L(t) \approx i_c(t)$ .
4. The simple model predicts that one pole is eliminated from the converter line-to-output and control-to-output transfer functions. Current programming does not alter the transfer function zeroes. The dc gains become load-dependent.
5. The more accurate model of Sect. 18.3 correctly accounts for the difference between the average inductor current  $\langle i_L(t) \rangle_{T_s}$  and the control input  $i_c(t)$ . This model predicts the nonzero line-to-output transfer function  $G_{vg}(s)$  of the buck converter. The current-programmed controller behavior is modeled by a block diagram, which is appended to the small-signal converter models derived in Chap. 7. Analysis of the resulting multiloop feedback system Sect. 18.4 then leads to the relevant transfer functions derived.
6. The more accurate model predicts that the inductor pole occurs at the crossover frequency  $f_c$  of the effective current feedback loop gain  $T_i(s)$ . The frequency  $f_c$  typically occurs in the vicinity of the converter switching frequency  $f_s$ . The more accurate model also predicts that the line-to-output transfer function  $G_{vg}(s)$  of the buck converter is nulled when  $m_a = 0.5m_2$ .
7. The more accurate averaged CPM model of Sect. 18.3 can be implemented as a SPICE subcircuit, as shown in Sect. 18.5. The averaged CPM model can then be combined with averaged switch models of Chap. 14 to construct averaged circuit models suitable for SPICE simulations.
8. A converter system incorporating current-programmed control often includes an outer voltage feedback loop, the purpose of which is to regulate the converter output voltage. Since current programming results in simpler control-to-output dynamics, wide-bandwidth output voltage control can usually be obtained without the use of compensator lead networks, as discussed in Sect. 18.6.
9. Current-programmed converters operating in the discontinuous conduction mode are modeled in Sect. 18.8. The averaged transistor waveforms can be modeled by a power sink, while the averaged diode waveforms are modeled by a power source. The power is controlled by  $i_c(t)$ . Perturbation and linearization of these averaged models, as usual, leads to small-signal equivalent circuits.
10. Neither the simple model of Sect. 18.1, which neglects inductor dynamics, nor the more accurate model of Sect. 18.3, which implies a single-pole response at high frequencies, predicts current-programmed instability or the need for the artificial ramp discussed in

Sect. 18.2. Section 18.7 explains high-frequency dynamics of current-programmed converters using sampled-data modeling techniques. The sampled-data model shows how the control-to-current frequency response exhibits peaking around one half of the switching frequency if the artificial ramp slope  $m_a$  is small, ultimately leading to instability for duty cycles greater than 0.5 if no artificial ramp is employed. Addition of artificial ramp leads to stable operation, reduced sensitivity to noise, and frequency responses that are well predicted by the more accurate averaged model of Sect. 18.3.

11. Average current-mode (ACM) control is another popular control technique where an average current is sensed and controlled using a feedback loop around a duty-cycle controlled converter. ACM controllers have improved noise immunity, and exhibit stable operation over wide range of duty cycles as well as relatively simple dynamics. In addition to construction of inner current control loops, ACM controllers are often used in applications that require direct control over the converter average input or output current, such as battery chargers, drivers for light emitting diodes, as well as grid-tied rectifiers and inverters.

## PROBLEMS

**18.1** A nonideal buck converter operates in the continuous conduction mode, with the values  $V_g = 10 \text{ V}$ ,  $f_2 = 100 \text{ kHz}$ ,  $L = 4 \mu\text{H}$ ,  $C = 75 \mu\text{F}$ , and  $R = 0.25 \Omega$ . The desired full-load output is 5 V at 20 A. The power stage contains the following loss elements: MOSFET on-resistance  $R_{on} = 0.1 \Omega$ , Schottky diode forward voltage drop  $V_D = 0.5 \text{ V}$ , inductor winding resistance  $R_L = 0.03 \Omega$ .

- (a) Steady-state analysis: determine the converter steady-state duty cycle  $D$ , the inductor current ripple slopes  $m_1$  and  $m_2$ , and the dimensionless parameter  $K = 2L/RT_s$ .
- (b) Determine the small-signal equations for this converter, for duty-cycle control.

A current-programmed controller is now implemented for this converter. An artificial ramp is used, having a fixed slope  $M_a = 0.5M_2$ , where  $M_2$  is the steady-state slope  $m_2$  obtained with an output of 5 V at 20 A.

- (c) Over what range of  $D$  is the current-programmed controller stable? Is it stable at rated output?

Note that the nonidealities affect the stability boundary.

- (d) Determine the control-to-output transfer function  $G_{vc}(s)$ , using the simple approximation  $\langle i_L(t) \rangle_{T_s} \approx i_c(t)$ . Give analytical expressions for the corner frequency and dc gain. Sketch the Bode plot of  $G_{vc}(s)$ .

**18.2** Use the averaged switch modeling approach to model the CCM boost converter with current-programmed control:

- (a) Define the switch network terminal quantities as in Fig. 14.13a. With the assumption that  $\langle i_L(t) \rangle_{T_s} \approx i_c(t)$ , determine expressions for the average values of the switch network terminal waveforms, and hence derive the equivalent circuit of Fig. 18.9a.
- (b) Perturb and linearize your model of part (a), to obtain the equivalent circuit of Fig. 18.13.
- (c) Solve your model of part (b), to derive expressions for the control-to-output transfer function  $G_{vc}(s)$  and the line-to-output transfer function  $G_{vg}(s)$ . Express your results in standard normalized form, and give analytical expressions for the corner frequencies and dc gains.

- 18.3** Use the averaged switch modeling approach to model the CCM Ćuk converter with current-programmed control. A Ćuk converter is diagrammed in Fig. 2.20.
- It is desired to model the switch network with an  $i_c$  current source and a dependent power source or sink, using the approach of Sect. 18.1.2. How should the switch network terminal voltages and currents be defined?
  - Sketch the switch network terminal voltage and current waveforms. With the assumption that  $\langle i_1(t) \rangle_{T_s} - \langle i_2(t) \rangle_{T_s} \approx i_c(t)$  (where  $i_1$  and  $i_2$  are the inductor currents defined in Fig. 2.20), determine expressions for the average values of the switch network terminal waveforms, and hence derive an equivalent circuit similar to the equivalent circuits of Fig. 18.9.
  - Perturb and linearize your model of part (b), to obtain a small-signal equivalent circuit similar to the model of Fig. 18.10. It is not necessary to solve your model.
- 18.4** The full-bridge converter of Fig. 6.20a operates with  $V_g = 320$  V, and supplies 1000 W to a 42 V resistive load. Losses can be neglected, the duty cycle is 0.7, and the switching period  $T_s$  defined in Fig. 6.21 is 10 µsec.  $L = 50\text{ }\mu\text{H}$  and  $C = 100\text{ }\mu\text{F}$ . A current-programmed controller is employed, whose waveforms are referred to the secondary side of the transformer. In the following calculations, you may neglect the transformer magnetizing current.
- What is the minimum artificial ramp slope  $m_a$  that will stabilize the controller at the given operating point? Express your result in terms of  $m_2$ .
  - An artificial ramp having the slope  $m_a = m_2$  is employed. Sketch the Bode plot of the current loop gain  $T_i(s)$ , and label numerical values of the corner frequencies and dc gains. It is not necessary to re-derive the analytical expression for  $T_i$ . Determine the crossover frequency  $f_c$ .
  - For  $m_a = m_2$ , sketch the Bode plots of the control-to-output transfer function  $G_{vc}(s)$  and line-to-output transfer function  $G_{vg}(s)$ , and label numerical values of the corner frequencies and dc gains. It is not necessary to re-derive analytical expressions for these transfer functions.
- 18.5** In a CCM current-programmed buck converter, it is desired to minimize the line-to-output transfer function  $G_{vg}(s)$  via the choice  $m_a = 0.5m_2$ . However, because of component tolerances, the value of inductance  $L$  can vary by  $\pm 10\%$  from its nominal value of  $100\text{ }\mu\text{H}$ . Hence,  $m_a$  is fixed in value while  $m_2$  varies, and  $m_a = 0.5m_2$  is obtained only at the nominal value of  $L$ . The switching frequency is 100 kHz, the output voltage is 15 V, the load current varies over the range 2 to 4 A, and the input voltage varies over the range 22 to 32 V. You may neglect losses. Determine the worst-case (maximum) value of the line-to-output dc gain  $G_{vg}(0)$ .
- 18.6** The nonideal flyback converter of Fig. 7.19 employs current-programmed control, with artificial ramp having slope  $m_a$ . MOSFET  $Q_1$  exhibits on-resistance  $R_{on}$ . All current-programmed controller waveforms are referred to the transformer primary side.
- Derive a block diagram which models the current-programmed controller, of form similar to Fig. 18.24. Give analytical expressions for the gains in your block diagram.
  - Combine your result of part (a) with the converter small-signal model. Derive a new expression for the control-to-output transfer function  $G_{vc}(s)$ .
- 18.7** A buck converter operates with current-programmed control. The element values are

$$\begin{array}{ll} V_g = 120 \text{ V} & D = 0.6 \\ R = 10 \Omega & f_s = 100 \text{ kHz} \\ L = 550 \mu\text{H} & C = 100 \mu\text{F} \end{array}$$

An artificial ramp is employed, having slope 0.15 A/μsec.

- (a) Construct the magnitude and phase asymptotes of the control-to-output transfer function  $G_{vd}(s)$  for duty-cycle control. On the same plot, construct the magnitude and phase asymptotes of the control-to-output transfer function  $G_{vc}(s)$  for current-programmed control. Compare.
- (b) Construct the magnitude asymptotes of the line-to-output transfer function  $G_{vg}(s)$  for duty-cycle control. On the same plot, construct the magnitude asymptotes of the line-to-output transfer function  $G_{vg-cpm}(s)$  for current-programmed control. Compare.

**18.8** A buck-boost converter operates in the discontinuous conduction mode. Its current-programmed controller has no compensating artificial ramp:  $m_a = 0$ .

- (a) Derive an expression for the control-to-output transfer function  $G_{vc}(s)$ , using the approximation  $L \approx 0$ . Give analytical expressions for the corner frequency and dc gain.
- (b) Repeat part (a), with the inductor included. Show that, provided the inductor is sufficiently small, then the inductor merely adds a high-frequency pole and zero to  $G_{vc}(s)$ , and the low-frequency pole derived in part (a) is essentially unchanged.
- (c) At the CCM-DCM boundary, what is the minimum value of the RHP zero frequency?

**18.9** A current-programmed boost converter interfaces a 3 V battery to a small portable 5 V load. The converter operates in the discontinuous conduction mode, with constant transistor on-time  $t_{on}$  and variable off-time; the switching frequency can therefore vary and is used as the control variable. There is no artificial ramp, and the peak transistor current  $i_c$  is equal to a fixed value  $I_c$ ; in practice,  $I_c$  is chosen to minimize the total loss.

- (a) Sketch the transistor and diode voltage and current waveforms. Determine expressions for the waveform average values, and hence derive a large-signal averaged equivalent circuit for this converter.
- (b) Perturb and linearize your model of part (a), to obtain a small-signal equivalent circuit. Note that the switching frequency  $f_s$  should be perturbed.
- (c) Solve your model of part (b), to derive an expression for the low-frequency control-to-output transfer function  $G_{vf}(s) = \hat{v}(s)/\hat{f}_s(s)$ . Express your results in standard normalized form, and give analytical expressions for the corner frequencies and dc gains.

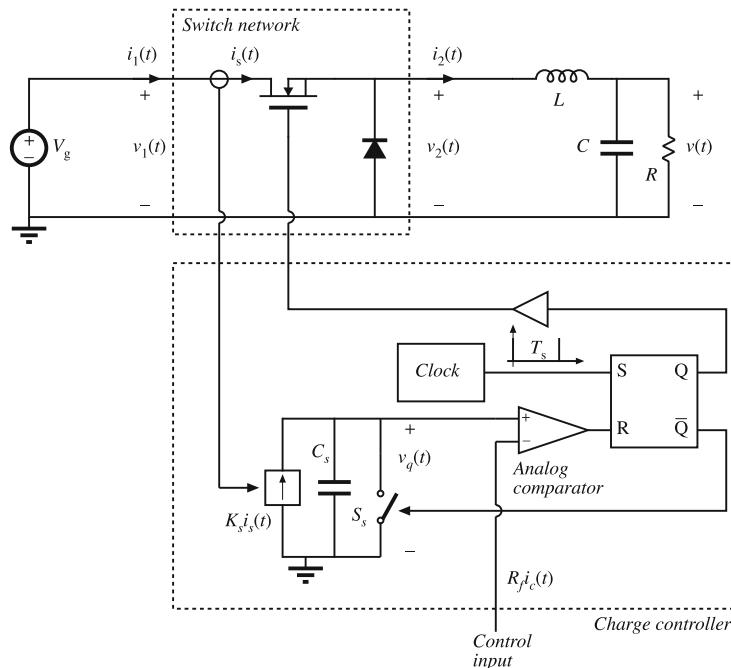
You may assume that  $L$  is small.

**18.10** A current-programmed boost converter is employed in a low-harmonic rectifier system, in which the input voltage is a rectified sinusoid:  $v_g(t) = V_M |\sin(\omega t)|$ . The dc output voltage is  $v(t) = V > V_M$ . The capacitance  $C$  is large, such that the output voltage contains negligible ac variations. It is desired to control the converter such that the input current  $i_g(t)$  is proportional to  $v_g(t)$ :  $i_g(t) = v_g(t)/R_e$ , where  $R_e$  is a constant, called the “emulated resistance.” The averaged boost converter model of Fig. 18.9a suggests that this can be accomplished by simply letting  $i_c(t)$  be proportional to  $v_g(t)$ , according to  $i_c(t) = v_g(t)/R_e$ . You may make the simplifying assumption that the converter always operates in the continuous conduction mode.

- (a) Solve the model of Fig. 18.9a, subject to the assumptions listed above, to determine the power  $\langle p(t) \rangle_{T_s}$ . Find the average value of  $\langle p(t) \rangle_{T_s}$ , averaged over one cycle of the ac input  $v_g(t)$ .

- (b) An artificial ramp is necessary to stabilize the current-programmed controller at some operating points. What is the minimum value of  $m_a$  that ensures stability at all operating points along the input rectified sinusoid? Express your result as a function of  $V$  and  $L$ . Show your work.
- (c) The artificial ramp and inductor current ripple cause the average input current to differ from  $i_c(t)$ . Derive an algebraic expression for  $\langle i_g(t) \rangle_{T_s}$ , as a function of  $i_c(t)$  and other quantities such as  $m_a$ ,  $v_g(t)$ ,  $V$ ,  $L$ , and  $T_s$ . For this part, you may assume that the inductor dynamics are negligible. Show your work.
- (d) Substitute  $v_g(t) = V_M |\sin(\omega t)|$  and  $i_c(t) = v_g(t)/R_e$ , into your result of part (c), to determine an expression for  $i_g(t)$ . How does  $i_g(t)$  differ from a rectified sinusoid?

- 18.11** Figure 18.65 shows a buck converter with a charge controller [179]. Operation of the charge controller is similar to operation of the current-programmed controller. At the beginning of each switching period, at time  $t = 0$ , a short clock pulse sets the SR latch. The logic high signal at the  $Q$  output of the latch turns the power MOSFET on. At the same time, the logic low signal at the  $\bar{Q}$  output of the latch turns the switch  $S_s$  off. Current  $K_s i_s$  proportional to the power MOSFET current charges the capacitor  $C_s$ . At  $t = dT_s$ , the capacitor voltage  $v_q(t)$  reaches the control input voltage  $R_f i_c$ , the comparator output goes high and resets the latch. The logic low signal at the  $Q$  output of the latch turns the power MOSFET off. At the same time, the logic high signal at the  $\bar{Q}$  output of the latch turns the switch  $S_s$  on, which quickly discharges the capacitor  $C_s$  to zero.



**Fig. 18.65** Buck converter with charge controller, Problem 18.11

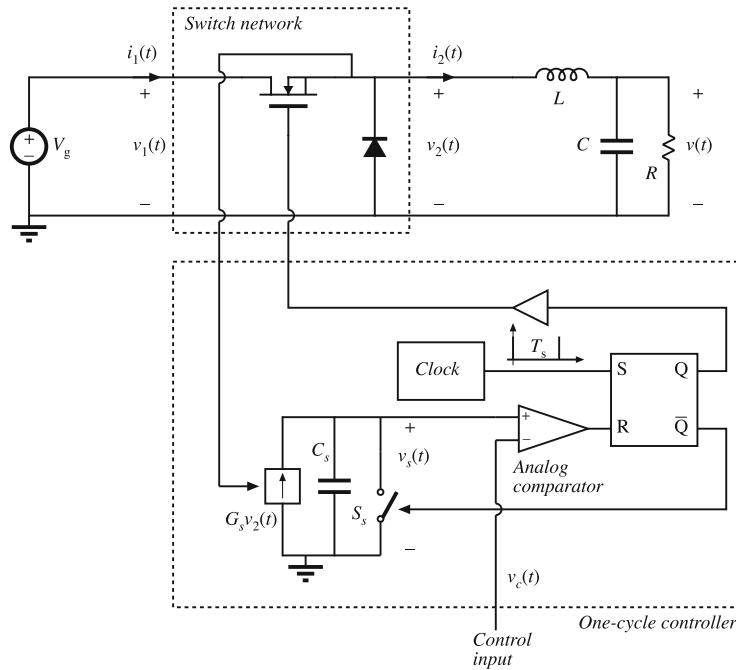
In this problem, the converter and controller parameters are:  $V_g = 24 \text{ V}$ ,  $f_s = 1/T_s = 100 \text{ kHz}$ ,  $L = 60 \mu\text{H}$ ,  $C = 100 \mu\text{F}$ ,  $R = 3 \Omega$ ,  $K_s T_s / C_s = R_f = 1 \Omega$ . You can assume that the converter operates in continuous conduction mode.

- (a) Find expressions for the average values of the switch network terminal waveforms, and hence derive a large-signal averaged switch model of the buck switch network with charge control. The control input to the model is the control current  $i_c$ . The averaged switch model should consist of a current source and a power source. The switch duty cycle  $d$  should not appear in the model.
- (b) Using the averaged switch model derived in part (a), find an expression for the quiescent output voltage  $V$  as a function of  $V_g$ ,  $I_c$ , and  $R$ . Given  $I_c = 2 \text{ A}$ , find numerical values for  $V$ ,  $I_1$ ,  $I_2$ , and the duty cycle  $D$ . For this quiescent operating point, sketch the waveforms  $i_1(t)$ ,  $i_2(t)$ , and  $v_q(t)$  during one switching period.
- (c) Perturb and linearize the averaged switch model from part (a) to derive a small-signal averaged switch model for the buck switch network with charge control. Find analytical expressions for all parameter values in terms of the converter parameters and the quiescent operating conditions. Sketch the complete small-signal model of the buck converter with the charge controller.
- (d) Solve the model obtained in part (c) to find the control-to-output transfer function  $G_{vc}(s) = \hat{v}/\hat{i}_c$ . At the quiescent operating point found in part (b), construct the Bode plot for the magnitude of  $G_{vc}$  and label all salient features of the magnitude response.
- (e) Comment on advantages charge control may have compared to duty-cycle control or current-programmed control.

- 18.12** Figure 18.66 shows a buck converter with a one-cycle controller [180]. Operation of the one-cycle controller is similar to operation of the current-programmed controller. At the beginning of each switching period, at time  $t = 0$ , a short clock pulse sets the SR latch. The logic high signal at the  $Q$  output of the latch turns the power MOSFET on. At the same time, the logic low signal at the  $\bar{Q}$  output of the latch turns the switch  $S_s$  off. Current  $G_s v_2(t)$  proportional to the voltage  $v_2(t)$  charges the capacitor  $C_s$ . At  $t = dT_s$ , the capacitor voltage  $v_s(t)$  reaches the control input voltage  $v_c$ , the comparator output goes high and resets the latch. The logic low signal at the  $Q$  output of the latch turns the power MOSFET off. At the same time, the logic high signal at the  $\bar{Q}$  output of the latch turns the switch  $S_s$  on, which quickly discharges the capacitor  $C_s$  to zero.

In this problem, the converter and controller parameters are:  $V_g = 24 \text{ V}$ ,  $f_s = 1/T_s = 100 \text{ kHz}$ ,  $L = 60 \mu\text{H}$ ,  $C = 100 \mu\text{F}$ ,  $R = 3 \Omega$ ,  $G_s T_s / C_s = 1$ . You can assume that the converter operates in the continuous conduction mode.

- (a) Find expressions for the average values of the switch network terminal waveforms, and hence derive a large-signal averaged switch model of the buck switch network with one-cycle control. The control input to the model is the control voltage  $v_c$ . The switch duty cycle  $d$  should not appear in the model.
- (b) Using the averaged switch model derived in part (a), find an expression for the quiescent output voltage  $V$  as a function of  $V_c$ . Given  $V_c = 10 \text{ V}$ , find the numerical values for  $V$ ,  $I_1$ ,  $I_2$ , and the duty cycle  $D$ . For this quiescent operating point, sketch the waveforms  $i_1(t)$ ,  $i_2(t)$ , and  $v_s(t)$  during one switching period.



**Fig. 18.66** Buck converter with one-cycle controller, Problem 18.12

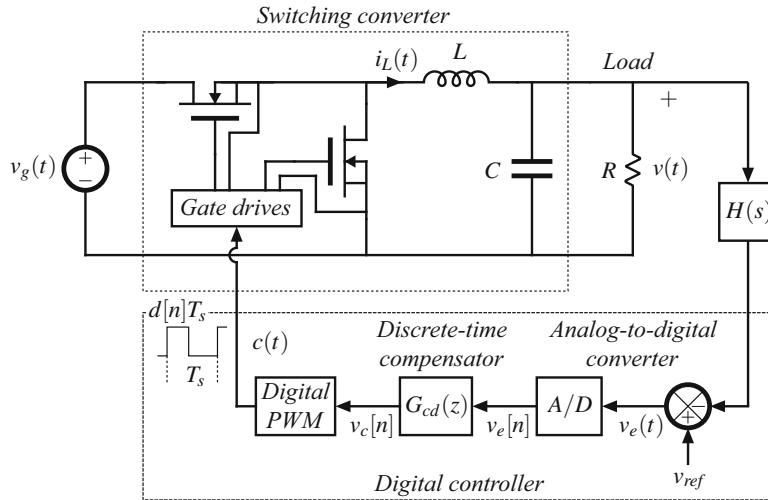
- (c) Perturb and linearize the averaged switch model from part (a) to derive a small-signal averaged switch model for the buck switch network with one-cycle control. Find analytical expressions for all parameter values in terms of the converter parameters and the quiescent operating conditions. Sketch the complete small-signal model of the buck converter with the one-cycle controller.
- (d) Solve the model obtained in part (c) to find the control-to-output transfer function  $G_{vc}(s) = \hat{v}/\hat{v}_c$ , and the line-to-output transfer function  $G_{vg}(s) = \hat{v}/\hat{v}_g$ . For the quiescent operating point found in part (b), sketch the magnitude Bode plots of these transfer functions, and label all salient features.
- (e) Comment on advantages one-cycle control may have compared to duty-cycle control.



## Digital Control of Switched-Mode Power Converters

Digital control methods and digital controllers based on general-purpose or dedicated microcontrollers, digital signal processors (DSP's), or programmable logic devices have been widely adopted in power electronics applications at relatively high-power levels, including motor drives or grid-tied three-phase inverters and rectifiers. In these applications, digital control offers clear technical and economic advantages in addressing complex control, management, and monitoring tasks. Digital control is also applicable to ubiquitous low-to-medium power switched-mode power conversion applications such as point-of-load (POL) regulators, non-isolated and isolated dc–dc converters, single-phase power factor correction (PFC) rectifiers and inverters, etc. In these applications, switching frequencies are typically in the range from hundreds of kilohertz to multiple megahertz, and much faster dynamic responses are required. The controller cost and the controller power consumption can easily present significant portions of the system cost and power dissipation. In many applications, control challenges have been successfully met by continuous advances of readily available analog controllers, using analysis, modeling, and design techniques discussed in other chapters of this book. More recently, practical digital control of high-frequency switched-mode power converters has moved from proof-of-concept laboratory demonstrations [181–189], to digital PWM controller (DPWM) chips commercially available from multiple vendors. A number of mixed-signal DPWM controller architectures and implementation strategies have been investigated and realized in practice. For example, many standard microcontrollers or DSP chips are now available, featuring multiple PWM and analog-to-digital (A/D) conversion channels, allowing software-based control and power management functions. High-performance digital control loops can also be realized using digital logic implemented in field-programmable gate array (FPGA) chips or specialized integrated circuits, together with custom DPWM and A/D blocks, while programmability, power management, and system interface functions are delegated to embedded microcontrollers.

In addition to taking advantage of continuous and rapid advances in digital controller realizations, digital control techniques have opened opportunities for advances in high-frequency switched-mode power conversion applications. Advantages of digital control include programmability of parameters and flexibility in applications. Furthermore, practical realizations of more advanced techniques have been demonstrated, including approaches leading to improved dynamic responses [190–201], system identification [202–205], auto-tuning and adaptive control methods [206–214], as well as efficiency optimization and power management functions [215–222].



**Fig. 19.1** Digitally controlled switched-mode power converter

The purpose of this chapter is to provide an introduction to analysis, modeling, and design of digital control for high-frequency switched-mode power converters. Figure 19.1 shows a digitally controlled converter, using the synchronous buck converter as an example. The objectives are to develop understanding of the operation of the digital PWM control loop, including the effects of delays and quantization, to model the loop dynamics, and to enable the reader to design high-performance digital control loops. It is assumed that the reader has mastery of the materials in the preceding chapters, especially Chaps. 7–9, but no background in discrete-time or digital control is assumed. Signal propagation and functional blocks in the digital control loop are discussed in Sect. 19.1. Section 19.2 presents an introduction to discrete-time systems. Discrete-time compensator design is presented in Sect. 19.3, while Sect. 19.4 gives an introduction to digital controller implementation techniques. A more detailed treatment of the subject of digital control of high-frequency switched-mode power converters can be found in [223].

## 19.1 Digital Control Loop

In the digitally controlled switching converter of Fig. 19.1, the output voltage is measured using a sensor with gain  $H(s)$ . The transfer function  $H(s)$  may include scaling and analog filtering of the output voltage. As in the conventional analog control loop, the sensor output signal is compared with a reference voltage  $v_{ref}$  to obtain the error signal  $v_e(t)$ . The error signal is sampled in time and quantized in amplitude by an analog-to-digital (A/D) converter. The A/D sampling usually occurs at a constant rate, which is called the sampling frequency  $f_{sampling} = 1/T_{sampling}$ . Then the A/D output  $v_e[n]$  is a digital word that represents the analog error signal  $v_e$  at time  $t = nT_{sampling}$ . The A/D sampling frequency is in general synchronized with the switching frequency  $f_s$ ,  $f_{sampling} = kf_s$ , where  $k$  is a positive integer. In practice, a common choice is to select the sampling period to be equal to the switching period:  $k = 1$ ,

$$T_{sampling} = T_s \quad (19.1)$$

Based on the discretized error signals  $v_e[n]$ , the digital compensator  $G_{cd}$  updates the duty-cycle command signal  $v_c[n]$  at the input of the digital pulse-width modulator (DPWM). Finally, given  $v_c[n]$ , the DPWM outputs a switch control signal  $c(t)$  with duty cycle  $d[n]$  proportional to the duty-cycle command  $v_c[n]$ . The digital control loop is conceptually very similar to the standard analog voltage-mode control loop discussed in Sect. 9.1, but with two significant differences due to (1) quantization in amplitude, and (2) sampling, *i.e.*, quantization in time.

### 19.1.1 A/D and DPWM Quantization

In the control loop illustrated in Fig. 19.1, the digital signals  $v_e[n]$  and  $v_c[n]$  are represented by digital variables having a finite number of bits. Practical A/D converters produce digital outputs having a limited number of bits such as 12 or 14. Digital pulse-width modulators similarly are limited in their resolution. This section introduces the quantization characteristics of the A/D converter and of the digital pulse-width modulator.

#### Analog-to-Digital Conversion

In addition to sampling in time, the A/D converter performs quantization in amplitude. Figure 19.2a shows the quantization characteristic  $Q_{A/D}$  of a standard A/D converter operating over an analog input voltage range from 0 to a full-scale voltage  $V_{FS}$ . The sensed analog signal  $Hv$  is quantized to an  $n_{A/D}$ -bit digital word. The least significant bit (LSB) value of this quantized signal is

$$q_{A/D} = \frac{V_{FS}}{2^{n_{A/D}}} \quad (19.2)$$

where  $n_{A/D}$  is the A/D resolution in bits. The example in Fig. 19.2a is shown for  $n_{A/D} = 3$ . The A/D-converted sensed analog signal is digitally subtracted from the reference voltage  $v_{ref}$  to obtain the digital error signal  $v_e[n]$ . As an alternative, the A/D quantization can be viewed as shown in Fig. 19.2b, where the quantization characteristic is centered around zero. Either way, analog voltages within a zero-error bin of width  $q_{A/D}$  produce a zero digital error signal  $v_e[n] = 0$ , which implies that the LSB resolution  $q_{A/D}$  determines how well the output voltage can be regulated by the digital control loop.

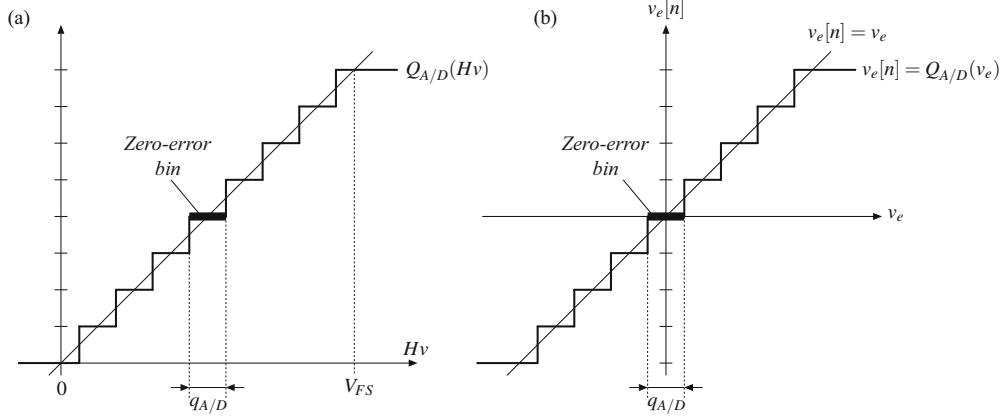
As an example, suppose that  $H = 1$ , and that it is desired to regulate the output dc voltage  $V$  within  $\pm 0.25\%$  of  $V_{ref} = 1$  V, *i.e.*, within  $\pm 2.5$  mV. The LSB resolution must therefore meet the condition  $q_{A/D} < 5$  mV. Equation (19.2) implies that the required A/D resolution in bits is

$$n_{A/D} > \log_2 \left( \frac{V_{FS}}{q_{A/D}} \right) \quad (19.3)$$

Suppose  $V_{FS} = 2$  V, which is a typical full-scale voltage value for standard A/D converters. Then an A/D resolution of at least  $n_{A/D} = 9$  bits is required to meet the dc voltage regulation specification. When the quantization is centered around zero, as shown in Fig. 19.2b, the same LSB resolution can be achieved but the voltage conversion range can be reduced, thus effectively reducing the number of bits required to represent  $v_e[n]$ . Such “window” A/D converters have been described in [181, 182, 184, 193].

#### Digital Pulse-Width Modulation

Digital pulse-width modulation, illustrated in Fig. 19.3a, follows the same principles as the standard analog PWM described in Sect. 7.3, Fig. 7.30. The duty-cycle command signal  $v_c[n]$  is

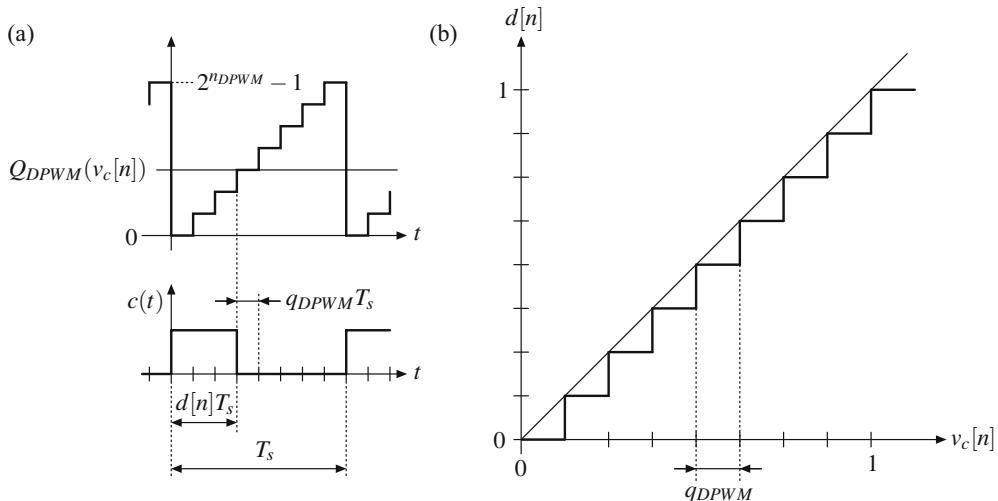


**Fig. 19.2** A/D quantization characteristic over (a)  $0 - V_{FS}$  voltage range, and (b) centered around zero error

compared with a digital saw-tooth ramp, so that the duty cycle  $d[n]$  of the output control signal  $c(t)$  is proportional to  $v_c[n]$ . As shown in Fig. 19.3a, the time resolution of the  $c(t)$  pulse is  $q_{DPWM} T_s$  where

$$q_{DPWM} = \frac{1}{2^{n_{DPWM}}} \quad (19.4)$$

and  $n_{DPWM}$  is the DPWM resolution in bits. In the example shown in Fig. 19.3,  $n_{DPWM} = 3$ .



**Fig. 19.3** Digital pulse-width modulator: (a) time-quantization of the gate-drive signal  $c(t)$  and (b) quantization characteristic

In Fig. 19.3a it is assumed that the amplitude of the digital saw-tooth ramp is  $1 - 2^{-n_{DPWM}}$  which corresponds to the equivalent DPWM gain equal to  $1 \text{ V}^{-1}$ , i.e.,  $V_M = 1 \text{ V}$ . The resulting DPWM quantization characteristic is shown in Fig. 19.3b.

In a standard DPWM implementation, the digital saw-tooth ramp is generated simply by a digital counter driven by a digital clock with frequency  $f_{clk}$ . The DPWM timing resolution is then determined by the clock period  $T_{clk} = 1/f_{clk}$ ,

$$q_{DPWM} T_s = T_{clk} \quad (19.5)$$

The duty-cycle resolution determines how precisely the converter output voltage can be positioned. For example, in a buck converter of Fig. 19.1, the dc output voltage is  $V = DV_g$ . Given the duty-cycle quantization, the output voltage positioning resolution is therefore

$$\Delta V = q_{DPWM} V_g \quad (19.6)$$

or,

$$\frac{\Delta V}{V} = q_{DPWM} \frac{V_g}{V} = \frac{1}{2^{n_{DPWM}}} \frac{1}{M} \quad (19.7)$$

Suppose that it is desired to position the output voltage within 0.1% in a converter with  $M = V/V_g = 0.2$ . Equation (19.7) implies that a 13-bit DPWM is required to meet the voltage positioning specification, while Eq. (19.5) implies that a standard DPWM implementation would require a clock frequency

$$f_{clk} = 2^{n_{DPWM}} f_s = 8192 f_s \quad (19.8)$$

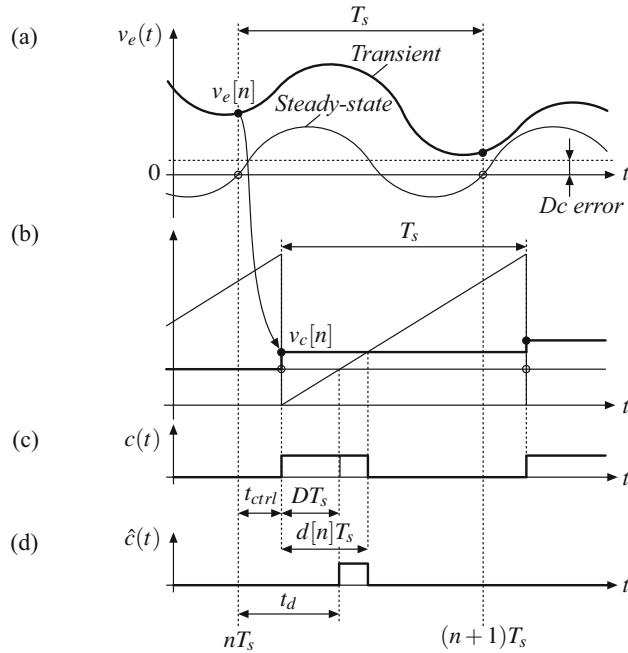
If, for example,  $f_s = 1 \text{ MHz}$ , the required time resolution is 122 ps, and the required clock frequency is  $f_{clk} = 8.192 \text{ GHz}$ . Equation (19.8) illustrates one of the practical challenges in implementation of digital PWM controllers for high-frequency switched-mode power converters: the high switching frequency and the need for high DPWM resolution require high system clock frequency. This problem has been addressed using alternative DPWM implementation techniques, resulting in practical high-frequency, high-resolution DPWM realizations [181, 182, 184, 185, 188, 224–234].

### Ideal Quantization Characteristics

The A/D and the DPWM quantization characteristics are highly nonlinear, which has implications on the stability and operation of the digitally controlled converter. Until we return to the A/D and the DPWM quantization effects in Sect. 19.4.2, we will assume that high-resolution A/D and DPWM units are available so that quantization-induced nonlinearities in the digital control loop can be neglected:

$$\begin{aligned} v_e[n] &= Q_{A/D}(v_e(nT_s)) \approx v_e(nT_s) \\ d[n] &\approx \frac{v_c[n]}{V_M} = \frac{v_c[n]}{1 \text{ V}} \end{aligned} \quad (19.9)$$

For the DPWM, a common assumption is that  $V_M = 1 \text{ V}$ . The ideal (very high resolution) quantization characteristics in Eq. (19.9) imply that the A/D converter and the DPWM blocks can be modeled simply as unity gain blocks,  $v_e[n]/v_e(nT_s) = 1$ ,  $d[n]/v_c[n] = 1 \text{ V}^{-1}$ .



**Fig. 19.4** Operating waveforms in a digitally controlled switched-mode power converter

### 19.1.2 Sampling and Delays in the Control Loop

Figure 19.4 illustrates steady-state and transient operation of a digitally controlled converter where Eq. (19.1) is satisfied, so that the A/D sampling rate equals the switching frequency. Ideally, the digital sample  $v_e[n]$  of the error signal equals the value of the analog error signal  $v_e(t)$  at time  $nT_s$ ,  $v_e[n] = v_e(nT_s)$ . The quantity controlled by the digital feedback loop is the sampled value  $v_e[n]$  of the analog error signal  $v_e(t)$ . Assuming a well-designed feedback loop with very large dc loop gain, the steady-state error is driven to zero, as shown in Fig. 19.4a:

$$v_e[n] \rightarrow 0 \quad (19.10)$$

In equilibrium, the dc value  $V_e$  of the analog error signal may not be equal to zero. The dc regulation error in the digitally controlled loop is a result of the fact that the error signal  $v_e(t)$  includes switching ripple so that the sample  $v_e[n]$  is not necessarily equal to the dc value  $V_e$ . The digitally controlled converter is a sampled-data system. With A/D sampling equal to the switching frequency, the dc error in equilibrium can be interpreted as aliasing of the switching ripple components to dc. The error is no larger than the amplitude of the ripple. A practical implication is that sampling should be performed away from points in time when the sampled

analog signal may include large noise caused by switching transitions, such as immediately after switching events. Aliasing errors can be reduced by including an “anti-aliasing” analog low-pass filter before the A/D converter, or by sampling the analog signal at a rate higher than the switching frequency and performing the anti-aliasing filtering digitally.

More generally, it should be understood that A/D sampling at  $f_s$  aliases any frequency components of the analog signal beyond the Nyquist rate  $f_s/2$  back to frequencies below  $f_s/2$  [235]. Therefore, when we discuss frequency responses of the discrete-time compensator  $G_{cd}$ , we will restrict our attention to frequencies up to the Nyquist frequency  $f_s/2$ .

Let us now consider propagation of the signals through the digital control loop. Since the A/D conversion is not instantaneous, the digital signal  $v_e[n]$  is available to the digital controller after a certain time interval commonly referred to as A/D conversion time. Given the updated  $v_e[n]$ , the discrete-time compensator  $G_{cd}$  computes an update to the digital duty-cycle command signal  $v_c[n]$  at the input of the digital pulse-width modulator (DPWM). Combined, the A/D conversion time plus the time it takes to compute  $v_c[n]$ , equal a controller time delay  $t_{ctrl}$  shown in Fig. 19.4. The duty-cycle command  $v_c[n]$  is held constant through the switching period, as shown in Fig. 19.4b. In response, the digital pulse-width modulator outputs a control pulse  $c(t)$  shown in Fig. 19.4c with duty cycle  $d[n]$ , where  $d[n] = v_c[n]/V_M = v_c[n]$ , assuming  $V_M = 1$  V. The difference  $\hat{c}(t)$  between the modulated and the steady-state pulse at the DPWM output is shown in Fig. 19.4d. Note that the response  $\hat{c}(t)$  occurs with delay  $DT_s$  after the time  $v_c[n]$  is updated, which is a result of the sampling process associated with pulse-width modulation, as discussed in Sect. 15.5.

It is important to note that there are *two* sampling processes in the digital control loop of Fig. 19.1: sampling by the A/D converter and sampling by the pulse-width modulator. The time between the two sampling events represents the delay in the digital control loop,

$$t_d = t_{ctrl} + t_{mod} = t_{ctrl} + DT_s \quad (19.11)$$

The control loop delay in Eq. (19.11) includes two components: the time  $t_{ctrl}$  required to perform A/D conversion and the time required by the digital compensator to compute an update of the signal  $v_c[n]$  at the DPWM inputs, and the modulator delay  $t_{mod} = DT_s$  associated with the trailing-edge digital pulse-width modulator. Other DPWM types, such as leading-edge or dual-edge DPWM offer different modulator delays, as summarized in Table 19.1 [223]. These results are consistent with the analysis presented in [68].

**Table 19.1** Delays in regularly sampled pulse-width modulators

PWM	Modulator delay $t_{mod}$
Trailing-edge	$DT_s$
Leading-edge	$(1 - D)T_s$
Dual-edge	$T_s/2$

In the frequency domain, the effect of the delay  $t_d$  in the digital control loop can be modeled by applying the Laplace transform to a signal delayed by  $t_d$ , as follows:

$$\mathcal{L}\{x(t - t_d)\} = \int_{t \rightarrow -\infty}^{t \rightarrow +\infty} x(t - t_d) e^{-st} dt = \int_{\tau \rightarrow -\infty}^{\tau \rightarrow +\infty} x(\tau) e^{-s(\tau+t_d)} d\tau = e^{-std} x(s) \quad (19.12)$$

It follows that the Laplace-transform frequency-domain model of the delay  $t_d$  is given by

$$G_{\text{delay}}(s) = e^{-std} \quad (19.13)$$

with magnitude response  $\|G_{\text{delay}}(j\omega)\| = 1$ , and phase response given by

$$\angle G_{\text{delay}}(j\omega) = -\omega t_d \quad (19.14)$$

The phase lag of Eq. (19.14) can be significant, and should be taken into account in the design of the discrete-time compensator. This issue is discussed further in Sect. 19.3.

## 19.2 Introduction to Discrete-Time Systems

The purpose of this section is to present a brief introduction to discrete-time system analysis and modeling techniques. The techniques presented in this section enable design of the discrete-time compensator  $G_{cd}(z)$  in the digitally controlled converter of Fig. 19.1.

### 19.2.1 Integration in Continuous Time and in Discrete Time

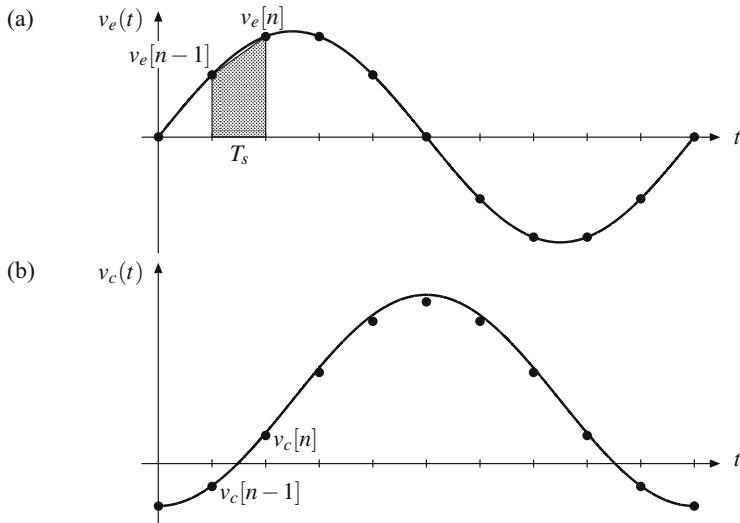
A standard analog control loop around a switching converter is shown in Fig. 7.1. The continuous-time compensator  $G_c(s)$  can be designed based on the frequency-domain techniques discussed in Chap. 9. Consider a simple integral compensator,

$$G_c(s) = \frac{v_c(s)}{v_e(s)} = \frac{\omega_o}{s} \quad (19.15)$$

where  $v_e$  is the error signal and  $v_c$  is the signal applied to the input of the pulse-width modulator. The continuous-time,  $s$ -domain transfer function  $G_c(s)$  has a pole at  $s = 0$ . In the time domain, the output  $v_c(t)$  of the compensator is an integral of the input  $v_e(t)$ ,

$$v_c(t) = v_c(0) + \omega_o \int_0^t v_e(\tau) d\tau \quad (19.16)$$

where  $v_c(0)$  is the initial condition at  $t = 0$ . Figure 19.5 illustrates an example of waveforms  $v_c(t)$  and  $v_e(t)$ . In this example,  $v_e(t)$  is a sinusoidal waveform at frequency  $f_s/10$ , where  $f_s = 1/T_s$  is the sampling frequency. Let us now consider how to realize the integral compensator in the digital controller shown in Fig. 19.1, *i.e.*, how to compute the samples  $v_c[n]$  at the discrete-time compensator output given the discrete-time samples  $v_e[n] = v_e(nT_s)$  at the compensator input. First, note that the continuous-time integration in Eq. (19.16) can be written as:



**Fig. 19.5** Continuous-time and discrete-time integration

$$v_c(t) = v_c(t - T_s) + \omega_o \int_{t-T_s}^t v_e(\tau) d\tau. \quad (19.17)$$

To reproduce Eq. (19.17) exactly, the discrete-time compensator should perform the following calculation:

$$v_c(nT_s) = v_c[n] = v_c[n-1] + \omega_o \int_{(n-1)T_s}^{nT_s} v_e(\tau) d\tau \quad (19.18)$$

where the integral over the interval  $(n-1)T_s$  to  $nT_s$  represents the area under the waveform  $v_e(t)$  over the sampling interval  $T_s$  between  $t = (n-1)T_s$  and  $t = nT_s$ . However, since values of  $v_e(t)$  are only available at discrete-times, the exact reproduction of the continuous-time integration in Eq. (19.18) is not feasible. Instead, one must perform the integration approximately, using only the available discrete-time samples of  $v_e$ . One approach, based on a trapezoidal approximation to the area under the waveform  $v_e$  over a sampling period  $T_s$ , is illustrated in Fig. 19.5:

$$v_c[n] = v_c[n-1] + \omega_o T_s \frac{v_e[n] + v_e[n-1]}{2} \quad (19.19)$$

The computation of  $v_c[n]$  in Eq. (19.19) is relatively simple, requiring only an addition of  $v_e[n-1]$  and  $v_e[n]$ , a multiplication by a constant, and an addition of the product and the previously computed  $v_c[n-1]$ . It is clear that Eq. (19.19) can easily be implemented in digital logic hardware or as simple lines of code in software. Figure 19.5 shows how the samples  $v_c[n]$  obtained by the approximate discrete-time integration in Eq. (19.19) are close to, but not exactly equal to the samples  $v_c(nT_s)$  of the analog integrator output signal  $v_c(t)$ . For a given  $v_e(t)$ , increase of the sampling frequency causes the differences between the samples  $v_c(nT_s)$  of the analog, continuous-time integration in Eq. (19.17) and the discrete-time integrator outputs  $v_c[n]$  in Eq. (19.19) to diminish.

The trapezoidal approximation leading to Eq. (19.19) is not the only possible way to approximate continuous-time integration in discrete-time. The backward Euler approximation is given by:

$$v_c[n] = v_c[n - 1] + \omega_o T_s v_e[n - 1] \quad (19.20)$$

The forward Euler approximation is

$$v_c[n] = v_c[n - 1] + \omega_o T_s v_e[n]. \quad (19.21)$$

All three approximations find application; generally the trapezoidal approximation is more accurate.

### 19.2.2 *z*-Transform and Frequency Responses of Discrete-Time Systems

Equations (19.19), (19.20), and (19.21) define three discrete-time integral compensators in the time domain. In the previous chapters, we have extensively relied on the continuous-time Laplace transform, *s*-domain transfer functions, as well as on frequency responses and frequency-domain analysis, modeling and design techniques. It is of interest to introduce the corresponding transforms and frequency-domain techniques developed for discrete-time systems [176]. The introduction here is intended to be very brief and at a basic level, but sufficient to enable the reader to undertake digital controller designs based on the standard analog, continuous-time background provided in the previous chapters.

In discrete-time systems, the *Z*-transform plays the role the Laplace transform has in continuous-time circuits and systems. Given a discrete-time signal  $x[n]$ , the *Z*-transform is defined as

$$\mathcal{Z}\{x[n]\} = x(z) = \sum_{n=-\infty}^{n \rightarrow +\infty} x[n]z^{-n} \quad (19.22)$$

Just like the Laplace transform, the *Z*-transform is linear:

$$\mathcal{Z}\{ax[n] + by[n]\} = a\mathcal{Z}\{x[n]\} + b\mathcal{Z}\{y[n]\} = ax(z) + by(z) \quad (19.23)$$

where  $a$  and  $b$  are constants. For a variable delayed by one sampling period, the *Z*-transform can be found as follows:

$$\mathcal{Z}\{x[n - 1]\} = \sum_{n=-\infty}^{n \rightarrow +\infty} x[n - 1]z^{-n} = \sum_{k=-\infty}^{k \rightarrow +\infty} x[k]z^{-(k+1)} = z^{-1} \sum_{k=-\infty}^{k \rightarrow +\infty} x[k]z^{-k} = z^{-1}x(z) \quad (19.24)$$

It follows that delaying a discrete-time signal by a sampling period in time domain is equivalent to multiplying the *Z*-transform of the signal by a factor  $z^{-1}$ . In other words,  $z^{-1}$  models a unit delay in the *z*-domain.

Application of the *Z*-transform, including Eq. (19.24), to the discrete-time integrator Eq. (19.19), yields

$$v_c(z) = z^{-1}v_c(z) + \omega_o T_s \frac{v_e(z) + z^{-1}v_e(z)}{2} \quad (19.25)$$

**Table 19.2** Transfer functions of discrete-time integrators

Approximation	$G_{cd}(z)$
Trapezoidal	$\frac{\omega_o T_s}{2} \frac{z+1}{z-1}$
Backward Euler	$\omega_o T_s \frac{1}{z-1}$
Forward Euler	$\omega_o T_s \frac{z}{z-1}$

which leads to the discrete-time,  $z$ -domain transfer function of the discrete-time integral compensator of Eq. (19.19), derived using the trapezoidal approximation in Sect. 19.2.1:

$$G_{cd}(z) = \frac{v_c(z)}{v_e(z)} = \frac{\omega_o T_s}{2} \frac{1+z^{-1}}{1-z^{-1}} = \frac{\omega_o T_s}{2} \frac{z+1}{z-1} \quad (19.26)$$

Table 19.2 shows the discrete-time  $z$ -domain transfer functions for the three considered discrete-time integrators.

For continuous-time  $s$ -domain transfer functions, such as the continuous-time integral compensator  $G_c(s)$  in Eq. (19.15), we know that the response to a sinusoidal perturbation at frequency  $\omega$  can be found by replacing  $s$  with  $j\omega$ , and evaluating the magnitude and phase of  $G_c(j\omega)$ . In particular, as discussed in Sect. 8.1 and shown in Fig. 8.3, the Bode plot of the integral compensator magnitude response is a straight line with  $-20$  dB/decade slope. What can be said about the frequency responses of  $G_{cd}(z)$ ? To answer this question, recall that  $z^{-1}$  models a unit delay in the  $z$ -domain. On the other hand, similar to the approach taken to model a delay in Eq. (19.12), applying the Laplace transform to a signal  $x(t)$  delayed by a sampling period  $T_s$  results in

$$\mathcal{L}\{x(t-T_s)\} = \int_{t \rightarrow -\infty}^{t \rightarrow +\infty} x(t-T_s)e^{-st} dt = \int_{\tau \rightarrow -\infty}^{\tau \rightarrow +\infty} x(\tau)e^{-s(\tau+T_s)} d\tau = e^{-sT_s}x(s) \quad (19.27)$$

By comparing Eq. (19.24) and Eq. (19.27), we conclude that the frequency response of a  $z$ -domain transfer function can be found by replacing  $z^{-1}$  with  $e^{-sT_s}$ , and then  $s$  with  $j\omega$ , as in the case of continuous-time  $s$ -domain transfer functions:

$$G_{cd}(j\omega) = G_{cd}(z)|_{z \rightarrow e^{j\omega T_s}} \quad (19.28)$$

Let us evaluate the frequency response of the discrete-time integral compensator in Eq. (19.26):

$$G_{cd}(j\omega) = \frac{\omega_o T_s}{2} \frac{1 + e^{-j\omega T_s}}{1 - e^{-j\omega T_s}} = \frac{\omega_o T_s}{2} \frac{e^{j\omega T_s/2} + e^{-j\omega T_s/2}}{e^{j\omega T_s/2} - e^{-j\omega T_s/2}} \quad (19.29)$$

Application of Euler's formula ( $e^{jx} = \cos x + j \sin x$ ) to Eq. (19.29) leads to

$$G_{cd}(j\omega) = -j \frac{\omega_o T_s}{2} \frac{\cos\left(\frac{\omega T_s}{2}\right)}{\sin\left(\frac{\omega T_s}{2}\right)} \quad (19.30)$$

It is of interest to compare the frequency responses of  $G_{cd}(j\omega)$  in Eq. (19.30) with the frequency response  $G_c(j\omega)$  of the original continuous-time integral compensator in (19.15),

$$G_c(j\omega) = -j \frac{\omega_o}{\omega} \quad (19.31)$$

The phase responses of  $G_{cd}(j\omega)$  in Eq. (19.30) and  $G_c(j\omega)$  in Eq. (19.31) are exactly the same at all frequencies. Both transfer functions exhibit  $-90^\circ$  phase at all frequencies. It should be noted that this is the case only for the discrete-time integrator based on the trapezoidal approximation. In contrast, the phase responses of the discrete-time integrator based on the forward Euler or the backward Euler approximations differ from the phase response of the continuous-time integrator.

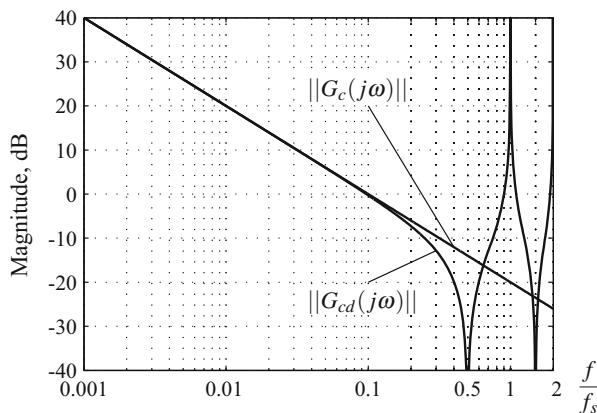
To compare the magnitude responses, consider first low frequencies such that  $(\omega T_s/2) \ll 1$ , i.e.,  $f \ll f_s/\pi$ ,

$$G_{cd}(j\omega) \Big|_{(\omega T_s/2) \ll 1} \approx -j \left( \frac{\omega_o T_s}{2} \right) \frac{1}{\left( \frac{\omega T_s}{2} \right)} = -j \frac{\omega_o}{\omega} = G_c(j\omega) \quad (19.32)$$

Equation (19.32) shows that the magnitude response of the discrete-time integrator approximates very well the magnitude response of the continuous-time integrator at frequencies sufficiently low compared to the sampling frequency ( $f \ll f_s/\pi$ ). At higher frequencies, however, the differences in magnitude responses increase. The mismatch in magnitude responses is visible in Fig. 19.5. In this example,  $f = f_s/10$ , and the mismatches between  $v_c[n]$  and the values  $v_c(nT_s)$  obtained at the output of the continuous-time integrator are relatively small, but visible. Furthermore, while  $\|G_c(j\omega)\| > 0$  at all frequencies,  $\|G_{cd}(j\omega)\| = 0$  at frequencies such that  $\omega T_s/2 = (2k + 1)\pi/2$ :

$$\|G_{cd}(j\omega)\| = 0, \text{ for } f = \frac{f_s}{2}, \frac{3f_s}{2}, \dots \quad (19.33)$$

The magnitude responses of  $G_c(s)$  and  $G_{cd}(z)$  are compared in Fig. 19.6 for  $f_s = 1$  MHz and  $f_o = 100$  kHz. The responses match closely at low frequencies, and depart more significantly at frequencies approaching  $f_s/2$  and beyond.



**Fig. 19.6** Magnitude responses of the continuous-time and discrete-time integrators,  $f_s = 1$  MHz,  $f_o = 100$  kHz. The discrete-time integrator is based on the trapezoidal approximation

### 19.2.3 Continuous Time to Discrete Time Mapping

Sections 19.2.1 and 19.2.2 introduced discrete-time systems using a simple integral compensator example. The objective of this section is to derive discrete-time compensator transfer functions  $G_{cd}(z)$  starting from more complex continuous-time compensator transfer functions  $G_c(s)$ , such as PI, PD and PID compensators discussed in Chap. 9. There are many different continuous-time to discrete-time mapping approaches, *i.e.*, approaches to finding  $G_{cd}(z)$  starting from an  $s$ -domain transfer function  $G_c(s)$  [176]. Here we describe a mapping approach that follows directly from the derivation of the discrete-time integrator in Sects. 19.2.1 and 19.2.2 using the trapezoidal approximation:

$$G_c(s) = \frac{\omega_o}{s} \rightarrow G_{cd}(z) = \frac{\omega_o T_s}{2} \frac{z+1}{z-1} \quad (19.34)$$

Equation (19.34) suggests that starting from an arbitrary  $G_c(s)$ ,  $G_{cd}(z)$  can be obtained by replacing  $s$  as follows:

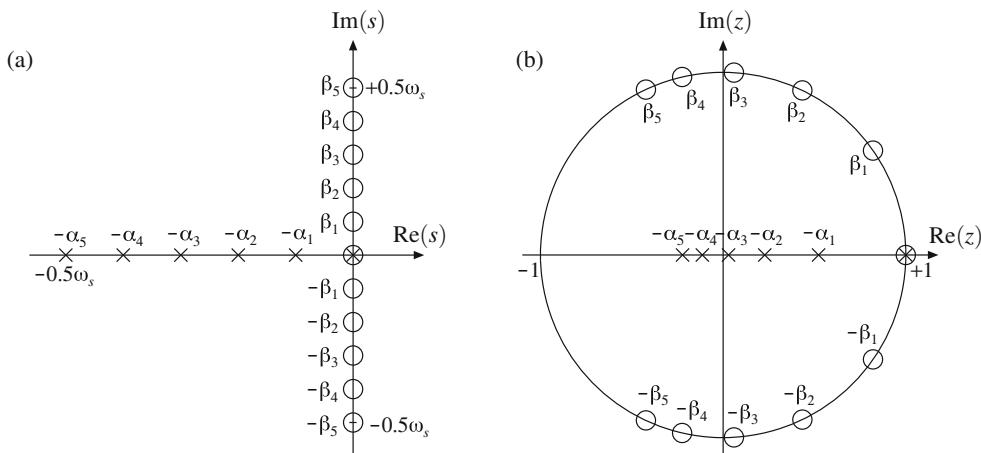
$$s \rightarrow \frac{2}{T_s} \frac{z-1}{z+1} \quad (19.35)$$

By use of Eq. (19.35),  $G_{cd}(z)$  can be found as:

$$G_{cd}(z) = G_c(s) \Big|_{s \rightarrow \frac{2}{T_s} \frac{z-1}{z+1}} \quad (19.36)$$

The mapping defined by Eqs. (19.35) and (19.36) is known as the bilinear or Tustin mapping [176]. Figure 19.7 illustrates several properties of the bilinear mapping. In this example, an  $s$ -domain transfer function contains several real poles at  $s = 0, -\alpha_1, \dots, -\alpha_5$  and several zeroes at  $s = 0, j\beta_1, -j\beta_1, \dots, -j\beta_5$ . The mapping of these poles and zeroes into the  $z$ -plane is found by solving for  $z$  in terms of  $s$  from Eq. (19.35):

$$z = \frac{1 + \frac{sT_s}{2}}{1 - \frac{sT_s}{2}} \quad (19.37)$$



**Fig. 19.7** Mapping from  $s$ -plane (a) to  $z$ -plane (b) using the bilinear method

The origin  $s = 0$  in the  $s$ -plane maps to  $z = 1$  in the  $z$ -plane. Recall that a continuous-time integrator has a pole at  $s = 0$ . Hence, a discrete-time integrator has a pole at  $z = +1$ . As shown in Table 19.2, this is true for all discrete-time integrators. From Eq. (19.37), it can be shown that points  $s = j\omega$  on the  $s$ -plane imaginary axis map to points on the unit circle  $\|z\| = 1$  in the  $z$ -plane. Points on the negative real axis in the  $s$  plane map to points on the real axis in the  $z$ -plane between  $z = +1$  and  $z = -1$ . The entire left half-plane in the  $s$ -plane maps to the interior of the unit circle in the  $z$ -plane.

As an example, consider mapping the PI compensator described in Sect. 9.5.2,

$$G_c(s) = G_{c\infty} \left( 1 + \frac{\omega_L}{s} \right) \quad (19.38)$$

First, we employ the bilinear mapping, Eq. (19.36), to express the compensator transfer function  $G_{cd}(z)$  as a function of  $z$ :

$$G_{cd}(z) = G_{c\infty} \left( 1 + \frac{\omega_L}{\left( \frac{2}{T_2} \frac{z-1}{z+1} \right)} \right) \quad (19.39)$$

With some algebra, this can be expressed in pole-zero form as

$$G_{cd}(z) = G_{c\infty} \left( 1 + \frac{\omega_L T_s}{2} \right) \frac{z - \frac{1 - \omega_L T_s / 2}{1 + \omega_L T_s / 2}}{z - 1} \quad (19.40)$$

Since  $f_L$  in PI compensators is usually very low compared to  $f_s$ ,  $(\omega_L T_s / 2) \ll 1$ , Eq. (19.40) can be simplified as follows:

$$G_{cd}(z) \approx G_{c\infty} \frac{z - (1 - \omega_L T_s)}{z - 1} \quad (19.41)$$

The discrete-time PI compensator has a pole at  $z = 1$ , and a real zero at approximately  $1 - \omega_L T_s$ . For a given sampling frequency  $f_s = 1/T_s$ , as  $\omega_L$  approaches zero, the discrete-time zero tends to  $z = 1$ . In general, mapping continuous-time low-frequency poles or zeroes results in discrete-time poles or zeroes close to the  $+1$  point of the  $z$ -plane. This can lead to roundoff errors and design constraints in implementation of discrete-time compensators, discussed further in Sect. 19.4.

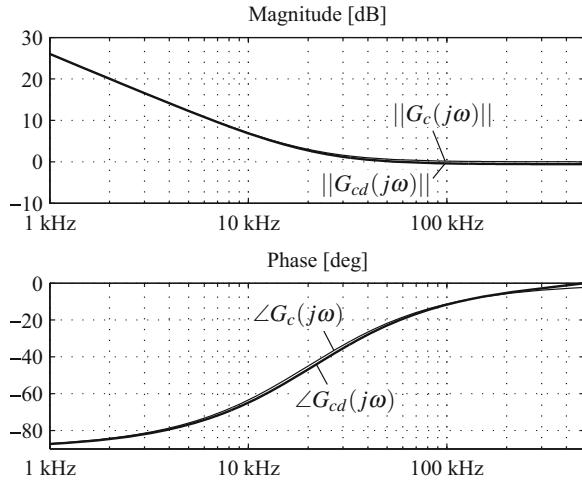
Figure 19.8 compares the magnitude and phase responses of the analog PI compensator  $G_c(s)$  in Eq. (19.38), with  $G_{c\infty} = 1$ ,  $f_L = 20$  kHz, and the discrete-time PI compensator in Eq. (19.40) obtained by bilinear mapping with  $f_s = 1$  MHz,

$$G_{cd}(z) = 1.063 \frac{z - 0.8743}{z - 1} \quad (19.42)$$

One may observe that the magnitude and phase responses match very well over frequencies well below the sampling rate  $f_s$ . The responses in Fig. 19.8 are plotted up to the Nyquist frequency  $f_s/2 = 500$  kHz.

As another example, consider mapping a PD compensator described in Sect. 9.5.1,

$$G_c(s) = G_{c0} \frac{\left( 1 + \frac{s}{\omega_z} \right)}{\left( 1 + \frac{s}{\omega_p} \right)} \quad (19.43)$$



**Fig. 19.8** Magnitude and phase responses of an analog, continuous-time PI compensator  $G_c(s)$ ,  $G_{c\infty} = 1$ ,  $f_L = 20$  kHz, and the discrete-time compensator  $G_{cd}(z)$  obtained by bilinear mapping,  $f_s = 1$  MHz

The bilinear mapping, Eq. (19.36), results in

$$G_{cd}(z) = G_{c0} \left( \frac{1 + \frac{2}{\omega_z T_s}}{1 + \frac{2}{\omega_p T_s}} \right) \frac{\left( z - \frac{1 - \omega_z T_s/2}{1 + \omega_z T_s/2} \right)}{\left( z - \frac{1 - \omega_p T_s/2}{1 + \omega_p T_s/2} \right)} \quad (19.44)$$

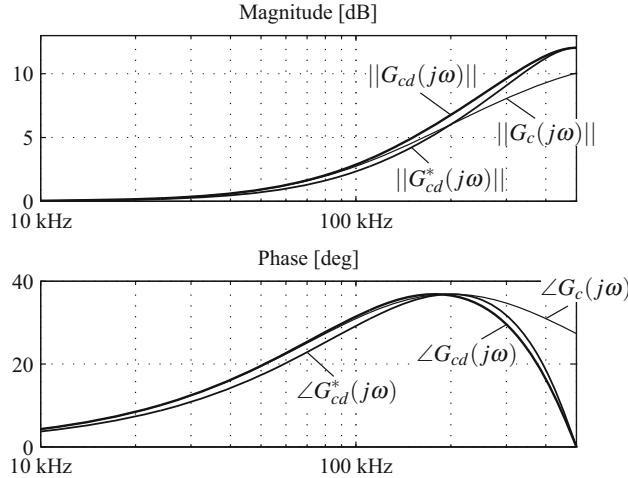
The discrete-time PD compensator has a zero and a pole on the real  $z$ -plane axis. Suppose that  $f_s = 1$  MHz and that it is desired to implement digitally a PD compensator with  $G_{c0} = 1$ ,  $f_z = 100$  kHz,  $f_p = 400$  kHz. Note that in this case the continuous-time zero and pole frequencies are not much lower than the sampling frequency  $f_s$ . By substituting the numerical values in Eq. (19.40), we get

$$G_{cd}(z) = 2.329 \frac{z - 0.5219}{z + 0.1137} \quad (19.45)$$

The frequency responses of  $G_c(s)$  and  $G_{cd}(z)$  are compared in Fig. 19.9. Since the PD compensator corner frequencies are relatively high, discrepancies can be observed in both magnitude and phase responses, especially at frequencies approaching  $f_s/2$ . After reaching a maximum phase lead at  $\sqrt{f_z f_p} = 200$  kHz, the phase of  $G_{cd}$  drops much faster with frequency than the phase of  $G_c$ . The magnitude of  $G_{cd}$  is larger than the magnitude of  $G_c$  at all frequencies of interest, and the difference in magnitude responses increases with frequency.

A generalization of the bilinear (Tustin) mapping known as frequency prewarping [176] can be applied to mitigate, to some extent, the differences between  $G_c$  and  $G_{cd}$  frequency responses in cases when corner frequencies of interest are relatively close to  $f_s/2$ . The bilinear mapping with prewarp is performed as follows:

$$s \rightarrow k_{\text{prewarp}} \frac{2}{T_s} \frac{z - 1}{z + 1}. \quad (19.46)$$



**Fig. 19.9** Magnitude and phase responses of an analog, continuous-time PD compensator  $G_c(s)$ ,  $G_{c0} = 1$ ,  $f_z = 100$  kHz,  $f_p = 400$  kHz, the discrete-time compensator  $G_{cd}(z)$  obtained by bilinear mapping,  $f_s = 1$  MHz, and the discrete-time compensator  $G_{cd}^*(z)$  obtained by bilinear mapping with prewarping at  $f_{\text{prewarp}} = 200$  kHz

$$G_{cd}^*(z) = G_c(s)|_{s \rightarrow k_{\text{prewarp}} \frac{2}{T_s} \frac{z-1}{z+1}} \quad (19.47)$$

where

$$k_{\text{prewarp}} = \frac{\omega_{\text{prewarp}} T_s / 2}{\tan(\omega_{\text{prewarp}} T_s / 2)} \quad (19.48)$$

is found so that the magnitude and the phase of  $G_c$  and  $G_{cd}^*$  match exactly at a particular frequency  $\omega_{\text{prewarp}}$ ,

$$\begin{aligned} \|G_{cd}^*(j\omega_{\text{prewarp}})\| &= \|G_c(j\omega_{\text{prewarp}})\| \\ \angle G_{cd}^*(j\omega_{\text{prewarp}}) &= \angle G_c(j\omega_{\text{prewarp}}) \end{aligned} \quad (19.49)$$

Figure 19.9 shows the frequency responses of the discrete-time compensator  $G_{cd}^*$  obtained by bilinear mapping with the prewarp frequency  $f_{\text{prewarp}} = \sqrt{f_z f_p} = 200$  kHz. The exact match between  $G_{cd}^*$  and  $G_c$  at the prewarp frequency, and the improved match around the prewarp frequency, are obtained at the expense of somewhat increased mismatch at lower frequencies.

As a final example in this section, consider mapping the continuous-time PID compensator described in Sect. 9.5.3. The compensator transfer function is

$$G_c(s) = G_{cm} \frac{\left(1 + \frac{\omega_L}{s}\right) \left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)} \quad (19.50)$$

Compared to the transfer function in Eq. (9.64), the second pole at  $f_{p2}$  has been dropped from the transfer function in Eq. (19.50). In a practical analog controller implementation, the high-frequency pole at  $f_{p2}$  must be present to cause the gain to roll off at high frequencies and to

prevent the switching ripple from disrupting the operation of the analog pulse-width modulator. Furthermore, the high-frequency pole is unavoidable due to analog circuit implementation limitations, such as the op amp gain-bandwidth product. In the digital controller realization of Fig. 19.1, the sensed analog voltage is sampled by the A/D converter at the rate equal to the switching frequency. As a result, the switching ripple components are not present in the digital compensator, and there is no reason to map the high-frequency pole at  $f_{p2}$  to discrete-time. Instead, the high-frequency (anti-aliasing) filtering can be left in the sensing transfer function  $H(s)$  in the analog domain, where it serves the purpose of attenuating switching ripples and noise before A/D conversion. Using Eq. (19.47), the z-domain, discrete-time transfer function of the PID compensator is obtained,

$$G_{cd}^*(z) = G_d \frac{(z - z_L)(z - z_z)}{(z - 1)(z - z_p)} \quad (19.51)$$

where

$$G_d = G_{cm} \frac{f_{p1}}{f_z} \frac{\left(1 + a \frac{f_L}{f_{\text{prewarp}}}\right) \left(1 + a \frac{f_z}{f_{\text{prewarp}}}\right)}{1 + a \frac{f_{p1}}{f_{\text{prewarp}}}} \quad (19.52)$$

$$z_L = \frac{1 - a \frac{f_L}{f_{\text{prewarp}}}}{1 + a \frac{f_L}{f_{\text{prewarp}}}}, \quad z_z = \frac{1 - a \frac{f_z}{f_{\text{prewarp}}}}{1 + a \frac{f_z}{f_{\text{prewarp}}}}, \quad z_p = \frac{1 - a \frac{f_{p1}}{f_{\text{prewarp}}}}{1 + a \frac{f_{p1}}{f_{\text{prewarp}}}} \quad (19.53)$$

$$a = \tan\left(\pi \frac{f_{\text{prewarp}}}{f_s}\right) \quad (19.54)$$

The mapping techniques discussed in this section, and many others, are well supported by computer tools such as MATLAB [236]. Table 19.3 summarizes the bilinear mapping (Eqs. 19.35, 19.36) and the bilinear mapping with prewarp (Eqs. 19.46–19.48), together with the corresponding MATLAB functions.

**Table 19.3** Continuous-time to discrete-time mapping

Method	mapping	MATLAB function
Bilinear (Tustin)	$s \rightarrow \frac{2}{T_s} \frac{z - 1}{z + 1}$	Gcd = c2d(Gc,Ts,'tustin')
Bilinear (Tustin) with prewarp	$s \rightarrow k_{\text{prewarp}} \frac{2}{T_s} \frac{z - 1}{z + 1}$	Gcd = c2d(Gc,Ts,'prewarp',wprewarp)

### 19.3 Discrete-Time Compensator Design

The loop gain  $T_d$  in a digitally controlled converter includes the sensor transfer function  $H(s)$ , the control-to-output transfer function  $G_{vd}(s)$ , the delay modeled as  $G_{delay}(s) = e^{-st_d}$ , and the compensator transfer function  $G_{cd}(z)$  (or  $G_{cd}^*(z)$ ). It should be noted that the loop gain does not include a zero-order-hold. The magnitude and phase responses of the loop gain  $T_d$  can be found as

$$T_d(j\omega) = \left( H(s) G_{vd}(s) e^{-st_d} \right) \Big|_{s \rightarrow j\omega} G_{cd}^*(z) \Big|_{z \rightarrow e^{j\omega T_s}} \quad (19.55)$$

Compared to the loop gain in an analog voltage-mode controlled converter, Eq. (9.4) with  $V_M = 1$ , Eq. (19.55) differs in two ways: the presence of the delay, and the sampled-data discrete-time nature of the compensator  $G_{cd}$ . These differences are illustrated in the following example.

#### Example

The objective of this example is to evaluate the loop gain frequency response in Eq. (19.55) and to compare it to the loop gain response with an analog controller. An analog PID compensator is designed for a synchronous buck converter operating at  $f_s = 1$  MHz switching frequency. The analog compensator transfer function given in Eq. (9.64), with  $f_L = 8$  kHz,  $f_z = 33$  kHz,  $G_{cm} = 5.45$ ,  $f_{p1} = 300$  kHz,  $f_{p2} = 1$  MHz, results in the crossover frequency  $f_c = 100$  kHz with  $52^\circ$  phase margin. In equilibrium,  $V = V_{ref} = 1.8$  V, so that  $D \approx V/V_g = 0.36$ .

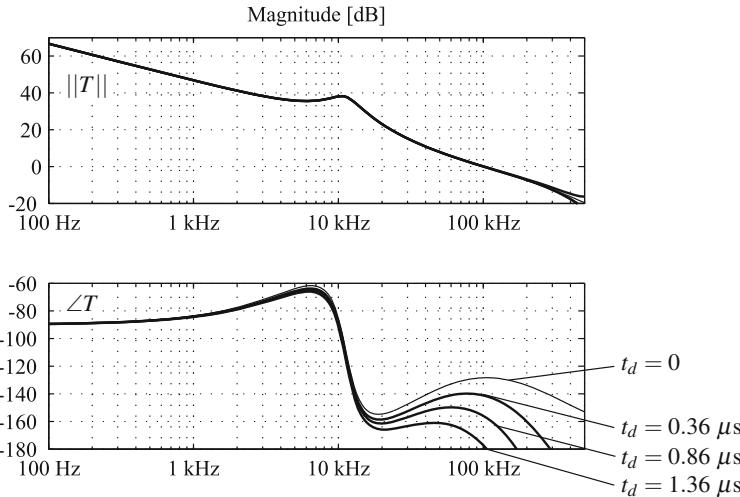
Before mapping the analog compensator to discrete-time, the high-frequency pole at  $f_{p2}$  is removed from the analog compensator transfer function. This pole is instead allocated to an analog anti-aliasing filter in voltage sensing before the A/D converter,

$$H(s) = \frac{1}{1 + \frac{s}{\omega_{p2}}} \quad (19.56)$$

Based on  $G_c(s)$  of Eq. (19.50), with the use of bilinear mapping with the prewarp frequency equal to the target crossover frequency, a discrete-time compensator of Eq. (19.51) is obtained from Eqs. (19.52)–(19.54):

$$G_{cd}^*(z) = 27.3898 \frac{(z - 0.9493)(z - 0.8063)}{(z - 1)(z - 0.01278)} \quad (19.57)$$

The magnitude and phase responses of the loop gain  $T_d$ , evaluated from Eq. (19.55), are shown in Fig. 19.10 for several values of the loop delay  $t_d$ , in comparison to the loop gain responses in the analog controlled converter ( $t_d = 0$ ). The bilinear mapping with prewarp frequency equal to the crossover frequency preserves the magnitude response very well. Furthermore, the delay term does not affect the magnitude responses at all. As a result, the magnitude responses in the digital control loop stay essentially the same as the loop gain magnitude response with the analog controller, and the crossover frequency remains the same,  $f_c \approx 100$  kHz. However, the digital control loop delay more significantly affects the phase responses and the resulting phase margins. The shortest considered delay  $t_d = DT_s = 0.36 \mu s$  assumes a high-performance digital controller where the A/D conversion and the compensator computations are completed very quickly so that  $t_{ctrl} \approx 0$ . From Eq. (19.14), the additional phase lag at the crossover frequency is  $-\omega_c t_d = -13^\circ$ , which reduces the phase margin to  $52^\circ - 13^\circ = 39^\circ$ . A delay of  $t_d = DT_s + T_s/2 = 0.86 \mu s$ , which corresponds to  $t_{ctrl} = T_s/2 = 0.5 \mu s$ , reduces the phase margin to  $52^\circ - 31^\circ = 21^\circ$ . The final case is when the A/D conversion and the compensator calculations take an entire switching period,  $t_{ctrl} = T_s$ , which is representative of a very low-performance digital



**Fig. 19.10** Loop gain magnitude and phase responses in the synchronous buck converter design example with the analog controller ( $t_d = 0$ ), and with digital controllers with several loop delays,  $t_d = DT_s = 0.36 \mu s$ ,  $t_d = DT_s + 0.5T_s = 0.86 \mu s$ ,  $t_d = DT_s + T_s = 1.36 \mu s$

implementation. In this case, the delay of  $t_d = DT_s + T_s = 1.36 \mu s$  reduces the phase margin to just  $52^\circ - 49^\circ = 3^\circ$ . The example illustrates that the loop delay can be a very significant factor in the design of high-performance, wide-bandwidth digital control loops for high-frequency switching power converters.

### 19.3.1 Design Procedure

A basic discrete-time compensator design procedure is described in this section based on the description of the digital control loop and loop delay in Sect. 19.1, the analog regulator design of Sect. 9.5, and the continuous-time to discrete-time mapping techniques of Sect. 19.2.3. The approach consists of four steps:

1. Find the system uncompensated loop gain  $T_{ud}(s)$ , including the anticipated delay  $t_d$  due to digital implementation, as discussed in Sect. 19.1, and anti-aliasing analog filtering in  $H(s)$ :
$$T_{ud}(s) = H(s)G_{vd}(s)G_{delay}(s) = H(s)G_{vd}(s)e^{-st_d} \quad (19.58)$$
2. Design an analog continuous-time compensator  $G_c(s)$  using techniques discussed in Sect. 9.5, except that high-frequency analog roll-off poles should not be included in  $G_c(s)$ . As explained further in the next section, in a PID compensator design, one may choose to position the high-frequency pole at  $f_{p1}$  according to Eq. (19.68) so that the resulting discrete-time compensator has the standard PID form of Eq. (19.69).
3. Map the analog compensator  $G_c(s)$  designed in Step 2 to the discrete-time compensator  $G_{cd}(z)$  using the bilinear mapping, or to the discrete-time compensator  $G_{cd}^*(s)$  using the bilinear mapping with prewarp, as discussed in Sect. 19.2.3. The crossover frequency  $f_c$  and

the phase margin designed in Step 2 can be preserved by choosing the prewarp frequency  $f_{\text{prewarp}}$  equal to the target crossover frequency  $f_c$ ,

$$f_{\text{prewarp}} = f_c \quad (19.59)$$

4. Evaluate magnitude and phase responses of the loop gain  $T_d$  using Eq. (19.55), and verify that the design targets are met. Furthermore, closed-loop frequency responses can be evaluated as in Eqs. (9.4), but with  $T_d$  from Eq. (19.55) replacing the continuous-time loop gain  $T$ .
5. Realize the discrete-time compensator as described in Sect. 19.4.

The digital compensator design approach described in this section is based on continuous-time small-signal averaged converter models, standard analog design techniques, and mapping from continuous time to discrete time. It should be noted that Eq. (19.58) is an approximation based on standard averaging techniques. Exact converter discrete-time converter models [237] allow applications of more advanced design techniques directly in  $z$ -domain [176]. These techniques are described in more detail in [223].

### 19.3.2 Design Example

The objective is to design a discrete-time digital compensator  $G_{cd}$  around the synchronous buck converter shown in Fig. 19.1. The input dc voltage is  $V_g = 5$  V, and the objective is to precisely regulate the output voltage to  $V = V_{ref} = 1.8$  V. The inductance is  $L = 1 \mu\text{H}$ , with a series resistance  $R_s = 30 \text{ m}\Omega$  that models a combination of MOSFET on-resistance and the inductor winding resistance. The output filter capacitor has  $C = 200 \mu\text{F}$  and an equivalent series resistance  $R_{esr} = 0.8 \text{ m}\Omega$ . The converter operates at  $f_s = 1 \text{ MHz}$  switching frequency, and the load current is between 0 A and 5 A. When the converter is unloaded ( $R$  is very large), the converter control-to-output transfer function is

$$G_{vd}(s) = G_{d0} \frac{1 + \frac{s}{\omega_{esr}}}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \quad (19.60)$$

where  $G_{d0} = V_g = 5$  V,  $f_{esr} = 1/(2\pi R_{esr} C) = 1 \text{ MHz}$ ,  $f_0 \approx 1/(2\pi\sqrt{LC}) = 11.3 \text{ kHz}$  and  $Q \approx \sqrt{L/C}/(R_s + R_{esr}) = 2.3$ .

Let us first design an analog PID compensator to achieve a crossover frequency  $f = 100 \text{ kHz}$  with a phase margin of  $52^\circ$ . Assuming  $H = 1$ , and  $V_M = 1 \text{ V}$ , following the design approach exemplified in Sect. 9.5.4, we arrive at the analog PID compensator

$$G_c(s) = G_{cm} \frac{\left(1 + \frac{\omega_L}{s}\right)\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \quad (19.61)$$

where  $G_{cm} = 5.45$ ,  $f_L = 8 \text{ kHz}$ ,  $f_z = 33 \text{ kHz}$ , and  $f_{p1} = 300 \text{ kHz}$  are determined to meet the crossover frequency and phase margin specifications, while  $f_{p2} = 1 \text{ MHz}$  represents a high-frequency pole in the analog control loop. The objective now is to follow the procedure outlined in this section to design a digital controller given the same crossover frequency and phase margin specifications.

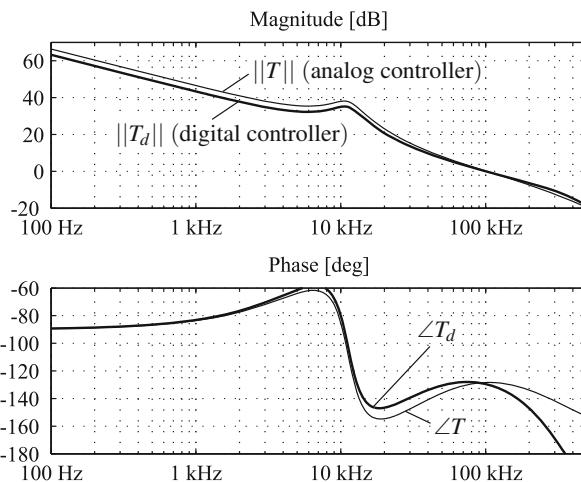
In the introductory part of this section, we have found that the loop delay can affect the digital control loop significantly, and that excessive loop delays make it impossible to design wide-bandwidth digital control loops. Let us assume a high-performance digital controller implementation, with the delay  $t_d = DT_s = 0.36 \mu\text{s}$  in the converter operating at  $f_s = 1 \text{ MHz}$ . The design objectives are the same as for the analog control loop: very large loop gain at low frequencies,  $f_c = 100 \text{ kHz}$  crossover frequency, and  $52^\circ$  phase margin. A single-pole anti-aliasing filter with a pole at  $f_{p2} = 1 \text{ MHz}$  is included in the voltage sensor transfer function, Eq. (19.56). Using the analog compensator design as a starting point, the PI corner frequency is kept the same,  $f_L = 8 \text{ kHz}$ . Since the delay  $t_d$  introduces  $-13^\circ$  phase at the target crossover frequency, the PD compensator must be redesigned to boost the phase lead at  $f_c$  to  $52^\circ + 13^\circ = 65^\circ$ . Given the required phase lead  $\theta = 65^\circ$  at  $f_c = 100 \text{ kHz}$ , Eq. (9.57) leads to  $f_z = 22 \text{ kHz}$ ,  $f_{p1} = 450 \text{ kHz}$ . Finally,  $G_{cm}$  is found to achieve the target crossover frequency,

$$G_{cm} = \sqrt{\frac{f_z}{f_{p1}}} \left( \frac{f_c}{f_o} \right)^2 \frac{1}{V_g} = 3.5 \text{ 1/V} \quad (19.62)$$

Now that all parameters in the analog compensator of Eq. (19.50) have been determined, Eqs. (19.52)–(19.54) yield the discrete-time compensator for  $f_{prewarp} = f_c$ ,

$$G_{cd}^*(z) = 31.7593 \frac{(z - 0.9493)(z - 0.8654)}{(z - 1)(z + 0.1881)} \quad (19.63)$$

Figure 19.11 compares the loop gain magnitude and phase responses in the synchronous buck regulator design example with the analog compensator in Eq. (19.61), and with the digital controller designed to take into account the loop delay  $t_d = DT_s = 0.36 \mu\text{s}$ . Note that approximately the same crossover frequency and phase margin have been achieved in the digitally controlled regulator.



**Fig. 19.11** Loop gain magnitude and phase responses in the synchronous buck regulator design example with the analog controller ( $t_d = 0$ ), and with the digital controller designed to take into account the loop delay  $t_d = DT_s = 0.36 \mu\text{s}$

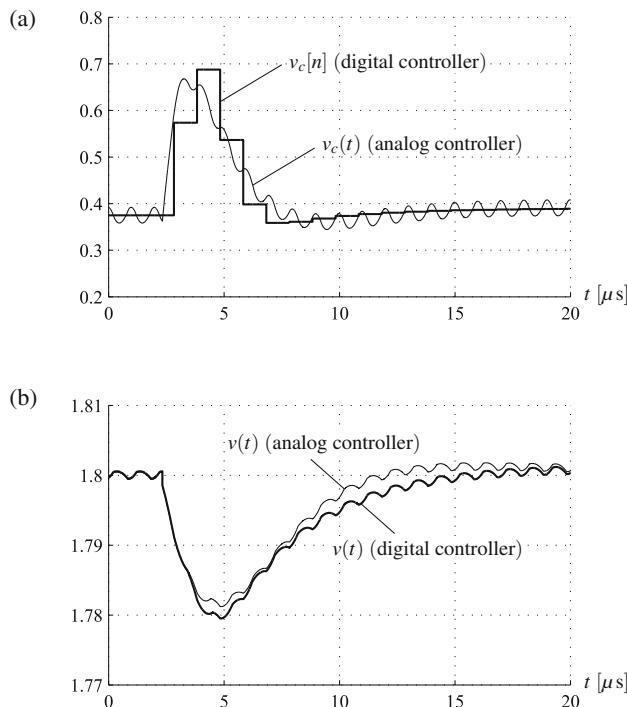
```

1 % Synchronous Buck converter parameters
2 Vg = 5; Vref = 1.8; D = Vref/Vg; % Input and reference voltages, duty cycle
3 L = 1e-6; RL = 30e-3; % Inductance and series resistance
4 C = 200e-6; Resr = 0.8e-3; % Capacitance and capacitor ESR
5 fo = 1/(2*pi*sqrt(L*C)); % Pole frequency
6 R = 1000; % Load resistance
7 fs = 1e6; Ts = 1/fs; % Switching frequency and period
8
9 s = tf('s'); z = tf('z',Ts); % Define s and z
10
11 % Open-loop control to output transfer function
12 Gvd = Vg*(Resr+1/s/C)/(Resr + 1/s/C + s*L + RL);
13 fp2 = 1e6; H = 1/(1 + s/2/pi/fp2); % Sensor transfer function
14 Tu = H * Gvd; % Uncompensated loop gain, no delay
15
16 % Analog PID compensator
17 fc = 100e3; % Cross-over frequency
18 fL = 8e3; fz = 33e3; fp1 = 300e3; % Corner frequencies
19 Gcm = sqrt(fz/fp1)*(fc/fo)^2/Vg; % Mid-frequency gain
20 % Analog compensator transfer function
21 Gc = Gcm*(1 + 2*pi*fL/s)*(1 + s/2/pi/fz)/(1+s/2/pi/fp1);
22 T = Gc*Tu; % Loop gain with analog compensator
23
24 % Uncompensated loop gain, including delay
25 td = D*Ts; % Delay in the digital control loop
26 Tu.IODelay = td; % Delay
27 Tud = c2d(Tu,Ts,'impulse'); % Mapping of Tu with delay
28 % Analog PID compensator redesigned for digital implementation
29 fL = 8e3; fz = 22e3; fp1 = 450e3; % Corner frequencies
30 Gcm = sqrt(fz/fp1)*(fc/fo)^2/Vg; % Mid-frequency gain
31 Gca = Gcm*(1 + 2*pi*fL/s)*(1 + s/2/pi/fz)/(1+s/2/pi/fp1);
32 % Digital compensator transfer function
33 Gcd = c2d(Gca, Ts, 'prewarp', 2*pi*fc);
34 Td = Tud*Gcd; % Loop gain with digital compensator
35
36 % Compare magnitude and phase responses of T and Td
37 options = bodeoptions; options.Grid = 'on';
38 options.FreqUnits = 'Hz'; options.XLim = [100, 500e3];
39 bode(T, 'k', options); % Bode plot of T
40 hold on; % Overlay plots
41 bode(Td, 'b', options); % Bode plot of Td

```

**Fig. 19.12** A MATLAB script that generates the analog and digital loop gain Bode plots shown in Fig. 19.11

A MATLAB script that generates the plots in Fig. 19.11 is shown in Fig. 19.12. The script starts by assigning the converter parameters (lines 1-7), followed by definitions of complex variables  $s$  and  $z$  (line 9). Open-loop control-to-output transfer function of the buck converter  $G_{vd}(s)$  and the uncompensated loop gain  $T_u(s)$  are formulated in lines 11-14. Analog PID compensator parameters are defined in lines 16-19 followed by the analog compensator transfer function  $G_c(s)$  in line 21 and the loop gain  $T(s)$  with the analog compensator in line 22. No delays are included in the analog controller. In line 26, delay  $t_d = DT_s$  is included as a property of the uncompensated loop gain, which is then mapped to discrete-time uncompensated loop gain  $T_{ud}(z)$  in line 27. The analog compensator, redesigned to take the delay into account, is defined in lines 28-31, and then mapped in line 33 to obtain the compensator  $G_{cd}^*(z)$ , and the loop gain  $T_d(z)$  in line 34. Bode plots of  $T(s)$  and  $T_d(z)$  are generated in lines 36-41 using the MATLAB `bode` command.



**Fig. 19.13** Step-load (2.5 A to 5 A) transient responses in the synchronous buck converter example with the analog controller ( $t_d = 0$ ), and with the digital controller designed to take into account the loop delay  $t_d = DT_s = 0.36 \mu s$ : (a) control signals  $v_c$  for the analog and digital controllers, (b) output voltage responses  $v(t)$  for the analog and digital controllers

Figure 19.13 compares step-load (2.5 A to 5 A) transient responses. While the output voltage  $v(t)$  responses in Fig. 19.13b are very similar, differences can be appreciated in the control signal responses shown in Fig. 19.13a. The digital controller produces discrete-time step-wise waveform  $v_c[n]$ , while  $v_c(t)$  in the analog controller is a continuous-time waveform that includes a switching-ripple component.

## 19.4 Digital Controller Implementation

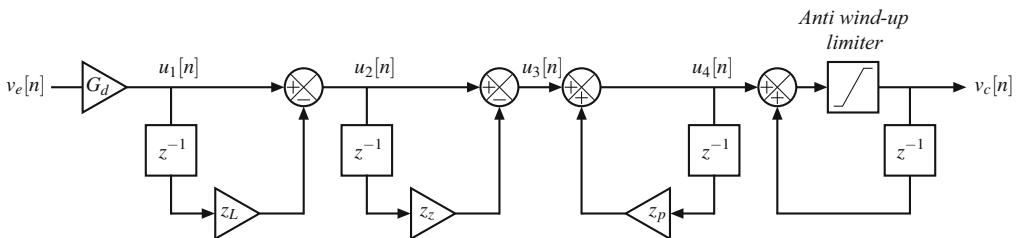
Digital controllers can be practically realized in a number of ways. For example, many standard microcontrollers or digital signal processing chips are now available, featuring multiple PWM and A/D conversion channels, allowing software-based control and power management functions. The digital controller and its digital compensation algorithm are implemented in the firmware of these chips, using a programming language such as C. An alternative approach consists of implementing the control loop in hardware, using field-programmable gate arrays (FPGA) or custom integrated circuits. In combination with specialized A/D and DPWM blocks, this approach enables high-performance designs at high switching frequencies. Controllers of this type can be developed, realized and tested using standard digital design flow starting from

logic functions described using a hardware description language (HDL) such as VHDL or Verilog, prototyping and experimental verifications using FPGA development platforms, ultimately targeting relatively small, relatively low gate-count integrated circuits capable of matching or surpassing state-of-the-art analog solutions in terms of dynamic performance, power consumption and cost. This section provides an introduction to digital controller implementation issues, with pointers to further details discussed in literature.

### 19.4.1 Discrete-Time Compensator Realization

Analog compensators are typically realized using  $RC$  networks around standard analog building blocks - operational or transconductance amplifiers. A discrete-time compensator  $G_{cd}$  is realized using digital building blocks: adders, multipliers, and storage elements. There are many possible ways to arrange these building blocks to realize a given  $G_{cd}(z)$  [176, 223]. This section presents two realization architectures particularly well suited for discrete-time PI or PID compensators in the digital control loop around a converter: a cascade realization, and a parallel realization.

The cascade realization of a PID transfer function  $G_{cd}(z)$  in Eq. (19.51) is shown in Fig. 19.14.



**Fig. 19.14** Cascade realization of the discrete-time PID compensator

The equations that can be used as a starting point in coding the compensator in microcontroller software or in HDL are as follows:

$$\begin{aligned} u_1[n] &= G_d v_e[n] \\ u_2[n] &= u_1[n] - z_L u_1[n-1] \\ u_3[n] &= u_2[n] - z_z u_2[n-1] \\ u_4[n] &= u_3[n] + z_p u_4[n-1] \\ v_c[n] &= u_4[n] + v_c[n-1] \end{aligned} \quad (19.64)$$

The compensator parameters, the gain  $G_d$ , the zeroes  $z_L$ ,  $z_z$  and the pole  $z_p$ , are the multiplicative factors, which can easily be programmable. Integration, which is performed in the last step of Eq. (19.64), includes a limiter. The purpose of the limiter is to prevent the duty-cycle command  $v_c[n]$  at the integrator output from drifting away from the allowed operating range (0 to 1, assuming DPWM with  $V_M = 1$ ). This "anti-windup" limiter function is similar to voltage limiting at the output of an analog compensator built around an op amp. In coding the compensator, one must also pay attention to the number of bits allocated to digital words representing the parameters and the signal values in order to prevent overflows or other calculation errors [223].

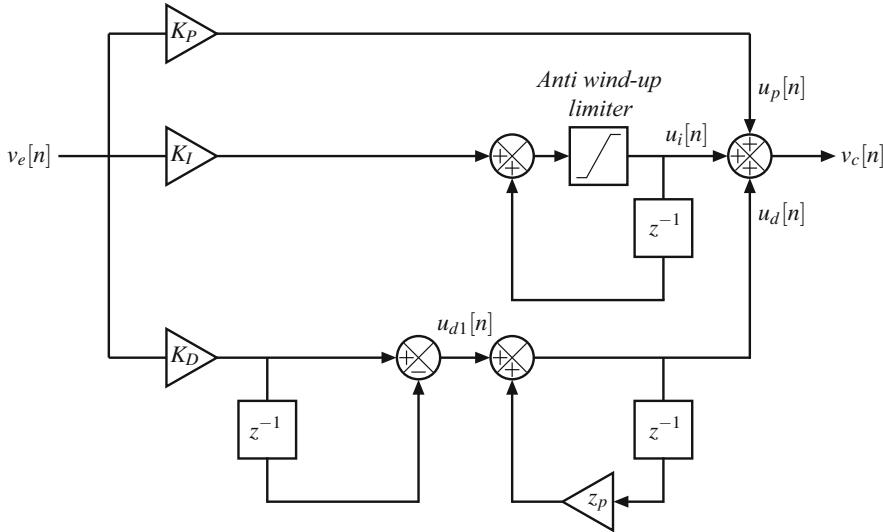
Another realization of the PID compensator is the parallel form, derived by a partial fraction expansion of  $G_{cd}$ :

$$G_{cd}(z) = G_d \frac{(z - z_L)(z - z_z)}{(z - 1)(z - z_p)} = K_P + K_I \frac{1}{1 - z^{-1}} + K_D \frac{1 - z^{-1}}{1 - z_p z^{-1}} \quad (19.65)$$

where the coefficients  $K_P$ ,  $K_D$ , and  $K_I$  can be found in terms of  $G_d$ ,  $z_L$ ,  $z_z$  and  $z_p$  parameters,

$$\begin{aligned} K_P &= G_d(z_L + z_z - z_p - (2 - z_p)z_L z_z) \\ K_I &= G_d \frac{(1 - z_L)(1 - z_z)}{1 - z_p} \\ K_D &= G_d \frac{(z_L - z_p)(z_z - z_p)}{(1 - z_p)^2} \end{aligned} \quad (19.66)$$

The parallel realization is shown in Fig. 19.15.



**Fig. 19.15** Parallel realization of the discrete-time PID compensator

The equations serving as a starting point for microcontroller or HDL coding are as follows:

$$\begin{aligned} u_p[n] &= K_P v_e[n] \\ u_i[n] &= K_I v_e[n] + u_i[n - 1] \\ u_{d1}[n] &= K_D(v_e[n] - v_e[n - 1]) \\ u_d[n] &= u_{d1}[n] + z_p u_d[n - 1] \\ v_c[n] &= u_p[n] + u_i[n] + u_d[n] \end{aligned} \quad (19.67)$$

Note that an anti-windup limiter is included in the integration stage.

The discrete-time PID transfer function in Eq. (19.65) has two zeroes and two poles. One pole is at  $z = 1$ , which correspond to the integral action in the compensator. The second pole at  $z = z_p$  corresponds to the high-frequency pole at  $f_{p1}$  in the continuous-time PID compensator. From Eq. (19.53), it follows that

$$f_{p1} = \frac{f_{\text{prewarp}}}{a} = \frac{f_{\text{prewarp}}}{\tan\left(\pi \frac{f_{\text{prewarp}}}{f_s}\right)} \quad (19.68)$$

results in  $z_p = 0$ . In this case, the discrete-time transfer function  $G_{cd}$  has a simple PID form [176], with  $K_P$ ,  $K_I$ , and  $K_D$  representing the proportional, integral, and derivative gains, respectively,

$$G_{cd}(z) = G_d \frac{(z - z_L)(z - z_z)}{z(z - 1)} = K_P + K_I \frac{1}{1 - z^{-1}} + K_D(1 - z^{-1}) \quad (19.69)$$

With  $z_p = 0$ , the realization in Fig. 19.15 is simplified because  $u_d = u_{d1}$ . The simple PID form is particularly well suited for design techniques based on tuning the gains  $K_P$ ,  $K_I$  and  $K_D$  directly [176, 223].

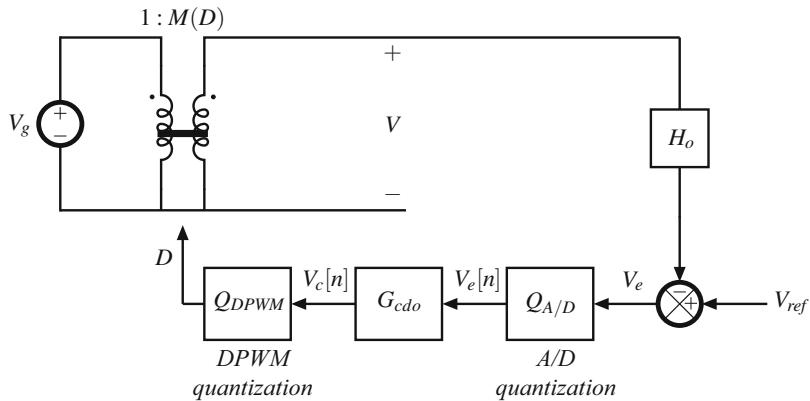
#### 19.4.2 Quantization Effects, Digital Pulse-Width Modulators and A/D Converters

Figures 19.2 and 19.3 show A/D and DPWM quantization characteristics, respectively. So far, in modeling and design of the digital control loop, we have neglected the quantization effects by simply assuming that very high-resolution A/D and DPWM blocks are employed, so that Eq. (19.9) holds. It has been observed that the nonlinearities introduced by practical, finite resolution A/D and DPWM blocks can result in persistent disturbances sometimes referred to as "limit cycling" [238–240]. The quantization effects, as well as basic conditions necessary to avoid limit-cycling disturbances, are discussed in this section first, followed by an overview of A/D and DPWM implementation approaches.

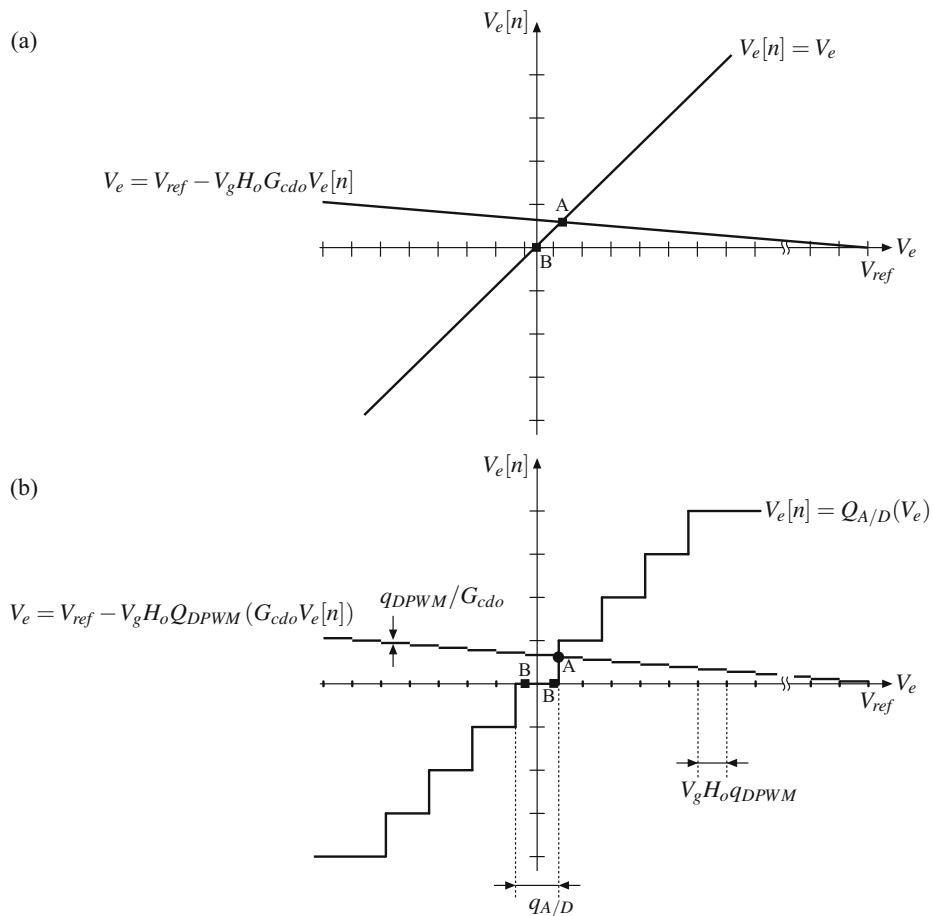
Assuming that a stable digital feedback control loop has been designed, a digitally controlled converter is expected to operate at an equilibrium point where all controller variables have constant values, and where all converter waveforms are periodic, with the period equal to  $T_s = 1/f_s$ . To find the equilibrium solution, consider a dc model of a digitally controlled converter, including A/D and DPWM quantization, as shown in Fig. 19.16. This is a static model, so the discrete-time compensator is represented by its dc gain  $G_{cd0}$ ,

$$G_{cd0} = G_{cd}(z) \Big|_{z \rightarrow 1} \quad (19.70)$$

while  $H_0$  is the sensor dc gain. Neglecting losses, the converter is represented by an ideal  $1 : M(D)$  transformer, where  $M(D) = V/V_g$  is the dc conversion ratio. The A/D quantization characteristics  $V_e[n] = Q_{A/D}(V_e(nT_s))$  is shown in Fig. 19.2, while the DWPM quantization  $D = Q_{DPWM}(V_c[n])$  is shown in Fig. 19.3. An equilibrium solution in the model of Fig. 19.16 can be found using a graphical approach illustrated in Fig. 19.17, where the digital error signal  $V_e[n]$  at the A/D converter output is shown as a function of the analog sample  $V_e = V_e(nT_s)$  at the A/D converter input.



**Fig. 19.16** Dc model of a digitally controlled converter, including A/D and DPWM quantization



**Fig. 19.17** Graphical approach to finding the quiescent operating point in a digitally controlled converter with A/D converter and DPWM having (a) infinite resolution, and (b) finite resolution. Expressions for  $V_e$  as a function of  $V_e[n]$  are shown for the synchronous buck converter example

Consider first the case in Fig. 19.17a where very high-resolution A/D and DPWM are employed, so that quantization effects can be neglected. In this case, the equilibrium solution is found at the intersection of the A/D characteristic:

$$V_e[n] = V_e \quad (19.71)$$

and the dc characteristic of the components around the loop:

$$V_e = V_{ref} - V_g H_0 G_{cd0} V_e[n] \quad (19.72)$$

This assumes a synchronous buck converter example with  $M(D) = D$ . Elimination of  $V_e$  from Eqs. (19.71) and (19.72) allows an equilibrium solution to be found algebraically:

$$V_e[n] = \frac{V_{ref}}{1 + V_g H_0 G_{cd0}} \quad (19.73)$$

When the dc gain  $G_{cd0}$  is large but finite, then the equilibrium point denoted as point A in Fig. 19.17a is achieved, which corresponds to a small but nonzero dc error. In the case when the compensator includes an integral action,  $G_{cd0} \rightarrow \infty$ , then the equilibrium solution is at point B, which corresponds to zero dc error. This is all consistent with the discussion in Sect. 9.2, which shows how a large dc loop gain drives the regulation error to zero.

Consider next a case where practical, finite resolution A/D and DPWM elements are employed. A graphical solution is illustrated Fig. 19.17b. The A/D quantization characteristic is now highly nonlinear,  $V_e[n] = Q_{A/D}(V_e)$ , with the widths of the A/D quantization bins equal to  $q_{A/D}$ . Because of the DPWM quantization, the characteristic around the loop is also nonlinear:

$$V_e = V_{ref} - V_g H_0 Q_{DPWM}(G_{cd0} V_e[n]) \quad (19.74)$$

Again this assumes a synchronous buck converter example with  $M(D) = D$ , and dc control-to-output gain equal to  $G_{d0} = V_g$ . The widths of the horizontal bins in the characteristic around the loop are equal to  $V_g H_0 q_{DPWM}$  where  $q_{DPWM} = 1/2^{n_{DPWM}}$  is the LSB resolution of the DPWM. The height of a vertical step in the characteristic given by Eq. (19.74) is equal to  $q_{DPWM}/G_{cd0}$ . If the compensator dc gain  $G_{cd0}$  is finite, then the equilibrium solution is at point A in Fig. 19.17b, on a *vertical* segment of the A/D characteristic. The A/D output  $V_e[n]$  can only be equal to an integer multiple of  $q_{A/D}$ , not a fraction of  $q_{A/D}$ . Therefore, the equilibrium point A in Fig. 19.17b is *not feasible*. Given a large, but finite dc gain of the compensator, the digitally controlled converter does not have a fixed equilibrium point. Instead, the A/D converter output must bounce among two or more quantization steps, resulting in a persistent disturbance (limit cycling) in converter waveforms.

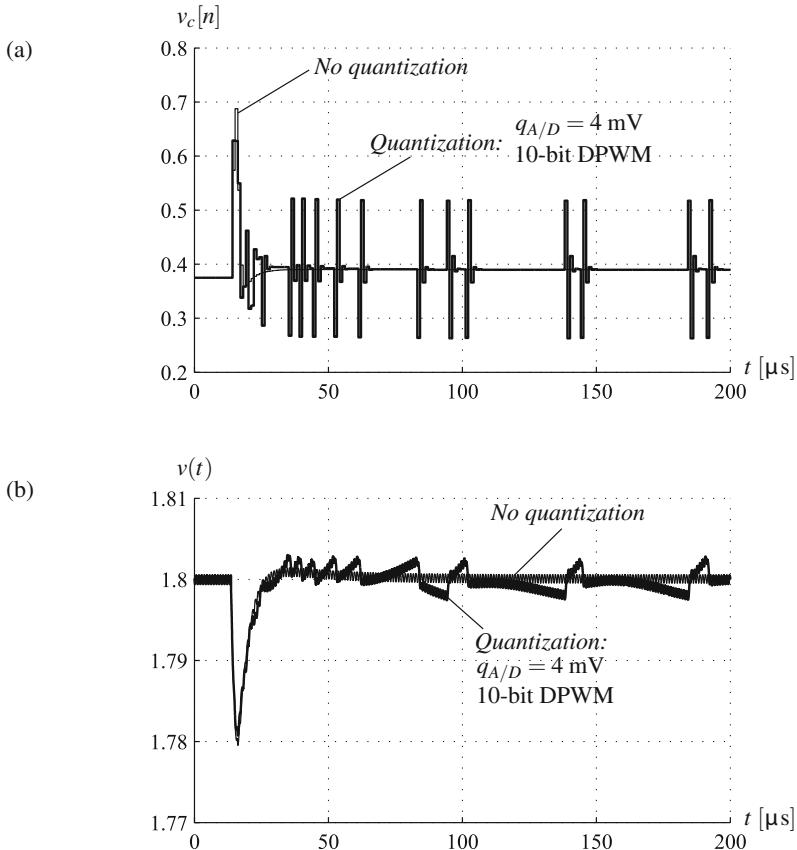
If the compensator includes an integral action,  $G_{cd0} \rightarrow \infty$ , the widths of the vertical steps in the characteristic given by Eq. (19.74) vanish. The characteristic around the A/D converter becomes a series of points,  $V_g H_0 q_{DPWM}$  apart on the horizontal ( $V_e$ ) axis. In this case, multiple equilibrium solutions are possible, as illustrated by two points B in Fig. 19.17b. Each one of the two possible equilibrium solutions is inside the A/D converter zero-error bin,  $V_e[n] = 0$ . It should be noted that the existence of multiple possible equilibrium solutions corresponding to  $V_e[n] = 0$  is predicated upon the assumption that the compensator includes integral action, and that the widths of the bins due to DPWM quantization are *shorter* than the A/D bins,

$$V_g H_0 q_{DPWM} < q_{A/D} \quad (19.75)$$

Equation (19.75) is a condition for the synchronous buck converter example where  $M(D) = D$  and  $G_{d0} = V_g$ . In general, a necessary condition for existence of an equilibrium solution in a digitally controlled converter can be written as:

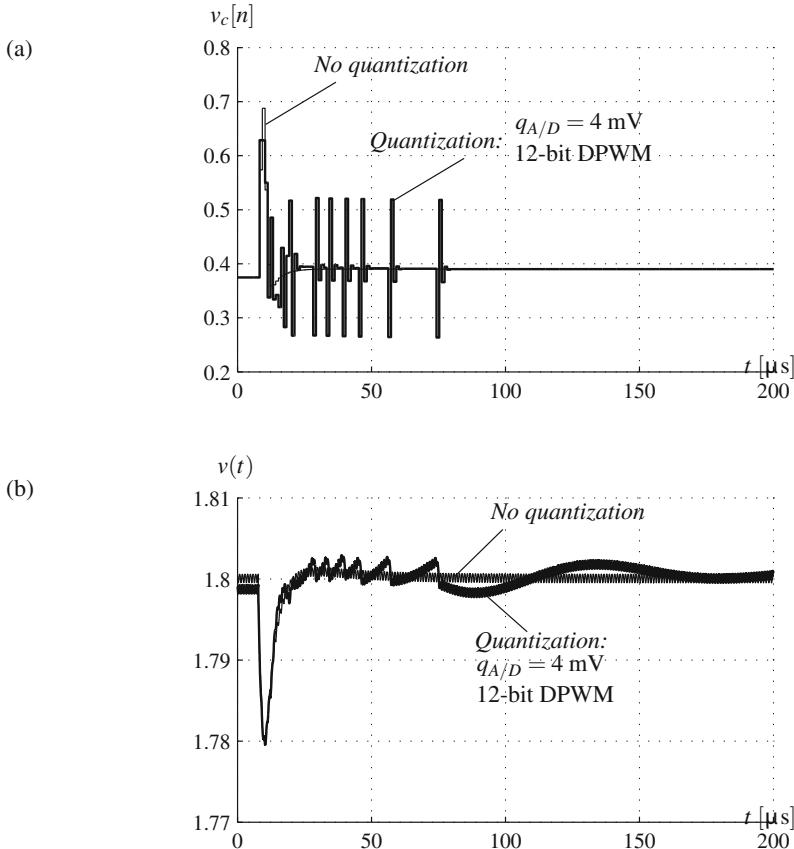
$$G_{d0}H_0q_{DPWM} < q_{A/D} \quad (19.76)$$

where  $G_{d0}$  is the converter dc control-to-output gain.



**Fig. 19.18** Comparison of step-load (2.5 A-to-5 A) transient responses in the digitally controlled synchronous buck regulator of Sect. 19.3.1 without and with quantization effects,  $q_{A/D} = 4 \text{ mV}$ ,  $n_{DPWM} = 10$

Figure 19.18 shows a comparison of step-load transient responses in the digitally controlled synchronous buck regulator example of Sect. 19.3.1, for the case when very high-resolution A/D and DPWM are employed so that quantization effects can be neglected, and for a case of practical, finite resolution components,  $q_{A/D} = 4 \text{ mV}$ ,  $n_{DPWM} = 10$ ,  $q_{DWPM} = 1/2^{10}$ ,  $V_g H_0 q_{DPWM} = 4.9 \text{ mV}$ . The compensator includes an integral action, so that  $G_{c0} \rightarrow \infty$ , but the DPWM resolution is not sufficiently high and the condition in Eq. (19.75) is not met. The step-load transient responses in Fig. 19.18 are similar, except that quantization effects result in periodic limit-cycling.

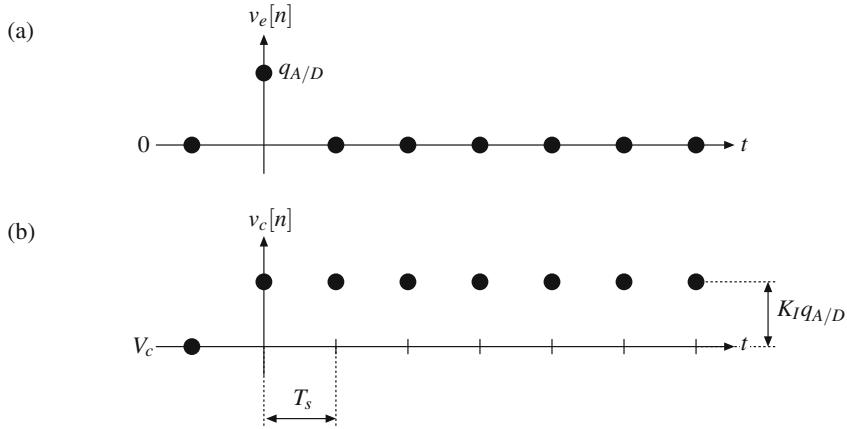


**Fig. 19.19** Comparison of step-load (2.5 A-to-5 A) transient responses in the digitally controlled synchronous buck regulator of Sect. 19.3.1 without and with quantization effects,  $q_{A/D} = 4 \text{ mV}$ ,  $n_{DPWM} = 12$

If Eq. (19.75) is not satisfied, the equilibrium solution may or may not exist, depending on whether there is a point in the characteristic given by Eq. (19.74) inside the A/D converter zero-error bin or not. Another important observation is that limit cycling, if it does occur, is relatively small in amplitude, in the order of the LSB resolution  $q_{A/D}$  of the A/D converter, as illustrated by the waveforms of Fig. 19.18.

Figure 19.19 shows a comparison of the same step-load transient responses but for the case when the DPWM resolution is increased to 12 bits,  $n_{DPWM} = 12$ ,  $q_{DPWM} = 1/2^{12}$ ,  $V_g H_0 q_{DPWM} = 1.2 \text{ mV}$ , thus meeting the condition in Eq. (19.75). After a brief transient, the regulator with practical A/D and DPWM components comes to equilibrium without limit cycling. Note that, after approximately 75  $\mu\text{s}$ , the output voltage remains within the zero-error bin, and small-amplitude ringing (undamped by feedback control) decays towards the quantized equilibrium point.

Related to the discussion of the existence of equilibrium solutions with A/D and DPWM quantization, it is of interest to note that the A/D quantization, in combination with the integral action in the compensator, results in an effective steady-state quantization of the duty-cycle



**Fig. 19.20** Waveforms illustrating quantization of the DPWM input signal  $v_c[n]$  due to A/D quantization and integral action of the digital compensator: (a) an impulse in error  $v_e[n]$ , and (b) impulse response of a digital compensator with integral gain  $K_I$

command  $V_c[n]$ . As a result, for an equilibrium solution to exist, it is not sufficient that the compensator includes integral action and that the DPWM resolution is sufficiently high. Consider the response of an integral compensator to a unit error impulse of amplitude equal to  $q_{A/D}$ , i.e., the smallest possible disturbance at the compensator input. The integrator response to this unit impulse is a step, as shown in Fig. 19.20, where  $K_I$  is the integral gain. The step amplitude in  $v_c[n]$  is equal to  $K_I q_{A/D}$ . In conclusion, because of the A/D quantization and the integral gain  $K_I$  in the compensator, the duty-cycle command signal  $V_c[n]$ , and therefore the duty cycle itself, are effectively quantized with a bin width equal to  $K_I q_{A/D}$ , regardless of how high the DPWM resolution may be. This effective DPWM quantization has exactly the same effect on the existence of an equilibrium solution as the DPWM LSB resolution  $q_{DPWM}$  in Eq. (19.76), which leads to another necessary condition,

$$G_{d0}H_0K_I q_{A/D} < q_{A/D} \quad (19.77)$$

or,

$$G_{d0}H_0K_I < 1 \quad (19.78)$$

When we combine the fact that an integral action is necessary, with the conditions in Eqs. (19.76) and (19.78), we find that the conditions for existence of an equilibrium solution in a digitally controlled converter can be written as follows:

$$\begin{aligned} G_{d0}H_0q_{DPWM} &< q_{A/D} \\ 0 < K_I &< \frac{1}{G_{d0}H_0} \end{aligned} \quad (19.79)$$

where  $G_{d0}$  is the converter dc control-to-output gain, and  $K_I$  is the compensator integral gain. In general, for any  $G_{cd}(z)$ ,  $K_I$  can be found as

$$K_I = \lim_{z \rightarrow 1} (z - 1)G_{cd}(z) \quad (19.80)$$

One may verify that with  $q_{A/D} = 4$  mV, and  $n_{DPWM} = 12$ , the conditions in Eq. (19.79) are both met for the compensator in the design example of Sect. 19.3.1.

If the conditions in Eq. (19.79) are met, a digitally controlled converter has at least one equilibrium solution in the zero-error bin of the A/D converter,  $V_e[n] = 0$ . It should be understood, however, that existence of an equilibrium solution is not sufficient to guarantee no limit cycling [238–240]. With quantization effects, the converter is a complex nonlinear dynamic system and limit-cycling disturbances can sometimes be observed even when the loop is designed for stable operation, and when the DPWM resolution and the compensator integral gain  $K_I$  meet Eq. (19.79). On the other hand, for a stable, well-designed loop with high-resolution A/D and DPWM components, the amplitude of any limit-cycling disturbances in the output voltage is relatively small, in the order of  $q_{A/D}$ , as illustrated in the example of Fig. 19.18. Therefore, in practice, such small-amplitude disturbances can often be tolerated.

Sections 19.1.1 and the discussion of quantization effects point to the need for fast, high-resolution A/D and DPWM components in a digitally controlled regulator.

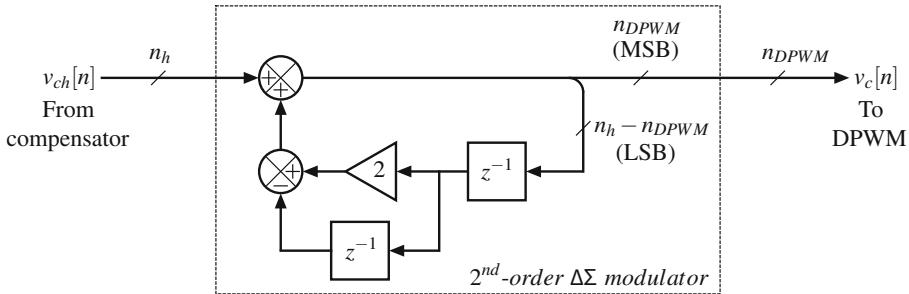
### Digital Pulse-Width Modulators

Modulators with high timing resolution are required so that the converter output voltage (or current) can be precisely regulated. Furthermore, high-resolution pulse-width modulators are needed to avoid or to minimize the amplitude of any limit-cycle disturbances. A digital modulator in combination with the converter power stage operates as a power digital-to-analog (D/A) converter, taking digital command  $v_c[n]$  as an input and producing converter voltage (or current) as an analog output. This power-D/A view has led to a number of DPWM developments based on techniques adopted from the signal D/A conversion area.

A traditional counter-based DPWM replicates analog pulse-width modulation as shown in Fig. 19.3: a saw-tooth or a triangular analog waveform is replaced by a digital counter clocked at  $f_{clk}$ , while a digital comparator outputs the modulated waveform by comparing the counter output with the digital duty-cycle command  $v_c[n]$ . A counter-based DPWM of resolution  $n_{DPWM}$  requires a clock frequency  $f_{clk} = 2^{n_{DPWM}} f_s$ , where  $f_s$  is the switching frequency. To achieve high resolution at high switching frequencies, prohibitively high clock rates may be required. To remove the need for very high clock frequencies, a fine time resolution can instead be achieved using a tapped delay line [224]. The delay cells in the delay line can also be designed to accomplish feed-forward compensation of the input voltage [184]. Hybrid DPWMs [225] combine delay-line and counter approaches to achieve desirable tradeoffs between clock rate and complexity or gate count. Various hybrid DPWM implementations have been described in [229, 232]. Other approaches in the area of high-resolution digital pulse-width modulation can be found in [226, 230, 232, 233]. An overview and classification of DPWM architectures and realizations has been presented in [227].

In addition to high-resolution DPWM hardware architectures, following the power-D/A view of a digitally controlled switched-mode power converter,  $\Delta\Sigma$  techniques, which have been used in signal processing and digital audio applications [241], have more recently been applied to digitally controlled converters.

In the digital control loop, the  $\Delta\Sigma$  modulator is placed between the discrete-time compensator  $G_{cd}$  and the DPWM. Figure 19.21 shows a second-order  $\Delta\Sigma$  modulator following the “error-feedback” architecture [241]. The error-feedback architecture has an advantage of including no delays in the forward path from the high-resolution  $n_h$ -bit compensator output  $v_{ch}[n]$  to the lower-resolution  $n_{DPWM}$ -bit duty-cycle command  $v_c[n]$  provided to the hardware DPWM



**Fig. 19.21** Second-order error-feedback  $\Delta\Sigma$  modulator placed between the compensator and the  $n_{DPWM}$ -bit DPWM can improve the effective DPWM resolution by  $n_x = n_h - n_{DPWM}$  bits

component. In the  $\Delta\Sigma$  modulator, the  $n_{DPWM}$  most significant bits (MSB) of the  $n_h$ -bit signal are delivered to the  $n_{DPWM}$ -bit DPWM, while the quantization error having  $n_x = n_h - n_{DPWM}$  least significant bits (LSB) is fed back through a simple digital filter. The  $\Delta\Sigma$  modulator shifts the quantization error (viewed as quantization noise) to high frequencies, where the noise is filtered by the low-pass action of the switched-mode power converter. Effective resolution improvements can be obtained, thus enabling digital pulse-width modulation at high frequencies and with low power consumption [188]. For example, with a 7-10-bit hardware DPWM, the second-order  $\Delta\Sigma$  modulator offers about 6-7 bits of effective resolution improvement. It has also been shown that effective resolution improvements are better with dual-edge (triangle-wave) DPWM compared to trailing-edge (saw-tooth) DPWM [231].

In conclusion, by combining delay-line or hybrid DPWM techniques with  $\Delta\Sigma$  modulation, DPWM's having very high effective resolution can be realized using relatively modest hardware resources, even at switching frequencies in the high megahertz range.

## A/D Converters

For fast control loops and precise regulation, A/D converters must have high effective resolution around a reference, and a short conversion time. Furthermore, simplicity, low-power consumption, and suitability for integration in digital VLSI processes are important. On the other hand, linearity or wide conversion range may be compromised in order to reduce the A/D complexity. These specifications differ from the typical requirements in standard A/D converters developed for signal processing, open-loop sensing, or slow control system applications, which is why various switching converter-specific A/D realizations have been investigated.

A window-flash A/D converter [182] consists of a small number of analog comparators centered around an analog reference  $V_{ref}$ , with a conversion characteristic shown in Fig. 19.2b. In some applications, as few as three A/D output levels ( $+q_{A/D}$ , 0, and  $-q_{A/D}$ ) are sufficient, which allows a window-flash A/D implementation using only two comparators [184]. Targeting implementation in digital VLSI processes, delay-line based window A/D converters have been introduced in [181]. Instead of analog comparators, the voltage-dependent delay characteristic of logic gates is used to perform voltage-to-delay and delay-to-digital conversion. Current sensing using delay-line A/D has been proposed in [242]. The delay-line A/D concept has been developed further in [189], where a high-performance, low-power, programmable architecture has been demonstrated. A similar approach, using a ring-oscillator A/D, targeting very

low-power mobile applications, has been described in [185]. An alternative A/D circuit realization approach, using threshold inverter quantization (TIQ) has been proposed in [243]. In the TIQ A/D approach, logic inverters with programmed thresholds replace analog comparators, enabling fast conversion and asynchronous sampling in a high-performance digital hysteretic controller [243].

## 19.5 Summary of Key Points

1. Digital control has become a practical technique for high-performance switching power conversion systems that enables higher-level control functionality in modern power management systems. These control systems include analog-to-digital converters and digital pulse-width modulators that perform signal quantization/sampling of both amplitude and time. These quantization effects introduce new phenomena that may limit controller performance and that should be considered in the closed-loop design.
2. The analog system modeling, analysis, and design techniques of earlier chapters can be adapted to the case when the controller/compensator is implemented digitally. The loop gain  $T_d(j\omega)$  of the digital control system includes both the gains of the analog portions such as  $G_{vd}(j\omega)$  and  $H(j\omega)$  as well as the gains of the A/D converter, digital compensator, and the DPWM.
3. An approach to incorporate the digital controller discrete-time response  $G_{cd}(z)$  into the continuous-time response  $G_{vd}(s)H(s)$  of the analog portion of the system is developed in this chapter. Approximations can be employed that relate the digital and analog signals associated with integration: the trapezoidal approximation Eq. (19.35) provides a way to connect the  $s$ -plane transfer functions of the analog portion and the  $z$ -plane transfer functions of the digital portion. The magnitude and phase of the loop gain  $T_d(j\omega)$  can be found and plotted, and the important quantities such as the crossover frequency and phase margin can be evaluated.
4. The  $\mathcal{Z}$ -transform is a well-known approach for modeling discrete-time digital systems such as the digital compensator. This approach provides a direct and simple way to represent the operation of digital compensators. The definition  $z = e^{sT_s}$ , or the trapezoidal approximation (19.35), leads to a direct connection between the  $\mathcal{Z}$ -transform of the digital domain and the Laplace transform of the analog domain.
5. The converter modeling and analog controller design techniques of earlier chapters can be employed as a starting point for design of a digital controller. The delays inherent in the digital controller elements must be added. A PI, PD, or PID compensator is designed as discussed in Chap. 9, that then is translated to the  $z$ -domain as discussed in Sect. 19.3. Section 19.4 describes implementation of the compensator algorithm in digital hardware.

## PROBLEMS

- 19.1** A microcontroller operates at  $f_{clk} = 120$  MHz clock frequency and has counter-based DPWM units. Assuming trailing-edge pulse-width modulation, calculate the DPWM resolution as the number of bits  $n_{DPWM}$  available when the microcontroller is used to implement a digital controller around a switched-mode power converter operating at different switching frequencies: (i)  $f_s = 100$  kHz, (ii)  $f_s = 250$  kHz, or (iii)  $f_s = 1$  MHz.

- 19.2** A microcontroller has high-resolution DPWM units, which offer 150 ps timing resolution. Assuming trailing-edge pulse-width modulation, calculate the DPWM resolution as the number of bits  $n_{DPWM}$  available when the microcontroller is used to implement a digital controller around a switched-mode power converter operating at different switching frequencies: (i)  $f_s = 100$  kHz, (ii)  $f_s = 250$  kHz, or (iii)  $f_s = 1$  MHz.
- 19.3** A digital controller, which includes an  $n_{DPWM}$ -bit DPWM, is used to control a switched-mode power converter having dc conversion ratio  $M(D) = V/V_g$ . Derive an expression for the voltage positioning resolution  $p_v = \Delta V/V$  in %, where  $\Delta V$  is a step in the output voltage  $V$  that corresponds to a least significant bit (LSB) step  $q_{DPWM}$  in duty cycle  $D$ . The expression for  $p_v$  should be in terms of  $M(D)$  and  $n_{DPWM}$ . Based on this general expression, derive  $p_v$  as a function of  $D$  and  $n_{DPWM}$  for the three basic conversion ratios: (i) buck  $M(D) = D$ , (ii) boost  $M(D) = 1/(1-D)$ , and (iii) buck-boost  $M(D) = D/(1-D)$ . In the three cases considered, how difficult is it to precisely position the output voltage at high step-down or high step-up conversion ratios?
- 19.4** A microcontroller has A/D converters with  $n_{A/D}$ -bit resolution and full-scale voltage  $V_{FS}$ . The microcontroller is used to implement a digital controller around a switched-mode power converter so that the output voltage is regulated at  $V = V_{ref}/H_o$ , where  $H_o$  is the voltage sensing gain at dc. To allow for proper operation during transients, the A/D converter must not saturate as long as the output voltage remains within  $\pm 10\%$  of the nominal output voltage  $V$ . Choose  $V_{ref}$  and  $H_o$  as functions of  $V$  and  $V_{FS}$  to achieve the best possible resolution  $\Delta V$  in output voltage regulation, where  $\Delta V$  corresponds to the zero-error bin of the A/D converter. Given  $n_{A/D} = 10$ ,  $V_{FS} = 2$  V, and  $V = 12$  V, calculate numerical values for  $V_{ref}$ ,  $H_o$ , and  $\Delta V$ .
- 19.5** A digital controller has a window A/D converter with a number of  $q_{A/D}$  bins centered around an analog reference voltage  $V_{ref}$ . The controller is used around a switched-mode power converter so that the output voltage is regulated at  $V = V_{ref}/H_o$ , where  $H_o$  is the voltage sensing gain at dc. To allow for proper operation during transients, the A/D converter must not saturate as long as the output voltage remains within  $\pm 10\%$  of the nominal output voltage  $V$ . How many  $q_{A/D}$  bins are required in the window A/D converter? Given  $V_{ref} = 2$  V,  $q_{A/D} = 5$  mV, and  $V = 12$  V, calculate numerical values for  $H_o$ ,  $\Delta V$  corresponding to  $q_{A/D}$ , and the number of bins required.
- 19.6** An analog proportional-derivative (PD) compensator transfer function is

$$G_c(s) = G_{c0} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}}$$

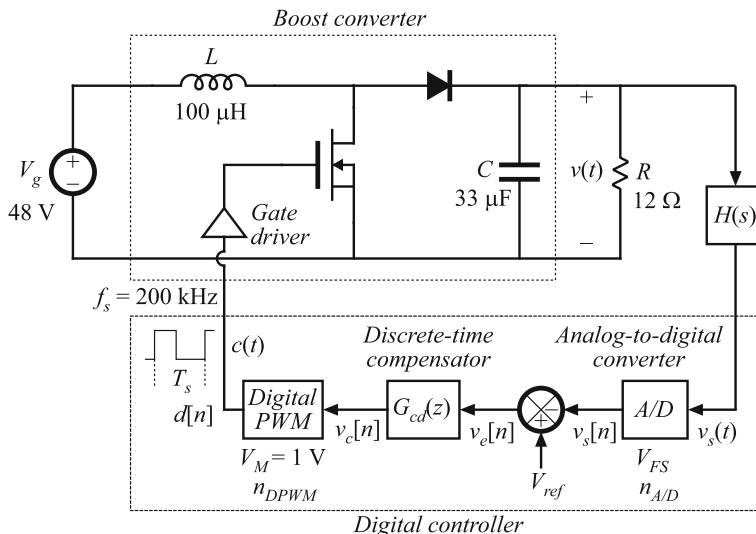
where  $G_{c0} = 1$ ,  $f_z = 10$  kHz and  $f_p = 100$  kHz. As discussed in Sect. 9.5.1, the analog PD compensator offers the largest phase lead at  $f_x = \sqrt{f_z f_p} = 31.6$  kHz. You may use MATLAB or a tool of your choice to perform mapping and calculations requested in this problem.

- (a) Construct the Bode plot of  $G_c(s)$  magnitude and phase. Calculate the magnitude (in dB) and phase (in degrees) responses at (i)  $f = f_z$ , (ii)  $f = f_x$ , and (iii)  $f = f_p$ .
- (b) Using bilinear mapping with prewarp at  $f_{prewarp} = f_x$ , map  $G_c(s)$  to  $G_{cd}^*(z)$ . Calculate the magnitude (in dB) and phase (in degrees) responses of  $G_{cd}^*$  at (i)  $f = f_z$ , (ii)  $f = f_x$ , and (iii)  $f = f_p$ , and compare to the results obtained in part (a) for three different sampling frequencies:  $f_s = 500$  kHz,  $f_s = 250$  kHz, and  $f_s = 150$  kHz. Overlay Bode plots of  $G_c$  and  $G_{cd}^*$  for the three different sampling frequencies.

- 19.7** Figure 19.22 shows a boost voltage regulator similar to the closed-loop regulated boost converter in Problem 9.3, except that the controller is implemented digitally. Converter components can be considered ideal. The voltage sensor transfer function is

$$H(s) = \frac{H_o}{1 + \frac{s}{\omega_p}}$$

where  $H_o = 1/120$ , and  $f_p = 10$  kHz. The voltage reference is  $V_{ref} = 1$  V. The full-scale voltage of the A/D converter is  $V_{FS} = 2$  V. The controller employs a trailing-edge DPWM with  $V_M = 1$  V, and an integral discrete-time compensator  $G_{cd}(z)$ . In parts (a)–(c) of the problem, you may assume that the A/D converter and the DPWM are very high-resolution components with unity gains. The A/D converter is sampling the sensed voltage  $v_s$  once per switching period, and the delay in the digital control loop is  $t_d = t_{mod} = DT_s$ . To construct requested Bode plots and to perform numerical calculations you may use MATLAB or a tool of your choice.

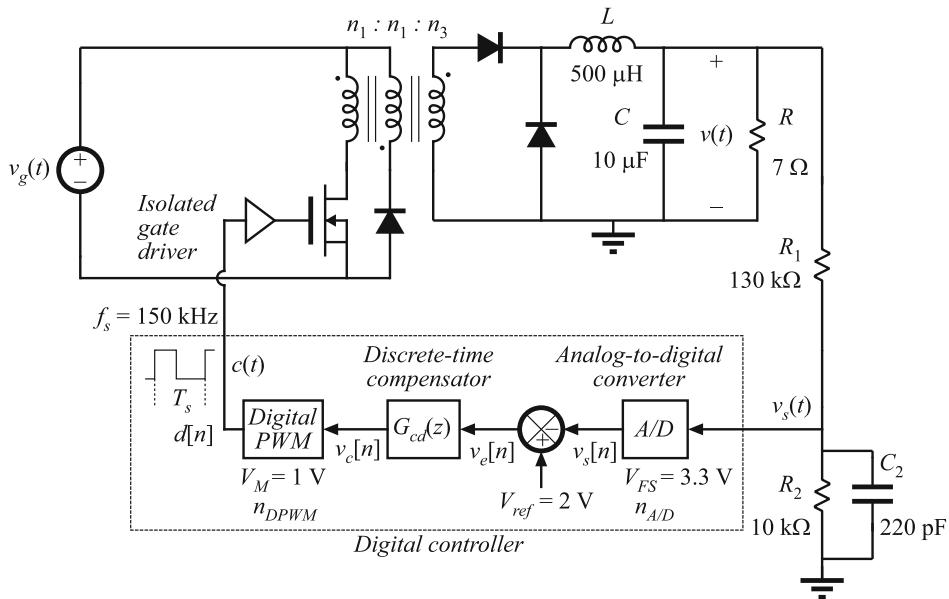


**Fig. 19.22** Digitally controlled boost converter of Problem 19.7

- (a) Determine steady-state dc output voltage  $V$ , duty cycle  $D$ , and delay  $t_d$  in the digital control loop.
- (b) Assuming analog controller implementation with a negligible delay, design an analog integral compensator  $G_c(s) = K_c/s$ , i.e., determine  $K_c$  to obtain crossover frequency  $f_c = 125$  Hz. With this  $G_c(s)$ , construct the Bode plot of the loop gain  $T(s)$  magnitude and phase. Label values of all corner frequencies and  $Q$ -factors, as appropriate. Determine phase margin.
- (c) Following the design procedure of Sect. 19.3, design a discrete-time integral compensator  $G_{cd}(z)$  to achieve the same crossover frequency and phase margin specifications

as in part (b). Overlay Bode plots of the magnitude and phase responses of  $T(s)$  and  $T_d(z)$  and numerically verify the values obtained for the crossover frequency and the phase margin.

- (d) Find the minimum A/D resolution  $n_{A/D}$  and the minimum DPWM resolution  $n_{DPWM}$  required so that the dc output voltage is regulated to within  $\pm 0.25$  V, and so that the necessary no-limit-cycling conditions in Eq. (19.79) are met.



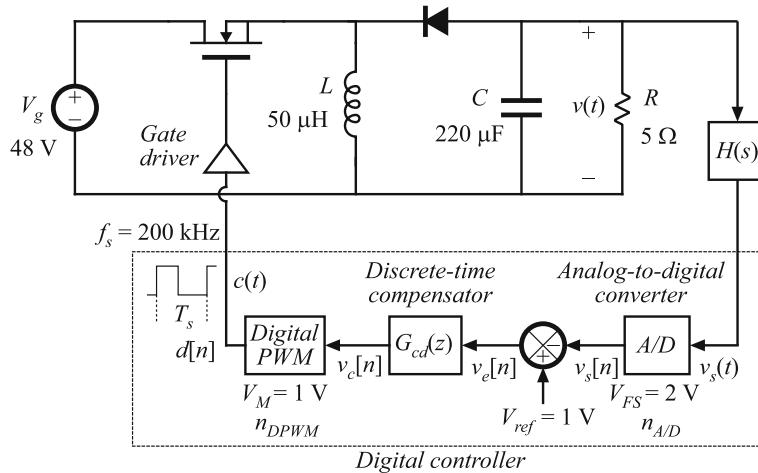
**Fig. 19.23** Digitally controlled forward converter of Problem 19.8

- 19.8** Figure 19.23 shows a digitally controlled forward converter. This closed-loop voltage regulator is similar to the system with the analog controller in Problem 9.5. The quiescent value of the input voltage is  $V_g = 380$  V. The transformer has turns ratio  $n_1/n_3 = 4.5$ . The duty cycle produced by the digital pulse-width modulator is restricted to the range  $0 \leq d(t) \leq 0.5$  and in that range  $d(t) = v_c[n]/V_M$  where  $V_M = 1$  V. The DPWM employs dual-edge modulation and has  $n_{DPWM} = 12$ -bit resolution. The A/D converter has  $n_{A/D} = 9$ -bit resolution and is sampling the sensed voltage  $v_s$  once per switching period  $T_s$ . The delay in the digital control loop is  $t_d = T_s/2$ . The A/D converter and the DPWM have unity gains. Converter components can be considered ideal, and parameter values are shown in Fig. 19.23. The small-signal models and transfer functions of forward and buck converters are similar. The transformer magnetizing inductance has negligible influence on the converter dynamics, and can be ignored. The discrete-time compensator is

$$G_{cd}(z) = 0.1152 \frac{z - 0.91}{z - 1}$$

You may use MATLAB or a tool of your choice to perform mapping, calculations, and plotting.

- (a) Determine the quiescent values of the duty cycle  $D$  and the output voltage  $V$ .
- (b) Derive expressions for the control-to-output transfer function  $G_{vd}(s)$  and the uncompensated loop gain  $T_u(s)$ , including effects of the voltage sensor transfer function  $H(s) = v_s/v$ , and delay  $t_d$  in the digital control loop.
- (c) Construct a Bode plot of the loop gain  $T_d$  magnitude and phase. What is the crossover frequency? What is the phase margin?
- (d) Are the necessary no-limit-cycling conditions in Eq. (19.79) satisfied for the system in Fig. 19.23?



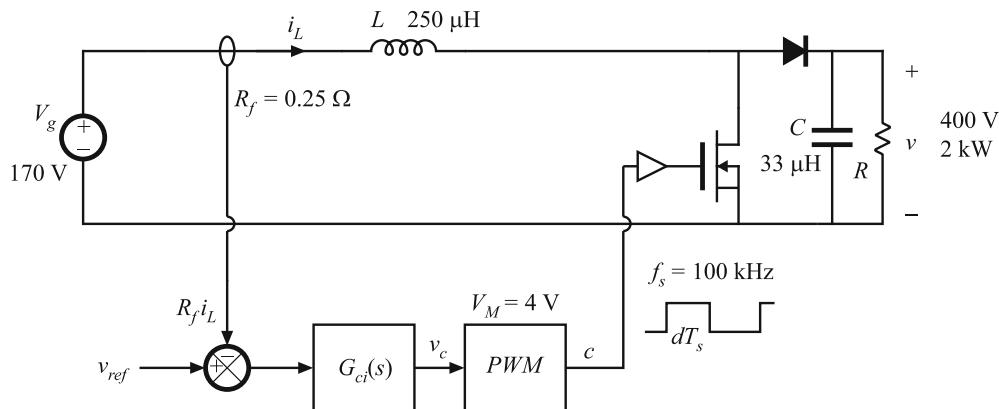
**Fig. 19.24** Digitally controlled buck-boost voltage regulator system, Problem 19.9

**19.9** Design of a digitally controlled buck-boost voltage regulator. This design problem is similar to Problem 9.9, except that the controller is implemented digitally. The buck-boost converter of Fig. 19.24 operates in the continuous conduction mode, with the element values shown. The nominal input voltage is  $V_g = 48 \text{ V}$ , and it is desired to regulate the output voltage at  $-15 \text{ V}$ . Design the best compensator that you can, which has high crossover frequency (but no greater than 10% of the switching frequency), large loop gain over the bandwidth of the feedback loop, and phase margin of at least  $45^\circ$ . The A/D converter, which has up to 12-bit resolution,  $n_{A/D} \leq 12$ , samples the sensed output voltage once per switching period. The DPWM, which has up to 10-bit resolution,  $n_{DPWM} \leq 10$  uses trailing-edge modulation. The delay in the digital control loop is  $t_d = t_{mod} = DT_s$ . The A/D converter and the DPWM have unity gains. The sensor  $H(s)$  has an inverting gain, and includes a single-pole anti-aliasing filter

$$H(s) = -\frac{H_0}{1 + \frac{s}{\omega_p}}$$

where  $H_0 > 0$  and  $f_p = 100 \text{ kHz}$ . In the design, you may use MATLAB or a tool of your choice to perform mapping, plotting and calculations.

- (a) Specify the required value of  $H_0$ . Select  $n_{A/D}$  and  $n_{DPWM}$  to achieve best possible dc voltage regulation while meeting the necessary no-limit-cycling condition expressed in Eq. (19.76).
- (b) Design the discrete-time compensator  $G_{cd}(z)$ . Construct Bode plots of the uncompensated loop gain  $T_{ud}$  magnitude and phase (including effects of delay in the feedback loop), as well as the magnitude and phase of your compensator transfer function  $G_{cd}(z)$ . Label the important features of your plots. Verify that the no-limit-cycling conditions expressed in Eq. (19.79) are satisfied.
- (c) Construct Bode diagrams of the magnitude and phase of your compensated loop gain  $T_d(z)$ , and also of the magnitude of the quantities  $T_d/(1 + T_d)$  and  $1/(1 + T_d)$ . Calculate crossover frequency and phase margin.
- (d) Discuss your design. What prevents you from further increasing the crossover frequency?



**Fig. 19.25** Boost converter with analog average current-mode control

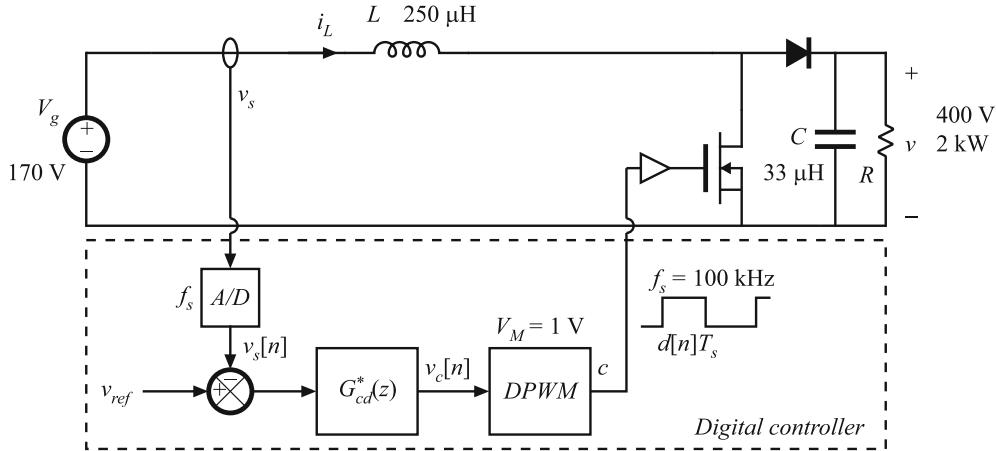
- 19.10** Figure 19.25 shows a boost converter with analog average current-mode control of the inductor current. The analog compensator transfer function is

$$G_{ci}(s) = G_{cm} \frac{1 + \frac{\omega_z}{s}}{1 + \frac{s}{\omega_p}}$$

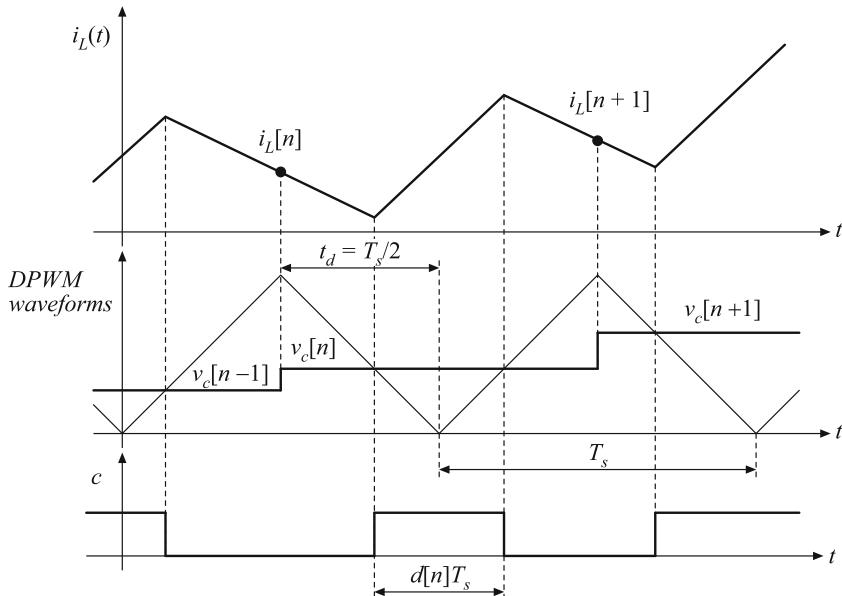
where  $G_{cm} = 0.63$ ,  $f_z = 4$  kHz,  $f_p = 25$  kHz. The current sensing gain is  $R_f = 0.25 \Omega$ . Figure 19.26 shows the same converter with average current-mode control implemented digitally. Current sensing includes an analog single-pole anti-aliasing filter

$$\frac{v_s}{i_L} = R_f \frac{1}{1 + \frac{s}{\omega_a}}$$

where  $R_f = 0.25 \Omega$  and  $f_a = 200$  kHz. In both cases, the power stage parameters are the same and losses can be neglected. You may assume that the A/D converter and



**Fig. 19.26** Boost converter with digital average current-mode control



**Fig. 19.27** Timing diagram for the digitally controlled boost converter in Fig. 19.26

the DPWM are very high-resolution components with unity gains. A timing diagram illustrating sampling of the inductor current and operation of the digital pulse-width modulator is shown in Fig. 19.27. Note that a dual-edge (triangle-wave) DPWM is employed. In the design of the digital controller you only need to consider the modular delay  $t_d = t_{mod} = T_s/2$ , as shown in Fig. 19.27. You may use MATLAB or a tool of your choice to perform calculations, and to construct Bode plots.

- a) For the analog average current-mode controlled converter of Fig. 19.25, determine the steady-state operating point, *i.e.*, find the dc values of  $I_L$ ,  $V$ ,  $D$ ,  $V_c$  and  $V_{ref}$ , where  $V_{ref}$  is the reference input for the current control loop.
- b) For the analog average current-mode controlled converter of Fig. 19.25, at the operating point found in part (a), plot the magnitude and phase responses of the current loop gain  $T_i(s)$ , and determine crossover frequency  $f_{ci}$  and phase margin  $\phi_i$ .
- c) For the digital average current-mode controlled converter of Fig. 19.26, determine the steady-state operating point, *i.e.*, find the dc values of  $I_L$ ,  $V$ ,  $D$ ,  $V_c[n]$ , and  $V_{ref}$ .
- d) Given the modulator delay  $t_d$ , find the additional phase lag  $\Delta\phi_d$  in the digital control loop at the frequency  $f_{ci}$  found in part (b).
- e) Design a discrete-time compensator  $G_{cid}^*(z)$  so that the crossover frequency and the phase margin in the digitally controlled converter are the same as the values found in part (b). Use bilinear mapping with prewarping at  $f_{ci}$ . Express  $G_{cid}^*(z)$  in factored pole/zero form. Show the work documenting your design process. Overlay plots of the magnitude and phase responses of the loop gain  $T_i$  found in part (b) and the loop gain  $T_{id}$  in the digitally controlled converter.

## **Part V**

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### **Modern Rectifiers and Power System Harmonics**

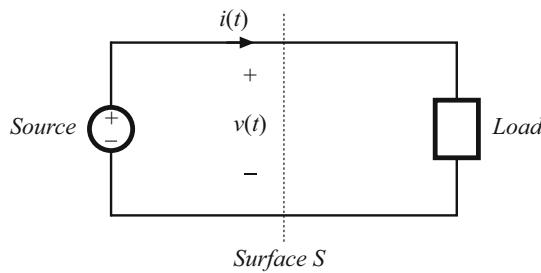


## Power and Harmonics in Nonsinusoidal Systems

Rectification used to be a much simpler topic. A textbook could cover the topic simply by discussing the various circuits, such as the peak-detection and inductor-input rectifiers, the phase-controlled bridge, polyphase transformer connections, and perhaps multiplier circuits. But recently, rectifiers have become much more sophisticated, and are now systems rather than mere circuits. They often include pulse-width modulated converters such as the boost converter, with control systems that regulate the ac input current waveform. So modern rectifier technology now incorporates many of the dc–dc converter fundamentals.

The reason for this is the undesirable ac line current harmonics, and low power factors, of conventional peak-detection and phase-controlled rectifiers. The adverse effects of power system harmonics are well-recognized. These effects include: unsafe neutral current magnitudes in three-phase systems, heating and reduction of life in transformers and induction motors, degradation of system voltage waveforms, unsafe currents in power factor correction capacitors, and malfunctioning of certain power system protection elements. In a real sense, conventional rectifiers are harmonic polluters of the ac power distribution system. With the widespread deployment of electronic equipment in our society, rectifier harmonics have become a significant and measurable problem. Thus there is a need for *high-quality rectifiers*, which operate with high power factor, high efficiency, and reduced generation of harmonics. Several international standards now exist that specifically limit the magnitudes of harmonic currents, for both high-power equipment such as industrial motor drives and low-power equipment such as electronic ballasts for fluorescent lamps and power supplies for office equipment.

This chapter treats the flow of energy in power systems containing nonsinusoidal waveforms. Average power, rms values, and power factor are expressed in terms of the Fourier series of the voltage and current waveforms. Harmonic currents in three-phase systems are discussed, and present-day standards are listed. The following chapters treat harmonics and harmonic mitigation in conventional line-commutated rectifiers, high-quality rectifier circuits and their models, and control of high-quality rectifiers.



**Fig. 20.1** Observe the transmission of energy through surface  $S$

## 20.1 Average Power

Let us consider the transmission of energy from a source to a load, through a given surface as in Fig. 20.1. In the network of Fig. 20.1, the voltage waveform  $v(t)$  (not necessarily sinusoidal) is given by the source, and the current waveform is determined by the response of the load. In the more general case in which the source output impedance is significant, then  $v(t)$  and  $i(t)$  both depend on the characteristics of the source and load. Balanced three-phase systems may be treated in the same manner, on a per-phase basis, using a line current and line-to-neutral voltage.

If  $v(t)$  and  $i(t)$  are periodic, then they may be expressed as Fourier series:

$$\begin{aligned} v(t) &= V_0 + \sum_{n=1}^{\infty} V_n \cos(n\omega t - \varphi_n) \\ i(t) &= I_0 + \sum_{n=1}^{\infty} I_n \cos(n\omega t - \theta_n) \end{aligned} \quad (20.1)$$

where the period of the ac line voltage waveform is defined as  $T = 2\pi/\omega$ . In general, the instantaneous power  $p(t) = v(t)i(t)$  can assume both positive and negative values at various points during the ac line cycle. Energy then flows in both directions between the source and load. It is of interest to determine the net energy transmitted to the load over one cycle, or

$$W_{cycle} = \int_0^T v(t)i(t) dt \quad (20.2)$$

This is directly related to the average power as follows:

$$P_{av} = \frac{W_{cycle}}{T} = \frac{1}{T} \int_0^T v(t)i(t) dt \quad (20.3)$$

Let us investigate the relationship between the harmonic content of the voltage and current waveforms, and the average power. Substitution of the Fourier series, Eq. (20.1), into Eq. (20.3) yields

$$P_{av} = \frac{1}{T} \int_0^T \left( V_0 + \sum_{n=1}^{\infty} V_n \cos(n\omega t - \varphi_n) \right) \left( I_0 + \sum_{n=1}^{\infty} I_n \cos(n\omega t - \theta_n) \right) dt \quad (20.4)$$

To evaluate this integral, we must multiply out the infinite series. It can be shown that the integrals of cross-product terms are zero, and the only contributions to the integral comes from the products of voltage and current harmonics of the same frequency:

$$\int_0^T (V_n \cos(n\omega t - \varphi_n)) (I_m \cos(m\omega t - \theta_m)) dt = \begin{cases} 0 & \text{if } n \neq m \\ \frac{V_n I_n}{2} \cos(\varphi_n - \theta_n) & \text{if } n = m \end{cases} \quad (20.5)$$

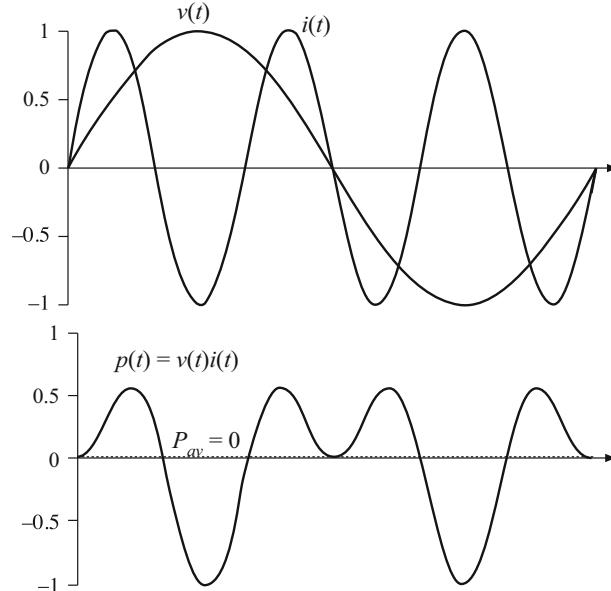
The average power is therefore

$$P_{av} = V_0 I_0 + \sum_{n=1}^{\infty} \frac{V_n I_n}{2} \cos(\varphi_n - \theta_n) \quad (20.6)$$

So net energy is transmitted to the load only when the Fourier series of  $v(t)$  and  $i(t)$  contain terms at the same frequency. For example, if  $v(t)$  and  $i(t)$  both contain third harmonic, then net energy is transmitted at the third harmonic frequency, with average power equal to

$$\frac{V_3 I_3}{2} \cos(\varphi_3 - \theta_3) \quad (20.7)$$

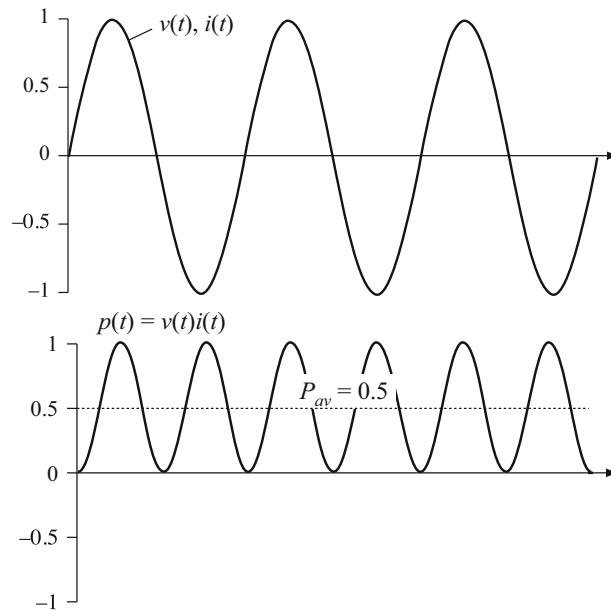
Here,  $V_3 I_3/2$  is equal to the rms volt-amperes of the third harmonic current and voltage. The  $\cos(\varphi_3 - \theta_3)$  term is a displacement term which accounts for the phase difference between the third harmonic voltage and current.



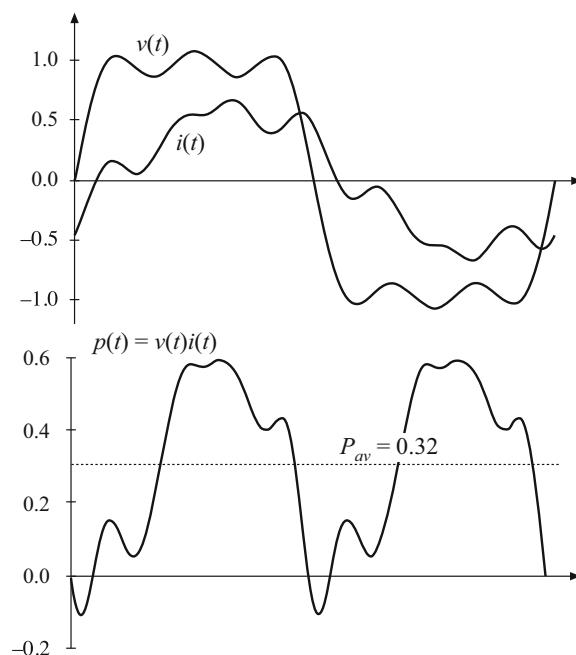
**Fig. 20.2** Voltage, current, and instantaneous power waveforms, example 1. The voltage contains only fundamental and the current contains only third harmonic. The average power is zero

Some examples of power flow in systems containing harmonics are illustrated in Figs. 20.2 to 20.4. In example 1, Fig. 20.2, the voltage contains fundamental only, while the current contains third harmonic only. It can be seen that the instantaneous power waveform  $p(t)$  has a zero average value, and hence  $P_{av}$  is zero. Energy circulates between the source and load, but over one cycle the net energy transferred to the load is zero. In example 2, Fig. 20.3, the voltage and current each contain only third harmonic. The average power is given by Eq. (20.7) in this case.

In example 3, Fig. 20.4, the voltage waveform contains fundamental, third harmonic, and fifth harmonic, while the current contains fundamental, fifth harmonic, and seventh harmonic, as follows:



**Fig. 20.3** Voltage, current, and instantaneous power waveforms, example 2. The voltage and current each contain only third harmonic, and are in phase. Net energy is transmitted at the third harmonic frequency



**Fig. 20.4** Voltage, current, and instantaneous power waveforms, example 3. The voltage contains fundamental, third, and fifth harmonics. The current contains fundamental, fifth, and seventh harmonics. Net energy is transmitted at the fundamental and fifth harmonic frequencies

$$\begin{aligned}v(t) &= 1.2 \cos(\omega t) + 0.33 \cos(3\omega t) + 0.2 \cos(5\omega t) \\i(t) &= 0.6 \cos(\omega t + 30^\circ) + 0.1 \cos(5\omega t + 45^\circ) + 0.1 \cos(7\omega t + 60^\circ)\end{aligned}\quad (20.8)$$

Average power is transmitted at the fundamental and fifth harmonic frequencies, since only these frequencies are present in both waveforms. The average power is found by evaluation of

Eq. (20.6); all terms are zero except for the fundamental and fifth harmonic terms, as follows:

$$p_{av} = \frac{(1.2)(0.6)}{2} \cos(30^\circ) + \frac{(0.2)(0.1)}{2} \cos(45^\circ) = 0.32 \quad (20.9)$$

The instantaneous power and its average are illustrated in Fig. 20.4.

## 20.2 Root-Mean-Square (RMS) Value of a Waveform

The rms value of a periodic waveform  $v(t)$  with period  $T$  is defined as

$$(\text{rms value}) = \sqrt{\frac{1}{T} \int_0^T v^2(t) dt} \quad (20.10)$$

The rms value can also be expressed in terms of the Fourier components. Insertion of Eq. (20.1) into Eq. (20.10), and simplification using Eq. (20.5), yields

$$(\text{rms value}) = \sqrt{V_0^2 + \sum_{n=1}^{\infty} \frac{V_n^2}{2}} \quad (20.11)$$

Again, the integrals of the cross-product terms are zero. This expression holds when the waveform is a current:

$$(\text{rms current}) = \sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}} \quad (20.12)$$

Thus, the presence of harmonics in a waveform always increases its rms value. In particular, in the case where the voltage  $v(t)$  contains only fundamental while the current  $i(t)$  contains harmonics, then the harmonics increase the rms value of the current while leaving the average power unchanged. This is undesirable, because the harmonics do not lead to net delivery of energy to the load, yet they increase the  $I_{rms}^2 R$  losses in the system.

In a practical system, series resistances always exist in the source, load, and/or transmission wires, which lead to unwanted power losses obeying the expression

$$(\text{rms current})^2 R_{series} \quad (20.13)$$

Examples of such loss elements are the resistance of ac generator windings, the resistance of the wire connecting the source and load, the resistance of transformer windings, and the resistance of semiconductor devices, and magnetics windings in switching converters. Thus, it is desired to make the rms current as small as possible, while transferring the required amount of energy and average power to the load.

Shunt resistances usually also exist, which cause power loss according to the relation

$$\frac{(\text{rms voltage})^2}{R_{shunt}} \quad (20.14)$$

Examples include the core losses in transformers and ac generators, and switching converter transistor switching loss. Therefore, it is desired to also make the rms voltage as small as possible while transferring the required average power to the load.

## 20.3 Power Factor

*Power factor* is a figure-of-merit that measures how effectively energy is transmitted between a source and load network. It is measured at a given surface as in Fig. 20.1, and is defined as

$$\text{power factor} = \frac{(\text{average power})}{(\text{rms voltage})(\text{rms current})} \quad (20.15)$$

The power factor always has a value between zero and one. The ideal case, unity power factor, occurs for a load that obeys Ohm's Law. In this case, the voltage and current waveforms have the same shape, contain the same harmonic spectrum, and are in phase. For a given average power throughput, the rms current and voltage are minimized at maximum (unity) power factor, that is, with a linear resistive load. In the case where the voltage contains no harmonics but the load is nonlinear and contains dynamics, then the power factor can be expressed as a product of two terms, one resulting from the phase shift of the fundamental component of the current, and the other resulting from the current harmonics.

### 20.3.1 Linear Resistive Load, Nonsinusoidal Voltage

In this case, the current harmonics are in phase with, and proportional to, the voltage harmonics. As a result, all harmonics result in the net transfer of energy to the load. The current harmonic magnitudes and phases are

$$I_n = \frac{V_n}{R} \quad (20.16)$$

$$\theta_n = \varphi_n \quad \text{so } \cos(\theta_n - \varphi_n) = 1 \quad (20.17)$$

The rms voltage is again

$$(\text{rms voltage}) = \sqrt{V_0^2 + \sum_{n=1}^{\infty} \frac{V_n^2}{2}} \quad (20.18)$$

and the rms current is

$$\begin{aligned} (\text{rms current}) &= \sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}} = \sqrt{\frac{V_0^2}{R^2} + \sum_{n=1}^{\infty} \frac{V_n^2}{2R^2}} \\ &= \frac{1}{R}(\text{rms voltage}) \end{aligned} \quad (20.19)$$

By use of Eq. (20.6), the average power is

$$\begin{aligned} P_{av} &= V_0 I_0 + \sum_{n=1}^{\infty} \frac{V_n I_n}{2} \cos(\varphi_n - \theta_n) \\ &= \frac{V_0^2}{R} + \sum_{n=1}^{\infty} \frac{V_n^2}{2R} \\ &= \frac{1}{R}(\text{rms voltage})^2 \end{aligned} \quad (20.20)$$

Insertion of Eqs. (20.19) and (20.20) into Eq. (20.15) then shows that the power factor is unity. Thus, if the load is linear and purely resistive, then the power factor is unity regardless of the harmonic content of  $v(t)$ . The harmonic content of the load current waveform  $i(t)$  is identical to that of  $v(t)$ , and all harmonics result in the transfer of energy to the load. This raises the possibility that one could construct a power distribution system based on nonsinusoidal waveforms in which the energy is efficiently transferred to the load.

### 20.3.2 Nonlinear Dynamical Load, Sinusoidal Voltage

If the voltage  $v(t)$  contains a fundamental component but no dc component or harmonics, so that  $V_0 = V_2 = V_3 = \dots = 0$ , then harmonics in  $i(t)$  do not result in transmission of net energy to the load. The average power expression, Eq. (20.6), becomes

$$P_{av} = \frac{V_1 I_1}{2} \cos(\varphi_1 - \theta_1) \quad (20.21)$$

However, the harmonics in  $i(t)$  do affect the value of the rms current:

$$(\text{rms current}) = \sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}} \quad (20.22)$$

Hence, as in example 1 (Fig. 20.2), harmonics cause the load to draw more rms current from the source, but not more average power. Increasing the current harmonics does not cause more energy to be transferred to the load, but does cause additional losses in series resistive elements  $R_{series}$ .

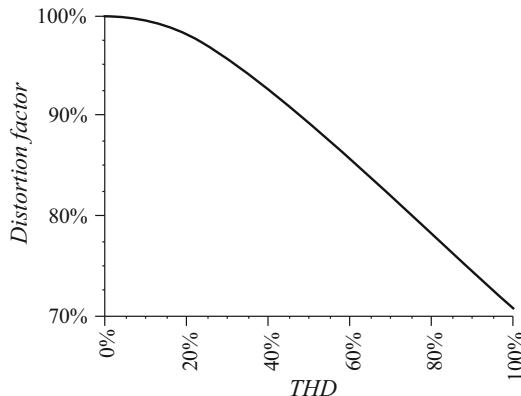
Also, the presence of load dynamics and reactive elements, which causes the phase of the fundamental components of the voltage and current to differ by  $(\theta_1 - \varphi_1)$ , also reduces the power factor. The  $\cos(\varphi_1 - \theta_1)$  term in the average power Eq. (20.21) becomes less than unity. However, the rms value of the current, Eq. (20.22), does not depend on the phase. So shifting the phase of  $i(t)$  with respect to  $v(t)$  reduces the average power without changing the rms voltage or current, and hence the power factor is reduced.

By substituting Eqs. (20.21) and (20.22) into (20.15), we can express the power factor for the sinusoidal voltage in the following form:

$$\begin{aligned} (\text{power factor}) &= \left( \frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}}} \right) (\cos(\varphi_1 - \theta_1)) \\ &= (\text{distortion factor})(\text{displacement factor}) \end{aligned} \quad (20.23)$$

So when the voltage contains no harmonics, then the power factor can be written as the product of two terms. The first, called the *distortion factor*, is the ratio of the rms fundamental component of the current to the total rms value of the current

$$(\text{distortion factor}) = \left( \frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}}} \right) = \frac{(\text{rms fundamental current})}{(\text{rms current})} \quad (20.24)$$



**Fig. 20.5** Distortion factor vs. total harmonic distortion

The second term of Eq. (20.23) is called the *displacement factor*, and is the cosine of the angle between the fundamental components of the voltage and current waveforms.

The *total harmonic distortion* (THD) is defined as the ratio of the rms value of the waveform not including the fundamental, to the rms fundamental magnitude. When no dc is present, this can be written as:

$$(THD) = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \quad (20.25)$$

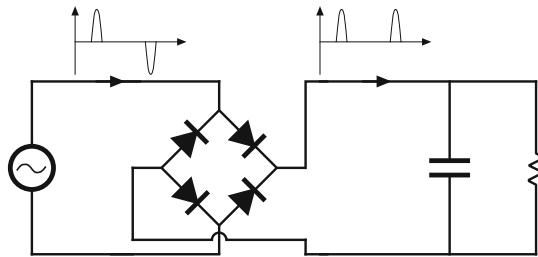
The total harmonic distortion and the distortion factor are closely related. Comparison of Eqs. (20.24) and (20.25), with  $I_0 = 0$ , leads to

$$(\text{distortion factor}) = \frac{1}{\sqrt{1 + (\text{THD})^2}} \quad (20.26)$$

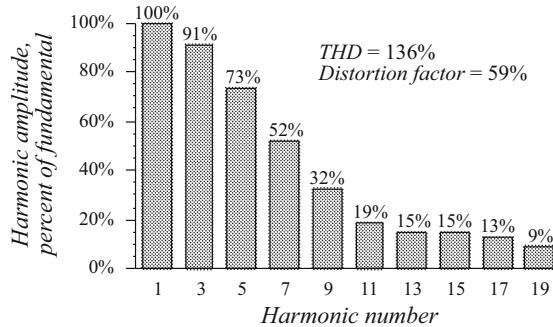
This equation is plotted in Fig. 20.5. The distortion factor of a waveform with a moderate amount of distortion is quite close to unity. For example, if the waveform contains third harmonic whose magnitude is 10% of the fundamental, the distortion factor is 99.5%. Increasing the third harmonic to 20% decreases the distortion factor to 98%, and a 33% harmonic magnitude yields a distortion factor of 95%. So the power factor is not significantly degraded by the presence of harmonics unless the harmonics are quite large in magnitude.

An example of a case in which the distortion factor is much less than unity is the conventional peak-detection rectifier of Fig. 20.6. In this circuit, the ac line current consists of short-duration current pulses occurring at the peak of the voltage waveform. The fundamental component of the line current is essentially in phase with the voltage, and the displacement factor is close to unity. However, the low-order current harmonics are quite large, close in magnitude to that of the fundamental—a typical current spectrum is given in Fig. 20.7. The distortion factor of peak-detection rectifiers is usually in the range 55%–65%. The resulting power factor is similar in value.

In North America, the standard 120 V power outlet is protected by a 15 A circuit breaker. In consequence, the available load power is quite limited. Derating the circuit breaker current



**Fig. 20.6** Conventional peak-detection rectifier



**Fig. 20.7** Typical ac line current spectrum of a single-phase peak-detection rectifier. Harmonics 1 to 19 are shown

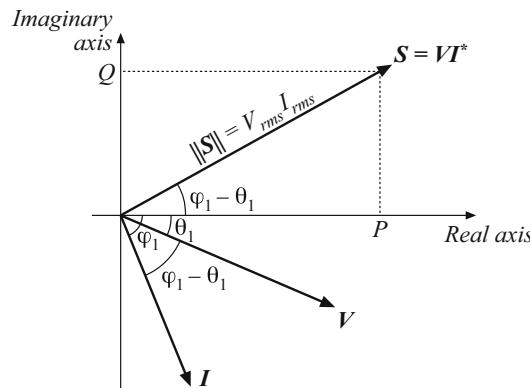
by 20%, assuming typical efficiencies for the dc–dc converter and peak-detection rectifier, and with a power factor of 55%, one obtains the following estimate for the maximum available dc load power:

$$\begin{aligned}
 & (\text{ac voltage}) (\text{derated breaker current}) (\text{power factor}) (\text{rectifier efficiency}) \\
 & = (120\text{V}) \quad (80\% \text{ of } 15 \text{ A}) \quad (0.55) \quad (0.98) \quad (20.27) \\
 & = 776 \text{ W}
 \end{aligned}$$

The less-than-unity efficiency of a dc–dc converter would further reduce the available dc load power. Using a peak-detection rectifier to supply a load power greater than this requires that the user installs higher amperage and/or higher voltage service, which is inconvenient and costly. The use of a rectifier circuit having nearly unity power factor would allow a significant increase in available dc load power:

$$\begin{aligned}
 & (\text{ac voltage}) (\text{derated breaker current}) (\text{power factor}) (\text{rectifier efficiency}) \\
 & = (120\text{V}) \quad (80\% \text{ of } 15\text{A}) \quad (0.99) \quad (0.93) \quad (20.28) \\
 & = 1325\text{W}
 \end{aligned}$$

or almost twice the available power of the peak-detection rectifier. This alone can be a compelling reason to employ high-quality rectifiers in commercial systems.



**Fig. 20.8** Power phasor diagram for a sinusoidal system, illustrating the voltage, current, and complex power phasors

## 20.4 Power Phasors in Sinusoidal Systems

The apparent power is defined as the product of the rms voltage and rms current. Apparent power is easily measured—it is simply the product of the readings of a voltmeter and ammeter placed in the circuit at the given surface. Many power system elements, such as transformers, must be rated according to the apparent power that they are able to supply. The unit of apparent power is the volt-ampere, or VA. The power factor, defined in Eq. (20.15), is the ratio of average power to apparent power.

In the case of sinusoidal voltage and current waveforms, we can additionally define the *complex power*  $S$  and the *reactive power*  $Q$ . If the sinusoidal voltage  $v(t)$  and current  $i(t)$  can be represented by the phasors  $V$  and  $I$ , then the complex power is a phasor defined as

$$S = VI^* = P + jQ \quad (20.29)$$

Here,  $I^*$  is the complex conjugate of  $I$ , and  $j$  is the square root of  $-1$ . The magnitude of  $S$ , or  $\|S\|$ , is equal to the *apparent power*, measured in VA. The real part of  $S$  is the average power  $P$ , having units of watts. The imaginary part of  $S$  is the reactive power  $Q$ , having units of reactive volt-amperes, or VARs.

A phasor diagram illustrating  $S$ ,  $P$ , and  $Q$ , is given in Fig. 20.8. The angle  $(\varphi_1 - \theta_1)$  is the angle between the voltage phasor  $V$  and the current phasor  $I$ .  $(\varphi_1 - \theta_1)$  is additionally the phase of the complex power  $S$ . The power factor in the purely sinusoidal case is therefore

$$\text{power factor} = \frac{P}{\|S\|} = \cos(\varphi_1 - \theta_1) \quad (20.30)$$

It should be emphasized that this equation is valid only for systems in which the voltage and current are purely sinusoidal. The distortion factor of Eq. (20.24) then becomes unity, and the power factor is equal to the displacement factor as in Eq. (20.30).

The reactive power  $Q$  does not lead to net transmission of energy between the source and load. When reactive power is present, the rms current and apparent power are greater than the minimum amount necessary to transmit the average power  $P$ . In an inductor, the current

lags the voltage by  $90^\circ$ , causing the displacement factor to be zero. The alternate storing and releasing of energy in an inductor leads to current flow and nonzero apparent power, but the average power  $P$  is zero. Just as resistors consume real (average) power  $P$ , inductors can be viewed as consumers of reactive power  $Q$ . In a capacitor, the current leads to voltage by  $90^\circ$ , again causing the displacement factor to be zero. Capacitors supply reactive power  $Q$ , and are commonly placed in the utility power distribution system near inductive loads. If the reactive power supplied by the capacitor is equal to the reactive power consumed by the inductor, then the net current (flowing from the source into the capacitor-inductive-load combination) will be in phase with the voltage, leading unity power factor and minimum rms current magnitude.

It will be seen in the next chapter that phase-controlled rectifiers produce a nonsinusoidal current waveform whose fundamental component lags the voltage. This lagging current does not arise from energy storage, but it does nonetheless lead to a reduced displacement factor, and to rms current and apparent power that are greater than the minimum amount necessary to transmit the average power.

## 20.5 Harmonic Currents in Three-Phase Systems

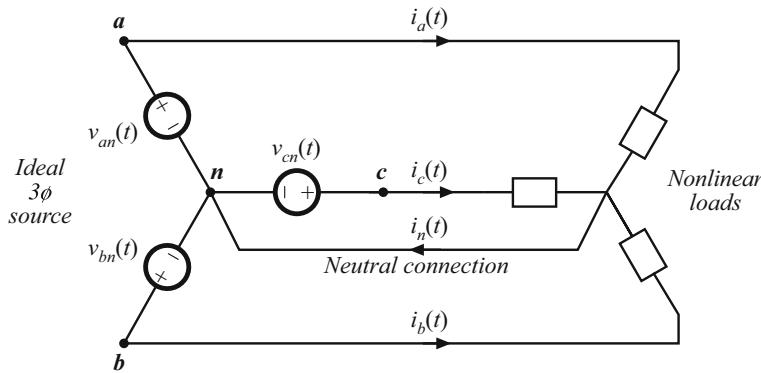
The presence of harmonic currents can also lead to some special problems in three-phase systems. In a four-wire three-phase system, harmonic currents can lead to large currents in the neutral conductors, which may easily exceed the conductor rms current rating. Power factor correction capacitors may experience significantly increased rms currents, causing them to fail. In this section, these problems are examined, and the properties of harmonic current flow in three-phase systems are derived.

### 20.5.1 Harmonic Currents in Three-Phase Four-Wire Networks

Let us consider the three-phase four-wire network of Fig. 20.9. In general, we can express the Fourier series of the line currents and line-neutral voltages as follows:

$$\begin{aligned} i_a(t) &= I_{a0} + \sum_{k=1}^{\infty} I_{ak} \cos(k\omega t - \theta_{ak}) \\ i_b(t) &= I_{b0} + \sum_{k=1}^{\infty} I_{bk} \cos(k(\omega t - 120^\circ) - \theta_{bk}) \\ i_c(t) &= I_{c0} + \sum_{k=1}^{\infty} I_{ck} \cos(k(\omega t + 120^\circ) - \theta_{ck}) \end{aligned} \quad (20.31)$$

$$\begin{aligned} v_{an}(t) &= V_m \cos(\omega t) \\ v_{bn}(t) &= V_m \cos(\omega t - 120^\circ) \\ v_{cn}(t) &= V_m \cos(\omega t + 120^\circ) \end{aligned} \quad (20.32)$$



**Fig. 20.9** Current flow in a three-phase four-wire network

The neutral current is therefore  $i_n = i_a + i_b + i_c$ , or

$$i_n(t) = I_{a0} + I_{b0} + I_{c0} + \sum_{k=1}^{\infty} [I_{ak} \cos(k\omega t - \theta_{ak}) + I_{bk} \cos(k(\omega t - 120^\circ) - \theta_{bk}) + I_{ck} \cos(k(\omega t + 120^\circ) - \theta_{ck})] \quad (20.33)$$

When the load is unbalanced (even though the voltages are balanced and undistorted), we can say little else about the neutral and line currents. If the load is unbalanced and nonlinear, then the line and neutral currents may contain harmonics of any order, including even and triplen harmonics.

Equation (20.33) is considerably simplified in the case where the loads are balanced. A balanced nonlinear load is one in which  $I_{ak} = I_{bk} = I_{ck} = I_k$  and  $\theta_{ak} = \theta_{bk} = \theta_{ck} = \theta_k$ , for all  $k$ ; that is, the harmonics of the three phases all have equal amplitudes and phase shifts. In this case, Eq. (20.33) reduces to

$$i_n(t) = 3I_0 + \sum_{k=3,6,9,\dots}^{\infty} 3I_k \cos(k\omega t - \theta_k) \quad (20.34)$$

Hence, the fundamental and most of the harmonics cancel out, and do not appear in the neutral conductor. Thus, it is in the interests of the utility to balance their nonlinear loads as well as their harmonics.

But not all of the harmonics cancel out of Eq. (20.34): the dc and *triplen* (triple- $n$ , or  $3, 6, 9, \dots$ ) harmonics add rather than cancel. The rms neutral current is

$$i_{n,rms} = 3 \sqrt{I_0^2 + \sum_{k=3,6,9,\dots}^{\infty} \frac{I_k^2}{2}} \quad (20.35)$$

#### Example

A balanced nonlinear load produces line currents containing fundamental and 20% third harmonic:  $i_{an}(t) = I_1 \cos(\omega t - \theta_1) + 0.2I_1 \cos(3\omega t - \theta_3)$ . Find the rms neutral current, and compare its amplitude to the rms line current amplitude.

*Solution:*

$$\begin{aligned} i_{n,rms} &= 3 \sqrt{\frac{(0.2I_1)^2}{2}} = \frac{0.6I_1}{\sqrt{2}} \\ i_{1,rms} &= \sqrt{\frac{I_1^2 + (0.2I_1)^2}{2}} = \frac{I_1}{\sqrt{2}} \sqrt{1+0.04} \approx \frac{I_1}{\sqrt{2}} \end{aligned} \quad (20.36)$$

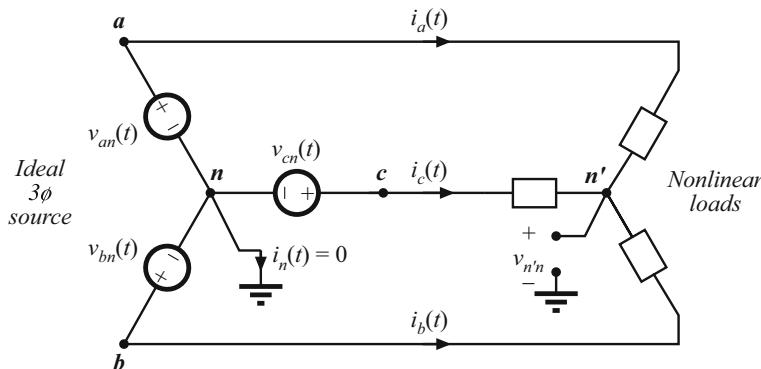
So the neutral current magnitude is 60% of the line current magnitude! The triplen harmonics in the three phases add, such that 20% third harmonic leads to 60% third harmonic neutral current. Yet the presence of the third harmonic has very little effect on the rms value of the line current. Significant unexpected neutral current flows.

### 20.5.2 Harmonic Currents in Three-Phase Three-Wire Networks

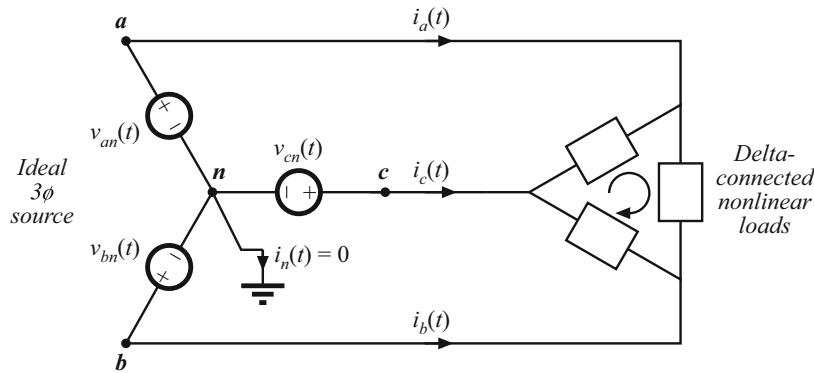
If there is no neutral connection to the wye-connected load, as in Fig. 20.10, then  $i_n(t)$  must be zero. If the load is balanced, then Eq. (20.34) still applies, and therefore the dc and triplen harmonics of the load currents must be zero. Therefore, the line currents  $i_a$ ,  $i_b$ , and  $i_c$  cannot contain triplen or dc harmonics. What happens is that a voltage is induced at the load neutral point  $n'$ , containing dc and triplen harmonics, which eliminates the triplen and dc load current harmonics.

This result is true only when the load is balanced. With an unbalanced load, all harmonics can appear in the line currents, including triplen and dc. In practice, the load is never exactly balanced, and some small amounts of third harmonic line currents are measured.

With a delta-connected load as in Fig. 20.11, there is also no neutral connection, so the line currents cannot contain triplen or dc components. But the loads are connected line-to-line, and are excited by undistorted sinusoidal voltages. Hence triplen harmonic and dc currents do, in general, flow through the nonlinear loads. Therefore, these currents simply circulate around the delta. If the load is balanced, then again no triplen harmonics appear in the line currents.



**Fig. 20.10** Current flow in a three-phase three-wire wye-connected network



**Fig. 20.11** A balanced nonlinear delta-connected load may generate triplen current harmonics. These harmonics circulate around the delta, but do not flow through the lines if the load phases are balanced

### 20.5.3 Harmonic Current Flow in Power Factor Correction Capacitors

Harmonic currents tend to flow through shunt-connected power factor correction capacitors. To some extent, this is a good thing because the capacitors tend to low-pass filter the power system currents, and prevent nonlinear loads from polluting the entire power system. The flow of harmonic currents is then confined to the nonlinear load and local power factor correction capacitors, and voltage waveform distortion is reduced. High-frequency harmonic currents tend to flow through shunt capacitors because the capacitor impedance decreases with frequency, while the inductive impedance of transmission lines increases with frequency. In this sense, power factor correction capacitors mitigate the effects of harmonic currents arising from nonlinear loads in much the same way that they mitigate the effects of reactive currents that arise from inductive loads.

But the problem is that the power factor correction capacitors may not be rated to handle these harmonic currents, and hence there is a danger that the capacitors may overheat and fail when they are exposed to significant harmonic currents. The loss in capacitors is modeled using an *equivalent series resistance* (ESR) as shown in Fig. 20.12. The ESR models dielectric loss (hysteresis of the dielectric  $D - E$  loop), contact resistance, and foil and lead resistances. Power loss occurs, equal to  $i_{rms}^2(\text{esr})$ . Dielectric materials are typically poor conductors of heat, so a moderate amount of power loss can cause a large temperature rise in the center of the capacitor. In consequence, the rms current must be limited to a safe value.

Typical power factor correction capacitors are rated by voltage  $V$ , frequency  $f$ , and reactive power in kVARs. These ratings are computed from the capacitance  $C$  and safe rms current  $I_{rms}$ , assuming undistorted sinusoidal waveforms, as follows:

$$\text{rated rms voltage } V_{rms} = \frac{I_{rms}}{2\pi f C} \quad (20.37)$$



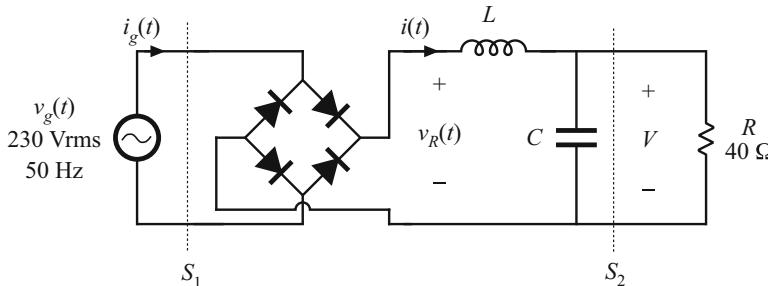
**Fig. 20.12** Capacitor equivalent circuit. Losses are modeled by an equivalent series resistance (ESR)

$$\text{rated rms voltage} = \frac{I_{rms}^2}{2\pi f C} \quad (20.38)$$

In an undistorted system, the rms current, and hence also the capacitor ESR loss, cannot increase unless the rms voltage is also increased. But high-frequency harmonics can lead to larger rms currents without an increased voltage. Any harmonics that flow result in increased rms current beyond the expected value predicted by Eq. (20.37). If the capacitor is not rated to handle additional power loss, then failure or premature aging can occur.

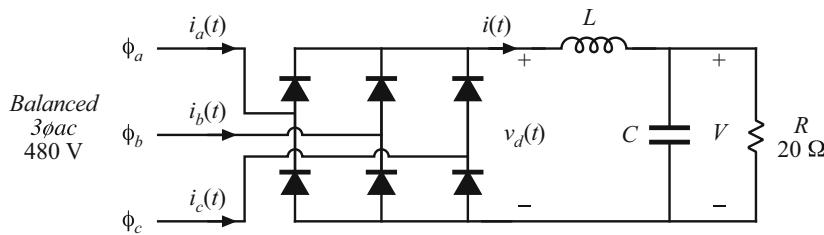
## PROBLEMS

- 20.1** Passive rectifier circuit. In the passive rectifier circuit of Fig. 20.13,  $L$  is very large, such that the inductor current  $i(t)$  is essentially dc. All components are ideal.



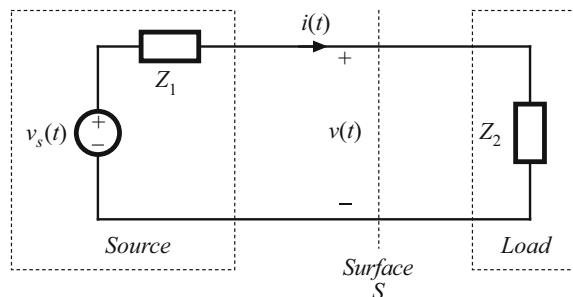
**Fig. 20.13** Passive rectifier circuit of Problem 20.1

- (a) Determine the dc output voltage, current, and power.
  - (b) Sketch the ac line current waveform  $i_g(t)$  and the rectifier output voltage waveform  $v_R(t)$ .
  - (c) Determine the ac line current rms magnitude, fundamental rms magnitude, and third harmonic rms magnitude. If it is required that the third harmonic magnitude be less than 2.3 A rms, would this rectifier network conform?
  - (d) Determine the power factor, measured at surfaces  $S_1$  and  $S_2$ .
- 20.2** The three-phase rectifier of Fig. 20.14 is connected to a balanced 60 Hz  $3\phi$  ac480V (rms, line-line) sinusoidal source as shown. All elements are ideal. The inductance  $L$  is large, such that the current  $i(t)$  is essentially constant, with negligible 360 Hz ripple.
- (a) Sketch the waveform  $v_d(t)$ .
  - (b) Determine the dc output voltage  $V$
  - (c) Sketch the line current waveforms  $i_a(t)$ ,  $i_b(t)$ , and  $i_c(t)$ .
  - (d) Find the Fourier series of  $i_a(t)$ .
  - (e) Find the distortion factor, displacement factor, power factor, and line current THD.



**Fig. 20.14** Three-phase rectifier circuit of Problem 20.2

**20.3** Harmonic pollution police. In the network of Fig. 20.15, voltage harmonics are observed at the indicated surface. The object of this problem is to decide whether to blame the source or the load for the observed harmonic pollution. Either the source element or the load element contains a nonlinearity that generates harmonics, while the other element is linear.



**Fig. 20.15** Single-phase power system of Problems 20.3 to 20.5

- (a) Consider first the case where the load is a passive linear impedance  $Z_2(s)$ , and hence its phase lies in the range  $-90^\circ \leq \angle Z_2(i\omega) \leq +90^\circ$  for all positive  $\omega$ . The source generates harmonics. Express the average power  $P$  in the form

$$P = \sum_{n=0}^{\infty} P_n$$

where  $P_n$  is the average power transmitted to the load by harmonic number  $n$ . What can you say about the polarities of the  $P_n$ s?

- (b) Consider next the case where the load is nonlinear, while the source is linear and can be modeled by a Thevenin-equivalent sinusoidal voltage source and linear impedance  $Z_1(s)$ . Again express the average power  $P$  as a sum of average powers, as in part (a). What can you say about the polarities of the  $P_n$ s in this case?
- (c) The following Fourier series are measured:

Harmonic number	$v(t)$		$i(t)$	
	Magnitude	Phase	Magnitude	Phase
1	230 V	0°	6 A	-20°
3	20 V	180°	4 A	20°
5	8 V	60°	1 A	-110°

Who do you accuse? Explain your reasoning.

- 20.4** For the network and waveforms of Problem 20.3, determine the power factor at the indicated surface, and the average power flowing to the load. Harmonics higher in frequency than the fifth harmonic are negligible in magnitude.

- 20.5** Repeat Problem 20.3(c), using the following Fourier series:

Harmonic number	$v(t)$		$i(t)$	
	Magnitude	Phase	Magnitude	Phase
1	120 V	0°	5 A	25°
3	4 V	60°	0.5 A	40°
5	2 V	-160°	0.2 A	-100°

- 20.6** A balanced three-phase wye-connected load is constructed using a  $20\ \Omega$  resistor in each phase. This load is connected to a balanced three-phase wye-connected voltage source, whose fundamental voltage component is 380 Vrms line-to-line. In addition, each (line-to-neutral) voltage source produces third and fifth harmonics. Each harmonic has amplitude 20 Vrms, and is in phase with the (line-to-neutral) fundamental.

- (a) The source and load neutral points are connected, such that a four-wire system is obtained. Find the Fourier series of the line currents and the neutral current.
- (b) The neutral connection is broken, such that a three-wire system is obtained. Find the Fourier series of the line currents. Also find the Fourier series of the voltage between the source and load neutral points.



## Pulse-Width Modulated Rectifiers

To obtain low ac line current THD, the passive techniques described in the previous chapter rely on low-frequency transformers and/or reactive elements. The large size and weight of these elements are objectionable in many applications. This chapter covers active techniques that employ converters having switching frequencies much greater than the ac line frequency. The reactive elements and transformers of these converters are small, because their sizes depend on the converter switching frequency rather than the ac line frequency.

Instead of making do with conventional diode rectifier circuits, and dealing after-the-fact with the resulting low-frequency harmonics, let us consider now how to build a rectifier that behaves as ideally as possible, without generation of line current harmonics. In this chapter, the properties of the *ideal rectifier* are explored, and a model is described. The ideal rectifier presents an effective resistive load to the ac power line; hence, if the supplied ac voltage is sinusoidal, then the current drawn by the rectifier is also sinusoidal and is in phase with the voltage. Converters that approximate the properties of the ideal rectifier are sometimes called *power factor corrected*, because their input power factor is essentially unity [244].

The boost converter, as well as a variety of other converters, can be controlled such that a near-ideal rectifier system is obtained. This is accomplished by control of a high-frequency switching converter, such that the ac line current waveform follows the applied ac line voltage. Both single-phase and three-phase rectifiers can be constructed using PWM techniques. A typical dc power supply system that is powered by the single-phase ac utility contains three major power-processing elements. First, a high-frequency converter with a wide-bandwidth input current controller functions as a near-ideal rectifier. Second, an energy storage capacitor smooths the pulsating power at the rectifier output, and a low-bandwidth controller causes the average input power to follow the power drawn by the load. Finally, a dc–dc converter provides a well-regulated dc voltage to the load. In this chapter, single-phase rectifier systems are discussed, expressions for rms currents are derived, and various converter approaches are compared.

The techniques developed in earlier chapters for modeling and analysis of dc–dc converters are extended in this chapter to treat the analysis, modeling, and control of low-harmonic rectifiers. The CCM models of Chap. 3 are used to compute the average losses and efficiency of CCM PWM converters operating as rectifiers. The results yield insight that is useful in power stage design. Several converter control schemes are known, including peak current programming, average current control, critical conduction mode control, and nonlinear carrier control. Ac modeling of the rectifier control system is also covered.

## 21.1 Properties of the Ideal Rectifier

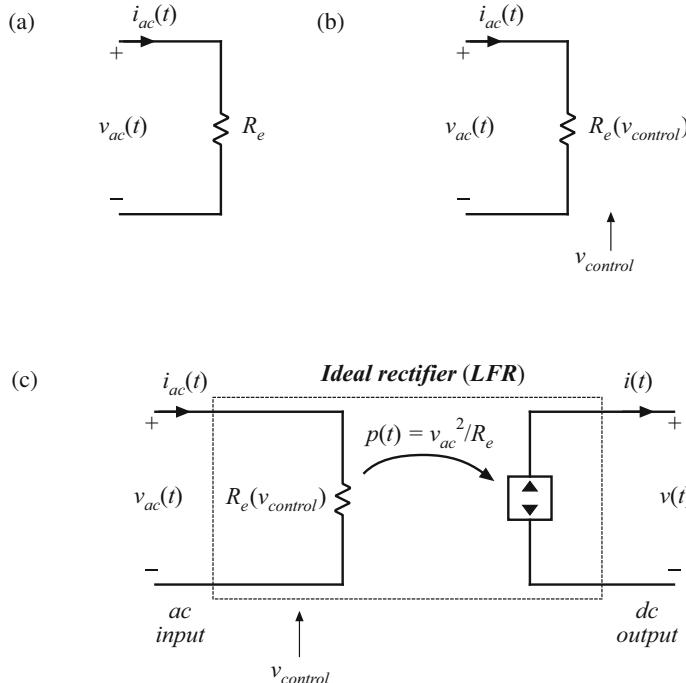
It is desired that the ideal single-phase rectifier presents a resistive load to the ac system. The ac line current and voltage will then have the same waveshape and will be in phase. Unity power factor rectification is the result. Thus, the rectifier input current  $i_{ac}(t)$  should be proportional to the applied input voltage  $v_{ac}(t)$ :

$$i_{ac}(t) = \frac{v_{ac}(t)}{R_e} \quad (21.1)$$

where  $R_e$  is the constant of proportionality. An equivalent circuit for the ac port of an ideal rectifier is therefore an effective resistance  $R_e$ , as shown in Fig. 21.1a.  $R_e$  is also known as the *emulated resistance*. It should be noted that the presence of  $R_e$  does not imply the generation of heat: the power apparently “consumed” by  $R_e$  is actually transferred to the rectifier dc output port.  $R_e$  simply models how the ideal rectifier loads the ac power system.

Output regulation is accomplished by variation of the effective resistance  $R_e$ , and hence the value of  $R_e$  must depend on a control signal  $v_{control}(t)$  as in Fig. 21.1b. This allows variation of the rectifier power throughput, since the average power consumed by  $R_e$  is

$$P_{av} = \frac{V_{ac,rms}^2}{R_e(v_{control})} \quad (21.2)$$



**Fig. 21.1** Development of the ideal rectifier equivalent circuit model: (a) input port resistor emulation; (b) the value of the emulated resistance, and hence the power throughput, is controllable; (c) output port power source characteristic, and complete model

Note that changing  $R_e$  results in a time-varying system, with generation of harmonics. To avoid generation of significant amounts of harmonics and degradation of the power factor, variations in  $R_e$  and in the control input must be slow with respect to the ac line frequency.

To the extent that the rectifier is lossless and contains negligible internal energy storage, the instantaneous power flowing into  $R_e$  must appear at the rectifier output port. Note that the instantaneous power throughput

$$p(t) = \frac{v_{ac}^2(t)}{R_e(v_{control}(t))} \quad (21.3)$$

is dependent only on  $v_{ac}(t)$  and the control input  $v_{control}(t)$ , and is independent of the characteristics of the load connected to the output port. Hence, the output port must behave as a source of constant power, obeying the relationship

$$v(t)i(t) = p(t) = \frac{v_{ac}^2(t)}{R_e} \quad (21.4)$$

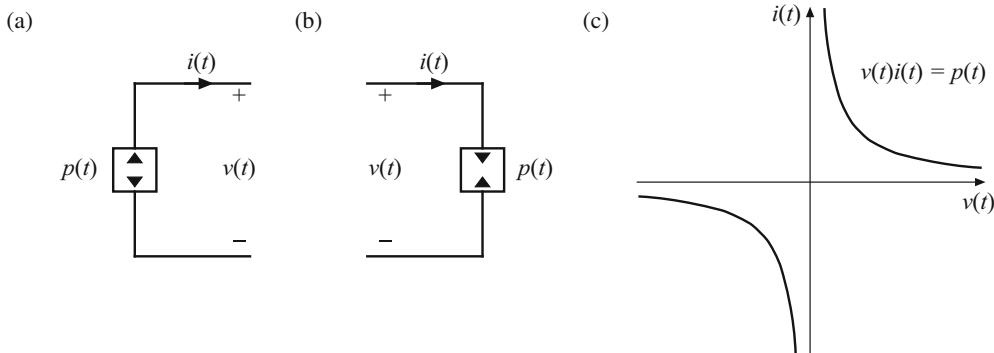
The *dependent power source* symbol of Fig. 21.2a is used to denote such an output characteristic. As illustrated in Fig. 21.1c, the output port is modeled by a power source that is dependent on the instantaneous power flowing into  $R_e$ .

Thus, a two-port model for the ideal unity-power-factor single-phase rectifier is as shown in Fig. 21.1c [132, 133, 245]. The two port model is also called a *loss-free resistor* (LFR) because (1) its input port obeys Ohm's law, and (2) power entering the input port is transferred directly to the output port without loss of energy. The defining equations of the LFR are as follows:

$$i_{ac}(t) = \frac{v_{ac}(t)}{R_e(v_{control})} \quad (21.5)$$

$$v(t)i(t) = p(t) \quad (21.6)$$

$$p(t) = \frac{v_{ac}^2(t)}{R_e(v_{control})} \quad (21.7)$$



**Fig. 21.2** The dependent power source: (a) power source schematic symbol, (b) power sink schematic symbol, (c)  $i$ - $v$  characteristic of power source

When the LFR output port is connected to a resistive load of value  $R$ , the dc output rms voltages and currents  $V_{rms}$  and  $I_{rms}$  are related to the ac input rms voltages and currents  $V_{ac,rms}$  and  $I_{ac,rms}$  as follows:

$$\frac{V_{rms}}{V_{ac,rms}} = \sqrt{\frac{R}{R_e}} \quad (21.8)$$

$$\frac{I_{ac,rms}}{I_{rms}} = \sqrt{\frac{R}{R_e}} \quad (21.9)$$

The properties of the power source and loss-free resistor network are discussed in Chap. 15. Regardless of the specific converter implementation, any single-phase rectifier having near-ideal properties can be modeled using the LFR two-port model.

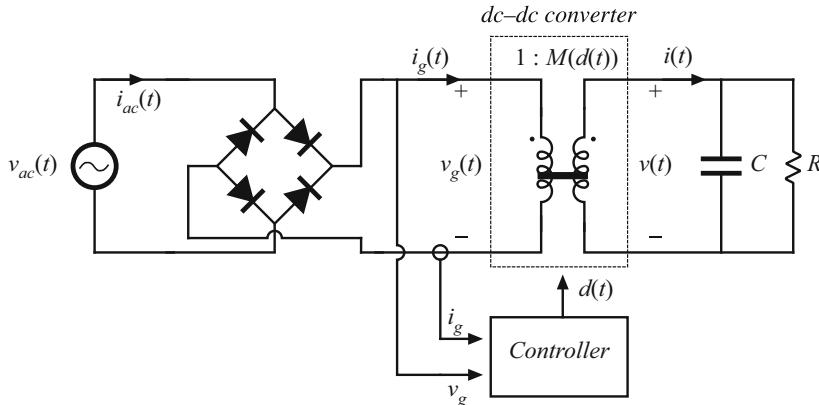
## 21.2 Realization of a Near-Ideal Rectifier

Feedback can be employed to cause a converter that exhibits controlled dc transformer characteristics to obey the LFR equations. In the single-phase case, the simplest and least expensive approach employs a full-wave diode rectifier network, cascaded by a dc–dc converter, as in Fig. 21.3. The dc–dc converter is represented by an ideal dc transformer, as discussed in Chap. 3. A control network varies the duty cycle, as necessary to cause the converter input current  $i_g(t)$  to be proportional to the applied input voltage  $v_g(t)$  as in Eq. (21.1). The effective turns ratio of the ideal transformer then varies with time. Ideal waveforms are illustrated in Fig. 21.4. If the applied input voltage  $v_{ac}(t)$  is sinusoidal,

$$v_{ac}(t) = V_M \sin(\omega t) \quad (21.10)$$

then the rectified voltage  $v_g(t)$  is

$$v_g(t) = V_M |\sin(\omega t)| \quad (21.11)$$



**Fig. 21.3** Synthesis of an ideal rectifier by varying the duty cycle of a PWM dc–dc converter

It is desired that the converter output voltage be a constant dc value  $v(t) = V$ . The converter conversion ratio must therefore be

$$M(d(t)) = \frac{v(t)}{v_g(t)} = \frac{V}{V_M |\sin(\omega t)|} \quad (21.12)$$

This expression neglects the converter dynamics. As can be seen from Fig. 21.4, the controller must cause the conversion ratio to vary between infinity (at the ac line voltage zero crossings) and some minimum value  $M_{min}$  (at the peaks of the ac line voltage waveform).  $M_{min}$  is given by

$$M_{min} = \frac{V}{V_M} \quad (21.13)$$

Any converter topology whose ideal conversion ratio can be varied between these limits can be employed in this application.

To the extent that the dc-dc converter is ideal (i.e., if the losses can be neglected and there is negligible low-frequency energy storage), the instantaneous input and output powers are equal. Hence, the output current  $i(t)$  in Fig. 21.3 is given by

$$i(t) = \frac{v_g(t)i_g(t)}{V} = \frac{v_g^2(t)}{VR_e} \quad (21.14)$$

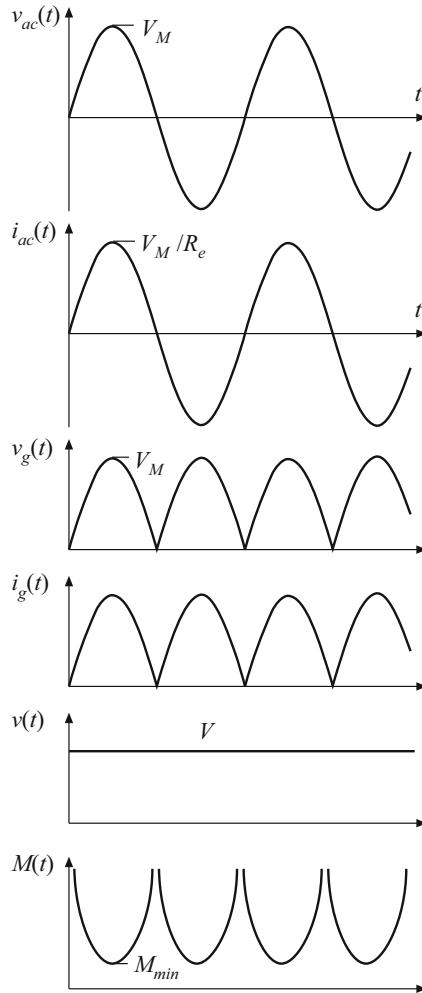
Substitution of Eq. (21.11) into Eq. (21.14) then leads to

$$\begin{aligned} i(t) &= \frac{V_M^2}{VR_e} \sin^2(\omega t) \\ &= \frac{V_M^2}{2VR_e} (1 - \cos(2\omega t)) \end{aligned} \quad (21.15)$$

Hence, the converter output current contains a dc component and a component at the second harmonic of the ac line frequency. One of the functions of capacitor  $C$  in Fig. 21.3 is to filter out the second harmonic component of  $i(t)$ , so that the load current (flowing through resistor  $R$ ) is essentially equal to the dc component

$$I = \langle i(t) \rangle_{T_L} = \frac{V_M^2}{2VR_e} \quad (21.16)$$

where  $T_L$  is the period of the applied ac line voltage.



**Fig. 21.4** Waveforms of the rectifier system of Fig. 21.3

The average power is

$$P = \frac{V_M^2}{2R_e} \quad (21.17)$$

The above equations are generally valid for PWM converters used as single-phase low-harmonic rectifiers.

### 21.2.1 CCM Boost Converter

A system based on the CCM boost converter is illustrated in Fig. 21.5 [244, 246, 247]. Ideally, the boost converter can produce any conversion ratio between one and infinity. Hence, the boost converter is capable of producing the  $M(d(t))$  given by Eq. (21.12), provided that  $V \geq V_M$ . Further, the boost converter can produce very low THD, with better transistor utilization than other approaches.

If the boost converter operates in continuous conduction mode, and if the inductor is small enough that its influence on the low-frequency components of the converter waveforms is negligible, then the duty ratio should follow  $M(d(t)) = 1/(1 - d(t))$ . This implies that the duty ratio should follow the function

$$d(t) = 1 - \frac{v_g(t)}{V} \quad (21.18)$$

This expression is true only in the continuous conduction mode. The boost converter operates in the continuous conduction mode provided that the inductor current ripple

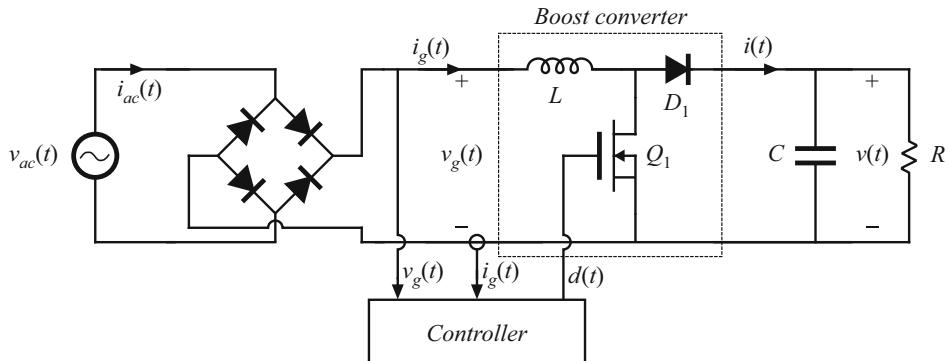
$$\Delta i_g(t) = \frac{v_g(t)d(t)T_s}{2L} \quad (21.19)$$

is greater than the average inductor current, or

$$\langle i_g(t) \rangle_{T_s} = \frac{v_g(t)}{R_e} \quad (21.20)$$

Hence, the converter operates in CCM when

$$\langle i_g(t) \rangle_{T_s} > \Delta i_g(t) \Rightarrow d(t) < \frac{2L}{R_e T_s} \quad (21.21)$$



**Fig. 21.5** Rectifier system based on the boost converter

Substitution of Eq. (21.18) into (21.21) and solution for  $R_e$  leads to

$$R_e < \frac{2L}{T_s(1 - \frac{v_g(t)}{V})} \quad \text{for CCM} \quad (21.22)$$

Since  $v_g(t)$  varies according to Eq. (21.11), Eq. (21.22) may be satisfied at some points on the ac line cycle, and not at others. Since  $0 \leq v_g(t) \leq V_M$ , we can conclude that the converter operates in CCM over the entire ac line cycle when

$$R_e < \frac{2L}{T_s} \quad (21.23)$$

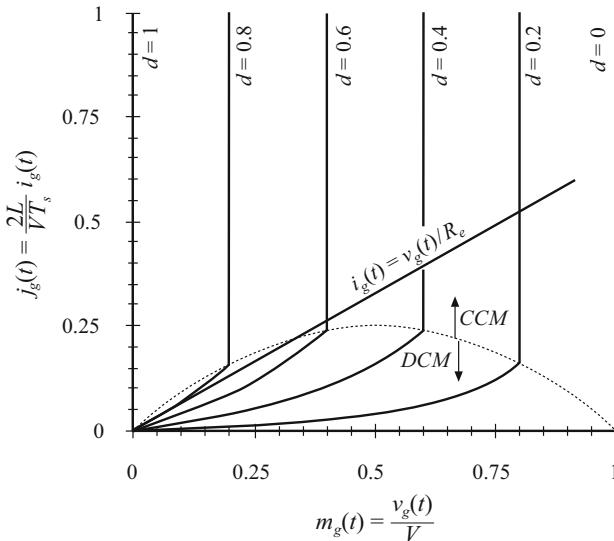
Equations (21.18) and (21.22) then hold for all  $t$ . The converter always operates in DCM when

$$R_e > \frac{2L}{T_s \left(1 - \frac{V_M}{V}\right)} \quad (21.24)$$

For  $R_e$  between these limits, the converter operates in DCM when  $v_g(t)$  is near zero, and in CCM when  $v_g(t)$  approaches  $V_M$ .

The static input characteristics of the open-loop boost converter are sketched in Fig. 21.6. The input current  $i_g(t)$  is plotted vs. input voltage  $v_g(t)$ , for various duty cycles  $d(t)$ . In CCM, the input characteristics of the boost converter are described by

$$\frac{v_g(t)}{V} = 1 - d(t) \quad \text{in CCM} \quad (21.25)$$



**Fig. 21.6** Static input characteristics of the boost converter. A typical linear resistive input characteristic is superimposed

To obtain a general plot, we can normalize the input current and input voltage as follows:

$$m_g(t) = \frac{v_g(t)}{V} \quad (21.26)$$

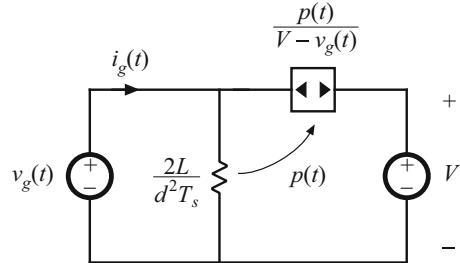
$$j_g(t) = \frac{2L}{VT_s} i_g(t) \quad (21.27)$$

Equation (21.25) then becomes

$$m_g(t) = 1 - d(t) \quad (21.28)$$

This equation is independent of the input current  $i_g(t)$ , and hence is represented by vertical lines in Fig. 21.6.

**Fig. 21.7** Averaged equivalent circuit model of the boost converter operating in DCM, derived in Chap. 15



To derive the boost input characteristic for DCM operation, we can solve the steady-state equivalent circuit model of Fig. 15.16b (reproduced in Fig. 21.7). *Beware:* the natural DCM effective resistance of Chap. 15,  $R_e = 2L/d^2T_s$ , does not necessarily coincide with the emulated resistance  $R_e = v_g/i_g$  of Eq. (21.1). In this chapter, the quantity  $R_e$  is defined according to Eq. (21.1). Solution of Fig. 21.7 for the input current  $i_g(t)$  leads to:

$$i_g(t) = \frac{v_g(t)}{\left(\frac{2L}{d^2 T_s}\right)} + \frac{p(t)}{V - v_g(t)} \quad (21.29)$$

The instantaneous power consumed by the effective resistor in the model of Fig. 21.7 is

$$p(t) = \frac{v_g^2(t)}{\left(\frac{2L}{d^2 T_s}\right)} \quad (21.30)$$

Substitution of Eq. (21.30) into Eq. (21.29) and simplification leads to

$$\frac{2L}{VT_s} i_g(t) \left(1 - \frac{v_g(t)}{V}\right) = d^2(t) \frac{v_g(t)}{V} \quad \text{in DCM} \quad (21.31)$$

Normalization of this equation according to Eqs. (21.26) and (21.27) yields

$$j_g(t) \left(1 - m_g(t)\right) = d^2 m_g(t) \quad (21.32)$$

This equation describes the curved (DCM) portions of the Fig. 21.6 input characteristics, for low  $i_g(t)$ .

To express the CCM/DCM mode boundary as a function of  $v_g(t)$  and  $i_g(t)$ , Eqs. (21.1) and (21.22) can be combined, leading to

$$\frac{2L}{VT_s} i_g(t) > \left( \frac{v_g(t)}{V} \right) \left( 1 - \frac{v_g(t)}{V} \right) \quad \text{for CCM} \quad (21.33)$$

Normalization of this equation, according to Eqs. (21.26) and (21.27), results in

$$j_g(t) > m_g(t)(1 - m_g(t)) \quad \text{for CCM} \quad (21.34)$$

This equation describes a parabola having roots at  $m_g = 0$  and  $m_g = 1$ , with the maximum value  $j_g = 0.25$  at  $m_g = 0.5$ . The mode boundary equation is plotted as a dashed line in Fig. 21.6.

The complete boost converter input characteristics in Fig. 21.6 have been plotted using Eqs.(21.28), (21.32), and (21.34). Figure 21.6 also illustrates the desired linear resistive input characteristic, Eq. (21.1). For the value of  $R_e$  illustrated, the converter operates in DCM for  $v_g(t)$  near zero, and in CCM for  $v_g(t)$  near  $V_M$ . The intersections of boost input characteristics with the desired linear input characteristic illustrate how the controller must choose the duty cycle at various values of  $v_g(t)$ .

Other converters capable of producing the  $M(d(t))$  of Eq. (21.12) include the buck-boost, SEPIC, and Ćuk converters. The boost, SEPIC, and Ćuk converters share the desirable property of nonpulsating input current, and hence require minimal input EMI filtering. The SEPIC produces a non-inverted output voltage. Isolated versions of these converters (see Chap. 6) are also sometimes employed [248–250]. Schemes involving the parallel resonant converter, as well as several types of quasi-resonant converters, are also documented in the literature [251–254].

The open-loop boost converter, when operated in discontinuous conduction mode, is also sometimes used as an approximation of an ideal rectifier. The DCM effective resistance  $2L/d^2(t)T_s$  of Fig. 21.7 is then taken as an approximation of the desired emulated resistance of Eq. (21.1). The model differs from that of the ideal rectifier model of Fig. 21.1c in that the power source is connected between the input and output terminals. As a result, harmonics are present in the input current waveform. For example, if  $v_g(t)$  is a rectified sinusoid, then the current through the effective resistance  $2L/d^2(t)T_s$  will also be a rectified sinusoid. However, the input current  $\langle i_g(t) \rangle_{T_s}$  is now equal to the sum of the current through  $R_e$  and the current flowing through the power source element. Since the power source is a nonlinear element,  $\langle i_g(t) \rangle_{T_s}$  contains harmonics. For large  $C$ , the output voltage is essentially constant. The input current waveform is then given by Eq. (21.31). If  $V$  is sufficiently large, then the term  $(1 - v_g(t)/V)$  is approximately equal to one, and the harmonics in  $\langle i_g(t) \rangle_{T_s}$  are small. The zero crossings of  $v_g(t)$ ,  $p(t)$ , and  $\langle i_g(t) \rangle_{T_s}$  coincide. So although the DCM boost converter generates some current harmonics, it is nonetheless possible to construct a low harmonic rectifier that meets harmonic limits. Again, this approach has the disadvantages of the increased peak currents of DCM, and the need for additional filtering of the high-frequency pulsating input currents.

A similar approach is to operate the boost converter at the boundary between the continuous and discontinuous conduction modes. This approach is known as “critical conduction mode” operation. It eliminates the distortion mechanism described above, but requires variable switching-frequency control. This approach is quite popular at low-power levels, and is described further in Sect. 21.3.3.

Other converters not capable of producing the  $M(d(t))$  of Eq. (21.12), such as the buck converter, are sometimes employed as the dc–dc converter of Fig. 21.3. Distortion of the ac line current waveform must then occur. Nonetheless, at low-power levels it may be possible to meet the applicable ac line current harmonic standards using such an approach.

### 21.2.2 Simulation Example: DCM Boost Rectifier

When a boost DCM converter operates at a constant switch duty cycle, the input current approximately follows the input voltage. The DCM effective resistance  $2L/d^2(t)T_s$  is an approximation of the emulated resistance  $R_e$  of the DCM boost rectifier. Ac line current harmonics are not zero, but the rectifier can still be designed to meet harmonic limits. In this section we consider a DCM boost rectifier example and test its performance by simulation.

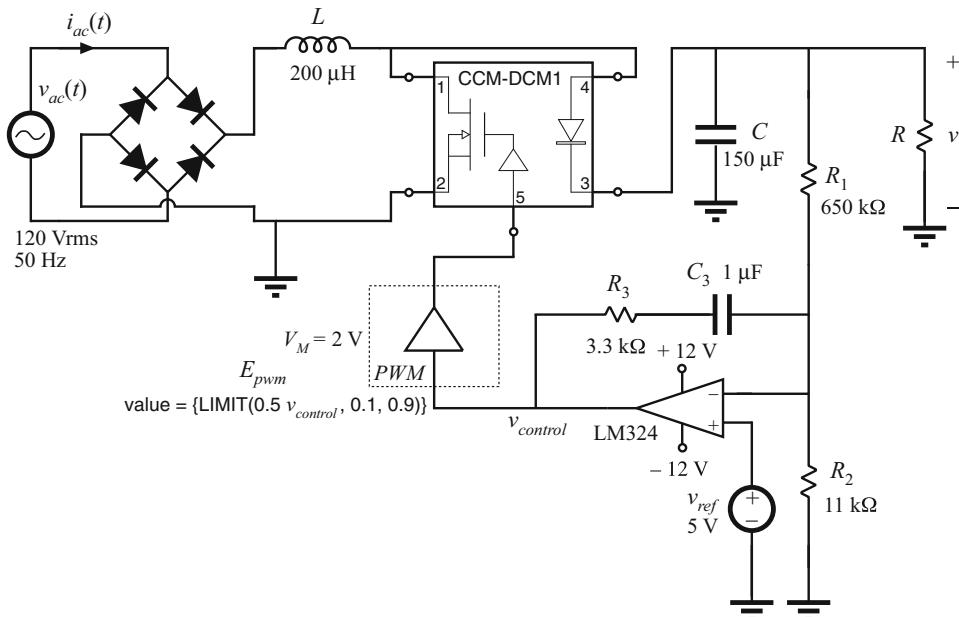
An averaged circuit model of the boost DCM rectifier is shown in Fig. 21.8. Full-wave rectified 120 Vrms, 50 Hz ac line voltage is applied to the input of the boost converter. The converter switches are replaced by the CCM-DCM1 averaged switch subcircuit. It is desired to regulate the dc output voltage at  $V = 300$  V at output power up to  $P_{out} = 120$  W across the load  $R$ . The switching frequency is  $f_s = 100$  kHz. Let us select the inductance  $L$  so that the converter always operates in DCM. From Eq. (21.24), the condition for DCM is as follows:

$$L < \frac{\left(1 - \frac{V_M}{V}\right)R_e}{2f_s} \quad (21.35)$$

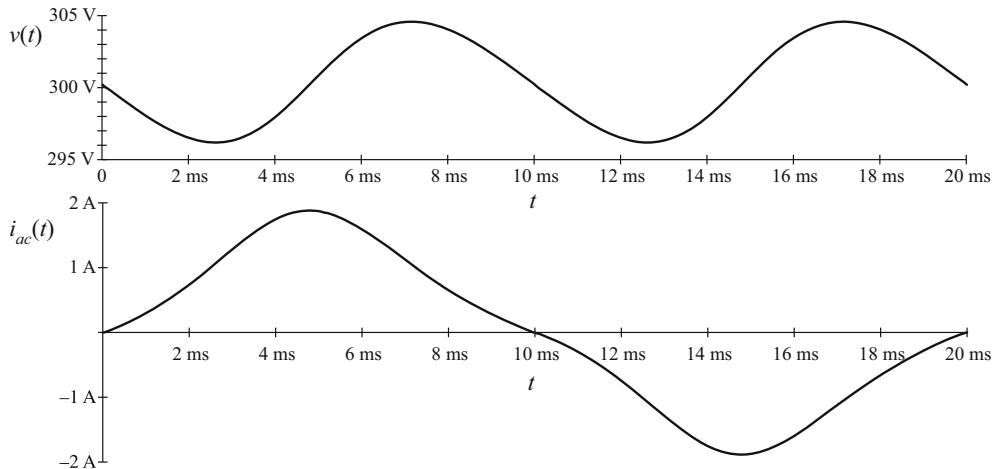
where  $R_e$  is the emulated resistance of the rectifier and  $V_M$  is the peak of the ac line voltage. When line current harmonics and losses are neglected, the rectifier emulated resistance  $R_e$  at the specified load power  $P$  is

$$R_e = \frac{V_M^2}{2P} \quad (21.36)$$

Given  $V_M = 170$  V and  $R_e$  found from Eq. (21.36), Eq. (21.35) gives  $L < 260\mu H$ . The selected inductance is  $L = 200\mu H$ . A low-bandwidth voltage feedback loop is closed around the



**Fig. 21.8** DCM boost rectifier example



**Fig. 21.9** Output voltage and ac line current in the DCM boost rectifier example

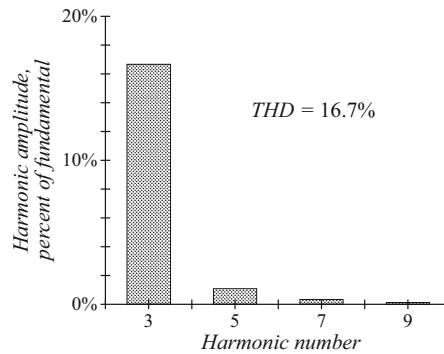
converter to regulate the dc output voltage. The output voltage is sensed and compared to the reference  $v_{ref}$ . A PI compensator is constructed around the LM324 op amp. The output  $v_{control}$  of the compensator is the input to the pulse-width modulator. By adjusting the switch duty ratio  $d$ ,  $v_{control}$  adjusts the emulated resistance  $R_e = 2L/d^2T_s$  of the rectifier, and thereby controls the power taken from the ac line. In steady state, the input power matches the output power. The dc output voltage  $V$  is regulated at the value set by the reference voltage  $v_{ref}$  and the voltage divider composed of  $R_1$  and  $R_2$ , as follows:

$$V = v_{ref} \frac{R_1 + R_2}{R_1} = 300V \quad (21.37)$$

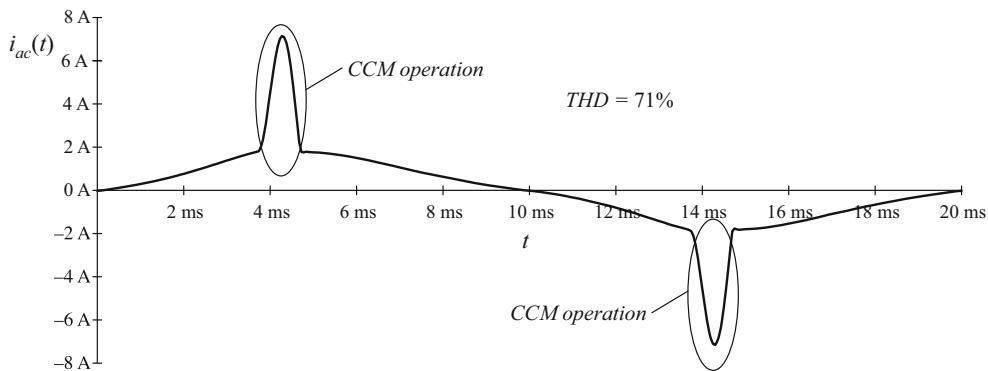
Modeling of the low-bandwidth voltage regulation loop is discussed in Sect. 21.4.2.

It is of interest to find ac line current harmonics. First, a long SPICE transient simulation is performed to reach steady-state operation. Then, current harmonics are computed using Fourier analysis applied to the ac line current waveform  $i_{ac}(t)$  during one line cycle in steady state. Figure 21.9 shows the steady-state ac line current and output voltage obtained for  $R = 900 \Omega$ , i.e., for 100 W of output power. The output voltage has a dc component equal to 300 V, and an ac ripple component at twice the line frequency. The peak-to-peak voltage ripple at twice the line frequency is approximately 8 V, which compares well with the value (7 V) found from Eq. (21.94). The ac line current has noticeable distortion. The spectrum of the ac line current is shown in Fig. 21.10. The largest harmonic, the third, has an amplitude of 16.6% of the fundamental, and the total harmonic distortion is 16.7%.

We can also examine what happens if the rectifier is overloaded. The steady-state ac line current waveform for the case when the load resistance is  $R = 500 \Omega$ , and the output power is 180 W, is shown in Fig. 21.11. The boost converter operates in CCM near the peak of the ac line voltage; this results in current spikes and significant harmonic distortion.



**Fig. 21.10** Spectrum of the ac line current in the DCM boost rectifier

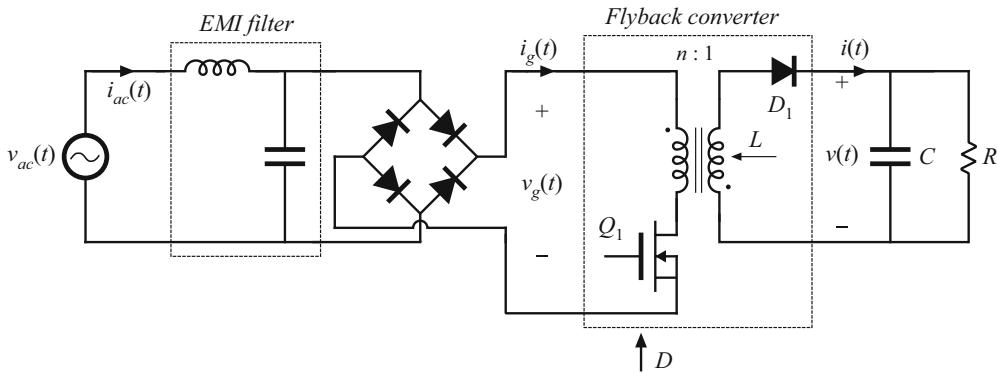


**Fig. 21.11** Ac line current of the DCM boost rectifier example, when the output is overloaded

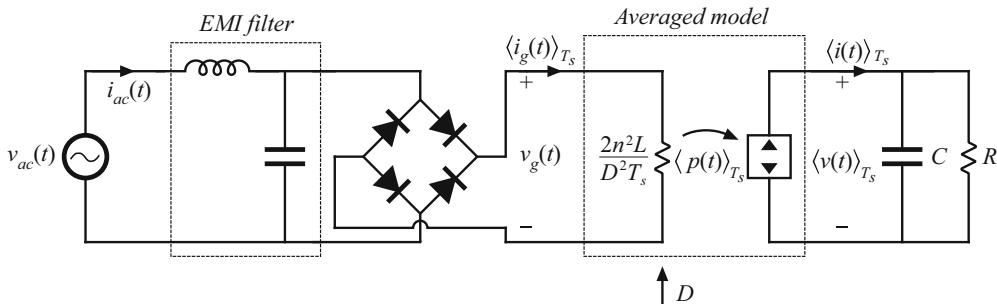
### 21.2.3 DCM Flyback Converter

In Chap. 15, the loss-free resistor network is used to model converters operating in discontinuous conduction mode. This suggests that DCM converters can also be used as near-ideal rectifiers. Indeed, the buck-boost, flyback, SEPIC, and Ćuk converters, when operated in discontinuous conduction mode without additional control, inherently behave as natural loss-free resistors. The DCM effective resistance  $R_e$  found in Chap. 15 to be equal to  $2L/D^2T_s$ , then coincides with the rectifier emulated resistance of Eq. (21.1). At low-power levels, this can be an effective and low-cost approach. Inrush current limiting is also inherent in this approach, and isolation and scaling via a turns ratio are provided by the transformer. Disadvantages are the increased peak currents of DCM, and the need for additional filtering of the high-frequency pulsating input currents.

A simple low-harmonic rectifier system based on the transformer-isolated flyback converter is illustrated in Fig. 21.12 [245]. The ac line voltage is connected through an input EMI filter to a bridge rectifier and a flyback converter. The flyback converter is operated at constant switching frequency  $f_s$  and constant duty cycle  $D$ . The converter is designed such that it operates in the discontinuous conduction mode under all conditions. The input EMI filter smooths the pulsating input current waveform, so that  $i_{ac}(t)$  is approximately sinusoidal.



**Fig. 21.12** Low-harmonic rectifier system incorporating a flyback converter that operates in the discontinuous conduction mode



**Fig. 21.13** Averaged equivalent circuit that models the system of Fig. 21.12

The flyback converter is replaced by its averaged equivalent circuit in Fig. 21.13. As discussed in Chap. 15, the terminal waveforms of the flyback converter have been averaged over the switching period  $T_s$ , resulting in the loss-free resistor model. This model illustrates how the DCM flyback converter presents a resistive load to the ac input. It also illustrates how the power flow can be controlled, by variation of  $D$  to control the value of the emulated resistance  $R_e$ .

To design this converter, one must select the value of inductance to be sufficiently small, such that the converter operates in DCM at all points on the ac sine wave, at maximum load. If we denote the lengths of the transistor conduction interval, diode conduction interval, and discontinuous interval as  $DT_s$ ,  $d_2T_s$ , and  $d_3T_s$ , respectively, then the converter operates in DCM provided that  $d_3$  is greater than zero. This implies that

$$d_2(t) < 1 - D \quad (21.38)$$

By volt-second balance on the transformer magnetizing inductance, we can express  $d_2(t)$  as

$$d_2(t) = D \frac{v_g(t)}{nV} \quad (21.39)$$

Substitution of Eq. (21.39) into Eq. (21.38) and solution for  $D$  yields

$$D < \frac{1}{\left(1 + \frac{v_g(t)}{nV}\right)} \quad (21.40)$$

During a given switching period, the converter will operate in DCM provided that the above inequality is satisfied. The worst case occurs when the rectified sinusoid  $v_g(t)$  is equal to its peak value  $V_M$ . The inequality then becomes

$$D < \frac{1}{\left(1 + \frac{V_M}{nV}\right)} \quad (21.41)$$

If Eq. (21.41) is satisfied, then the converter operates in DCM at all points on the ac line sinusoid.

In steady state, the dc output voltage is given by Eq. (21.8). Upon substitution of the expression for  $R_e$  and solution for  $D$ , this equation becomes

$$D = \frac{2nV}{V_M} \sqrt{\frac{L}{RT_s}} \quad (21.42)$$

Insertion of this relationship into Eq. (21.41), and solution for  $L$ , yields

$$L < L_{crit} = \frac{RT_s}{4\left(1 + \frac{nV}{V_M}\right)^2} \quad (21.43)$$

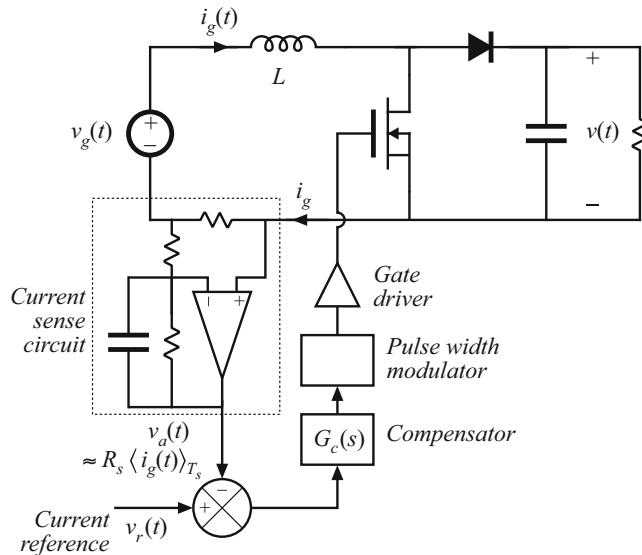
For variations in load  $R$  and peak ac input voltage  $V_M$ , the worst case will occur at minimum  $R$  (maximum power) and minimum  $V_M$ . Hence, the designer should choose  $L$  to satisfy

$$L < L_{crit-min} = \frac{R_{min}T_s}{4\left(1 + \frac{nV}{V_{M-min}}\right)^2} \quad (21.44)$$

If this equation is violated, then at maximum load power and minimum input voltage amplitude, the convert will operate in CCM near the peak of the ac sinewave. This will lead to an input current waveform having substantial distortion.

### 21.3 Control of the Current Waveform

A wide variety of approaches are known for active control of the input current waveform to attain input resistor emulation [177, 178, 255–272]. Average current control [177, 178], input voltage feedforward [177], current-programmed control [258–261], hysteretic control and critical conduction mode control [262–266], and nonlinear carrier control [267–269] are briefly surveyed here. Other approaches include sliding-mode control [270], charge control [271], and ASDTIC control [272].



**Fig. 21.14** Sensing and control of the average input current of a boost converter

### 21.3.1 Average Current Control

Average current control is a popular method of implementing control of the input current waveform in a low-harmonic rectifier. This approach works in both continuous and discontinuous conduction modes, and can produce high-quality current waveforms over a wide range of input voltages and load powers. The problems of crossover distortion, found in some competing schemes such as current programmed control, are largely avoided. Several popular integrated circuits are available that implement average current control. Small-signal modeling of average current controlled converters is discussed in Sect. 18.9.

Figure 21.14 illustrates average current control of the input current waveform  $\langle i_g(t) \rangle_{T_s}$  in a boost converter. The input current  $i_g(t)$  flows through a shunt resistor. The voltage across this shunt resistor is amplified by an op amp circuit. This op amp circuit contains a low-pass filter characteristic that attenuates the high-frequency switching harmonics. The output voltage  $v_a(t)$  of the op amp circuit is proportional to the low-frequency average value of  $i_g(t)$ :

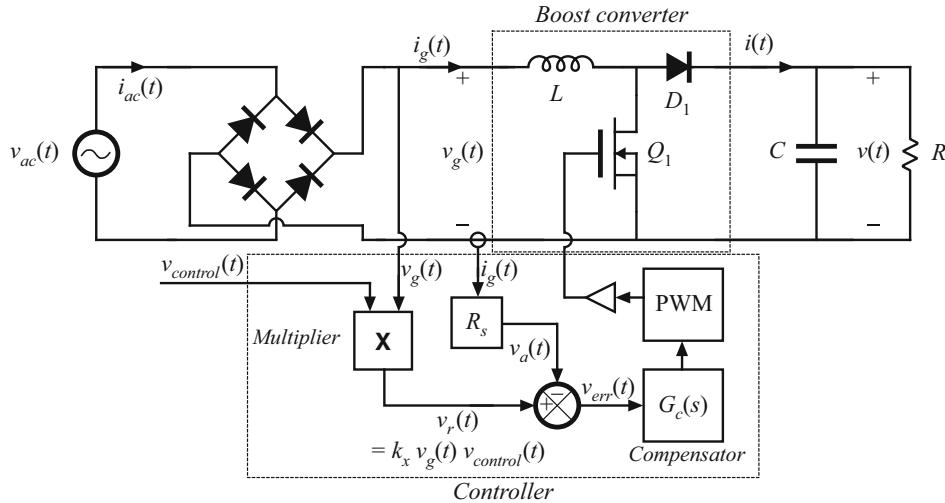
$$v_a(t) = R_s \langle i_g(t) \rangle_{T_s} \quad (21.45)$$

This signal is compared to the reference voltage  $v_r(t)$ , to produce an error signal that drives the compensator network and pulse-width modulator as illustrated. If the feedback loop is well designed, then the error signal is small:

$$v_a(t) \approx v_r(t) \quad (21.46)$$

The average current controller causes the sensed current  $i_g(t)$  to follow the reference waveform  $v_r(t)$ .

To cause the input current to be proportional to the input voltage, the reference voltage  $v_r(t)$  is derived from the sensed input voltage waveform, as in Fig. 21.15. The current reference



**Fig. 21.15** Average current control of a boost converter, to obtain a low-harmonic rectifier

signal  $v_r(t)$  is derived from the sensed input voltage  $v_g(t)$ , and hence has a sinusoidal waveshape. Hence, the average current controller causes the average input current  $i_g(t)$  to be proportional to the input voltage  $v_g(t)$ . The multiplier illustrated in Fig. 21.15 allows adjustment of the constant of proportionality, so that the magnitude of the emulated resistance can be controlled via a control signal  $v_{control}(t)$ . Let us assume that the multiplier terminal equations are

$$v_r(t) = k_x v_g(t) v_{control}(t) \quad (21.47)$$

Then the emulated resistance is

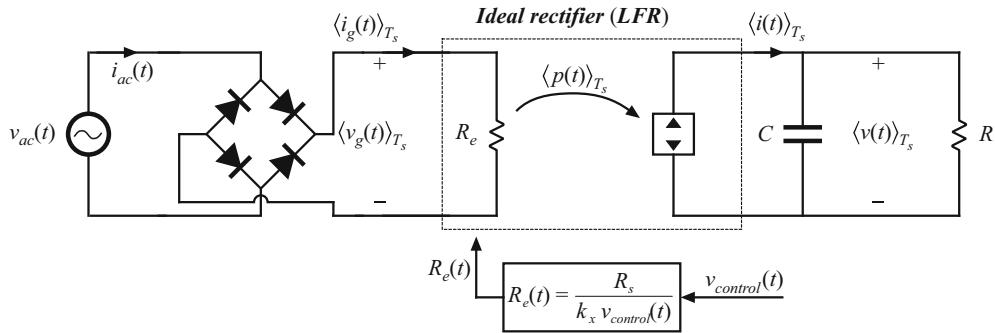
$$R_e = \frac{v_g(t)}{i_g(t)} = \frac{\left( \frac{v_r(t)}{k_x v_{control}(t)} \right)}{\left( \frac{v_a(t)}{R_s} \right)} \quad (21.48)$$

Here, Eqs. (21.47) and (21.45) have been used to eliminate  $v_g$  and  $i_g$ . Substitution of Eq. (21.46) leads to the result

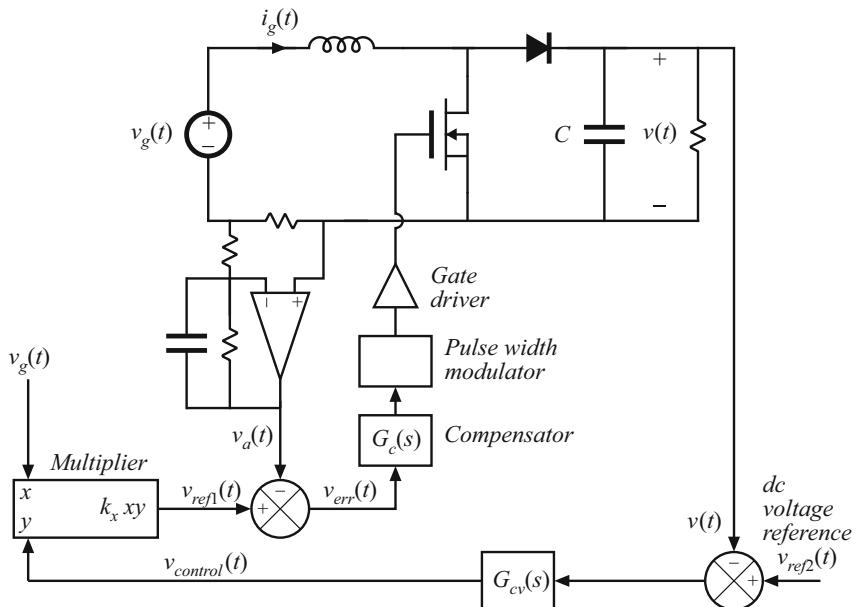
$$R_e(v_{control}(t)) = \frac{R_s}{k_x v_{control}(t)} \quad (21.49)$$

Hence, if the feedback loop is well designed, then the system of Fig. 21.15 can be represented by the LFR model as in Fig. 21.16. The average current controller scheme of Fig. 21.15 and the model of Fig. 21.16 are independent of the dc–dc converter topology, and can be applied to systems containing CCM boost, buck–boost, Ćuk, SEPIC, and other topologies.

Average power flow and the output voltage are regulated by variation of the emulated resistance  $R_e$ , in average current control as well as in most other schemes. This is usually accomplished by use of a multiplier in the input voltage sensing path, as shown in Fig. 21.17.



**Fig. 21.16** Model of the system of Fig. 21.5, based on the loss-free resistor model of Fig. 21.1c, which predicts the low-frequency system waveforms. This model assumes that the feedback loop of Fig. 21.15 operates ideally

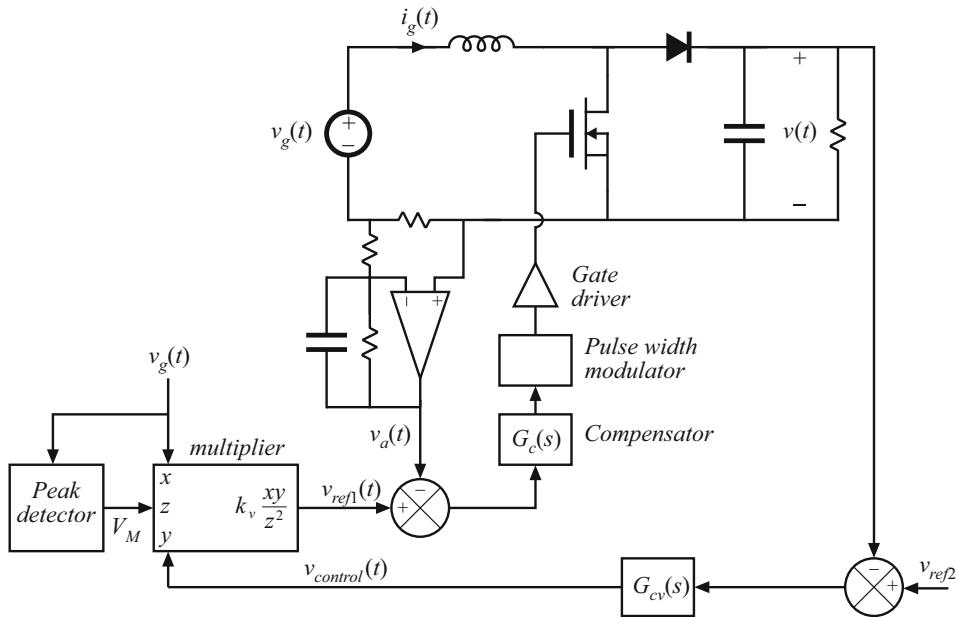


**Fig. 21.17** Average current control incorporating a multiplier for regulation of the output voltage

This control loop continually adjusts  $R_e$  to maintain balance of the average rectifier power  $P_{av} = V_{g,rms}^2/R_e$  and the load power  $P_{load}$ , such that the following relation is obeyed:

$$P_{av} = \frac{V_{g,rms}^2}{R_e} = P_{load} \quad (21.50)$$

Average current control works quite well. Its only disadvantages are the need to sense the average input current, rather than the transistor current, and the need for a multiplier in the controller circuit.



**Fig. 21.18** Average current control incorporating input voltage feedforward

Most average current control implementations include provisions for feedforward of the input voltage amplitude. This allows disturbances in the ac input voltage amplitude to be canceled out by the controller, such that the dc output voltage is unaffected.

Combination of Eqs. (21.47), (21.49), and (21.50), and solution for  $v_{ref1}(t)$  leads to

$$v_{ref1}(t) = \frac{P_{av} v_g(t) R_s}{V_{g,rms}^2} \quad (21.51)$$

This equation shows how the reference voltage should be varied to maintain a given rectifier average power throughput  $P_{av}$ . Apparently, it is necessary to divide by the square of the rms input voltage amplitude. A controller that implements Eq. (21.51) is illustrated in Fig. 21.18. The multiplier block of Fig. 21.17 has been generalized to perform the function  $k_v xy / z^2$ . It is somewhat complicated to compute the rms value of a general ac waveform; however, the ac input voltage  $v_g(t)$  normally is sinusoidal with negligible harmonics. Hence, the peak value of  $v_g(t)$  is directly proportional to its rms value, and we can use the peak value  $V_M$  in place of  $V_{g,rms}$ . So the controller of Fig. 21.18 produces the reference voltage

$$v_{ref1}(t) = \frac{k_v v_{control}(t) v_g(t)}{V_M^2} \quad (21.52)$$

Comparison of Eqs. (21.51) and (21.52) leads to the conclusion that

$$P_{av} = \frac{k_v v_{control}(t)}{2R_s} \quad (21.53)$$

So the average power throughput is directly controlled by  $v_{control}(t)$ , and is independent of the input voltage  $v_g(t)$ .

Feedforward can cause the rectifier dc output voltage to be less sensitive to variations in the ac line voltage. A disadvantage is the ac line current distortion introduced by variations in the voltage produced by the peak detector.

To aid in the design of the inner feedback loop that controls the ac line current waveshape, a converter model is needed that describes how the converter average input current depends on the duty cycle. We would prefer to apply the averaged small-signal modeling techniques of Chap. 7 here. The problem is that the variations in the duty cycle  $d(t)$ , as well as in the ac input voltage  $v_g(t)$  and current  $i_g(t)$ , are not small. As a result, in general the small-signal assumptions are violated, and we are faced with the design of a control system that exhibits significant nonlinear time-varying behavior.

When the rectifier operates near periodic steady state, the output voltage  $v(t)$  of a well-designed system exhibits small variations. So we can write

$$\langle v(t) \rangle_{T_s} = V + \hat{v}(t) \quad (21.54)$$

with

$$|\hat{v}(t)| \ll |V| \quad (21.55)$$

In other words, the small-signal assumption continues to be valid with respect to the rectifier output voltage. In the case of the boost converter, this allows us to linearize the converter input characteristics.

Following the approach of Chap. 7, we can express the average inductor voltage of the boost converter as

$$L \frac{d\langle i_g(t) \rangle_{T_s}}{dt} = \langle v_g(t) \rangle_{T_s} - d'(t)\langle v(t) \rangle_{T_s} \quad (21.56)$$

This equation contains the nonlinear term  $d'(t)\langle v(t) \rangle_{T_s}$ . Substitution of Eq. (21.54) into (21.56) yields

$$L \frac{d\langle i_g(t) \rangle_{T_s}}{dt} = \langle v_g(t) \rangle_{T_s} - d'(t)V - d'(t)\hat{v}(t) \quad (21.57)$$

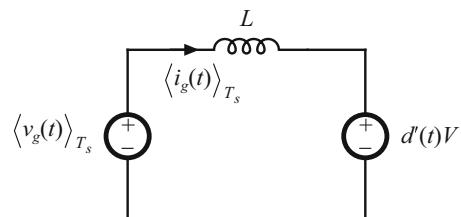
When Eq. (21.55) is satisfied, then the nonlinear term  $-d'(t)\hat{v}(t)$  is much smaller in magnitude than the linear term  $-d'(t)V$ . Therefore, we can discard the nonlinear term to obtain

$$L \frac{d\langle i_g(t) \rangle_{T_s}}{dt} = \langle v_g(t) \rangle_{T_s} - d'(t)V \quad (21.58)$$

This linear differential equation is valid even though  $i_g(t)$ ,  $v_g(t)$ , and  $d(t)$  contain large variations.

An equivalent circuit corresponding to Eq. (21.58) is given in Fig. 21.19. This circuit predicts that the averaged control-to-input-current and input-voltage-to-input-current transfer functions are described by

**Fig. 21.19** Linearized model describing the boost converter input dynamics, corresponding to Eq. (21.58)



$$\begin{aligned} i_g(s) &= \frac{V}{sL} d(s) + \frac{1}{sL} v_g(s) \\ &= G_{id}(s)d(s) + G_{ig}(s)v_g(s) \end{aligned} \quad (21.59)$$

where  $i_g(s)$  is the Laplace transform of  $\langle i_g(t) \rangle_{T_s}$  and  $v_g(s)$  is the Laplace transform of  $\langle v_g(t) \rangle_{T_s}$ . So the input characteristics of the boost rectifier can be linearized, even though the ac input variations are not small.

Unfortunately, Eq. (21.55) is not sufficient to linearize the equations describing the input characteristics of the buck-boost, SEPIC, Ćuk, and most other single-phase rectifiers. The control system design engineer must then deal with a truly nonlinear time-varying dynamical system.

One approach that is sometimes suggested employs the *quasi-static approximation* [273, 274]. It is assumed that the ac line variations are much slower than the rectifier system dynamics, such that the rectifier always operates near equilibrium. The quiescent operating point changes slowly along the input sinusoid; an equilibrium analysis can be performed to find expressions for the slowly-varying “equilibrium” duty ratio and converter voltages and currents. The small-signal dc–dc converter transfer functions derived in Chaps. 7 and 8 are evaluated using this time-varying operating point. The converter poles, zeroes, and gains are found to vary along the ac input sinusoid. An average current controller is designed using these time-varying transfer functions, such that the current loop gain has a positive phase margin at all operating points.

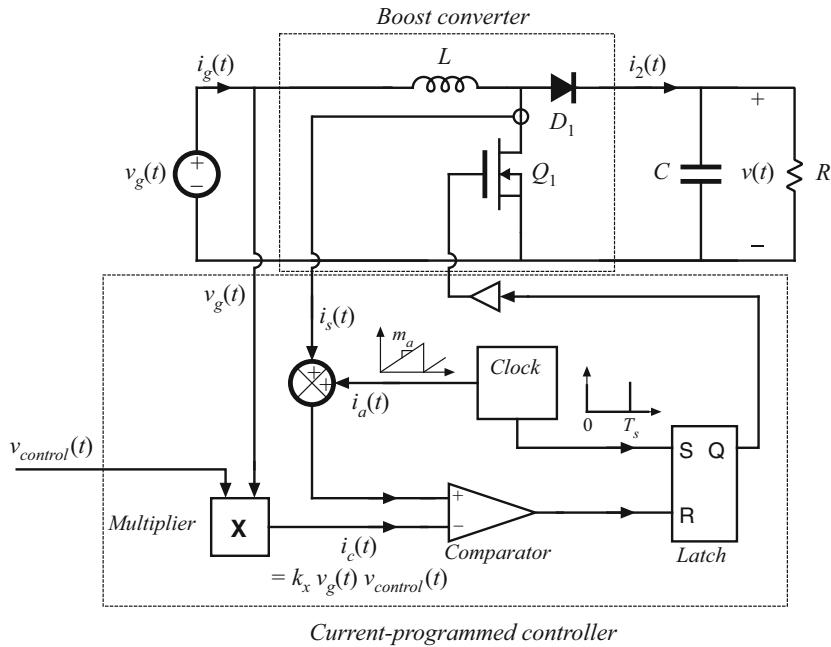
We expect that the quasi-static approximation should be valid if the rectifier system dynamics are sufficiently fast, and it is reasonable to anticipate that high-frequency PWM converters have dynamics that are much faster than the ac line frequency. The problem is that no good condition on system parameters, which can justify the approximation, is known for the basic converter topologies. There is room for additional research in this area.

It is well-understood in the field of control systems that when the rectifier system dynamics are not sufficiently fast, the quasi-static approximation yields neither sufficient nor necessary conditions for stability of the resulting design. Time-varying “loop gains” that always have a positive phase margin may nonetheless be unstable, and a negative phase margin does not always imply instability. Such phenomena are sometimes observed in rectifier systems. Even worse, it is difficult to justify the use of the Laplace transform on rectifiers described by time-varying differential equations, unless the quasi-static approximation can be validated.

### 21.3.2 Current-Programmed Control

Another well-known approach to attaining input resistor emulation is the use of current-programmed control. As illustrated in Fig. 21.20, the programmed current  $i_c(t)$  is made proportional to the ac input voltage. This causes the average inductor current, and hence also  $\langle i_g(t) \rangle_{T_s}$ , to approximately follow  $v_g(t)$ . As in average current control, a multiplier is used to adjust the emulated resistance and average power flow; the control signal  $v_{control}(t)$  is typically used to stabilize the dc output voltage magnitude. Several rectifier control ICs are commercially available, which implement current-programmed control.

As discussed in Chap. 18, several mechanisms cause the average inductor current and hence also  $\langle i_g(t) \rangle_{T_s}$  to differ from the programmed  $i_c(t)$ . These mechanisms introduce crossover distortion and line current harmonics. An artificial ramp having sufficiently large slope  $m_a$  is necessary to stabilize the current-programmed boost converter when it operates in CCM with  $d(t) > 0.5$ . The addition of this ramp causes  $\langle i_g(t) \rangle_{T_s}$  to differ from  $i_c(t)$ . Additional deviation is introduced



**Fig. 21.20** Current-programmed control of a boost rectifier

by the inductor current ripple. Both mechanisms are most pronounced when the inductor current is small, near the zero crossings of the ac line waveforms.

The static input characteristics, that is, the average input current vs. the input voltage, of the current-programmed boost converter are given by

$$\langle i_g(t) \rangle_{T_s} = \begin{cases} v_g(t) \frac{Li_c^2(t)f_s V}{2(V - v_g(t))(v_g(t) + m_a L)^2} & \text{in DCM} \\ i_c(t) - \left(1 - \frac{v_g(t)}{V}\right) \left(m_a + \frac{v_g(t)}{2L}\right) T_s & \text{in CCM} \end{cases} \quad (21.60)$$

The converter operates in the continuous conduction mode when

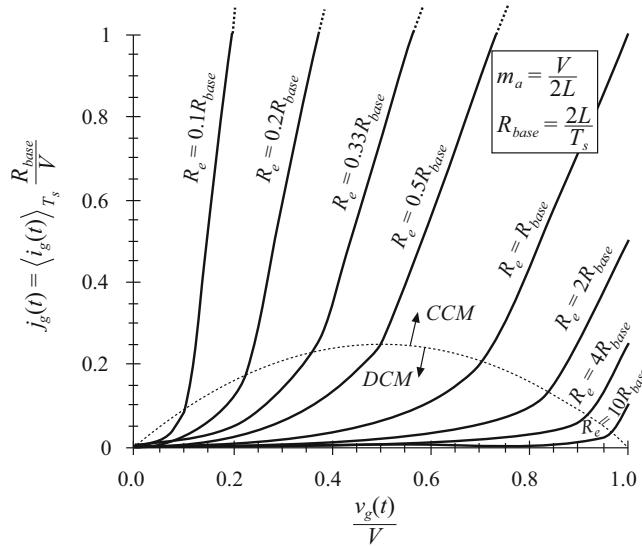
$$\langle i_g(t) \rangle_{T_s} > \frac{T_s V}{2L} \frac{v_g(t)}{V} \left(1 - \frac{v_g(t)}{V}\right) \quad (21.61)$$

In terms of the control current  $i_c(t)$ , the condition for operation in CCM can be expressed

$$i_c(t) > \frac{T_s V}{L} \left(\frac{m_a L}{V} + \frac{v_g(t)}{V}\right) \left(1 - \frac{v_g(t)}{V}\right) \quad (21.62)$$

In the conventional current-programmed rectifier control scheme, the control current  $i_c(t)$  is simply proportional to the ac input voltage:

$$i_c(t) = \frac{v_g(t)}{R_e} \quad (21.63)$$



**Fig. 21.21** Static input characteristics of a current-programmed boost converter, with minimum stabilizing artificial ramp as in Eq. (21.64)

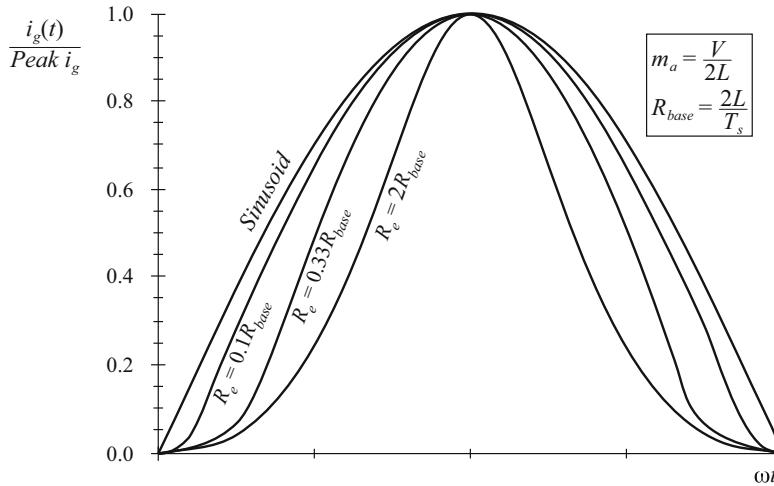
where  $R_e$  is the emulated resistance that would be obtained if the average input current exactly followed the reference current  $i_c(t)$ . The static input characteristics given by Eqs. (21.60) to (21.63) are plotted in Fig. 21.21. The average input current  $\langle i_g(t) \rangle_{T_s}$  is plotted as a function of the applied input voltage  $v_g(t)$ , for several values of emulated resistance  $R_e$ . The region near the CCM-DCM boundary is shown. The curves are plotted for a fixed artificial ramp having slope

$$m_a = \frac{V}{2L} \quad (21.64)$$

This is the minimum value of artificial ramp that stabilizes the boost current-programmed controller at all static operating points. Decreasing  $m_a$  below this value leads to instability at operating points in the continuous conduction mode at low  $v_g(t)/V$ .

To obtain resistor emulation, it is desired that the static input characteristics be linear and pass through the origin. It can be seen from Fig. 21.21 that this is not the case: the curves are reasonably linear in the continuous conduction mode, but exhibit significant curvature as the CCM-DCM boundary is approached. The resulting average current waveforms are summarized in Fig. 21.22.

To minimize the line current THD, it is apparent that the converter should be designed to operate deeply in the continuous conduction mode for most of the ac line cycle. This is accomplished with emulated resistances  $R_e$  that are much smaller than  $R_{base} = 2L/T_s$ . In addition, the artificial ramp slope  $m_a$  should be no greater than otherwise necessary. In practice, THD of 5% to 10% can easily be obtained in rectifiers that function over a narrow range of rms input voltages and load currents. However, low THD cannot be obtained at all operating points in universal-input rectifiers; THD of 20% to 50% may be observed at maximum ac input



**Fig. 21.22** Input current waveforms predicted by the static input characteristics of Fig. 21.21, compared with a pure sinusoid. Curves are plotted for the case  $V_M = 0.8V$ , with minimum stabilizing artificial ramp

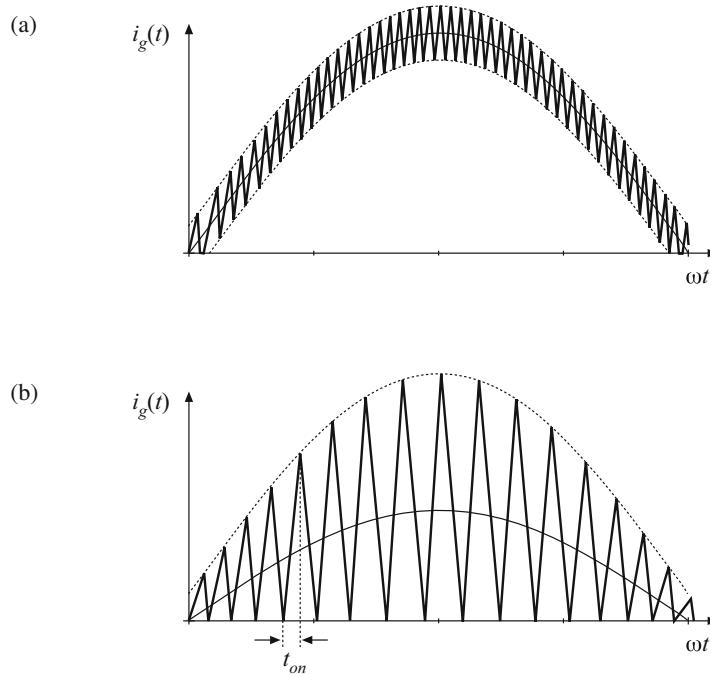
voltage. This problem can be solved by biasing the current reference waveform. Design of current-programmed rectifiers is discussed in [258–261], and some strategies for solving this problem are addressed in [258].

### 21.3.3 Critical Conduction Mode and Hysteretic Control

Another control scheme sometimes used in low-harmonic rectifiers, as well as in dc–dc converters and dc–ac inverters, is hysteretic control. Rather than operating at a fixed switching frequency and duty cycle, the hysteretic controller switches the transistor on and off as necessary to maintain a waveform within given limits. A special case of hysteretic control, called *critical conduction mode* control, is implemented in several commercially available ICs, and is popular for low-harmonic rectifiers rated below several hundred Watts [262–264].

An example is the sinusoid of Fig. 21.23a, in which the boost converter input current is controlled to follow a sinusoidal reference with  $\pm 10\%$  tolerance. The inductor current increases when the transistor is on, and decreases when the transistor is off. So this hysteretic controller switches the transistor on whenever the input current falls below 90% of the reference input. The controller switches the transistor off whenever the input current exceeds 110% of the reference. Hysteretic controllers tend to have simple implementations. However, they have the disadvantages of variable switching frequency and reduced noise immunity.

Another example of hysteretic control is the waveform of Fig. 21.23b. The lower limit is chosen to be zero, while the upper limit is twice the reference input. This controller operates the boost converter at the boundary between the continuous and discontinuous conduction modes. An alternative control scheme that generates the same waveform simply operates the transistor with constant on-time: the transistor is switched on when the inductor current reaches zero, and is switched off after a fixed interval of length  $t_{on}$ . The resulting inductor current waveform will have a peak value that depends directly on the applied input voltage, and whose average value



**Fig. 21.23** Input current waveforms of two boost converters with hysteretic control: (a)  $\pm 10\%$  regulation band, (b) critical conduction mode operation ( $\pm 100\%$  regulation band)

is one-half of its peak. With either control approach, the converter naturally exhibits loss-free-resistor or ideal rectifier behavior. The emulated resistance is

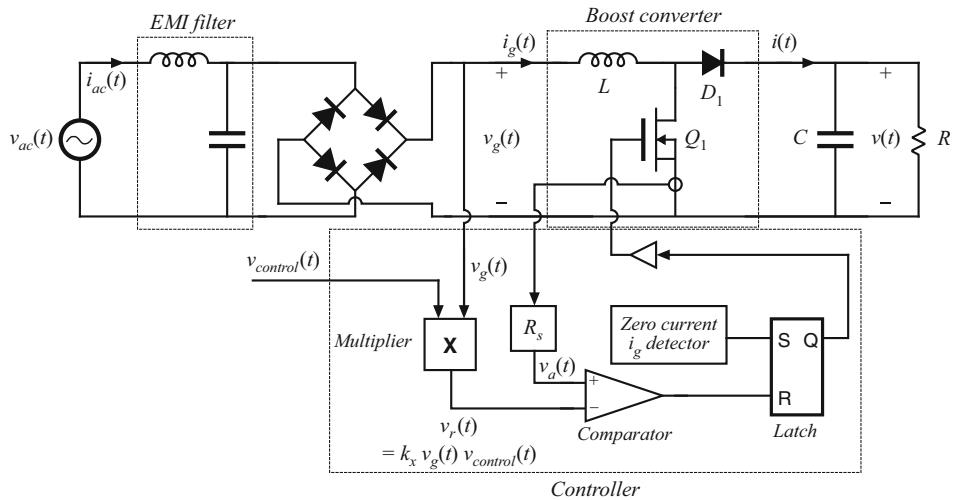
$$R_e = \frac{2L}{t_{on}} \quad (21.65)$$

This scheme has the advantage of small inductor size and low-cost control ICs. Disadvantages are increased peak currents, variable switching frequency, and the need for additional input EMI filtering.

A typical critical conduction mode controller is illustrated in Fig. 21.24. A zero-current detector senses when  $i_g(t)$  (the inductor current) is zero; this is typically accomplished by monitoring the voltage across the inductor. The zero-current detector sets a latch, turning on the transistor and initiating the switching period. The transistor current is also monitored, and is compared to a sinusoidal reference  $v_r(t)$  that is proportional to the applied input voltage  $v_g(t)$ . When the sensed current is equal to the reference, the latch is reset and the transistor is turned off.

Since the switching frequency can vary, possibly over a wide range, it is important to carefully design the converter power stage. For a given power  $P$ , the required transistor on-time  $t_{on}$  can be found by combining Eqs. (21.17) and (21.65), and solving for  $t_{on}$ :

$$t_{on} = \frac{4LP}{V_M^2} \quad (21.66)$$



**Fig. 21.24** A typical implementation of critical conduction mode

Application of the principle of volt-second balance to inductor  $L$  of Fig. 21.24 leads to the following equation:

$$v_g t_{on} + (v_g - V) t_{off} = 0 \quad (21.67)$$

Hence, the transistor off-time is given by

$$t_{off} = t_{on} \frac{v_g}{(V - v_g)} \quad (21.68)$$

The switching period  $T_s$  is equal to

$$T_s = t_{off} + t_{on} \quad (21.69)$$

Substitution of Eqs. (21.66) and (21.68) into Eq. (21.69) yields

$$T_s = \frac{4LP}{V_M^2} \frac{1}{\left(1 - \frac{v_g(t)}{V}\right)} \quad (21.70)$$

The following expression for switching frequency is found by substitution of Eq. (21.11) into Eq. (21.70):

$$f_s = \frac{1}{T_s} = \frac{V_M^2}{4LP} \left(1 - \frac{V_M}{V} |\sin(\omega t)|\right) \quad (21.71)$$

The maximum switching frequency occurs when  $\sin(\omega t)$  equals zero:

$$\max f_s = \frac{V_M^2}{4LP} \quad (21.72)$$

The minimum switching frequency occurs at the peak of the sine wave:

$$\min f_s = \frac{V_M^2}{4LP} \left(1 - \frac{V_M}{V}\right) \quad (21.73)$$

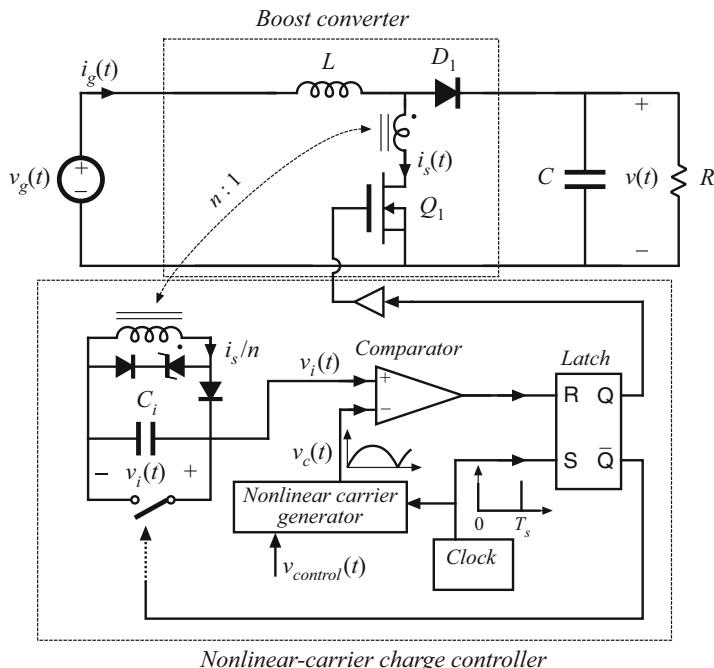
Equations (21.72) and (21.73) can be used to select the value of the inductance  $L$  and the output voltage  $V$ , so that the switching frequency varies over an acceptable range.

### 21.3.4 Nonlinear Carrier Control

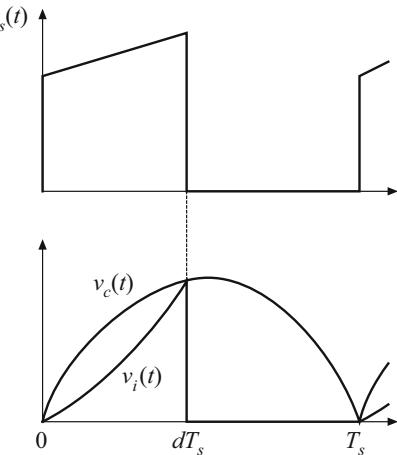
The nonlinear carrier controller (NLC) is capable of attaining input resistor emulation in boost and other converters that operate in the continuous conduction mode. Implementation of the controller is quite simple, with no need for sensing of the input voltage or input current. There is also no need for a current loop error amplifier. The boost nonlinear-carrier charge controller is inherently stable and is free from the stability problems that require addition of an artificial ramp in current-programmed controllers.

A CCM boost rectifier system with nonlinear-carrier charge control is illustrated in Fig. 21.25, and waveforms are given in Fig. 21.26. The reasoning behind this approach is as follows. It is desirable to control the transistor switch current  $i_s(t)$ . This pulsating current is much easier to sense than the continuous converter input current—a simple current transformer can be used, as in Fig. 21.25. Further, it is desirable to control the integral of this current, or the charge, for two reasons: (1) integration of the waveform leads to improved noise immunity and (2) the integral of the waveform is directly related to its average value,

$$\langle i_s(t) \rangle_{T_s} = \frac{1}{T_s} \int_t^{t+T_s} i_s(\tau) d\tau \quad (21.74)$$



**Fig. 21.25** Nonlinear carrier charge control of a boost converter



**Fig. 21.26** Transistor current  $i_s(t)$ , parabolic carrier voltage  $v_c(t)$ , and integrator voltage  $v_i(t)$  waveforms for the NLC-controller boost rectifier of Fig. 21.25

In a fixed-frequency system,  $T_s$  is constant, and the integral over one switching period is proportional to the average value. Hence the average switch current can be controlled to be proportional to a reference signal by simply switching the transistor off when the integral of the switch current is equal to the reference. In the controller of Fig. 21.25, the switch current  $i_s(t)$  is scaled by the transformer turns ratio  $n$ , and then integrated by capacitor  $C_i$ , such that

$$v_i(t) = \frac{1}{C_i} \int_0^{dT_s} \frac{i_s(\tau)}{n} d\tau \quad \text{for } 0 < t < dT_s \quad (21.75)$$

The integrator voltage  $v_i(t)$  is reset to zero at the end of each switching period, and the integration process begins anew at the beginning of the next switching period. So at the instant that the transistor is switched off, the voltage  $v_i(dT_s)$  is proportional to the average switch current:

$$v_i(dT_s) = \frac{\langle i_s \rangle_{T_s}}{n C_i f_s} \quad \text{for interval } 0 < t < T_s \quad (21.76)$$

How should the average switch current be controlled? To obtain input resistor emulation, it is desired that

$$\langle i_g(t) \rangle_{T_s} = \frac{\langle v_g(t) \rangle_{T_s}}{R_e(v_{control})} \quad (21.77)$$

It is further desired to avoid sensing either  $i_g(t)$  or  $v_g(t)$ . As with other schemes, we will sense the dc output voltage  $\langle v(t) \rangle_{T_s}$  to construct a low-bandwidth feedback loop that balances the average input and output powers. So let us determine the relationship between  $\langle i_s(t) \rangle_{T_s}$  and  $\langle v(t) \rangle_{T_s}$  implied by Eq. (21.77). If we assume that the boost converter operates in the continuous conduction mode, then we can write

$$\langle i_s(t) \rangle_{T_s} = d(t) \langle i_g(t) \rangle_{T_s} \quad (21.78)$$

and

$$\langle v_g(t) \rangle_{T_s} = d'(t) \langle v(t) \rangle_{T_s} \quad (21.79)$$

Substitution of Eqs. (21.78) and (21.79) into Eq. (21.77) leads to

$$\langle i_s(t) \rangle_{T_s} = d(t)(1-d(t)) \frac{\langle v(t) \rangle_{T_s}}{R_e(v_{control})} \quad (21.80)$$

The controller of Fig. 21.25 implements this equation.

The nonlinear carrier generator of Fig. 21.25 produces the parabolic waveform  $v_c(t)$ , given by

$$\begin{aligned} v_c(t) &= v_{control} \left( \frac{t}{T_s} \right) \left( 1 - \frac{t}{T_s} \right) \quad \text{for } 0 \leq t \leq T_s \\ v_c(t + T_s) &= v_c(t) \end{aligned} \quad (21.81)$$

This waveform is illustrated in Fig. 21.26. Note that Eq. (21.81) resembles Eq. (21.80), with  $d(t)$  replaced by  $(t/T_s)$ . The controller switches the transistor off at time  $t = dT_s$  when the integrator voltage  $v_j(t)$  is equal to the carrier waveform  $v_c(t)$ . Hence, it is true that

$$v_i(dT_s) = v_c(dT_s) = v_{control}(t)d(t)(1-d(t)) \quad (21.82)$$

Substitution of Eq. (21.76) yields

$$\frac{\langle i_s(t) \rangle_{T_s}}{nC_i f_s} = v_{control}(t)d(t)(1-d(t)) \quad (21.83)$$

This is of the same form as Eq. (21.80). Comparison of Eqs. (21.80) and (21.83) reveals that the emulated resistance  $R_e$  is given by

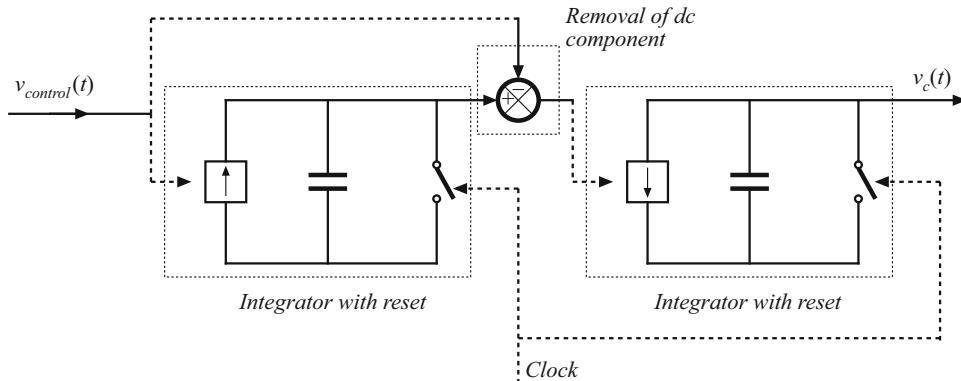
$$R_e(v_{control}) = d(t)(1-d(t)) \frac{\langle v(t) \rangle_{T_s}}{\langle i_s(t) \rangle_{T_s}} = \frac{\langle v(t) \rangle_{T_s}}{nC_i f_s v_{control}(t)} \quad (21.84)$$

If the dc output voltage and the control voltage have negligible ac variation, then  $R_e$  is essentially constant, and the ac line current will exhibit low harmonic distortion. So neither the input voltage nor the input current need to be sensed, and input resistor emulation can be obtained in CCM boost converters by sensing only the switch current.

A simple way to generate the parabolic carrier waveform uses two integrators, as illustrated in Fig. 21.27. The slowly varying control voltage  $v_{control}(t)$  is integrated, to obtain a ramp waveform  $v_r(t)$  whose peak amplitude is proportional to  $v_{control}(t)$ . The dc component of this waveform is removed, and then integrated again. The output of the second integrator is the parabolic carrier  $v_c(t)$ , illustrated in Fig. 21.26 and given by Eq. (21.81). Both integrators are reset to zero before the end of each switching period by the clock generator. The amplitude of the parabolic carrier, and hence also the emulated resistance, can be controlled by variation of  $v_{control}(t)$ .

Equations (21.78) and (21.79) are valid only when the converter operates in the continuous conduction mode. In consequence, the ac line current waveform is distorted when the converter operates in DCM. Since this occurs near the zero crossings of the ac line voltage, crossover distortion is generated. Nonetheless, the harmonic distortion is less severe than in current-programmed schemes, and it is feasible to construct universal-input rectifiers that employ the NLC control approach. Total harmonic distortion is analyzed and plotted in [267].

Nonlinear carrier control can be applied to current-programmed boost rectifiers, as well as to other rectifiers based on the buck-boost, SEPIC, Ćuk, or other topologies, with either integral charge control or peak-current-programmed control [267, 268]. In these cases, a different carrier waveform must be employed. A nonlinear carrier controller in which the ac input voltage  $v_g(t)$  is sensed, rather than the switch current  $i_s(t)$ , is described in [269].



**Fig. 21.27** Generation of parabolic carrier waveform by double integration

## 21.4 Single-Phase Converter Systems Incorporating Ideal Rectifiers

An additional issue that arises in PWM rectifier systems is the control of power drawn from the ac line, the power delivered to the dc load, and the energy stored in a bulk energy storage capacitor.

### 21.4.1 Energy Storage

It is usually desired that the dc output voltage of a converter system can be regulated with high accuracy. In practice, this is easily accomplished using a high-gain wide-bandwidth feedback loop. A well-regulated dc output voltage  $v(t) = V$  is then obtained, which has negligible ac variations. For a given constant load characteristic, the load current  $I$  and the instantaneous load power  $p_{load}(t) = P_{load}$  are also constant:

$$p_{load}(t) = v(t)i(t) = VI \quad (21.85)$$

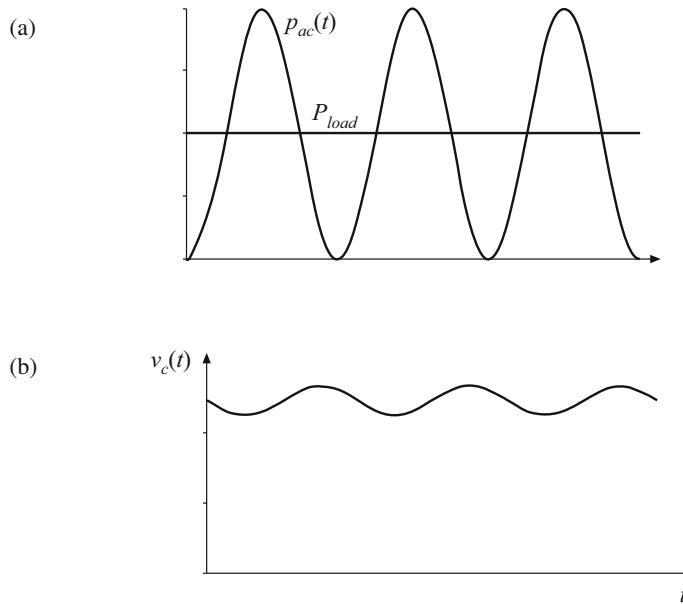
However, the instantaneous input power  $p_{ac}(t)$  of a single-phase ideal rectifier is not constant:

$$p_{ac}(t) = v_g(t)i_g(t) \quad (21.86)$$

If  $v_g(t)$  is given by Eq. (21.11), and if  $i_g(t)$  follows Eq. (21.1), then the instantaneous input power becomes

$$p_{ac}(t) = \frac{V_M^2}{R_e} \sin^2(\omega t) = \frac{V_M^2}{2R_e} (1 - \cos(2\omega t)) \quad (21.87)$$

which varies with time. The instantaneous input power is zero at the zero crossings of the ac input voltage. Equations (21.85) and (21.87) are illustrated in Fig. 21.28a. Note that the desired instantaneous load power  $p_{load}(t)$  is not equal to the desired instantaneous rectifier input power  $p_{ac}(t)$ . Some element within the rectifier system must supply or consume the difference between these two instantaneous powers.



**Fig. 21.28** Waveforms of a single-phase ideal rectifier system: (a) pulsating ac input power  $p_{in}(t)$ , and constant dc load power  $P_{load}$ ; (b) energy storage capacitor voltage  $v_C(t)$

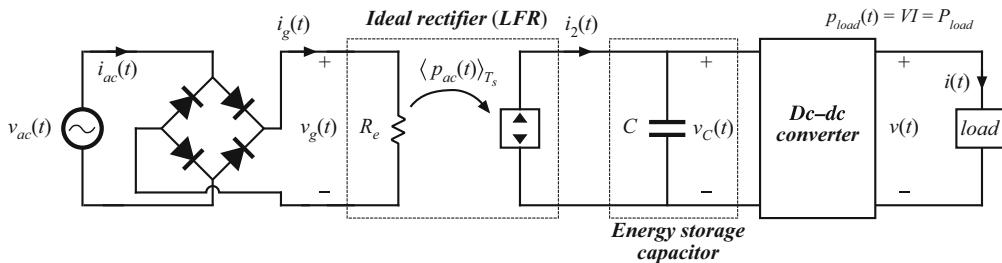
Since the ideal rectifier does not consume or generate power, nor does it contain significant internal energy storage, it is necessary to add to the system a low-frequency energy storage element such as an electrolytic capacitor. The difference between the instantaneous input and load powers flows through this capacitor.

The waveforms of rectifier systems containing reactive elements can be determined by solution of the rectifier energy equation [275, 276]. If the energy storage capacitor  $C$  is the only system element capable of significant low-frequency energy storage, then the power  $p_C(t)$  flowing into the capacitor is equal to the difference between the instantaneous input and output powers:

$$p_C(t) = \frac{dE_C(t)}{dt} = \frac{d\left(\frac{1}{2}Cv_C^2(t)\right)}{dt} = p_{ac}(t) - p_{load}(t) \quad (21.88)$$

where  $C$  is the capacitance,  $v_C(t)$  is the capacitor voltage, and  $E_C(t)$  is the energy stored in the capacitor. Hence as illustrated in Fig. 21.28b, when  $p_{ac}(t) > p_{load}(t)$  then energy flows into the capacitor, and  $v_C(t)$  increases. Likewise,  $v_C(t)$  decreases when  $p_{ac}(t) < p_{load}(t)$ . So the capacitor voltage  $v_C(t)$  must be allowed to increase and decrease as necessary to store and release the required energy. In steady state, the average values of  $p_{ac}(t)$  and  $p_{load}(t)$  must be equal, so that over one ac line cycle there is no net change in capacitor stored energy.

Where can the energy storage capacitor be placed? It is necessary to separate the energy storage capacitor from the regulated dc output, so that the capacitor voltage is allowed to independently vary as illustrated in Fig. 21.28b. A conventional means of accomplishing this is illustrated in Fig. 21.29. A second dc-dc converter is inserted, between the energy storage capacitor and the regulated dc load. A wide-bandwidth feedback loop controls this converter, to attain a well-regulated dc load voltage. The capacitor voltage  $v_C(t)$  is allowed to vary. Thus, this



**Fig. 21.29** Elements of a single-phase-ac to dc power supply, in which the ac line current and dc load voltage are independently regulated with high bandwidth. An internal independent energy storage capacitor is required

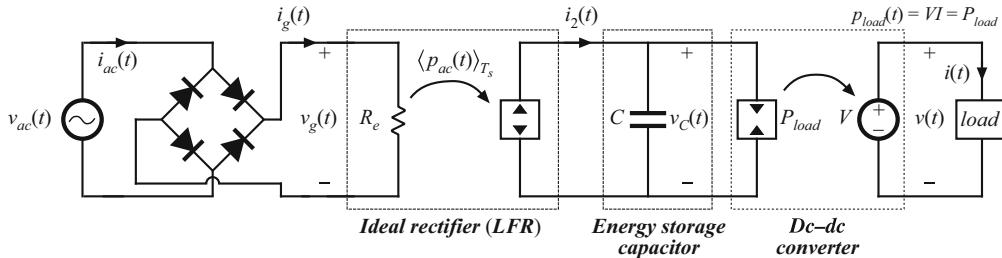
system configuration is capable of (1) wide-bandwidth control of the ac line current waveform, to attain unity power factor, (2) internal low-frequency energy storage, and (3) wide-bandwidth regulation of the dc output voltage. It is also possible to integrate these functions into a single converter, provided that the required low-frequency independence of the input, output, and capacitor voltages is maintained [277].

The energy storage capacitor also allows the system to function in other situations in which the instantaneous input and output powers differ. For example, it is commonly required that the output voltage remains regulated during ac line voltage failures of short duration. The *hold-up time* is the duration that the output voltage  $v(t)$  remains regulated after  $v_{ac}(t)$  has become zero. A typical requirement is that the system continues to supply power to the load during one complete missing ac line cycle, that is, for 20 msec in a 50 Hz system. During the hold-up time, the load power is supplied entirely by the energy storage capacitor. The value of capacitance should be chosen such that at the end of the hold-up time, the capacitor voltage  $v_C(t)$  exceeds the minimum value that the dc–dc converter requires to produce the desired load voltage.

The energy storage function could be performed by an element other than a capacitor, such as an inductor. However, use of an inductor is a poor choice, because of its high weight and cost. For example, a  $100\ \mu\text{F}$  100 V electrolytic capacitor and a  $100\ \mu\text{H}$  100 A inductor can each store 1 Joule of energy. But the capacitor is considerably smaller, lighter, and less expensive.

A problem introduced by the energy storage capacitor is the large *inrush current* observed during the system turn-on transient. The capacitor voltage  $v_C(t)$  is initially zero; substantial amounts of charge and energy are required to raise this voltage to its equilibrium value. The boost converter is not capable of limiting the magnitude of the resulting inrush current: even when  $d(t) = 0$ , a large current flows through the boost converter diode to the capacitor, as long as the converter output voltage is less than the input voltage. Some additional circuitry is required to limit the inrush current of the boost converter. Converters having a buck–boost type conversion ratio are inherently capable of controlling the inrush current. This advantage comes at the cost of additional switch stress.

It is also possible to design the ideal rectifier to operate correctly when connected to utility power systems anywhere in the world. *Universal input* rectifiers can operate with nominal ac rms voltage magnitudes as low as the 100 V encountered in a portion of Japan, or as high as the 260 V found in western Australia, with ac line frequencies of either 50 Hz or 60 Hz. Regardless of the ac input voltage, the universal-input rectifier produces a constant nominal dc output voltage  $V_C$ .



**Fig. 21.30** Low-frequency equivalent circuit of the system of Fig. 21.29

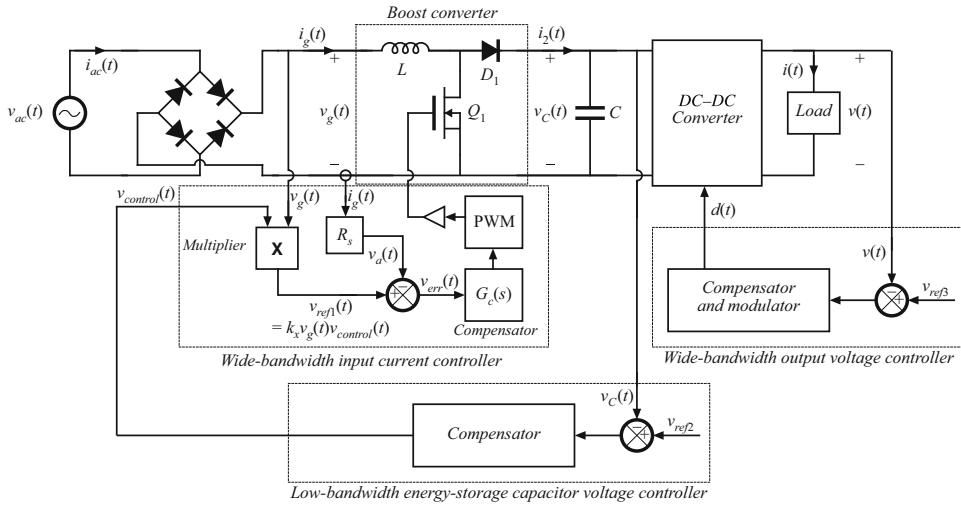
Let us now consider in more detail the low-frequency energy storage process of the system of Fig. 21.29. Let us assume that the dc–dc converter contains a controller having bandwidth much greater than the ac line frequency, such that the load voltage contains negligible low-frequency variations. A low-frequency model of the dc–dc converter is then as illustrated in Fig. 21.30. The dc–dc converter produces constant voltage  $v(t) = V$  modeled by a voltage source as shown. This causes the load to draw constant current  $i(t) = I$ , leading to load power  $p_{load}(t) = P_{load}$ . To the extent that converter losses can be neglected, the dc–dc converter input port draws power  $P_{load}$ , regardless of the value of  $v_C(t)$ . So the dc–dc converter input port can be modeled as a constant power sink, of value  $P_{load}$ .

The model of Fig. 21.30 implies that the difference between the rectifier power  $p_{ac}(t)$  and the load power  $P_{load}$  flows into the capacitor, as given by Eq. (21.88). The capacitor voltage increases when  $p_{ac}(t)$  exceeds  $P_{load}$ , and decreases when  $p_{ac}(t)$  is less than  $P_{load}$ . In steady state, the average values of  $p_{ac}(t)$  and  $P_{load}$  must be equal. But note that  $p_{ac}(t)$  is determined by the magnitudes of  $v_{ac}(t)$  and  $R_e$ , and not by the load. The system of Fig. 21.30 contains no mechanism to cause the average rectifier power and load power to be equal. In consequence, it is necessary to add an additional control system that adjusts  $R_e$  as necessary, to cause the average rectifier output power and dc–dc converter input power to balance. The conventional way to accomplish this is simply to regulate the dc component of  $v_C(t)$ .

A complete system containing ideal rectification, energy storage, and wide-bandwidth output voltage regulation is illustrated in Fig. 21.31. This system incorporates the boost converter and controller of Fig. 21.5, as well as a generic dc–dc converter with output voltage feedback. In addition, the system contains a low-bandwidth feedback loop, which regulates the dc component of the energy storage capacitor voltage to be equal to a reference voltage  $v_{ref2}$ . This is accomplished by slow variations of  $v_{control}(t)$  and  $R_e$ . This controller should have sufficiently small loop gain at the even harmonics of the ac line frequency, so that variations in  $R_e$  are much slower than the ac line frequency.

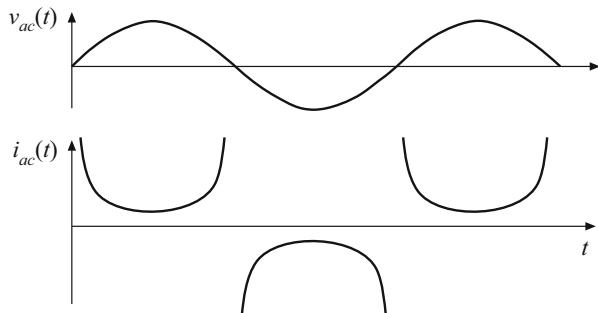
Increasing the bandwidth of the energy storage capacitor voltage controller can lead to significant ac line current harmonics. When this controller has wide bandwidth and high gain, then it varies  $R_e(t)$  quickly, distorting the ac line current waveform. In the extreme limit of perfect regulation of the energy storage capacitor voltage  $v_C(t) = V_C$ , then the capacitor stored energy is constant, and the instantaneous input ac line power  $p_{ac}(t)$  and load power  $p_{load}(t)$  are equal. The controller prevents the energy storage capacitor from performing its low-frequency energy storage function. The ac line current then becomes

$$i_{ac}(t) = \frac{p_{ac}(t)}{v_{ac}(t)} = \frac{p_{load}(t)}{v_{ac}(t)} = \frac{P_{load}}{V_M \sin(\omega t)} \quad (21.89)$$



**Fig. 21.31** A complete dc power supply system incorporating a near-ideal single-phase boost rectifier system, energy storage capacitor, and dc–dc converter. Wide-bandwidth feedback loops regulate the ac line current waveform and the dc load voltage, and a slow feedback loop regulates the energy storage capacitor voltage

**Fig. 21.32** Ac line current waveform of the single-phase ideal rectifier with output voltage feedback, in the hypothetical case where constant instantaneous power is supplied to a dc load. The THD tends to infinity, and the power factor tends to zero



This waveform is sketched in Fig. 21.32. In this idealized limiting case, the ac line current tends to infinity at the zero crossings of the ac line voltage waveform, such that the instantaneous input power is constant. It can be shown that the THD of this current waveform is infinite, and its distortion factor and power factor are zero. So the bandwidth of this controller should be limited.

The energy storage capacitor voltage ripple can be found by integration of Eq. (21.88). Under steady-state conditions, where the average value of  $p_{ac}(t) = P_{load}$ , integration of Eq. (21.88) yields

$$E_C(t) = \frac{1}{2} C v_C^2(t) = E_C(0) + \int_0^t (-P_{load} \cos(2\omega t)) dt \quad (21.90)$$

where  $\omega$  is the ac line frequency. Evaluation of the integral leads to

$$E_C(t) = E_C(0) - \frac{P_{load} \sin(2\omega t)}{2\omega} \quad (21.91)$$

Therefore, the capacitor voltage waveform is

$$v_C(t) = \sqrt{\frac{2E_C(t)}{C}} = \sqrt{v_C^2(0) - \frac{P_{load}}{\omega C} \sin(2\omega t)} \quad (21.92)$$

It can be verified that the rms value of this waveform is  $V_{C,rms} = v_C(0)$ . Hence, Eq. (21.92) can be written

$$v_C(t) = V_{C,rms} \sqrt{1 - \frac{P_{load}}{\omega C V_{C,rms}^2} \sin(2\omega t)} \quad (21.93)$$

This waveform is sketched in Fig. 21.28b. The minimum and maximum values of the capacitor voltage occur when  $\sin(2\omega t)$  is equal to 1 and -1, respectively. Therefore, the peak-to-peak capacitor voltage ripple is

$$2\Delta v_C = V_{C,rms} \left[ \sqrt{1 + \frac{P_{load}}{\omega C V_{C,rms}^2}} - \sqrt{1 - \frac{P_{load}}{\omega C V_{C,rms}^2}} \right] \approx \frac{P_{load}}{\omega C V_{C,rms}} \quad (21.94)$$

The approximation is valid for  $P_{load}/(\omega C V_{C,rms}^2)$  sufficiently less than one, a condition that is satisfied whenever the ac voltage ripple is sufficiently less than  $V_{C,rms}$ .

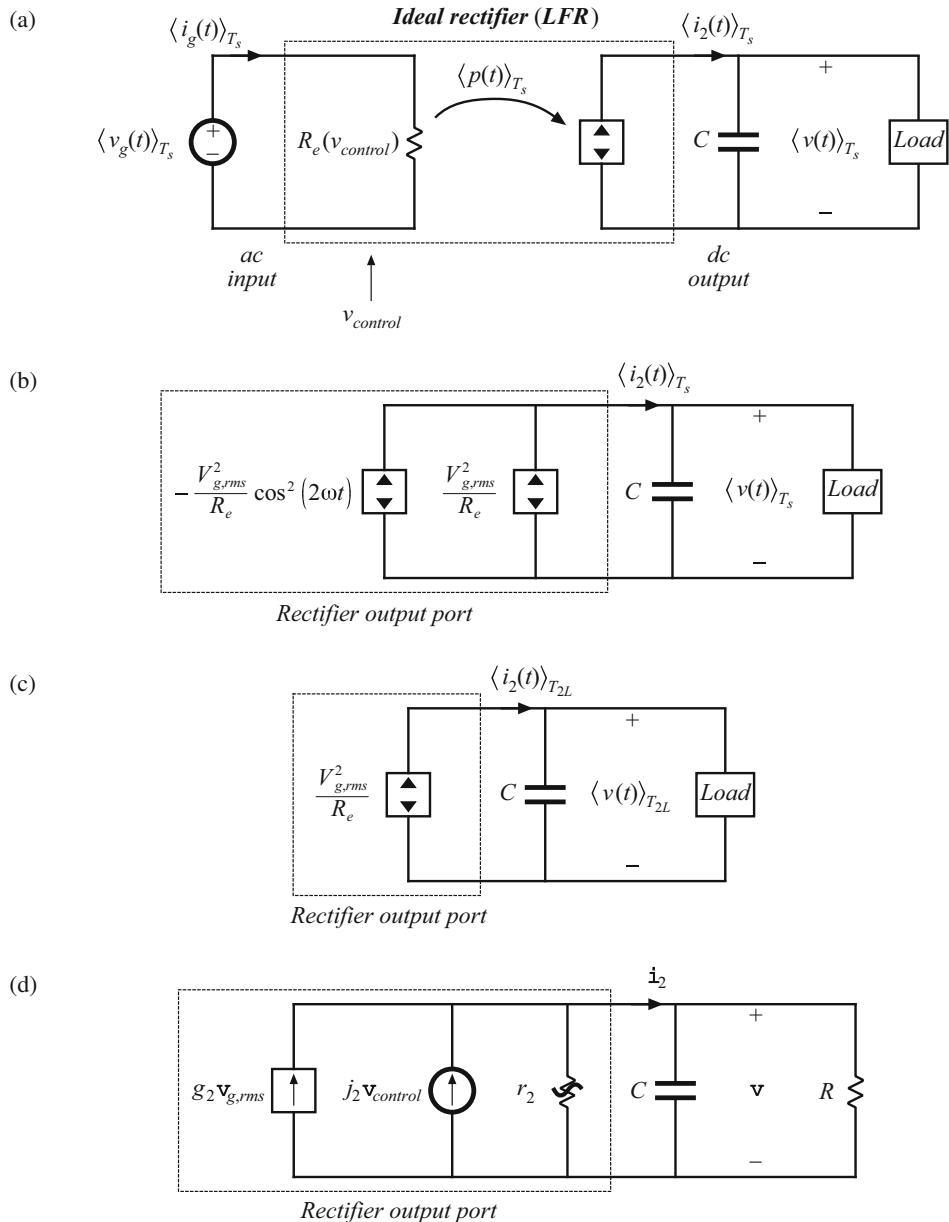
### 21.4.2 Modeling the Outer Low-Bandwidth Control System

As discussed above, the outer low-bandwidth controller, which varies the emulated resistance as necessary to balance the average ac input and dc load powers, is common to all near-ideal rectifier systems. For design of this controller, the rectifier can be modeled using the loss-free resistor (LFR) model. Perturbation and linearization of the LFR lead to a small-signal equivalent circuit that predicts the relevant small-signal transfer functions. Such a model is derived in this section [245, 276, 278].

It is desirable to stabilize the rectifier output voltage against variations in load power, ac line voltage, and component characteristics. Hence, a voltage feedback loop is necessary. As discussed in Sect. 21.4.1, this loop cannot attempt to remove the capacitor voltage ripple that occurs at the second harmonic of the ac line frequency,  $2\omega$ , since doing so would require that  $R_e(t)$  change significantly at the second harmonic frequency. This would introduce significant distortion, phase shift, and power factor degradation into the ac line current waveform. In consequence this loop must have sufficiently small gain at frequency  $2\omega$ , and hence its bandwidth must be low. Therefore, for the purposes of designing the low-bandwidth outer control loop, it is unnecessary to model the system high-frequency behavior. It can be assumed that any inner wide-bandwidth controller operates ideally at low frequencies, such that the ideal rectifier model of Fig. 21.33a adequately represents the low-frequency system behavior.

A small-signal model is derived here that correctly predicts the control-to-output transfer function and output impedance of any rectifier system that can be modeled as a loss-free resistor. The model neglects the complicating effects of high-frequency switching ripple, and is valid for control variations at frequencies sufficiently less than the ac line frequency. Both resistive and dc–dc converter/regulator loads are treated.

The steps in the derivation of the small-signal ac model are summarized in Fig. 21.33. Figure 21.33a is the basic ideal rectifier model, in which the converter high-frequency switching



**Fig. 21.33** Steps in the derivation of the low-frequency small-signal rectifier model: (a) large-signal LFR model, averaged over one switching period  $T_s$ ; (b) separation of power source into its constant and time-varying components; (c) removal of second harmonic components by averaging over one-half of the ac line period  $T_{2L}$ ; (d) small-signal model obtained by perturbation and linearization of (c)

ripple is removed via averaging over the switching period  $T_s$ , but waveform frequency components slower than the switching frequency are correctly modeled, including the  $2\omega$  second-harmonic and dc components of output voltage. It is difficult to use this model in design of the feedback loop because it is highly nonlinear and time-varying.

If the ac input voltage  $v_g(t)$  is

$$v_g(t) = \sqrt{2}v_{g,rms} |\sin(\omega t)| \quad (21.95)$$

then the model of Fig. 21.33a predicts that the instantaneous output power  $\langle p(t) \rangle_{T_s}$  is

$$\langle p(t) \rangle_{T_s} = \frac{\langle v_g(t) \rangle_{T_s}^2}{R_e(v_{control}(t))} = \frac{v_{g,rms}^2}{R_e(v_{control}(t))} (1 - \cos(2\omega t)) \quad (21.96)$$

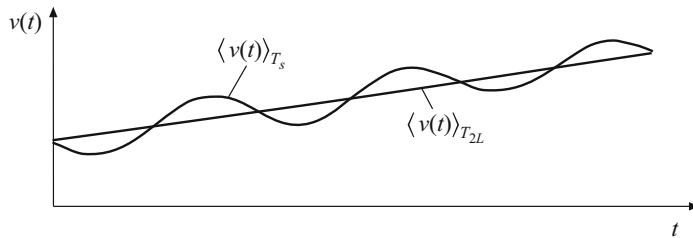
The output power is comprised of a constant term  $v_{g,rms}^2/R_e$ , and a term that varies at the second harmonic of the ac line frequency. These two terms are explicitly identified in Fig. 21.33b.

The second-harmonic variation in  $\langle p(t) \rangle_{T_s}$  leads to time-varying system equations, and slow variations in  $v_{control}(t)$  lead to an output voltage spectrum containing components not only at the frequencies present in  $v_{control}(t)$ , but also at the even harmonics of the ac line frequency and their sidebands, as well as at the switching frequency and its harmonics and sidebands. It is desired to model only the low-frequency components excited by slow variations in  $v_{control}(t)$ , the load, and the ac line voltage amplitude  $v_{g,rms}$ . The even harmonics of the ac line frequency can be removed by averaging over one-half of the ac line period

$$T_{2L} = \frac{1}{2} \frac{2\pi}{\omega} = \frac{\pi}{\omega} \quad (21.97)$$

Hence, we average over the switching period  $T_s$  to remove the switching harmonics, and then average again over one-half of the ac line period  $T_{2L}$  to remove the even harmonics of the ac line frequency. The resulting model is valid for frequencies sufficiently less than the ac line frequency  $\omega$ . Averaging of the rectifier output voltage is illustrated in Fig. 21.34: averaging over  $T_{2L}$  removes the ac line frequency harmonics, leaving the underlying low-frequency variations. By averaging the model of Fig. 21.33b over  $T_{2L}$ , we obtain the model of Fig. 21.33c. This step removes the second-harmonic variation in the power source.

The equivalent circuit of Fig. 21.33c is time-invariant, but nonlinear. We can now perturb and linearize as usual, to construct a small-signal ac model that describes how slow variations



**Fig. 21.34** Removal of components of  $v(t)$  at the harmonics of the ac line frequency, by averaging over one-half of the ac line period  $T_{2L}$

in  $v_{control}(t)$ ,  $v_{g,rms}$ , and the load, affect the rectifier output waveforms. Let us assume that the averaged output voltage  $\langle v(t) \rangle_{T_{2L}}$ , rectifier averaged output current  $\langle i_2(t) \rangle_{T_{2L}}$ , rms line voltage amplitude  $v_{g,rms}$ , and control voltage  $v_{control}(t)$  can be represented as quiescent values plus small slow variations:

$$\begin{aligned}\langle v(t) \rangle_{T_{2L}} &= V + \hat{v}(t) \\ \langle i_2(t) \rangle_{T_{2L}} &= I_2 + \hat{i}_2(t) \\ v_{g,rms} &= V_{g,rms} + \hat{v}_{g,rms}(t) \\ v_{control}(t) &= V_{control} + \hat{v}_{control}(t)\end{aligned}\quad (21.98)$$

with

$$\begin{aligned}V &\gg |\hat{v}(t)| \\ I_2 &\gg |\hat{i}_2(t)| \\ V_{g,rms} &\gg |\hat{v}_{g,rms}(t)| \\ V_{control} &\gg |\hat{v}_{control}(t)|\end{aligned}\quad (21.99)$$

In the averaged model of Fig. 21.33c,  $\langle i_2(t) \rangle_{T_{2L}}$  is given by

$$\begin{aligned}\langle i_2(t) \rangle_{T_{2L}} &= \frac{\langle p(t) \rangle_{T_{2L}}}{\langle v(t) \rangle_{T_{2L}}} = \frac{V_{g,rms}^2(t)}{R_e(v_{control}(t))\langle v(t) \rangle_{T_{2L}}} \\ &= f(V_{g,rms}(t), \langle v(t) \rangle_{T_{2L}}, v_{control}(t))\end{aligned}\quad (21.100)$$

This equation resembles DCM buck-boost Eq. (15.50), and linearization proceeds in a similar manner. Expansion of Eq. (21.100) in a three-dimensional Taylor series about the quiescent operating point, and elimination of higher-order nonlinear terms, leads to

$$\hat{i}_2(t) = g_2 \hat{v}_{g,rms}(t) + j_2 \hat{v}_{control}(t) - \frac{\hat{v}(t)}{r_2} \quad (21.101)$$

where

$$g_2 = \left. \frac{df(V_{g,rms}, V, V_{control})}{dv_{g,rms}} \right|_{V_{g,rms}=V_{g,rms}} = \frac{2}{R_e(V_{control})} \frac{V_{g,rms}}{V} \quad (21.102)$$

$$\left( -\frac{1}{r_2} \right) = \left. \frac{df(V_{g,rms}, \langle v \rangle_{T_{2L}}, V_{control})}{d\langle v \rangle_{T_{2L}}} \right|_{\langle v \rangle_{T_{2L}}=V} = -\frac{I_2}{V} \quad (21.103)$$

$$j_2 = \left. \frac{df(V_{g,rms}, V, v_{control})}{dv_{control}} \right|_{v_{control}=V_{control}} = -\frac{V_{g,rms}^2}{VR_e^2(V_{control})} \left. \frac{dR_e(v_{control})}{dv_{control}} \right|_{v_{control}=V_{control}} \quad (21.104)$$

A small-signal equivalent circuit based on Eq. (21.101) is given in Fig. 21.33d. Expressions for the parameters  $g_2$ ,  $j_2$ , and  $r_2$  for several controllers are listed in Table 21.1. This model is valid for the conditions of Eq. (21.99), with the additional assumption that the output voltage ripple is sufficiently small. Figure 21.33d is useful only for determining the various ac transfer functions; no information regarding dc conditions can be inferred. The ac resistance  $r_2$  is derived from the

**Table 21.1** Small-signal model parameters for several types of rectifier control schemes

Controller type	$g_2$	$j_2$	$r_2$
Average current control with feedforward, Fig. 21.18	0	$\frac{P_{av}}{VV_{control}}$	$\frac{V^2}{P_{av}}$
Current-programmed control, Fig. 21.20	$\frac{2P_{av}}{VV_{g,rms}}$	$\frac{P_{av}}{VV_{control}}$	$\frac{V^2}{P_{av}}$
Nonlinear-carrier charge control of boost rectifier, Fig. 21.25	$\frac{2P_{av}}{VV_{g,rms}}$	$\frac{P_{av}}{VV_{control}}$	$\frac{V^2}{2P_{av}}$
Boost with critical conduction mode control, Fig. 21.24	$\frac{2P_{av}}{VV_{g,rms}}$	$\frac{P_{av}}{VV_{control}}$	$\frac{V^2}{P_{av}}$
DCM buck-boost, flyback, SEPIC, or Ćuk converters	$\frac{2P_{av}}{VV_{g,rms}}$	$\frac{2P_{av}}{VD}$	$\frac{V^2}{P_{av}}$

slope of the average value of the power source output characteristic, evaluated at the quiescent operating point. The other coefficients,  $j_2$  and  $g_2$ , are also derived from the slopes of the same characteristic, taken with respect to  $v_{control}(t)$  and  $v_{g,rms}$  and evaluated at the quiescent operating point. The resistance  $R$  is the incremental resistance of the load, evaluated at the quiescent operating point. In the boost converter with hysteretic control, the transistor on-time  $t_{on}$  replaces  $v_{control}$  as the control input; likewise, the transistor duty cycle  $d$  is taken as the control input to the DCM buck-boost, flyback, SEPIC, and Ćuk converters. Harmonics are ignored for the current-programmed and NLC controllers; the expressions given in Table 21.1 assume that the converter operates in CCM with negligible harmonics.

The control-to-output transfer function is

$$\frac{\hat{v}(s)}{\hat{v}_{control}(s)} = j_2 R \| r_2 \frac{1}{1 + sC R \| r_2} \quad (21.105)$$

The line-to-output transfer function is

$$\frac{\hat{v}(s)}{\hat{v}_{g,rms}(s)} = g_2 R \| r_2 \frac{1}{1 + sCR \| r_2} \quad (21.106)$$

Thus, the small-signal transfer functions of the high-quality rectifier contain a single pole, ascribable to the output filter capacitor operating in conjunction with the incremental load resistance  $R$  and  $r_2$ , the effective output resistance of the power source. Although this model is based on the ideal rectifier, its form is similar to that of the dc-dc DCM buck-boost converter ac model of Chap. 15. This is natural, because the DCM buck-boost converter is itself a natural loss-free resistor. The major difference is that the rms value of the ac input voltage must be used, and that the second harmonic components of  $r_2$ ,  $j_2$ , and  $g_2$  must additionally be removed via averaging. Nonetheless, the equivalent circuit and ac transfer functions are of similar form.

When the rectifier drives a regulated dc-dc converter as in Fig. 21.29, then the dc-dc converter presents a constant power load to the rectifier, as illustrated in Fig. 21.30. In equilibrium, the rectifier and dc-dc converter operate with the same average power  $P_{av}$  and the same dc voltage  $V$ . The incremental resistance  $R$  of the constant power load is negative, and is given by

$$R = -\frac{V^2}{P_{av}} \quad (21.107)$$

which is equal in magnitude but opposite in polarity to the rectifier incremental output resistance  $r_2$ , for all controllers except the NLC controller. The parallel combination  $r_2||R$  then tends to an open circuit, and the control-to-output and line-to-output transfer functions become

$$\frac{\hat{v}(s)}{\hat{v}_{control}(s)} = \frac{j_2}{sC} \quad (21.108)$$

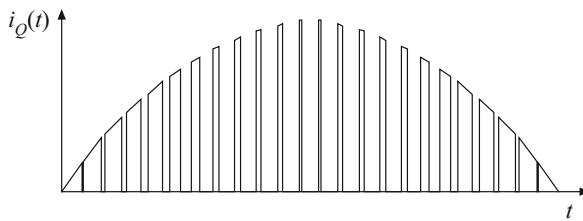
and

$$\frac{\hat{v}(s)}{\hat{v}_{g,rms}(s)} = \frac{g_2}{sC} \quad (21.109)$$

In the case of the NLC controller, the parallel combination  $r_2||R$  becomes equal to  $r_2/2$ , and Eqs. (21.105) and (21.106) continue to apply.

## 21.5 RMS Values of Rectifier Waveforms

To correctly specify the power stage elements of a near-ideal rectifier, it is necessary to compute the root-mean-square values of their currents. A typical waveform such as the transistor current of the boost converter, Fig. 21.35, is pulse-width modulated, with both the duty cycle and the peak amplitude varying with the ac input voltage. When the switching frequency is much larger than the ac line frequency, then the rms value can be well-approximated as a double integral. The square of the current is integrated first to find its average over a switching period, and the result is then integrated to find the average over the ac line period.



**Fig. 21.35** Modulated transistor current waveform, boost rectifier

Computation of the rms and average values of the waveforms of a PWM rectifier can be quite tedious, and this can impede the effective design of the power stage components. In this section, several approximations are developed, which allow relatively simple analytical expressions to be written for the rms and average values of the power stage currents, and which allow comparison of converter approaches [255, 279]. The rms transistor current in the boost rectifier is found to be quite low.

The rms value of the transistor current is defined as

$$I_{Qrms} = \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} i_Q^2(t) dt} \quad (21.110)$$

where  $T_{ac}$  is the period of the ac line waveform. The integral can be expressed as a sum of integrals over all of the switching periods contained in one ac line period:

$$I_{Qms} = \sqrt{\frac{1}{T_{ac}} T_s \sum_{n=1}^{T_{ac}/T_s} \left( \frac{1}{T_s} \int_{(n-1)T_s}^{nT_s} i_Q^2(t) dt \right)} \quad (21.111)$$

where  $T_s$  is the switching period. The quantity inside the parentheses is the value of  $i_Q^2$  averaged over the  $n$ th switching period. The summation can be approximated by a Riemann integral in the case when  $T_s$  is much less than  $T_{ac}$ . This approximation corresponds to taking the limit as  $T_s$  tends to zero, as follows:

$$\begin{aligned} I_{Qrm} &\approx \sqrt{\frac{1}{T_{ac}} \lim_{T_s \rightarrow 0} \left[ T_s \sum_{n=1}^{T_{ac}/T_s} \left( \frac{1}{T_s} \int_{(n-1)T_s}^{nT_s} i_Q^2(\tau) d\tau \right) \right]} \\ &= \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} \frac{1}{T_s} \int_t^{t+T_s} i_Q^2(\tau) d\tau dt} \\ &= \sqrt{\langle \langle i_Q^2(t) \rangle_{T_s} \rangle_{T_{ac}}} \end{aligned} \quad (21.112)$$

So  $i_Q^2(t)$  is first averaged over one switching period. The result is then averaged over the ac line period, and the square root is taken of the result.

### 21.5.1 Boost Rectifier Example

For the boost rectifier, the transistor current  $i_Q(t)$  is equal to the input current when the transistor conducts, and is zero when the transistor is off. Therefore, the average of  $i_Q^2(t)$  over one switching period is

$$\begin{aligned} \langle i_Q^2 \rangle_{T_s} &= \frac{1}{T_s} \int_t^{t+T_s} i_Q^2(t) dt \\ &= d(t) i_{ac}^2(t) \end{aligned} \quad (21.113)$$

If the input voltage is given by

$$v_{ac}(t) = V_M |\sin \omega t| \quad (21.114)$$

then the input current will be

$$i_{ac}(t) = \frac{V_M}{R_e} |\sin \omega t| \quad (21.115)$$

where  $R_e$  is the emulated resistance. With a constant output voltage  $V$ , the transistor duty cycle must obey the relationship

$$\frac{V}{v_{ac}(t)} = \frac{1}{1 - d(t)} \quad (21.116)$$

This assumes that the converter dynamics are fast compared to the ac line frequency. Substitution of Eq. (21.114) into (21.116) and solution for  $d(t)$  yields

$$d(t) = 1 - \frac{V_M}{V} |\sin \omega t| \quad (21.117)$$

Substitution of Eqs. (21.115) and (21.117) into Eq. (21.113) yields the following expression

$$\langle i_Q^2 \rangle_{T_s} = \frac{V_M^2}{R_e^2} \left( 1 - \frac{V_M}{V} |\sin \omega t| \right) \sin^2(\omega t) \quad (21.118)$$

One can now plug this expression into Eq. (21.112):

$$\begin{aligned} I_{Qrms} &= \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} \langle i_Q^2 \rangle_{T_s} dt} \\ &= \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} \frac{V_M^2}{R_e^2} \left( 1 - \frac{V_M}{V} |\sin \omega t| \right) \sin^2(\omega t) dt} \end{aligned} \quad (21.119)$$

which can be further simplified to

$$I_{Qrms} = \sqrt{\frac{2}{T_{ac}} \frac{V_M^2}{R_e^2} \int_0^{T_{ac}/2} \left( \sin^2(\omega t) - \frac{V_M}{V} \sin^3(\omega t) \right) dt} \quad (21.120)$$

This involves integration of powers of  $\sin(\omega t)$  over a complete half-cycle. The integral can be evaluated with the help of the following formula:

$$\frac{1}{\pi} \int_0^\pi \sin^n(\theta) d\theta = \begin{cases} \frac{2}{\pi} \frac{2 \cdot 4 \cdot 6 \cdots (n-1)}{1 \cdot 3 \cdot 5 \cdots n} & \text{if } n \text{ is odd} \\ \frac{1 \cdot 3 \cdot 5 \cdots (n-1)}{2 \cdot 4 \cdot 6 \cdots n} & \text{if } n \text{ is even} \end{cases} \quad (21.121)$$

This type of integral commonly arises in rms calculations involving PWM rectifiers. The values of the integral for several choices of  $n$  are listed in Table 21.2. Evaluation of the integral in Eq. (21.120) using Eq. (21.121) leads to the following result:

$$I_{Qrms} = \frac{V_M}{\sqrt{2} R_e} \sqrt{1 - \frac{8}{3\pi} \frac{V_M}{V}} = I_{ac\ rms} \sqrt{1 - \frac{8}{3\pi} \frac{V_M}{V}} \quad (21.122)$$

**Table 21.2** Solution of the integral of Eq. (21.121), for several values of  $n$

$n$	$\frac{1}{\pi} \int_0^\pi \sin^n(\theta) d\theta$
1	$\frac{2}{\pi}$
2	$\frac{1}{2}$
3	$\frac{4}{3\pi}$
4	$\frac{3}{8}$
5	$\frac{16}{15\pi}$
6	$\frac{15}{48}$

It can be seen that the rms transistor current is minimized by choosing the output voltage  $V$  to be as small as possible. The best that can be done is to choose  $V = V_M$ , which leads to

$$I_{Qrms} = 0.39I_{ac\ rms} \quad (21.123)$$

Larger values of  $V$  lead to a larger rms transistor current.

A similar analysis for the rms diode current leads to the following expression

$$I_{Drms} = I_{ac\ rms} \sqrt{\frac{8}{3\pi} \frac{V_M}{V}} \quad (21.124)$$

The choice  $V = V_M$  maximizes the rms diode current, with the result

$$I_{Drms} = 0.92I_{ac\ rms} \quad (21.125)$$

Larger values of  $V$  lead to smaller rms diode current.

Average currents can be computed in a similar way. The results are

$$\begin{aligned} I_{Qav} &= I_{ac\ rms} \frac{2\sqrt{2}}{\pi} \left( 1 - \frac{\pi}{8} \frac{V_M}{V} \right) \\ I_{Dav} &= I_{ac\ rms} \frac{V_M}{2\sqrt{2}V} \end{aligned} \quad (21.126)$$

Expressions for rms, average, and peak currents of the power stage components of the continuous conduction mode boost converter are summarized in Table 21.3. Expressions are also tabulated for flyback and SEPIC topologies, operating in the continuous conduction mode. In the case of the flyback converter, an  $L_1 - C_1$  input filter is also included. In all cases, the effects of switching ripple are neglected.

### 21.5.2 Comparison of Single-Phase Rectifier Topologies

When isolation is not a rectifier requirement, and when it is acceptable that the dc output voltage be marginally larger than the peak ac input voltage, then the boost converter is a very effective approach. For example, consider the design of a 1 kW rectifier operating from the 240 Vrms input line voltage. If the converter efficiency and power factor are both approximately unity, then the rms input current is  $I_{rms} = (1000W)/(240V) = 4.2$  A. The dc output voltage is chosen to be 380 V, or slightly larger than the peak ac input voltage. By use of Eq. (21.122), the rms transistor current is found to be 2 A. This is quite a low value—less than half of the rms input current, which demonstrates how effectively the converter utilizes the power switch. The rms diode current is 3.6 A, and the transistor and diode blocking voltages are 380 V. With a 120 A ac input voltage, the transistor and diode rms currents increase to 6.6 A and 5.1 A, respectively.

The only real drawback of the boost converter is its inability to limit inrush currents. When the dc output voltage is less than the instantaneous input voltage, the control circuit of the boost rectifier loses control of the inductor current waveform. A very large inrush current occurs when the dc output capacitor is initially charged. Additional circuitry must be employed to limit the magnitude of this current.

Buck-boost, SEPIC, and Ćuk topologies can be used to solve the inrush current problem. Since these converters have a  $d/(1-d)$  conversion ratio, their waveforms can be controlled

**Table 21.3** Summary of PWM rectifier current stresses for several converter topologies

	rms	Average	Peak
CCM boost			
Transistor	$I_{ac\ rms} \sqrt{1 - \frac{8}{3\pi} \frac{V_M}{V}}$	$I_{ac\ rms} \frac{2\sqrt{2}}{\pi} \left(1 - \frac{\pi}{8} \frac{V_M}{V}\right)$	$I_{ac\ rms} \sqrt{2}$
Diode	$I_{dc} \sqrt{\frac{16}{3\pi} \frac{V}{V_M}}$	$I_{dc}$	$2I_{dc} \frac{V}{V_M}$
Inductor	$I_{ac\ rms}$	$I_{ac\ rms} \frac{2\sqrt{2}}{\pi}$	$I_{ac\ rms} \sqrt{2}$
CCM flyback, with $n : 1$ isolation transformer and input filter			
Transistor, xfmr primary	$I_{ac\ rms} \sqrt{1 + \frac{8}{3\pi} \frac{V_M}{nV}}$	$I_{ac\ rms} \frac{2\sqrt{2}}{\pi}$	$I_{ac\ rms} \sqrt{2} \left(1 + \frac{V_M}{nV}\right)$
$L_1$	$I_{ac\ rms}$	$I_{ac\ rms} \frac{2\sqrt{2}}{\pi}$	$I_{ac\ rms} \sqrt{2}$
$C_1$	$I_{ac\ rms} \sqrt{\frac{8}{3\pi} \frac{V_M}{nV}}$	0	$I_{ac\ rms} \sqrt{2} \max\left(1, \frac{V_M}{nV}\right)$
Diode, xfmr secondary	$I_{dc} \sqrt{\frac{3}{2} + \frac{16}{3\pi} \frac{nV}{V_M}}$	$I_{dc}$	$2I_{dc} \left(1 + \frac{nV}{V_M}\right)$
CCM SEPIC, nonisolated			
Transistor	$I_{ac\ rms} \sqrt{1 + \frac{8}{3\pi} \frac{V_M}{V}}$	$I_{ac\ rms} \frac{2\sqrt{2}}{\pi}$	$I_{ac\ rms} \sqrt{2} \left(1 + \frac{V_M}{V}\right)$
$L_1$	$I_{ac\ rms}$	$I_{ac\ rms} \frac{2\sqrt{2}}{\pi}$	$I_{ac\ rms} \sqrt{2}$
$C_1$	$I_{ac\ rms} \sqrt{\frac{8}{3\pi} \frac{V_M}{V}}$	0	$I_{ac\ rms} \sqrt{2} \max\left(1, \frac{V_M}{V}\right)$
$L_2$	$I_{ac\ rms} \frac{V_M}{V} \frac{\sqrt{3}}{2}$	$\frac{I_{ac\ rms}}{\sqrt{2}} \frac{V_M}{V}$	$I_{ac\ rms} \frac{V_M}{V} \sqrt{2}$
Diode	$I_{dc} \sqrt{\frac{3}{2} + \frac{16}{3\pi} \frac{V}{V_M}}$	$I_{dc}$	$2I_{dc} \left(1 + \frac{V}{V_M}\right)$
CCM SEPIC, with $n : 1$ isolation transformer			
Transistor	$I_{ac\ rms} \sqrt{1 + \frac{8}{3\pi} \frac{V_M}{nV}}$	$I_{ac\ rms} \frac{2\sqrt{2}}{\pi}$	$I_{ac\ rms} \sqrt{2} \left(1 + \frac{V_M}{nV}\right)$
$L_1$	$I_{ac\ rms}$	$I_{ac\ rms} \frac{2\sqrt{2}}{\pi}$	$I_{ac\ rms} \sqrt{2}$
$C_1$ , xfmr primary	$I_{ac\ rms} \sqrt{\frac{8}{3\pi} \frac{V_M}{nV}}$	0	$I_{ac\ rms} \sqrt{2} \max\left(1, \frac{V_M}{nV}\right)$
Diode, xfmr secondary	$I_{dc} \sqrt{\frac{3}{2} + \frac{16}{3\pi} \frac{nV}{V_M}}$	$I_{dc}$	$2I_{dc} \left(1 + \frac{nV}{V_M}\right)$

with, in all cases,  $\frac{I_{ac\ rms}}{I_{dc}} = \sqrt{2} \frac{V}{V_M}$ , ac input voltage =  $V_M \sin(\omega t)$ , dc output voltage =  $V$ .

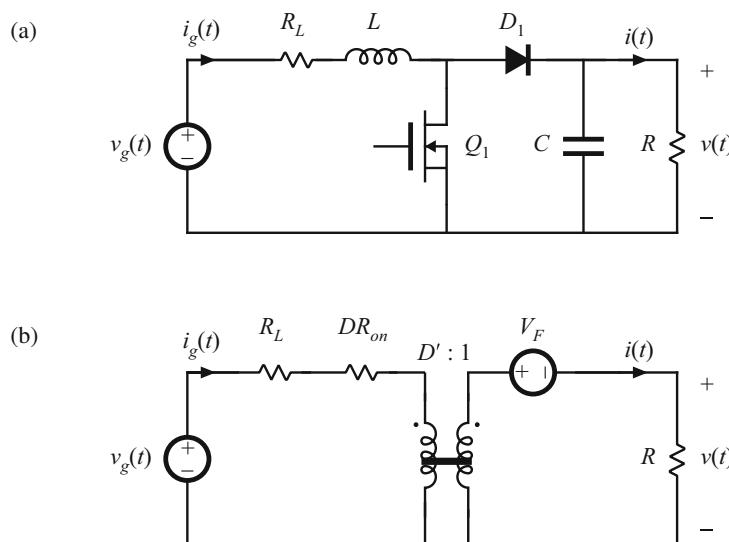
when the output voltage is any positive value, but the price paid for this capability is increased component stresses. For the same 1 kW rectifier with 240 Vrms ac input and 380 V output, the transistor rms current and peak voltage of the nonisolated SEPIC are 5.5 A and 719 V. The rms diode current is 4.85 A. The semiconductor voltage stresses can be reduced by reducing the output voltage, at the expense of increased rms currents. With a 120 V ac input voltage, the transistor and diode rms currents increase to 9.8 A and 6.1 A, respectively.

Isolation can also be obtained in the SEPIC and other topologies, as discussed in Chap. 6. The turns ratio of the isolation transformer can also be used to reduce the primary-side currents when the dc output voltage is low. But the transformer winding rms currents are higher than those of a dc–dc converter, because of the pulsating (twice-line frequency) power flow. For the 1 kW, 240 V ac input SEPIC example, with a 42 V 23.8 A dc load, and a 4:1 transformer turns ratio, the rms transformer currents are 5.5 A (primary) and 36.4 A (secondary). The rms transistor current is 6.9 A. At 120 V ac input voltage, these currents increase to 7.7 A, 42.5 A, and 11.4 A, respectively.

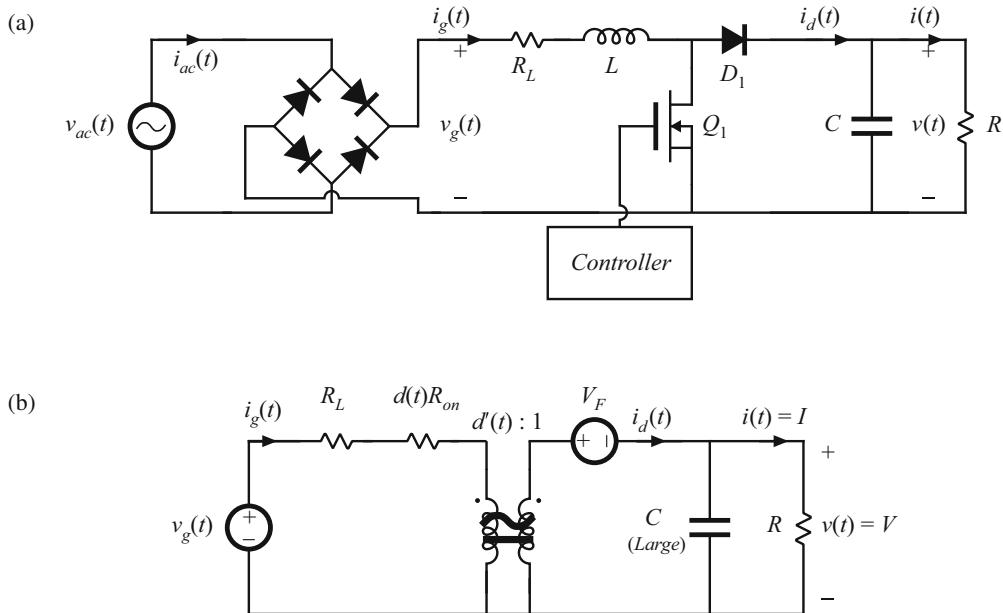
## 21.6 Modeling Losses and Efficiency in CCM High-Quality Rectifiers

As in the case of dc–dc converters, we would like to model the converter loss elements so that we can correctly specify the power stage components. The equivalent circuit approach used in the dc–dc case can be generalized to include ac–dc low-harmonic rectifiers, although the resulting equations are more complicated because of the low-frequency ac modulation of the waveforms.

A dc–dc boost converter and its steady-state equivalent circuit are illustrated in Fig. 21.36. When the converter operates in equilibrium, the model of Fig. 21.36b can be solved to determine



**Fig. 21.36** Dc–dc boost converter (a) and a steady-state equivalent circuit (b), which models the inductor resistance  $R_L$ , MOSFET on-resistance  $R_{on}$ , and diode forward voltage drop  $V_F$



**Fig. 21.37** Ac-dc boost rectifier (a) and a low-frequency equivalent circuit (b), that models converter losses and efficiency

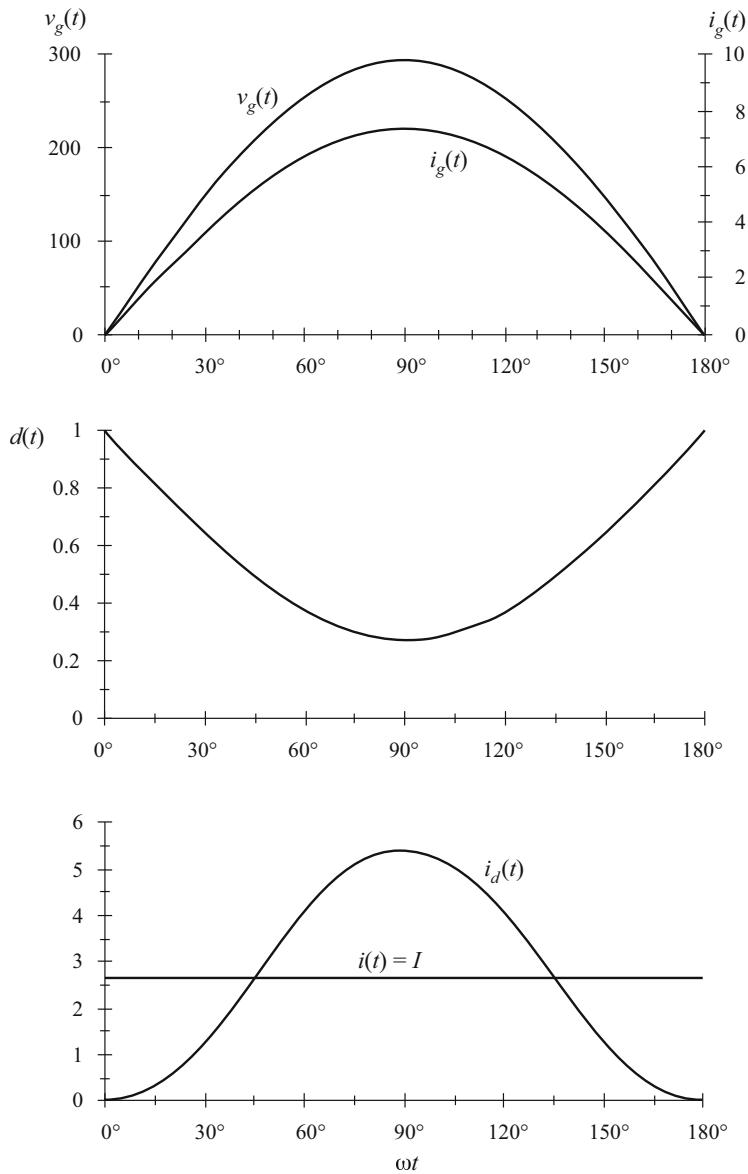
the converter losses and efficiency. In the ac-dc case, the input voltage  $v_g(t)$  is a rectified sinusoid, and the controller varies the duty cycle  $d(t)$  to cause  $i_g(t)$  to follow  $v_g(t)$  according to

$$i_g(t) = \frac{v_g(t)}{R_e} \quad (21.127)$$

The emulated resistance  $R_e$  is chosen by the controller such that the desired dc output voltage is obtained. Ac variations in  $d(t)$ ,  $v_g(t)$ , and several other system waveforms are not small, and hence the small-signal approximation employed in Chaps. 7 to 18 is not justified. We can continue to model the low-frequency components of the converter via averaging, but the resulting equivalent circuits are, in general, time-varying and nonlinear.

For the purposes of determining the rectifier efficiency, it is assumed that (1) the inductor is sufficiently small, such that it has negligible influence on the ac-line frequency components of the system waveforms and (2) the capacitor is large, so that the output voltage  $v(t)$  is essentially equal to its equilibrium dc value, with negligible low- or high-frequency ac variations. So in the ac-dc case, the model becomes as shown in Fig. 21.37. Low-frequency components ( $\ll f_s$ ) of the controller waveforms are sketched in Fig. 21.38.

To find the rectifier waveforms, losses, and efficiency, we must solve the circuit of Fig. 21.37b, under the conditions that the controller varies the duty cycle  $d(t)$  such that Eq. (21.127) is satisfied. This leads to time-varying circuit elements  $d(t)R_{on}$  and the  $d'(t) : 1$  transformer. The solution that follows involves the following steps: (1) solve for the  $d(t)$  waveform; (2) average  $i_d(t)$  to find its dc component, equal to the load current  $I$ ; and (3) find other quantities of interest such as the rectifier efficiency.



**Fig. 21.38** Typical low-frequency components of the boost rectifier waveforms

The simplified boost converter circuit model of Fig. 21.39, in which only the MOSFET conduction loss is accounted for, is solved here. However, the results can be generalized directly to the circuit of Fig. 21.37b; doing so is left as a homework problem. A similar procedure can also be followed to derive expressions for the losses and efficiencies of other rectifier topologies.

### 21.6.1 Expression for Controller Duty Cycle $d(t)$

The controller varies the duty cycle  $d(t)$  such that Eq. (21.127) is satisfied. By solving the input-side loop of Fig. 21.39, we obtain

$$i_g(t)d(t)R_{on} = v_g(t) - d'(t)v \quad (21.128)$$

Substitute Eq. (21.127) into (21.128) to eliminate  $i_g(t)$ :

$$\frac{v_g(t)}{R_e}d(t)R_{on} = v_g(t) - d'(t)v \quad (21.129)$$

$$\text{with } v_g(t) = V_M |\sin \omega t| \quad (21.130)$$

We can now solve for the duty cycle  $d(t)$ . The result is

$$d(t) = \frac{v - v_g(t)}{v - v_g(t)\frac{R_{on}}{R_e}} \quad (21.131)$$

This expression neglects the converter dynamics, an assumption that is justified when these dynamics are sufficiently faster than the ac line voltage variation. The expression also neglects operation in the discontinuous conduction mode near the zero crossing of the ac line voltage waveform. This is justified when the rectifier operates in the continuous conduction mode for most of the ac line cycle, because the power loss near the zero crossing is negligible.

### 21.6.2 Expression for the DC Load Current

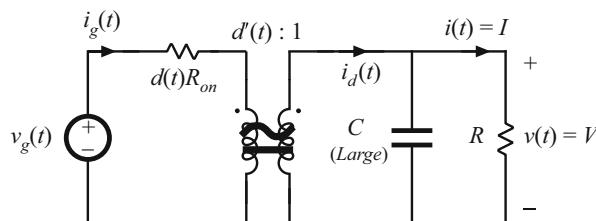
By charge balance on output capacitor  $C$ , the dc load current  $I$  is equal to the dc component of the diode current  $i_d$ :

$$I = \langle i_d \rangle_{T_{ac}} \quad (21.132)$$

Solution of Fig. 21.39 for  $i_d(t)$  yields

$$i_d(t) = d'(t)i_g(t) = d'(t)\frac{v_g(t)}{R_e} \quad (21.133)$$

From Eq. (21.131),  $d'(t) = 1 - d(t)$  is given by



**Fig. 21.39** Simplified boost power stage low-frequency equivalent circuit, in which only the MOSFET on-resistance is modeled

$$d'(t) = \frac{v_g(t) \left(1 - \frac{R_{on}}{R_e}\right)}{v - v_g(t) \frac{R_{on}}{R_e}} \quad (21.134)$$

so

$$i_d(t) = \frac{v_g^2(t)}{R_e} \frac{\left(1 - \frac{R_{on}}{R_e}\right)}{v - v_g(t) \frac{R_{on}}{R_e}} \quad (21.135)$$

Now substitute  $v_g(t) = V_M \sin \omega t$ , and integrate to find  $\langle i_d(t) \rangle_{T_{ac}}$ :

$$I = \langle i_d \rangle_{T_{ac}} = \frac{2}{T_{ac}} \int_0^{T_{ac}/2} \left( \frac{V_M^2}{R_e} \right) \frac{\left(1 - \frac{R_{on}}{R_e}\right) \sin^2(\omega t)}{\left(v - \frac{V_M R_{on}}{R_e} \sin(\omega t)\right)} dt \quad (21.136)$$

Again,  $T_{ac} = 2\pi/\omega$  is the ac line period. Equation (21.136) can be rewritten as

$$I = \frac{2}{T_{ac}} \frac{V_M^2}{VR_e} \left(1 - \frac{R_{on}}{R_e}\right) \int_0^{T_{ac}/2} \frac{\sin^2(\omega t)}{1 - a \sin(\omega t)} dt \quad (21.137)$$

$$\text{where } a = \left(\frac{V_M}{V}\right) \left(\frac{R_{on}}{R_e}\right) \quad (21.138)$$

By waveform symmetry, we need only integrate from 0 to  $T_{ac}/4$ . Also, make the substitution  $\theta = \omega t$ :

$$I = \frac{V_M^2}{VR_e} \left(1 - \frac{R_{on}}{R_e}\right) \frac{2}{\pi} \int_0^{\pi/2} \frac{\sin^2(\theta)}{1 - a \sin(\theta)} d\theta \quad (21.139)$$

Evaluation of this integral is tedious. It arises in not only the boost rectifier, but in a number of other high-quality rectifier topologies as well. The derivation is not given here, but involves the substitution  $z = \tan(\theta/2)$ , performing a partial fraction expansion of the resulting rational function of  $z$ , and integration of the results. The solution is

$$\frac{4}{\pi} \int_0^{\pi/2} \frac{\sin^2(\theta)}{1 - a \sin(\theta)} d\theta = F(a) = \frac{2}{a^2 \pi} \left(-2a - \pi + \frac{4 \sin^{-1}(a) + 2 \cos^{-1}(a)}{\sqrt{1 - a^2}}\right) \quad (21.140)$$

This equation is somewhat complicated, but it is in closed form, and can easily be evaluated by computer spreadsheet. The quantity  $a$ , which is a measure of the loss resistance  $R_{on}$  relative to the emulated resistance  $R_e$ , is typically much smaller than 1.  $F(a)$  is plotted in Fig. 21.40. The function  $F(a)$  can be well-approximated as follows:

$$F(a) \approx 1 + 0.862a + 0.78a^2 \quad (21.141)$$

For  $|a| \leq 0.15$ , the  $F(a)$  predicted by this approximate expression is within 0.1% of the exact value. If the  $a^2$  term is omitted, then the accuracy drops to  $\pm 2\%$  over the same range of  $a$ . The rectifier efficiency  $\eta$  calculated in the next section depends directly on  $F(a)$ , and hence the accuracy of  $F(a)$  coincides with the accuracy of  $\eta$ .

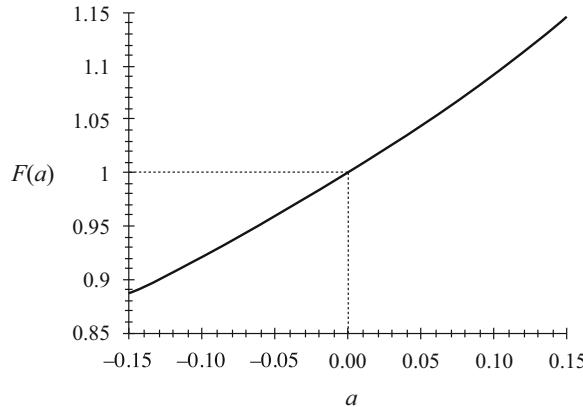


Fig. 21.40 Plot of the integral  $F(a)$  vs.  $a$

### 21.6.3 Solution for Converter Efficiency $\eta$

Now that we have found the dc load current, we can calculate the converter efficiency  $\eta$ . The average input power is

$$P_{in} = \langle p_{in}(t) \rangle_{T_{ac}} = \frac{V_M^2}{2R_e} \quad (21.142)$$

The average load power is

$$P_{out} = VI = (V) \left( \frac{V_M^2}{VR_e} \left( 1 - \frac{R_{on}}{R_e} \right) \frac{F(a)}{2} \right) \quad (21.143)$$

$$\text{where } a = \left( \frac{V_M}{V} \right) \left( \frac{R_{on}}{R_e} \right) \quad (21.144)$$

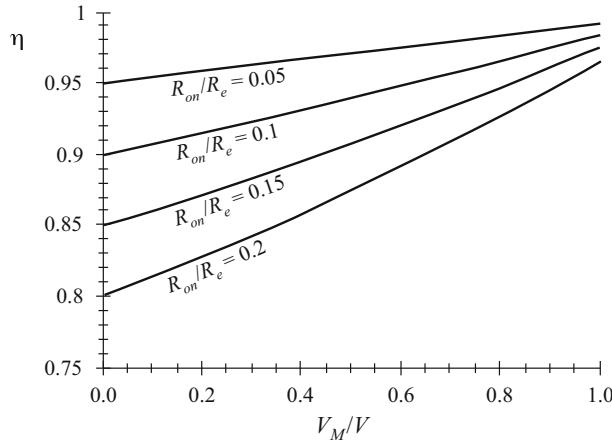
Here, we have substituted Eq. (21.139) for  $I$ . The efficiency is therefore

$$\eta = \frac{P_{out}}{P_{in}} = \left( 1 - \frac{R_{on}}{R_e} \right) F(a) \quad (21.145)$$

by substitution of Eqs. (21.142) and (21.143). If desired, the parabolic approximation for  $F(a)$ , Eq. (21.141), can be employed. This leads to

$$\eta \approx \left( 1 - \frac{R_{on}}{R_e} \right) \left( 1 + 0.862 \frac{V_M}{V} \frac{R_{on}}{R_e} + 0.78 \left( \frac{V_M}{V} \frac{R_{on}}{R_e} \right)^2 \right) \quad (21.146)$$

Equations (21.145) and (21.146) show how the efficiency varies with MOSFET on-resistance  $R_{on}$  and with ac peak voltage  $V_M$ . Equation (21.145) is plotted in Fig. 21.41. It can be seen that high efficiency is obtained when the peak ac line voltage  $V_M$  is close to the dc output voltage  $V$ . Efficiencies in the range 90% to 95% can then be obtained, even with MOSFET on-resistances as high as  $0.2R_e$ . Of course, Fig. 21.41 is optimistic because it neglects sources of loss other than the MOSFET conduction loss.



**Fig. 21.41** Boost rectifier efficiency, Eq. (21.145), accounting for MOSFET on-resistance

#### 21.6.4 Design Example

Let us utilize Fig. 21.41 to design for a given efficiency. Consider the following specifications:

Output voltage	390 V
Output power	500 W
rms input voltage	120 V
Efficiency	95%

Assume that losses other than the MOSFET conduction loss are negligible. The average input power is

$$P_{in} = \frac{P_{out}}{\eta} = \frac{500W}{0.95} = 526 \text{ W} \quad (21.147)$$

The emulated resistance is therefore

$$R_e = \frac{V_{g,rms}^2}{P_{in}} = \frac{(120V)^2}{526W} = 27.4\Omega \quad (21.148)$$

Also,

$$\frac{V_M}{V} = \frac{120\sqrt{2}V}{390V} = 0.435 \quad (21.149)$$

From Fig. 21.41, or by evaluation of the exact equation (21.145), 95% efficiency with  $V_M/V = 0.435$  occurs with  $R_{on}/R_e \approx 0.077$ . So we require a MOSFET having an on-resistance of

$$R_{on} \leq (0.077)R_e = (0.077)(27.4\Omega) = 2.11\Omega \quad (21.150)$$

Of course, other converter losses have not been accounted for, which will reduce the efficiency.

It is instructive to compare this result with that obtained using the expressions for rms current from Sect. 21.5. The rms transistor current of the ideal CCM boost converter is given by

Eq. (21.122). The rms input current will be equal to  $P_{in}/V_{g,rms} = (526\text{W})/(120\text{V}) = 4.38 \text{ A}$ . Hence, Eq. (21.122) predicts an rms transistor current of

$$\begin{aligned} I_{Qrms} &= I_{ac\ rms} \sqrt{1 - \frac{8}{3\pi} \frac{V_M}{V}} \\ &= (4.38 \text{ A}) \sqrt{1 - \frac{8}{3\pi} \frac{(120 \text{ V}) \sqrt{2}}{(390 \text{ V})}} \\ &= 3.48 \text{ A} \end{aligned} \quad (21.151)$$

Hence, the MOSFET on-resistance should be chosen according to

$$R_{on} \leq \frac{P_{in} - P_{out}}{I_{Qrms}^2} = \frac{(526 \text{ W}) - (500 \text{ W})}{(4.38 \text{ A})^2} = 2.17\Omega \quad (21.152)$$

This calculation is approximate because Eq. (21.122) was derived using the waveforms of the ideal (lossless) converter. Nonetheless, it gives an answer that is very close to the more exact result of Eq. (21.150). We would expect this approximate approach to exhibit good accuracy in this example, because of the high 95% efficiency.

## 21.7 Ideal Three-Phase Rectifiers

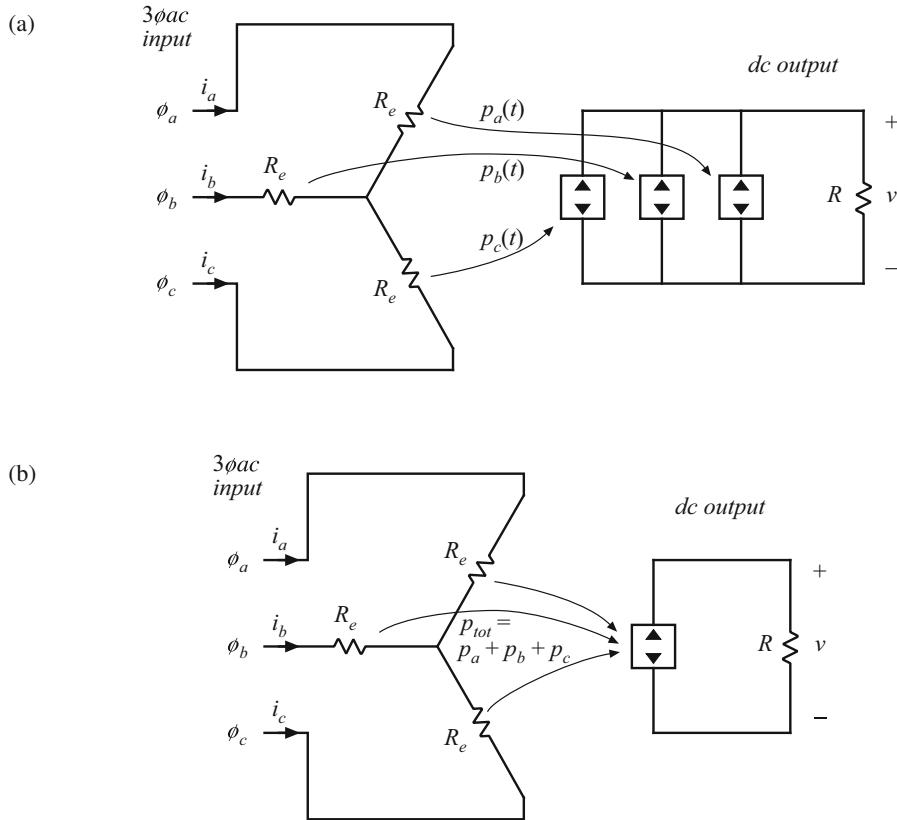
The single-phase ideal rectifier concepts of the previous sections can be generalized to cover ideal three-phase rectifiers. Figure 21.42a illustrates the properties of an ideal three-phase rectifier, which presents a balanced resistive load to the utility system. A three-phase converter system is controlled such that resistor emulation is obtained in each input phase. The rectifier three-phase input port can then be modeled by per-phase effective resistances  $R_e$ , as illustrated in Fig. 21.42a. The instantaneous powers apparently consumed by these resistors are transferred to the rectifier dc output port. The rectifier output port can therefore be modeled by power sources equal to the instantaneous powers flowing into the effective resistances  $R_e$ . It is irrelevant whether the three power sources are connected in series or in parallel; in either event, they can be combined into a single source equal to the total three-phase instantaneous input power as illustrated in Fig. 21.42b.

If the three-phase ac input voltages are

$$\begin{aligned} v_{an}(t) &= V_M \sin(\omega t) \\ v_{bn}(t) &= V_M \sin(\omega t - 120^\circ) \\ v_{cn}(t) &= V_M \sin(\omega t - 240^\circ) \end{aligned} \quad (21.153)$$

then the instantaneous powers flowing into the phase  $a$ ,  $b$ , and  $c$  effective resistances  $R_e$  are

$$\begin{aligned} p_a(t) &= \frac{v_{an}^2(t)}{R_e} = \frac{V_M^2}{2R_e} (1 - \cos(2\omega t)) \\ p_b(t) &= \frac{v_{bn}^2(t)}{R_e} = \frac{V_M^2}{2R_e} (1 - \cos(2\omega t - 240^\circ)) \\ p_c(t) &= \frac{v_{cn}^2(t)}{R_e} = \frac{V_M^2}{2R_e} (1 - \cos(2\omega t - 120^\circ)) \end{aligned} \quad (21.154)$$



**Fig. 21.42** Development of the ideal three-phase rectifier model: (a) three ideal single-phase rectifiers, (b) combination of the three power sources into an equivalent single power source

Each instantaneous phase power contains a dc term  $V_M^2/(2R_e)$ , and a second-harmonic term. The total instantaneous three-phase power is

$$p_{tot}(t) = p_a(t) + p_b(t) + p_c(t) = \frac{3}{2} \frac{V_M^2}{R_e} \quad (21.155)$$

This is the instantaneous power which flows out of the rectifier dc output port. Note that the second harmonic terms add to zero, such that the rectifier instantaneous output power is constant. This is a consequence of the fact that the instantaneous power flow in any balanced three-phase ac system is constant. So, unlike the single-phase case, the ideal three-phase rectifier can supply constant instantaneous power to a dc load, without the need for internal low-frequency energy storage.

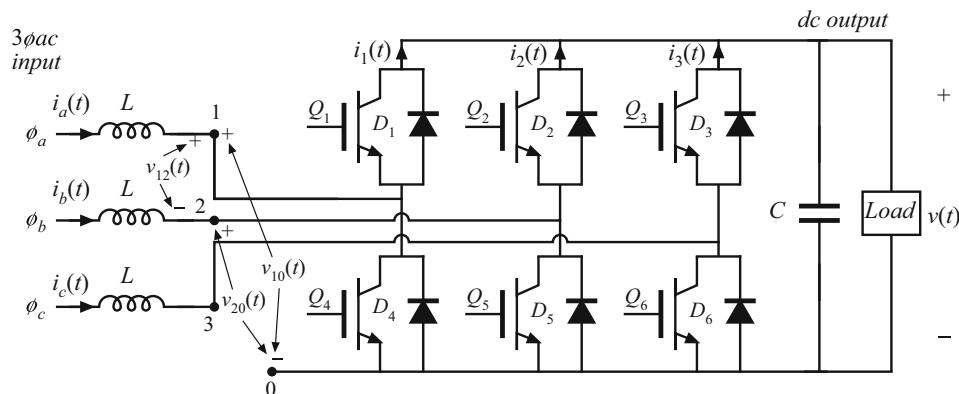
A variety of 3øac-dc PWM rectifiers are known; a few of the many references on this subject are listed in the references [8, 22, 280–294]. The most well-known topology is the three-phase ac-dc boost rectifier, illustrated in Fig. 21.43. This converter requires six SPST current-bidirectional two-quadrant switches. The inductors and capacitor filter the high-frequency switching harmonics, and have little influence on the low-frequency ac components of the wave-

forms. The switches of each phase are controlled to obtain input resistor emulation, either with a multiplying controller scheme similar to Fig. 21.5, or with some other approach. To obtain undistorted line current waveforms, the dc output voltage  $V$  must be greater than or equal to the peak line-to-line ac input voltage  $V_{L,pk}$ . In a typical realization,  $V$  is somewhat greater than  $V_{L,pk}$ . This converter resembles the voltage-source inverter, discussed briefly in Chap. 4, except that the converter is operated as a rectifier, and the converter input currents are controlled via high-frequency pulse-width modulation.

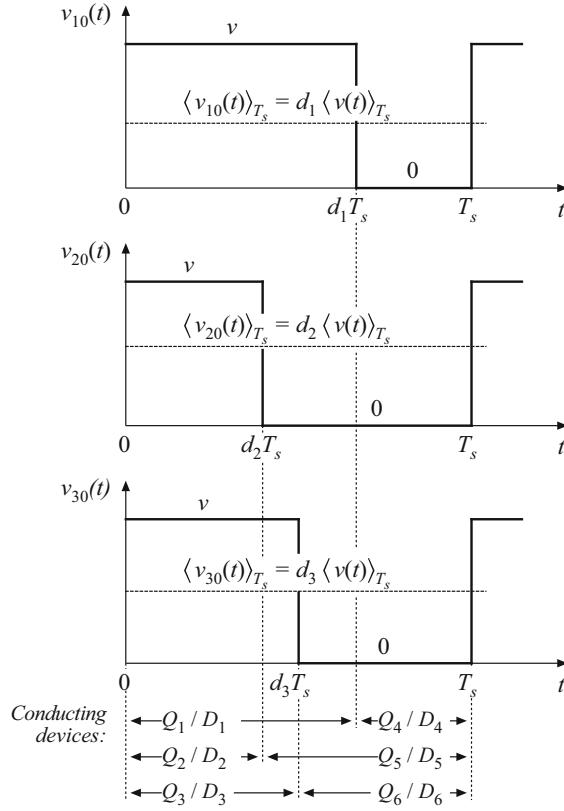
The three-phase boost rectifier of Fig. 21.43 has several attributes that make it the leading candidate for most 3øac-dc rectifier applications. The ac input currents are nonpulsating, and hence very little additional input EMI filtering is required. As in the case of the single-phase boost rectifier, the rms transistor currents and also the conduction losses of the three-phase boost rectifier are low relative to other 3øac-dc topologies such as the current source inverter. The converter is capable of bidirectional power flow. A disadvantage is the requirement for six active devices: when compared with a dc-dc converter of similar ratings, the active semiconductor utilization (discussed in Chap. 6) is low. Also, since the rectifier has a boost characteristic, it is not suitable for direct replacement of traditional buck-type phase-controlled rectifiers. The circuit of Fig. 21.43 coincides with the voltage-source inverter of Fig. 4.14; indeed, the current-bidirectional switches allow bidirectional current flow and also power flow in either direction.

The literature contains a wide variety of schemes for controlling the switches of a six-switch three-phase bridge network, which are applicable for control of the switches of Fig. 21.43. The basic operation of the converter can be most easily understood by assuming that the switches are controlled via simple sinusoidal pulse-width modulation. Transistor  $Q_1$  is driven with duty cycle  $d_1(t)$ , while transistor  $Q_4$  is driven by the complement of  $d_1(t)$ , or  $d'_1(t) = 1 - d_1(t)$ . Transistors  $Q_2$  and  $Q_5$  are driven with duty cycles  $d_2(t)$  and  $d'_2(t)$ , respectively, and transistors  $Q_3$  and  $Q_6$  are driven with duty cycles  $d_3(t)$  and  $d'_3(t)$ , respectively. The switch voltage waveforms of Fig. 21.44 are obtained. The average switch voltages are

$$\begin{aligned}\langle v_{10}(t) \rangle_{T_s} &= d_1(t) \langle v(t) \rangle_{T_s} \\ \langle v_{20}(t) \rangle_{T_s} &= d_2(t) \langle v(t) \rangle_{T_s} \\ \langle v_{30}(t) \rangle_{T_s} &= d_3(t) \langle v(t) \rangle_{T_s}\end{aligned}\quad (21.156)$$



**Fig. 21.43** Boost-type three-phase ac-dc PWM rectifier

**Fig. 21.44** Switch waveforms, 3φac–dc boost rectifier

The averaged line-to-line switch voltages are therefore

$$\begin{aligned}\langle v_{12}(t) \rangle_{T_s} &= \langle v_{10}(t) \rangle_{T_s} - \langle v_{20}(t) \rangle_{T_s} = (d_1(t) - d_2(t)) \langle v(t) \rangle_{T_s} \\ \langle v_{23}(t) \rangle_{T_s} &= \langle v_{20}(t) \rangle_{T_s} - \langle v_{30}(t) \rangle_{T_s} = (d_2(t) - d_3(t)) \langle v(t) \rangle_{T_s} \\ \langle v_{31}(t) \rangle_{T_s} &= \langle v_{30}(t) \rangle_{T_s} - \langle v_{10}(t) \rangle_{T_s} = (d_3(t) - d_1(t)) \langle v(t) \rangle_{T_s}\end{aligned}\quad (21.157)$$

In a similar manner, the average switch currents can be shown to be

$$\begin{aligned}\langle i_1(t) \rangle_{T_s} &= d_1(t) \langle i_a(t) \rangle_{T_s} \\ \langle i_2(t) \rangle_{T_s} &= d_2(t) \langle i_b(t) \rangle_{T_s} \\ \langle i_3(t) \rangle_{T_s} &= d_3(t) \langle i_c(t) \rangle_{T_s}\end{aligned}\quad (21.158)$$

Equations (21.157) and (21.158) lead to the circuit-averaged model of Fig. 21.45.

With sinusoidal PWM, the duty cycles are varied sinusoidally in synchronism with the ac line, as follows:

$$\begin{aligned} d_1(t) &= D_0 + \frac{1}{2}D_m \sin(\omega t - \varphi) \\ d_2(t) &= D_0 + \frac{1}{2}D_m \sin(\omega t - \varphi - 120^\circ) \\ d_3(t) &= D_0 + \frac{1}{2}D_m \sin(\omega t - \varphi - 240^\circ) \end{aligned} \quad (21.159)$$

where  $\omega$  is the ac line frequency. Since each instantaneous duty cycle must lie in the interval  $[0,1]$ , the dc bias  $D_0$  is required. The factor  $D_m$  is called the *modulation index*; for  $D_0 = 0.5$ ,  $D_m$  must be less than or equal to one. Other choices of  $D_0$  further restrict  $D_m$ . In general, the modulation index can be defined as equal to the peak-to-peak amplitude of the fundamental component of the duty cycle variation.

If the switching frequency is sufficiently large, then filter inductors  $L$  can be small in value, such that they have negligible effect on the low-frequency ac waveforms. The averaged switch voltage  $\langle v_{12}(t) \rangle_{T_s}$  then becomes approximately equal to the ac line-line voltage  $v_{ab}(t)$ :

$$\langle v_{12}(t) \rangle_{T_s} = (d_1(t) - d_2(t))\langle v(t) \rangle_{T_s} \approx v_{ab}(t) \quad (21.160)$$

Substitution of Eqs. (21.153) and (21.159) leads to

$$\frac{1}{2}D_m [\sin(\omega t - \varphi) - \sin(\omega t - \varphi - 120^\circ)] \langle v(t) \rangle_{T_s} = V_M [\sin(\omega t) - \sin(\omega t - 120^\circ)] \quad (21.161)$$

For small  $L$ , the angle  $\varphi$  must tend to zero, and hence the sinusoidal terms in Eq. (21.161) cancel out. In steady state, the dc output voltage is  $\langle v(t) \rangle_{T_s} = V$  Eq. (21.161) then becomes

$$\frac{1}{2}D_m V = V_M \quad (21.162)$$

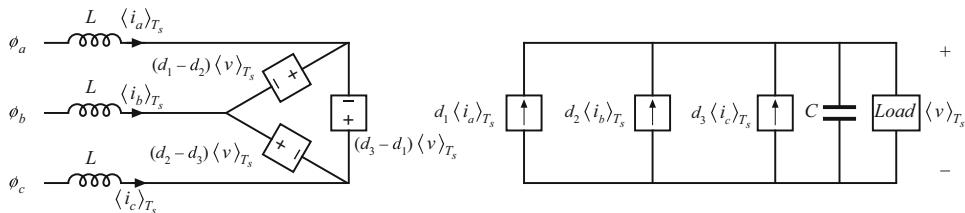
Solution for the dc output voltage  $V$  leads to

$$V = \frac{2V_M}{D_m} \quad (21.163)$$

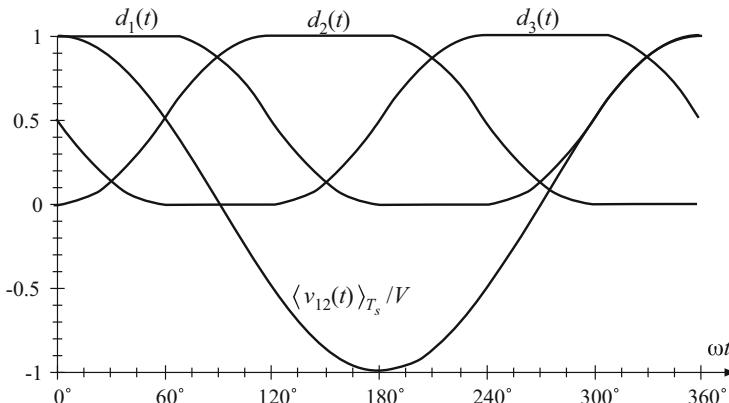
Equation (21.163) can be written in terms of the peak line-to-line voltage  $V_{L,pk}$ , as

$$V = \frac{2}{\sqrt{3}} \frac{V_{L,pk}}{D_m} = 1.15 \frac{V_{L,pk}}{D_m} \quad (21.164)$$

With  $D_m \leq 1$ , the dc output voltage  $V$  must be greater than or equal to 1.15 times the peak line-to-line ac input voltage. Thus, the rectifier has a boost characteristic.



**Fig. 21.45** Averaged model of the open-loop  $3\varphi$ ac-dc boost rectifier

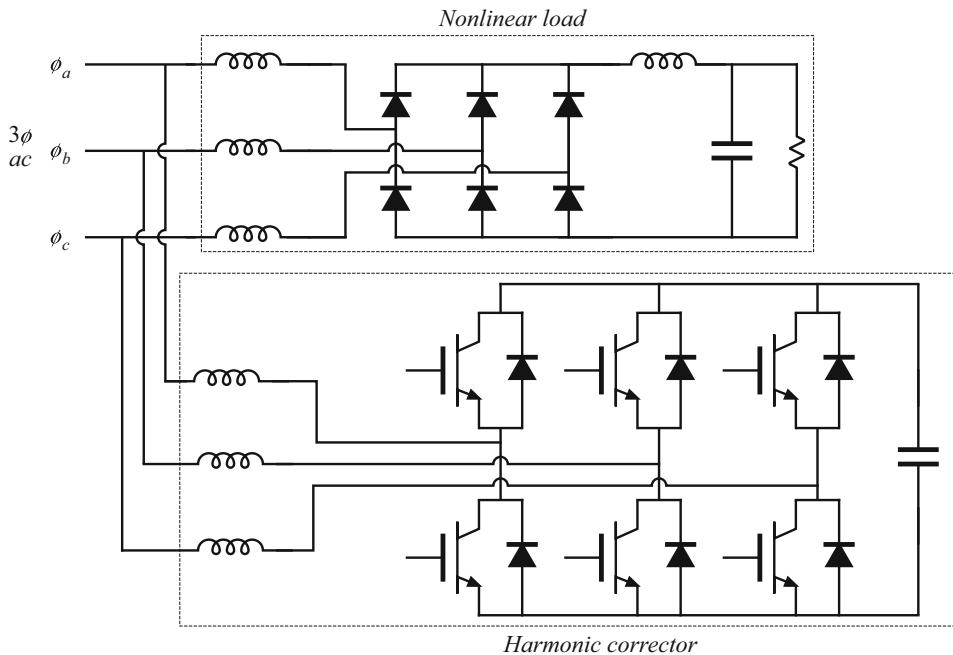


**Fig. 21.46** A modulation strategy that leads to a dc output voltage equal to the peak input line-line voltage

The sinusoidal PWM approach of Eq. (21.159) is not the only way to vary the duty cycles to obtain sinusoidal ac voltages and currents. For example, triplen harmonics can be added to the duty-cycle expressions of Eq. (21.159). These triplen harmonics cancel out in Eq. (21.157), such that the average inverter input voltages  $\langle v_{12}(t) \rangle_{T_s}$ ,  $\langle v_{23}(t) \rangle_{T_s}$ , and  $\langle v_{31}(t) \rangle_{T_s}$  contain only fundamental. Figure 21.46 illustrates duty cycle variations that lead to a dc output voltage  $V$  equal to  $V_{L,pk}$ . The effective modulation index in this case is 1.15. The ac-side voltages and currents are again undistorted. Further increases in the modulation index can be attained only by introduction of distortion in the ac-side voltages and currents. Of course, in practice the duty-cycle modulations are usually generated by the feedback loops that control the input current waveforms to attain resistor emulation.

Three-phase ac-to-dc rectifiers having buck, buck-boost, or other characteristics are possible, but find much less use than the boost topology. A 3Øac-dc rectifier system can also be constructed simply using three separate single-phase rectifiers [273]; however, each single-phase rectifier must then contain transformer isolation, leading to substantially increased switch stress and loss. Other unconventional approaches to three-phase low-harmonic rectification have also been recently explored, such as the Vienna rectifier [292, 294], single-switch approaches [285–291], and other circuits [281–284, 293].

Yet another approach to solving the problem of three-phase rectifier harmonics is the *harmonic correction* scheme illustrated in Fig. 21.47. An active six-switch three-phase bridge removes the harmonics generated by a nonlinear three-phase load such as an uncontrolled rectifier. The harmonic corrector is controlled such that its ac line currents contain harmonics that are equal in magnitude but opposite in phase to the harmonics generated by the nonlinear load. No average power flows into the harmonic corrector. The total kVA rating of the harmonic corrector semiconductor devices depends on the magnitudes of the harmonics produced by the nonlinear load. If the THD generated by the load is not too large, then the harmonic corrector scheme requires less total active silicon than the CCM boost-type rectifier of Fig. 21.43. But if the uncontrolled rectifier contains small ac line inductances, such that it operates in the discontinuous conduction mode with large THD, then it is probably better to simply replace the uncontrolled rectifier with the CCM boost-type rectifier of Fig. 21.43.



**Fig. 21.47** A harmonic corrector, based on the  $3\phi$ ac-dc boost converter of Fig. 21.43

## 21.8 Summary of Key Points

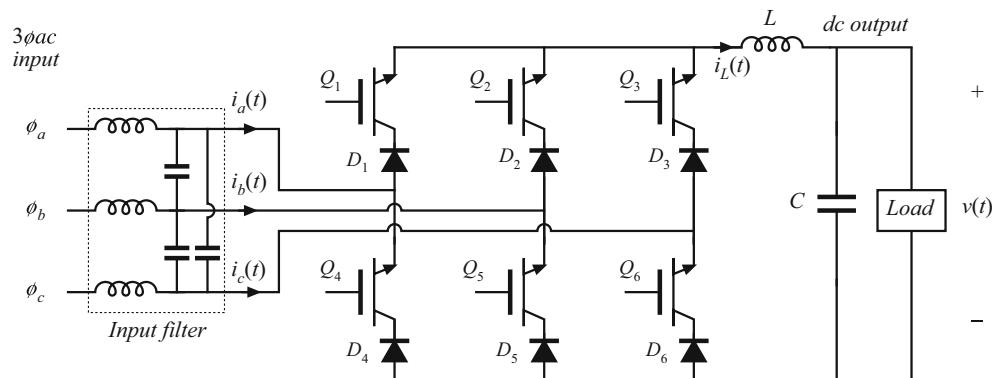
1. The ideal rectifier presents an effective resistive load, the emulated resistance  $R_e$ , to the ac power system. The power apparently “consumed” by  $R_e$  is transferred to the dc output port. In a three-phase ideal rectifier, input resistor emulation is obtained in each phase. In both the single-phase and three-phase cases, the output port follows a power source characteristic, dependent on the instantaneous ac input power. Ideal rectifiers can perform the function of low-harmonic rectification, without need for low-frequency reactive elements.
2. The dc–dc boost converter, as well as other converters capable of increasing the voltage according to Eq. (21.12), can be adapted to the ideal rectifier application. A control system causes the input current to be proportional to the input voltage. The converter may operate in CCM, DCM, or in both modes. The mode boundary can be expressed as a function of  $R_e$ ,  $2L/T_s$ , and the instantaneous voltage ratio  $v_g(t)/V$ . A well-designed average current controller leads to resistor emulation regardless of the operating mode; however, other schemes may lead to distorted current waveforms when the mode boundary is crossed.
3. In a single-phase system, the instantaneous ac input power is pulsating, while the dc load power is constant. Whenever the instantaneous input and output powers are not equal, the ideal rectifier system must contain energy storage. A large capacitor is commonly employed; the voltage of this capacitor must be allowed to vary independently, as necessary to store and release energy. A slow feedback loop regulates the dc component of the capacitor voltage, to ensure that the average ac input power and dc load power are balanced.

4. RMS values of rectifiers waveforms can be computed by double integration. In the case of the boost converter, the rms transistor current can be as low as 39% of the rms ac input current, when the dc output voltage  $V$  is close in value to the peak ac input voltage  $V_M$ . Other converter topologies such as the buck–boost, SEPIC, and Ćuk converters exhibit significantly higher rms transistor currents but are capable of limiting the converter inrush current.
5. In the three-phase case, a boost-type rectifier based on the PWM voltage-source inverter also exhibits low rms transistor currents. This approach requires six active switching elements, and its dc output voltage must be greater than the peak input line-to-line voltage. Average current control can be used to obtain input resistor emulation. An equivalent circuit can be derived by averaging the switch waveforms. The converter operation can be understood by assuming that the switch duty cycles vary sinusoidally; expressions for the average converter waveforms can then be derived.
6. Converter losses and efficiency can be modeled using the steady-state equivalent circuit models of Chap. 3, with a time-varying duty cycle. The output current is averaged over one ac line period, to determine its dc component. The converter losses and efficiency can then be computed. This approach is approximate, in that (i) it assumes that the converter dynamics are much faster than the ac line frequency and (ii) it neglects operation in the discontinuous conduction mode.
7. Average current control involves direct regulation of the low-frequency components of the rectifier input current to follow the input voltage. Feedforward can also be added, to cancel the influence of ac line voltage variations on the dc output voltage.
8. Current-programmed control can also be adapted to attain input resistor emulation in rectifiers. The programmed current reference signal  $i_c(t)$  is made proportional to the ac input voltage. The difference between  $i_c(t)$  and the average inductor current leads to distortion, owing to the inductor current ripple and the need for a stabilizing artificial ramp. Several approaches are known for reducing the resulting harmonic distortion of the line current waveform.
9. Hysteretic control, particularly with 100% current ripple, has a simple controller implementation. The disadvantages are variable switching frequency, and increased peak currents.
10. Nonlinear carrier control also leads to a simple controller implementation, and has the advantage of CCM operation with small peak transistor current.
11. The outer low-bandwidth control system, which regulates the dc output voltage to balance the rectifier and load powers, can be modeled by averaging the rectifier waveforms over one-half of the ac line period  $T_{2L}$ . This causes the dc-side system equations to become time-invariant. A small-signal model is then obtained by perturbation and linearization.
12. The inner high-bandwidth control system, which regulates the ac input current waveform to attain resistor emulation, is in general highly nonlinear. However, in the case of the boost rectifier, a valid small-signal model can be derived. This approach is unsuccessful in the case of other converters; one must then resort to other approaches such as the quasi-static approximation or simulation.

## PROBLEMS

- 21.1** The boost converter of Fig. 21.5 is replaced by a buck–boost converter. Inductor energy storage has negligible influence on the low-frequency components of the converter waveforms. The average load power is  $P_{load}$ . The dc output voltage is  $V$  and the sinusoidal ac input voltage has peak amplitude  $V_M$ .
- Determine expressions for the duty cycle variations  $d(t)$  and the inductor current variation  $i(t)$ , assuming that the converter operates in the continuous conduction mode.
  - Derive the conditions for operation in the continuous conduction mode. Manipulate your result to show that the converter operates in CCM when  $R_e$  is less than  $R_{e,crit}(L, T_s, v_g(t), V)$ , and determine  $R_{e,crit}$ .
  - For what values of  $R_e$  does the converter always operate in CCM? in DCM?
  - The ac input voltage has rms amplitude in the range 108 V to 132 V. The maximum load power is 100 W, and the minimum load power is 10 W. The dc output voltage is 120 V. The switching frequency is 75 kHz. What value of  $L$  guarantees that the converter always operates in CCM? in DCM?
- 21.2** Derive expressions for the input characteristics of the buck–boost converter, similar to Eqs. (21.25) to (21.33). Sketch the converter input characteristics, and label the CCM–DCM boundary.
- 21.3** Derive expressions for the rms transistor and diode currents of rectifiers based on the single-phase CCM Ćuk topology. Express your results in forms similar to those of Table 21.3.
- 21.4** To obtain an isolated dc output, the boost converter in Fig. 21.5 is replaced by the full-bridge transformer-isolated CCM boost converter of Fig. 6.36. Derive an expression for the rms transistor current. Express your result as a function of  $I_{ac\ rms}$ ,  $n$ ,  $V$ , and  $V_M$ .
- 21.5** Comparison of CCM boost and isolated SEPIC topologies as universal-input single-phase rectifiers. You are given that the dc output voltage is  $V = 400$  V, the load power is  $P = 500$  W, and the rms input voltage varies between 90 and 270 V, such that the peak ac input voltage  $V_M$  varies between  $V_{M\ min} = 127$  V and  $V_{M\ max} = 382$  V. Define the transistor stress  $S$  as the product of the worst-case peak transistor voltage and the worst-case rms transistor current. It is desired to minimize  $S$ .
- Determine  $S$  for the boost converter in this application.
  - Briefly discuss your result of part (a): if universal input operation was not required, and hence  $V_M = 382$  V always, what  $S$  would result?  
In the isolated SEPIC, the transformer turns ratio  $n : 1$  can be chosen to optimize the design.
  - Express  $S$  for the SEPIC as a function of  $n$ ,  $V$ ,  $P$ ,  $V_{M\ min}$ , and  $V_{M\ max}$ .
  - Choose  $n$  for the SEPIC such that  $S$  is minimized in this application. Compare with the results of parts (a) and (b).
- 21.6** In the boost-type dc-3Øac rectifier of Fig. 21.43, the ac-side inductances  $L$  are not small: they exhibit line frequency impedances that should not be ignored. The three-phase ac voltages are given by Eq. (21.153), and the duty cycles are modulated as in Eq. (21.159). The converter operates in the continuous conduction mode.
- Determine the magnitudes and phases of the line-to-neutral average voltages at the ac inputs to the switch network. Express your result in terms of  $D_m$ ,  $V$ , and  $\varphi$ .

- (b) Determine the real power  $P$  and reactive power  $Q$  drawn from the  $3\varphi$ ac source. Express your results as functions of  $V_M$ ,  $V$ ,  $D_m$ ,  $\varphi$ , and  $\omega L$ .
- (c) How must  $\varphi$  be chosen to obtain unity power factor?
- 21.7** In the boost-type dc- $3\varphi$ ac rectifier of Fig. 21.43, the switch duty ratios are modulated as illustrated in Fig. 21.46. When the inductances  $L$  are sufficiently small, a dc output voltage  $V$  equal to the peak line-to-line ac input voltage can be obtained, with undistorted ac line currents. As illustrated in Fig. 21.46,  $d_1(t)$  is equal to 1 for  $0^\circ \leq \omega t \leq 60^\circ$ , where  $\omega t = 0^\circ$  when  $\langle v_{12}(t) \rangle_{T_s} = V$ .
- (a) Derive expressions for  $d_2(t)$  and  $d_3(t)$ , over the interval  $0^\circ \leq \omega t \leq 60^\circ$ .
- (b) State how  $d_1(t)$ ,  $d_2(t)$ , and  $d_3(t)$  should vary over each  $60^\circ$  interval.
- 21.8** The buck-type  $3\varphi$ ac-dc rectifier of Fig. 21.48 operates in the continuous conduction mode. Transistors  $Q_1$  to  $Q_6$  operate with duty cycles  $d_1(t)$  to  $d_6(t)$ , respectively.



**Fig. 21.48** Buck-type  $3\varphi$ ac-dc rectifier, Problem 21.8

- (a) Determine the constraints on switch operation. Which transistors must not conduct simultaneously? Which duty cycles must total unity?
- (b) Average the  $3\varphi$  bridge switch network, to determine expressions for the average ac-side switch currents  $\langle i_a(t) \rangle_{T_s}$ ,  $\langle i_b(t) \rangle_{T_s}$ , and  $\langle i_c(t) \rangle_{T_s}$ .
- (c) Show that the average dc-side switch voltage can be expressed as

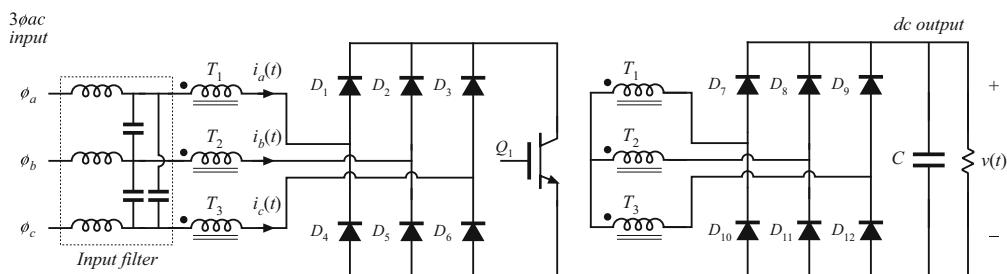
$$\langle v_d(t) \rangle_{T_s} = (d_1(t) - d_4(t))\langle v_{an}(t) \rangle_{T_s} + (d_2(t) - d_5(t))\langle v_{bn}(t) \rangle_{T_s} + (d_3(t) - d_6(t))\langle v_{cn}(t) \rangle_{T_s}$$

- (d) The duty cycles are varied as follows:

$$\begin{aligned} d_1(t) &= \frac{1}{3} + \frac{1}{2}D_m \sin(\omega t - \varphi) \\ d_2(t) &= \frac{1}{3} + \frac{1}{2}D_m \sin(\omega t - \varphi - 120^\circ) \\ d_3(t) &= \frac{1}{3} + \frac{1}{2}D_m \sin(\omega t - \varphi - 240^\circ) \\ d_4(t) &= \frac{1}{3} - \frac{1}{2}D_m \sin(\omega t - \varphi) \\ d_5(t) &= \frac{1}{3} - \frac{1}{2}D_m \sin(\omega t - \varphi - 120^\circ) \\ d_6(t) &= \frac{1}{3} - \frac{1}{2}D_m \sin(\omega t - \varphi - 240^\circ) \end{aligned}$$

with the ac input voltages given by Eq. (21.153). The input filter has negligible effect of the low-frequency components of the converter waveforms. Determine the steady-state dc output voltage  $V$ , as a function of  $V_M$ ,  $D_m$ , and  $\varphi$ .

- (e) Determine the power factor. You may assume that the input filter completely removes the switching harmonics from the currents  $i_a(t)$ ,  $i_b(t)$ , and  $i_c(t)$ . However, the input filter elements consume or supply negligible line frequency reactive power.
- 21.9** In the three-phase DCM flyback rectifier of Fig. 21.49, the input filter has negligible effect on the low-frequency components of the input ac waveforms. The transistor operates with switching frequency  $f_s$  and duty cycle  $d$ . Flyback transformers  $T_1$ ,  $T_2$ , and  $T_3$  each have magnetizing inductance  $L$  referred to the primary, turns ratio  $n : 1$ , and have negligible leakage inductances.



**Fig. 21.49** Isolated 3 $\varphi$ ac–dc rectifier based on the flyback converter operating in discontinuous conduction mode, Problem 21.9

- (a) Determine expressions for the low-frequency components of the ac input and dc output currents.  
 (b) Derive an averaged equivalent circuit model for the converter, and give expressions for the element values.  
 (c) Derive the conditions for operation in the discontinuous conduction mode.
- 21.10** Power stage design of a universal-input boost rectifier. The objective of this problem is to work out the power stage design of a low-harmonic rectifier based on the boost converter. This converter is to be designed to operate anywhere in the world, and hence the input voltage may vary over the range 90 to 270 Vrms, 50 to 60 Hz. The converter produces a regulated 385 V dc output, at 1000 W. The switching frequency  $f_s$  is 100 kHz. You may assume that the controller operates perfectly, to produce an undistorted ac line current waveform and a well-regulated dc output voltage.
- (a) Derive an expression for how the duty cycle  $d(t)$  will vary over the ac line cycle. You may neglect converter dynamics and losses. Sketch  $d(t)$  under conditions of maximum and minimum ac line voltage.  
 (b) Specify the inductor:  
 (i) Specify the value of  $L$  such that, at the peak of the sinusoidal input voltage, and under worst-case conditions, the inductor current ripple  $\Delta i_g$  is 20% of the instantaneous low-frequency current  $i_g(t)$ .

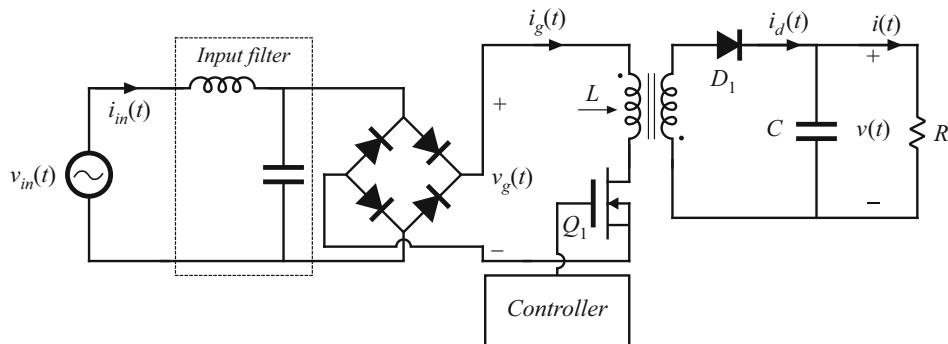
- (ii) Specify the worst-case values of the peak and rms inductor current, assuming 100% efficiency.
- (c) Determine the worst-case rms currents of the MOSFET and diode, assuming 100% efficiency.
- (d) Specify the value of  $C$  that leads to a worst-case low-frequency ( $\ll f_s$ ) output voltage peak-peak ripple of 5 V.
- (e) Given the following loss elements

Inductor winding resistance  $0.1\Omega$   
 MOSFET on-resistance  $0.4\Omega$   
 Diode forward voltage drop  $1.5\text{ V}$   
 Switching loss: model as  $i_g^2(t)(0.25\Omega)$

For a constant  $1000\text{ W}$  load, and assuming that the controller operates perfectly as described above, find the rectifier efficiency

- (i) at an ac input voltage of  $90\text{ V}$  rms
- (ii) at an ac input voltage of  $270\text{ V}$  rms

- 21.11** The flyback converter shown in Fig. 21.50 operates in the continuous conduction mode. The MOSFET has on-resistance  $R_{on}$ , and diode  $D_1$  has a constant forward voltage drop  $V_D$ . All other loss elements can be neglected. The turns ratio of the flyback transformer is  $1:1$ . The controller varies the duty cycle such that  $\langle i_g(t) \rangle_{T_S}$  is equal to  $v_g(t)/R_e$ , where  $R_e$  is the emulated resistance. The input voltage is  $v_{in}(t) = V_M \sin(\omega t)$ . The input filter removes the switching harmonics from the input current  $i_g(t)$ , but has negligible effect on the low-frequency components of the converter waveforms.

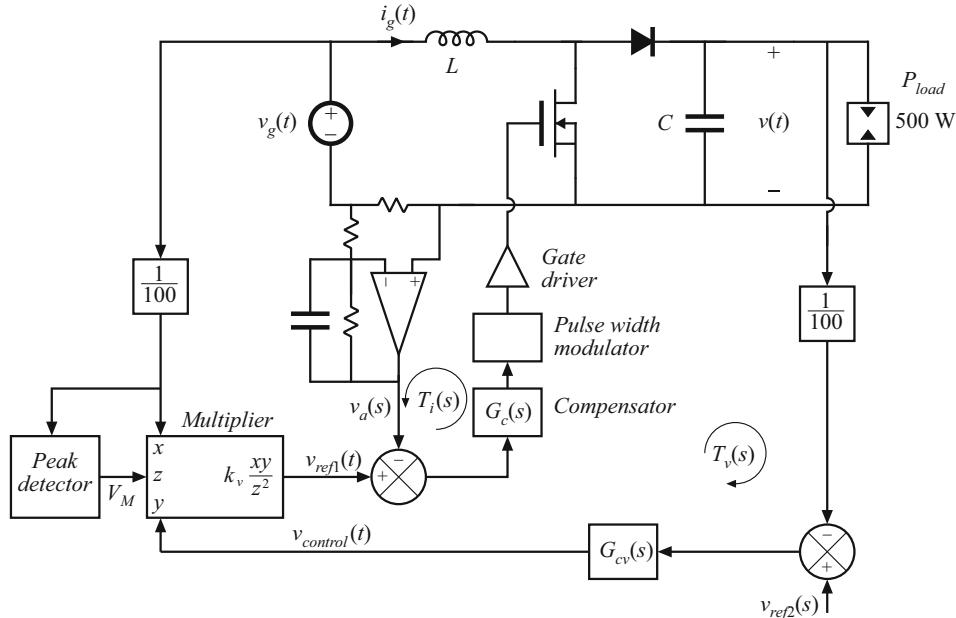


**Fig. 21.50** Low-harmonic rectifier system based on the CCM flyback converter, Problem 21.11

- (a) Derive an expression for the rectifier efficiency, in terms of  $V_M$ ,  $V$ ,  $V_D$ ,  $R_{on}$ , and  $R_e$ .
- (b) Given the following values, find the value of MOSFET on-resistance which leads to an efficiency of 96%.

rms input voltage	120 V
Dc output voltage	120 V
Diode $D_1$ forward voltage drop	1.5 V
Load power	200 W

- 21.12** Derive an expression for the emulated resistance  $R_e(V_{g,rms}, R_s, k_v, v_{control})$  of the average-current-controlled boost rectifier with ac line voltage feedforward, Fig. 21.18.
- 21.13** Derive the CPM boost rectifier static input characteristics, Eq. (21.60).
- 21.14** The boost rectifier system of Fig. 21.51 employs average current control with ac line voltage feedforward.



**Fig. 21.51** Average current controlled boost rectifier with input voltage feedforward, Problem 21.14

The ac line frequency is 50 Hz. The rectifier drives a constant power load of 500 W. The pulse-width modulator contains a ramp having a peak-to-peak amplitude of 3 V. There is no compensator in the inner wide-bandwidth average current control feedback loop. The average current sensing circuit has gain

$$\frac{v_a(s)}{i_g(s)} = \frac{R_s}{\left(1 + \frac{s}{\omega_0}\right)}$$

Other converter parameter values are

$$f_s = 100\text{kHz} \quad L = 2.5\text{mH}$$

$$f_0 = \frac{\omega_0}{2\pi} = 10\text{kHz} \quad R_s = 1\Omega$$

$$V = 385\text{V} \quad V_{g,rms} = 230\text{V}$$

- (a) Construct the magnitude and phase Bode diagrams of the loop gain  $T_i(s)$  of the average-current-control loop. Label important features.

- (b) Determine numerical values of the crossover frequency and phase margin of  $T_i(s)$ . The outer low-bandwidth feedback loop has loop gain  $T_v(s)$ . The compensator of this loop has constant gain  $G_{cv}(s) = 330$ . The multiplier gain is  $k_v = 2$ . The capacitor value is  $C = 680\mu\text{F}$ . The reference voltage  $v_{ref2}(t)$  is 3.85 V.
- (c) Determine the peak magnitude of the output 100 Hz voltage ripple.
- (d) Determine the quiescent control voltage  $V_{control}$ .
- (e) Construct the magnitude and phase Bode diagrams of the loop gain  $T_v(s)$  of the outer feedback loop. Label important features.
- (d) Determine numerical values of the crossover frequency and phase margin of  $T_v(s)$ .
- 21.15** A critical conduction mode controller causes a boost rectifier to exhibit an ac input current waveform similar to Fig. 21.23b. The ac input voltage is 120 Vrms at 60 Hz. The rectifier supplies 225 Vdc to a 120 W load. The boost converter inductance is  $L = 600\mu\text{H}$ .
- (a) Determine the emulated resistance  $R_e$ .
  - (b) Write the numerical expression for the converter switching frequency  $f_s$ , as a function of  $t_{on}$  and the applied terminal voltages. Sketch  $f_s$  vs. time.
  - (c) What is the maximum switching frequency? What is the minimum switching frequency?
  - (d) Derive an analytical expression for the rms transistor current for this control method, as a function of the magnitude of the sinusoidal line current. Compare the rms transistor current of this approach with a CCM boost rectifier having negligible current switching ripple.
- 21.16** To obtain an isolated dc output, the boost converter in Fig. 21.5 is replaced by the full-bridge transformer-isolated CCM boost converter of Fig. 6.36. The transformer has negligible magnetizing current. The inductor current and capacitor voltage ripples are small, the output capacitance is very large, and the converter is loaded with resistor  $R$ .
- (a) Derive an expression for the RMS transistor current.
  - (b) Derive an expression for the RMS output capacitor current.

## **Part VI**

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### **Resonant Converters**

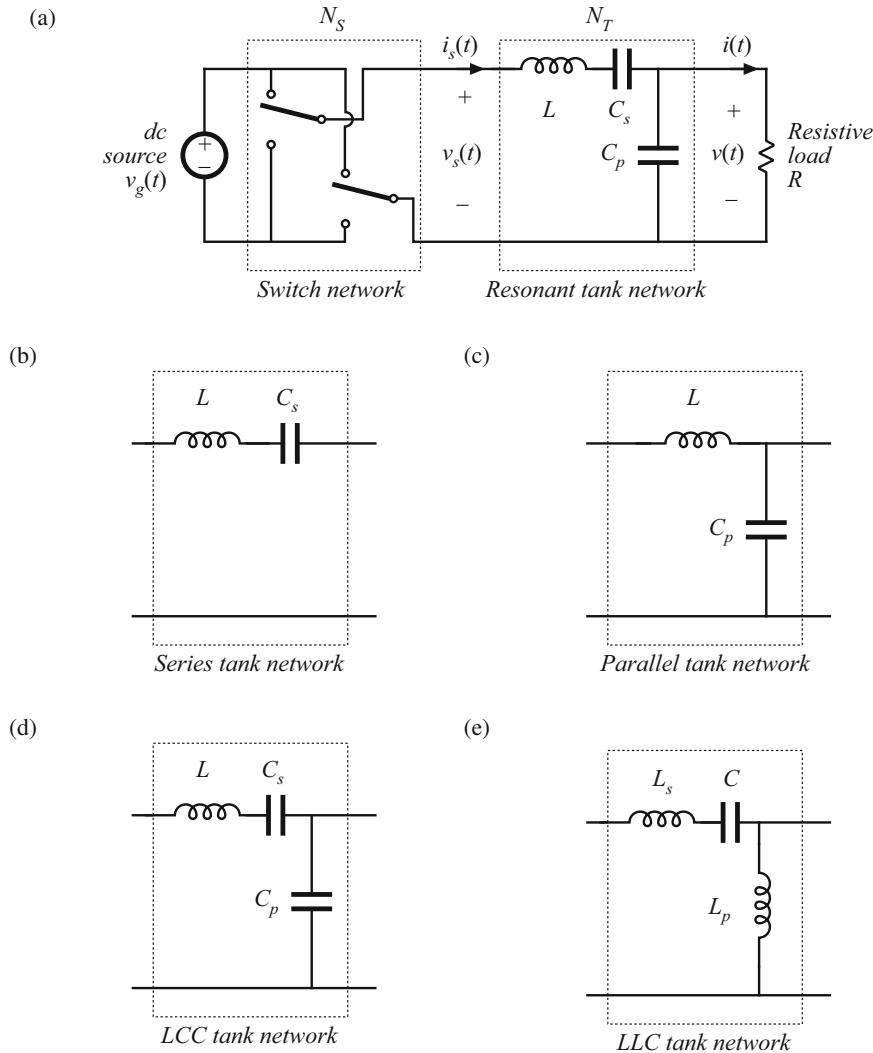


## Resonant Conversion

Part VI of this text deals with a class of converters whose operation differs significantly from the PWM converters covered in Parts I to V. *Resonant power converters* [272, 295–329] contain resonant  $L-C$  networks whose voltage and current waveforms vary sinusoidally during one or more subintervals of each switching period. These sinusoidal variations are large in magnitude, and hence the small-ripple approximation introduced in Chap. 2 does not apply.

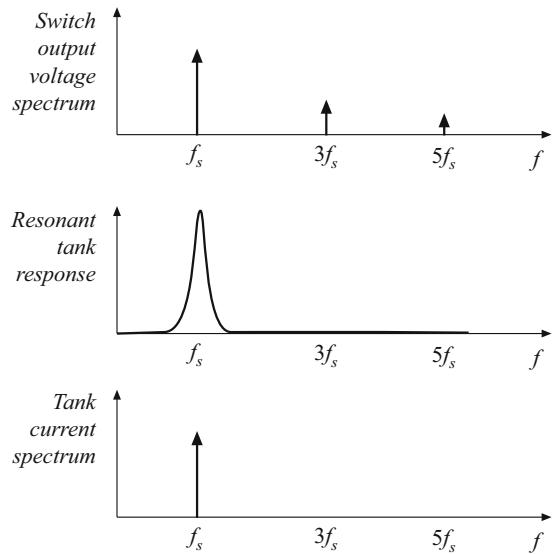
Dc-to-high-frequency-ac inverters are required in a variety of applications, including wireless power transfer, electronic ballasts for gas-discharge lamps [296, 297], induction heating and cooking, electrosurgical generators, and applications employing piezoelectric transformers or actuators. These applications typically require generation of a sinusoid of tens or hundreds of kHz, having moderate or low total harmonic distortion. A simple resonant inverter system is illustrated in Fig. 22.1a. A switch network produces a square wave voltage  $v_s(t)$ . As illustrated in Fig. 22.2, the spectrum of  $v_s(t)$  contains fundamental plus odd harmonics. This voltage is applied to the input terminals of a resonant tank network. The tank network resonant frequency  $f_0$  is tuned to the fundamental component of  $v_s(t)$ , that is, to the switching frequency  $f_s$ , and the tank exhibits negligible response at the harmonics of  $f_s$ . In consequence, the tank current  $i_s(t)$ , as well as the load voltage  $v(t)$  and load current  $i(t)$ , have essentially sinusoidal waveforms of frequency  $f_s$ , with negligible harmonics. By changing the switching frequency  $f_s$  (closer to or further from the resonant frequency  $f_0$ ), the magnitudes of  $i_s(t)$ ,  $v(t)$ , and  $i(t)$  can be controlled. Other schemes for control of the output voltage, such as phase-shift control of the bridge switch network, are also possible. A variety of resonant tank networks can be employed; Fig. 22.1b–e illustrate the well-known *series*, *parallel*, *LCC*, and *LLC* tank networks. Inverters employing the series resonant tank network are known as the *series resonant*, or *series loaded*, inverter. In the *parallel resonant* or *parallel loaded* inverter, the load voltage is equal to the resonant tank capacitor voltage. The *LCC* inverter employs tank capacitors both in series and in parallel with the load, while the *LLC* inverter employs both series and shunt tank inductors.

Figure 22.3 illustrates a high-frequency inverter of an electronic ballast for a gas-discharge lamp. A half-bridge configuration of the LCC inverter drives the lamp with an approximately sinusoidal high-frequency ac waveform. The converter is controlled to provide a relatively high voltage to start the lamp, and a lower voltage thereafter. When the ballast is powered by the ac utility, a low-harmonic rectifier typically provides the input dc voltage for the inverter.

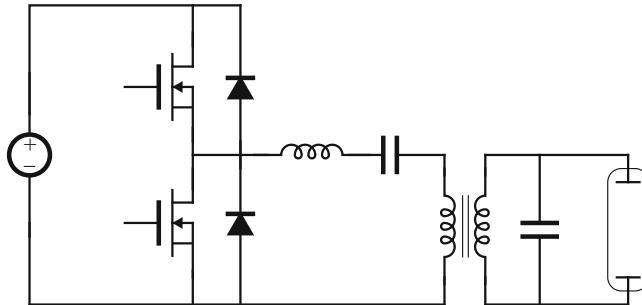


**Fig. 22.1** A basic class of resonant inverters that consist of (a) a switch network  $N_S$  that drives a resonant tank network  $N_T$  near resonance. Several common tank networks: (b) series, (c) parallel, (d) LCC, (e) LLC

A resonant dc–dc converter can be constructed by rectifying and filtering the ac output of a resonant inverter. Figure 22.4 illustrates a series resonant dc–dc converter, in which the approximately sinusoidal resonant tank output current  $i_R(t)$  is rectified by a diode bridge rectifier, and filtered by a large capacitor to supply a dc load having current  $I$  and voltage  $V$ . Again, by variation of the switching frequency  $f_s$  (closer to or further from the resonant frequency  $f_0$ ), the magnitude of the tank current  $i_R(t)$ , and hence also the dc load current  $I$ , can be controlled. Resonant dc–dc converters based on series, parallel, LCC, and other resonant tank networks are well understood. These converters are employed when specialized application requirements



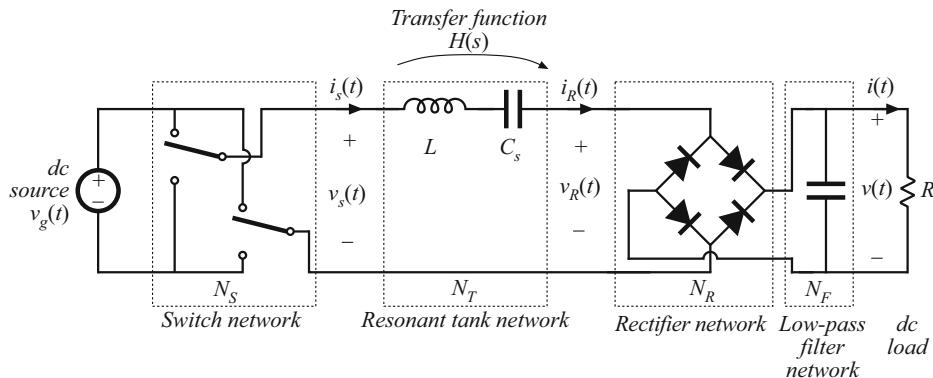
**Fig. 22.2** The tank network responds primarily to the fundamental component of the applied waveforms



**Fig. 22.3** Half-bridge LLC inverter circuit, as an electronic ballast for a gas-discharge lamp

justify their use. For example, they are commonly employed in high-voltage dc power supplies [298, 299], because the substantial leakage inductance and winding capacitance of high-voltage transformers leads unavoidably to a resonant tank network. The same principle can be employed to construct *resonant link* inverters or resonant link cycloconverters [300–302]; controllable switch networks are then employed on both sides of the resonant tank network.

Figure 22.5 illustrates another approach to resonant power conversion, in which resonant elements are inserted into the switch network of an otherwise-PWM converter. A *resonant switch* network, or *quasi-resonant* converter, is then obtained. For example, in Fig. 22.5b, resonant elements  $L_r$  and  $C_r$  are combined with the switch network transistor and diode. The resonant frequency of these elements is somewhat higher than the switching frequency. This causes the switch network waveforms  $i_1(t)$  and  $v_2(t)$  to become quasi-sinusoidal pulses. The resonant switch network of Fig. 22.5b can replace the PWM switch network of Fig. 22.5a in nearly any PWM converter. For example, insertion of the resonant switch network of Fig. 22.5b into the converter circuit of Fig. 22.5c leads to a quasi-resonant buck converter. Numerous resonant



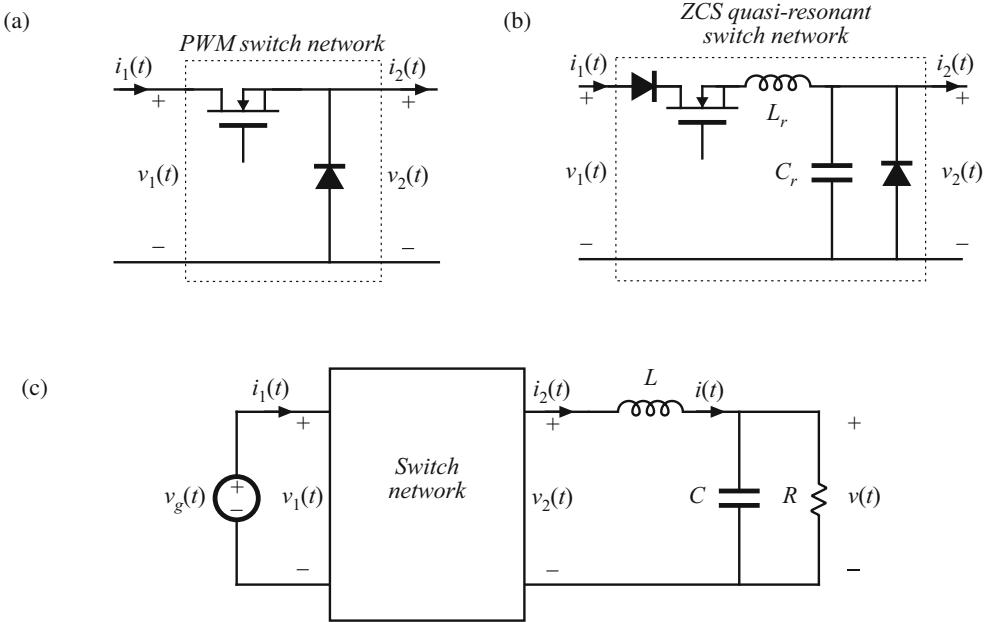
**Fig. 22.4** Derivation of a resonant dc–dc converter, by rectification and filtering of the output of a resonant inverter

switch networks are known, which lead to a large number of resonant switch versions of buck, boost, buck–boost, and other converters. Quasi-resonant converters are described in Chap. 23.

The chief advantage of resonant converters is their reduced switching loss, via mechanisms known as *zero-current switching* (ZCS), and *zero-voltage switching* (ZVS). The turn-on and/or turn-off transitions of the various converter semiconductor elements can occur at zero crossings of the resonant converter quasi-sinusoidal waveforms. This eliminates some of the switching loss mechanisms described in Chap. 4. Hence, switching loss is reduced, and resonant converters can operate at switching frequencies that are higher than in comparable PWM converters. Zero-voltage switching can also eliminate some of the sources of converter-generated electromagnetic interference.

Resonant converters exhibit several disadvantages. Although the resonant element values can be chosen such that good performance with high efficiency is obtained at a single operating point, typically it is difficult to optimize the resonant elements such that good performance is obtained over a wide range of load currents and input voltages. Significant currents may circulate through the tank elements, even when the load is removed, leading to poor efficiency at light load. Also, the quasi-sinusoidal waveforms of resonant converters exhibit greater peak values than those exhibited by the rectangular waveforms of PWM converters, provided that the PWM current spikes due to diode stored charge are ignored. For these reasons, resonant converters exhibit increased conduction losses and tank inductor losses, which can offset their reduced switching losses.

In this chapter, the properties of the series, parallel, and other resonant inverters and dc–dc converters are investigated using the *sinusoidal approximation* [296, 303–305]. Harmonics of the switching frequency are neglected, and the tank waveforms are assumed to be purely sinusoidal. This allows simple equivalent circuits to be derived for the bridge inverter, tank, rectifier, and output filter portions of the converter, whose operation can be understood and solved using standard linear ac analysis. This intuitive approach is quite accurate for operation in the continuous conduction mode with a high-*Q* response, but becomes less accurate when the tank is operated with a low *Q*-factor or for operation of dc–dc resonant converters in or near the discontinuous conduction mode.



**Fig. 22.5** Derivation of a quasi-resonant converter: (a) conventional PWM switch network, (b) a ZCS quasi-resonant switch network, (c) a quasi-resonant buck converter is obtained by employing a quasi-resonant switch network such as (b) in a buck converter

For dc–dc resonant converters, the important result of this approach is that the dc voltage conversion ratio of a continuous conduction mode resonant converter is given approximately by the ac transfer function of the tank circuit, evaluated at the switching frequency. The tank is loaded by an effective output resistance, having a value nearly equal to the output voltage divided by the output current. It is thus quite easy to determine how the tank components and circuit connections affect the converter behavior. The influence of tank component losses, transformer nonidealities, etc., on the output voltage and converter efficiency can also be found. Several resonant network theorems are presented, which allow the load dependence of conduction loss and of the zero-voltage-or zero-current-switching properties to be explained in a simple and intuitive manner.

It is found that the series resonant converter operates with a step-down voltage conversion ratio. With a 1:1 transformer turns ratio, the dc output voltage is ideally equal to the dc input voltage when the transistor switching frequency is equal to the tank resonant frequency. The output voltage is reduced as the switching frequency is increased or decreased away from resonance. On the other hand, the parallel resonant converter is capable of both step-up and step-down of voltage levels, depending on the switching frequency and the effective tank  $Q$ -factor. The exact steady-state solutions of the ideal series and parallel resonant dc–dc converters are stated in Sect. 22.5.

Zero-voltage switching and zero-current switching mechanisms of the series resonant converter are described in Sect. 22.3. In Sect. 22.4, the dependence of resonant inverter properties on load is examined. A simple frequency-domain approach explains why some resonant con-

verters, over certain ranges of operating points, exhibit large circulating tank currents and low efficiency. The boundaries of zero-voltage switching and zero-current switching are also determined.

It is also possible to modify the PWM converters of the previous chapters, so that zero-current or zero-voltage switching is obtained. A number of diverse approaches are known that lead to *soft switching* in buck, boost, forward, flyback, bridge, and other topologies. Chapter 23 summarizes some of the well-known schemes, including resonant switches, quasi-square wave switches, the full-bridge zero-voltage transition converter, and zero-voltage switching in forward and flyback converters containing active-clamp snubbers. A detailed description of soft-switching mechanisms of diodes, MOSFETs, and IGBTs is also given.

## 22.1 Sinusoidal Analysis of Resonant Converters

Consider the class of resonant converters that contain a controlled switch network  $N_s$  that drives a linear resonant tank network  $N_T$ . In a resonant inverter, the tank network drives a resistive load as in Fig. 22.1. The reactive component of the load impedance, if any, can be effectively incorporated into the tank network. In the case of a resonant dc–dc converter, the resonant tank network is connected to an uncontrolled rectifier network  $N_R$ , filter network  $N_F$  and load  $R$ , as illustrated in Fig. 22.4. Many well-known converters can be represented in this form, including the series, parallel, LCC, and LLC topologies.

In the most common modes of operation, the controlled switch network produces a square wave voltage output  $v_s(t)$  whose frequency  $f_s$  is close to the tank network resonant frequency  $f_0$ . In response, the tank network rings with approximately sinusoidal waveforms of frequency  $f_s$ . In the case where the resonant tank responds primarily to the fundamental component  $f_s$  of the switch waveform  $v_s(t)$ , and has negligible response at the harmonic frequencies  $n f_s$ ,  $n = 3, 5, 7, \dots$ , then the tank waveforms are well approximated by their fundamental components. As shown in Fig. 22.2, this is indeed the case when the tank network contains a high- $Q$  resonance at or near the switching frequency, and a low-pass characteristic at higher frequencies. Hence, let us neglect harmonics, and compute the relationships between the fundamental components of the tank terminal waveforms  $v_s(t)$ ,  $i_s(t)$ ,  $i_R(t)$ , and  $v_R(t)$ .

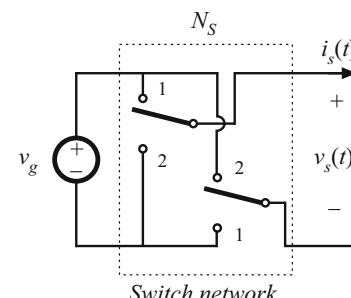
### 22.1.1 Controlled Switch Network Model

If the switch network of Fig. 22.6 is controlled to produce a square wave of frequency  $f_s = \omega_s/2\pi$  as in Fig. 22.7, then its output voltage waveform  $v_s(t)$  can be expressed in the Fourier series

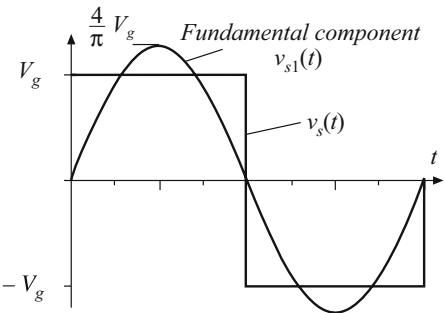
$$v_s(t) = \frac{4V_g}{\pi} \sum_{n=1,3,5,\dots} \frac{1}{n} \sin(n\omega_s t) \quad (22.1)$$

The fundamental component is

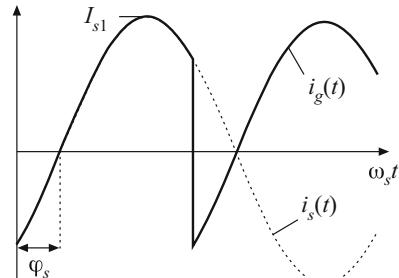
$$v_{s1}(t) = \frac{4V_g}{\pi} \sin(\omega_s t) = V_{s1} \sin(\omega_s t) \quad (22.2)$$



**Fig. 22.6** An ideal switch network



**Fig. 22.7** Switch network voltage  $v_s(t)$  and its fundamental component  $v_{s1}(t)$



**Fig. 22.8** Switch network waveforms  $i_s(t)$  and  $i_g(t)$

which has a peak amplitude of  $(4/\pi)$  times the dc input voltage  $V_g$ , and is in phase with the original square wave  $v_s(t)$ . Hence, the switch network output terminal is modeled as a sinusoidal voltage generator,  $v_{s1}(t)$ .

It is also of interest to model the converter dc input port. This requires computation of the dc component  $I_g$  of the switch input current  $i_g(t)$ . The switch input current  $i_g(t)$  is equal to the output current  $i_s(t)$  when the switches are in position 1, and its inverse  $-i_s(t)$  when the switches are in position 2. Under the conditions described above, the tank rings sinusoidally and  $i_s(t)$  is well approximated by a sinusoid of some peak amplitude  $I_{s1}$  and phase  $\varphi_s$ :

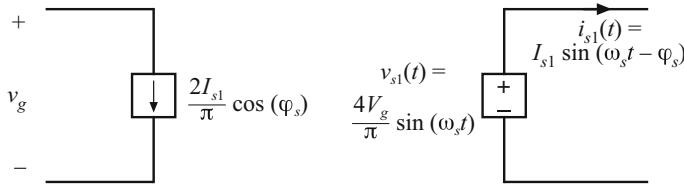
$$i_s(t) \approx I_{s1} \sin(\omega_s t - \varphi_s) \quad (22.3)$$

The input current waveform is shown in Fig. 22.8.

The dc component, or average value, of the input current can be found by averaging  $i_g(t)$  over one half-switching period:

$$\begin{aligned} \langle i_g(t) \rangle_{T_s} &= \frac{2}{T_s} \int_0^{T_s/2} i_g(\tau) d\tau \\ &\approx \frac{2}{T_s} \int_0^{T_s/2} I_{s1} \sin(\omega_s \tau - \varphi_s) d\tau \\ &= \frac{2}{\pi} I_{s1} \cos(\varphi_s) \end{aligned} \quad (22.4)$$

Thus, the dc component of the converter input current depends directly on the peak amplitude of the tank input current  $I_{s1}$  and on the cosine of its phase shift  $\varphi_s$ .



**Fig. 22.9** An equivalent circuit for the switch network, which models the fundamental component of the output voltage waveform and the dc component of the input current waveform

An equivalent circuit for the switch is given in Fig. 22.9. This circuit models the basic energy conversion properties of the switch: the dc power supplied by the voltage source  $V_g$  is converted into ac power at the switch output. Note that the dc power at the source is the product of  $V_g$  and the dc component of  $i_s(t)$ , and the ac power at the switch is the average of  $v_s(t)i_s(t)$ . Furthermore, if the harmonics of  $v_s(t)$  are negligible, then the switch output voltage can be represented by its fundamental component, a sinusoid  $v_{s1}(t)$  of peak amplitude  $4V_g/\pi$ . It can be verified that the switch network dc input power and fundamental average output power, predicted by Fig. 22.9, are equal.

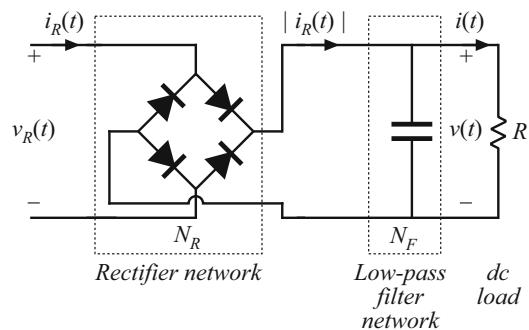
### 22.1.2 Modeling the Rectifier and Capacitive Filter Networks

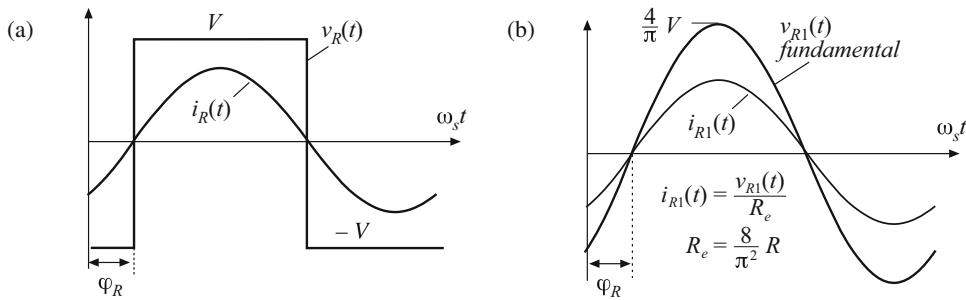
In the series resonant dc–dc converter, the output rectifier is driven by the nearly sinusoidal tank output current  $i_R(t)$ . A large capacitor  $C_F$  is placed at the dc output, so that the output voltage  $v(t)$  contains negligible harmonics of the switching frequency  $f_s$ , as shown in Fig. 22.10. Hence, we can make the small-ripple approximation as usual:  $v(t) \approx V$ ,  $i(t) \approx I$ . The diode rectifiers switch when  $i_R(t)$  passes through zero, as shown in Fig. 22.11. The rectifier input voltage  $v_R(t)$  is essentially a square wave, equal to  $+v(t)$  when  $i_R(t)$  is positive and  $-v(t)$  when  $i_R(t)$  is negative. Note that  $v_R(t)$  is in phase with  $i_R(t)$ .

If the tank output current  $i_R(t)$  is a sinusoid with peak amplitude  $I_{R1}$  and phase shift  $\varphi_R$ :

$$i_R(t) = I_{R1} \sin(\omega_s t - \varphi_R) \quad (22.5)$$

**Fig. 22.10** Uncontrolled rectifier with capacitive filter network, as in the series resonant converter





**Fig. 22.11** Rectifier network input terminal waveforms: (a) actual waveforms  $v_R(t)$  and  $i_R(t)$ , (b) fundamental components  $v_{R1}(t)$  and  $i_{R1}(t)$

then the rectifier input voltage may be expressed in the Fourier series

$$v_R(t) = \frac{4V}{\pi} \sum_{n=1,3,5,\dots}^{\infty} \frac{1}{n} \sin(n\omega_s t - \varphi_R) \quad (22.6)$$

where  $\varphi_R$  is the phase shift of  $i_R(t)$ , with respect to  $v_s(t)$ . This voltage waveform is impressed on the output port of the resonant tank network. Again, if the tank network responds primarily to the fundamental component ( $f_s$ ) of  $v_R(t)$ , and has negligible response at the harmonic frequencies  $nf_s$ ,  $n = 3, 5, 7 \dots$ , then the harmonics of  $v_R(t)$  can be ignored. The voltage waveform  $v_R(t)$  is then well approximated by its fundamental component  $v_{R1}(t)$ :

$$v_{R1}(t) = \frac{4V}{\pi} \sin(\omega_s t - \varphi_R) = V_{R1} \sin(\omega_s t - \varphi_R) \quad (22.7)$$

The fundamental voltage component  $v_{R1}(t)$  has a peak value of  $(4/\pi)$  times the dc output voltage  $V$ , and is in phase with the current  $i_R(t)$ .

$$R_e = \frac{8}{\pi^2} R$$

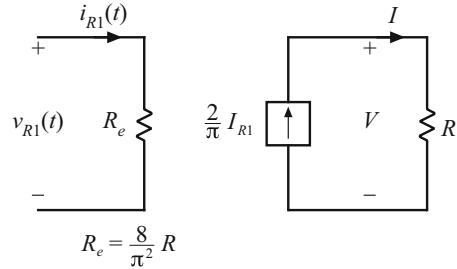
The rectified tank output current,  $|i_R(t)|$ , is filtered by capacitor  $C_F$ . Since no dc current can pass through  $C_F$ , the dc component of  $|i_R(t)|$  must be equal to the steady-state load current  $I$ . By equating dc components we obtain

$$\begin{aligned} I &= \frac{2}{T_s} \int_0^{T_s/2} |I_{R1}| \sin(\omega_s t - \varphi_R) dt \\ &= \frac{2}{\pi} I_{R1} \end{aligned} \quad (22.8)$$

Therefore, the load current and the tank output current amplitudes are directly related in steady state.

Since  $v_{R1}(t)$ , the fundamental component of  $v_R(t)$  is in phase with  $i_R(t)$ , the rectifier presents an effective resistive load  $R_e$  to the tank circuit. The value of  $R_e$  is equal to the ratio of  $v_{R1}(t)$  to  $i_R(t)$ . Division of Eq. (22.7) by Eq. (22.5), and elimination of  $I_{R1}$  using Eq. (22.8) yields

**Fig. 22.12** An equivalent circuit for the rectifier and filter network, which models the fundamental components of the rectifier ac input waveforms and the dc components of the load waveforms. The rectifier presents an effective resistive load  $R_e$  to the tank network



$$R_e = \frac{v_{R1}(t)}{i_R(t)} = \frac{8}{\pi^2} \frac{V}{I} \quad (22.9)$$

With a resistive load  $R$  equal to  $V/I$ , this equation reduces to

$$R_e = \frac{8}{\pi^2} R = 0.8106 R \quad (22.10)$$

Thus, the tank network is damped by an effective load resistance  $R_e$  equal to 81% of the actual load resistance  $R$ . An equivalent circuit that models the rectifier network input port fundamental components and output port dc components is given in Fig. 22.12.

### 22.1.3 Resonant Tank Network

We have postulated that the effects of harmonics can be neglected, and we have consequently shown that the bridge can be modeled as a fundamental voltage source  $v_{s1}(t)$ . In the case of a dc–dc converter, the rectifier can be modeled using an effective resistor of value  $R_e$ . We can now solve the resonant tank network by standard linear analysis.

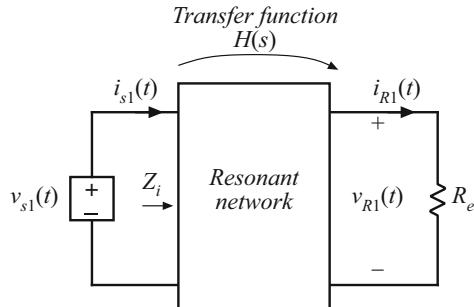
As shown in Fig. 22.13, the tank circuit is a linear network with the following voltage transfer function:

$$\frac{v_{R1}(s)}{v_{s1}(s)} = H(s) \quad (22.11)$$

Hence, the ratio  $V_{R1}/V_{s1}$  of the peak magnitudes of  $v_{R1}(t)$  and  $v_{s1}(t)$  is given by

$$\frac{V_{R1}}{V_{s1}} = \|H(s)\|_{s=j\omega_s} \quad (22.12)$$

**Fig. 22.13** The linear tank network, excited by an effective sinusoidal input source and driving an effective resistive load



In addition,  $i_R(s)$  is given by

$$i_R(s) = \frac{v_{R1}(s)}{R_e} = \frac{H(s)}{R_e} v_{s1}(s) \quad (22.13)$$

So the peak magnitude of  $i_R(t)$  is

$$I_{R1} = \frac{\|H(s)\|_{s=j\omega_s}}{R_e} V_{s1} \quad (22.14)$$

Thus, the magnitude of the tank transfer function is found, with an effective resistive load.

#### 22.1.4 Solution of Converter Voltage Conversion Ratio $M = V/V_g$

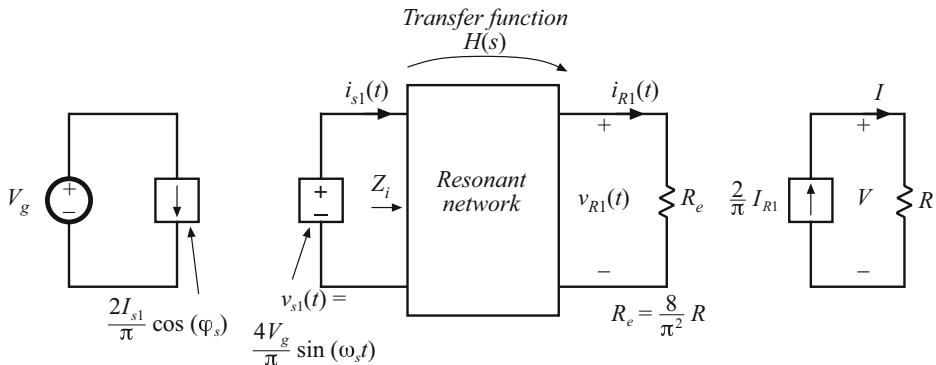
An equivalent circuit of a complete dc–dc resonant converter is depicted in Fig. 22.14. The voltage conversion ratio of the resonant converter can now be found:

$$M = \frac{V}{V_g} = \underbrace{\left(\frac{V}{I}\right)}_{(R)} \underbrace{\left(\frac{2}{\pi}\right)}_{\left(\frac{1}{R_e}\right)} \underbrace{\left(\|H(s)\|_{s=j\omega_s}\right)}_{\left(\frac{4}{\pi}\right)} \underbrace{\left(\frac{V_{R1}}{V_{s1}}\right)}_{\left(\frac{I_{R1}}{I_{R1}}\right)} \quad (22.15)$$

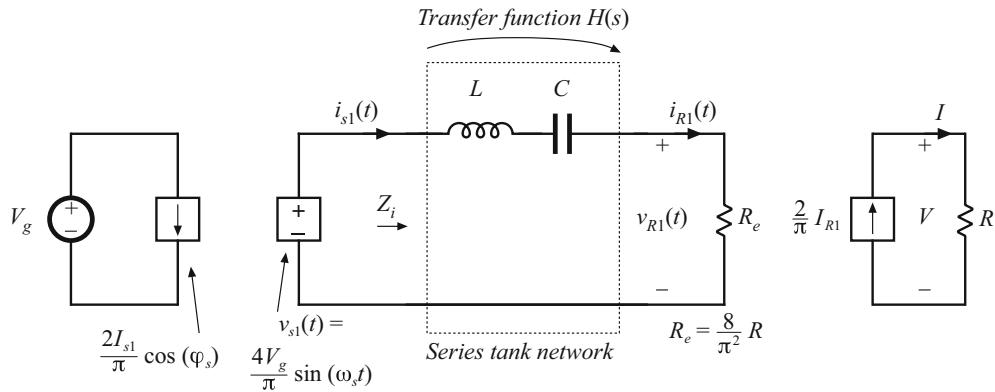
Simplification by use of Eq. (22.10) yields

$$\frac{V}{V_g} = \|H(s)\|_{s=j\omega_s} \quad (22.16)$$

Equation (22.16) is the desired result. It states that the dc conversion ratio of the resonant converter is approximately the same as the ac transfer function of the resonant tank circuit, evaluated at the switching frequency  $f_s$ . This intuitive result can be applied to converters with many different types of tank circuits. However, it should be reemphasized that Eq. (22.16) is valid only if the response of the tank circuit to the harmonics of  $v_s(t)$  is negligible compared to the



**Fig. 22.14** Steady-state equivalent circuit that models the dc and fundamental components of resonant converter waveforms



**Fig. 22.15** Steady-state equivalent circuit of the series resonant converter

fundamental response, an assumption that is not always justified. In addition, we have assumed that the switch network is controlled to produce a square wave and that the rectifier network drives a capacitive-type filter network. Finally, the transfer function  $H(s)$  is evaluated using the effective load resistance  $R_e$  given by Eq. (22.9).

## 22.2 Examples

### 22.2.1 Series Resonant DC–DC Converter Example

The series resonant converter with switching-frequency control is shown in Fig. 22.4. Current-bidirectional two-quadrant switches are necessary. For this circuit, the tank network consists of a series  $L$ – $C$  circuit, and Fig. 22.14 can be redrawn as in Fig. 22.15. The transfer function  $H(s)$  is therefore:

$$\begin{aligned}
 H(s) &= \frac{R_e}{Z_i(s)} = \frac{R_e}{R_e + sL + \frac{1}{sC}} \\
 &= \frac{\left(\frac{s}{Q_e \omega_0}\right)}{1 + \left(\frac{s}{Q_e \omega_0}\right) + \left(\frac{s}{\omega_0}\right)^2} \tag{22.17}
 \end{aligned}$$

where

$$\omega_0 = \frac{1}{\sqrt{LC}} = 2\pi f_0$$

$$R_0 = \sqrt{\frac{L}{C}}$$

$$Q_e = \frac{R_0}{R_e}$$

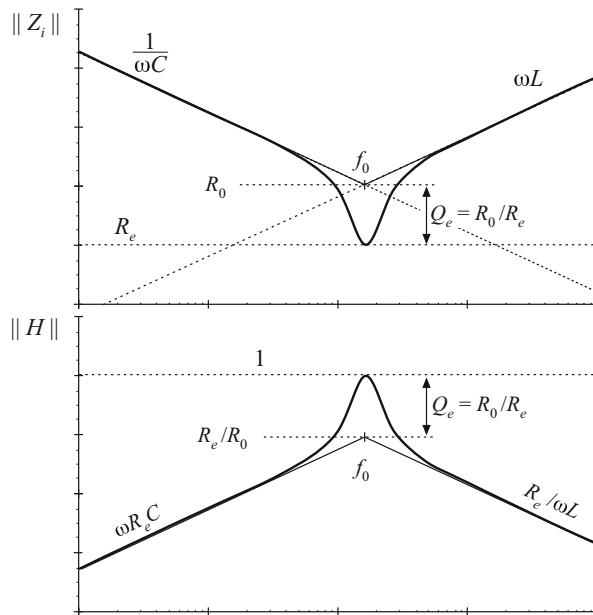
The magnitude of  $H(j\omega_s)$ , which coincides with the converter dc conversion ratio  $M = V/V_g$ , is

$$M = \|H(j\omega_s)\| = \frac{1}{\sqrt{1 + Q_e^2 \left(\frac{1}{F} - F\right)^2}} \quad (22.18)$$

where

$$F = f_s/f_0 \quad (22.19)$$

The Bode diagrams of  $Z_i(s)$  and  $H(s)$  are constructed in Fig. 22.16, using the graphical construction method of Chap. 8. The series resonant impedance  $Z_i(s)$  is dominated by the capacitor  $C$  at low frequency, and by the inductor  $L$  at high frequency. At the resonant frequency  $f_0$ , the impedances of the inductor and capacitor are equal in magnitude and opposite in phase; hence, they cancel. The series resonant impedance  $Z_i(s)$  is equal to  $R_e$  at  $f = f_0$ .

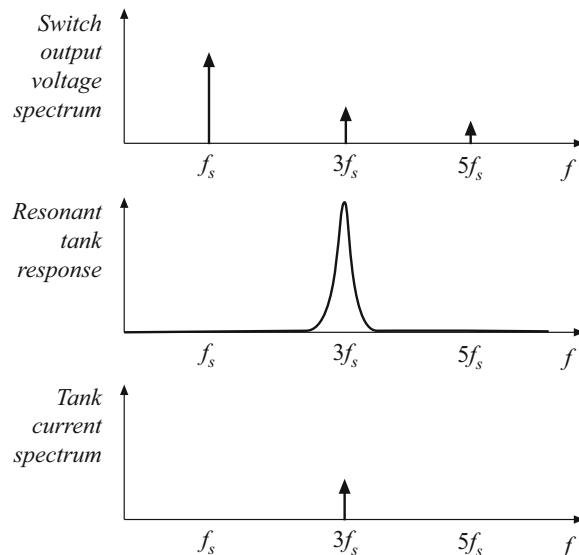


**Fig. 22.16** Construction of the Bode diagrams of  $Z_i(s)$  and  $H(s)$  for the series resonant converter

The transfer function  $\|H(j\omega)\|$  is constructed graphically, by division of  $R_e$  by the  $\|Z_i\|$  asymptotes of Fig. 22.16. At resonance, one obtains  $\|H\| = R_e/R_e = 1$ . At frequencies above or below the resonant frequency,  $\|Z_i\| > R_e$  and hence  $\|H\| < 1$ . So the conversion ratio  $M$  is less than or equal to 1. It can also be seen that a decrease in the load resistance  $R$ , which increases the effective quality factor  $Q_e$ , causes a more peaked response in the vicinity of resonance. Exact characteristics of the series resonant converter are plotted in Fig. 22.49.

Over what range of switching frequencies is Eq. (22.18) accurate? The response of the tank to the fundamental component of  $v_s(t)$  must be sufficiently greater than the response to the harmonics of  $v_s(t)$ . This is certainly true for operation above resonance because  $H(s)$  contains a bandpass characteristic that decreases with a single-pole slope for  $f_s > f_0$ . For the same reason, Eq. (22.18) is valid when the switching frequency is below but near resonance.

However, for switching frequencies  $f_s$  much less than the resonant frequency  $f_0$ , the sinusoidal approximation breaks down completely because the tank responds more strongly to the harmonics of  $v_s(t)$  than to its fundamental. For example, at  $f_s = f_0/3$ , the third harmonic of  $v_s(t)$  is equal to  $f_0$  and directly excites the tank resonance. Some other type of analysis must be used to understand what happens at these lower frequencies. Also, in the low- $Q$  case, the approximation is less accurate because the filter response is less peaked, and hence does not favor the fundamental component as strongly. As shown in a later section, discontinuous conduction modes may then occur whose waveforms are highly nonsinusoidal.



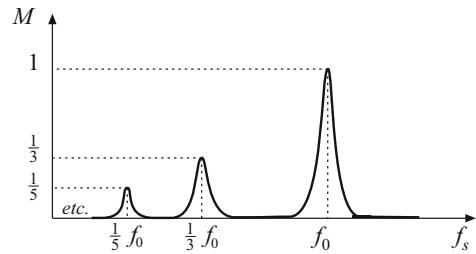
**Fig. 22.17** Excitation of the tank network by the third harmonic of the switching frequency

### 22.2.2 Subharmonic Modes of the Series Resonant Converter

If the  $n^{\text{th}}$  harmonic of the switch output waveform  $v_s(t)$  is close to the resonant tank frequency,  $nf_s \sim f_0$ , and if the tank effective quality factor  $Q_e$  is sufficiently large, then as illustrated in Fig. 22.17, the tank responds primarily to harmonic  $n$ . All other components of the tank waveforms can then be neglected, and it is a good approximation to replace  $v_s(t)$  with its  $n^{\text{th}}$  harmonic component:

$$v_s(t) \approx v_{sn}(t) = \frac{4V_g}{n\pi} \sin(n\omega_s t) \quad (22.20)$$

This expression differs from Eq. (22.2) because the amplitude is reduced by a factor of  $1/n$ , and the frequency is  $nf_s$  rather than  $f_s$ .



**Fig. 22.18** The subharmonic modes of the series resonant converter. These modes occur when the harmonics of the switching frequency excite the tank resonance

The arguments used to model the tank and rectifier/filter networks are unchanged from Sect. 22.1. The rectifier presents an effective resistive load to the tank, of value  $R_e = 8R/\pi^2$ . In consequence, the converter dc conversion ratio is given by

$$M = \frac{V}{V_g} = \frac{\|H(jn\omega_s)\|}{n} \quad (22.21)$$

This is a good approximation provided that  $nf_s$  is close to  $f_0$ , and that  $Q_e$  is sufficiently large. Typical characteristics are sketched in Fig. 22.18.

The series resonant converter is not generally designed to operate in a subharmonic mode, since the fundamental modes yield greater output voltage and power, and hence higher efficiency. Nonetheless, the system designer should be aware of their existence, because inadvertent operation in these modes can lead to large signal instabilities.

### 22.2.3 Parallel Resonant DC–DC Converter Example

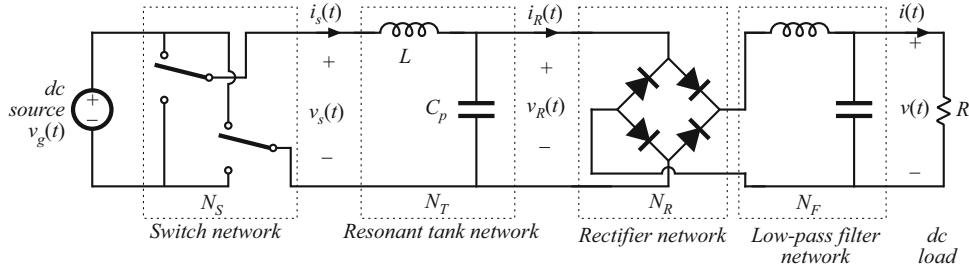
The parallel resonant dc–dc converter is diagrammed in Fig. 22.19. It differs from the series resonant converter in two ways. First, the tank capacitor appears in parallel with the rectifier network rather than in series: this causes the tank transfer function  $H(s)$  to have a different form. Second, the rectifier drives an inductive-input low-pass filter. In consequence, the value of the effective resistance  $R_e$  differs from that of the rectifier with a capacitive filter. Nonetheless, sinusoidal approximations can be used to understand the operation of the parallel resonant converter.

As in the series resonant converter, the switch network is controlled to produce a square wave  $v_s(t)$ . If the tank network responds primarily to the fundamental component of  $v_s(t)$ , then arguments identical to those of Sect. 22.1 can be used to model the output fundamental components and input dc components of the switch waveforms. The resulting equivalent circuit is identical to Fig. 22.9.

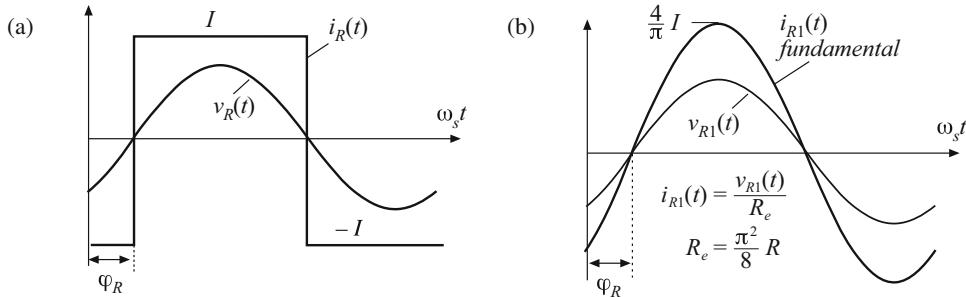
The uncontrolled rectifier with inductive filter network can be described using the dual of the arguments of Sect. 22.1.2. In the parallel resonant converter, the output rectifiers are driven by the nearly sinusoidal tank capacitor voltage  $v_R(t)$ , and the diode rectifiers switch when  $v_R(t)$  passes through zero as in Fig. 22.20. If the filter inductor current ripple is small, then in steady state the filter inductor current is essentially equal to the dc load current  $I$ . The rectifier input current  $i_R(t)$  is therefore a square wave of amplitude  $I$ , and is in phase with the tank capacitor voltage  $v_R(t)$ :

$$i_R(t) = \frac{4I}{\pi} \sum_{n=1,3,5,\dots}^{\infty} \frac{1}{n} \sin(n\omega_s t - \varphi_R) \quad (22.22)$$

where  $\varphi_R$  is the phase shift of  $v_R(t)$ .



**Fig. 22.19** Block diagram of the parallel resonant converter



**Fig. 22.20** Rectifier network input terminal waveforms, for the parallel resonant converter: (a) actual waveforms  $v_R(t)$  and  $i_R(t)$ , (b) fundamental components  $v_{R1}(t)$  and  $i_{R1}(t)$

The fundamental component of  $i_R(t)$  is

$$i_{R1}(t) = \frac{4I}{\pi} \sin(\omega_s t - \varphi_R) \quad (22.23)$$

Hence, the rectifier again presents an effective resistive load to the tank circuit, equal to

$$R_e = \frac{v_{R1}(t)}{i_{R1}(t)} = \frac{\pi V_{R1}}{4I} \quad (22.24)$$

The ac components of the rectified tank capacitor voltage  $|v_R(t)|$  are removed by the output low-pass filter. In steady state, the output voltage  $V$  is equal to and inductive filter network of the parallel resonant the dc component of  $|v_R(t)|$ :

$$V = \frac{2}{T_s} \int_0^{T_s/2} V_{R1} |\sin(\omega_s t - \varphi_R)| dt = \frac{2}{\pi} V_{R1} \quad (22.25)$$

So the load voltage  $V$  and the tank capacitor voltage amplitude are directly related in steady state. Substitution of Eq. (22.25) and resistive load characteristics  $V = IR$  into Eq. (22.24) yields

$$R_e = \frac{\pi^2}{8} R = 1.2337R \quad (22.26)$$

An equivalent circuit for the uncontrolled rectifier with inductive filter network is given in Fig. 22.21. This model is similar to the one used for the series resonant converter, Fig. 22.12, except that the roles of the rectifier input voltage  $v_R(t)$  and current  $i_R(t)$  are interchanged, and the effective resistance  $R_e$  has a different value. The model for the complete converter is given in Fig. 22.22.

Solution of Fig. 22.22 yields the converter dc conversion ratio:

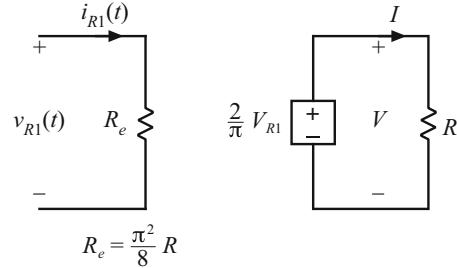
$$M = \frac{V}{V_g} = \frac{8}{\pi^2} \|H(s)\|_{s=j\omega_s} \quad (22.27)$$

where  $H(s)$  is the tank transfer function

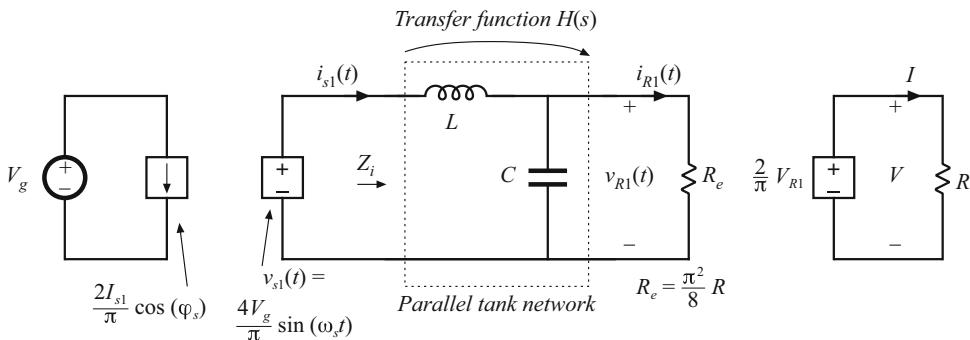
$$H(s) = \frac{Z_o(s)}{sL} \quad (22.28)$$

and

$$Z_o(s) = sL \left| \frac{1}{sC} \right| R_e \quad (22.29)$$



**Fig. 22.21** An equivalent circuit for the rectifier and inductive filter network of the parallel resonant converter, which models the fundamental components of the rectifier ac input waveforms and the dc components of the load waveforms



**Fig. 22.22** Equivalent circuit for the parallel resonant converter, which models the fundamental components of the tank waveforms and the dc components of the converter input current and output voltage

The Bode magnitude diagrams of  $H(s)$  and  $Z_o(s)$  are constructed in Fig. 22.23, using the graphical construction method of Chap. 8. The impedance  $Z_o(s)$  is the parallel combination of the impedances of the tank inductor  $L$ , capacitor  $C$ , and effective load  $R_e$ . The magnitude asymptote of the parallel combination of these components, at a given frequency, is equal to the smallest of the individual asymptotes  $\omega L$ ,  $1/\omega C$ , and  $R_e$ . Hence, at low frequency where the inductor impedance dominates the parallel combination,  $\|Z_o(s)\| \cong \omega L$ , while at high frequency the capacitor dominates and  $\|Z_o(s)\| \cong 1/\omega C$ . At resonance, the impedances of the inductor and capacitor are equal in magnitude but opposite in phase, so that their effects cancel. The impedance  $\|Z_o(s)\|$  is then equal to  $R_e$ :

$$\|Z_o(s)\|_{s=j\omega_s} = \frac{1}{\frac{1}{j\omega_0 L} + j\omega_0 C + \frac{1}{R_e}} = R_e \quad (22.30)$$

with

$$\omega_0 L = \frac{1}{\omega_0 C} = R_0$$

The dc conversion ratio is therefore

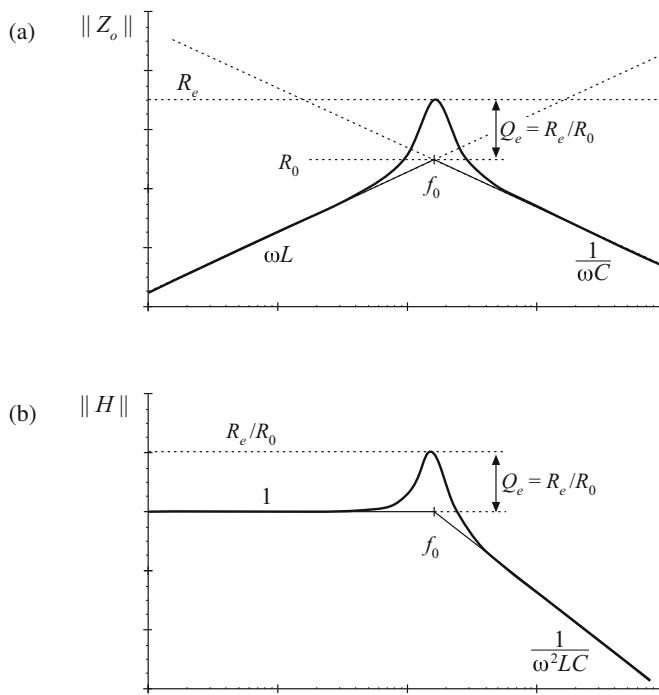
$$\begin{aligned} M &= \frac{8}{\pi^2} \left\| \frac{Z_o(s)}{sL} \right\|_{s=j\omega_s} = \frac{8}{\pi^2} \left\| \frac{1}{1 + \frac{s}{Q_e \omega_0} + \left(\frac{s}{\omega_0}\right)^2} \right\|_{s=j\omega_s} \\ &= \frac{8}{\pi^2} \frac{1}{\sqrt{(1 - F^2)^2 + \left(\frac{F}{Q_e}\right)^2}} \end{aligned} \quad (22.31)$$

where  $F = f_s/f_0$ .

At resonance, the conversion ratio is

$$M = \frac{8}{\pi^2} \frac{R_e}{R_0} = \frac{R}{R_0} \quad (22.32)$$

The actual peak value of  $M$  occurs at a switching frequency slightly below the resonant frequency, with peak  $M$  slightly greater than Eq. (22.32). Provided that the load resistance  $R$  is greater than the tank characteristic impedance  $R_e$ , the parallel resonant converter can produce conversion ratios both greater than and less than one. In fact, the ideal parallel resonant converter can produce conversion ratios approaching infinity, provided that the output current is limited to values less than  $V_g/R_0$ . Of course, losses limit the maximum output voltage that can be produced by practical converters.



**Fig. 22.23** Construction of Bode diagrams of  $Z_i(s)$  and  $H(s)$  for the parallel resonant converter

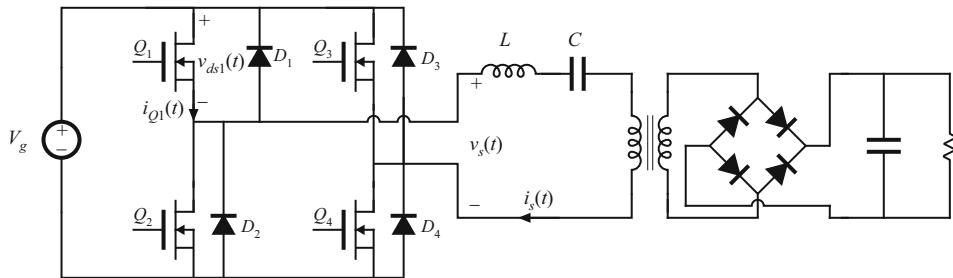
## 22.3 Soft Switching

As mentioned previously, the soft-switching phenomena known as zero-current switching (ZCS) and zero-voltage switching (ZVS) can lead to reduced switching loss. When the turn-on and/or turn-off transitions of a semiconductor switching device coincide with the zero crossings of the applied waveforms, some of the switching loss mechanisms discussed in Sect. 4.6 are eliminated. In converters containing MOSFETs and diodes, zero-voltage switching mitigates the switching loss otherwise caused by diode recovered charge and semiconductor output capacitance.

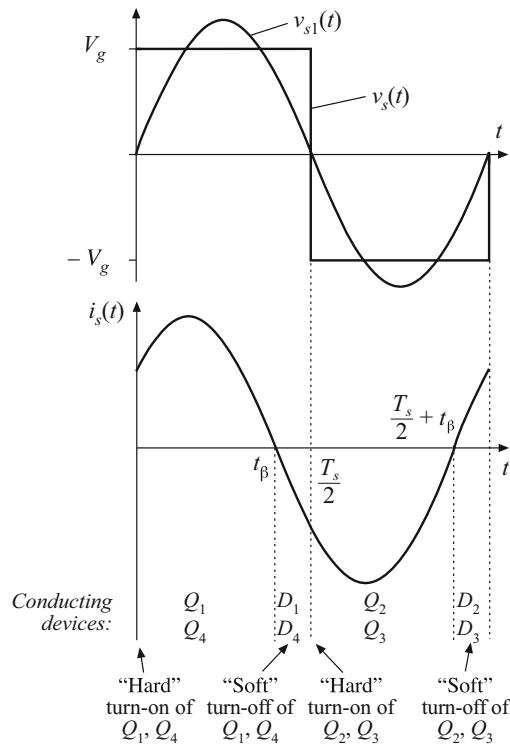
Zero-current switching can mitigate the switching loss caused by current tailing in IGBTs and by stray inductances. Zero-current switching can also be used for commutation of SCRs. In the majority of applications, where diode recovered charge and semiconductor output capacitances are the dominant sources of PWM switching loss, zero-voltage switching is preferred.

### 22.3.1 Operation of the Full Bridge Below Resonance: Zero-Current Switching

When the series and parallel resonant inverters and dc–dc converters are operated below resonance, the zero-current switching phenomenon can occur, in which the circuit causes the transistor current to go to zero before the transistor is turned off. Let us consider the operation of the full-bridge switch network of the series resonant converter in detail.

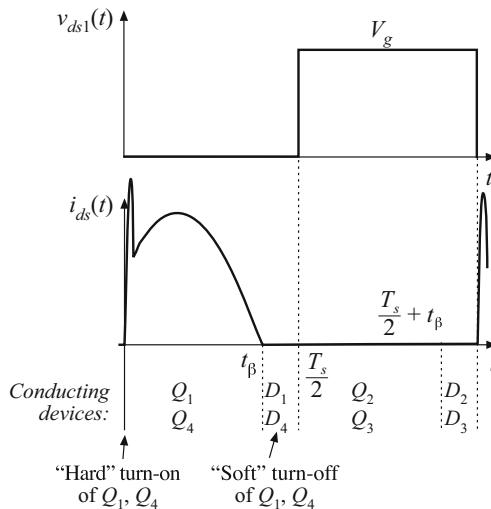


**Fig. 22.24** A series resonant converter incorporating a full-bridge switch network



**Fig. 22.25** Switch network output waveforms for the series resonant converter, operated below resonance in the  $k = 1$  CCM. Zero-current switching aids the transistor turn-off process

A full-bridge circuit, realized using power MOSFETs and antiparallel diodes, is shown in Fig. 22.24. The switch output voltage  $v_{s1}(t)$ , and its fundamental component  $v_s(t)$ , as well as the approximately sinusoidal tank current waveform  $i_s(t)$ , are illustrated in Fig. 22.25. At frequencies less than the tank resonant frequency, the input impedance of the series resonant tank network  $Z_i(s)$  is dominated by the tank capacitor impedance (see Fig. 22.16a). Hence, the tank presents an effective capacitive load to the bridge, and switch current  $i_s(t)$  leads the switch volt-



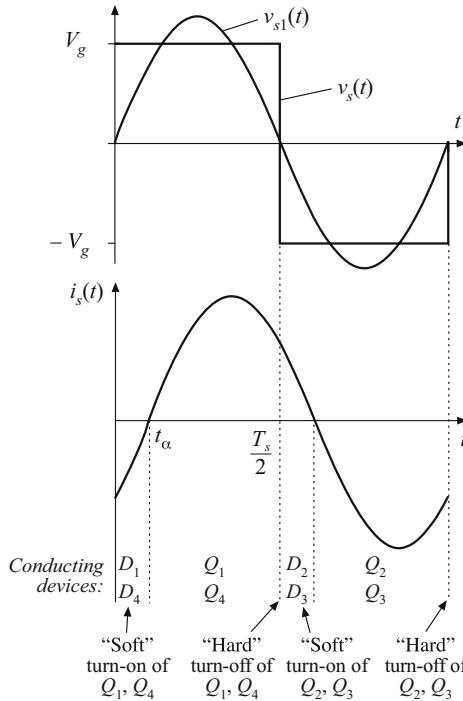
**Fig. 22.26** Transistor  $Q_1$  voltage and current waveforms, for operation of the series resonant converter below resonance in the  $k = 1$  CCM

age fundamental component  $v_{s1}(t)$ , as shown in Fig. 22.25. In consequence, the zero crossing of the current waveform  $i_s(t)$  occurs before the zero crossing of the voltage  $v_s(t)$ .

For the half-cycle  $0 < t < T_s/2$ , the switch voltage  $v_s$  is equal to  $+V_g$ . For  $0 < t < t_\beta$ , the current  $i_s(t)$  is positive and transistors  $Q_1$  and  $Q_4$  conduct. Diodes  $D_1$  and  $D_4$  conduct when  $i_s(t)$  is negative, over the interval  $t_\beta < t < T_s/2$ . The situation during  $T_s/2 < t < T_s$  is symmetrical. Since  $i_{s1}(t)$  leads  $v_{s1}(t)$ , the transistors conduct before their respective antiparallel diodes. Note that, at any given time during the  $D_1$  conduction interval  $t_\beta < t < T_s/2$ , transistor  $Q_1$  can be turned off without incurring switching loss. The circuit naturally causes the transistor turn-off transition to be lossless, and long turn-off switching times can be tolerated.

In general, zero-current switching can occur when the resonant tank presents an effective capacitive load to the switches, so that the switch current zero crossings occur before the switch voltage zero crossings. In the bridge configuration, zero-current switching is characterized by the half-bridge conduction sequence  $Q_1-D_1-Q_2-D_2$ , such that the transistors are turned off while their respective antiparallel diodes conduct. It is possible, if desired, to replace the transistors with naturally commutated thyristors whenever the zero-current-switching property occurs at the turn-off transition.

The transistor turn-on transition in Fig. 22.26 is similar to that of a PWM switch: it is hard-switched and is not lossless. During the turn-on transition of  $Q_1$ , diode  $D_2$  must turn off. Neither the transistor current nor the transistor voltage is zero,  $Q_1$  passes through a period of high instantaneous power dissipation, and switching loss occurs. As in the PWM case, the reverse recovery current of diode  $D_2$  flows through  $Q_1$ . This current spike can be the largest component of switching loss. In addition, the energy stored in the drain-to-source capacitances of  $Q_1$  and  $Q_2$  and in the depletion layer capacitance of  $D_1$  is lost when  $Q_1$  turns on. These turn-on transition switching loss mechanisms can be a major disadvantage of zero-current-switching schemes.



**Fig. 22.27** Switch network output waveforms for the series resonant converter, operated above resonance in the continuous conduction mode. Zero-voltage switching aids the transistor turn-on process

Since zero-current switching does not address the switching loss mechanisms that dominate in MOSFET converters, improvements in efficiency typically are not observed.

### 22.3.2 Operation of the Full-Bridge Above Resonance: Zero-Voltage Switching

When the series resonant converter is operated above resonance, the zero-voltage switching phenomenon can occur, in which the circuit causes the transistor voltage to become zero before the controller turns the transistor on. With a minor circuit modification, the transistor turn-off transitions can also be caused to occur at zero voltage. This process can lead to significant reductions in the switching losses of converters based on MOSFETs and diodes.

For the full-bridge circuit of Fig. 22.24, the switch output voltage  $v_s(t)$ , and its fundamental component  $v_{s1}(t)$ , as well as the approximately sinusoidal tank current waveform  $i_s(t)$ , are plotted in Fig. 22.27. At frequencies greater than the tank resonant frequency, the input impedance of the tank network  $Z_i(s)$  is dominated by the tank inductor impedance. Hence, the tank presents an effective inductive load to the bridge, and the switch current  $i_s(t)$  lags the switch voltage fundamental component  $v_{s1}(t)$ , as shown in Fig. 22.27. In consequence, the zero crossing of the voltage waveform  $v_s(t)$  occurs before the current waveform  $i_s(t)$ .

For the half-cycle  $0 < t < T_s/2$ , the switch voltage  $v_s(t)$  is equal to  $+V_g$ . For  $0 < t < t_\alpha$ , the current  $i_s(t)$  is negative and diodes  $D_1$  and  $D_4$  conduct. Transistors  $Q_1$  and  $Q_4$  conduct when  $i_s(t)$  is positive, over the interval  $t_\alpha < t < T_s/2$ . The waveforms during  $T_s/2 < t < T_s$  are

symmetrical. Since the zero crossing of  $v_s(t)$  leads the zero crossing of  $i_s(t)$ , the transistors conduct after their respective antiparallel diodes. Note that, at any given time during the  $D_1$  conduction interval  $0 < t < t_\alpha$ , transistor  $Q_1$  can be turned on without incurring switching loss. The circuit naturally causes the transistor turn-on transition to be lossless, and long turn-on switching times can be tolerated. A particularly significant implication of this is that the switching loss associated with reverse recovery of the antiparallel diodes is avoided. Relatively slow diodes, such as the MOSFET body diodes, can be employed for realization of diodes  $D_1$  to  $D_4$ . In addition, the output capacitances of transistors  $Q_1$  to  $Q_4$  and diodes  $D_1$  to  $D_4$  do not lead to switching loss.

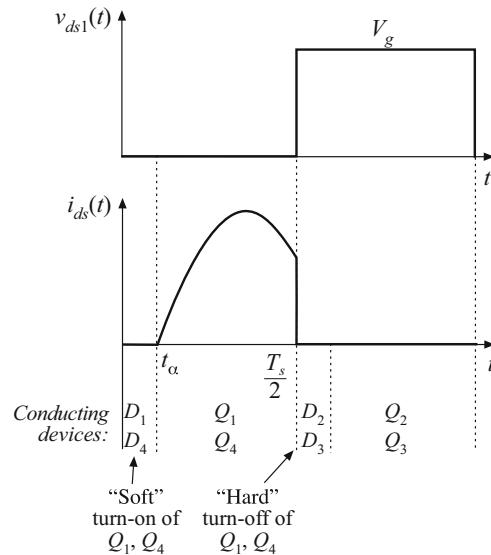
In general, zero-voltage switching can occur when the resonant tank presents an effective inductive load to the switches, and hence the switch voltage zero crossings occur before the switch current zero crossings. In the bridge configuration, zero-voltage switching is characterized by the half-bridge conduction sequence  $D_1-Q_1-D_2-Q_2$ , such that the transistors are turned on while their respective antiparallel diodes conduct. Since the transistor voltage is zero during the entire turn-on transition, switching loss due to slow turn-on times or due to energy storage in any of the device capacitances does not occur at turn-on.

The transistor turn-off transition in Fig. 22.28 is similar to that of a PWM switch. In converters that employ IGBTs or other minority-carrier devices, significant switching loss may occur at the turn-off transitions. The current tailing phenomenon causes  $Q_1$  to pass through a period of high instantaneous power dissipation, and switching loss occurs.

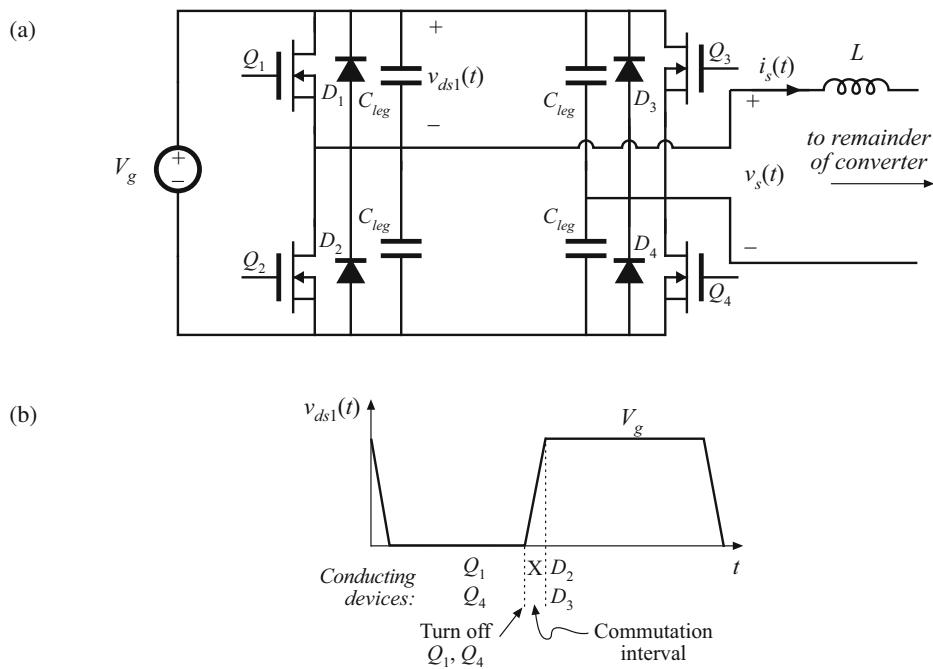
To assist the transistor turn-off process, small capacitors  $C_{leg}$  may be introduced into the legs of the bridge, as demonstrated in Fig. 22.29. In a converter employing MOSFETs, the device output capacitances are sufficient for this purpose, with no need for external discrete capacitors. A delay is also introduced into the gate drive signals, so that there is a short commutation interval when all four transistors are off. During the normal  $Q_1$ ,  $D_1$ ,  $Q_2$ , and  $D_2$  conduction intervals, the leg capacitors appear in parallel with the semiconductor switches, and have no effect on the converter operation. However, these capacitors introduce commutation intervals at transistor turn-off. When  $Q_1$  is turned off, the tank current  $i_s(T_s/2)$  flows through the switch capacitances  $C_{leg}$  instead of  $Q_1$ , and the voltage across  $Q_1$  and  $C_{leg}$  increases. Eventually, the voltage across  $Q_1$  reaches  $V_g$ ; diode  $D_2$  then becomes forward-biased. If the MOSFET turn-off time is sufficiently fast, then the MOSFET is switched fully off before the drain voltage rises significantly above zero, and negligible turn-off switching loss is incurred. The energy stored in the device capacitances, that is, in  $C_{leg}$ , is transferred to the tank inductor. The fact that none of the semiconductor device capacitances or stored charges lead to switching loss is the major advantage of zero-voltage switching, and is the most common motivation for its use. MOSFET converters can typically be operated in this manner, using only the internal drain-to-source capacitances. However, other devices such as IGBTs typically require substantial external capacitances to reduce the losses incurred during the IGBT turn-off transitions.

An additional advantage of zero-voltage switching is the reduction of EMI associated with device capacitances. In conventional PWM converters and also, to some extent, in zero-current switching converters, significant high-frequency ringing and current spikes are generated by the rapid charging and discharging of the semiconductor device capacitances during the turn-on and/or turn-off transitions.

Ringing is conspicuously absent from the waveforms of converters in which all semiconductor devices switch at zero voltage; these converters inherently do not generate this type of EMI.



**Fig. 22.28** Transistor  $Q_1$  voltage and current waveforms, for operation of the series resonant converter above resonance in the  $k = 0$  CCM

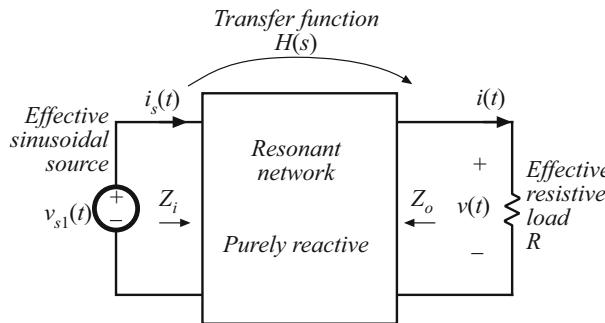


**Fig. 22.29** Introduction of small capacitors  $C_{leg}$ , which reduce the turn-off-transition switching loss when the series resonant converter is operated above resonance: (a) bridge circuit, (b) transistor voltage waveform

## 22.4 Load-Dependent Properties of Resonant Converters

The properties of the CCM PWM converters studied in previous chapters are largely unaffected by the load current. In consequence, these converters exhibit several desirable properties that are often taken for granted. The transistor current is proportional to the load current; hence conduction losses become small at light load, leading to good light-load efficiency. Also, the output impedance is low, and hence the dc output voltage does not significantly depend on the load  $i - v$  characteristic (at least, in CCM). Unfortunately, these good properties are not necessarily shared by resonant converters. Of central importance in design of a resonant converter is the selection of the resonant tank topology and element values, so that the transistor conduction losses at light load are minimized, so that zero-voltage switching is obtained over a wide range of load currents (preferably, for all anticipated loads, but at least at full and intermediate load powers), and so that the converter dynamic range is compatible with the load  $i - v$  characteristic. These design issues are addressed in this section.

The conduction loss caused by circulating tank currents is well-recognized as a problem in resonant converter design. These currents are independent of, or only weakly dependent on, the load current, and lead to poor efficiency at light load. In Fig. 22.30, the switch current  $i_s(s)$  is equal to  $v_s(s)/Z_i(s)$ . If we want the switch current to track the load current, then at the switching frequency  $\|Z_i\|$  should be dominated by, or at least strongly influenced by, the load resistance  $R$ . Unfortunately, this is often not consistent with the requirement for zero-voltage switching, in which  $Z_i$  is dominated by a tank inductor.



**Fig. 22.30** Resonant inverter model

To design a resonant converter that exhibits good properties, the engineer must develop physical insight into how the load resistance  $R$  affects the tank input impedance and output voltage.

In this section, the inverter output characteristics, zero-voltage switching boundary, and the dependence of transistor current on load resistance, are related to the properties of the tank network under the extreme conditions of an open-circuited or short-circuited load. The undamped tank network responses are easily plotted, and the insight needed to optimize the tank network design can be gained quickly.

### 22.4.1 Inverter Output Characteristics

Let us first investigate how the magnitude of the inverter output voltage  $\|v\|$  depends on the load current magnitude  $\|i\|$ . Consider the resonant inverter system of Fig. 22.30. Let  $H_\infty(s)$  be the open-circuit ( $R \rightarrow \infty$ ) transfer function of the tank network:

$$H_\infty(s) = \frac{v(s)}{v_{s1}(s)} \Big|_{R \rightarrow \infty} \quad (22.33)$$

and let  $Z_{o0}(s)$  be the output impedance, determined when the source  $v_{s1}(s)$  is short-circuited. Then we can model the output port of the tank network using the Thevenin-equivalent circuit of Fig. 22.31. Solution of this circuit using the voltage divider formula leads to

$$v(s) = H_\infty(s)v_{s1}(s) \frac{R}{R + Z_{o0}(s)} \quad (22.34)$$

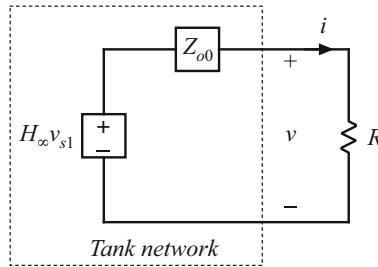
At a given angular switching frequency  $\omega_s = 2\pi f_s$ , the phasor representing the magnitude and phase of the ac output voltage is found by letting  $s = j\omega_s$ :

$$v(j\omega_s) = H_\infty(j\omega_s)v_{s1}(j\omega_s) \frac{R}{R + Z_{o0}(j\omega_s)} \quad (22.35)$$

The magnitude can be found by noting that

$$\|v(j\omega_s)\|^2 = v(j\omega_s)v^*(j\omega_s) \quad (22.36)$$

where  $v^*(j\omega_s)$  is the complex conjugate of  $v(j\omega_s)$ . Substitution of Eq. (22.35) into Eq. (22.36) leads to



**Fig. 22.31** Thevenin-equivalent circuit that models the output port of the tank network

$$\begin{aligned} \|v(j\omega_s)\|^2 &= \left( H_\infty(j\omega_s)v_{s1}(j\omega_s) \frac{R}{R + Z_{o0}(j\omega_s)} \right) \left( H_\infty(j\omega_s)v_{s1}(j\omega_s) \frac{R}{R + Z_{o0}(j\omega_s)} \right)^* \\ &= H_\infty(j\omega_s)H_\infty^*(j\omega_s)v_{s1}(j\omega_s)v_{s1}^*(j\omega_s) \frac{R^2}{(R + Z_{o0}(j\omega_s))(R + Z_{o0}(j\omega_s))^*} \\ &= \|H_\infty(j\omega_s)\|^2 \|v_{s1}(j\omega_s)\|^2 \frac{R^2}{(R + Z_{o0}(j\omega_s))(R + Z_{o0}(j\omega_s))^*} \end{aligned} \quad (22.37)$$

This result can be further simplified with the assumption that the tank network contains only purely reactive elements, i.e., that any losses or other resistive elements within the tank network have negligible effect. Then the output impedance  $Z_{o0}(j\omega_s)$ , as well as all other driving-point impedances of the tank network, are purely imaginary quantities. This implies that the complex conjugate  $Z_{o0}^*(j\omega_s)$  is given by

$$Z_{o0}^*(j\omega_s) = -Z_{o0}(j\omega_s) \quad (22.38)$$

Substitution of Eq. (22.38) into Eq. (22.37) and simplification leads to

$$\|v(j\omega_s)\|^2 = \frac{\|H_\infty(j\omega_s)\|^2 \|v_s(j\omega_s)\|^2}{\left(1 + \frac{\|Z_{o0}(j\omega_s)\|^2}{R^2}\right)} \quad (22.39)$$

with

$$R = \frac{\|v(j\omega_s)\|}{\|i(j\omega_s)\|} \quad (22.40)$$

Substitution of Eq. (22.40) into Eq. (22.39) and rearrangement of terms yields

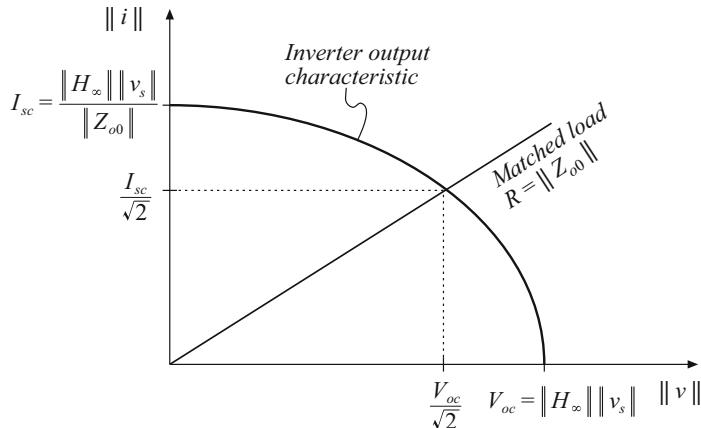
$$\|v(j\omega_s)\|^2 + \|i(j\omega_s)\|^2 \|Z_{o0}(j\omega_s)\|^2 = \|H_\infty(j\omega_s)\|^2 \|v_s(j\omega_s)\|^2 \quad (22.41)$$

Hence, at a given frequency, the inverter output characteristic, that is, the relationship between  $\|v(j\omega_s)\|$  and  $\|i(j\omega_s)\|$  is elliptical. Equation (22.41) can be further rearranged, into the form

$$\frac{\|v(j\omega_s)\|^2}{V_{oc}^2} + \frac{\|i(j\omega_s)\|^2}{I_{sc}^2} = 1 \quad (22.42)$$

where the open-circuit voltage  $V_{oc}$  and short-circuit current  $I_{sc}$  are given by

$$\begin{aligned} V_{oc} &= \|H_\infty(j\omega_s)\| \|v_s(j\omega_s)\| \\ I_{sc} &= \frac{\|H_\infty(j\omega_s)\| \|v_s(j\omega_s)\|}{\|Z_{o0}(j\omega_s)\|} = \frac{V_{oc}}{\|Z_{o0}(j\omega_s)\|} \end{aligned} \quad (22.43)$$



**Fig. 22.32** Elliptical output characteristics of resonant inverters. A resistive matched load is also illustrated

These inverter output characteristics are constructed in Fig. 22.32. This characteristic describes how, at a given switching frequency, the ac output voltage magnitude varies as the circuit is loaded. The equilibrium output voltage is given by the intersection of this elliptical characteristic with the load  $i - v$  characteristic. For example, Fig. 22.32 also illustrates a superimposed resistive load line having slope  $1/R$ , in the special case where  $R = \|Z_{o0}(j\omega_s)\|$ . This value of  $R$  corresponds to matched-load operation, in which the converter output power is maximized. It can be shown that the operating point is then given by

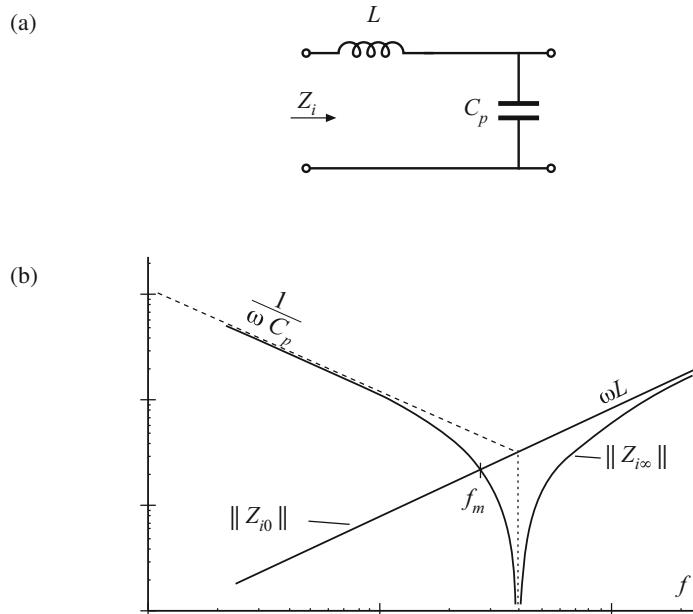
$$\begin{aligned}\|v(j\omega_s)\|^2 &= \frac{V_{oc}}{\sqrt{2}} \\ \|i(j\omega_s)\|^2 &= \frac{I_{sc}}{\sqrt{2}}\end{aligned}\quad (22.44)$$

Note that Fig. 22.32 can also be applied to the output  $i - v$  characteristics of resonant dc–dc converters, since the output rectifier then loads the tank with an effective resistive load  $R_e$ .

### 22.4.2 Dependence of Transistor Current on Load

The transistors must conduct the current appearing at the input port of the tank network,  $i_s(t)$ . This current is determined by the tank network input impedance  $Z_i(j\omega_s)$ :

$$i_{s1}(j\omega_s) = \frac{v_{s1}(j\omega_s)}{Z_i(j\omega_s)} \quad (22.45)$$



**Fig. 22.33** Tank network, parallel resonant converter example: (a) tank circuit, (b) bode plot of input impedance magnitude  $\|Z_i\|$  for the limiting cases  $R \rightarrow 0$  and  $R \rightarrow \infty$

As described previously, obtaining good light-load efficiency requires that  $\|Z_i(j\omega_s)\|$  increase as the load resistance  $R$  increases. To understand how  $\|Z_i(j\omega_s)\|$  depends on  $R$ , let us sketch  $\|Z_i(j\omega_s)\|$  in the extreme cases of an open-circuited ( $R \rightarrow \infty$ ) and short-circuited ( $R \rightarrow 0$ ) load:

$$\begin{aligned} Z_{i0}(j\omega_s) &= Z_i(j\omega_s)|_{R \rightarrow 0} \\ Z_{i\infty}(j\omega_s) &= Z_i(j\omega_s)|_{R \rightarrow \infty} \end{aligned} \quad (22.46)$$

For example, consider the parallel resonant converter of Figs. 22.19, 22.20, 22.21, 22.22, 22.23. The Bode diagrams of the impedances  $\|Z_{i0}(j\omega_s)\|$  and  $\|Z_{i\infty}(j\omega_s)\|$  are constructed in Fig. 22.33.  $Z_{i0}(s)$  is found with the load  $R$  shorted, and is equal to the inductor impedance  $sL$ .  $Z_{i\infty}(s)$ , found with the load  $R$  open-circuited, is given by the series combination  $(sL + 1/sC)$ . It can be seen in Fig. 22.33 that the impedance magnitudes  $\|Z_{i0}(j\omega_s)\|$  and  $\|Z_{i\infty}(j\omega_s)\|$  intersect at frequency  $f_m$ . If the switching frequency is chosen such that  $f_s < f_m$ , then  $\|Z_{i\infty}(j\omega_s)\| > \|Z_{i0}(j\omega_s)\|$ . The converter then exhibits the desirable characteristic that the no-load switch current magnitude  $\|v_s(j\omega_s)\|/\|Z_{i\infty}(j\omega_s)\|$  is smaller than the switch current under short-circuit conditions,  $\|v_s(j\omega_s)\|/\|Z_{i0}(j\omega_s)\|$ . In fact, the short-circuit switch current is limited by the impedance of the tank inductor, while the open-circuit switch current is determined primarily by the impedance of the tank capacitor.

If the switching frequency is chosen such that  $f_s > f_m$ , then  $\|Z_{i\infty}(j\omega_s)\| < \|Z_{i0}(j\omega_s)\|$ . The no-load switch current is then greater in magnitude than the switch current when the load is short-circuited! When the load current is reduced or removed, the transistors will continue to conduct large currents and generate high conduction losses. This causes the efficiency at light load to be poor. It can be concluded that, to obtain good light-load efficiency in the parallel resonant converter, one should choose  $f_s$  sufficiently less than  $f_m$ . Unfortunately, this requires operation below resonance, leading to reduced output voltage dynamic range and a tendency to lose the zero-voltage switching property. Input impedances of the series, parallel, and LCC tank circuits are sketched in Fig. 22.34.

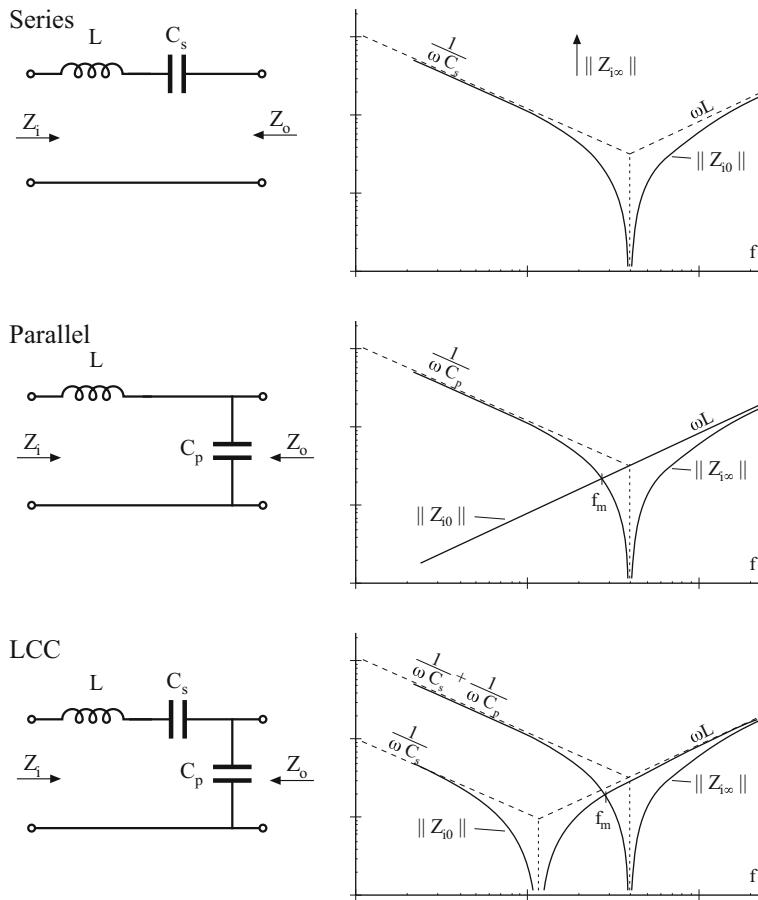
A remaining question is how  $\|Z_i(j\omega_s)\|$  behaves for intermediate values of load between the open-circuit and short-circuit conditions. The answer is given by Theorem 22.1 below:  $\|Z_i(j\omega_s)\|$  varies monotonically with  $R$ , and therefore is bounded by  $\|Z_{i0}(j\omega_s)\|$  and  $\|Z_{i\infty}(j\omega_s)\|$ . Hence, the Bode plots of the limiting cases  $\|Z_{i0}(j\omega_s)\|$  and  $\|Z_{i\infty}(j\omega_s)\|$  provide a correct qualitative understanding of the behavior of  $\|Z_i\|$  for all  $R$ . The theorem is valid for lossless tank networks.

**Theorem 22.1.** *If the tank network is purely reactive, then its input impedance  $\|Z_i\|$  is a monotonic function of the load resistance  $R$ .*

This theorem is proven by use of Middlebrook's Extra Element Theorem (see Chap. 16). The tank network input impedance  $Z_i(s)$  can be expressed as a function of the load resistance  $R$  and the tank network driving-point impedances, as follows:

$$Z_i(s) = Z_{i0}(s) \frac{\left(1 + \frac{R}{Z_{o0}(s)}\right)}{\left(1 + \frac{R}{Z_{o\infty}(s)}\right)} = Z_{i\infty}(s) \frac{\left(1 + \frac{Z_{o0}(s)}{R}\right)}{\left(1 + \frac{Z_{o\infty}(s)}{R}\right)} \quad (22.47)$$

where  $Z_{i0}$  and  $Z_{i\infty}$  are the resonant network input impedances, with the load short-circuited or open-circuited, respectively, and  $Z_{o0}$  and  $Z_{o\infty}$  are the resonant network output impedances, with



**Fig. 22.34** Series, parallel, and LCC resonant tank networks, and their input impedances  $Z_{i0}$  and  $Z_{i\infty}$

the source input short-circuited or open-circuited, respectively. These terminal impedances are simple functions of the tank elements, and their Bode diagrams are easily constructed. The input impedances of the series resonant, parallel resonant, and LCC inverters are listed in Fig. 22.34. Since these impedances do not depend on the load, they are purely reactive, ideally have zero real parts [330], and their complex conjugates are given by  $Z_{o0}^* = -Z_{o0}$ ,  $Z_{o\infty}^* = -Z_{o\infty}$ , etc. Again, recall that the magnitude of a complex impedance  $Z(j\omega)$  can be expressed as the square root of  $Z(j\omega)Z^*(j\omega)$ . Hence, the magnitude of  $Z_i(s)$  is given by

$$\begin{aligned}
\|Z_i\|^2 &= Z_i Z_i^* = Z_{i0}(s) Z_{i0}^*(s) \frac{\left(1 + \frac{R}{Z_{o0}(s)}\right) \left(1 + \frac{R}{Z_{o0}^*(s)}\right)}{\left(1 + \frac{R}{Z_{o\infty}(s)}\right) \left(1 + \frac{R}{Z_{o\infty}^*(s)}\right)} \\
&= \|Z_{i0}\|^2 \frac{\left(1 + \frac{R^2}{\|Z_{o0}\|^2}\right)}{\left(1 + \frac{R^2}{\|Z_{o\infty}\|^2}\right)}
\end{aligned} \tag{22.48}$$

where  $Z_i^*$  is the complex conjugate of  $Z_i$ .

Next, let us differentiate Eq. (22.48) with respect to  $R$ :

$$\frac{d\|Z_i\|^2}{dR} = 2R\|Z_{i0}\|^2 \frac{\left(\frac{1}{\|Z_{o0}\|^2} - \frac{1}{\|Z_{o\infty}\|^2}\right)}{\left(1 + \frac{R^2}{\|Z_{o\infty}\|^2}\right)^2} \tag{22.49}$$

The derivative has roots at (i)  $R = 0$ , (ii)  $R = \infty$ , and in the special case (iii) where  $\|Z_{i0}\| = \|Z_{i\infty}\|$ . Since the derivative is otherwise nonzero, the resonant network input impedance  $\|Z_i\|$  is a monotonic function of  $R$ , over the range  $0 < R < \infty$ . In special case (iii),  $\|Z_i\|$  is independent of  $R$ . Therefore, Theorem 22.1 is proved.

An example is given in Figs. 22.36 and 22.35, for the LCC inverter. Figure 22.35 illustrates the impedance asymptotes of the limiting cases  $\|Z_{i0}\|$  and  $\|Z_{i\infty}\|$ . Variation of  $\|Z_i\|$  between these limits, for finite nonzero  $R$ , is illustrated in Fig. 22.36. The open-circuit resonant frequency  $f_\infty$  and the short-circuit resonant frequency  $f_0$  are given by

$$\begin{aligned}
f_0 &= \frac{1}{2\pi\sqrt{LC_s}} \\
f_\infty &= \frac{1}{2\pi\sqrt{LC_s\|C_p\|}}
\end{aligned} \tag{22.50}$$

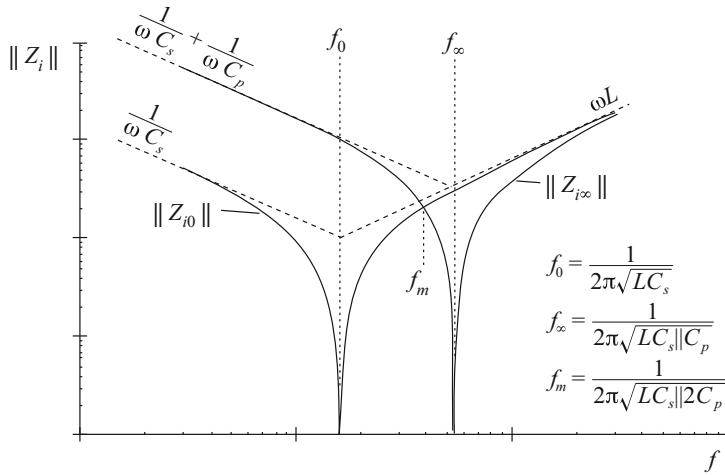
where  $C_s\|C_p\|$  denotes inverse addition of  $C_s$  and  $C_p$ :

$$C_s\|C_p = \frac{1}{\frac{1}{C_s} + \frac{1}{C_p}} \tag{22.51}$$

For the LCC inverter, the impedance magnitudes  $\|Z_{i0}\|$  and  $\|Z_{i\infty}\|$  are equal at frequency  $f_m$ , given by

$$f_m = \frac{1}{2\pi\sqrt{LC_s\|2C_p\|}} \tag{22.52}$$

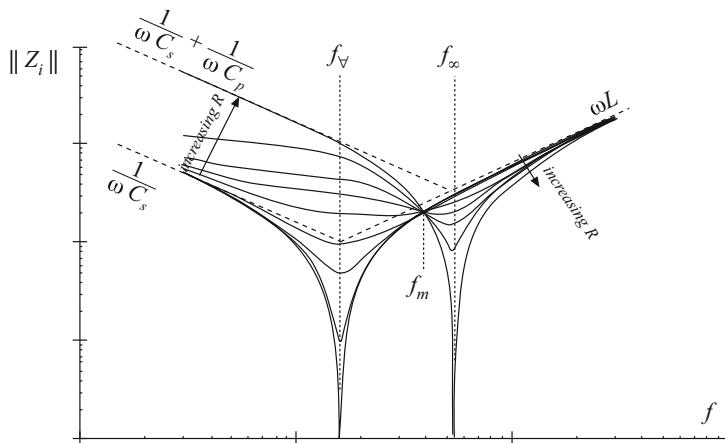
If the switching frequency is chosen to be greater than  $f_m$ , then  $\|Z_{i\infty}\|$  is less than  $\|Z_{i0}\|$ . This implies that, as the load current is decreased, the transistor current will increase. Such a converter will have poor efficiency at light load, and will exhibit significant circulating currents. If the switching frequency is chosen to be less than  $f_m$ , then the transistor current will increase with decrease with decreasing load current. The short-circuit current is limited by  $\|Z_{i0}\|$ , while



**Fig. 22.35** Construction of the quantities  $\|Z_{i0}\|$  and  $\|Z_{i\infty}\|$ , for the LCC inverter

the circulating currents under open-circuit conditions are determined by  $\|Z_{i\infty}\|$ . In general, if  $f > f_m$ , then the transistor current is greater than or equal to the short-circuit current for all  $R$ . The inequality is reversed when  $f < f_m$ .

The impedance magnitudes  $\|Z_{i0}\|$  and  $\|Z_{i\infty}\|$  are illustrated in Fig. 22.34 for the series, parallel, and LCC tank networks. In the case of the series tank network,  $\|Z_{i\infty}\| = \infty$ . In consequence, the no-load transistor current is zero, both above resonance and below resonance. Hence, the series resonant inverter exhibits the desirable property that the transistor current is proportional to the load current. In addition, when the load is short-circuited, the current magnitude is limited by the impedance of the series resonant tank. For the parallel and LCC inverters, it is desirable to operate below the frequency  $f_m$ .



**Fig. 22.36** Variation of tank network input impedance  $\|Z_i\|$  with load resistance  $R$ , LCC inverter. As the load resistance is increased,  $\|Z_i\|$  changes monotonically from  $\|Z_{i0}\|$  to  $\|Z_{i\infty}\|$

Thus, the dependence of the transistor current on load can be easily determined, using an intuitive frequency-domain approach.

### 22.4.3 Dependence of the ZVS/ZCS Boundary on Load Resistance

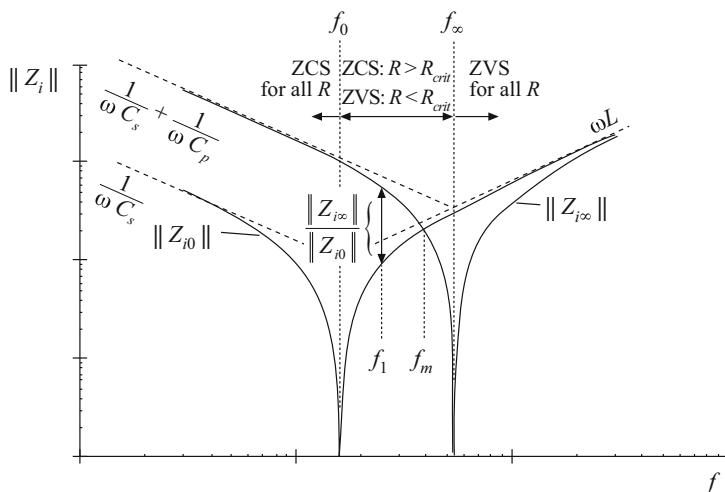
It is also necessary to determine the critical load resistance  $R = R_{crit}$  at the boundary between ZVS and ZCS. This boundary can also be expressed as a function of the impedances  $Z_{i0}$  and  $Z_{i\infty}$ .

As discussed in Sect. 22.3, zero-voltage switching occurs when the switch current  $i_s(t)$  lags the switch voltage  $v_s(t)$ . Zero-voltage switching occurs when  $i_s(t)$  leads  $v_s(t)$ . This definition ignores the effects of semiconductor output capacitances, and hence gives an approximate ZVS/ZCS boundary. The phase between the switch current and switch voltage is again determined by the input impedance of the tank network:

$$i_{s1}(j\omega_s) = \frac{v_{s1}(j\omega_s)}{Z_i(j\omega_s)} \quad (22.53)$$

Hence, zero-voltage switching occurs when  $Z_i(j\omega_s)$  is inductive in nature, zero-current switching occurs when  $Z_i(j\omega_s)$  is capacitive in nature, and the ZVS/ZCS boundary occurs where  $Z_i(j\omega_s)$  has zero phase.

It is instructive to again consider the limiting cases of a short-circuited and open-circuited load. The Bode plots of  $Z_{i0}(j\omega_s)$  and  $Z_{i\infty}(j\omega_s)$  for an LCC inverter example are sketched in Fig. 22.37. Since, in these limiting cases, the input impedance  $Z_i$  is composed only of the reactive tank elements,  $Z_{i0}(j\omega_s)$  and  $Z_{i\infty}(j\omega_s)$  are purely imaginary quantities having phase of either  $-90^\circ$  or  $+90^\circ$ . For  $f_s < f_0$ , both  $Z_{i0}(j\omega_s)$  and  $Z_{i\infty}(j\omega_s)$  are dominated by the tank capacitor or capacitors; the phase of  $Z_i(j\omega_s)$  is therefore  $-90^\circ$ . Hence, zero-current switching is obtained under both short-circuit and open-circuit conditions. For  $f_s > f_\infty$ , both  $Z_{i0}(j\omega_s)$  and  $Z_{i\infty}(j\omega_s)$  are dominated by the tank inductor; hence the phase of  $Z_i(j\omega_s)$  is  $+90^\circ$ . Zero-voltage switching



**Fig. 22.37** Use of the input impedance quantities  $Z_{i0}$  and  $Z_{i\infty}$  to determine the ZCS/ZVS boundaries, LCC example

is obtained for both a short-circuited and an open-circuited load. For  $f_0 < f_s < f_\infty$ ,  $Z_{i0}(j\omega_s)$  is dominated by the tank inductor while  $Z_{i\infty}(j\omega_s)$  is dominated by the tank capacitors. This implies that zero-voltage switching is obtained under short-circuit conditions, and zero-voltage switching is obtained under open-circuit conditions. For this case, there must be some critical value of load resistance  $R = R_{crit}$  that represents the boundary between ZVS and ZCS, and that causes the phase of  $Z_i(j\omega_s)$  to be equal to  $0^\circ$ .

The behavior of  $Z_i(j\omega_s)$  for nonzero finite  $R$  is easily extrapolated from the limiting cases discussed above. Theorem 22.2 below shows that:

1. If zero-current switching occurs for both an open-circuited load and a short-circuited load [i.e.,  $Z_{i0}(j\omega_s)$  and  $Z_{i\infty}(j\omega_s)$  both have phase  $+90^\circ$ ], then zero-current switching occurs for all loads.
2. If zero-voltage switching occurs for both an open-circuited load and a short-circuited load [i.e.,  $Z_{i0}(j\omega_s)$  and  $Z_{i\infty}(j\omega_s)$  both have phase  $-90^\circ$ ], then zero-voltage switching occurs for all loads.
3. If zero-voltage switching occurs for an open-circuited load and zero-current switching occurs for a short-circuited load [i.e.,  $Z_{i0}(j\omega_s)$  has phase  $-90^\circ$  and  $Z_{i\infty}(j\omega_s)$  has phase  $+90^\circ$ ], then zero-voltage switching occurs for  $R > R_{crit}$ , and zero-current switching occurs for  $R < R_{crit}$ , with  $R_{crit}$  given by Eq. (22.54) below.
4. If zero-current switching occurs for an open-circuited load and zero-voltage switching occurs for a short-circuited load [i.e.,  $Z_{i0}(j\omega_s)$  has phase  $+90^\circ$  and  $Z_{i\infty}(j\omega_s)$  has phase  $-90^\circ$ ], then zero-current switching occurs for  $R > R_{crit}$ , and zero-voltage switching occurs for  $R < R_{crit}$ , with  $R_{crit}$  given by Eq. (22.54) below.

For the LCC example, we can therefore conclude that, for  $f_s < f_0$ , zero-current switching occurs for all values of  $R$ . For  $f_s > f_\infty$ , zero-voltage switching occurs for all values of  $R$ . For  $f_0 < f_s < f_\infty$ , the boundary between ZVS and ZCS is given by Eq. (22.54).

**Theorem 22.2.** *If the tank network is purely reactive, then the boundary between zero-current switching and zero-voltage switching occurs when the load resistance  $R$  is equal to the critical value  $R_{crit}$ , given by*

$$R_{crit} = \|Z_{o0}\| \sqrt{\frac{-Z_{i\infty}}{Z_{i0}}} \quad (22.54)$$

This theorem relies on the assumption that zero-current switching occurs when the tank input impedance is capacitive in nature, while zero-voltage switching occurs for inductive-input impedances. The boundary therefore occurs where the phase of  $Z_i(j\omega)$  is zero. This definition gives a necessary but not sufficient condition for zero-voltage switching when significant semiconductor output capacitance is present.

The result is derived by finding the value of  $R$  which causes the imaginary part of  $Z_i(j\omega)$  in Eq. (22.47) to be zero. Since the tank network is assumed to ideal and lossless, the impedances  $Z_{o\infty}$ ,  $Z_{o0}$ , and  $Z_{i\infty}$  must have zero real parts. Hence,

$$\text{Im}(Z_i(R_{crit})) = \text{Im}(Z_{i\infty}) \text{Re} \left( \frac{1 + \frac{Z_{o0}}{R_{crit}}}{1 + \frac{Z_{o\infty}}{R_{crit}}} \right) = \text{Im}(Z_{i\infty}) \frac{\left( 1 - \frac{Z_{o0}Z_{o\infty}}{R_{crit}^2} \right)}{\left( 1 + \frac{\|Z_{o\infty}\|^2}{R_{crit}^2} \right)} = 0 \quad (22.55)$$

where  $\text{Im}(Z)$  and  $\text{Re}(Z)$  denote the imaginary and real parts of the complex quantity  $Z$ . The nontrivial solution to Eq. (22.55) is given by

$$1 = \frac{Z_{o0}Z_{o\infty}}{R_{crit}^2} \quad (22.56)$$

hence,

$$R_{crit} = \sqrt{Z_{o0}Z_{o\infty}} \quad (22.57)$$

A useful equivalent form makes use of the reciprocity identities

$$\frac{Z_{o0}}{Z_{o\infty}} = \frac{Z_{i0}}{Z_{i\infty}} \quad (22.58)$$

Use of Eq. (22.58) to eliminate  $Z_{o\infty}$  from Eq. (22.57) leads to

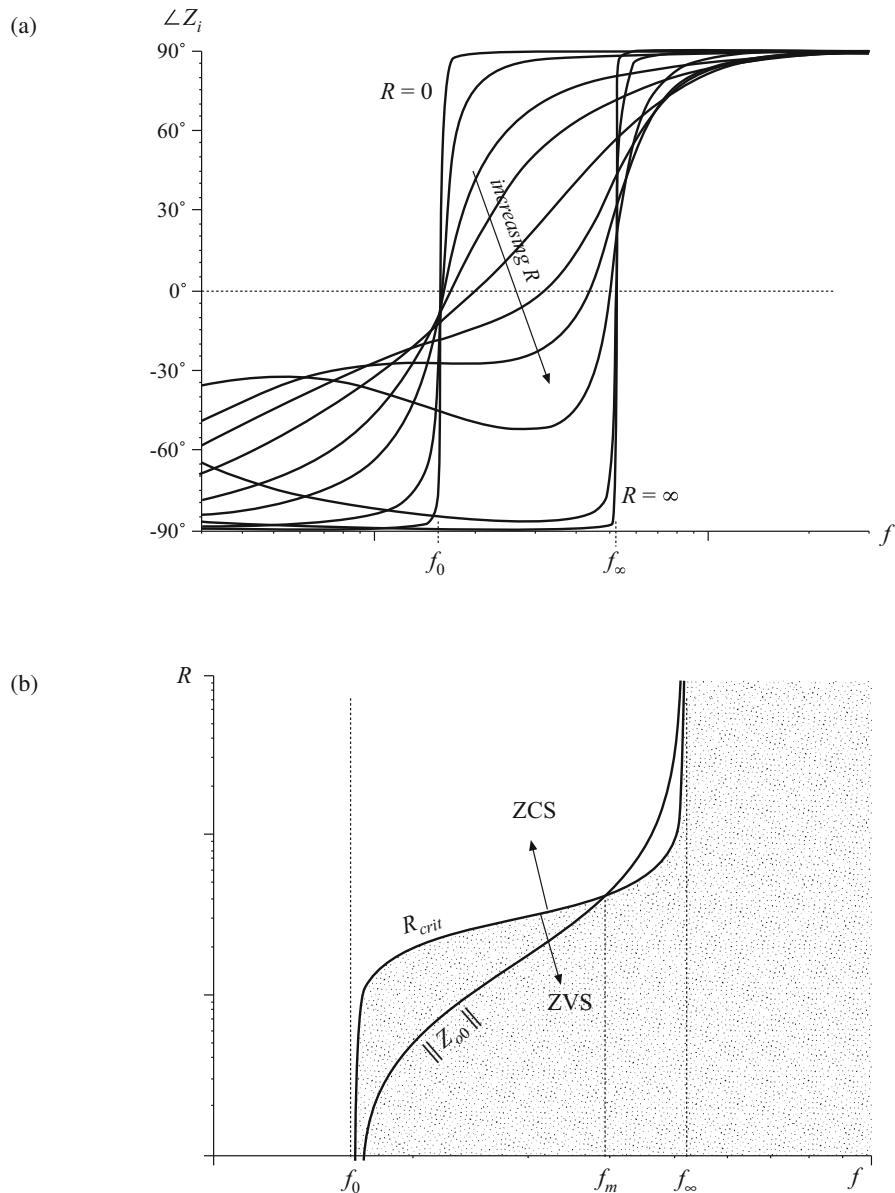
$$R_{crit} = \|Z_{o0}\| \sqrt{\frac{-Z_{i\infty}}{Z_{i0}}} \quad (22.59)$$

This is the desired result. The quantity  $Z_{o0}$  is the inverter output impedance, and  $R = \|Z_{o0}\|$  corresponds to operation at matched load with maximum output power. The impedances  $Z_{i\infty}$  and  $Z_{i0}$  are purely imaginary, and hence Eq. (22.59) has no real solution unless  $Z_{i\infty}$  and  $Z_{i0}$  are of opposite phase. As illustrated in Fig. 22.37, if at a given frequency  $Z_{i\infty}$  and  $Z_{i0}$  are both inductive, then zero-voltage switching occurs for all loads. Zero-current switching occurs for all loads when  $Z_{i\infty}$  and  $Z_{i0}$  are both capacitive. Therefore, Theorem 22.2 is proved.

Figure 22.38a illustrates the phase response of  $Z_i(j\omega)$  as  $R$  varies from 0 to  $\infty$ , for the LCC inverter. A typical dependence of  $R_{crit}$  and the matched-load impedance  $\|Z_{o0}\|$  on frequency is illustrated in Fig. 22.38b. Zero-voltage switching occurs for all loads when  $f > f_\infty$ , and zero-current switching occurs for all loads when  $f < f_0$ . Over the range  $f_0 < f < f_\infty$ ,  $Z_{i0}$  is inductive while  $Z_{i\infty}$  is capacitive; hence, zero-voltage switching occurs for  $R < R_{crit}$  while zero-current switching occurs for  $R > R_{crit}$ . At frequency  $f_m$ ,  $R_{crit} = \|Z_{o0}\|$ , and hence the ZVS/ZCS boundary is encountered exactly at matched load. It is commonly desired to obtain zero-voltage switching at matched load, with low circulating currents and good efficiency at light load. It is apparent that this requires operation in the range  $f_0 < f < f_m$ . Zero-voltage switching will then be obtained under matched-load and short-circuit conditions, but will be lost at light load. The choice of element values such that  $\|Z_{i0}\| \ll \|Z_{i\infty}\|$  is advantageous in that the range of loads leading to zero-voltage switching is maximized.

#### 22.4.4 Another Example

As another example, let us consider selection of the resonant tank elements to obtain a given output characteristic at a certain switching frequency, and let us evaluate the effect of this choice on  $R_{crit}$ . It is desired to operate a resonant inverter at switching frequency  $f_s = 100$  kHz, with an input voltage of  $V_g = 160$  V. The converter should be capable of producing an open-circuit peak output voltage  $V_{oc} = 400$  V, and should also produce a nominal output of 150 Vrms at 25 W. It is desired to select resonant tank elements that accomplish this.



**Fig. 22.38** ZCS/ZVS boundary, LCC inverter example: (a) variation of tank network input impedance phase shift with load resistance, (b) comparison of  $R_{crit}$  with matched-load impedance  $\|Z_{o0}\|$

The specifications imply that the converter should exhibit an open-circuit transfer function of

$$\|H_{\infty}(j\omega_s)\| = \frac{V_{oc}}{V_{s1}} = \frac{(400 \text{ V})}{\left(\frac{4}{\pi} 160 \text{ V}\right)} = 1.96 \quad (22.60)$$

The required short-circuit current is found by solving Eq. (22.42) for  $I_{sc}$ :

$$I_{sc} = \frac{I}{\sqrt{1 - \left(\frac{V}{V_{oc}}\right)^2}} \quad (22.61)$$

The specifications also imply that the peak voltage and current at the nominal operating point are

$$\begin{aligned} V &= 150 \sqrt{2} = 212 \text{ V} \\ I &= \frac{P}{V_{rms}} \sqrt{2} = \frac{25 \text{ W}}{150 \text{ V}} \sqrt{2} = 0.236 \text{ A} \\ R_{nom} &= \frac{V}{I} = 900 \Omega \end{aligned} \quad (22.62)$$

Substitution of Eq. (22.62) into Eq. (22.61) yields

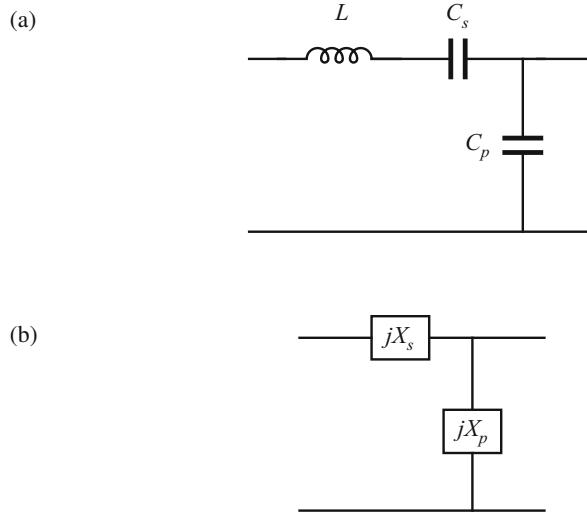
$$I_{sc} = \frac{(0.236 \text{ A})}{\sqrt{1 - \left(\frac{212 \text{ V}}{400 \text{ V}}\right)^2}} = 0.278 \text{ A} \quad (22.63)$$

Matched load therefore occurs at the operating point

$$\begin{aligned} V_{mat} &= \frac{V_{oc}}{\sqrt{2}} = 283 \text{ V} \\ I_{mat} &= \frac{I_{sc}}{\sqrt{2}} = 0.196 \text{ A} \\ \|Z_{o0}(j\omega_s)\| &= \frac{V_{oc}}{I_{sc}} = 1439 \Omega \end{aligned} \quad (22.64)$$

Let us select the values of the tank elements in the LCC tank network illustrated in Fig. 22.39a. The impedances of the series and parallel branches can be represented using the reactances  $X_s$  and  $X_p$  illustrated in Fig. 22.39b, with

$$\begin{aligned} jX_s &= j\omega_s L + \frac{1}{j\omega_s C_s} = j\left(\omega_s L - \frac{1}{\omega_s C_s}\right) \\ jX_p &= \frac{1}{j\omega_s C_p} = j\left(-\frac{1}{\omega_s C_p}\right) \end{aligned} \quad (22.65)$$



**Fig. 22.39** Tank network of the LCC inverter example: (a) schematic, (b) representation of series and parallel branches by reactances  $X_s$  and  $X_p$

The transfer function  $H_\infty(j\omega_s)$  is given by the voltage divider formula

$$H_\infty(j\omega_s) = \frac{jX_p}{jX_s + jX_p} \quad (22.66)$$

The output impedance  $Z_{o0}(j\omega_s)$  is given by the parallel combination

$$Z_{o0}(j\omega_s) = jX_s \| jX_p = \frac{-X_s X_p}{j(X_s + X_p)} \quad (22.67)$$

Solution of Eqs. (22.66) and (22.67) for  $X_p$  and  $X_s$  leads to

$$\begin{aligned} jX_p &= \frac{Z_{o0}(j\omega_s)}{1 - H_\infty(j\omega_s)} \\ X_s &= X_p \frac{1 - H_\infty(j\omega_s)}{H_\infty(j\omega_s)} \end{aligned} \quad (22.68)$$

Hence, the capacitance  $C_p$  should be chosen equal to

$$C_p = -\frac{1}{\omega_s X_p} = \frac{H_\infty(j\omega_s) - 1}{\omega_s \|Z_{o0}(j\omega_s)\|} = \frac{(1.96) - 1}{(2\pi 100\text{kHz})(1439\Omega)} \cong 1\text{nF} \quad (22.69)$$

and the reactance of the series branch should be chosen according to

$$X_s = X_p \frac{1 - H_\infty(j\omega_s)}{H_\infty(j\omega_s)} = (-1493\Omega) \frac{1 - (1.96)}{(1.96)} = 733\Omega \quad (22.70)$$

Since  $X_s$  is comprised of the series combination of the inductor  $L$  and capacitor  $C_s$ , there is a degree of freedom in choosing the values of  $L$  and capacitor  $C_s$  to realize  $X_s$ . For example, we could choose  $C_s$  very large (tending to a short circuit); this effectively would result in a parallel resonant converter with  $L = X_s/\omega_s = 1.17\text{mH}$ . For nonzero  $C_s$ ,  $L$  must be chosen according to

$$L = \frac{1}{\omega_s} \left( X_s + \frac{1}{\omega_s C_s} \right) \quad (22.71)$$

For example, the choice  $C_s = C_p = 1.06\text{nF}$  leads to  $L = 3.5\text{mH}$ . Designs using different  $C_s$  will exhibit exactly the same characteristics at the design frequency; however, the behavior at other switching frequencies will differ.

For the tank network illustrated in Fig. 22.39, the value of  $R_{crit}$  is completely determined by the parameters of the output characteristic ellipse; i.e., by the specification of  $V_g$ ,  $V_{oc}$ , and  $I_{sc}$ . Note that  $Z_{o\infty}$ , the tank output impedance with the tank input port open-circuited, is equal to  $jX_p$ . Substitution of expressions for  $Z_{o\infty}$  and  $Z_{o0}$  into Eq. (22.57) leads to the following expression for  $R_{crit}$ :

$$R_{crit} = \sqrt{\frac{Z_{o0}^2(j\omega_s)}{1 - H_\infty(j\omega_s)}} \quad (22.72)$$

Since  $Z_{o0}$  and  $H_\infty$  are determined by the operating point specifications, then  $R_{crit}$  is also. Evaluation of Eq. (22.72) for this example leads to  $R_{crit} = 1466\Omega$ . Therefore, the inverter will operate with zero-voltage switching for  $R < 1466\Omega$ , including at the nominal operating point  $R = 900\Omega$ . Other topologies of tank network, more complex than the circuit illustrated in Fig. 22.39b, may have additional degrees of freedom that allow  $R_{crit}$  to be independently chosen.

The choice  $C_s = 3C_p = 3.2\text{nF}$  leads to  $L = 1.96\mu\text{H}$ . The following frequencies are obtained:

$$\begin{aligned} f_\infty &= 127\text{kHz} \\ f_m &= 100.6\text{kHz} \\ f_s &= 100.0\text{kHz} \\ f_0 &= 64\text{kHz} \end{aligned} \quad (22.73)$$

Regardless of how  $C_s$  is chosen, the open-circuit tank input impedance is

$$Z_{i\infty} = j(X_s + X_p) = j(733\Omega + (-1493\Omega)) = -j760\Omega \quad (22.74)$$

Therefore, when the load is open-circuited, the transistor peak current has magnitude

$$I_{s1} = \frac{V_{s1}}{\|Z_{i\infty}\|} = \frac{\frac{4}{\pi}(160\text{V})}{760\Omega} = 0.268\text{A} \quad (22.75)$$

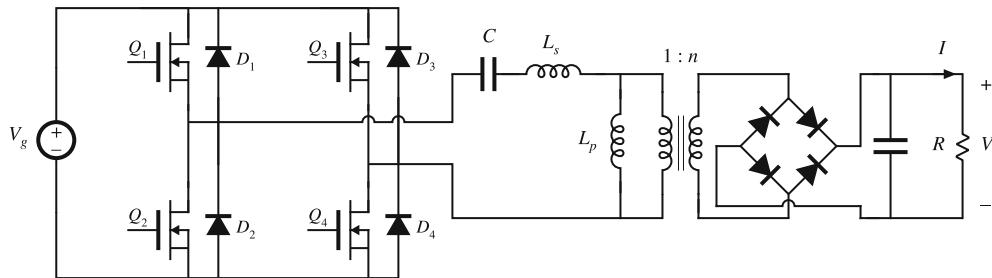
When the load is short-circuited, the transistor peak current has magnitude

$$I_{s1} = \frac{V_{s1}}{\|Z_{i0}\|} = \frac{V_{s1}}{|X_s|} = \frac{\frac{4}{\pi}(160\text{V})}{(733\Omega)} = 0.278\text{A} \quad (22.76)$$

which is nearly the same as the result in Eq. (22.75). The somewhat large open-circuit switch current occurs because of the relatively high specified open-circuit output voltage; lower values of  $V_{oc}$  would reduce the result in Eq. (22.75).

### 22.4.5 LLC Example

A transformer-isolated dc–dc converter based on the *LLC* tank network is illustrated in Fig. 22.40. This converter finds application in off-line dc power supplies, including charger adapters for laptop computers. Tank capacitor  $C$  also functions as a dc blocking capacitor that ensures transformer volt-second balance. Tank inductors  $L_s$  and  $L_p$  can partly or wholly be implemented using the transformer leakage and magnetizing inductances. When the converter is properly designed, the transistors can operate with zero-voltage switching.



**Fig. 22.40** A transformer-isolated dc–dc converter based on the *LLC* resonant tank circuit

The tank input impedances  $Z_{i0}$  (with load shorted) and  $Z_{i\infty}$  (with load open-circuited) are illustrated in Fig. 22.41. Under short-circuit conditions, the tank resonant frequency is

$$f_0 = \frac{1}{2\pi\sqrt{L_s C}} \quad (22.77)$$

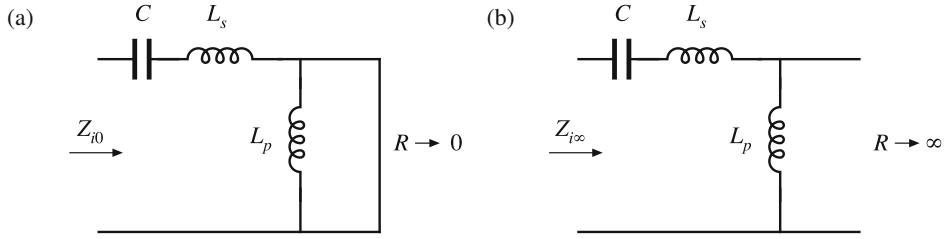
Under open-circuit conditions, the tank resonant frequency is

$$f_\infty = \frac{1}{2\pi\sqrt{(L_s + L_p)C}} \quad (22.78)$$

In each case, the tank input impedance  $Z_i$  is a series resonant circuit, with the short-circuit resonant frequency being higher than the open-circuit resonant frequency. The tank input impedance  $\|Z_i\|$  is constructed in Fig. 22.42.

At low switching frequency  $f_s < f_\infty$ , the transistors operate with zero-current switching for all loads. At high switching frequency  $f_s > f_0$ , the transistors operate with zero-voltage switching for all loads. Over the intermediate frequency range  $f_\infty < f_s < f_0$ , the transistors operate with zero-voltage switching at light load  $R > R_{crit}$ , and with zero-current switching at heavy load  $R < R_{crit}$ . The critical resistance  $R_{crit}$  can be shown to be

$$R_{crit} = R_{o0} \frac{nF}{\sqrt{1+n}} \sqrt{\frac{1 - \frac{F^2}{1+n}}{F^2 - 1}} \quad (22.79)$$



**Fig. 22.41** Tank network of the LLC inverter example: (a) with load shorted, (b) with load open-circuited

with

$$\begin{aligned} R_{o0} &= \sqrt{\frac{L_s}{C}} \\ n &= \frac{L_p}{L_s} \\ F &= \frac{f_s}{f_\infty} \end{aligned} \quad (22.80)$$

For switching frequencies \$f\_s > f\_m\$, the tank circuit exhibits the desirable property that the tank input current decreases as the load current decreases. Operation of this converter at high frequency \$f\_s > f\_0\$ combines the desirable properties of zero-voltage switching at all loads and of tank input current that scales monotonically with load current. Over this range of frequencies, the *LLC* exhibits a conversion ratio less than unity, similar to the series resonant circuit. In the vicinity of \$f\_\infty\$, the *LLC* is capable of boost-type conversion ratios that can become large at light load.

Figure 22.43 illustrates the output characteristic of the *LLC*, for the example \$f\_m < f\_s < f\_0\$. It can be observed that, for this example, \$R\_{crit} < R\_{o0}\$; therefore, the converter exhibits the desirable property that the zero-voltage switching region includes the matched-load conditions as well as open-circuit conditions.

Figure 22.44 illustrates typical control plane \$M\$ vs. \$F\$ characteristics of the *LLC* converter, as predicted by the CCM sinusoidal approximation result of Eq. (22.85). Contours for various values of load resistance are shown, with the specific choice \$L\_p = 5L\_s\$. For low \$Q\$ (large load resistance), the characteristics exhibit a resonance near \$f\_\infty\$ with parallel resonant (boost) characteristics. For large \$Q\$ (low load resistance), the characteristics exhibit a resonance near \$f\_0\$ with series resonant (buck) characteristics.

#### 22.4.6 Results for Basic Tank Networks

The tank networks of Fig. 22.1 can be written in the form shown in Fig. 22.39b. The series and shunt branch reactances are listed in Table 22.1. In this section, the resonant converter general solution and key equations are listed, as functions of the branch reactances \$X\_s\$ and \$X\_p\$.

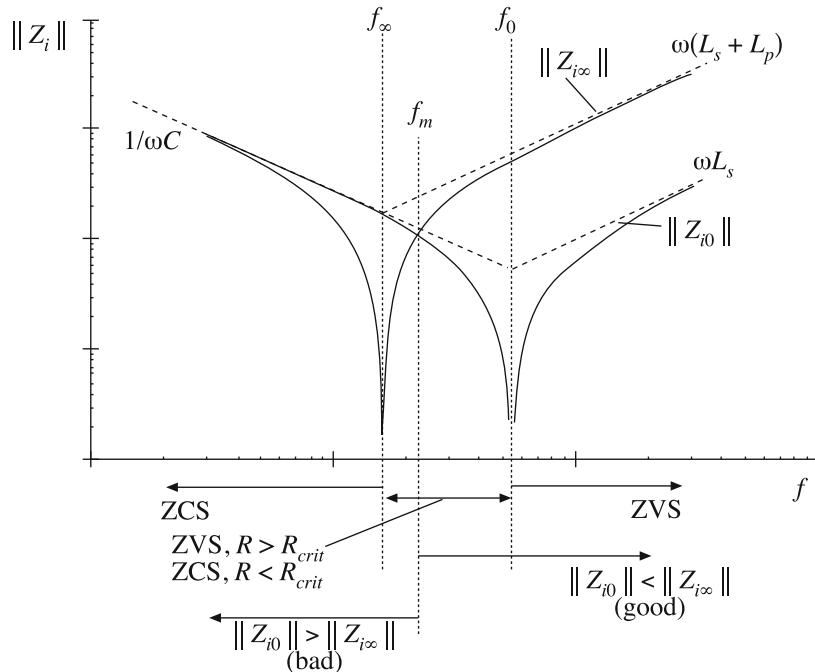
The tank network input impedance is \$Z\_{i0} = jX\_s\$ for \$R\_e = 0\$, and is \$Z\_{i\infty} = j(X\_s + X\_p)\$ for \$R\_e = \infty\$. The unloaded tank transfer function is

$$H_\infty(\omega) = \frac{X_p}{X_p + X_s} \quad (22.81)$$

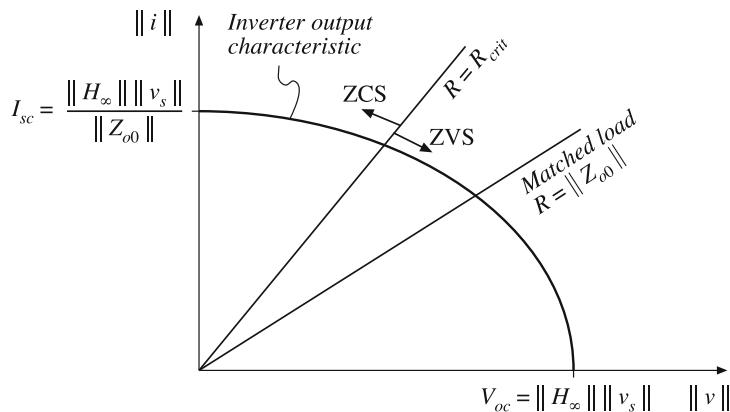
The matched-load impedance (tank output impedance when the input is shorted) is

$$Z_{o0}(\omega) = \frac{jX_s X_p}{X_s + X_p} = jX_s H_\infty(\omega) \quad (22.82)$$

Matched-load resistance occurs at  $R_e = R_{o0}$ , where  $R_{o0} = \|Z_{o0}\|$ .



**Fig. 22.42** Tank input impedance  $\|Z_i\|$  for the LLC tank circuit



**Fig. 22.43** Output plane characteristic of the LLC inverter

The critical load resistance at the boundary between ZVS and ZCS is

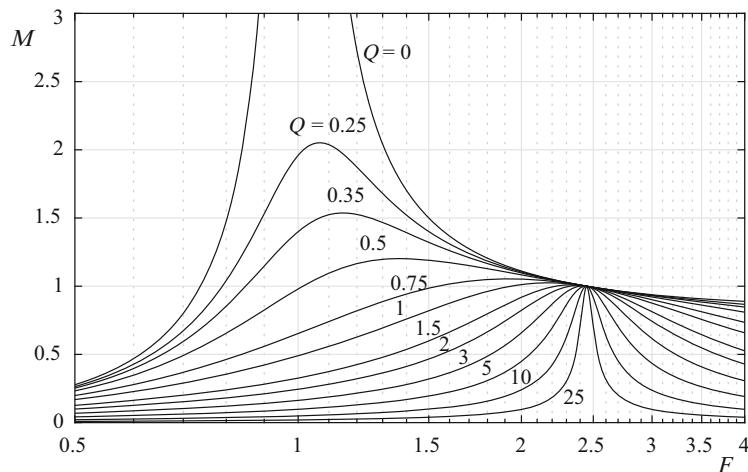
$$R_{crit} = \|Z_{o0}\| \sqrt{-\frac{Z_{i\infty}}{Z_{i0}}} = |X_p| \sqrt{-\frac{X_s}{X_s + X_p}} \quad (22.83)$$

The frequency  $f = f_m$ , where  $\|Z_{i\infty}\| = \|Z_{i0}\|$ , can be shown to occur at the frequency where  $X_s = -X_p/2$ .

If we define the conversion ratio  $M = V_{out}/V_{in}$ , the normalized load current  $J = I_{out}R_0/V_{in}$ , and the effective quality factor as  $Q_e = R_0/R_e$ , then the elliptical output characteristic can be written

$$\left(\frac{M}{a}\right)^2 + \left(\frac{J}{b}\right)^2 = 1 \quad (22.84)$$

and the control characteristic can be written



**Fig. 22.44** Typical control plane characteristic of the LLC inverter, as predicted by the CCM sinusoidal approximation

**Table 22.1** Branch reactances of basic tank networks

Tank	Series branch reactance $X_s$	Shunt branch reactance $X_p$
Series	$\omega L - \frac{1}{\omega C}$	$\infty$
Parallel	$\omega L$	$-\frac{1}{\omega C}$
LCC	$\omega L - \frac{1}{\omega C_s}$	$-\frac{1}{\omega C_p}$
LLC	$\omega L_s - \frac{1}{\omega C}$	$\omega L_p$

$$M = \frac{1}{\sqrt{\frac{1}{a^2} + \left(\frac{Q_e}{b}\right)^2}} \quad (22.85)$$

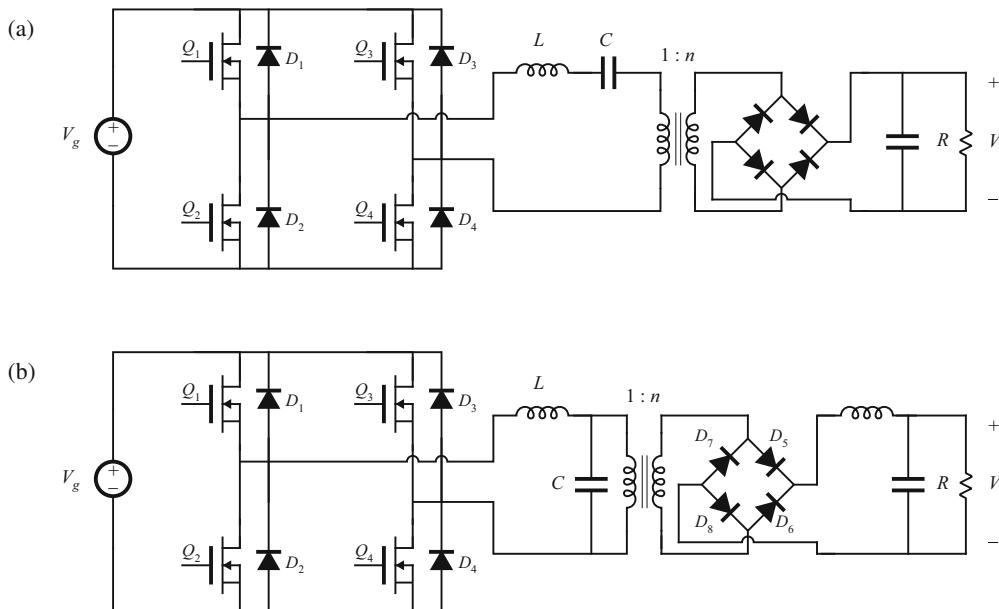
where the parameters  $a$  and  $b$  are given by

$$\begin{aligned} a &= \|H_{\infty}(\omega)\| = \frac{|X_p|}{|X_p + X_s|} \\ b &= \frac{\|H_{\infty}(\omega)\| R_0}{\|Z_{o0}(\omega)\|} = \frac{R_0}{|X_s|} \end{aligned} \quad (22.86)$$

The above equations describe the solutions of all of the inverters of Fig. 22.1, based on the sinusoidal approximation. For the series tank,  $a = 1$ .

## 22.5 Exact Characteristics of the Series and Parallel Resonant Converters

The exact steady-state behavior of resonant converters can be determined via methods such as state plane analysis. A detailed analysis of resonant dc–dc converters is beyond the scope of this book. However, the exact steady-state characteristics of ideal series [272, 306–313] and parallel [299, 315–318] resonant dc–dc converters (Fig. 22.45) are summarized in this section. Small-signal ac modeling has also been described in the literature; several relevant papers are [320–323].



**Fig. 22.45** Transformer-isolated resonant dc–dc converters: (a) series resonant converter, (b) parallel resonant converter

### 22.5.1 Series Resonant Converter

At a given switching frequency, the series resonant dc–dc converter can operate in one continuous conduction mode, and possibly in several discontinuous conduction modes. The mode index  $k$  is defined as the integer that satisfies

$$\frac{f_0}{k+1} < f_s < \frac{f_0}{k} \quad \text{or} \quad \frac{1}{k+1} < F < \frac{1}{k} \quad (22.87)$$

where  $F = f_s/f_0$  is the normalized switching frequency. The subharmonic number  $\xi$  is defined as

$$\xi = k + \frac{1 + (-1)^k}{2} \quad (22.88)$$

Values of  $k$  and  $\xi$  as functions of  $f_s$  are summarized in Fig. 22.46a. The subharmonic number  $\xi$  denotes the dominant harmonic that excites the tank resonance. When the converter is heavily loaded, it operates in type  $k$  continuous conduction mode. As the load is reduced (i.e., as the load resistance  $R$  is increased), the converter enters the type  $k$  discontinuous conduction mode. Further reducing the load causes the converter to enter the type  $(k - 1)$  DCM, type  $(k - 2)$  DCM, . . . , type 1 DCM. There is no type 0 DCM, and hence when the converter operates above resonance, only the type 0 continuous conduction mode is possible.

In the type  $k$  continuous conduction mode, the series resonant converter exhibits elliptical output characteristics, given by

$$M^2 \xi^2 \sin^2\left(\frac{\gamma}{2}\right) + \frac{1}{\xi^2} \left(\frac{J\gamma}{2} + (-1)^k\right)^2 \cos^2\left(\frac{\gamma}{2}\right) = 1 \quad (22.89)$$

For the transformer-isolated converters of Fig. 22.45,  $M$  and  $J$  are related to the load voltage  $V$  and load current  $I$  according to

$$M = \frac{V}{nV_g} \quad J = \frac{InR_0}{V_g} \quad (22.90)$$

Again,  $R_0$  is the tank characteristic impedance, referred to the transformer primary side. The quantity  $\gamma$  is the angular length of one-half of the switching period:

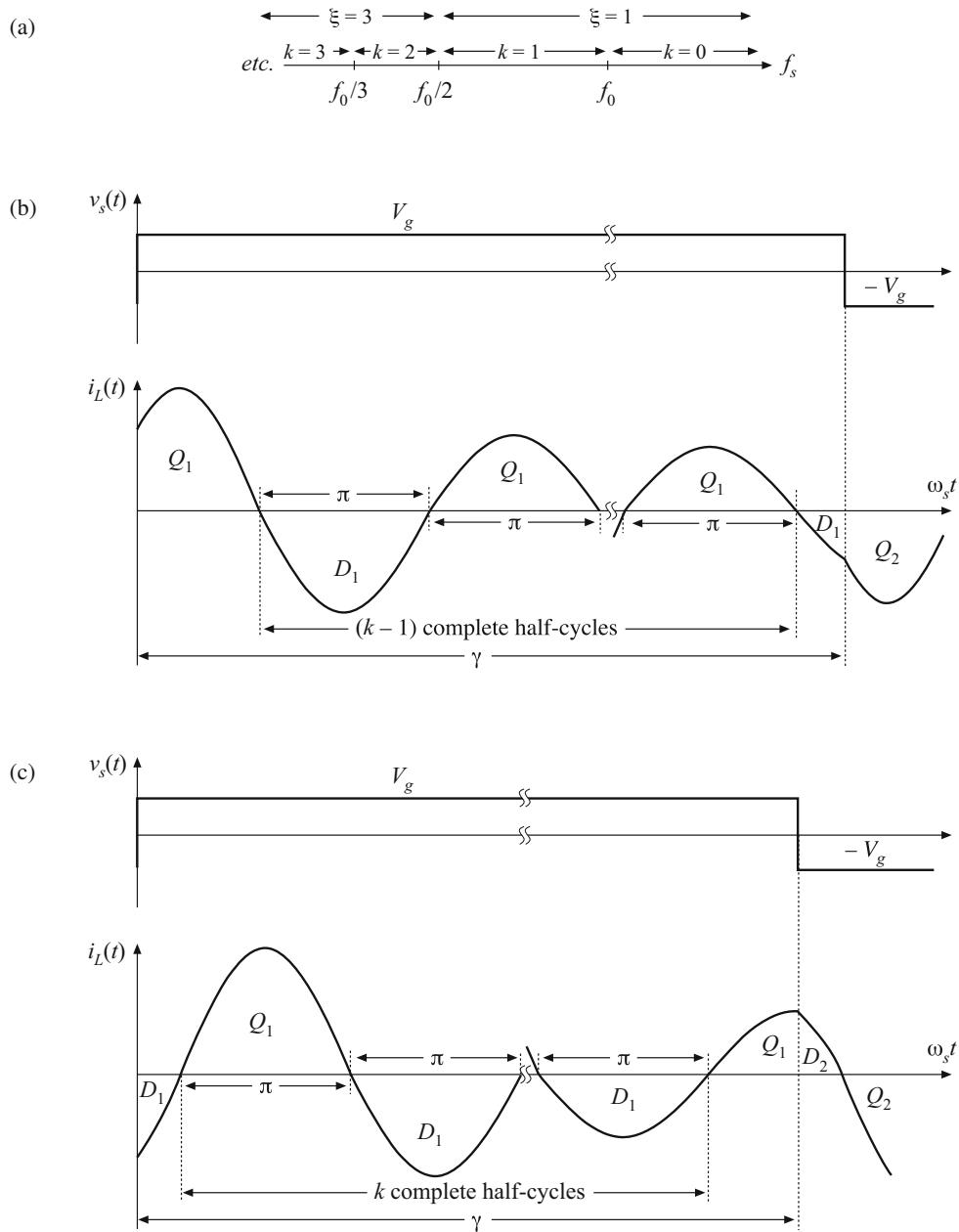
$$\gamma = \frac{\omega_0 T_s}{2} = \frac{\pi}{F} \quad (22.91)$$

Equation (22.89) is valid only for  $k$  satisfying Eq. (22.87). It predicts that the voltage conversion ratio  $M$  is restricted to the range

$$0 \leq M \leq \frac{1}{\xi} \quad (22.92)$$

This is consistent with Eq. (22.21).

Typical CCM tank current waveforms are illustrated in Fig. 22.46. When  $k$  is even, the tank inductor current is initially negative. In consequence, the switch network antiparallel diodes conduct first, for a fraction of a half resonant cycle. If  $k$  is odd, then each half-switching period is initiated by conduction of the switch network transistors. In either case, this is followed by  $(\xi - 1)$  complete tank half-cycles of ringing. The half-switching period is then concluded by



**Fig. 22.46** Continuous conduction modes of the series resonant converter: (a) switching frequency ranges over which various mode indices  $k$  and subharmonic numbers  $\xi$  occur; (b) tank inductor current waveform, type  $k$  CCM, for odd  $k$ ; (c) tank inductor current waveform, type  $k$  CCM, for even  $k$

a subinterval shorter than one complete resonant half-cycle, in which the device that did not initially conduct is on. The next half-switching period then begins, and is symmetrical.

The steady-state control plane characteristic can be found for a resistive load  $R$  obeying  $V = IR$ , by substitution of the normalized relation  $J = MQ$  into Eq. (22.89), where  $Q = n^2 R_0 / R$ . Use of the quadratic formula and some algebraic manipulations allows solution for  $M$ , as a function of load (via  $Q$ ) and switching frequency (via  $\gamma$ ):

$$M = \frac{\left(\frac{Q\gamma}{2}\right)}{\xi^4 \tan^2\left(\frac{\gamma}{2}\right) + \left(\frac{Q\gamma}{2}\right)^2} \left[ (-1)^{k+1} + \sqrt{1 + \frac{\left[\xi^2 - \cos^2\left(\frac{\gamma}{2}\right)\right]\left[\xi^4 \tan^2\left(\frac{\gamma}{2}\right) + \left(\frac{Q\gamma}{2}\right)^2\right]}{\left(\frac{Q\gamma}{2}\right)^2 \cos^2\left(\frac{\gamma}{2}\right)}} \right] \quad (22.93)$$

This is the closed-form relationship between the conversion ratio  $M$  and the switching frequency, for a resistive load. It is valid for any continuous conduction mode  $k$ .

The type  $k$  discontinuous conduction modes, for  $k$  odd, occur over the frequency range

$$f_s < \frac{f_0}{k} \quad (22.94)$$

In these modes, the output voltage is independent of both load current and switching frequency, and is described by

$$M = \frac{1}{k} \quad (22.95)$$

The type  $k$  discontinuous conduction mode, for odd  $k$ , occurs over the range of load currents given by

$$\frac{2(k+1)}{\gamma} > J > \frac{2(k-1)}{\gamma} \quad (22.96)$$

In the odd discontinuous conduction modes, the tank current rings for  $k$  complete resonant half-cycles. All four output bridge rectifier diodes then become reverse-biased, and the tank current remains at zero until the next switching half-period begins, as illustrated in Fig. 22.51. Series resonant converters are not normally purposely designed to operate in odd discontinuous conduction modes, because the output voltage is not controllable. Nonetheless, when the load is removed with  $f_s < f_0$ , the series resonant converter operates in  $k = 1$  DCM with  $M = 1$ .

The type  $k$  discontinuous conduction mode, for  $k$  even, also occurs over the frequency range

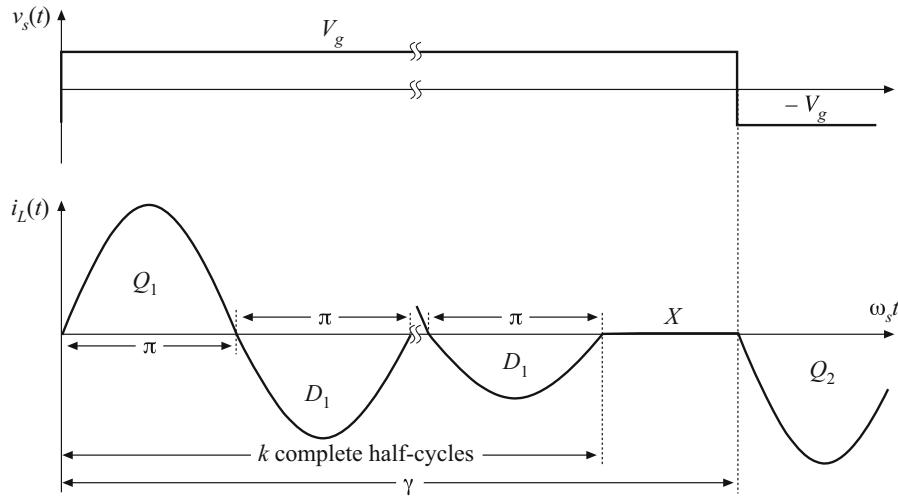
$$f_s < \frac{f_0}{k} \quad (22.97)$$

Even discontinuous conduction modes exhibit current source characteristics, in which the load current is a function of switching frequency and input voltage, but not of the load voltage. The output relationship is

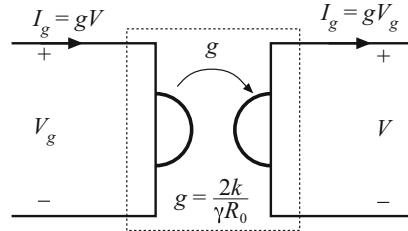
$$J = \frac{2k}{\gamma} \quad (22.98)$$

Operation in this mode occurs for

$$\frac{1}{k-1} > M > \frac{1}{k+1} \quad (22.99)$$



**Fig. 22.47** Tank inductor current waveform, type  $k$  DCM, for even  $k$

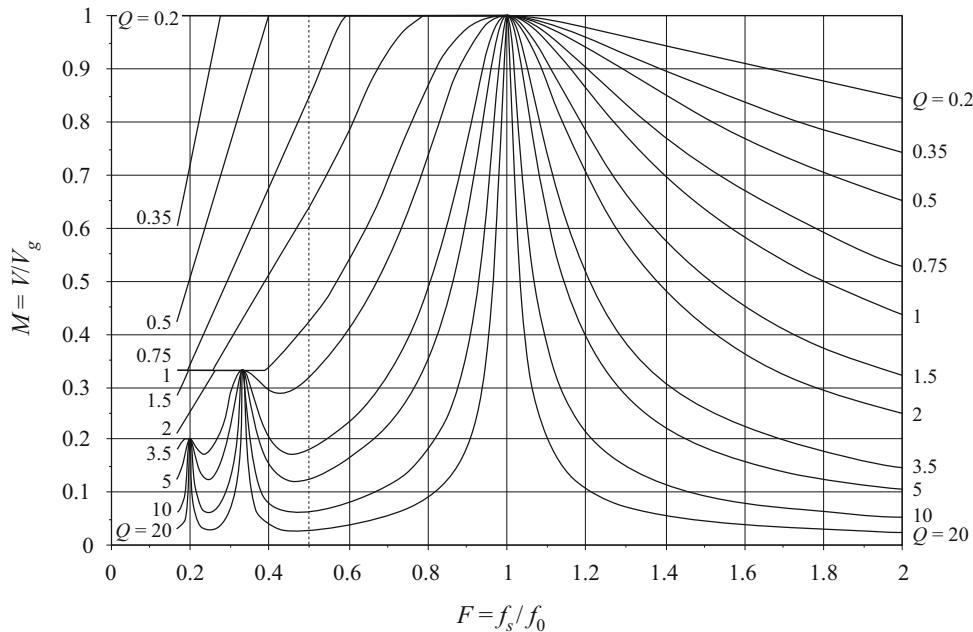


**Fig. 22.48** Steady-state equivalent circuit model for an even discontinuous conduction mode: an effective gyrator. The converter exhibits current source characteristics

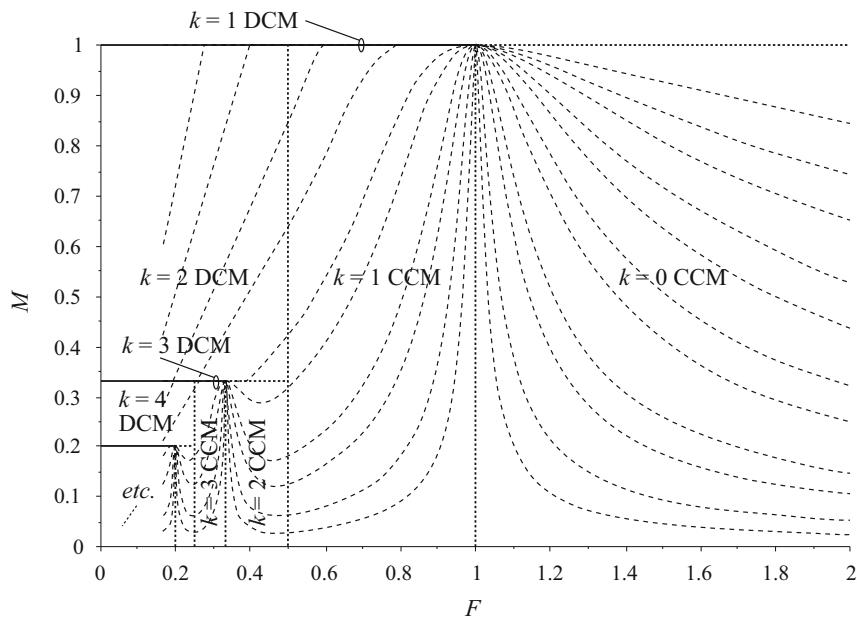
In the even discontinuous conduction modes, the tank current rings for  $k$  complete resonant half-cycles during each switching half-period. All four output bridge then become reverse-biased, and the tank current remains at zero until the next switching half-period is initiated. Tank current waveforms are illustrated in Fig. 22.47 for even DCM.

The series resonant converter possesses some unusual properties when operated in an even discontinuous conduction mode. A dc equivalent circuit is given in Fig. 22.48, consisting of a gyrator with gyration conductance  $g = 2k/gn^2R_0$ . The gyrator has the property of transforming circuits into their dual networks; in the typical dc–dc converter application, the input voltage source  $V_g$  is effectively transformed into its dual, an output current source of value  $gV_g$ . Series resonant converters have been purposely designed to operate in the  $k = 2$  DCM, at power levels of several tens of kW.

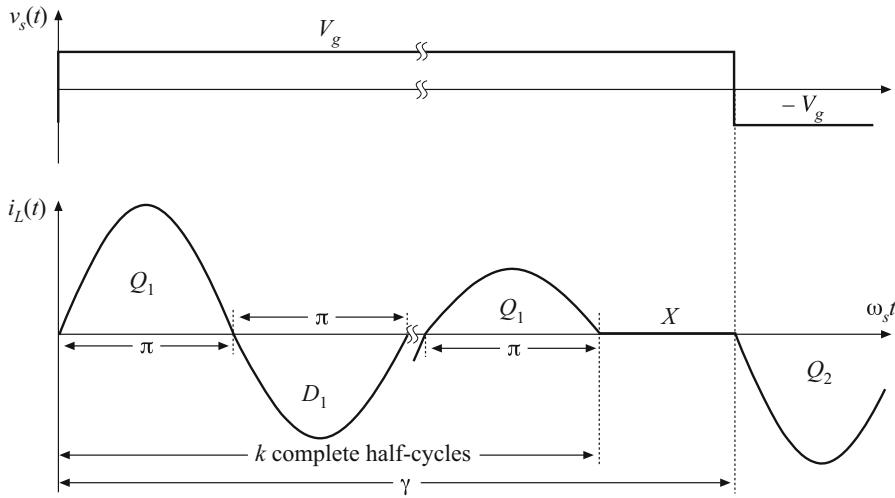
The complete control plane characteristics can now be plotted using Eqs. (22.87)–(22.99). The result is shown in Fig. 22.49, and the mode boundaries are explicitly diagrammed in Fig. 22.50. It can be seen that, for operation above resonance, the only possible operating mode is the  $k = 0$  CCM, and that the output voltage decreases monotonically with increasing switch-



**Fig. 22.49** Complete control plane characteristics of the series resonant converter, for  $0.2 \leq F \leq 2$



**Fig. 22.50** Continuous and discontinuous conduction mode boundaries



**Fig. 22.51** Tank inductor current waveform, type  $k$  DCM, for odd  $k$

ing frequency. Reduction in load current (or increase in load resistance, which decreases  $Q$ ) causes the output voltage to increase. A number of successful designs that operate above resonance and utilize zero-voltage switching have been documented in the literature [300, 314].

Operation below resonance is complicated by the presence of subharmonic and discontinuous conduction modes. The  $k = 1$  CCM and  $k = 2$  DCM are well behaved, in that the output voltage increases monotonically with increasing switching frequency. Increase of the load current again causes the output voltage to decrease. Successful designs that operate in these modes and employ zero-current switching are numerous. However, operation in the higher-order modes ( $k = 2$  CCM,  $k = 4$  DCM, etc.) is normally avoided.

Given  $F$  and  $Q$ , the operating mode can be evaluated directly, using the following algorithm. First, the continuous conduction mode  $k$  corresponding to operation at frequency  $F$  with heavy loading is found:

$$k = \text{INT}\left(\frac{1}{F}\right) \quad (22.100)$$

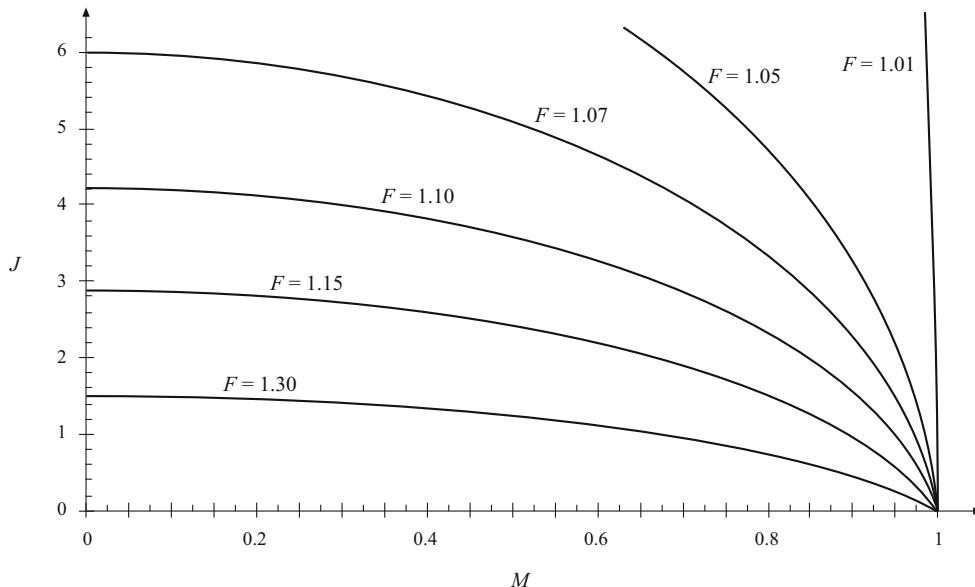
where  $\text{INT}(x)$  denotes the integer part of  $x$ . Next, the quantity  $k_1$  is determined:

$$k_1 = \text{INT}\left(\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{Q\pi}{2F}}\right) \quad (22.101)$$

The converter operates in type  $k$  CCM provided that:

$$k_1 > k \quad (22.102)$$

Otherwise, the converter operates in type  $k_1$  DCM. A simple algorithm can therefore be defined, in which the conversion ratio  $M$  is computed for a given  $F$  and  $Q$ . First, Eqs. (22.100) to (22.102) are evaluated, to determine the operating mode. Then, the appropriate equation (22.93), (22.95), or (22.98) is evaluated to find  $M$ .



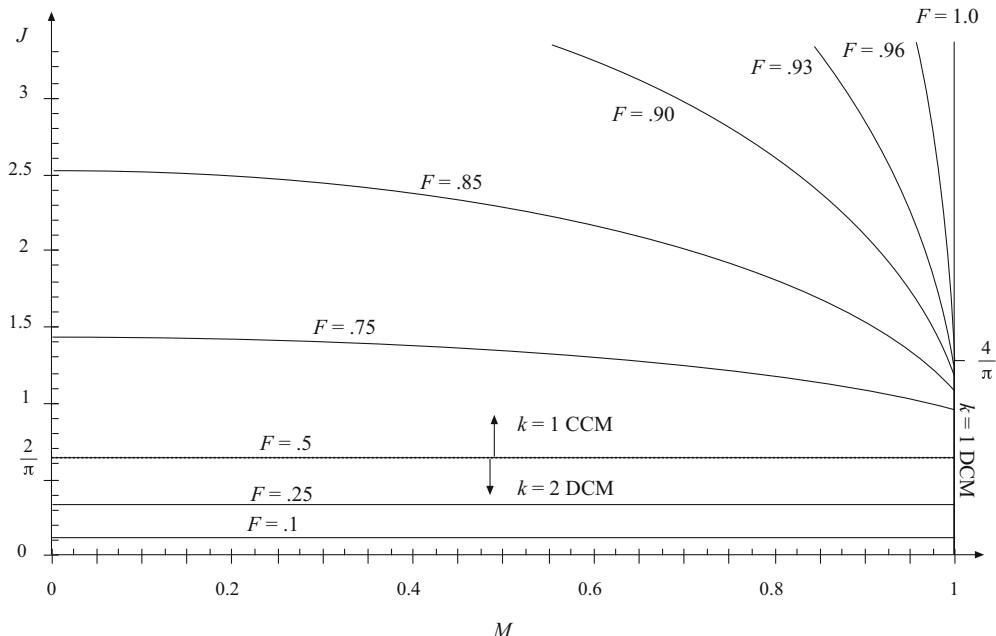
**Fig. 22.52** Output characteristics,  $k = 0$  CCM (above resonance)

Output  $I - V$  plane characteristics for the  $k = 0$  CCM, plotted using Eq. (22.89), are shown in Fig. 22.52. The constant-frequency curves are elliptical, and all pass through the point  $M = 1$ ,  $J = 0$ . For a given switching frequency, the operating point is given by the intersection of the elliptical converter output characteristic with the load  $I - V$  characteristic.

Output plane characteristics that combine the  $k = 1$  CCM,  $k = 1$  DCM, and  $k = 2$  DCM are shown in Fig. 22.53. These were plotted using Eqs. (22.89), (22.95), and (22.98). These curves were plotted with the assumption that the transistors are allowed to conduct no longer than one tank half-cycle during each switching half-period; this eliminates subharmonic modes and causes the converter to operate in  $k = 2$  or  $k = 1$  DCM whenever  $f_s < 0.5f_0$ . It can be seen that the constant-frequency curves are elliptical in the continuous conduction mode, vertical (voltage source characteristic) in the  $k = 1$  DCM, and horizontal (current source characteristic) in the  $k = 2$  DCM.

### 22.5.2 Parallel Resonant Converter

For operation in the frequency range  $0.5f_0 < f_s < \infty$ , the parallel resonant dc–dc converter exhibits one continuous conduction mode and one discontinuous conduction mode. Typical CCM switch voltage  $v_s(t)$ , tank inductor current  $i_L(t)$ , and tank capacitor voltage  $v_C(t)$  waveforms are illustrated in Fig. 22.54. The CCM converter output characteristics are given by



**Fig. 22.53** Output characteristics,  $k = 1$  CCM,  $k = 1$  DCM, and  $k = 2$  DCM (below resonance)

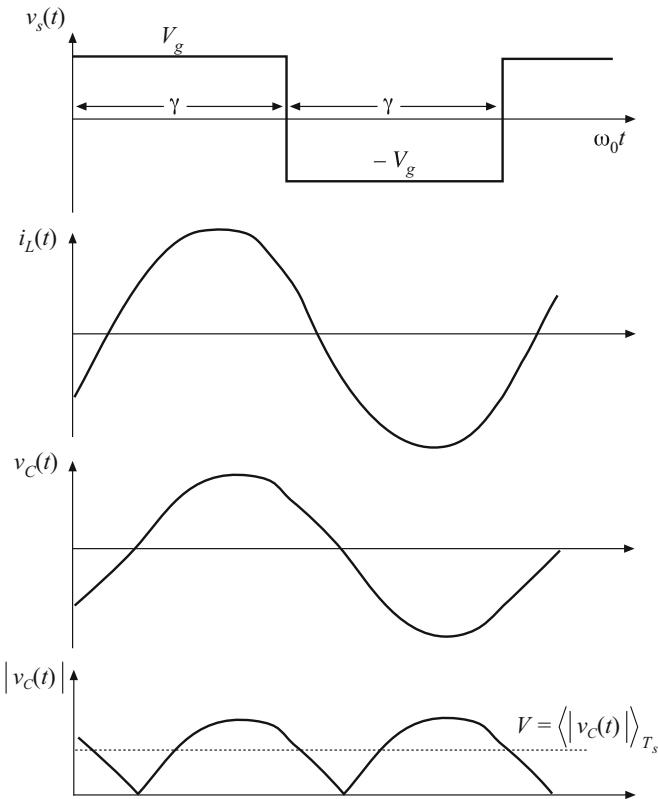
$$M = \left( \frac{2}{\gamma} \right) \left( \varphi - \frac{\sin(\varphi)}{\cos\left(\frac{\gamma}{2}\right)} \right) \quad (22.103)$$

$$\varphi = \begin{cases} -\cos^{-1} \left( \cos\left(\frac{\gamma}{2}\right) + J \sin\left(\frac{\gamma}{2}\right) \right) & \text{for } 0 < \gamma < \pi \text{ (above resonance)} \\ +\cos^{-1} \left( \cos\left(\frac{\gamma}{2}\right) + J \sin\left(\frac{\gamma}{2}\right) \right) & \text{for } \pi < \gamma < 2\pi \text{ (below resonance)} \end{cases} \quad (22.104)$$

and where  $M$ ,  $J$ , and  $\gamma$  are again defined as in Eqs. (22.90) and (22.91). Given the normalized load current  $J$  and the half-switching-period-angle  $\gamma$ , one can evaluate Eq. (22.104) to find  $\varphi$ , and then evaluate Eq. (22.103) to find the converter voltage conversion ratio  $M$ . In other words, the output voltage can be found for a given load current and switching frequency, without need for computer iteration.

A discontinuous conduction mode mechanism occurs in the parallel resonant converter which is the dual of the discontinuous conduction mode mechanism of the series resonant converter. In this mode, a discontinuous subinterval occurs in which all four output bridge rectifier diodes are forward-biased, and the tank capacitor voltage remains at zero. This mode occurs both above and below resonance when the converter is heavily loaded. Typical DCM tank capacitor voltage and inductor current waveforms are illustrated in Fig. 22.55. The condition for operation in the discontinuous conduction mode is

$$\begin{aligned} J > J_{crit}(\gamma) &\quad \text{for DCM} \\ J < J_{crit}(\gamma) &\quad \text{for CCM} \end{aligned} \quad (22.105)$$



**Fig. 22.54** Typical waveforms of the parallel resonant converter, operating in the continuous conduction mode

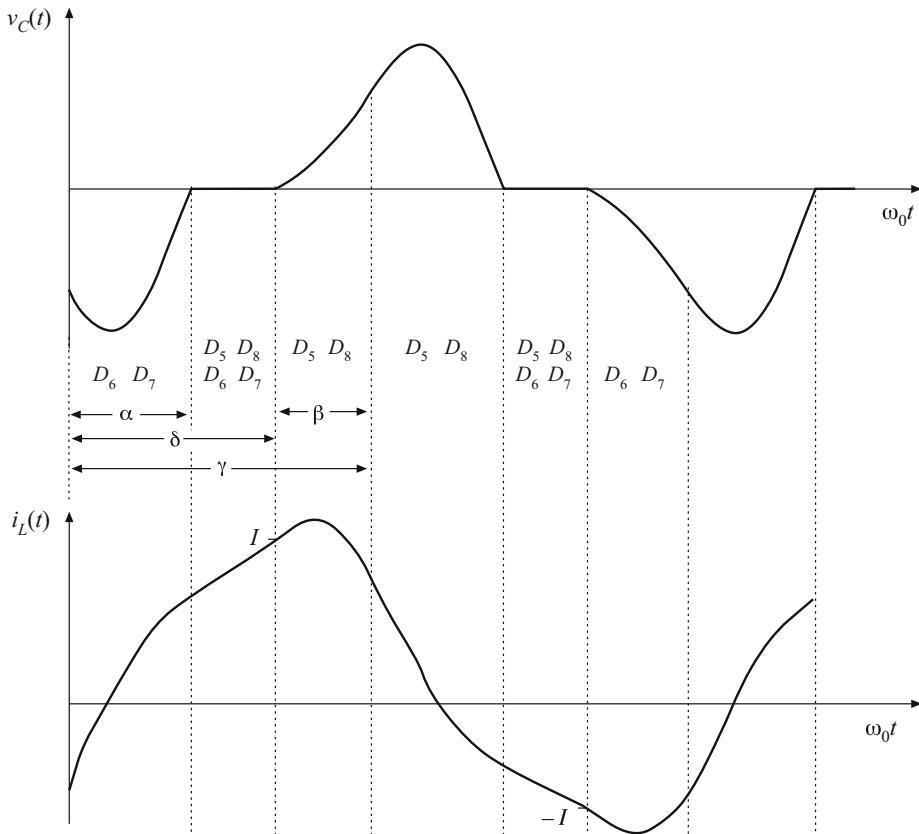
where

$$J_{crit}(\gamma) = -\frac{1}{2} \sin(\gamma) + \sqrt{\sin^2\left(\frac{\gamma}{2}\right) + \frac{1}{4} \sin^2(\gamma)} \quad (22.106)$$

The discontinuous conduction mode is described by the following set of equations:

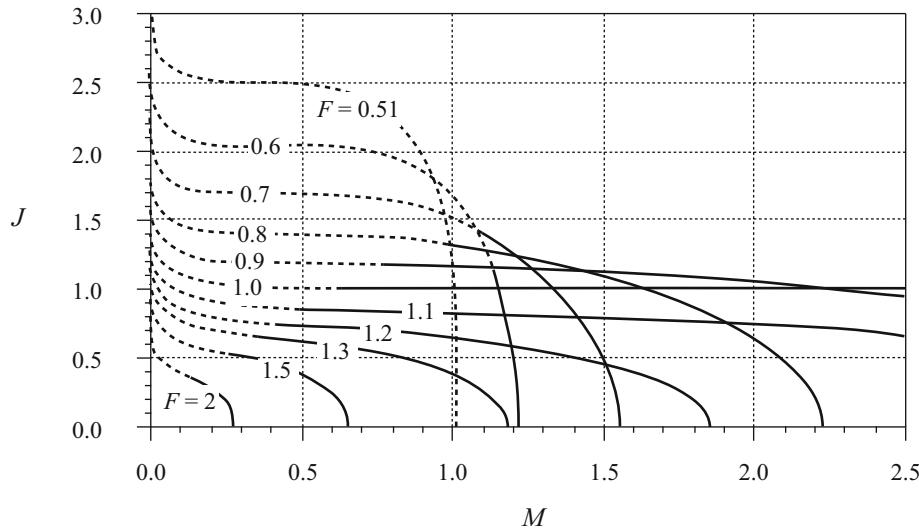
$$\begin{aligned} M_{C0} &= 1 - \cos(\beta) \\ J_{L0} &= J + \sin(\beta) \\ \cos(\alpha + \beta) - 2 \cos(\alpha) &= -1 \\ -\sin(\alpha + \beta) + 2 \sin(\alpha) + (\delta - \alpha) &= 2J \\ \beta + \delta &= \gamma \\ M &= 1 + \left(\frac{2}{\gamma}\right)(J - \delta) \end{aligned} \quad (22.107)$$

Unfortunately, the solution to this set of equations is not known in closed form, because of the mixture of linear and trigonometric terms. In consequence, the equations must be solved

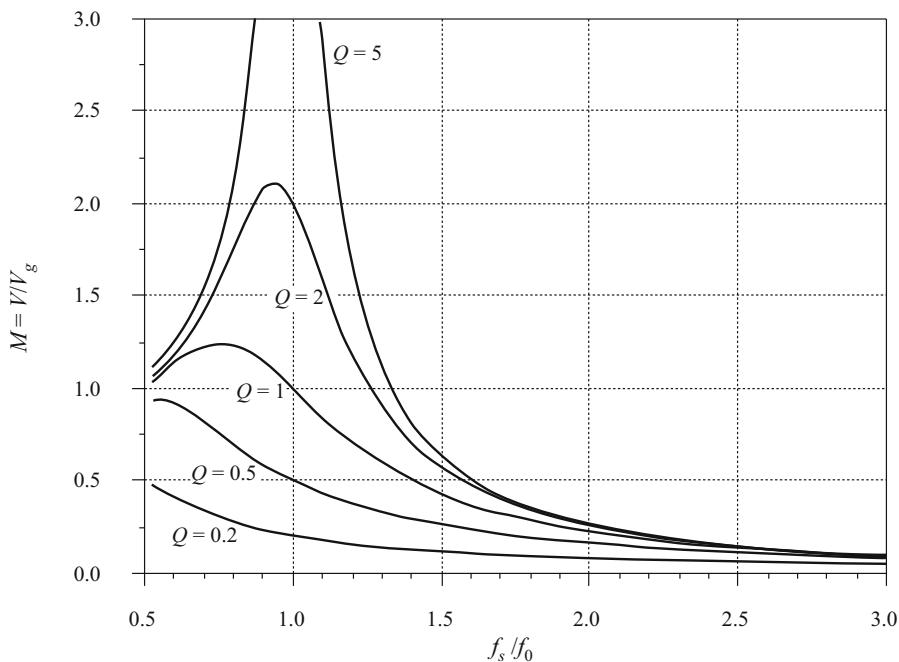


**Fig. 22.55** Typical waveforms of the parallel resonant converter, operating in the discontinuous conduction mode

iteratively. For a given  $\gamma$  and  $J$ , a computer is used to iteratively find the angles  $\alpha$ ,  $\beta$ , and  $\delta$ .  $M$  is then evaluated, and the output plane characteristics can be plotted. The result is given in Fig. 22.56. The dashed lines are the DCM solutions, and the solid lines are the valid CCM solutions. Figure 22.56 describes the complete dc behavior of the ideal parallel resonant converter for all switching frequencies above  $0.5f_0$ . For given values of normalized switching frequency  $F = f_s/f_0 = \pi/\gamma$ , the relationship between the normalized output current  $J$  and the normalized output voltage  $M$  is approximately elliptical. At resonance ( $F = 1$ ), the CCM ellipse degenerates to the horizontal line  $J = 1$ , and the converter exhibits current source characteristics. Above resonance, the converter can both step-up the voltage ( $M > 1$ ) and step-down the voltage ( $M < 1$ ). The normalized load current is then restricted to  $J < 1$ , corresponding to  $I < V_g/nR_0$ . For a given switching frequency greater than the resonant frequency, the actual limit on maximum load current is even more restrictive than this limit. Below resonance, the converter can also step-up and step-down the voltage. Normalized load currents  $J$  greater than one are also obtainable, depending on  $M$  and  $F$ . However, no solutions occur when  $M$  and  $J$  are simultaneously large.



**Fig. 22.56** Exact output characteristics of the parallel resonant converter, for  $F > 0.5$ . Solid curves: CCM, dashed curves: DCM



**Fig. 22.57** Exact control characteristics of the parallel resonant converter, with a resistive load. Both CCM and DCM operation is included, for  $0.5 \leq F \leq 3$

In Fig. 22.57, the control plane characteristics are plotted for a resistive load. The parameter  $Q$  is defined for the parallel resonant converter as  $Q = R/n^2R_0$ . The normalized load current is then given by  $J = M/Q$ .

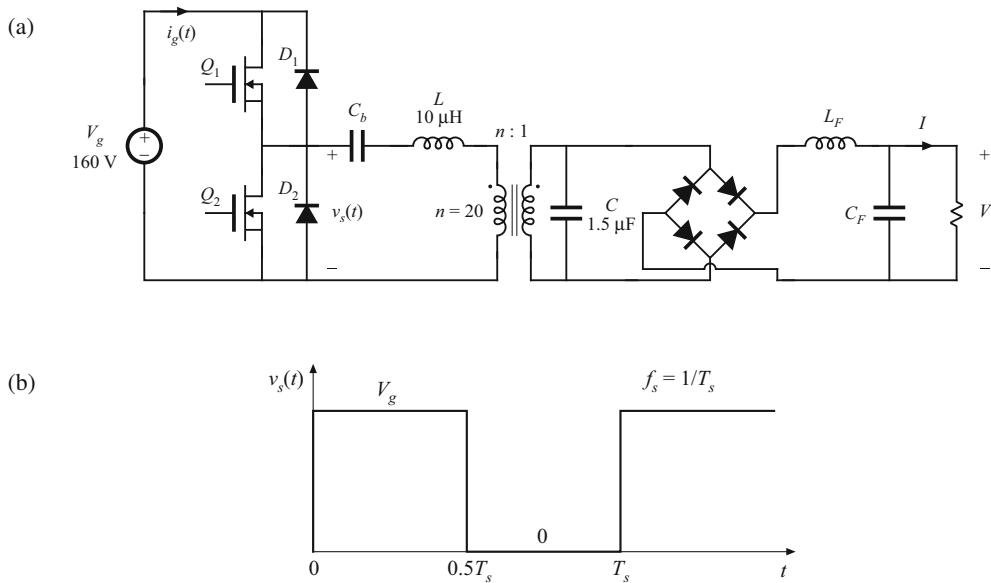
## 22.6 Summary of Key Points

1. The sinusoidal approximation allows a great deal of insight to be gained into the operation of resonant inverters and dc–dc converters. The voltage conversion ratio of dc–dc resonant converters can be directly related to the tank network transfer function. Other important converter properties, such as the output characteristics, dependence (or lack thereof) of transistor current on load current, and zero-voltage- and zero-current-switching transitions, can also be understood using this approximation. The approximation is accurate provided that the effective  $Q$ -factor is sufficiently large, and provided that the switching frequency is sufficiently close to resonance.
2. Simple equivalent circuits are derived, which represent the fundamental components of the tank network waveforms, and the dc components of the dc terminal waveforms.
3. Exact solutions of the ideal dc–dc series and parallel resonant converters are listed here as well. These solutions correctly predict the conversion ratios, for operation not only in the fundamental continuous conduction mode, but in discontinuous and subharmonic modes as well.
4. Zero-voltage switching mitigates the switching loss caused by diode recovered charge and semiconductor device output capacitances. When the objective is to minimize switching loss and EMI, it is preferable to operate each MOSFET and diode with zero-voltage switching.
5. Zero-current switching leads to natural commutation of SCRs, and can also mitigate the switching loss due to current tailing in IGBTs.
6. The input impedance magnitude  $\|Z_i\|$ , and hence also the transistor current magnitude, are monotonic functions of the load resistance  $R$ . The dependence of the transistor conduction loss on the load current can be easily understood by simply plotting  $\|Z_i\|$  in the limiting cases as  $R \rightarrow \infty$  and as  $R \rightarrow 0$ , or  $\|Z_{i\infty}\|$  and  $\|Z_{i0}\|$ .
7. The ZVS/ZCS boundary is also a simple function of  $Z_{i\infty}$  and  $Z_{i0}$ . If ZVS occurs at open-circuit and at short-circuit, then ZVS occurs for all loads. If ZVS occurs at short-circuit, and ZCS occurs at open-circuit, then ZVS is obtained at matched load provided that  $\|Z_{i\infty}\| > \|Z_{i0}\|$ .
8. The output characteristics of all resonant inverters considered here are elliptical, and are described completely by the open-circuit transfer function magnitude  $\|H_\infty\|$ , and the output impedance  $\|Z_{o0}\|$ . These quantities can be chosen to match the output characteristics to the application requirements.

## PROBLEMS

### 22.1 Analysis of a half-bridge dc–dc parallel resonant converter, operated above resonance.

In Fig. 22.58, the elements  $C_b$ ,  $L_F$ , and  $C_F$  are large in value, and have negligible switching ripple. You may assume that all elements are ideal. You may use the sinusoidal approximation as appropriate.



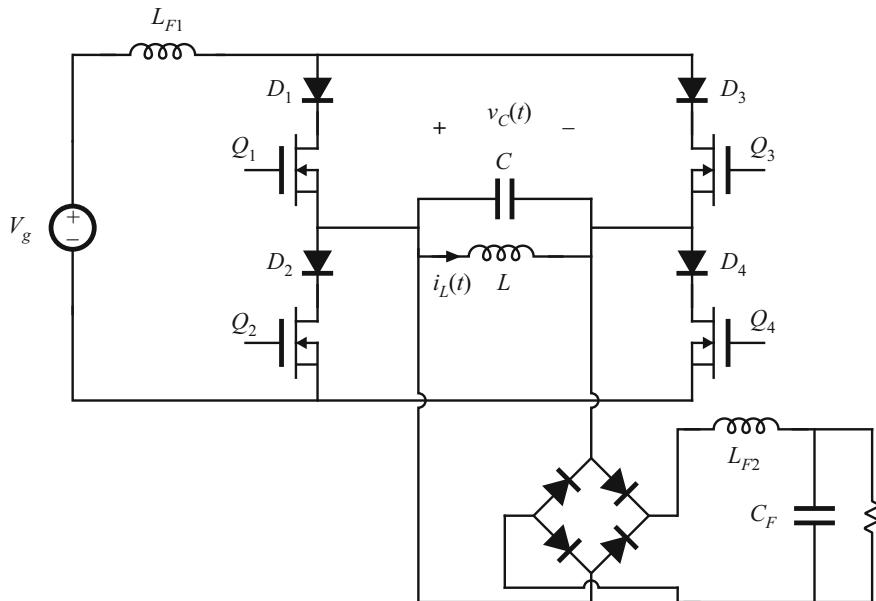
**Fig. 22.58** Half-bridge parallel resonant converter of Problem 22.1: (a) schematic, (b) switch voltage waveform

- (a) Sketch the waveform of the current  $i_g(t)$ .
  - (b) Construct an equivalent circuit for this converter, similar to Fig. 22.22, which models the fundamental components of the tank waveforms and the dc components of the converter input current and output voltage. Clearly label the values and/or give expressions for all elements in your model, as appropriate.
  - (c) Solve your model to derive an expression for the conversion ratio  $V/V_g = M(F, Q_e, n)$ . At rated (maximum) load, this converter produces  $I = 20 \text{ A}$  at  $V = 3.3 \text{ V}$ .
  - (d) What is the converter switching frequency  $f_s$  at rated load?
  - (e) What is the magnitude of the peak transistor current at rated load?  
At minimum load, the converter produces  $I = 2 \text{ A}$  at  $V = 3.3 \text{ V}$ .
  - (f) What is the converter switching frequency  $f_s$  at minimum load?
  - (g) What is the magnitude of the peak transistor current at minimum load? Compare with your answer from part (e)—what happens to the conduction loss and efficiency at minimum load?
- 22.2** A dc–dc resonant converter contains an LCC tank network (Fig. 22.1d), with an output filter containing a filter inductor as in the parallel resonant dc–dc converter.
- (a) Sketch an equivalent circuit model for this converter, based on the approximate sinusoidal analysis method of Sect. 22.1. Give expressions for all elements in your model.
  - (b) Solve your model, to derive an expression for the conversion ratio  $M = V/V_g$ . Express  $M$  as a function of  $F = f_s/f_\infty$ ,  $Q_e = R_e/R_0$ , and  $n = C_s/C_p$ , where  $f_\infty$  is defined as in Eq. (22.50) and  $R_0$  is

$$R_0 = \sqrt{\frac{L(C_s + C_p)}{C_s C_p}}$$

- (c) Plot  $M$  vs.  $F$ , for  $n = 1$  and  $Q_e = 1, 2$ , and 5.  
 (d) Plot  $M$  vs.  $F$ , for  $n = 0.25$  and  $Q_e = 1, 2$ , and 5.

**22.3** Dual of the series resonant converter. In the converter illustrated in Fig. 22.59,  $L_{F1}$ ,  $L_{F2}$ , and  $C_F$  are large filter elements, whose switching ripples are small.  $L$  and  $C$  are tank elements, whose waveforms  $i_L(t)$  and  $v_C(t)$  are nearly sinusoidal.



**Fig. 22.59** Dual of the series resonant converter, Problem 22.3

- (a) Using the sinusoidal approximation method, develop equivalent circuit models for the switch network, tank network, and rectifier network.  
 (b) Sketch a Bode diagram of the parallel  $LC$  parallel tank impedance.  
 (c) Solve your model. Find an analytical solution for the converter voltage conversion ratio  $M = V/V_g$ , as a function of the effective  $Q_e$  and the normalized switching frequency  $F = f_s/f_0$ . Sketch  $M$  vs.  $F$ .  
 (d) What can you say about the validity of the sinusoidal approximation for this converter? Which parts of your  $M$  vs.  $F$  plot of part (c) are valid and accurate?

**22.4** The converter of Problem 22.3 operates below resonance.

- (a) Sketch the waveform  $v_C(t)$ . For each subinterval, label: (i) which of the diodes  $D_1$  to  $D_4$  and transistors  $Q_1$  to  $Q_4$  conduct current, and (ii) which devices block voltage.  
 (b) Does the reverse recovery process of diodes  $D_1$  to  $D_4$  lead to switching loss? Do the output capacitances of transistors  $Q_1$  to  $Q_4$  lead to switching loss?

- (c) Repeat parts (a) and (b) for operation above resonance.
- 22.5** A parallel resonant converter operates with a dc input voltage of  $V_g = 270$  V. The converter supplies 5 V to a dc load. The dc load power varies over the range 20 W–200 W. It is desired to operate the power transistors with zero-voltage switching. The tank element values are  $L = 57 \mu\text{H}$ ,  $C_p = 0.9 \text{ nF}$ , referred to the transformer primary. The parallel resonant tank network contains an isolation transformer having a turns ratio of 52:1.
- Define  $F$  as in Eq. (22.19). Derive an expression for  $F$ , as a function of  $M$  and  $Q_e$ .
  - Determine the switching frequency, peak transistor current, and peak tank capacitor voltage at the maximum load power operating point.
  - Determine the switching frequency, peak transistor current, and peak tank capacitor voltage at the minimum load power operating point.
- 22.6** In a certain resonant inverter application, the dc input voltage is  $V_g = 320$  V. The inverter must produce an approximately sinusoidal output voltage having a frequency of 200 kHz. Under no load (output opencircuit) conditions, the inverter should produce a peak-to-peak output voltage of 1500 V. The nominal resistive operating point is 200 Vrms applied to  $100 \Omega$ . A nonisolated LCC inverter is employed. It is desired that the inverter operate with zero-voltage switching, at least for load resistances less than  $200 \Omega$ .
- Derive expressions for the output open-circuit voltage  $V_{oc}$  and short-circuit current  $I_{sc}$  of the LCC inverter. Express your results as functions of  $F = f_s/f_\infty$ ,  $V_g$ ,  $R_\infty = L/C_s||C_p$  and  $n = C_s/C_p$ . The open-circuit resonant frequency  $f_\infty$  is defined in Eq. (22.50).
  - To meet the given specifications, how should the short-circuit current  $I_{sc}$  be chosen?
  - Specify tank element values that meet the specifications.
  - Under what conditions does your design operate with zero-voltage switching?
  - Compute the peak transistor current under no-load and short-circuit conditions.
- 22.7** A series resonant dc–dc converter operates with a dc input voltage of  $V_g = 550$  V. The converter supplies 30 kW to a load. The dc load power varies over the range 5 kW–25 kW. It is desired to operate the power transistors with zero-voltage switching. The maximum feasible switching frequency is 50 kHz. An isolation transformer having a  $1:n$  turns ratio is connected in series with the tank network. The peak tank capacitor voltage should be no greater than 2000 V, referred to the primary.
- Derive expressions for the peak tank capacitor voltage and peak tank inductor current.
  - Select values for the tank inductance, tank capacitance, and turns ratio, such that the given specifications are met. Attempt to minimize the peak tank inductor current, while maximizing the worst-case minimum switching frequency.
- 22.8** Figure 22.60 illustrates a full-bridge resonant inverter containing an LLC tank network.
- Sketch the Bode diagrams of the input impedance under short-circuit and open-circuit conditions:  $\|Z_{i0}(j\omega)\|$  and  $\|Z_{i\infty}(j\omega)\|$ . Give analytical expressions for the resonant frequencies and asymptotes.
  - Describe the conditions on switching frequency and load resistance that lead to zero-voltage switching.
  - Derive an expression for the frequency  $f_m$ , where  $\|Z_{i0}\| = \|Z_{i\infty}\|$ .
  - Sketch the Bode plot of  $\|H_\infty(j\omega)\|$ . Label the resonant frequency, and give analytical expressions for the asymptotes.

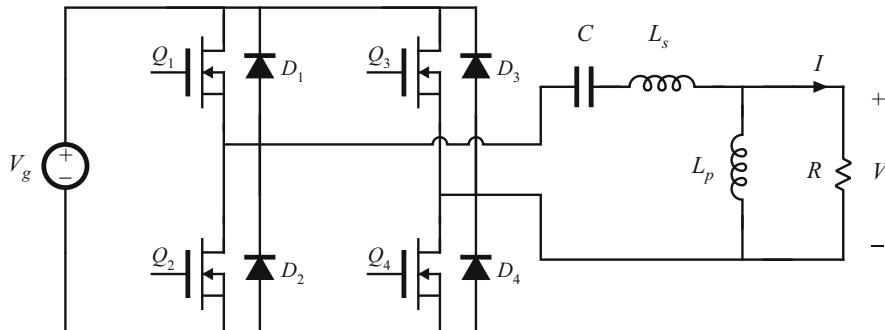


Fig. 22.60 LLC inverter of Problem 22.8

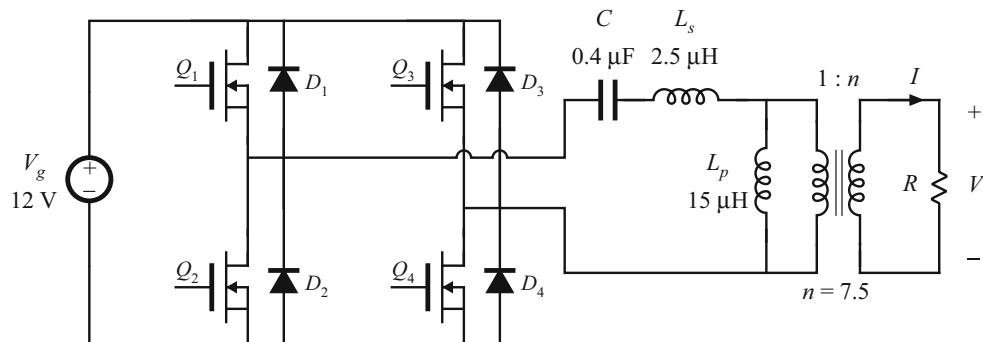


Fig. 22.61 Transformer-isolated LLC inverter, Problem 22.9

**22.9** You are given the LLC inverter circuit of Fig. 22.61. Under nominal conditions, this converter operates at switching frequency  $f_s = 100$  kHz. All elements are ideal.

- Determine the numerical values of the open-circuit peak output voltage  $V_{oc}$  and the short-circuit peak output current  $I_{sc}$ .
- Sketch the elliptical output characteristic. Over what portion of this ellipse does the converter operate with zero-voltage switching? Does it operate with zero-voltage switching at matched load?
- Sketch the Bode plots of  $\|Z_{i\infty}\|$  and  $\|Z_{i0}\|$ , and label the numerical values of  $f_0$ ,  $f_\infty$ ,  $f_m$ , and  $f_s$ .
- What is the numerical value of the peak transistor current when  $R = 0$ ? When  $R \rightarrow \infty$ ?
- The inverter operates with load resistances that can vary between  $500 \Omega$  and an open-circuit. What is the resulting range of output voltage? Does the inverter always operate with zero-voltage switching?

**22.10** It is desired to obtain a converter with current source characteristics. Hence, a series resonant converter is designed for operation in the  $k = 2$  discontinuous conduction mode. The switching frequency is chosen to be  $f_s = 0.225f_0$ , where  $f_0$  is the tank resonant

frequency (consider only open-loop operation). The load  $R$  is a linear resistance which can assume any positive value:  $0 \leq R < \infty$ .

- (a) Plot the output characteristics ( $M$  vs.  $J$ ), for all values of  $R$  in the range  $0 \leq R < \infty$ . Label mode boundaries, evaluate the short-circuit current, and give analytical expressions for the output characteristics.
- (b) Over what range of  $R$  (referred to the tank characteristic impedance  $R_0$ ) does the converter operate as intended, in the  $k = 2$  discontinuous conduction mode?

**22.11** The parallel resonant converter as a single-phase high-quality rectifier. It is desired to utilize a transformer-isolated parallel resonant dc–dc converter in a single-phase low-harmonic rectifier system. By properly varying the converter switching frequency, a near-ideal rectifier system that can be modeled as in Fig. 21.16 is obtained. You may utilize the results of Sect. 22.5.2 to answer this problem. The parallel resonant tank network contains an isolation transformer having a  $1:n$  turns ratio. You may use either approximate graphical analysis or computer iteration to answer parts (b) and (c).

- (a) Plot the normalized input characteristics (normalized input voltage  $m_g = nv_g/v$  vs. normalized input current  $j_g = i_g n R_0/v$ ) of the parallel resonant converter, operated in the continuous conduction mode above resonance. Plot curves for  $F = f_s/f_0 = 1.0, 1.1, 1.2, 1.3, 1.5$ , and  $2.0$ . Compare these characteristics with the desired linear resistive input characteristic  $v_g/i_g = R_{emulated}$ .
- (b) The converter is operated open-loop, with  $F = 1.1$ . The applied normalized input voltage is a rectified sinusoid of unity magnitude:  $m_g(t) = |\sin(\omega t)|$ . Sketch the resulting normalized input current waveform  $j_g(t)$ . Approximately how large is the peak current? The crossover dead time?
- (c) A feedback loop is now added, which regulates the input current to follow the input voltage such that  $i_g(t) = v_g(t)/R_{emulated}$ . You may assume that the feedback loop operates perfectly. For the case  $R_{emulated} = R_0$ , and with the same applied  $m_g(t)$  waveform as in part (b), sketch the switching-frequency waveform for one ac line period [i.e., show how the controller must vary  $F$  to regulate  $i_g(t)$ ]. What is the maximum value of  $F$ ? Note: In practice, the converter would be designed to operate with a smaller peak value of  $j_g$ , so that the switching-frequency variations would be better behaved.
- (d) Choose element values (tank inductance, tank capacitance, and transformer turns ratio) such that the converter of part (c) meets the following specifications:

Ac input voltage 120 Vrms, 60 Hz

Dc output voltage 42 V

Average power 800 W

Maximum switching frequency 200 kHz

Refer the element values to the primary side of the transformer.



## Soft Switching

In addition to the resonant circuits introduced in Chap. 22, there has been much interest in reducing the switching loss of the PWM converters of the previous chapters. Several of the more popular approaches to obtaining *soft switching* in buck, boost, and other converters are discussed in this chapter.

Mechanisms that cause switching loss are discussed in Chap. 4, including diode reverse recovery, semiconductor output capacitances, and IGBT current tailing. Soft switching involves mitigation of one or more of these switching loss mechanisms in a PWM converter. The energy that would otherwise be lost is recovered, and is transferred to the converter source or load. The operation of a semiconductor device, during a given turn-on or turn-off switching transition, can be classified as hard-switched, zero-current switched, or zero-voltage switched. Operation of diodes and transistors with soft switching is examined in Sect. 23.1. In particular, it is preferable to operate diodes with zero-voltage switching at their turn-off transitions, and to operate MOSFETs with zero-voltage switching during their turn-on transitions. However, zero-voltage switching comes at the expense of increased conduction loss, and so the engineer must consider the effect of soft switching on the overall converter efficiency.

*Resonant switch* converters are a broad class of converters in which the PWM switch network of a conventional buck, boost, or other converter is replaced with a switch cell containing resonant elements. These resonant elements are positioned such that the semiconductor devices operate with zero-current or zero-voltage switching, and such that one or more of the switching loss mechanisms is reduced or eliminated. Other soft-switching approaches may employ resonant switching transitions, but otherwise exhibit the approximately rectangular waveforms of hard-switched converters. In any case, the resulting hybrid converter combines the properties of the resonant switching network and the parent hard-switched PWM converter.

Soft-switching converters can exhibit reduced switching loss, at the expense of increased conduction loss. Obtaining zero-voltage or zero-current switching requires that the resonant elements have large ripple; often, these elements are operated in a manner similar to the discontinuous conduction modes of the series or parallel resonant converters. As in other resonant schemes, the objectives of designing such a converter are: (1) to obtain smaller transformer and low-pass filter elements via increase of the switching frequency and/or (2) to reduce the switching loss induced by component nonidealities such as diode stored charge, semiconductor device capacitances, and transformer leakage inductance and winding capacitance.

The resonant switch and soft-switching ideas are quite general, and can be applied to a variety of topologies and applications. A large number of resonant switch networks have been documented in the literature; a few basic approaches are listed here [70, 72, 73, 251, 328, 331–349]. The basic zero-current-switching quasi-resonant switch network is analyzed in detail in Sect. 23.2. Expressions for the average components of the switch network terminal waveforms are found, leading to determination of the *switch conversion ratio*  $\mu$ . The switch conversion ratio  $\mu$  performs the role of the duty cycle  $d$  of CCM PWM switch networks. For example, the buck converter exhibits conversion ratio  $M$  equal to  $\mu$ . Both half-wave and full-wave ringing of the tank network are considered; these lead to different switch conversion ratio functions  $\mu$ . In general, given a PWM CCM converter having conversion ratio  $M(d)$ , we can replace the PWM switch network with a resonant switch network having switch conversion ratio  $\mu$ . The resulting quasi-resonant converter will then have conversion ratio  $M(\mu)$ . So we can obtain soft-switching versions of all of the basic converters (buck, boost, buck-boost, forward, flyback, etc.) that exhibit zero-voltage or zero-current switching and other desirable properties.

In Sect. 23.3, the characteristics of several other resonant switch networks are listed: the zero-voltage-switching quasi-resonant switch network, the zero-current-switching and zero-voltage-switching quasi-square-wave networks, and the multiresonant switch network. One can obtain zero-voltage switching in all transistors and diodes using these networks.

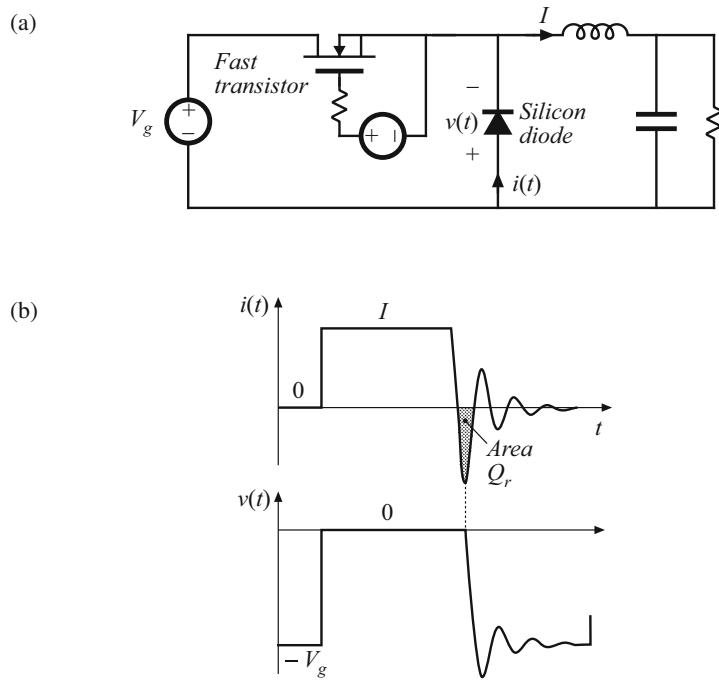
Several related soft-switching approaches are now popular, which attain zero-voltage switching of the transistor or transistors in commonly used converters. The zero-voltage transition approach finds application in full-bridge buck-derived converters. Active-clamp snubbers are often added to forward and flyback converters, to attain zero-voltage switching and to reset the transformer. These circuits lead to zero-voltage switching of the transistors, but (less-than-optimal) zero-current switching of the secondary-side diodes. Nonetheless, high efficiency can be achieved. An auxiliary resonant commutated pole can achieve zero-voltage switching in voltage-source inverters. These converters are briefly discussed in Sect. 23.4.

## 23.1 Soft-Switching Mechanisms of Semiconductor Devices

When loosely used, the terms “zero-current switching” and “zero-voltage switching” normally refer to one or more switching transitions of the transistor in a converter. However, to fully understand how a converter generates switching loss, one must closely examine the switching transitions of every semiconductor device. As described in Sect. 4.6, there are typically several mechanisms that are sources of significant switching loss. At the turn-off transition of a diode, its reverse-recovery process can induce loss in the transistor or other elements of the converter. The energy stored in the output capacitance of a MOSFET can be lost when the MOSFET turns on. IGBTs can lose significant energy during their turnoff transition, owing to the current tailing phenomenon. The effects of zero-current switching and zero-voltage switching on each of these devices are discussed in detail below.

### 23.1.1 Diode Switching

As discussed in Chap. 4, the reverse-recovery process usually leads to significant switching loss associated with the turn-off transition of diodes. This is often the largest single source



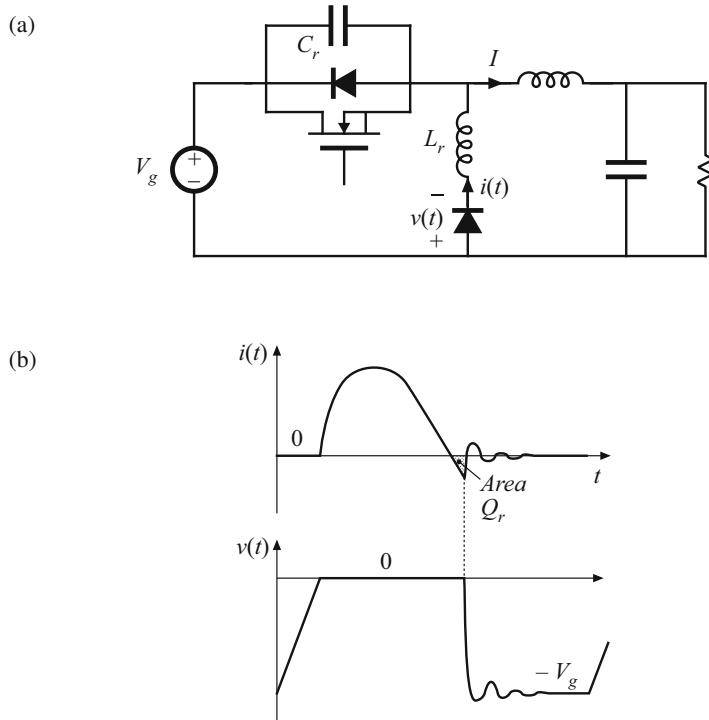
**Fig. 23.1** Hard switching at the turn-off transition of a diode, conventional buck converter example: **(a)** schematic, **(b)** diode voltage and current waveforms

of loss in a hard-switched converter. Normally, negligible loss is associated with the turn-on transition of power diodes. Three types of diode turn-off transition waveforms are commonly encountered in modern switching converters: hard switching, zero-current switching, and zero-voltage switching.

Figure 23.1 illustrates a conventional hard-switched PWM buck converter. The diode voltage and current waveforms  $v(t)$  and  $i(t)$  are also illustrated, with an exaggerated reverse recovery time. The output inductor current ripple is small. The diode turns off when the transistor is turned on; the reverse recovery process leads to a negative peak current of large amplitude. The diode must immediately support the full reverse voltage  $V_g$ , and hence both  $v(t)$  and  $i(t)$  must change with large slopes during reverse recovery. As described in Sect. 4.3.3, hard switching of the diode induces energy loss  $W_D$  in the transistor, given approximately by

$$W_D = V_g Q_r + t_r V_g I \quad (23.1)$$

where  $Q_r$  is the diode recovered charge and  $t_r$  is the reverse recovery time, both taken to be positive quantities. The recovered charge is relatively large because the slope  $di/dt$  is large during the turn-off transition. The resonant circuit formed by the diode output capacitance  $C_j$  and the diode package and other wiring inductances leads to ringing at the end of the reverse recovery time.



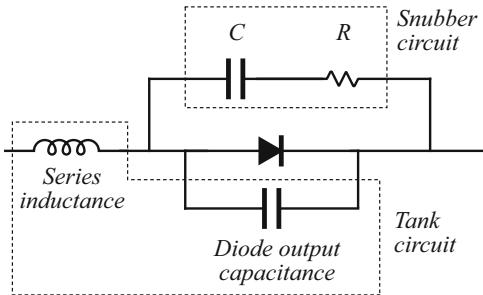
**Fig. 23.2** Zero-current switching at the turn-off transition of a diode, ZCS quasi-resonant buck converter example: (a) converter schematic, (b) diode voltage and current waveforms

Figure 23.2 illustrates zero-current switching at the turn-off transition of a diode. The converter example is a quasi-resonant zero-voltage switching buck converter (see Sect. 23.3.1). The output inductor current ripple is again small. However, tank inductor  $L_r$  is now connected in series with the diode. The resulting diode current waveform  $i(t)$  changes with a limited slope as shown. The diode reverse-recovery process commences when  $i(t)$  passes through zero and becomes negative. The negative  $i(t)$  actively removes stored charge from the diode; during this reverse recovery time, the diode remains forward-biased. When the stored charge is removed, then the diode voltage must rapidly change to  $-V_g$ . As described in Sect. 4.6.1, energy  $W_D$  is stored in inductor  $L_r$  at the end of the reverse recovery time, given by

$$W_D = V_g Q_r \quad (23.2)$$

The resonant circuit formed by  $L_r$  and the diode output capacitance  $C_j$  then cause this energy to be circulated between  $L_r$  and  $C_j$ . This energy is eventually dissipated by parasitic resistive elements in the circuit, and hence is lost. Since Eqs. (23.1) and (23.2) are similar in form, the switching losses induced by the reverse-recovery processes of diodes operating with hard switching and with zero-current switching are similar in magnitude. Zero-current switching may lead to somewhat lower loss because the reduced  $di/dt$  leads to less recovered charge  $Q_r$ .

**Fig. 23.3** A dissipative snubber circuit, for protection of a diode from excessive voltage caused by ringing



Zero-current switching of diodes also typically leads to increased peak inverse diode voltage during the ringing of  $L_r$  and  $C_j$ , because of the relatively large value of  $L_r$ .

When a diode operates with hard switching or zero-current switching, and when substantial inductance is present in series with the diode, then significant ringing is observed in the diode voltage waveform. A resonant circuit, comprised of the series inductance and the diode output capacitance, is excited by the diode reverse recovery process, and the resulting ringing voltage can be of large enough magnitude to lead to breakdown and failure of the diode. A common example is the diodes on the secondary side of a hard-switched transformer-isolated converter; the resonant circuit is then formed by the transformer leakage inductance and the diode output capacitance. Other examples are the circuits of Figs. 23.2 and 23.36, in which the series inductance is a discrete tank inductor.

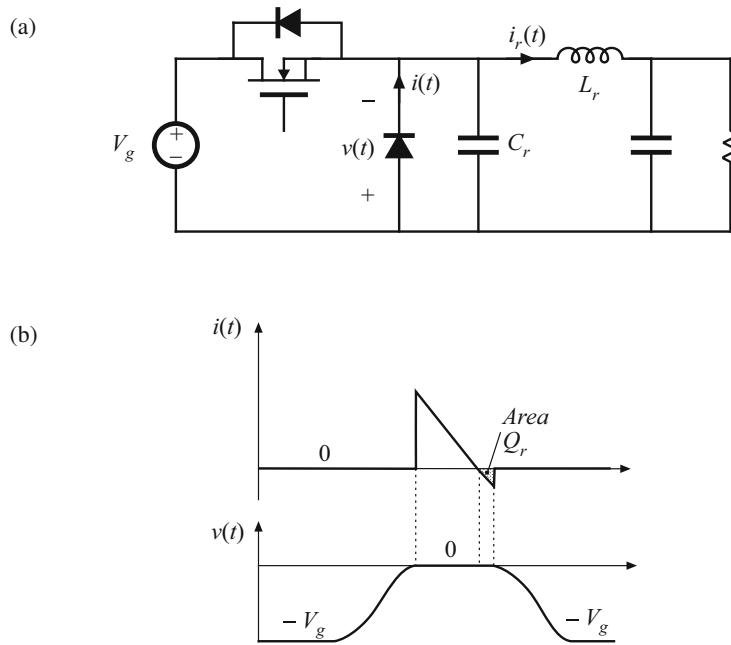
A simple snubber circuit that is often used to protect the diode from excessive reverse voltage is illustrated in Fig. 23.3. Resistor  $R$  damps the ringing of the resonant circuit. Capacitor  $C$  prevents the off-state voltage of the diode from causing excessive power loss in  $R$ . Nonetheless, the energy consumed by  $R$  per switching period is typically greater than Eqs. (23.1) or (23.2).

Figure 23.4 illustrates zero-voltage switching at the turn-off transition of a diode. The figure illustrates the example of a zero-voltage switching quasi-square wave buck converter, discussed in Sect. 23.3.3. The output inductor  $L_r$  of this converter assumes the role of the tank inductor, and exhibits large current ripple that causes the current  $i_r(t)$  to reverse polarity. While the diode conducts, its current  $i(t)$  is equal to  $i_r(t)$ . When  $i_r(t)$  becomes negative, the diode continues to conduct until its stored charge  $Q_r$  has been removed. The diode then becomes reverse-biased, and  $i_r(t)$  flows through capacitor  $C_r$  and the diode output capacitance  $C_j$ . The diode voltage and current both change with limited slope in this type of switching, and the loss induced by the diode reverse-recovery process is negligible because the waveforms are not significantly damped by parasitic resistances in the circuit, and because the peak currents during reverse recovery are relatively low. The diode stored charge and diode output capacitance both behave as an effective nonlinear capacitor that can be combined with (or replace) tank capacitor  $C_r$ . Snubber circuits such as Fig. 23.3 are not necessary when the diode operates with zero-voltage switching.

Thus, zero-voltage switching at the turn-off transition of a diode is the preferred approach that leads to minimum switching loss. Zero-current switching at the turn-off transition can be problematic, because of the high peak inverse voltage induced across the diode by ringing.

### 23.1.2 MOSFET Switching

The switching loss mechanisms typically encountered by a MOSFET in a hard-switched converter are discussed in Chap. 4, and typical MOSFET voltage and current waveforms are illustrated in Fig. 23.5. The most significant components of switching loss in the MOSFET of this circuit are: (1) the loss induced by the diode reverse recovery process and (2) the loss of the energy stored in the MOSFET output capacitance  $C_{ds}$ . Both loss mechanisms occur during the MOSFET turn-on process.

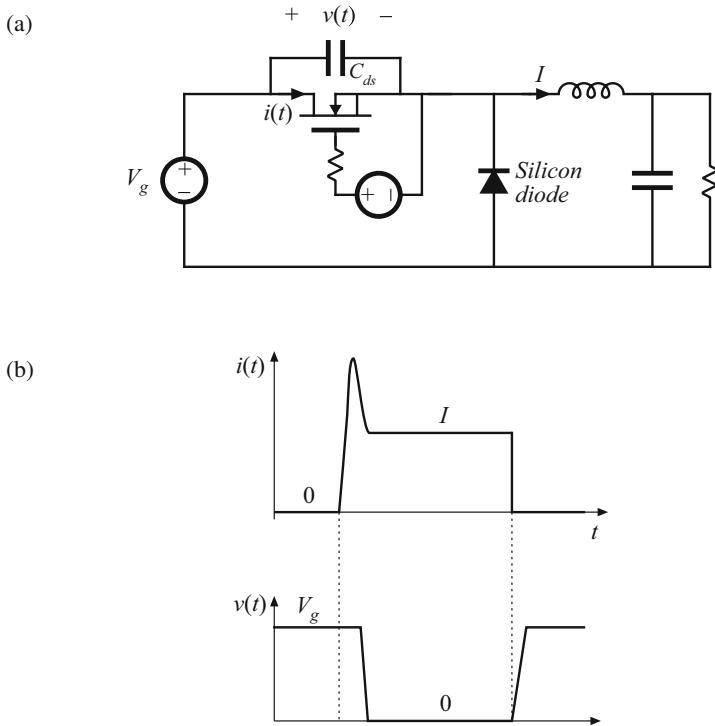


**Fig. 23.4** Zero-voltage switching at the turn-off transition of a diode, ZVS quasi-square wave buck converter example: (a) converter schematic, (b) diode current and voltage waveforms

In the hard-switched circuit of Fig. 23.5, with a fast gate driver there is essentially no switching loss incurred during the MOSFET turn-off transition. This occurs because of the substantial output capacitance  $C_{ds}$  of the MOSFET. This capacitance holds the voltage  $v(t)$  close to zero while the MOSFET turns off, so that the turn-off switching loss is very small. After the MOSFET has turned off, the output inductor current  $I$  flows through  $C_{ds}$ . The voltage  $v(t)$  then increases until  $v = V_g$  and the diode becomes forward-biased.

However, when the MOSFET turns on, a high peak current flows through the MOSFET channel, induced by the diode reverse recovery and by the output capacitances of the MOSFET and diode. This leads to substantial energy loss during the hard-switched turn-on transition of the MOSFET.

When a MOSFET (or other transistor) operates with hard switching, and when substantial inductance is present in series with the MOSFET, then significant ringing is observed in the



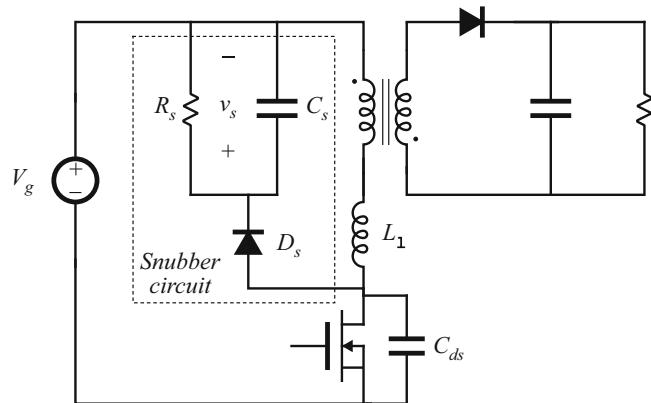
**Fig. 23.5** Hard switching of a MOSFET in a conventional buck converter: (a) schematic, (b) MOSFET voltage and current waveforms

MOSFET voltage waveform. A resonant circuit, composed of the MOSFET output capacitance and the series inductance, is excited when the MOSFET turns off, and the resulting ringing voltage can be of large enough magnitude to lead to breakdown and failure of the MOSFET. A common example is the MOSFET of the flyback converter, in which series inductance is introduced by the transformer leakage inductance. An  $R-C$  snubber circuit, similar to that used for the diode in Fig. 23.3, can be used to protect the MOSFET from damage caused by excessive applied voltage. Another common snubber circuit is illustrated in Fig. 23.6. When the MOSFET turns off, the current flowing in the transformer leakage inductance  $L_\ell$  begins to flow into the MOSFET capacitance  $C_{ds}$ . These parasitic elements then ring, and the peak transistor voltage can significantly exceed the ideal value of  $(D/D')V_g$ .

One simple way to design the snubber circuit of Fig. 23.6 is to choose the capacitance  $C_s$  to be large, so that  $v_s(t) \approx V_s$  contains negligible switching ripple. The resistance  $R_s$  is then chosen so that the power consumption of  $R_s$  at the desired voltage  $V_s$  is equal to the switching loss caused by  $L_\ell$ :

$$\frac{V_s^2}{R_s} \approx \frac{1}{2} L_\ell^2 f_s \quad (23.3)$$

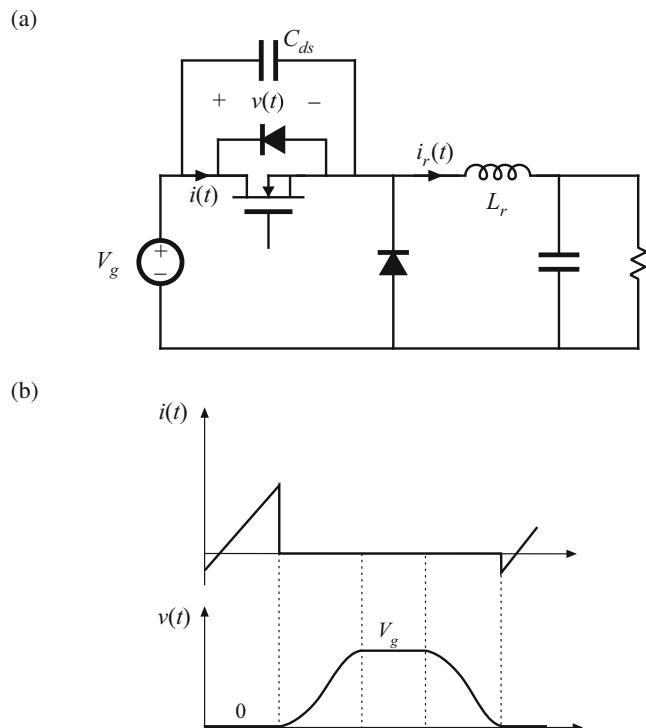
**Fig. 23.6** Insertion of a dissipative voltage-clamped snubber circuit into a flyback converter. The MOSFET voltage is clamped to a peak value of  $(V_g + V_s)$



The current  $i$  is equal to the current flowing in the transformer primary just before the MOSFET is turned off. This approximate expression is useful for obtaining a first estimate of how to choose  $R_s$  to obtain a given desired  $V_s$ .

Zero-current switching does not affect the switching loss that arises from the MOSFET output capacitance, and it may or may not influence the loss induced by diode reverse recovery. In consequence, zero-current switching is of little or no help in improving the efficiency of converters that employ MOSFETs.

**Fig. 23.7** Zero-voltage switching of a MOSFET, ZVS quasi-square wave buck converter example. The MOSFET, its body diode, and its output capacitance  $C_{ds}$  are illustrated. (a) Schematic, (b) MOSFET voltage and current waveforms



Zero-voltage switching can prevent both diode reverse recovery and semiconductor output capacitances from inducing switching loss in MOSFETs. An example is illustrated in Fig. 23.7. This circuit is again a zero-voltage switching quasi-square wave example, discussed in Sect. 23.3.3. The converter circuit naturally discharges the energy stored in  $C_{ds}$ , before the MOSFET is switched on. When the drain-to-source voltage  $v(t)$  passes through zero, the MOSFET body diode becomes forward-biased. The MOSFET can then be turned on at zero voltage, without incurring turn-on switching loss. The MOSFET turn-on transition must be completed before the tank inductor current  $i_r(t)$  becomes positive. The MOSFET turn-off transition is also lossless, and is similar to the hard-switched case discussed above.

Zero-voltage switching of a MOSFET also causes its body diode to operate with zero-voltage switching. This can eliminate the switching loss associated with reverse recovery of the slow body diode, and improve the reliability of circuits that forward-bias this diode.

Zero-voltage switching can also eliminate the overvoltage problems associated with transformer leakage inductances, removing the need for voltage-clamped snubber circuits such as in Fig. 23.6. An example is discussed in Sect. 23.4.2.

### 23.1.3 IGBT Switching

Like the MOSFET, the IGBT typically encounters substantial switching loss during its turn-on transition, induced by the reverse-recovery process of diodes within the converter. In addition, the IGBT exhibits significant switching loss during its turn-off transition, caused by the current tailing phenomenon (see Chap. 4).

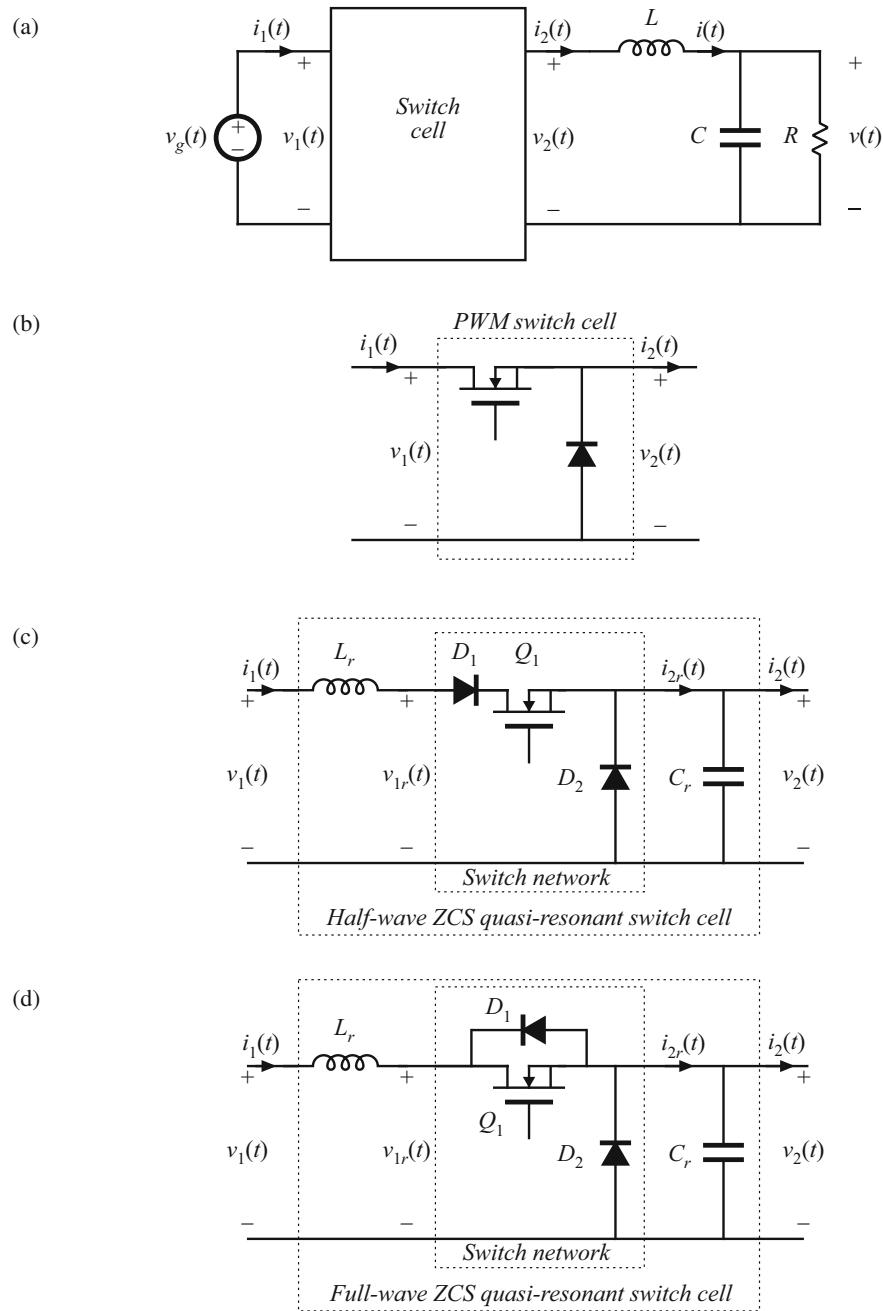
Zero-voltage switching has been successfully applied to IGBT circuits—an example is the auxiliary resonant commutation circuit discussed in Sect. 23.4.3. This has the principal advantage of eliminating the switching loss caused by diode reverse recovery. Although zero-voltage switching can reduce the loss incurred during the turn-off transition, it is difficult to eliminate the substantial loss caused by current tailing.

## 23.2 The Zero-Current Switching Quasi-Resonant Switch Cell

Figure 23.8a illustrates a generic buck converter, consisting of a switch cell cascaded by an  $L-C$  low-pass filter. When the switch cell is realized as in Fig. 23.8b, then a conventional PWM buck converter is obtained. Figures 23.8b,c illustrate two other possible realizations of the switch cell: the half-wave and full-wave zero-current-switching quasi-resonant switches [331, 332]. In these switch cells, a resonant tank capacitor  $C_r$  is placed in parallel with diode  $D_2$ , while resonant tank capacitor  $L_r$  is placed in series with the active transistor element.

Both resonant switch cells require a two-quadrant SPST switch. In the half-wave switch cell of Fig. 23.8c, diode  $D_1$  is added in series with transistor  $Q_1$ . This causes the  $Q_1-D_1$  SPST switch to turn off at the first zero crossing of the tank inductor current  $i_1(t)$ . In the full-wave switch cell of Fig. 23.8d, antiparallel diode  $D_1$  allows bidirectional flow of the tank inductor current  $i_1(t)$ . With this switch network, the  $Q_1-D_1$  SPST switch is normally turned off at the second zero crossing of the  $i_1(t)$  waveform. In either switch cell, the  $L_r$  and  $C_r$  elements are relatively small in value, such that their resonant frequency  $f_0$  is greater than the switching frequency  $f_s$ , where

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} = \frac{\omega_0}{2\pi} \quad (23.4)$$



**Fig. 23.8** Implementation of the switch cell in a buck converter: (a) buck converter, with arbitrary switch cell; (b) PWM switch cell; (c) half-wave ZCS quasi-resonant switch cell; (d) full-wave ZCS quasi-resonant switch cell

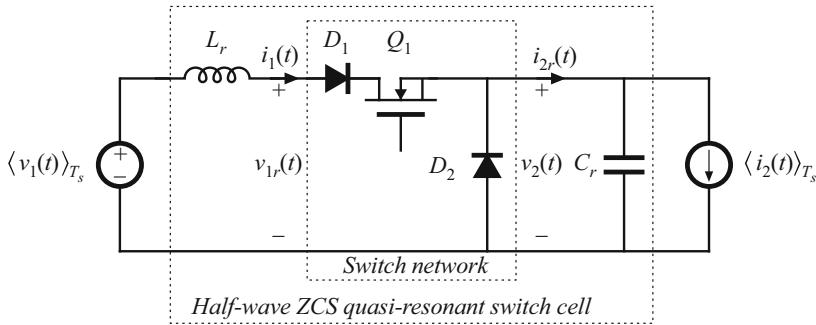
In the analysis which follows, it is assumed that the converter filter element values  $L$  and  $C$  have negligible switching ripple. Hence, the switch cell terminal waveforms  $v_1(t)$  and  $i_2(t)$  are well-approximated by their average values:

$$\begin{aligned} i_2(t) &\approx \langle i_2(t) \rangle_{T_s} \\ v_1(t) &\approx \langle v_1(t) \rangle_{T_s} \end{aligned} \quad (23.5)$$

with the average defined as in Eq. (7.3). In steady-state, we can further approximate  $v_1(t)$  and  $i_2(t)$  by their dc components  $V_1$  and  $I_2$ :

$$\begin{aligned} i_2(t) &\approx I_2 \\ v_1(t) &\approx V_1 \end{aligned} \quad (23.6)$$

Thus, the small-ripple approximation is employed for the converter filter elements, as usual.



**Fig. 23.9** The half-wave ZCS quasi-resonant switch cell, driven by the terminal quantities  $\langle v_1(t) \rangle_{T_s}$  and  $\langle i_2(t) \rangle_{T_s}$

To understand the operation of the half-wave ZCS quasi-resonant switch cell, we can solve the simplified circuit illustrated in Fig. 23.9. In accordance with the averaged switch modeling approach of Sects. 14.1 and 15.2, it is desired to determine the average terminal waveforms  $\langle v_2(t) \rangle_{T_s}$  and  $\langle i_1(t) \rangle_{T_s}$ , as functions of the applied quantities  $\langle v_1(t) \rangle_{T_s}$  and  $\langle i_2(t) \rangle_{T_s}$ . The switch conversion ratio  $\mu$  is then given by

$$\mu = \frac{\langle v_2(t) \rangle_{T_s}}{\langle v_{1r}(t) \rangle_{T_s}} = \frac{\langle i_1(t) \rangle_{T_s}}{\langle i_{2r}(t) \rangle_{T_s}} \quad (23.7)$$

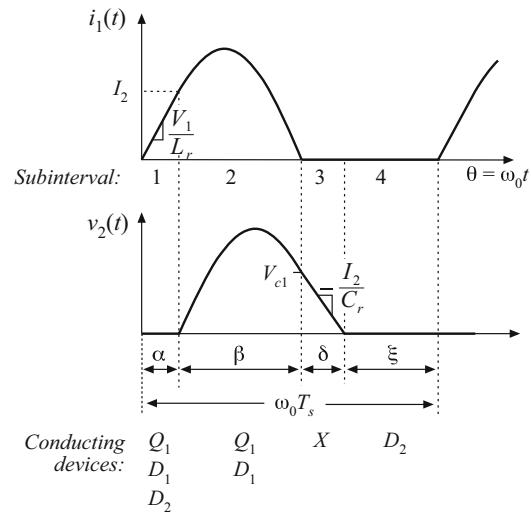
In steady state, we can write

$$\mu = \frac{V_2}{V_1} = \frac{I_1}{I_2} \quad (23.8)$$

The steady-state analysis of this section employs Eq. (23.8) to determine  $\mu$ .

### 23.2.1 Waveforms of the Half-Wave ZCS Quasi-Resonant Switch Cell

Typical waveforms of the half-wave cell of Fig. 23.9 are illustrated in Fig. 23.10. Each switching period consists of four subintervals as shown, having angular lengths  $\alpha, \beta, \delta$ , and  $\xi$ . The



switching period begins when the controller turns on transistor  $Q_1$ . The initial values of the tank inductor current  $i_1(t)$  and tank capacitor voltage  $v_2(t)$  are zero. During subinterval 1, all three semiconductor devices conduct. Diode  $D_2$  is forward-biased because  $i_1(t)$  is less than  $I_2$ . In consequence, during subinterval 1 the switch cell reduces to the circuit of Fig. 23.11.

The slope of the inductor current is given by

$$\frac{di_1(t)}{dt} = \frac{V_1}{L_r} \quad (23.9)$$

with the initial condition  $i_1(0) = 0$ . The solution is

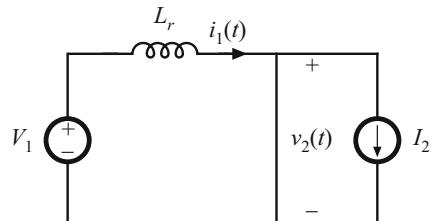
$$i_1(t) = \frac{V_1}{L_r} t = \omega_0 t \frac{V_1}{R_0} \quad (23.10)$$

where the tank characteristic impedance  $R_0$  is defined as

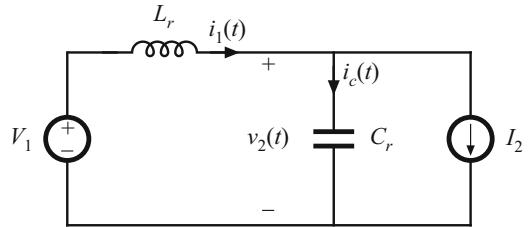
$$R_0 = \sqrt{\frac{L_r}{C_r}} \quad (23.11)$$

It is convenient to express the waveforms in terms of the angle  $\theta = \omega_0 t$ , instead of time  $t$ . At the end of subinterval 1,  $\omega_0 t = \alpha$ . The subinterval ends when diode  $D_2$  becomes reverse-biased. Since the diode  $D_2$  current is equal to  $I_2 - i_1(t)$ , this occurs when  $i_1(t) = I_2$ . Hence, we can write

**Fig. 23.11** Circuit of the switch network during subinterval 1



**Fig. 23.12** Circuit of the switch network during subinterval 2



$$i_1(\alpha) = \alpha \frac{V_1}{R_0} = I_2 \quad (23.12)$$

Solution for  $\alpha$  yields

$$\alpha = \frac{I_2 R_0}{V_1} \quad (23.13)$$

During subinterval 2, transistor  $Q_1$  and diode  $D_1$  conduct, while diode  $D_2$  is reverse-biased. The switch network then becomes the circuit illustrated in Fig. 23.12. The resonant  $L_r-C_r$  tank network is excited by the constant sources  $V_1$  and  $I_2$ . The network equations are

$$\begin{aligned} L_r \frac{di_1(\omega_0 t)}{dt} &= V_1 - v_2(\omega_0 t) \\ C_r \frac{dv_2(\omega_0 t)}{dt} &= i_1(\omega_0 t) - I_2 \end{aligned} \quad (23.14)$$

with the initial conditions

$$\begin{aligned} v_2(\alpha) &= 0 \\ i_1(\alpha) &= I_2 \end{aligned} \quad (23.15)$$

The solution is

$$\begin{aligned} i_1(\omega_0 t) &= I_2 + \frac{V_1}{R_0} \sin(\omega_0 t - \alpha) \\ v_2(\omega_0 t) &= V_1(1 - \cos(\omega_0 t - \alpha)) \end{aligned} \quad (23.16)$$

The tank inductor current rises to a peak value given by

$$I_{1pk} = I_2 + \frac{V_1}{R_0} \quad (23.17)$$

The subinterval ends at the first zero crossing of  $i_1(t)$ . If we denote the angular length of the subinterval as  $\beta$ , then we can write

$$i_1(\alpha + \beta) = I_2 + \frac{V_1}{R_0} \sin(\beta) = 0 \quad (23.18)$$

Solution for  $\sin(\beta)$  yields

$$\sin(\beta) = -\frac{I_2 R_0}{V_1} \quad (23.19)$$

Care must be employed when solving Eq. (23.19) for the angle  $\beta$ . It can be observed from Fig. 23.10 that the angle  $\beta$  is greater than  $\pi$ . The correct branch of the arcsine function must be selected, as follows:

$$\beta = \pi + \sin^{-1} \left( \frac{I_2 R_0}{V_1} \right) \quad (23.20)$$

where

$$-\frac{\pi}{2} < \sin^{-1}(x) \leq \frac{\pi}{2}$$

Note that the inequality

$$I_2 < \frac{V_1}{R_0} \quad (23.21)$$

must be satisfied; otherwise, there is no solution to Eq. (23.19). At excessive load currents, where Eq. (23.21) is not satisfied, the tank inductor current never reaches zero, and the transistor does not switch off at zero current.

The tank capacitor voltage at the end of subinterval 2 is found by evaluation of Eq. (23.16) at  $\omega_0 t = (\alpha + \beta)$ . The  $\cos(\beta)$  term can be expressed as

$$\cos(\beta) = -\sqrt{1 - \sin^2(\beta)} = -\sqrt{1 - \left( \frac{I_2 R_0}{V_1} \right)^2} \quad (23.22)$$

Substitution of Eq. (23.22) into Eq. (23.16) leads to

$$v_2(\alpha + \beta) = V_{c1} = V_1 \left( 1 + \sqrt{1 - \left( \frac{I_2 R_0}{V_1} \right)^2} \right) \quad (23.23)$$

At the end of subinterval 2, diode  $D_1$  becomes reverse-biased. Transistor  $Q_1$  can then be switched off at zero current.

During subinterval 3, all semiconductor devices are off, and the switch cell reduces to the circuit of Fig. 23.13. The tank capacitor  $C_r$  is discharged by the filter inductor current  $I_2$ . Hence, the tank capacitor voltage  $v_2$  decreases linearly to zero. The circuit equations are

$$C_r \frac{dv_2(\omega_0 t)}{dt} = -I_2 \quad (23.24)$$

$$v_2(\alpha + \beta) = V_{c1}$$

The solution is

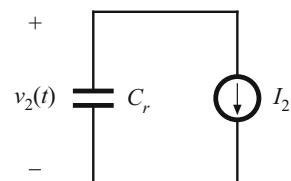
$$v_2(\omega_0 t) = V_{c1} - I_2 R_0 (\omega_0 t - \alpha - \beta) \quad (23.25)$$

Subinterval 3 ends when the tank capacitor voltage reaches zero. Diode  $D_2$  then becomes forward-biased. Hence, we can write

$$v_2(\alpha + \beta + \delta) = V_{c1} - I_2 R_0 \delta = 0 \quad (23.26)$$

where  $\delta$  is the angular length of subinterval 3. Solution for  $\delta$  yields

**Fig. 23.13** Circuit of the switch network during subinterval 3



$$\delta = \frac{V_{c1}}{I_2 R_0} = \frac{V_1}{I_2 R_0} \left( 1 - \sqrt{1 - \left( \frac{I_2 R_0}{V_1} \right)^2} \right) \quad (23.27)$$

Subinterval 4, of angular length  $\xi$ , is identical to the diode conduction subinterval of the conventional PWM switch network. Diode  $D_2$  conducts the filter inductor current  $I_2$ , and the tank capacitor voltage  $v_2$  is equal to zero. Transistor  $Q_1$  is off, and the input current  $i_1$  is equal to zero.

The angular length of the switching period is

$$\omega_0 T_s = \alpha + \beta + \delta + \xi = \frac{2\pi f_0}{f_s} = \frac{2\pi}{F} \quad (23.28)$$

where

$$F = \frac{f_s}{f_0} \quad (23.29)$$

Quasi-resonant switch networks are usually controlled by variation of the switching frequency  $f_s$  or, in normalized terms, by variation of  $F$ . Note that the interval lengths  $\alpha, \beta$ , and  $\delta$  are determined by the response of the tank network. Hence, control of the switching frequency is equivalent to control of the fourth subinterval length  $\xi$ . The subinterval length  $\xi$  must be positive, and hence, the minimum switching period is limited as follows:

$$\omega_0 T_s \geq \alpha + \beta + \delta \quad (23.30)$$

Substitution of Eqs. (23.13), (23.20), and (23.27) into Eq. (23.30) yields

$$\frac{2\pi}{F} \geq \frac{I_2 R_0}{V_1} + \pi + \sin^{-1} \left( \frac{I_2 R_0}{V_1} \right) + \frac{V_1}{I_2 R_0} \left( 1 - \sqrt{1 - \left( \frac{I_2 R_0}{V_1} \right)^2} \right) \quad (23.31)$$

This expression limits the maximum switching frequency, or maximum  $F$ , of the half-wave ZCS quasi-resonant switch cell.

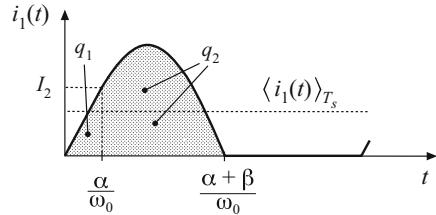
### 23.2.2 The Average Terminal Waveforms

It is now desired to solve for the power processing function performed by the switch network. The switch conversion ratio  $\mu$  is a generalization of the duty cycle  $d$ . It expresses how a resonant switch network controls the average voltages and currents of a converter. In our buck converter example, we can define  $\mu$  as the ratio of  $\langle v_2(t) \rangle_{T_s}$  to  $\langle v_1(t) \rangle_{T_s}$ , or equivalently, the ratio of  $\langle i_1(t) \rangle_{T_s}$  to  $\langle i_2(t) \rangle_{T_s}$ . In a hard-switched PWM network, this ratio is equal to the duty cycle  $d$ . Hence, analytical results derived for hard-switched PWM converters can be adapted to quasi-resonant converters, simply by replacing  $d$  with  $\mu$ . In this section, we derive an expression for  $\mu$ , by averaging the terminal waveforms of the switch network.

The switch input current waveform  $i_1(t)$  of Fig. 23.10 is reproduced in Fig. 23.14. The average switch input current is given by

$$\langle i_1(t) \rangle_{T_s} = \frac{1}{T_s} \int_t^{t+T_s} i_1(t) dt = \frac{q_1 + q_2}{T_s} \quad (23.32)$$

**Fig. 23.14** Input current waveform  $i_1(t)$ , and the areas  $q_1$  and  $q_2$  during subintervals 1 and 2, respectively



The charge quantities  $q_1$  and  $q_2$  are the areas under the  $i_1(t)$  waveform during the first and second subintervals, respectively. The charge  $q_1$  is given by the triangle area formula

$$q_1 = \int_0^{\frac{\alpha}{\omega_0}} i_1(t) dt = \frac{1}{2} \left( \frac{\alpha}{\omega_0} \right) (I_2) \quad (23.33)$$

The time  $\alpha/\omega_0$  is the length of subinterval 1. The charge  $q_2$  is

$$q_2 = \int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_1(t) dt \quad (23.34)$$

According to Fig. 23.12, during subinterval 2 the current  $i_1(t)$  can be related to the tank capacitor current  $i_C(t)$  and the switch output current  $I_2$  by the node equation

$$i_1(t) = i_C(t) + I_2 \quad (23.35)$$

Substitution of Eq. (23.35) into Eq. (23.34) leads to

$$q_2 = \int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_C(t) dt + \int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} I_2 dt \quad (23.36)$$

Both integrals in Eq. (23.36) can easily be evaluated, as follows. Since the second term involves the integral of the constant current  $I_2$ , this term is

$$\int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} I_2 dt = I_2 \frac{\beta}{\omega_0} \quad (23.37)$$

The first term in Eq. (23.36) involves the integral of the capacitor current over subinterval 2. Hence, this term is equal to the change in capacitor charge over the second subinterval:

$$\int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_C(t) dt = C \left( v_2 \left( \frac{\alpha + \beta}{\omega_0} \right) - v_2 \left( \frac{\alpha}{\omega_0} \right) \right) \quad (23.38)$$

(recall that  $\Delta q = C\Delta v$  in a capacitor). During the second subinterval, the tank capacitor voltage is initially zero, and has a final value of  $V_{c1}$ . Hence, Eq. (23.38) reduces to

$$\int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_C(t) dt = C (V_{c1} - 0) = CV_{c1} \quad (23.39)$$

Substitution of Eqs. (23.37) and (23.39) into Eq. (23.36) leads to the following expression for  $q_2$ :

$$q_2 = CV_{c1} + I_2 \frac{\beta}{\omega_0} \quad (23.40)$$

Equations (23.33) and (23.40) can now be inserted into Eq. (23.32), to obtain the following expression for the switch input current:

$$\langle i_1(t) \rangle_{T_s} = \frac{\alpha I_2}{2\omega_0 T_s} + \frac{CV_{c1}}{T_s} + \frac{\beta I_2}{\omega_0 T_s} \quad (23.41)$$

Substitution of Eq. (23.41) into (23.8) leads to the following expression for the switch conversion ratio:

$$\mu = \frac{\langle i_1(t) \rangle_{T_s}}{I_2} = \frac{\alpha}{2\omega_0 T_s} + \frac{CV_{c1}}{I_2 T_s} + \frac{\beta}{\omega_0 T_s} \quad (23.42)$$

Finally, the quantities  $\alpha, \beta$ , and  $V_{c1}$  can be eliminated, using Eqs. (23.13), (23.20), (23.23). The result is

$$\mu = F \frac{1}{2\pi} \left[ \frac{1}{2} J_s + \pi + \sin^{-1}(J_s) + \frac{1}{J_s} \left( 1 + \sqrt{1 - J_s^2} \right) \right] \quad (23.43)$$

where

$$J_s = \frac{I_2 R_0}{V_1} \quad (23.44)$$

Equation (23.43) is of the form

$$\mu = FP_{\frac{1}{2}}(J_s) \quad (23.45)$$

where

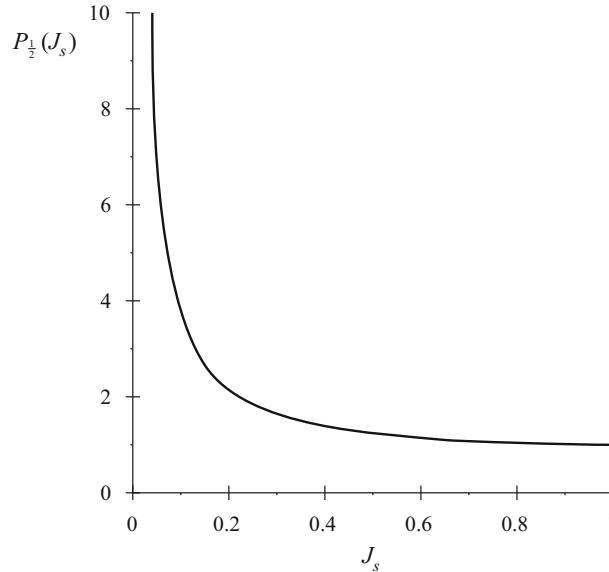
$$P_{\frac{1}{2}}(J_s) = \frac{1}{2\pi} \left[ \frac{1}{2} J_s + \pi + \sin^{-1}(J_s) + \frac{1}{J_s} \left( 1 + \sqrt{1 - J_s^2} \right) \right] \quad (23.46)$$

Thus, the switch conversion ratio  $\mu$  is directly controllable by variation of the switching frequency, through  $F$ . The switch conversion ratio is also a function of the applied terminal voltage  $V_1$  and current  $I_2$ , via  $J_s$ . The function  $P_{\frac{1}{2}}(J_s)$  is sketched in Fig. 23.15. The switch conversion ratio  $\mu$  is sketched in Fig. 23.16, for various values of  $F$  and  $J_s$ . These characteristics are similar in shape to the function  $P(J_s)$ , and are simply scaled by the factor  $F$ . It can be seen that the conversion ratio  $\mu$  is a strong function of the current  $I_2$ , via  $J_s$ . The characteristics end at  $J_s = 1$ ; according to Eq. (23.31), the zero-current switching property is lost when  $J_s > 1$ . The characteristics also end at the maximum switching-frequency limit given by Eq. (23.31). This expression can be simplified by use of Eq. (23.43), to express the limit in terms of  $\mu$  as follows:

$$\mu \leq 1 - \frac{J_s F}{4\pi} \quad (23.47)$$

The switch conversion ratio  $\mu$  is thus limited to a value slightly less than 1.

The averaged waveforms of converters containing half-wave ZCS quasi-resonant switches can now be determined. The results of the analysis of PWM converters operating in the continu-



**Fig. 23.15** The function  $P_{\frac{1}{2}}(J_s)$

ous conduction mode can be directly adapted to the related quasi-resonant converters, simply by replacing the duty cycle  $d$  with the switch conversion ratio  $\mu$ . For the buck converter example, the conversion ratio is

$$M = \frac{V}{V_g} = \mu \quad (23.48)$$

This result could also be derived by use of the principle of inductor volt-second balance. The average voltage across the filter inductor is  $(\mu V_g - V)$ . Upon equating this voltage to zero, we obtain Eq. (23.48).

In the buck converter,  $I_2$  is equal to the load current  $I$ , while  $V_1$  is equal to the converter input voltage  $V_g$ . Hence, the quantity  $J_s$  is

$$J_s = \frac{IR_0}{V_g} \quad (23.49)$$

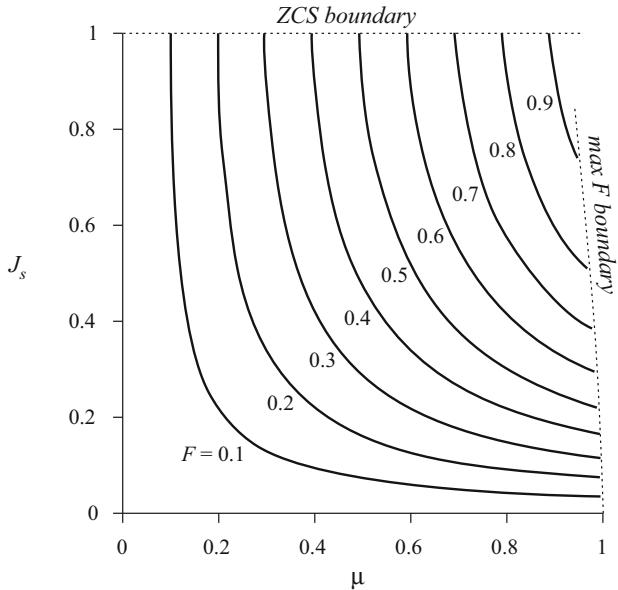
Zero-current switching occurs for

$$I \leq \frac{V_g}{R_0} \quad (23.50)$$

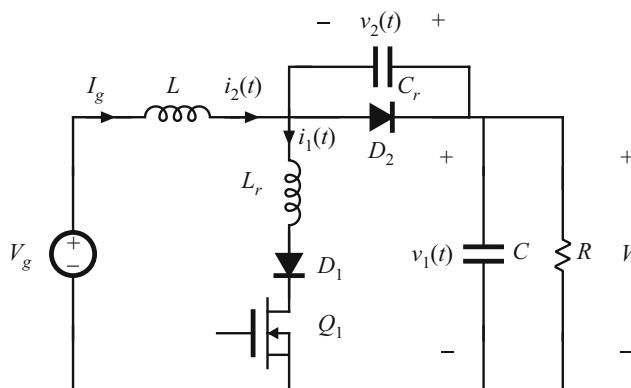
The output voltage can vary over the range

$$0 \leq V \leq V_g - \frac{FIR_0}{4\pi} \quad (23.51)$$

which nearly coincides with the PWM output voltage range  $0 \leq V \leq V_g$ .



**Fig. 23.16** Characteristics of the half-wave ZCS quasi-resonant switch



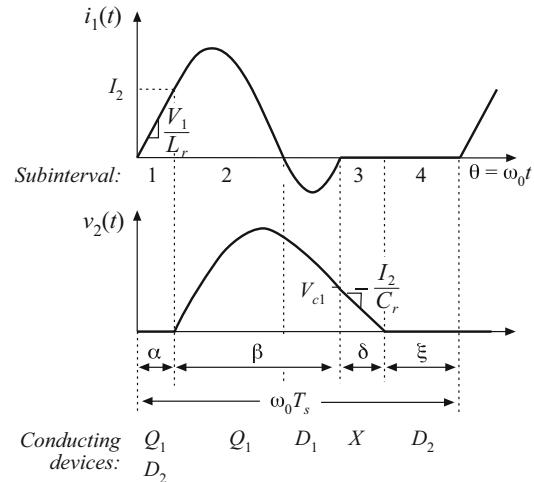
**Fig. 23.17** Boost converter containing a half-wave ZCS quasi-resonant switch

A boost converter employing a half-wave ZCS quasi-resonant switch is illustrated in Fig. 23.17. The conversion ratio of the boost converter is given by

$$M = \frac{V}{V_g} = \frac{1}{1 - \mu} \quad (23.52)$$

The half-wave switch conversion ratio  $\mu$  is again given by Eqs. (23.44) to (23.46). For the boost converter, the applied switch voltage  $V_1$  is equal to the output voltage  $V$ , while the applied switch current  $I_2$  is equal to the filter inductor current, or  $I_g$ . Hence, the quantity  $J_s$  is

$$J_s = \frac{I_2 R_0}{V_1} = \frac{I_g R_0}{V} \quad (23.53)$$



**Fig. 23.18** Tank inductor current and capacitor voltage waveforms, for the full-wave ZCS quasi-resonant switch cell of Fig. 23.8d

Also, the input current  $I_g$  of the boost converter is related to the load current  $I$  according to

$$I_g = \frac{I}{1 - \mu} \quad (23.54)$$

Equations (23.52) to (23.54), in conjunction with Eqs. (23.44) to (23.46), describe the averaged waveforms of the half-wave quasi-resonant ZCS boost converter.

### 23.2.3 The Full-Wave ZCS Quasi-Resonant Switch Cell

The full-wave ZCS quasi-resonant switch cell is illustrated in Fig. 23.8d. It differs from the half-wave cell in that elements  $D_1$  and  $Q_1$  are connected in antiparallel, to form a current-bidirectional two-quadrant switch. Typical tank inductor current and tank capacitor voltage waveforms are illustrated in Fig. 23.18. These waveforms are similar to those of the half-wave case, except that the  $Q_1/D_1$  switch interrupts the tank inductor current  $i_1(t)$  at its second zero crossing. While  $i_1(t)$  is negative, diode  $D_1$  conducts, and transistor  $Q_1$  can be turned off at zero current.

The analysis is nearly the same as for the half-wave case, with the exception of subinterval 2. The subinterval 2 angular length  $\beta$  and final voltage  $V_{c1}$  can be shown to be

$$\beta = \begin{cases} \pi + \sin^{-1}(J_s) & \text{(half wave)} \\ 2\pi - \sin^{-1}(J_s) & \text{(full wave)} \end{cases} \quad (23.55)$$

$$V_{c1} = \begin{cases} V_1 \left( 1 + \sqrt{1 - J_s^2} \right) & \text{(half wave)} \\ V_1 \left( 1 - \sqrt{1 - J_s^2} \right) & \text{(full wave)} \end{cases} \quad (23.56)$$

In either case, the switch conversion ratio  $\mu$  is given by Eq. (23.42). For the full-wave switch, one obtains

$$\mu = FP_1(J_s) \quad (23.57)$$

where  $P_1(J_s)$  is given by

$$P_1(J_s) = \frac{1}{2\pi} \left[ \frac{1}{2} J_s + 2\pi - \sin^{-1}(J_s) + \frac{1}{J_s} \left( 1 - \sqrt{1 - J_s^2} \right) \right] \quad (23.58)$$

In the full-wave case,  $P_1(J_s)$  is essentially independent of  $J_s$ :

$$P_1(J_s) \approx 1 \quad (23.59)$$

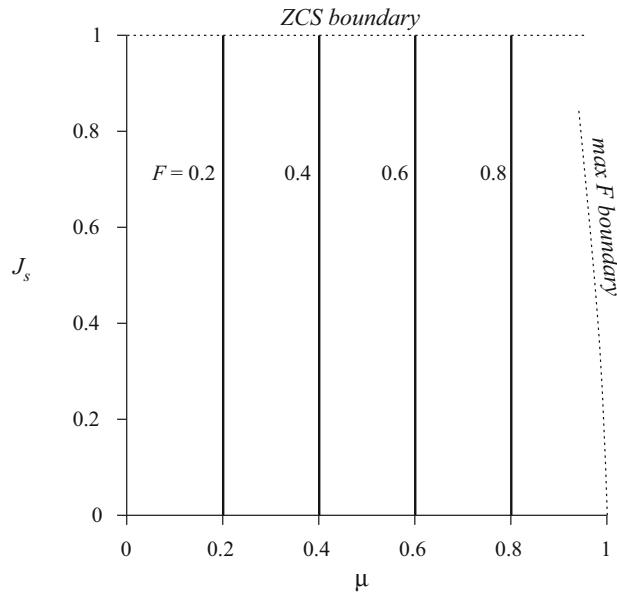
The worst-case deviation of  $P_1(J_s)$  from 1 occurs as  $J_s$  tends to 1, where  $P_1(J_s)$  tends to 0.96. So  $P_1(J_s)$  lies within 4% of unity for  $0 < J_s < 1$ . Hence, for the full-wave case, it is a good approximation to express the switch conversion ratio as

$$\mu \approx F = \frac{f_s}{f_0} \quad (23.60)$$

The full-wave quasi-resonant switch therefore exhibits voltage-source output characteristics, controllable by  $F$ . Equations describing the average waveforms of CCM PWM converters can be adapted to apply to full-wave ZCS quasi-resonant converters, simply by replacing the duty cycle  $d$  with the normalized switching frequency  $F$ . The conversion ratios of full-wave quasi-resonant converters exhibit negligible dependence on the load current.

The variation of the switch conversion ratio  $\mu$  with  $F$  and  $J_s$  is plotted in Fig. 23.19. For a typical voltage regulator application, the range of switching-frequency variations is much smaller in the full wave mode than in the half-wave mode, because  $\mu$  does not depend on the load current. Variations in the load current do not induce the controller to significantly change the switching frequency.

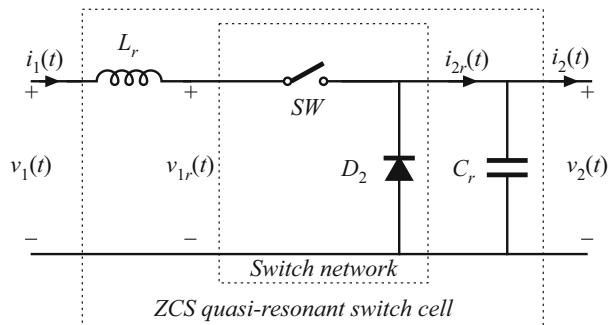
**Fig. 23.19** Characteristics of the full-wave ZCS quasi-resonant switch



### 23.3 Resonant Switch Topologies

So far, we have considered the zero-current-switching quasi-resonant switch cell, illustrated in Fig. 23.20. The ideal SPST switch is realized using a voltage-bidirectional or current-bidirectional two-quadrant switch, to obtain half-wave or full-wave ZCS quasi-resonant switch networks, respectively.

**Fig. 23.20** Basic ZCS quasi-resonant switch cell

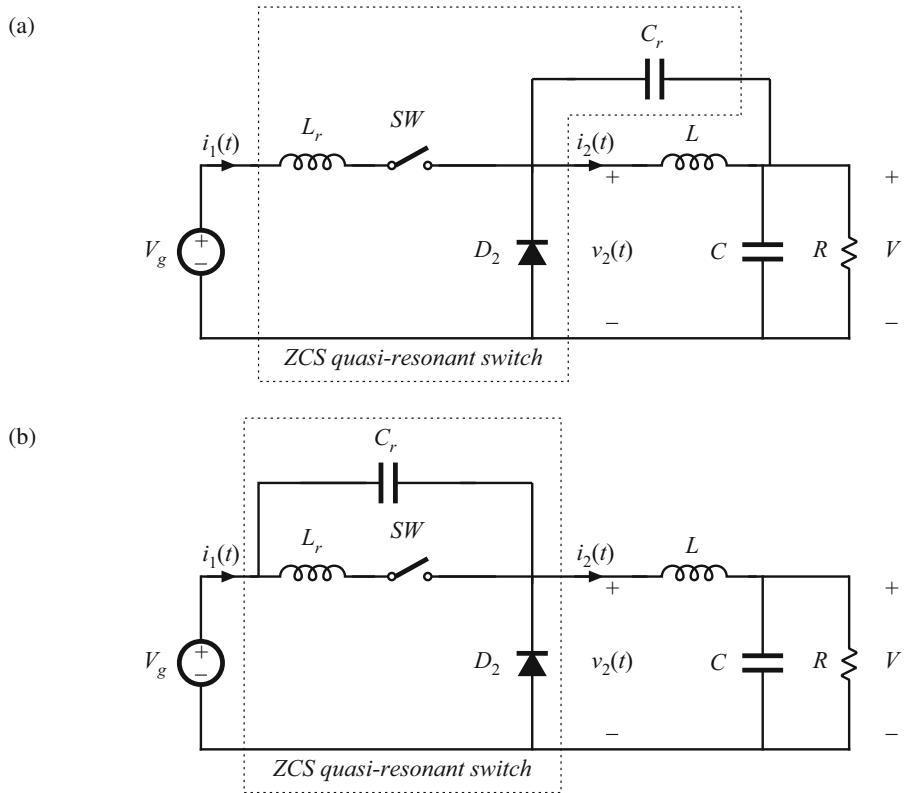


The resonant elements  $L_r$  and  $C_r$  can be moved to several different positions in the converter, without altering the basic switch properties. For example, Fig. 23.21 illustrates connection of the resonant tank capacitor  $C_r$  between the cathode of diode  $D_2$ , and the converter output or input terminals. Although this may change the dc component of the tank capacitor voltage, the ac components of the tank capacitor voltage waveform are unchanged. Also, the terminal voltage waveform  $v_2(t)$  is unchanged. The voltages  $v_g(t)$  and  $v(t)$  contain negligible high-frequency ac components, and hence the converter input and output terminal potentials can be considered to be at high-frequency ac ground.

A test to determine the topology of a resonant switch network is to replace all low-frequency filter inductors with open circuits, and to replace all dc sources and low-frequency filter capacitors with short circuits [343]. The elements of the resonant switch cell remain. In the case of the zero-current-switching quasi-resonant switch, the network of Fig. 23.22 is always obtained.

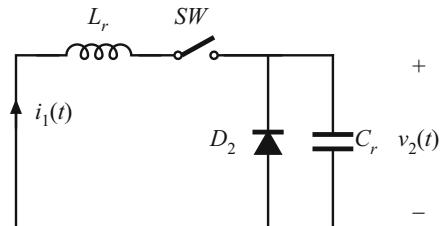
It can be seen from Fig. 23.22 that diode  $D_2$  switches on and off at the zero crossings of the tank capacitor voltage  $v_2(t)$ , while the switch elements  $Q_1$  and  $D_1$  switch at the zero crossings of the tank inductor current  $i_1(t)$ . Zero-voltage switching of diode  $D_2$  is highly advantageous, because it essentially eliminates the switching loss caused by the recovered charge and output capacitance of diode  $D_2$ . Zero-current switching of  $Q_1$  and  $D_1$  can be used to advantage when  $Q_1$  is realized by an SCR or IGBT. However, in high-frequency converters employing MOSFETs, zero-current switching of  $Q_1$  and  $D_1$  is generally a poor choice. Significant switching loss due to the output capacitances of  $Q_1$  and  $D_1$  may be observed. In addition, in the full-wave case, the recovered charge of diode  $D_1$  leads to significant ringing and switching loss at the end of subinterval 2 [333].

The ZCS quasi-resonant switch exhibits increased conduction loss, relative to an equivalent PWM switch, because the peak transistor current is increased. The peak transistor current is given by Eq. (23.17); since  $J_s \leq 1$ , the peak current is  $I_{1pk} \geq 2I_2$ . In addition, the full-wave ZCS switch exhibits poor efficiency at light load, owing to the conduction loss caused by circulating tank currents. The half-wave ZCS switch exhibits additional conduction loss due to the added



**Fig. 23.21** Connection of the tank capacitor of the ZCS quasi-resonant cell to other points at ac ground: (a) connection to the dc output, (b) connection to the dc input. In each case, the ac components of the waveforms are unchanged

**Fig. 23.22** Elimination of converter low-frequency elements causes the ZCS quasi-resonant switch cell to reduce to this network



forward voltage drop of diode  $D_1$ . The peak transistor voltage is  $V_1$ , which is identical to the PWM case.

### 23.3.1 The Zero-Voltage-Switching Quasi-Resonant Switch

The resonant switch network illustrated in Fig. 23.23 is the dual of the network of Fig. 23.22. This network is known as the zero-voltage-switching quasi-resonant switch [334]. Since the tank capacitor  $C_r$  appears in parallel with the SPST switch, the elements  $Q_1$  and  $D_1$  used to

realize the SPST switch turn on and off at zero voltage. The tank inductor  $L_r$  is effectively in series with diode  $D_2$ , and hence diode  $D_2$  switches at zero current. Converters containing ZVS quasi-resonant switches can be realized in a number of ways. The only requirement is that, when the low-frequency filter inductors, filter capacitors, and sources are replaced by open-or short circuits as described above, then the high-frequency switch network of Fig. 23.23 should remain.

For example, a zero-voltage-switching quasi-resonant buck converter is illustrated in Fig. 23.24a. Typical tank capacitor voltage and tank inductor current waveforms are given in Fig. 23.24b. A current-bidirectional realization of the two-quadrant SPST switch is shown; this causes the ZVS quasi-resonant switch to operate in the half-wave mode. Use of a voltage-bidirectional two-quadrant SPST switch allows full-wave operation.

By analysis similar to that of Sect. 23.2, it can be shown that the switch conversion ratio  $\mu$  of the half-wave ZVS quasi-resonant switch is

$$\mu = 1 - FP_{\frac{1}{2}} \left( \frac{1}{J_s} \right) \quad (23.61)$$

The function  $P_{\frac{1}{2}}(J_s)$  is again given by Eq. (23.46), and the quantity  $J_s$  is defined in Eq. (23.44). For the full-wave ZVS quasi-resonant switch, one obtains

$$\mu = 1 - FP_1 \left( \frac{1}{J_s} \right) \quad (23.62)$$

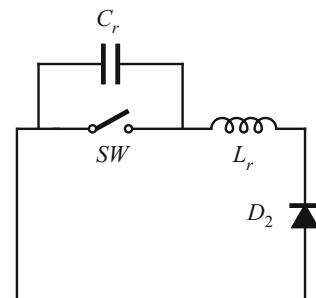
where  $P_1(J_s)$  is given by Eq. (23.58). The condition for zero-voltage switching is

$$J_s \geq 1 \quad (23.63)$$

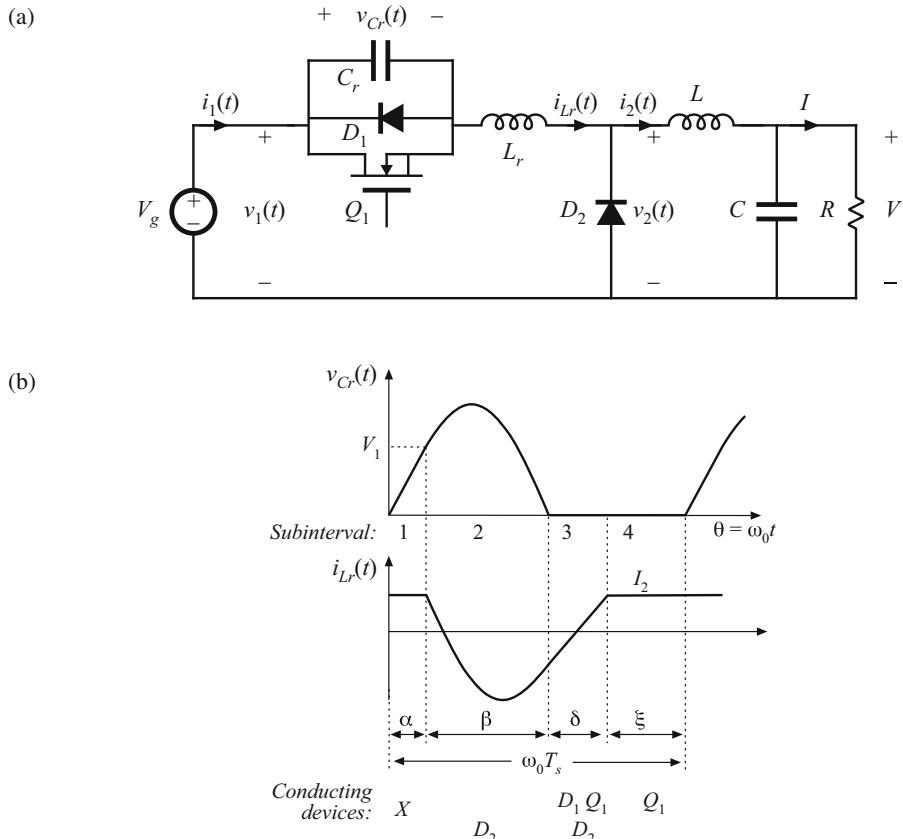
Thus, the zero-voltage switching property is lost at light load. The peak transistor voltage is given by

$$\text{peak transistor voltage } V_{cr,pk} = (1 + J_s)V_1 \quad (23.64)$$

This equation predicts that load current variations can lead to large voltage stress on transistor  $Q_1$ . For example, if it is desired to obtain zero-voltage switching over a 5:1 range of load current variations, then  $J_s$  should vary between 1 and 5. According to Eq. (23.64), the peak transistor voltage then varies between two times and six times the applied voltage  $V_1$ . The maximum transistor current is equal to the applied current  $I_2$ . Although the maximum transistor current in the ZVS quasi-resonant switch is identical to that of the PWM switch, the peak transistor blocking voltage is substantially increased. This leads to increased conduction loss, because transistor on-resistance increases rapidly with rated blocking voltage.



**Fig. 23.23** Elimination of converter low-frequency elements reduces the ZVS quasi-resonant switch cell to this network



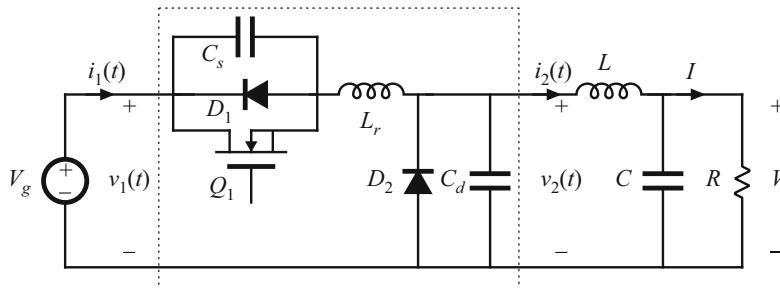
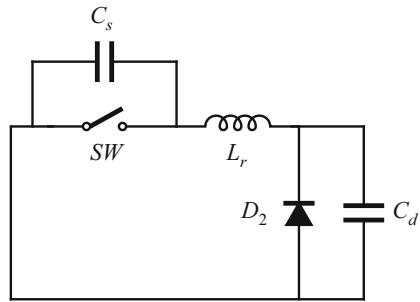
**Fig. 23.24** A ZVS quasi-resonant buck converter: (a) circuit, (b) tank waveforms

### 23.3.2 The Zero-Voltage-Switching Multiresonant Switch

The resonant switch network of Fig. 23.25 contains tank capacitor  $C_d$  in parallel with diode  $D_2$ , as in the ZCS switch network of Fig. 23.22. In addition, it contains tank capacitor  $C_s$  in parallel with the SPST switch, as in the ZVS switch network of Fig. 23.23. In consequence, all semiconductor elements switch at zero voltage. This three-element resonant switch network is known as the zero-voltage-switching multiresonant switch (ZVS MRS). Since no semiconductor output capacitances or diode recovered charges lead to ringing or switching loss, the ZVS MRS exhibits very low switching loss. For the same reason, generation of electromagnetic interference is reduced.

A half-wave ZVS MRS realization of the buck converter is illustrated in Fig. 23.26. In a typical design that must operate over a 5:1 load range and with  $0.4 \leq \mu \leq 0.6$ , the designer might choose a maximum  $F$  of 1.0, a maximum  $J$  of 1.4, and  $C_d/C_s = 3$ , where these quantities are defined as follows:

**Fig. 23.25** Elimination of converter low-frequency elements reduces the ZVS multiresonant switch cell to this network



**Fig. 23.26** Half-wave ZVS multiresonant buck converter

$$\begin{aligned} f_0 &= \frac{1}{2\pi\sqrt{LC_t}} \quad R_0 = \sqrt{\frac{L}{C_t}} \\ F &= \frac{f_s}{f_0} \quad J = \frac{I_2 R_0}{V_1} \end{aligned} \quad (23.65)$$

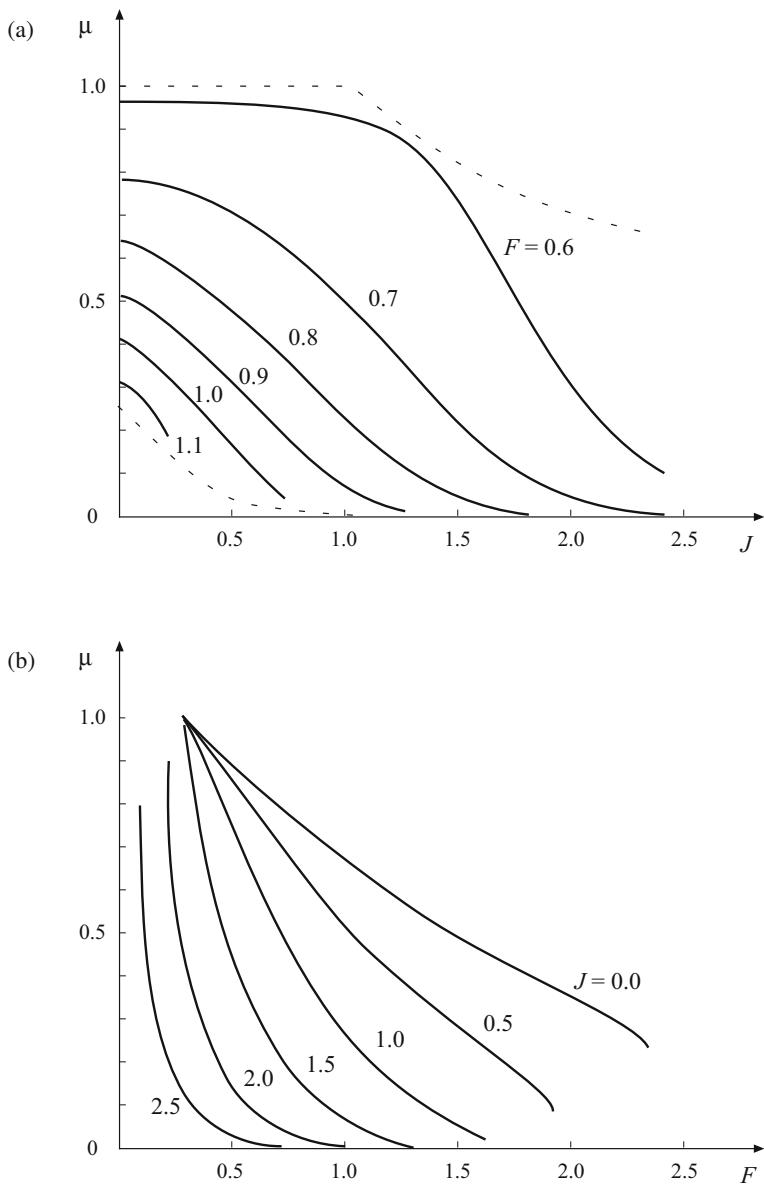
As usual, the conversion ratio is defined as  $\mu = V_2/V_1$ . The resulting peak transistor voltage for this typical design is approximately  $2.8 V_1$ , while the peak transistor current is  $2I_2$ . Hence, conduction losses are higher than in an equivalent PWM switch. The range of switch conversion ratios  $\mu$  is a function of the capacitor ratio  $C_d/C_s$ ; in a good design, values of  $\mu$  ranging from nearly one to nearly zero can be obtained, with a wide range of dc load currents and while maintaining zero-voltage switching.

Analysis and design charts for the ZVS MRS are given in [335–338]. Results for the typical choice  $C_d = 3C_s$  are plotted in Fig. 23.27. These plots illustrate how the switch conversion ratio  $\mu$  varies as a function of load current and switching frequency. Figure 23.27a also illustrates the boundary of zero-voltage switching: ZVS is lost for operation outside the dashed lines. Decreasing the ratio of  $C_d$  to  $C_s$  reduces the area of the ZVS region.

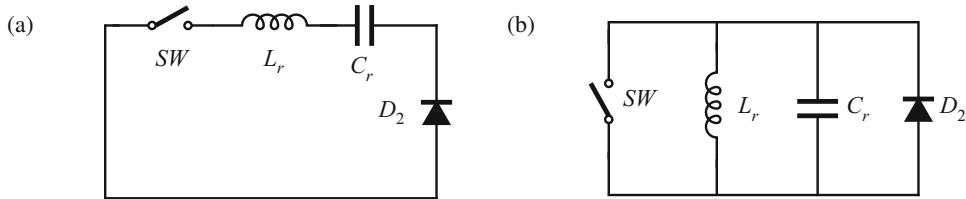
Other resonant converters in which all semiconductor devices operate with zero-voltage switching are known. Examples include some operating modes of the parallel and LCC resonant converters described in Chap. 22, as well as the class-E converters described in [340–342].

### 23.3.3 Quasi-Square-Wave Resonant Switches

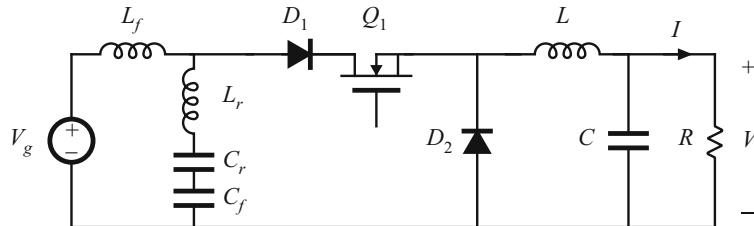
Another basic class of resonant switch networks is the quasi-square wave converters. Both zero-voltage switching and zero-current switching versions are known; the resonant tank networks



**Fig. 23.27** Conversion ratio  $\mu$  for the multiresonant switch with  $C_d = 3C_s$ : (a) conversion ratio  $\mu$  vs. normalized current  $J$  (solid lines: conversion ratio; dashed lines: boundaries of zero-voltage switching), (b) conversion ratio  $\mu$  vs. normalized switching frequency  $F$



**Fig. 23.28** Elimination of converter low-frequency elements reduces the quasi-resonant switch cells to these networks: (a) ZCS quasi-square-wave network, (b) ZVS quasi-square-wave network



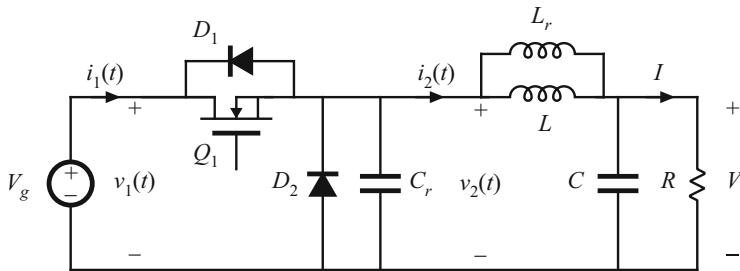
**Fig. 23.29** Incorporation of a ZCS quasi-square-wave resonant switch into a buck converter containing an  $L-C$  input filter

are illustrated in Fig. 23.28. In the network of Fig. 23.28a, all semiconductor devices are effectively in series with the tank inductor, and hence operate with zero-current switching. In the network of Fig. 23.28b, all semiconductor devices are effectively in parallel with the tank capacitor, and hence operate with zero-voltage switching.

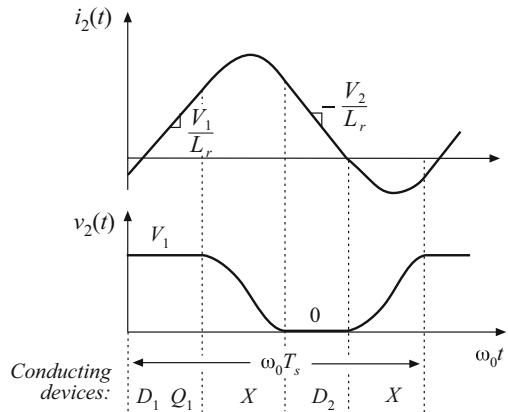
Figure 23.29 illustrates implementation of a zero current switching quasi-square wave resonant switch, in a buck converter with input filter. Elements  $L_f$  and  $C_f$  are large in value, and constitute a single-section  $L-C$  input filter. Elements  $L_r$  and  $C_r$  form the series resonant tank; these elements are placed in series with input filter capacitor  $C_f$ . Since  $C_r$  and  $C_f$  are connected in series, they can be combined into a single small-value capacitor. In this zero-current switching converter, the peak transistor current is identical to the peak transistor current of an equivalent PWM converter. However, the peak transistor blocking voltage is increased. The ZCS QSW resonant switch exhibits a switch conversion ratio  $\mu$  that is restricted to the range  $0 \leq \mu \leq 0.5$ . Analysis of this resonant switch is given in [343, 344].

A buck converter, containing a zero-voltage-switching quasi-square wave (ZVS QSW) resonant switch, is illustrated in Fig. 23.30. Typical waveforms are given in Fig. 23.31. Since the tank inductor  $L_r$  and the output filter inductor  $L$  are connected in parallel, these two elements can be combined into a single inductor having a small value nearly equal to  $L_r$ . Analyses of the ZVS QSW resonant switch are given in [70, 344, 345]. A related full-bridge converter is described in [328]. The ZVS QSW resonant switch is notable because zero-voltage switching is obtained in all semiconductor devices, yet the peak transistor voltage is identical to that of an equivalent PWM switch [343]. However, the peak transistor currents are increased.

Characteristics of the zero-voltage-switching quasi-square wave resonant switch are plotted in Fig. 23.32. The switch conversion ratio  $\mu = V_2/V_1$  is plotted as a function of normalized switching frequency  $F$  and normalized output current  $J$ , where these quantities are defined as



**Fig. 23.30** Incorporation of a ZVS quasi-square-wave resonant switch into a buck converter



**Fig. 23.31** Waveforms of the ZVS quasi-square-wave resonant switch converter of Fig. 23.30

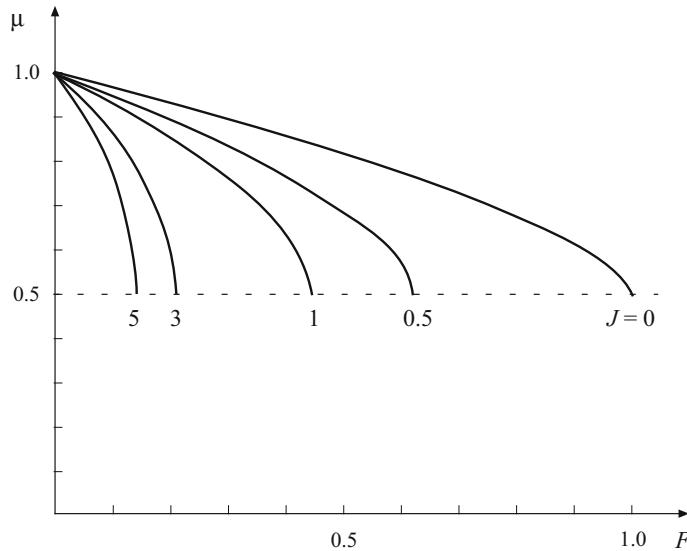
follows:

$$f_0 = \frac{1}{2\pi \sqrt{L_r C_r}} R_0 = \sqrt{\frac{L_r}{C_r}} \quad (23.66)$$

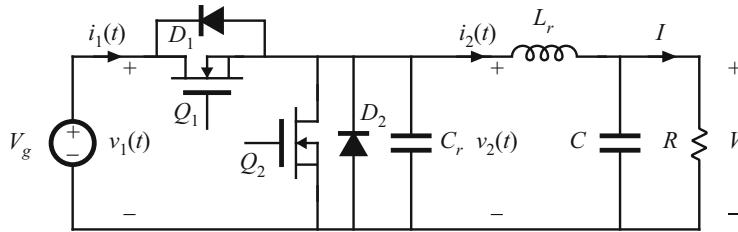
$$F = \frac{f_s}{f_0} \quad J = \frac{I_2 R_0}{V_1}$$

In addition, the zero-voltage-switching boundary is plotted. It can be seen that the requirement for zero-voltage switching limits the switch conversion ratio  $\mu$  to the range  $0.5 \leq \mu \leq 1$ . In consequence, the buck converter of Fig. 23.30 cannot produce output voltages less than  $0.5V_g$  without losing the ZVS property. A version which attains  $0 \leq \mu \leq 1$ , at the expense of increased transistor voltage stress, is described in [346]. In addition, the two-switch version of the ZVS QSW switch can operate with ZVS for  $\mu < 0.5$ .

A useful variant of the converter of Fig. 23.30 involves replacement of the diode with a synchronous rectifier, as illustrated in Fig. 23.33 [338, 339]. The second transistor introduces an additional degree of freedom in control of the converter, because this transistor can be allowed to conduct longer than the diode would otherwise conduct. This fact can be used to extend the region of zero-voltage switching to conversion ratios approaching zero, and also to operate the converter with constant switching frequency.



**Fig. 23.32** Characteristics of the ZVS quasi-square-wave resonant switch network: switch conversion ratio  $\mu$ , as a function of  $F$  and  $J$ . Dashed line: ZVS boundary

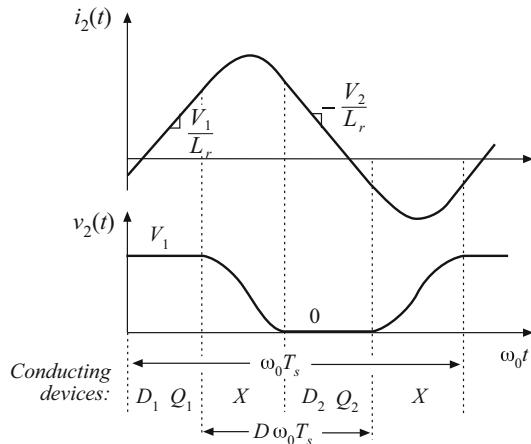


**Fig. 23.33** Quasi-square-wave ZVS buck converter containing a synchronous rectifier

Typical tank element waveforms for the circuit of Fig. 23.33 are illustrated in Fig. 23.34. These waveforms resemble those of the single switch case, Fig. 23.31, except that the tank current is negative while transistor  $Q_2$  conducts. The duty cycle  $D$  is defined with respect to the turn-off transitions of transistors  $Q_1$  and  $Q_2$ , as illustrated.

Characteristics of the two-switch QSW-ZVS switch network are plotted in Fig. 23.35, for the case of constant switching frequency at  $F = 0.5$ . The boundary of zero-voltage switching is also illustrated. Operation at a lower value of  $F$  causes the ZVS boundary to be extended to larger values of  $J$ , and to values of  $\mu$  that more closely approach the extreme values  $\mu = 0$  and  $\mu = 1$ .

To the extent that the commutation intervals can be neglected, one would expect that the switch conversion ratio  $\mu$  is simply equal to the duty cycle  $D$ . It can be seen from Fig. 23.35 that this is indeed the case. The characteristics are approximately horizontal lines, nearly independent of load current  $J$ .



**Fig. 23.34** Waveforms for the two-switch QSW-ZVS converter of Fig. 23.33

Zero-voltage switching quasi-square wave converters exhibit very low switching loss, because all semiconductor elements operate with zero-voltage switching. In the constant-frequency case containing a synchronous rectifier, the converter behavior is nearly the same as for the hard-switched PWM case, since  $\mu \approx D$ . The major disadvantage is the increased conduction loss, caused by the reversal of the inductor current.

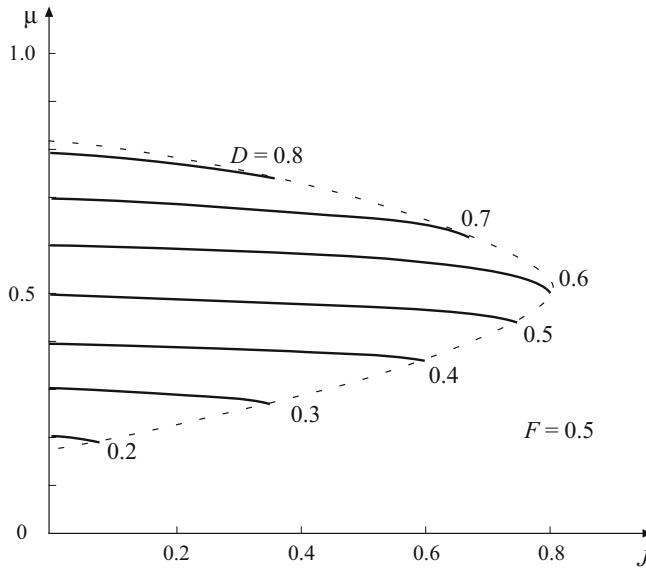
## 23.4 Soft Switching in PWM Converters

The quasi-square wave approach of the previous section is notable because it attains zero-voltage switching without increasing the peak voltage applied to the transistor. Several related soft-switching approaches have now become popular, which also attain zero-voltage switching without increasing the transistor peak voltage stress. In this section, popular zero-voltage switching versions of the full bridge, forward, and flyback converters, as well as the voltage-source inverter, are briefly discussed.

### 23.4.1 The Zero-Voltage Transition Full-Bridge Converter

It is possible to obtain soft switching in other types of converters as well. An example is the zero-voltage transition (ZVT) converter based on the full-bridge transformer-isolated buck converter, illustrated in Fig. 23.36 [324–327]. The transistor and diode output capacitances are represented in the figure by capacitances  $C_{leg}$ . Commutating inductor  $L_c$  is placed in series with the transformer; the net inductance  $L_c$  includes both transformer leakage inductance and the inductance of an additional discrete element. This inductor causes the full-bridge switch network to drive an effective inductive load, and results in zero-voltage switching of the primary-side semiconductor devices. Although the waveforms are not sinusoidal, it can nonetheless be said that the switch network output current  $i_c(t)$  lags the voltage  $v_s(t)$ , because the zero crossings of  $i_c(t)$  occur after the ZVS switching transitions are completed.

The output voltage is controlled via phase control. As illustrated in Fig. 23.37, both halves of the bridge switch network operate with a 50% duty cycle, and the phase difference between the half-bridge switch networks is controlled. The idealized waveforms of Fig. 23.37 neglect



**Fig. 23.35** Conversion ratio  $\mu$ , as a function of duty cycle  $D$  and normalized load current  $J$ , for the two-switch QSW-ZVS converter illustrated in Fig. 23.33. Curves are plotted for constant-frequency control with  $F = 0.5$ . The dashed line is the zero-voltage switching boundary

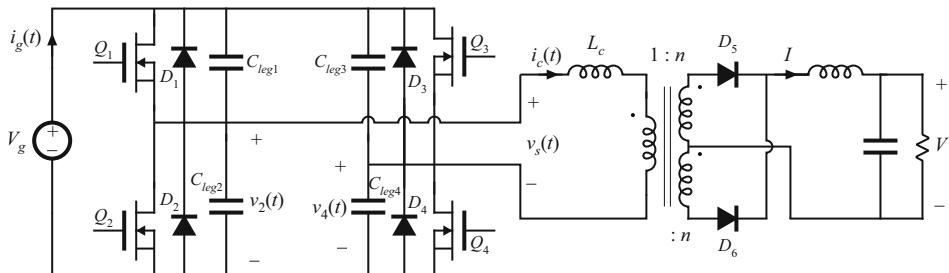
the switching transitions, and the subinterval numbers correspond to those of the more detailed Fig. 23.38. The phase-shift variable  $\phi$  lies in the range  $0 \leq \phi \leq 1$ , and assumes the role of the duty cycle  $d$  in this converter. The quantity  $\phi$  is defined as

$$\phi = \frac{(t_1 - t_0)}{\left(\frac{T_s}{2}\right)} \quad (23.67)$$

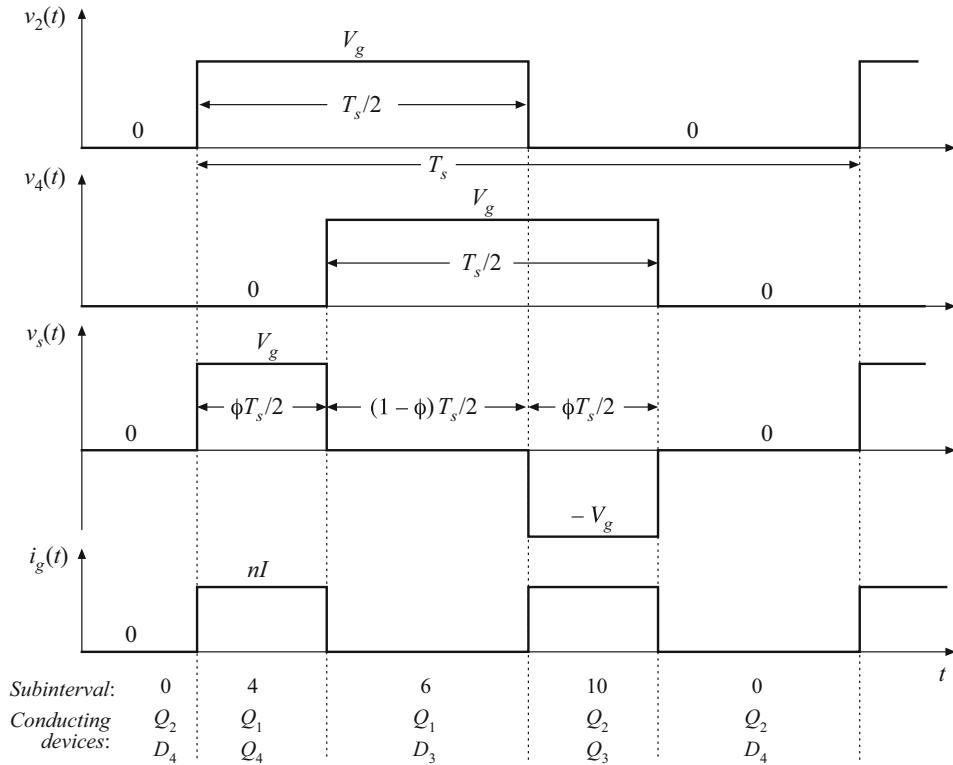
By volt-second balance on the secondary-side filter inductor, the conversion ratio  $M(\phi)$  is expressed as

$$M(\phi) = \frac{V}{V_g} = n\phi \quad (23.68)$$

This expression neglects the lengths of the switching transitions.



**Fig. 23.36** Zero-voltage transition converter, based on the full-bridge isolated buck converter



**Fig. 23.37** Phase-shift control of the ZVT full-bridge converter. Switching transitions are neglected in this figure, and subinterval numbering follows Fig. 23.38

Although the circuit appears symmetrical, the phase-shift control scheme introduces an asymmetry that causes the two half-bridge switch networks to behave quite differently during the switching transitions. During subintervals 4 and 10, energy is actively transmitted from the source  $V_g$  through the switches and transformer. These subintervals are initiated by the switching of the half-bridge network composed of the elements  $Q_1$ ,  $D_1$ ,  $Q_2$ , and  $D_2$ , called the “passive-to-active” (P-A) transition [326]. Subintervals 4 and 10 are terminated by the switching of the half-bridge network comprised by the elements  $Q_3$ ,  $D_3$ ,  $Q_4$ , and  $D_4$ , called the “active-to-passive” (A-P) transition.

The turn-on and turn-off switching processes of this converter are similar to the zero-voltage-switching turn-off process described in the previous section. Detailed primary-side waveforms are illustrated in Fig. 23.38. During subinterval 0,  $Q_2$  and  $D_4$  conduct. If the transformer magnetizing current  $i_M$  is negligible, then the commutating inductor current is given by  $i_c(t_0) = -nI$ , where  $I$  is the load current. The passive-to-active transition is initiated when transistor  $Q_2$  is turned off. The negative  $i_c$  then causes capacitors  $C_{leg1}$  and  $C_{leg2}$  to charge, increasing  $v_2(t)$ . During subinterval 1,  $L_c$ ,  $C_{leg1}$ , and  $C_{leg2}$  form a resonant network that rings with approximately sinusoidal waveforms. If sufficient energy was initially stored in  $L_c$ , then  $v_2(t)$  eventually reaches  $V_g$ , terminating subinterval 1. Diode  $D_1$  then clamps  $v_2(t)$  to  $V_g$  during subinterval 2. Transistor

$Q_1$  is turned on at zero voltage during subinterval 2; in practice, this is implemented by insertion of a small delay between the switching transitions of transistors  $Q_2$  and  $Q_1$ .

If  $L_c$  does not initially store sufficient energy to charge the total capacitance ( $C_{leg1} + C_{leg2}$ ) from  $v_2 = 0$  to  $v_2 = V_g$  during subinterval 1, then  $v_2(t)$  will never reach  $V_g$ . Switching loss will then occur when transistor  $Q_1$  is turned on. This situation typically occurs at light load, where  $I$  is small. Sometimes, the design engineer may choose to simply accept this power loss; after all, other losses such as conduction loss are small at light load. An alternative is to modify the circuit to increase the energy stored in  $L_c$  at  $t = t_0$  under light load conditions. One way to accomplish this is to increase the transformer magnetizing current  $i_M(t_0)$  to a significant level; at the beginning of subinterval 1,  $i_c$  is then equal to  $i_c(t_0) = -nI + i_M(t_0)$  with  $i_M(t_0) < 0$ . At light load where  $I$  is small, the magnetizing current maintains the required level of  $i_c$ .

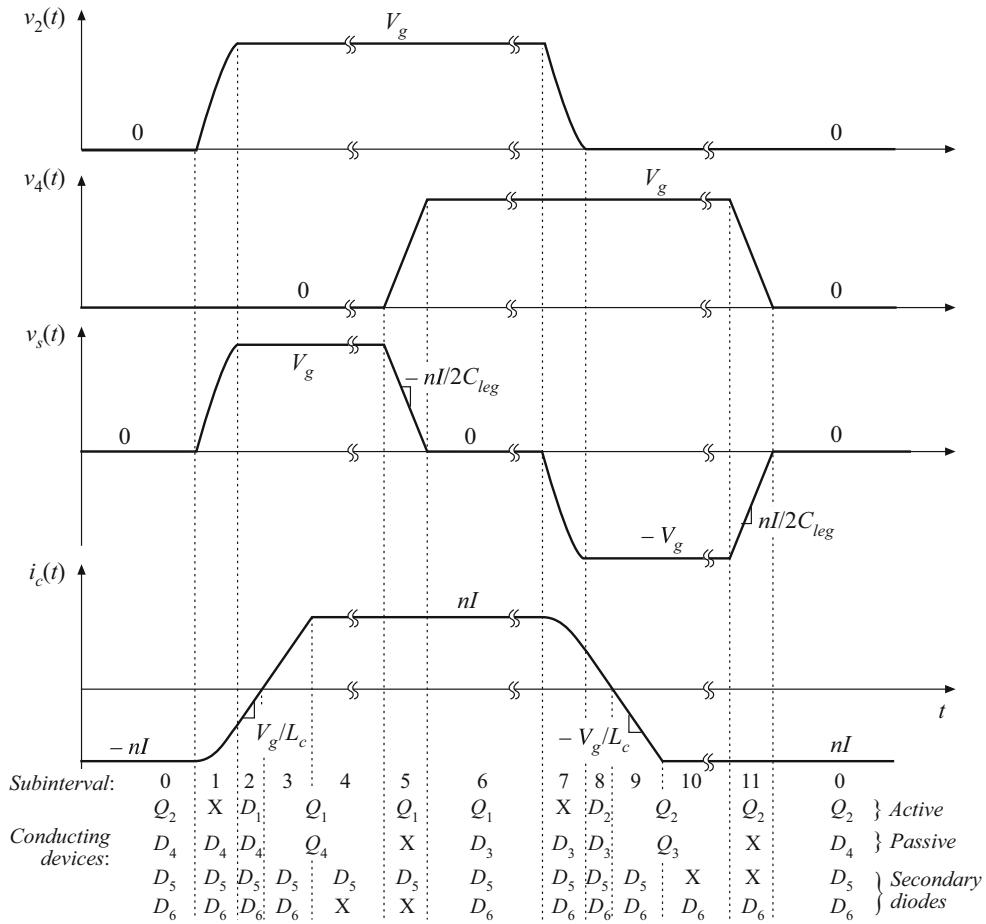
During subintervals 0, 1, 2, and 3, secondary-side diodes  $D_5$  and  $D_6$  both conduct; hence, zero voltage appears across all transformer windings. In consequence, voltage  $V_g$  is applied to commutating inductor  $L_c$  during subintervals 2 and 3, causing  $i_c(t)$  to increase with slope  $V_g/L_c$ . Current  $i_c(t)$  reaches zero at the end of subinterval 2, and increases to the positive value  $+nI$  at the end of subinterval 3. The reversal of polarity of  $i_c(t)$  enables zero-voltage switching during the next switching transitions, subinterval 5 and subintervals 7–9.

At the end of subinterval 3, the current in diode  $D_6$  has decreased to zero.  $D_6$  then becomes reverse-biased, with zero-current switching. At this instant, diode  $D_6$  must begin to block voltage  $2nV_g$ . The output capacitance of  $D_6$  prevents the voltage from changing immediately to  $2nV_g$ ; instead, the resonant circuit formed by  $L_c$  and the  $D_6$  output capacitance begins to ring in a manner similar to Fig. 4.76. Peak  $D_6$  voltages are typically observed that are considerably in excess of  $2nV_g$ , and it is usually necessary to add voltage-clamp snubbers that prevent the secondary-side diode voltages from exceeding a safe value. Several dissipative and non-dissipative approaches are discussed in [325–327].

The active-to-passive switching transition occurs during subinterval 5. This subinterval is initiated when transistor  $Q_4$  is turned off. The positive current  $i_c(t_1)$  is equal to the reflected load current  $nI$ , and charges capacitors  $C_{leg3}$  and  $C_{leg4}$  from  $v_4 = 0$  to  $v_4 = V_g$ . Subinterval 5 ends when  $v_4$  reaches  $V_g$ ; Diode  $D_3$  then becomes forward-biased. Transistor  $Q_3$  is then turned on during subinterval 6, with zero-voltage switching. This is typically implemented by insertion of a small delay between the switching of transistors  $Q_4$  and  $Q_3$ . Because  $i_c$  is constant and equal to  $nI$  during subinterval 5, the active-to-passive transition maintains zero-voltage switching at all load currents.

Circuit behavior during the next half switching period, comprising subintervals 6 to 11, is symmetrical and therefore similar to the behavior observed during subintervals 0 to 5. The switching transitions of transistors  $Q_1$  and  $Q_2$  are passive-to-active transitions, and occur with zero-voltage switching provided that sufficient energy is stored in  $L_c$  as described above. The switching transitions of  $Q_3$  and  $Q_4$  are active-to-passive, and occur with zero-voltage switching at all loads.

The zero-voltage transition converter exhibits low primary-side switching loss and generated EMI. Conduction loss is increased with respect to an ideal PWM full-bridge topology, because of the current  $i_c$  that circulates through the primary-side semiconductors during subintervals 0 and 6. However, this increase in conduction loss can be small if the range of input voltage variations is narrow. This soft-switching approach has now found commercial success.

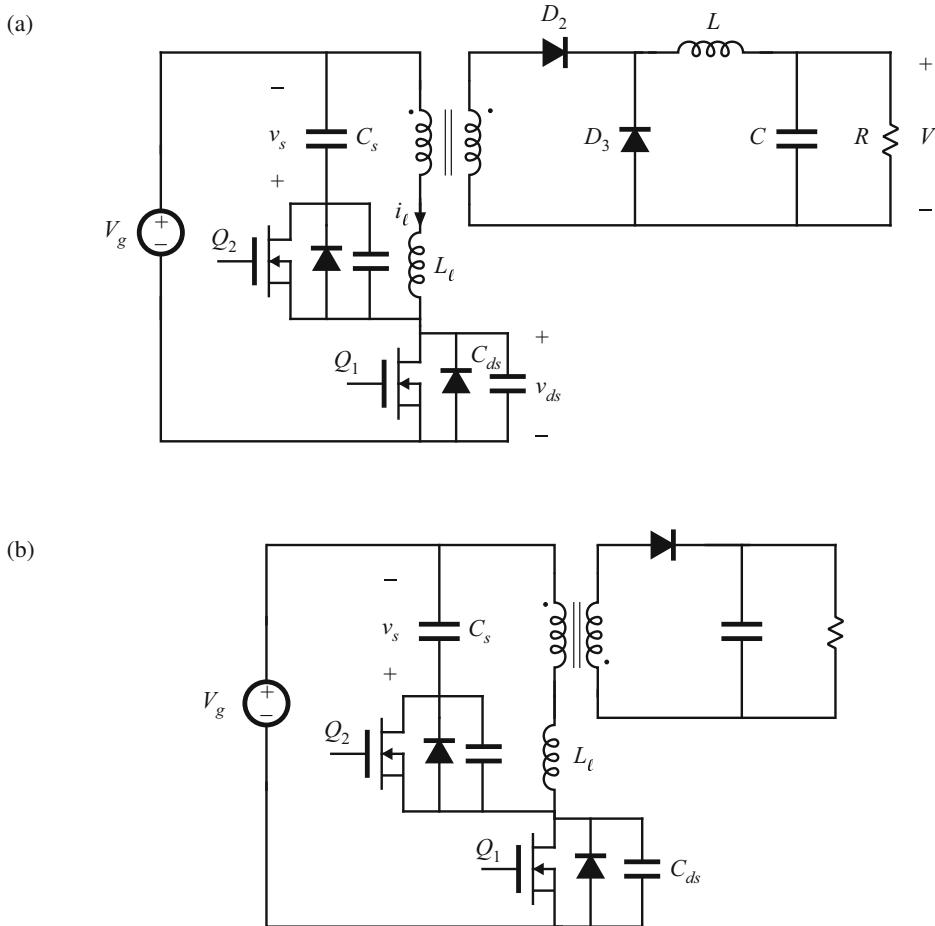


**Fig. 23.38** Detailed diagram of primary-side waveforms of the ZVT full-bridge converter, illustrating the zero-voltage switching mechanisms. An ideal transformer is assumed

### 23.4.2 The Auxiliary Switch Approach

A similar approach can be used in forward, flyback, and other transformer-isolated converters. As illustrated in Fig. 23.39, an “active-clamp snubber” network consisting of a capacitor and auxiliary MOSFET  $Q_2$  is added, that is effectively in parallel with the original power transistor  $Q_1$  [350]. The MOSFET body diodes and output drain-to-source capacitances, as well as the transformer leakage inductance  $L_\ell$ , participate in the circuit operation. These elements lead to zero-voltage switching, with waveforms similar to those of the ZVT full-bridge converter of Sect. 23.4.1 or the two-transistor QSW-ZVS switch of Sect. 23.3.3. The transistors are driven by complementary signals; for example, after turning off  $Q_1$ , the controller waits for a short delay time and then turns on  $Q_2$ .

The active-clamp snubber can be viewed as a voltage-clamp snubber, similar to the dissipative snubber illustrated in Fig. 23.6. However, the snubber contains no resistor; instead, MOS-



**Fig. 23.39** Active-clamp snubber circuits: (a) forward converter, (b) flyback converter

FET  $Q_2$  allows bidirectional power flow, so that the energy stored in capacitor  $C_s$  can flow back into the converter.

The voltage  $v_s$  can be found by volt-second inductance on the transformer magnetizing inductance. If the lengths of the commutation intervals are neglected, and if the voltage ripple in  $v_s(t)$  can be neglected, then one finds that

$$V_s = \frac{D}{D'} V_g \quad (23.69)$$

The voltage  $v_s$  is effectively an unloaded output of the converter. With the two-quadrant switch provided by  $Q_2$ , this output operates in continuous conduction mode with no load, and hence the peak voltage of  $Q_1$  is clamped to the minimum level necessary to balance the volt-seconds applied to the transformer magnetizing inductance.

Typical waveforms for a forward converter incorporating an active-clamp snubber are illustrated in Fig. 23.40. The current  $i_t(t)$  reverses direction while  $Q_2$  conducts. When  $Q_2$  turns

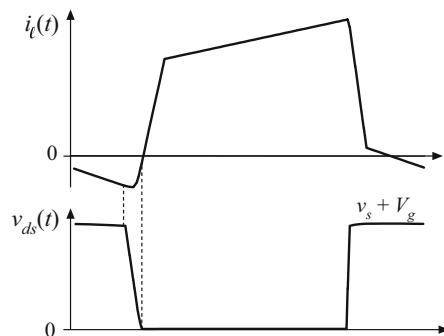
off, capacitor  $C_{ds}$  begins to discharge. When  $v_{ds}$  reaches zero, the body diode of  $Q_1$  becomes forward-biased.  $Q_1$  can then be turned on at zero voltage.

An added benefit of the active-clamp snubber, when used in a forward converter, is that it resets the transformer. Consequently, the converter can operate at any duty cycle, including duty cycles greater than 50%. When the converter must operate with a wide range of input voltages, this can allow substantial improvements in transistor stresses and efficiency. The MOSFETs in Fig. 23.39 operate with zero-voltage switching, while the secondary-side diodes operate with zero-current switching.

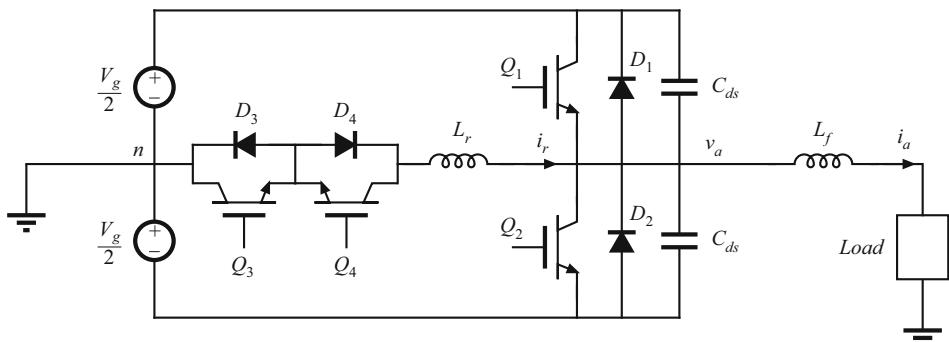
This approach is quite versatile, and similar auxiliary circuits can be added to other converter circuits to obtain zero-voltage switching [351–353].

### 23.4.3 Auxiliary Resonant Commutated Pole

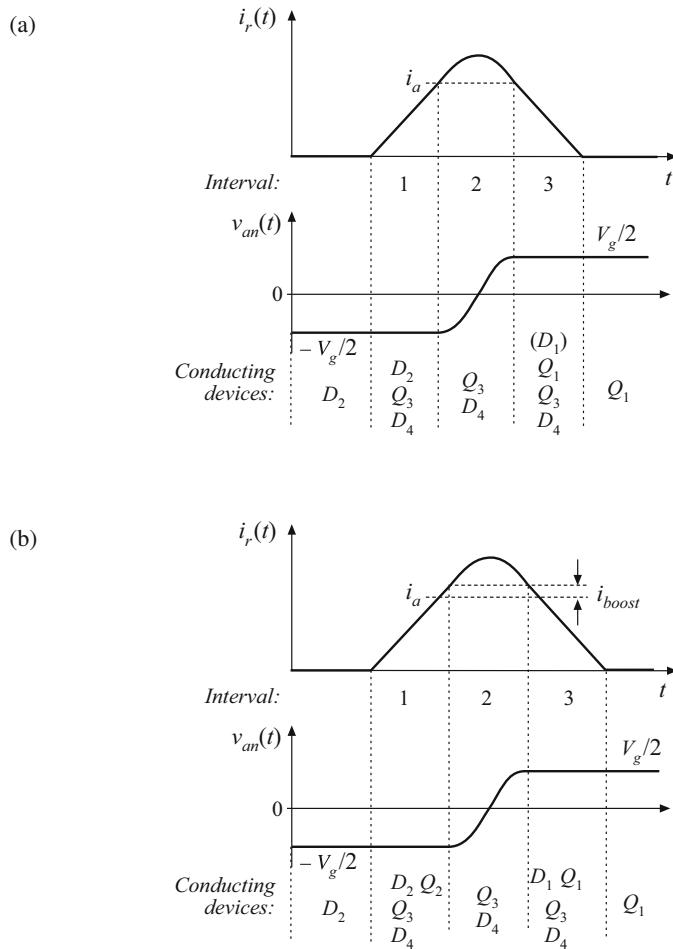
The auxiliary resonant commutated pole (ARCP) is a related circuit that uses an auxiliary four-quadrant switch (or two equivalent two-quadrant switches) to obtain soft switching in the transistors of a bridge inverter circuit [354–356]. This approach finds application in dc–ac inverter circuits. Figure 23.41 illustrates a half-bridge circuit, or one phase of a three-phase voltage-source inverter, driving an ac load. This circuit can lead to zero-voltage switching that mitigates the switching loss induced by the reverse recovery of diodes  $D_1$  and  $D_2$ . Filter inductor  $L_f$  is relatively large, so that the output current  $i_a(t)$  is essentially constant during the resonant com-



**Fig. 23.40** Waveforms of the active-clamp snubber circuit of Fig. 23.39a



**Fig. 23.41** Half-bridge circuit driving an ac load, with ARCP zero-voltage switching



**Fig. 23.42** Waveforms of the ARCP circuit of Fig. 23.41: (a) basic waveforms, (b) with current boost

mutation interval. Capacitors  $C_{ds}$  are relatively small, and model the output capacitances of the semiconductor devices. Inductor  $L_r$  is also relatively small, and elements  $L_r$  and  $C_{ds}$  form a resonant circuit that rings during part of the commutation process. Semiconductor switching devices  $Q_3, Q_4, D_3$ , and  $D_4$  form an auxiliary four-quadrant switch that turns on to initiate the resonant commutation process.

Typical commutation waveforms are illustrated in Fig. 23.42a, for the case in which the ac load current  $i_a$  is positive. Diode  $D_2$  is initially conducting the output current  $i_a$ . It is desired to turn off  $D_2$  and turn on  $Q_1$ , with zero-voltage switching. This is accomplished with the following sequence:

- Interval 1. Turn on transistor  $Q_3$ . Devices  $D_2$ ,  $Q_3$ , and  $D_4$  conduct.
- Interval 2. When the current in  $D_2$  reaches zero,  $D_2$  turns off. A resonant ringing interval occurs.
- Interval 3. When the voltage  $v_{an}$  reaches  $V_g/2$ , diode  $D_1$  begins to become forward-biased. Transistor  $Q_1$  is then immediately turned on at zero voltage.

At the conclusion of interval 3,  $i_r(t)$  reaches zero and diode  $D_3$  turns off. For negative current, the process for commutation of diode  $D_1$  is similar, except that transistor  $Q_4$  and diode  $D_3$  conduct the resonant current  $i_r(t)$ .

One issue related to the waveforms of Fig. 23.42a is that the circuit always operates at the boundary of zero-voltage switching. At the end of interval 2, diode  $D_1$  is not actually forward-biased, because its current never actually becomes positive. Instead, transistor  $Q_1$  should be turned on at the beginning of interval 3. If transistor  $Q_1$  is gated on late, then the continued ringing will cause voltage  $v_{an}(t)$  to decrease, and zero-voltage switching will be lost.

To further assist in the zero-voltage switching commutation process, transistor  $Q_2$  can be turned on while  $D_2$  conducts, as illustrated in Fig. 23.42b. Transistor  $Q_2$  is used to lengthen the duration of interval 1: now, when the current  $i_r(t)$  exceeds current  $i_a$  by an amount  $i_{boost}$ , then the controller turns off  $Q_2$  to end interval 1. This causes diode  $D_1$  to become forward-biased during the beginning of interval 3. Transistor  $Q_1$  is then turned on with zero-voltage switching, while  $D_1$  is conducting.

Regardless of whether the circuit operates with the waveforms of Fig. 23.42a or b, the ARCP approach eliminates the switching loss caused by the reverse recovery of diodes  $D_1$  and  $D_2$ . Unlike the previous circuits of this chapter, the ARCP has no circulating currents that cause conduction loss, because the tank inductor current  $i_r(t)$  is nonzero only in the vicinity of the commutation interval. The approach of Fig. 23.42a does not completely eliminate the loss caused by the device output capacitances. This loss is eliminated using the current boost of Fig. 23.42b, but additional conduction loss is incurred because of the increased peak  $i_r(t)$ . The waveforms of Fig. 23.42b may, in fact, lead to reduced efficiency relative to Fig. 23.42a!

## 23.5 Summary of Key Points

1. In a resonant switch converter, the switch network of a PWM converter is replaced by a switch network containing resonant elements. The resulting hybrid converter combines the properties of the resonant switch network and the parent PWM converter.
2. Analysis of a resonant or soft-switching switch cell involves determination of the switch conversion ratio  $\mu$ . The resonant switch waveforms are determined, and are then averaged. The switch conversion ratio  $\mu$  is a generalization of the PWM CCM duty cycle  $d$ . The results of the averaged analysis of PWM converters operating in CCM can be directly adapted to the related resonant switch converter, simply by replacing  $d$  with  $\mu$ .
3. In the zero-current-switching quasi-resonant switch, diode  $D_2$  operates with zero-voltage switching, while transistor  $Q_1$  and diode  $D_1$  operate with zero-current switching. In the zero-voltage-switching quasi-resonant switch, the transistor  $Q_1$  and diode  $D_1$  operate with zero-voltage switching, while diode  $D_2$  operates with zero-current switching.
4. In the zero-voltage-switching multiresonant switch, all semiconductor devices operate with zero-voltage switching. In consequence, very low switching loss is observed.

5. In the quasi-square-wave zero-voltage-switching resonant switches, all semiconductor devices operate with zero-voltage switching, and with peak voltages equal to those of the parent PWM converter. The switch conversion ratio is restricted to the range  $0.5 \leq \mu \leq 1$ . Versions containing synchronous rectifiers can operate with values of  $\mu$  approaching zero.
6. The zero-voltage transition approach, as well as the active-clamp snubber approach, lead to zero-voltage switching of the transistors and zero-current switching of the diodes. These approaches have been successful in substantially improving the efficiencies of transformer-isolated converters. The auxiliary resonant commutated pole induces zero-voltage switching in bridge circuits such as the voltage-source inverter.

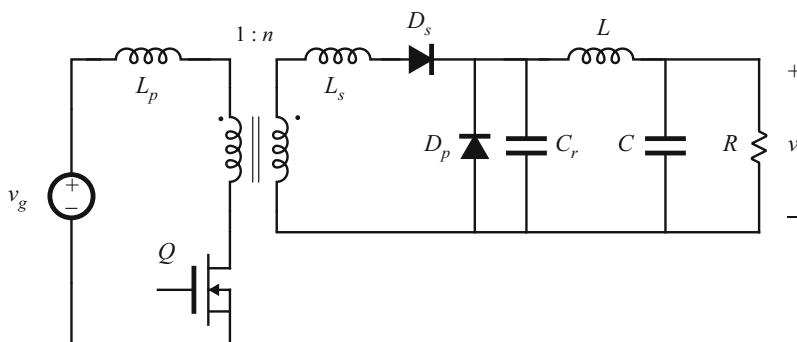
## PROBLEMS

**23.1** In the forward converter of Fig. 23.43,  $L$  and  $C$  are large filter elements while  $L_p$ ,  $L_s$ , and  $C_r$  have relatively small values. The transformer reset mechanism is not shown; for this problem, you may assume that the transformer is ideal.

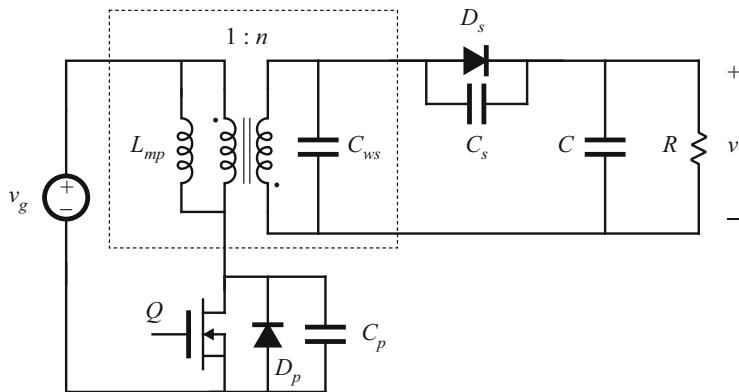
- (a) Classify the resonant switch.
- (b) Which semiconductor devices operate with zero-voltage switching? With zero-current switching?
- (c) What is the resonant frequency?

**23.2** In the high-voltage converter of Fig. 23.44, capacitor  $C$  is relatively large in value. The transformer model includes an ideal  $1:n$  transformer, in conjunction with magnetizing inductance  $L_{mp}$  (referred to the primary side) and winding capacitance  $C_{ws}$  (referred to the secondary side). Transistor  $Q$  and diode  $D_p$  exhibit total output capacitance  $C_p$ , while the output capacitance of diode  $D_s$  is  $C_s$ . Other nonidealities, such as transformer leakage inductance, can be ignored. The resonant switch is well-designed, such that all elements listed above contribute to ideal operation of the converter and resonant switch.

- (a) What type of resonant switch is employed? What is the parent PWM converter?
- (b) Which semiconductor devices operate with zero-voltage switching? With zero-current switching?



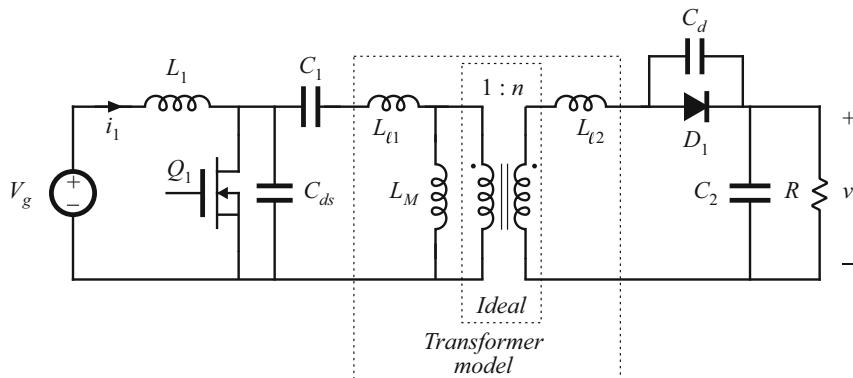
**Fig. 23.43** Forward converter with resonant switch, Problem 23.1



**Fig. 23.44** High-voltage dc-dc converter containing a resonant switch network, Problem 23.2

- (c) What is the tank resonant frequency?
- (d) Sketch the waveforms of the transistor drain-to-source voltage and transformer magnetizing current.

**23.3** In the transformer-isolated dc-dc converter of Fig. 23.45, capacitors  $C_1$  and  $C_2$  and inductors  $L_1$  and  $L_M$  are relatively large in value, so that they have small switching ripples. The transformer model includes an ideal  $1:n$  transformer, in conjunction with magnetizing inductance  $L_M$  (referred to the primary side) and leakage inductances  $L_{t1}$  and  $L_{t2}$  as shown. Transistor  $Q_1$  exhibits output capacitances  $C_{ds}$ , while the output capacitance of diode  $D_1$  is  $C_d$ . MOSFET  $Q_1$  contains a body diode (not explicitly shown). Other nonidealities can be ignored. The resonant switch is well-designed, such that all elements listed above contribute to ideal operation of the converter and resonant switch.



**Fig. 23.45** Transformer-isolated dc-dc converter containing a resonant switch network, Problem 23.3

- (a) What type of resonant switch is employed? What is the parent PWM converter?
- (b) Which semiconductor devices operate with zero-voltage switching? With zero-current switching?

**23.4** A buck-boost converter is realized using a half-wave ZCS quasi-resonant switch. The load resistance has value  $R$ , the input voltage has value  $V_g$ , and the converter switching frequency is  $f_s$ .

- (a) Sketch the circuit schematic.
- (b) Write the complete system of equations that can be solved to determine the output voltage  $V$ , in terms of the quantities listed above and the component values. It is not necessary to actually solve your equations. You may also quote results listed in this textbook.

**23.5** It is desired to design a half-wave zero-current-switching quasi-resonant forward converter to operate with the following specifications:  $V_g = 320\text{ V}$ ,  $V = 42\text{ V}$ ,  $5\text{ W} \leq P \leq 100\text{ W}$ . Design the converter to operate with a maximum switching frequency of 1 MHz and a switch conversion ratio of  $\mu = 0.45$ . Attempt to minimize the peak transistor current, while maintaining zero-current switching at all operating points. You may neglect the transformer magnetizing current, and ignore the transformer reset scheme.

- (a) Specify your choices for the turns ratio  $n$ , and the tank elements  $L_r$  and  $C_r$ , referred to the transformer secondary side.
- (b) For your design of part (a), what is the minimum switching frequency?
- (c) What is the worst-case peak transistor current?

**23.6** Analysis of the ZVS quasi-resonant switch of Fig. 23.24.

- (a) For each subinterval, sketch the resonant switch cell circuit, and derive expressions for the tank inductor current and capacitor voltage waveforms.
- (b) For subinterval 2, in which  $Q_1/D_1$  are off and  $D_2$  conducts, write the loop equation which relates the tank capacitor voltage, tank inductor voltage, and any other network voltages as appropriate. Hence, for subinterval 2 relate the integral of the tank capacitor voltage to the change in tank inductor current.
- (c) Determine the switch network terminal-waveform average values, and hence derive an expression for the switch conversion ratio  $\mu$ . Verify that your result coincides with Eq. (23.61).

**23.7** Analysis of the full-bridge zero-voltage transition converter of Sect. 23.4.1. The converter of Fig. 23.36 operates with the waveforms illustrated in Fig. 23.38. According to Eq. (23.68), the conversion ratio of this converter is given approximately by  $M(\phi) = n\phi$ . Derive an exact expression for  $M$ , based on the waveforms given in Fig. 23.38. Your result should be a function of the length of subinterval 4, the load current, the switching frequency, and the values of the inductance and capacitances. *Note:* there is a reasonably simple answer to this question.

# A

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## RMS Values of Commonly Observed Converter Waveforms

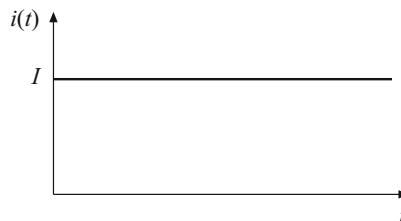
The waveforms encountered in power electronics converters can be quite complex, containing modulation at the switching frequency and often also at the ac line frequency. During converter design, it is often necessary to compute the rms values of such waveforms. In this appendix, several useful formulas and tables are developed which allow these rms values to be quickly determined.

RMS values of the doubly modulated waveforms encountered in PWM rectifier circuits are discussed in Sect. 21.5.

### A.1 Some Common Waveforms

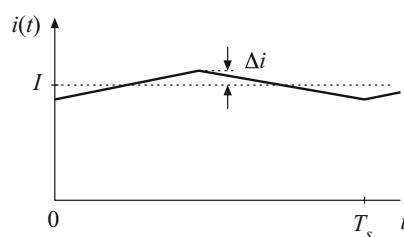
DC:

$$rms = I \quad (\text{A.1})$$



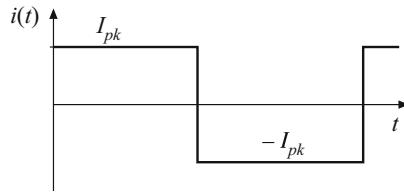
DC plus linear ripple:

$$rms = I \sqrt{1 + \frac{1}{3} \left( \frac{\Delta i}{I} \right)^2} \quad (\text{A.2})$$



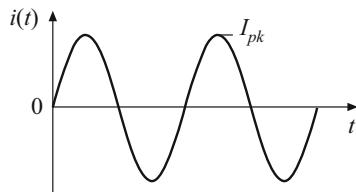
Square wave:

$$rms = I_{pk} \quad (A.3)$$



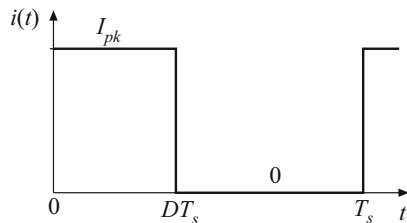
Sine wave:

$$rms = \frac{I_{pk}}{\sqrt{2}} \quad (A.4)$$



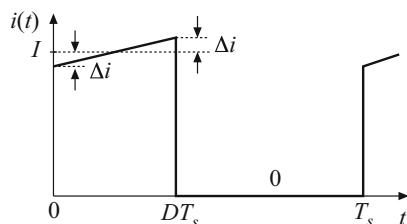
Pulsating waveform:

$$rms = I_{pk} \sqrt{D} \quad (A.5)$$



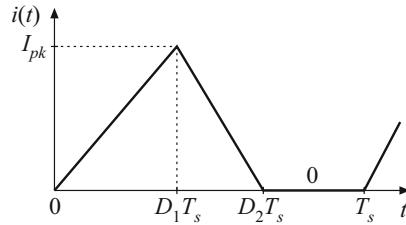
Pulsating waveform with linear ripple:

$$rms = I \sqrt{D} \sqrt{1 + \frac{1}{3} \left( \frac{\Delta i}{I} \right)^2} \quad (A.6)$$



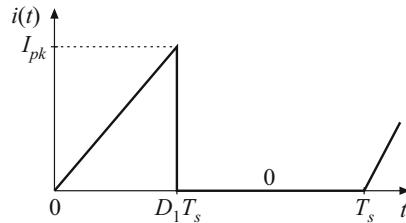
Triangular waveform:

$$rms = I_{pk} \sqrt{\frac{D_1 + D_2}{3}} \quad (\text{A.7})$$



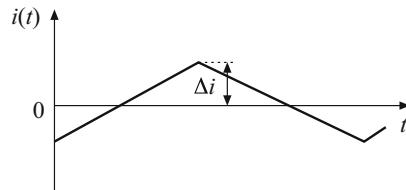
Triangular waveform:

$$rms = I_{pk} \sqrt{\frac{D_1}{3}} \quad (\text{A.8})$$



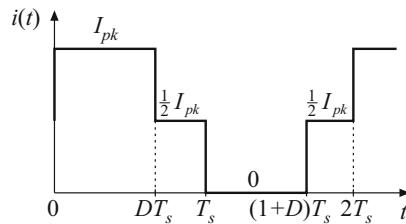
Triangular waveform, no dc component:

$$rms = \frac{\Delta i}{\sqrt{3}} \quad (\text{A.9})$$



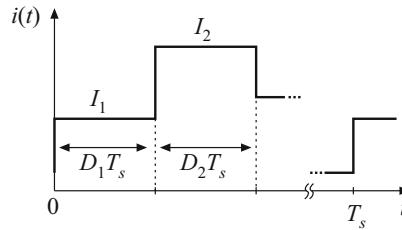
Center-tapped bridge winding waveform:

$$rms = \frac{1}{2} I_{pk} \sqrt{1 + D} \quad (\text{A.10})$$

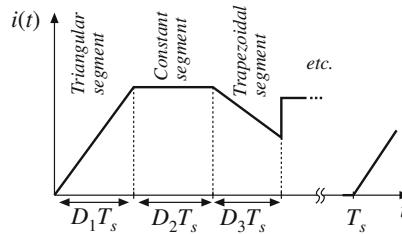


General stepped waveform:

$$rms = \sqrt{D_1 I_1^2 + D_2 I_2^2 + \dots} \quad (A.11)$$



## A.2 General Piecewise Waveform



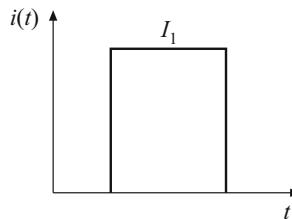
For a periodic waveform composed of  $n$  piecewise segments as shown above, the rms value is

$$rms = \sqrt{\sum_{k=1}^n D_k u_k} \quad (A.12)$$

where  $D_k$  is the duty cycle of segment  $k$ , and  $u_k$  is the contribution of segment  $k$ . The  $u_k$ s depend on the shape of the segments—several common segment shapes are listed below.

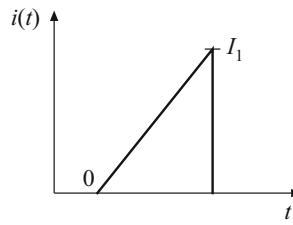
Constant segment:

$$u_k = I_1^2 \quad (A.13)$$



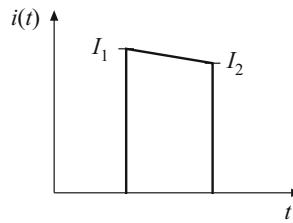
Triangular segment:

$$u_k = \frac{1}{3} I_1^2 \quad (\text{A.14})$$



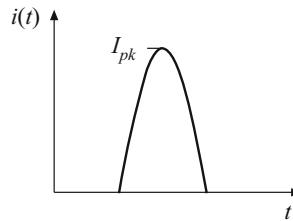
Trapezoidal segment:

$$u_k = \frac{1}{3} (I_1^2 + I_1 I_2 + I_2^2) \quad (\text{A.15})$$



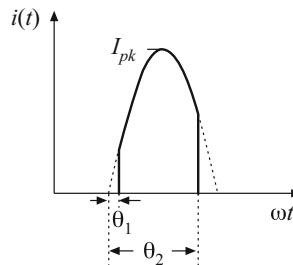
Sinusoidal segment, half or full period:

$$u_k = \frac{1}{2} I_{pk}^2 \quad (\text{A.16})$$

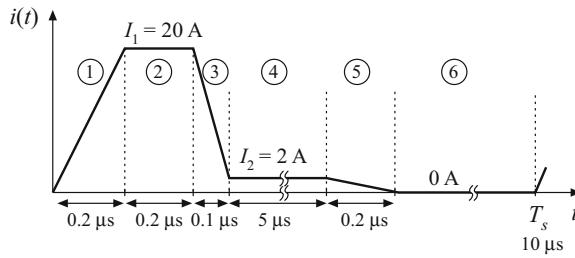


Sinusoidal segment, partial period: a sinusoidal segment of less than one half-period, which begins at angle  $\theta_1$  and ends at angle  $\theta_2$ . The angles  $\theta_1$  and  $\theta_2$  are expressed in radians:

$$u_k = \frac{1}{2} I_{pk}^2 \left( 1 - \frac{\sin(\theta_2 - \theta_1) \cos(\theta_2 + \theta_1)}{(\theta_2 - \theta_1)} \right) \quad (\text{A.17})$$



*Example*



A transistor current waveform contains a current spike due to the stored charge of a free-wheeling diode. The observed waveform can be approximated as shown above. Estimate the rms current.

The waveform can be divided into six approximately linear segments, as shown. The  $D_k$  and  $u_k$  for each segment are

1. Triangular segment:

$$D_1 = (0.2\mu s)/(10\mu s) = 0.02$$

$$u_1 = I_1^2/3 = (20A)^2/3 = 133A^2$$

2. Constant segment:

$$D_2 = (0.2\mu s)/(10\mu s) = 0.02$$

$$u_2 = I_1^2 = (20A)^2 = 400A^2$$

3. Trapezoidal segment:

$$D_3 = (0.1\mu s)/(10\mu s) = 0.01$$

$$u_3 = (I_1^2 + I_2^2 + I_3^2)/3 = 148A^2$$

4. Constant segment:

$$D_4 = (5\mu s)/(10\mu s) = 0.5$$

$$u_4 = I_2^2 = (2A)^2 = 4A^2$$

5. Triangular segment:

$$D_5 = (0.2\mu s)/(10\mu s) = 0.02$$

$$u_5 = I_2^2/3 = (2A)^2/3 = 1.3A^2$$

6. Zero segment:

$$u_6 = 0$$

The rms value is

$$rms = \sqrt{\sum_{k=1}^6 D_k u_k} = 3.76A \quad (A.18)$$

Even though its duration is very short, the current spike has a significant impact on the rms value of the current—without the current spike, the rms current is approximately 2.0 A.

## B

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### Magnetics Design Tables

Geometrical data for several standard ferrite core shapes are listed here. The geometrical constant  $K_g$  is a measure of core size, useful for designing inductors and transformers that attain a given copper loss [99]. The  $K_g$  method for inductor design is described in Chap. 11.  $K_g$  is defined as

$$K_g = \frac{A_c^2 W_A}{MLT} \quad (\text{B.1})$$

where  $A_c$  is the core cross-sectional area,  $W_A$  is the window area, and  $MLT$  is the winding mean-length-per-turn. The geometrical constant  $K_{gfe}$  is a similar measure of core size, which is useful for designing ac inductors and transformers when the total copper plus core loss is constrained. The  $K_{gfe}$  method for magnetics design is described in Chap. 12.  $K_{gfe}$  is defined as

$$K_{gfe} = \frac{W_A A_c^{2(1-1/\beta)}}{MLT \ell_m^{2/\beta}} u(\beta) \quad (\text{B.2})$$

where  $\ell_m$  is the core mean magnetic path length, and  $\beta$  is the core loss exponent:

$$P_{fe} = K_{fe} B_{max}^\beta \quad (\text{B.3})$$

For modern ferrite materials,  $\beta$  typically lies in the range 2.6 to 2.8. The quantity  $u(\beta)$  is defined as

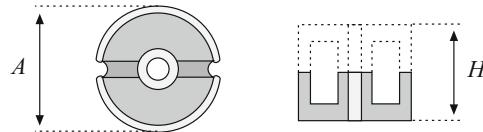
$$u(\beta) = \left[ \left( \frac{\beta}{2} \right)^{-\left( \frac{\beta}{\beta+2} \right)} + \left( \frac{\beta}{2} \right)^{\left( \frac{2}{\beta+2} \right)} \right]^{-\left( \frac{\beta+2}{\beta} \right)} \quad (\text{B.4})$$

$u(\beta)$  is equal to 0.305 for  $\beta = 2.7$ . This quantity varies by roughly 5% over the range  $2.6 \leq \beta \leq 2.8$ . Values of  $K_{gfe}$  are tabulated for  $\beta = 2.7$ ; variation of  $K_{gfe}$  over the range  $2.6 \leq \beta \leq 2.8$  is typically quite small.

Thermal resistances are listed in those cases where published manufacturer's data are available. The thermal resistances listed are the approximate temperature rise from the center leg of the core to ambient, per watt of total power loss. Different temperature rises may be observed under conditions of forced air cooling, unusual power loss distributions, etc. Listed window areas are the winding areas for conventional single-section bobbins.

An American Wire Gauge table is included at the end of this appendix.

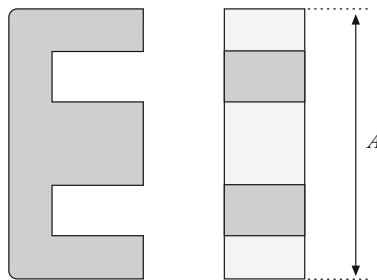
## B.1 Pot Core Data



**Fig. B.1** Pot core

Core type (AH) (mm)	Geometrical constant $K_g$ cm <sup>5</sup>	Geometrical constant $K_{gfe}$ cm <sup>x</sup>	Cross-sectional area $A_c$ (cm <sup>2</sup> )	Bobbin winding area $W_A$ (cm <sup>2</sup> )	Mean length per turn $MLT$ (cm)	Magnetic path length $\ell_m$ (cm)	Thermal resistance $R_{th}$ (°C/W)	Core weight (g)
704	$0.738 \cdot 10^{-6}$	$1.61 \cdot 10^{-6}$	0.070	$0.22 \cdot 10^{-3}$	1.46	1.0		0.5
905	$0.183 \cdot 10^{-3}$	$256 \cdot 10^{-6}$	0.101	0.034	1.90	1.26		1.0
1107	$0.667 \cdot 10^{-3}$	$554 \cdot 10^{-6}$	0.167	0.055	2.30	1.55		1.8
1408	$2.107 \cdot 10^{-3}$	$1.1 \cdot 10^{-3}$	0.251	0.097	2.90	2.00	100	3.2
1811	$9.45 \cdot 10^{-3}$	$2.6 \cdot 10^{-3}$	0.433	0.187	3.71	2.60	60	7.3
2213	$27.1 \cdot 10^{-3}$	$4.9 \cdot 10^{-3}$	0.635	0.297	4.42	3.15	38	13
2616	$69.1 \cdot 10^{-3}$	$8.2 \cdot 10^{-3}$	0.948	0.406	5.28	3.75	30	20
3019	0.180	$14.2 \cdot 10^{-3}$	1.38	0.587	6.20	4.50	23	34
3622	0.411	$21.7 \cdot 10^{-3}$	2.02	0.748	7.42	5.30	19	57
4229	1.15	$41.1 \cdot 10^{-3}$	2.66	1.40	8.60	6.81	13.5	104

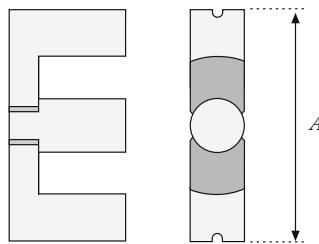
## B.2 EE Core Data



**Fig. B.2** EE core

Core type (A) (mm)	Geometrical constant $K_g$ (cm <sup>5</sup> )	Geometrical constant $K_{gfe}$ (cm <sup>x</sup> )	Cross-sectional area $A_c$ (cm <sup>2</sup> )	Bobbin area $W_A$ (cm <sup>2</sup> )	Mean length per turn $MLT$ (cm)	Magnetic path length $\ell_m$ (cm)	Core weight (g)
EE12	$0.731 \cdot 10^{-3}$	$0.458 \cdot 10^{-3}$	0.14	0.085	2.28	2.7	2.34
EE16	$2.02 \cdot 10^{-3}$	$0.842 \cdot 10^{-3}$	0.19	0.190	3.40	3.45	3.29
EE19	$4.07 \cdot 10^{-3}$	$1.3 \cdot 10^{-3}$	0.23	0.284	3.69	3.94	4.83
EE22	$8.26 \cdot 10^{-3}$	$1.8 \cdot 10^{-3}$	0.41	0.196	3.99	3.96	8.81
EE30	$85.7 \cdot 10^{-3}$	$6.7 \cdot 10^{-3}$	1.09	0.476	6.60	5.77	32.4
EE40	0.209	$11.8 \cdot 10^{-3}$	1.27	1.10	8.50	7.70	50.3
EE50	0.909	$28.4 \cdot 10^{-3}$	2.26	1.78	10.0	9.58	116
EE60	1.38	$36.4 \cdot 10^{-3}$	2.47	2.89	12.8	11.0	135
EE70/68/19	5.06	$75.9 \cdot 10^{-3}$	3.24	6.75	14.0	18.0	280

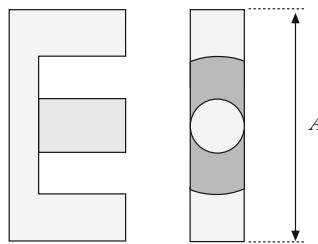
### B.3 EC Core Data



**Fig. B.3** EC core

Core type	Geometrical constant	Geometrical constant	Cross-sectional area	Bobbin winding area	Mean length per turn	Magnetic path length	Thermal resistance	Core weight
(A) (mm)	$K_g$ ( $\text{cm}^5$ )	$K_{gfe}$ ( $\text{cm}^x$ )	$A_c$ ( $\text{cm}^2$ )	$W_A$ ( $\text{cm}^2$ )	$MLT$ (cm)	$\ell_m$ (cm)	$R_{th}$ ( $^\circ\text{C}/\text{W}$ )	(g)
EC35	0.131	$9.9 \cdot 10^{-3}$	0.843	0.975	5.30	7.74	18.5	35.5
EC41	0.374	$19.5 \cdot 10^{-3}$	1.21	1.35	5.30	8.93	16.5	57.0
EC52	0.914	$31.7 \cdot 10^{-3}$	1.80	2.12	7.50	10.5	11.0	111
EC70	2.84	$56.2 \cdot 10^{-3}$	2.79	4.71	12.9	14.4	7.5	256

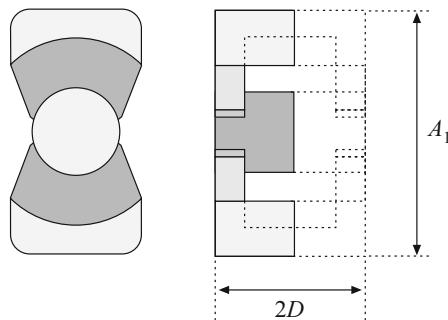
## B.4 ETD Core Data



**Fig. B.4** ETD core

Core type	Geometrical constant	Geometrical constant	Cross-sectional area	Bobbin winding area	Mean length per turn	Magnetic path length	Thermal resistance	Core weight
(A) (mm)	$K_g$ (cm <sup>5</sup> )	$K_{gfe}$ (cm <sup>x</sup> )	$A_c$ (cm <sup>2</sup> )	$W_A$ (cm <sup>2</sup> )	MLT (cm)	$\ell_m$ (cm)	$R_{th}$ (°C/W)	(g)
ETD29	0.0978	$8.5 \cdot 10^{-3}$	0.76	0.903	5.33	7.20		30
ETD34	0.193	$13.1 \cdot 10^{-3}$	0.97	1.23	6.00	7.86	19	40
ETD39	0.397	$19.8 \cdot 10^{-3}$	1.25	1.74	6.86	9.21	15	60
ETD44	0.846	$30.4 \cdot 10^{-3}$	1.74	2.13	7.62	10.3	12	94
ETD49	1.42	$41.0 \cdot 10^{-3}$	2.11	2.71	8.51	11.4	11	124

## B.5 PQ Core Data



**Fig. B.5** PQ core

Core type	Geometrical constant ( $A_1/2D$ ) (mm)	Geometrical constant $K_g$ ( $\text{cm}^5$ )	Geometrical constant $K_{gfe}$ ( $\text{cm}^x$ )	Cross-sectional area $A_c$ ( $\text{cm}^2$ )	Bobbin area $W_A$ ( $\text{cm}^2$ )	Mean length per turn $MLT$ (cm)	Magnetic path length $\ell_m$ (cm)	Core weight (g)
PQ20/16	$22.4 \cdot 10^{-3}$	$3.7 \cdot 10^{-3}$	$0.62$	$0.256$	$4.4$	$3.74$	$13$	
PQ20/20	$33.6 \cdot 10^{-3}$	$4.8 \cdot 10^{-3}$	$0.62$	$0.384$	$4.4$	$4.54$	$15$	
PQ26/20	$83.9 \cdot 10^{-3}$	$7.2 \cdot 10^{-3}$	$1.19$	$0.333$	$5.62$	$4.63$	$31$	
PQ26/25	$0.125$	$9.4 \cdot 10^{-3}$	$1.18$	$0.503$	$5.62$	$5.55$	$36$	
PQ32/20	$0.203$	$11.7 \cdot 10^{-3}$	$1.70$	$0.471$	$6.71$	$5.55$	$42$	
PQ32/30	$0.384$	$18.6 \cdot 10^{-3}$	$1.61$	$0.995$	$6.71$	$7.46$	$55$	
PQ35/35	$0.820$	$30.4 \cdot 10^{-3}$	$1.96$	$1.61$	$7.52$	$8.79$	$73$	
PQ40/40	$1.20$	$39.1 \cdot 10^{-3}$	$2.01$	$2.50$	$8.39$	$10.2$	$95$	

## B.6 American Wire Gauge Data

AWG #	Bare area, $10^{-3} \text{ cm}^2$	Resistance, $10^{-6} \Omega/\text{cm}$	Diameter, cm
0000	1072.3	1.608	1.168
000	850.3	2.027	1.040
00	674.2	2.557	0.927
0	534.8	3.224	0.825
1	424.1	4.065	0.735
2	336.3	5.128	0.654
3	266.7	6.463	0.583
4	211.5	8.153	0.519
5	167.7	10.28	0.462
6	133.0	13.0	0.411
7	105.5	16.3	0.366
8	83.67	20.6	0.326
9	66.32	26.0	0.291
10	52.41	32.9	0.267
11	41.60	41.37	0.238
12	33.08	52.09	0.213
13	26.26	69.64	0.190
14	20.02	82.80	0.171
15	16.51	104.3	0.153
16	13.07	131.8	0.137
17	10.39	165.8	0.122
18	8.228	209.5	0.109
19	6.531	263.9	0.0948
20	5.188	332.3	0.0874
21	4.116	418.9	0.0785
22	3.243	531.4	0.0701
23	2.508	666.0	0.0632
24	2.047	842.1	0.0566
25	1.623	1062.0	0.0505
26	1.280	1345.0	0.0452
27	1.021	1687.6	0.0409
28	0.8046	2142.7	0.0366
29	0.6470	2664.3	0.0330

(continued)

AWG #	Bare area, $10^{-3} \text{ cm}^2$	Resistance, $10^{-6} \Omega/\text{cm}$	Diameter, cm
30	0.5067	3402.2	0.0294
31	0.4013	4294.6	0.0267
32	0.3242	5314.9	0.0241
33	0.2554	6748.6	0.0236
34	0.2011	8572.8	0.0191
35	0.1589	10849	0.0170
36	0.1266	13608	0.0152
37	0.1026	16801	0.0140
38	0.08107	21266	0.0124
39	0.06207	27775	0.0109
40	0.04869	35400	0.0096
41	0.03972	43405	0.00863
42	0.03166	54429	0.00762
43	0.02452	70308	0.00685
44	0.0202	85072	0.00635

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