UCC28950 600W Phase Shifted Full Bridge Design Review/Application Report

Texas Instruments
Michael O'Loughlin
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Introduction:

In high power server applications to meet high efficiency and green standards some power supply designers have found it easier to use a phase shifted full bridge converter. This is because the phase shifted full bridge can obtain zero voltage switching on the primary side of the converter reducing switching losses and increasing overall efficiency. The purpose of this application report is to review the design of 600W phase shifted full bridge converter for one of these power systems, using TI's new UCC28950 phase shifted full bridge controller and was based on typical values. In a production design the values need to be modified for worst case conditions. Hopefully this information will aid other power supply designers in their efforts to design an efficient phase shifted full bridge converter.

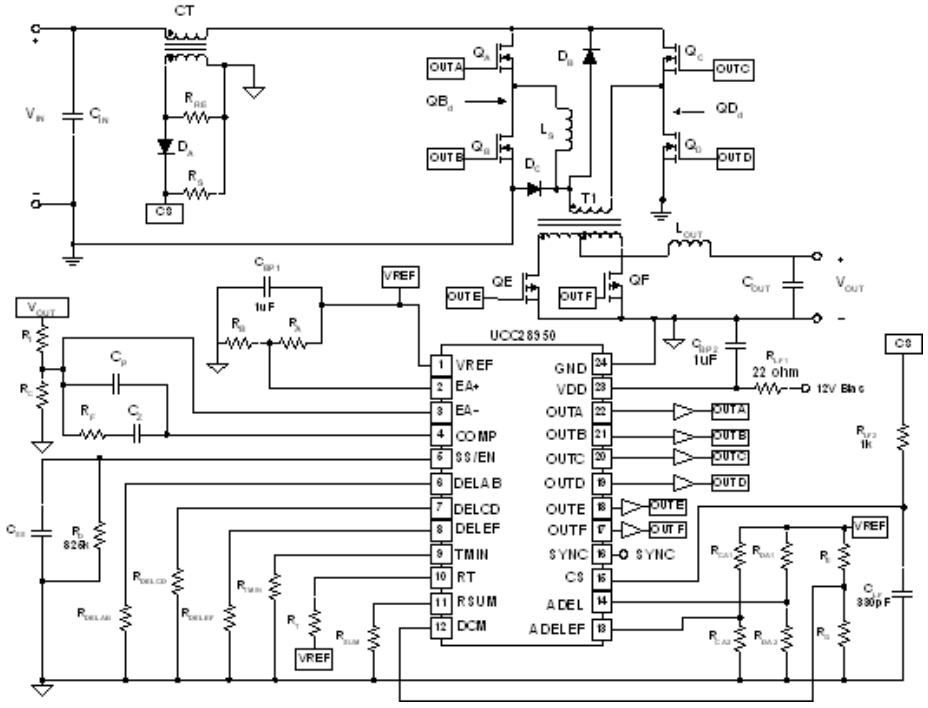
Note this Mathcad file can be modified to support individual design requirements.

MathCAD File:

Design Specifications:

Description			
Input Voltage		Output Voltage	
$Vinmin := 370V$	Minimum	$Vout := 12V$	Typical
$Vin := 390V$	Typical	Full Load Efficiency	
$Vinmax := 410V$	Maximum	$\eta 1 := 93\%$	Minimum
Output Power		Inductor Switching Frequency	
$Pout := 600W$	Maximum	$fs := 200 \cdot 10^3 Hz$	Typical
Allowable Output Voltage Transient for 90% Load Step			
$Vtran := 0.6V$	Typical		

Functional Schematic:



Power Budget:

To meet the efficiency goal a power budget needs to be set.

Figure 1

Preliminary Transformer Calculations (T1):

Transformer Turns Ratio (a1):

$$\eta 1 = \frac{\text{Pout}}{\text{Pout} + \text{PBudget}}$$

$$\text{PBudget} := \text{Pout} \cdot \frac{1 - \eta 1}{\eta 1}$$

$$\text{PBudget} = 45.161\ \text{W}$$

Estimated FET voltage drop (V_{RDSON}):

Select transformer turns based on 70% duty cycle (D_{MAX}) at minimum specified input voltage. This will give some room for dropout if a PFC front end is used.

$$a1 = \frac{Np}{Ns} = \frac{Vp}{Vs} = \frac{Is}{Ip}$$

$Vrdson := 0.3V$

Care needs to be taken in selecting *a transformer with the correct amount of* magnetizing inductance (L_{MAG}). The following equations calculate the minimum magnetizing inductance of the primary of the transformer (T1) to ensure the converter operates in current mode control. If L_{MAG} is too small the magnetizing current could cause the converter to operate in voltage mode control instead of peak current mode control. This is because the magnetizing current is too large it will act as a PWM ramp swamping out the current sense signal across R_S.

$Dmax := 70\%$

Calculated typical duty cycle (D_{TYP}) based on average input voltage.

$$a1 := \frac{Dmax \cdot (Vinmin - 2 \cdot Vrdson)}{Vout + Vrdson}$$

$a1 = 21.023$

Turns ratio rounded to the nearest hole turn

$a1 := 21$

$$Dtyp := \frac{(Vout + Vrdson) \cdot a1}{Vin - 2 \cdot Vrdson}$$

$Dtyp = 0.663$

Figure 2 shows T1 primary current ($I_{PRIMARY}$) and synchronous rectifiers QE (I_{QE}) and QF (I_{QF}) currents with respect to the synchronous rectifier gate drive currents. Note that I_{QE} and I_{QF} are also T1's secondary winding currents as well. Variable D is the converters duty cycle.

$$dILout := \frac{Pout \cdot 0.2}{Vout}$$

$dILout = 10\,A$ Output Inductor to be designed for 20% Inductor Ripple Current

$$Lmag := \frac{Vin \cdot (1 - Dtyp)}{\frac{dILout \cdot 0.5}{a1} \cdot fs}$$

$Lmag = 2.757 \times 10^{-3}\,H$

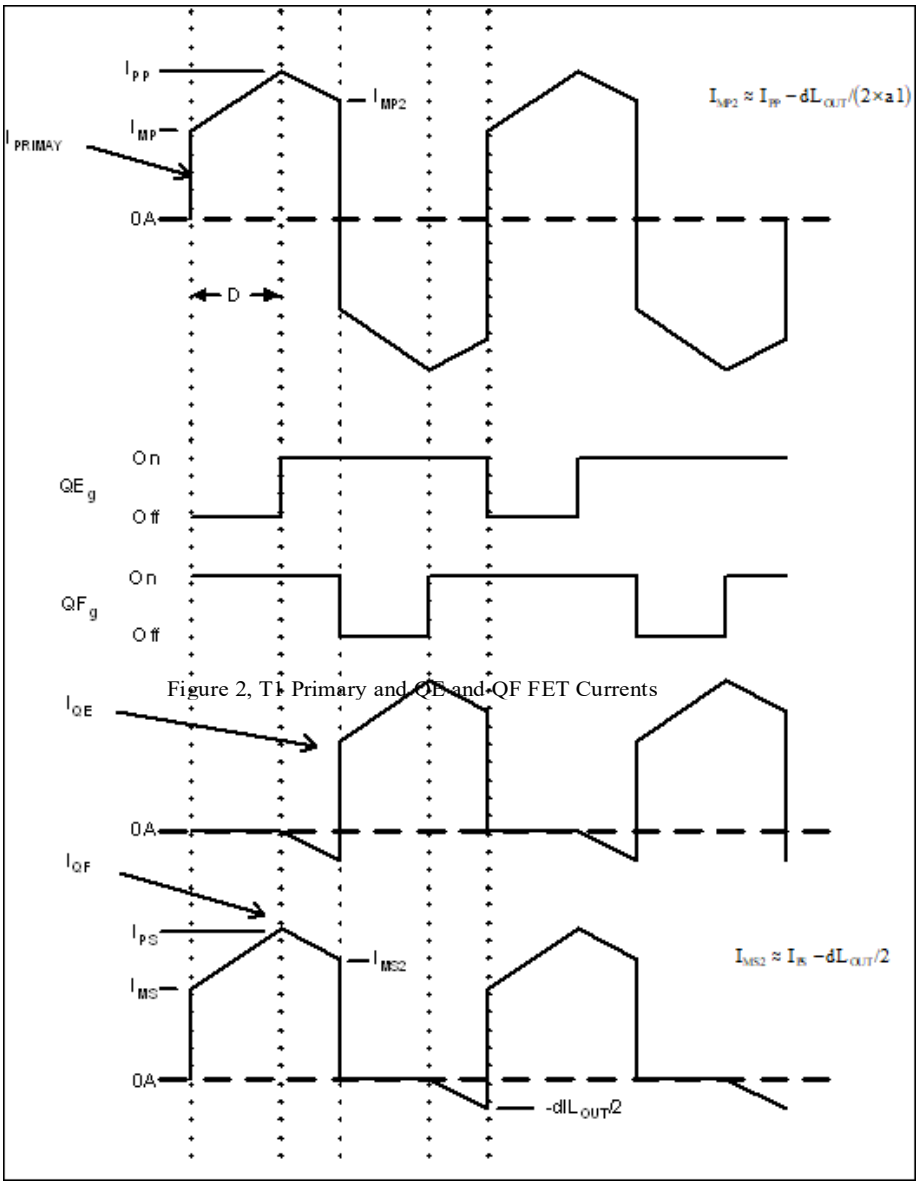


Figure 2, T1 Primary and QE and QF FET Currents

Secondary RMS current (I_{SRMS1}) when energy is being delivered to the secondary:

Calculate T1 Secondary RMS Current(Isrms)

Secondary RMS current I_{SRMS2} when current is circulating through the transformer when QE and QF are both on.

$$Ips := \frac{Pout}{Vout} + \frac{dILout}{2}$$

$$Ims := \frac{Pout}{Vout} - \frac{dILout}{2}$$

$$Ims2 := Ips - \frac{dILout}{2}$$

$Ips = 55\,A$ $Ims = 45\,A$ $Ims2 = 50\,A$

Secondary RMS current (I_{SRMS3}) caused by the negative current in the opposing winding during freewheeling period, please refer to figure 2.

$$Isrms1 := \sqrt{\left(\frac{Dmax}{2}\right)\cdot\left[Ips\cdot Ims + \frac{(Ips - Ims)^2}{3}\right]}$$

$Isrms1 = 29.63\,A$

$$Isrms2 := \sqrt{\left(\frac{1 - Dmax}{2}\right)\cdot\left[Ips\cdot Ims2 + \frac{(Ips - Ims2)^2}{3}\right]}$$

$Isrms2 = 20.341\,A$

Calculate T1 Primary RMS Current (I_{PRMS}):

$$Isrms3 := \frac{dILout}{2}\sqrt{\frac{1 - Dmax}{3\cdot 2}}$$

$Isrms3 = 1.118\,A$

Total Secondary single winding RMS current (Isrms):

$$Isrms := \sqrt{Isrms1^2 + Isrms2^2 + Isrms3^2}$$

T1 Primary RMS (I_{PRMS1}) current when energy is being delivered to the secondary.

$$Isrms = 35.957\ A$$

$$dILmag := \frac{Vinmin \cdot Dmax}{Lmag \cdot fs}$$ Primary magnetizing inductance current

$$dILmag = 0.47\ A$$

$$Ipp := \left(\frac{Pout}{Vout \cdot \eta 1} + \frac{dILout}{2}\right) \cdot \frac{1}{a1} + dILmag$$

$$Ipp = 3.268\ A$$

$$Imp := \left(\frac{Pout}{Vout \cdot \eta 1} - \frac{dILout}{2}\right) \cdot \frac{1}{a1} + dILmag$$

$$Imp = 2.792\ A$$

Total T1 Primary RMS Current (I_{PRMS})

$$Iprms1 := \sqrt{(Dmax) \cdot \left[Ipp \cdot Imp + \frac{(Ipp - Imp)^2}{3}\right]}$$

$$Iprms1 = 2.538\ A$$

Estimated transform losses (P_{T1}) are twice the copper loss. Note this is just an estimate and the total losses and may vary based on magnetic design.

$$Imp2 := Ipp - \left(\frac{dILout}{2}\right) \cdot \frac{1}{a1}$$

$$Imp2 = 3.03\ A$$

$$Iprms2 := \sqrt{(1 - Dmax)\cdot\left[Ipp\cdot Imp2 + \frac{(Ipp - Imp2)^2}{3}\right]}$$

$Iprms2 = 1.725\ A$

$$Iprms := \sqrt{Iprms1^2 + Iprms2^2}$$

QA, QB, QC, QD FET selection:
In this design to meet efficiency and voltage requirements 20A, 650V, CoolMOS FETs from Infineon were chosen for QA..QD for this design.

$Iprms = 3.068\ A$

For this design a Vitec transformer was chosen for the design that would dissipate roughly 6W. The transformer part number is 75P8107

$a1 := 21$ $Lmag := 2.8\ 10^{-3} H$

$Llk := 4\mu H$ Measured leakage inductance

Calculate average C_{OSS}

$DCRp := 0.215 ohm$ $DCRs := 0.58\cdot 10^{-3} ohm$

$$PT1 := 2\cdot\left(Iprms^2\cdot DCRp + 2\cdot Isrms^2\cdot DCRs\right)$$

$Iprms = 3.068\ A$

$PT1 = 7.048\ W$

$Isrms = 35.957\ A$

Calculate Remaining Power Budget

$PBudget := PBudget - PT1$

$PBudget = 38.113\ W$

Calculate QA losses (P_{OA}) based o

$RdsonQA := 0.220 ohm$ FET drain to source on resistance

$Coss\_qa\_spec := 780 pF$ FET Specified Coss

Selecting L_S:
Calculating the shim inductor (L_S) is based on the amount of energy required to achieve zero voltage switching. This inductor needs to able to deplete the energy from the parasitic capacitance at the switch node. The following equation selects L_S to achieve ZVS down to 50% load based on the primary FET's average total C_{OSS} at the switch node. **Note there may be more parasitic capacitance than was estimated at the switch node and L_S may have to be adjusted based on the actual parasitic capacitance in the final design.**

$Vds\_qa\_spec := 25V$ Voltage across drain to source where Coss was measured, data sheet parameter

$QAg := 15 \cdot 10^{-9} C$ FET Gate Charge

$$Coss\_avg\_qa := Coss\_qa\_spec \cdot \sqrt{\frac{Vds\_qa\_spec}{Vinmax}}$$

$$Coss\_avg\_qa = 1.926 \times 10^{-10} F$$

$Vg := 12V$ Voltage applied to the gate to activate the FET

Coss energy is supposed to be recovered and is not part of the thermal calculations

For this design a 26 uH Vitec inductor was chosen for the design, part number 60PR964. The shim inductor had the following specifications.

$$PQA\_Calculated := Iprms^2 \cdot RdsonQA + 2QAg \cdot Vg \cdot \frac{fs}{2}$$

Estimate L_S power loss (P_{LS}) and readjust remaining power budget

$PQA\_Calculated = 2.107\ W$

$PQA := PQA\_Calculated$

$PQA = 2.107\ W$

Recalculate Remaining Power Budget

$PBudget := PBudget - 4 \cdot PQA$

$PBudget = 29.684\ W$

Output Inductor Selection (L_{OUT}):
Inductor L1 was designed for 20% inductor ripple current (dI_{LOUT}):

Calculate output inductor RMS current ($I_{LOUT\ RMS}$):

A 2 uH inductor from Vitec Electronics Corparation, part number 75PR108, was chosen for this design. The inductor had the following specifications.

$$Ls := 2 \cdot Coss\_avg\_qa \cdot \frac{Vin^2}{\left(\frac{Ipp}{2} - \frac{dILout}{2 \cdot a1}\right)^2} - Llk$$

$$Ls = 2.607 \times 10^{-5}\,H$$

Calculate Output Inductor Losses (P_{LOUT}) and Recalculate Power Budget. Note P_{LOUT} is an estimate of inductor losses that is twice the copper loss. Note this may vary based on magnetic manufactures. It is advisable to double check the magnetic loss with the magnetic manufacture.

$Ls := 26\mu H$ $DCRls := 0.027ohm$

$$PLs := 2\left(Iprms^2 \cdot DCRls\right)$$

$$PLs = 0.508\,W$$

$$PBudget := PBudget - PLs$$

$$PBudget = 29.176\,W$$

Output Capacitance (C_{OUT}):
The output capacitor is being selected based on holdup and transient (V_{TRAN}) load requirements.

$$Lout := \frac{Vout \cdot (1 - Dtyp)}{dILout \cdot (fs)}$$

During load transients most of the current will immediately go through the capacitors equivalent series resistance ($ESRC_{OUT}$). The following equations are used to select ESR_{COUT} and C_{OUT} based on a 90% load step in current. The ESR is selected for 90% of the allowable transient voltage (V_{TRAN}), while the output capacitance (C_{OUT}) is selected for 10% of V_{TRAN}.

$$Lout = 2.02 \times 10^{-6}\,H$$

$$ILout\_rms := \sqrt{\left(\frac{Pout}{Vout}\right)^2 + \left(\frac{dILout}{\sqrt{3}}\right)^2}$$ RMS Current Solved in Quadrature

$$ILout\_rms = 50.332\,A$$

$Lout := 2 \cdot 10^{-6} H$ $DCRlout := 0.75 \cdot 10^{-3} ohm$

Before selecting the output capacitance it is also required to calculate the output capacitor RMS current (I_{COUT_RMS}).

To meet our design requirements five 1500uF, aluminum electrolytic capacitors were chosen for the design from United Chemi-Con, part number EKY-160ELL152MJ30S. These capacitors had an ESR of 31 mohms.

$PLout := 2 ILout\_rms^{2} \cdot DCRlout$

$PLout = 3.8\,W$

Recalculate Power Budget

$PBudget := PBudget - PLout$

$PBudget = 25.376\,W$

$$thu := \frac{Lout \cdot \frac{Pout \cdot 0.9}{Vout}}{Vout}$$

Time it takes Lout to change 90% of its full load current

$thu = 7.5 \times 10^{-6} s$

Recalculate Remaining Power Budget

$$ESRCout := \frac{Vtran \cdot 0.9}{\frac{Pout \cdot 0.9}{Vout}}$$

$ESRCout = 0.012\,\Omega$

$$Cout := \frac{\frac{Pout \cdot 0.9 \cdot thu}{Vout}}{Vtran \cdot 0.1}$$

$Cout = 5.625 \times 10^{-3} F$

Select FETs QE and QF:
Selecting FETs for a design is always trial and error. To meet the power requirements of this design we selected 75V, 120A FETs, from Fairchild, part number FDP032N08. These FETs' had the following characteristics.

$$Icout\_rms := \frac{dILout}{\sqrt{3}}$$

$Icout\_rms = 5.774\ A$

Calculate average FET C_{OSS} ($C_{OSS\_QE\_AVG}$) based on the data sheet parameters for C_{OSS} (C_{OSS_SPEC}), and drain to source voltage where C_{OSS_SPEC} was measured (V_{ds_spec}), and the maximum drain to source voltage in the design (Vds_off) that will be applied to the FET in the application.

$n := 5$ Number of output capacitors

$Capacitance := 1500\mu F$ Single Capacitance Value

$Cout := n \cdot Capacitance$ Total output capacitance

$Cout = 7.5 \times 10^{-3}\ F$

$ESR := 0.031\,ohm$ ESR of single capacitor

$$ESRCout := \frac{ESR}{n}$$ Effective ESR

$ESRCout = 6.2 \times 10^{-3}\ \Omega$

Calculate Output Capacitor Loss (Pcout)

$PCout := Icout\_rms^{2} \cdot ESRCout$

$PCout = 0.207\ W$

$PBudget := PBudget - PCout$

$PBudget = 25.169\ W$

Maximum gate charge at the end of the miller plateau

$QEg := 152 \times 10^{-9} C$ FET Gate Charge

$Rdsonqe := 0.0032 ohm$

Minimum gate charge at the end of the miller plateau

Note the FETs in this design were driven with UCC27324 setup to drive 4A (I_P) of gate drive current.

$$Vdsqe := \frac{Vinmax}{a1}$$

Estimated FET V_{ds} rise and fall time

$Vdsqe = 19.524\ V$ Voltage across FET in application

$Coss\_spec := 1810 pF$ Specified output capacitance from the data sheet

$Vds\_spec := 25V$ Voltage where FET Coss is specified

$$Coss\_qe\_avg := Coss\_spec \cdot \sqrt{\frac{Vdsqe}{Vds\_spec}}$$

$Coss\_qe\_avg = 1.6 \times 10^{-9} F$

$Iqe\_rms := Isrms$

$Iqe\_rms = 35.957\ A$ QE and QF RMS Current

Estimate QE and QF FET Losses (P_{OE})

To estimate FET switching loss the V_g vs. Q_g curve from the FET data sheet needs to be studied. First the gate charge at the beginning of the miller plateau needs to be determined (QE_{MILLER_MIN}) and the gate charge at the end of the miller plateau (QE_{MILLER_MAX}) for the given V_{ds}.

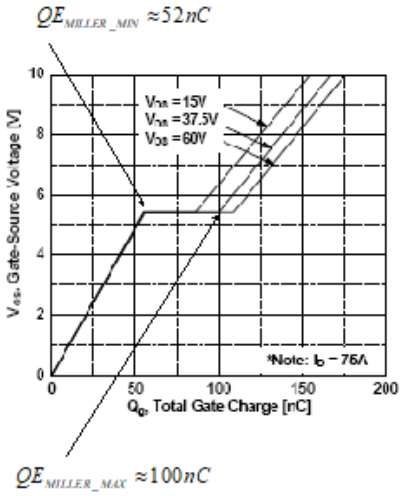


Figure 3, V_g vs. Q_g for QE and QF FETs

Input Capacitance (C_{IN}):

If this converter was designed for a 390V input, which is generally fed by the output of a PFC boost pre-regulator. The input capacitance is generally selected based on holdup and ripple requirements.

$QEgmiller\_max := 100 \times 10^{-9} C$

V_{DROP} is the minimum input voltage where the converter can still maintain output regulation. The converter's input voltage would only drop down this low during a brownout or line drop condition if this converter was following a PFC pre-regulator.

$QEgmiller\_min := 52 \cdot 10^{-9} C$

$Ip := 4A$

$$tr := \frac{QEgmiller\_max - QEgmiller\_min}{\frac{Ip}{2}}$$

$tr = 2.4 \times 10^{-8} s$

$tf := tr$

Calculate high frequency RMS current (I_{CINRMS}).

To meet the input capacitance and RMS current requirements for this design we chose a 330uF capacitor from Panasonic part number EETHC2W331EA.

$$PQE := Isrms^2 \cdot Rdsonqe + \frac{Pout}{Vout} \cdot Vdsqe \cdot (tr + tf) \cdot \frac{fs}{2} + 2Coss\_qe\_avg \cdot Vdsqe^2 \cdot \frac{fs}{2} + 2QEg \cdot Vg \cdot \frac{fs}{2}$$

Estimate Cin Power Disipation (P_{CIN})

$PQE = 9.31\ W$

Recalculate power budget

$PBudget := PBudget - 2PQE$

$PBudget = 6.549\ W$

$$fr := \frac{1}{2 \cdot \pi \sqrt{Ls \cdot 2Coss\_avg\_qa}}$$

$fr = 1.59 \times 10^6\ Hz$

Setting up the current sense network (CT, R_S, R_{RE}, D_A):
The CT chosen for this design had a turn's ratio (a2) of 100:1

$$tdelay := \frac{2}{4 \cdot fr}$$

$$a2 = \frac{I_P}{I_S}$$

$$Dclamp := \left(\frac{1}{fs} - tdelay\right) \cdot fs$$

$Dclamp = 0.937$

Calculate nominal peak current (I_P) at V_{INMIN}:

$$Vdrop := \frac{2 \cdot Dclamp \cdot Vrdson + a1 \cdot (Vout + Vrdson)}{Dclamp}$$

Calculate current sense resistor (R_S) and leave 200mV for slope compensation:

$$Vdrop = 276.232\ V$$

$$Cin := \frac{2Pout \cdot \frac{1}{60Hz}}{Vin^2 - Vdrop^2}$$

Select a standard resistor for R_S

$$Cin = 2.639 \times 10^{-4}\ F$$

Estimate Power Loss for R_S:

$$Icinrms := \sqrt{Iprms1^2 - \left(\frac{Pout}{Vinmin \cdot \eta 1}\right)^2}$$

$$Icinrms = 1.844\ A$$

$Cin := 330\mu F$ $ESRcin := 0.150ohm$

$$Pcin := Icinrms^2 \cdot ESRcin$$

$$Pcin = 0.51\ W$$

Recalculate remaining power budget

$$PBudget := PBudget - Pcin$$

$$PBudget = 6.039\ W$$

Resistor R_{LF} and capacitor C_{LF} form a low pass filter for the current sense signal (Pin 15). For this design we chose the following values. This filter has a low frequency pole (f_{LFP}) at 482 kHz. This should work for most applications but maybe adjusted to suit individual layouts and EMI present in the design.

The UCC28950 VREF output (Pin 1) needs a high frequency bypass capacitor to filter out high frequency noise. This pin needs at least 1uF of high frequency bypass capacitance (C_{BP1}). Please refer to figure 1 for proper placement.

$a2 := 100$

$Vp := 2V$ The Voltage where the peak limit comparitor will trip.

$$Ip1 := \left(\frac{\frac{Pout}{Vout} + \frac{dILout}{2}}{\eta 1} \right) \cdot \frac{1}{a1} + \frac{Vinmin \cdot Dmax}{Lmag \cdot fs}$$

$Ip1 = 3.279\,A$

The voltage amplifier reference voltage (Pin 2, EA +) can be set with a voltage divider (R_A, R_B), for this design example we are going to set the error amplifier reference voltage (V1) to 2.5V. Select a standard resistor value for R_B and then calculate resistor value R_A.

$$Rs := \frac{Vp - 0.2V}{\frac{Ip1}{a2} \cdot 1.1}$$

$Rs = 49.909\,\Omega$

$Rs := 48.7ohm$

Voltage divider formed by resistor R_C and R_I are chosen to set the DC output voltage (V_{OUT}) at Pin 3 (EA -).

$$Prs := \left(\frac{Iprms1}{a2} \right)^2 \cdot Rs$$

Select a standard resistor for R_C

$Prs = 0.031\,W$

Calculate R_I

Calculate Maximum Reverse Voltage Diode DA:

Compensating the feedback loop can be accomplished by properly selecting the feedback components (R_F, C_Z and C_P). These components are placed as close to pin 3 and 4 as possible of the UCC28950.

$$Vreset \cdot (1 - Dmax) = Vp \cdot Dmax$$

$$Vda := Vp \cdot \frac{Dclamp}{1 - Dclamp}$$

$$Vda = 29.806\,V$$

Estimate Rectifier Diode Loss Pda:

$$Vf := 0.6V$$

$$Pda := \frac{Pout \cdot Vf}{Vinmin \cdot \eta 1 \cdot a2}$$

Calculate load impedance at 10% load (R_{LOAD})

$$Pda = 0.01\,W$$

$$Rlf := 1 \cdot 10^{3} ohm$$

$$Clf := 330 \cdot 10^{-12} F$$

$$flfp := \frac{1}{2 \cdot \pi \cdot Rlf \cdot Clf}$$

$$flfp = 4.823 \times 10^{5} Hz$$

Compensate the voltage loop with the type 2 feedback network. The fowling transfer function is the compensation gain as a function of frequency ($G_C(f)$). Please refer to figure 1 for component placement.

$$Cbp1 := 1\mu F$$

$$Vref := 5V$$

Calculate voltage loop feedback resistor (R_F) based on crossing the voltage (f_C) loop over at a 10^{th} of the double pole frequency (f_{PP}).

$V1 := 2.5V$

$Rb := 2.37 \cdot k\Omega$ Select standard resistor

$$Ra := \frac{Rb \cdot (Vref - V1)}{V1}$$

$Ra = 2.37 \times 10^3 \Omega$

Select a standard resistor for R_F

Calculate the feedback capacitor (C_Z) to give added phase at crossover

$Rc := 2.37 \cdot k\Omega$

$$Ri := \frac{Rc \cdot (Vout - V1)}{V1}$$

$Ri = 9.006 \times 10^3 \Omega$

Select a standard capacitance value for the design.

Select Standard Component

$Ri := 9.09 \cdot K\Omega$

Put a pole at two times f_C.

$$f := 100Hz, 110Hz .. \frac{fs}{2}$$

$S(f) := 2j \cdot \pi \cdot f$

Select a standard capacitance value for the design.

$$RLoad := \frac{Vout^2}{Pout \cdot 0.1}$$

Loop gain as a function of frequency ($T_V(f)$) in dB.

$$T_V dB(f) = 20 \log\left(\left|G_C(f) \times G_{CO}(f)\right|\right)$$

Control to output gain (Gco(f))

$$fpp := \frac{fs}{4}$$

$$fpp = 5 \times 10^4 \frac{1}{s}$$

$$Gco(f) := a1 \cdot a2 \cdot \frac{RLoad}{Rs} \cdot \left(\frac{1 + S(f) \cdot ESRCout \cdot Cout}{1 + S(f) \cdot RLoad \cdot Cout}\right) \cdot \frac{1}{1 + \frac{S(f)}{2 \cdot \pi \cdot fpp} + \left(\frac{S(f)}{2 \cdot \pi \cdot fpp}\right)^2}$$

Plot theoretical loop gain and phase to graphically check for loop stability. The theoretical loop gain crossed over at roughly 3.7 kHz with a phase margin of greater than 90 degrees. Note it is wise to check your loop stability of your final design with transient testing and/or a network analyzer and adjust the compensation ($G_C(f)$) feedback as necessary.

$$Gc(f) = \frac{S(f) \cdot Rf \cdot Cz + 1}{S(f) \cdot (Cz + Cp) \cdot Ri \cdot \left(S(f) \cdot \frac{Cp \cdot Cz}{Cp + Cz} \cdot Rf + 1\right)}$$

$$fc := \frac{fpp}{10}$$

$$fc = 5 \times 10^3 \frac{1}{s}$$

$$\left|Gco(fc)\right| = 0.326$$

$$Rf := Ri \cdot \frac{1}{|Gco(fc)|}$$

$$Rf = 2.792 \times 10^{4}\,\Omega$$

$$Rf := 27.4 \cdot 10^{3}\,ohm$$

$$Cz := \frac{1}{2 \cdot \pi \cdot \frac{fc}{5} \cdot Rf}$$

$$Cz = 5.809 \times 10^{-9}\,F$$

$$Cz := 5.6nF$$

To limit over shoot during power up the UCC28950 has a soft start function (SS, Pin 5) which in this application was set for a soft start time of 15ms (t_{SS}).

$$Cp := \frac{1}{2 \cdot \pi \cdot Rf \cdot fc \cdot 2}$$

$$Cp = 5.809 \times 10^{-10}\,F$$

This application note presents a fixed delay approach to achieving ZVS from 100% load to 50% load. When the converter is operating below 50% load the converter will be operating in valley switching. In order to achieve zero voltage switching on switch node of QB_d, the turn-on (t_{ABSET}) delays of FETs QA and QB needs to be initially set based on the interaction of L_S and the theoretical switch node capacitance. The following equations are used to set t_{ABSET} initially:

$$Cp := 560pF$$

$$Gc(f) := \frac{S(f) \cdot Rf \cdot Cz + 1}{S(f) \cdot (Cz + Cp) \cdot Ri \cdot \left(S(f) \cdot \frac{Cp \cdot Cz}{Cz + Cp} \cdot Rf + 1 \right)}$$

Equate shim inductance and switch node impedance

Calculate Tank frequency

Plot Loop gain and Phase (Tv(f))

$$Tv(f) := Gco(f) \cdot Gc(f)$$

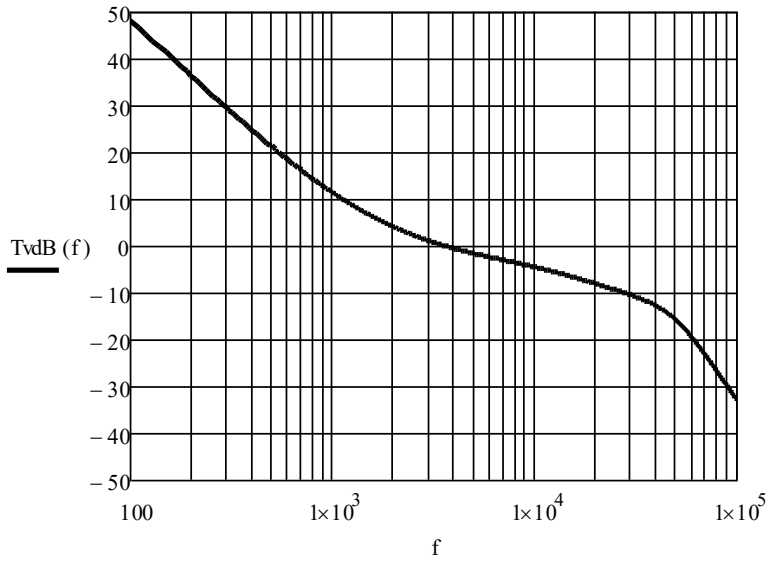
$$TvdB(f) := 20 \cdot \log(|Tv(f)|)$$

The resistor divider formed by R_{DA1} and R_{DA2} programs the t_{ABSET}, t_{CDSET} delay range of the UCC28950. Select a standard resistor value for R_{DA1}. Note that t_{ABSET} can be programmed between 29ns to 1000ns.

$$\theta Tv(f) := \arg(Tv(f)) \cdot \frac{180}{\pi} + 180$$

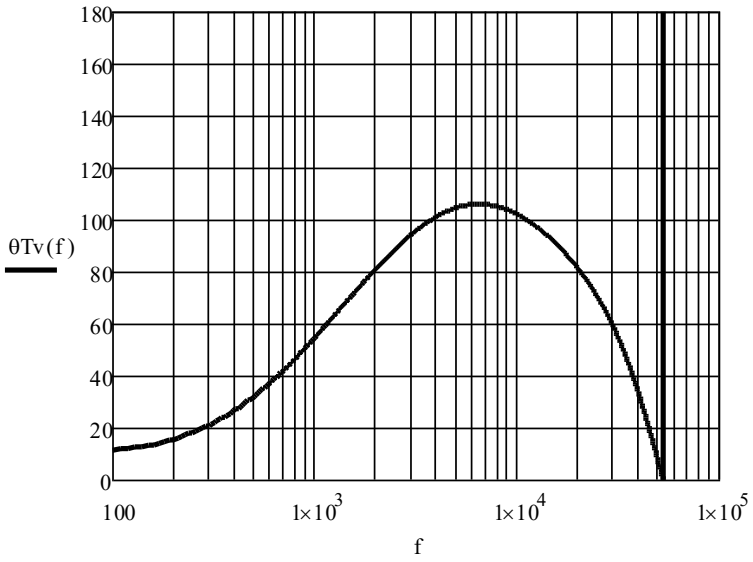
V_{ADEL} = 0.2V, t_{ABSET} can be programmed between 155 ns and 1000 ns.

V_{ADEL} = 1.8V, t_{ABSET} can be programmed between 29 ns and 155 ns.



Recalculate V_{ADEL} based on resistor divider selection:

Resistor R_{DELAB} programs t_{ABSET}:



$$TvdB(3.7KHz) = -0.099$$

$$\theta Tv(3.7kHz) = 99.484$$

$Tss := 15 \cdot 10^{-3} s$ soft start time(Tss)

Note once soft start time(Tss) and running it is recommended you fine tune t_{ABSET} at light load to the peak and valley of the resonance between L_S and the switch node capacitance. In this design the delay was set at 10% load. Please refer to figure 5.

$$Css := \frac{Tss \cdot 25 \cdot 10^{-6} A}{V1 + 0.55V}$$

Select a standard capacitor for the design

$Css := 150nF$

$Css = 150\,nF$

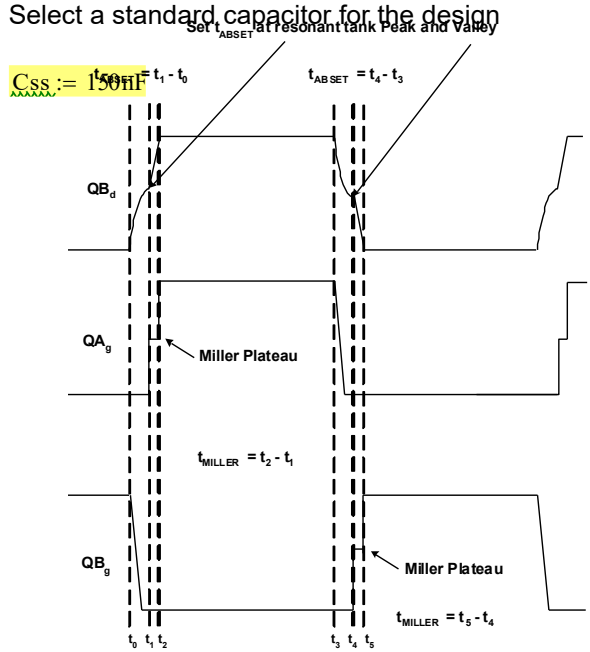


Figure 5, t_{ABSET} to achieve valley switching at light loads

$$2\pi \cdot fr \cdot Ls = \frac{1}{2 \cdot \pi \cdot fr \cdot (2 \cdot Coss\_avg\_qa)}$$

$$fr := \frac{1}{2 \cdot \pi \sqrt{Ls \cdot 2Coss\_avg\_qa}}$$

$$fr = 1.59 \times 10^{6}\,Hz$$

The initial starting point for the QC and QD turn on delays (t_{CDSET}) should be initially set for the same delay as the QA and QB turn on delays (Pin 6). The following equation programs the QC and QD turn-on delays (t_{CDSET}) by properly selecting resistor R_{DELCD} (Pin 7).

$$tabset := \frac{2}{4 \cdot fr}$$

$$tabset = 3.458 \times 10^{-7}\,s$$ Set intial dealy time

Resistor R_{DELCE} programs t_{CDSET}:

$$Rda1 := 8.25 \cdot 10^{3}\,ohm$$

$$VADEL := \begin{cases} 0.2\,V & \text{if } tabset > 155 \cdot 10^{-9}\,s \\ 1.8\,V & \text{if } tabset \le 155 \cdot 10^{-9}\,s \end{cases}$$

$$VADEL = 0.2\,V$$

$$\frac{VREF - VADEL}{Rda1} = \frac{VADEL}{Rda2}$$

$$Rda2 := \frac{Rda1 \cdot VADEL}{5V - VADEL}$$

$$Rda2 = 343.75\,\Omega$$

Select Closest Standard Value

$$Rda2 := 348\,ohm$$

Note once you have a prototype up and running it is recommended to fine tune t_{CDSET} at light load. In this design the CD node was set to valley switch at roughly 10% load. Please refer to figure 6. Obtaining ZVS at lighter loads with switch node QD_d is easier due to the reflected output current present in the primary of the transformer at FET QD and QC turnoff/on. This is because there was more peak current available to energize L_S before this transition, compared to the QA and QB turnoff/on.

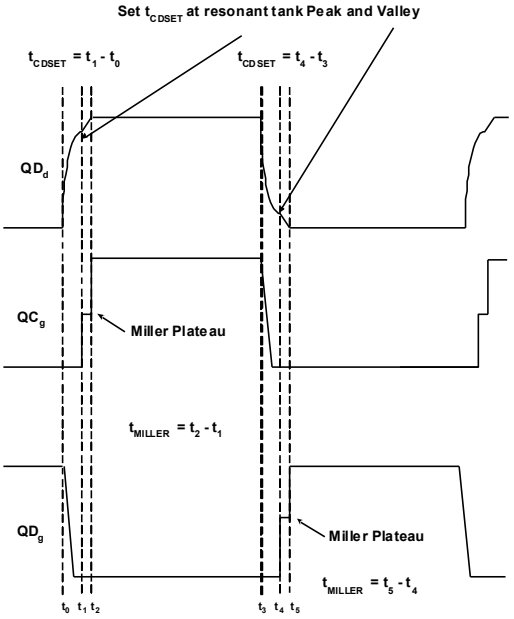


Figure 6, t_{CDSET} to achieve valley switching at light loads

There is a programmable delay for the turnoff of FET QF after FET QA turnoff (t_{AFSET}) and the turnoff of FET QE after FET QB turnoff (t_{BESET}). A good place to set these delays is 50% of t_{ABSET}. This will ensure that the appropriate synchronous rectifier turns off before the AB ZVS transition. If this delay is too large it will cause OUTE and OUTF not to overlap correctly and it will create excess body diode conduction on FETs QE and QF.

$$VADEL := \frac{5V \cdot Rda2}{Rda1 + Rda2}$$

$$VADEL = 0.202\,V$$

$$Rdelab := \frac{\left(tabset - 5 \times 10^{-9} s\right) \cdot (0.15V + VADEL \cdot 1.46) \cdot 10^3}{5 \times 10^{-9} s \cdot 1A}$$

The following equations were used to program t_{AFSET} by properly selecting resistor R_{DELEF}.

$$Rdelab = 3.037 \times 10^4 \Omega$$

Select Closest Standard Resistor Value

$$Rdelab := 30.1 \cdot 10^3 ohm$$

Check timing with resistor selected

If t_{AFSET} < 170 ns set V_{ADEL} = 0.2V, t_{ABSET} can be programmed between 32 ns and 170 ns.

tabset = 3.458×10^{-7} s

If t_{ABSET} > or = 170 ns set V_{ADEL} = 1.7V, t_{ABSET} can be programmed between 170 ns and 1100 ns.

$$\left(\frac{5 \cdot \frac{Rdelab \cdot V}{1 \cdot 10^{3} ohm}}{0.15V + VADEL \cdot 1.46}\right) 10^{-9} s + 5\,10^{-9} s = 3.428 \times 10^{-7} s$$

The following equation was used to program t_{AFSET} and t_{BESET} by properly selecting resistor R_{DELEF}.

Resistor R_{TMIN} programs the minimum duty cycle on time (t_{MIN}) that the UCC28950 (Pin 9) can demand before entering burst mode. If the UCC28950 controller tries to demand a duty cycle on time of less than t_{MIN} the power supply will go into burst mode operation. Please see the UCC28950 data sheet for details regarding burst mode. For this design we set the minimum on time to 100ns.

tcdset := tabset

$$Rdelcd := \frac{\left(tabset - 5 \times 10^{-9} s\right) \cdot (0.15V + VADEL \cdot 1.46) \cdot 10^{3}}{5 \times 10^{-9} s \cdot 1A}$$

The minimum on time is set by selecting R_{TMIN} with the following equation.

Rdelcd = $3.037 \times 10^{4}\ \Omega$

Rdelcd := $30.1 \cdot 10^{3}$ ohm Select a standard resistor

There is a pin that is provided for setting up the converter switching frequency (Pin 10). The frequency can be selected by adjusting timing resistor R_T.

The UCC28950 also provides slope compensation for peak current mode control (Pin 12). This can be set by setting R_{SUM} with the following equations. The following equations will calculate the required amount of slope compensation (V_{SLOPE}) that is needed for loop stability. Note the change in magnetizing current on the primary dIL_{MAG} contributes to slope compensation.

To help improve noise immunity V_{SLOPE} is set to have a total slope that will equal 0.2V over one inductor switching period.

$$tafset := 0.5 \cdot tabset$$

$$tafset = 1.729 \times 10^{-7}\,s$$

$$VADELEF := \begin{cases} 0.2\,V & \text{if } tafset < 170 \cdot 10^{-9}\,s \\ 1.7\,V & \text{if } tafset \geq 170 \cdot 10^{-9}\,s \end{cases}$$

$$VADELEF = 1.7\,V$$

To increase efficiency at lighter loads the UCC28950 is programmed (Pin 12, DCM) under light load conditions to turn off the synchronous FETs on the secondary side of the converter (Q_E and Q_F). This threshold is programmed with resistor divider formed by R_E and R_G. This DCM threshold needs to be set at a level before the inductor current goes discontinues. The following equation sets the synchronous rectifiers to turnoff at roughly 15% load current.

$$Rca1 := Rda1$$

$$Rca1 = 8.25 \times 10^{3}\,\Omega$$

$$\frac{VREF - VADELEF}{Rca1} = \frac{VADELEF}{Rca2}$$

$$Rca2 := \frac{Rca1 \cdot VADELEF}{5V - VADELEF} \qquad VADELEF = 1.7\,V \qquad Rca1 = 8.25 \times 10^{3}\,\Omega$$

$$Rca2 = 4.25 \times 10^{3}\,\Omega$$

Select Standard Resistor Value

$$Rca2 := 4.22 \cdot 10^{3}\,ohm$$

Recalculate VADELEF

$$VADELEF := \frac{5V \cdot Rca2}{Rca1 + Rca2}$$

$$VADELEF = 1.692\,V$$

$$Rdelef := \frac{\left(tafset - 4 \times 10^{-9}\,s\right) \cdot (2.65V - VADELEF \cdot 1.32) \cdot 10^{3}}{5 \times 10^{-9}\,s \cdot 1A}$$

$$Rdelef = 1.407 \times 10^{4}\,\Omega$$

Select a standard resistor.

$$Rdelef := 14.0 \cdot 10^{3}\,ohm$$

Check tafset timing $tafset = 1.729 \times 10^{-7}\,s$

$$\left(5 \cdot \frac{Rdelef \cdot V}{1 \cdot 10^{3}\,ohm} \Big/ (2.65\,V - VADELEF \cdot 1.32)\right) 10^{-9}\,s + 4\,10^{-9}\,s = 1.721 \times 10^{-7}\,s$$

$tmin := 100 \cdot 10^{-9}\,s$

$$Rtmin := \frac{(tmin - 15 \cdot 10^{-9}\,s) \cdot 10^{3} \cdot 1ohm}{6.6 \cdot 10^{-9}\,s}$$

$Rtmin = 1.288 \times 10^{4}\,\Omega$

A standard resistor value is then chosen for the design

$Rtmin := 13.0 \cdot 10^{3}\,ohm$

$$Rt := \left(\frac{2.5 \cdot 10^{6} \cdot \frac{ohm \cdot Hz}{V}}{\frac{fs}{2}} - \frac{ohm}{V}\right) \cdot (Vref - 2.5 \cdot V) \cdot 10^{3}$$

$Rt = 6 \times 10^{4}\,\Omega$

Select a standard value for the design

$Rt := 61.9 \cdot 10^{3}\,ohm$

$$dILpm := Vin \cdot \frac{1 - Dtyp}{Lmag \cdot fs}$$

$$Lmag = 2.8 \times 10^{-3}\,H$$

$$dILpm = 0.234\,A$$

$$Vslope1 := 0.2V \cdot fs$$

$$Vslope2 := \frac{\left(\frac{dILout}{a1 \cdot 2} - dILpm\right) \cdot Rs \cdot fs}{a2 \cdot (1 - Dtyp)}$$

$$Vslope := \begin{cases} Vslope1 & \text{if } Vslope2 < Vslope1 \\ Vslope2 & \text{if } Vslope2 \geq Vslope1 \end{cases}$$

$$Vslope1 = 0.04\,\frac{V}{\mu s}$$

$$a1 = 21$$

$$a2 = 100$$

$$Vslope2 = 1.049 \times 10^{-3}\,\frac{V}{\mu s}$$

$$Rsum := \frac{2.5V \cdot 10^{3}\,ohm}{Vslope \cdot 0.5 \cdot 10^{-6}\,s}$$

$$Vslope = 0.04\,\frac{V}{\mu s}$$

$$Rsum = 1.25 \times 10^{5}\,ohm$$

$$Rsum := 127 \cdot 10^{3}\,ohm$$

$$Vrs := Rs \cdot \frac{\frac{Pout \cdot 0.15}{Vout} + \frac{dILout}{2}}{a1 \cdot a2}$$

$$Vrs = 0.29\,V$$

$Rg := 1 \cdot 10^{3}\,ohm$ Chose Standard Resistor

$$Re := \frac{Rg \cdot (Vref - Vrs)}{Vrs}$$

$Re = 1.625 \times 10^{4}\,\Omega$

$Re := 16.9 \cdot 10^{3}\,ohm$ Chose a standard resistor for the design