

Robert W. Erickson
Dragan Maksimović

Fundamentals of Power Electronics

Third Edition

Fundamentals of Power Electronics

Robert W. Erickson • Dragan Maksimović

Fundamentals of Power Electronics

Third Edition



Springer

Robert W. Erickson
Department of Electrical, Computer,
and Energy Engineering
University of Colorado Boulder
Boulder, CO, USA

Dragan Maksimović
Department of Electrical, Computer,
and Energy Engineering
University of Colorado Boulder
Boulder, CO, USA

ISBN 978-3-030-43879-1 ISBN 978-3-030-43881-4 (eBook)
<https://doi.org/10.1007/978-3-030-43881-4>

1st edition: © Springer Science+Business Media Dordrecht 1997

2nd edition: © Kluwer Academic Publishers 2001

© Springer Nature Switzerland AG 2020

This work is subject to copyright. All rights are reserved by the Publisher, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, reuse of illustrations, recitation, broadcasting, reproduction on microfilms or in any other physical way, and transmission or information storage and retrieval, electronic adaptation, computer software, or by similar or dissimilar methodology now known or hereafter developed.

The use of general descriptive names, registered names, trademarks, service marks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

The publisher, the authors, and the editors are safe to assume that the advice and information in this book are believed to be true and accurate at the date of publication. Neither the publisher nor the authors or the editors give a warranty, expressed or implied, with respect to the material contained herein or for any errors or omissions that may have been made. The publisher remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

This Springer imprint is published by the registered company Springer Nature Switzerland AG
The registered company address is: Gewerbestrasse 11, 6330 Cham, Switzerland

Dedicated to

*Linda, William, and Richard
Lidiya, Filip, Nikola, and Stevan*

Preface

The objective of the First and Second Editions was to serve as a textbook for introductory power electronics courses where the fundamentals of power electronics are defined, rigorously presented, and treated in sufficient depth so that students acquire the knowledge and skills needed to design practical power electronic systems. An additional goal was to contribute as a reference book for engineers who practice power electronics design, and for students who want to develop their knowledge of the area beyond the level of introductory courses. In this Third Edition, the basic objectives and philosophy of the earlier editions have not been changed.

Since we wrote the Second Edition, the field of power electronics has grown tremendously, including new significant commercial applications such as electric vehicles, wireless power transfer, and utility microgrids. Technical growth includes the commercialization of wide bandgap power semiconductors, widespread digital control of switching converters, and maturation of converter modeling. Our university power electronics curriculum has evolved as well, in content as well as in organization. This edition is a response to these changes, and represents a significant revision relative to the previous edition.

As of 2020, at the University of Colorado we offer a sequence of three core graduate courses in power electronics. The first course, *Introduction to Power Electronics*, covers basic converter analysis, converter controllers, and magnetics. In the Third Edition, this material is presented in Chaps. 1–12, at the level and in the order covered in this class. Our second course, *Modeling and Control of Power Electronics Systems*, covers more advanced topics of power converter applications, control, and design-oriented analysis. This material is covered in detail in Chaps. 13–21 in the Third Edition; this portion of the text represents a major revision of technical material and coverage. Our third course, *Resonant and Soft Switching Phenomena in Power Electronics*, relies primarily on supplementary notes rather than this textbook. Chapters 22 and 23 of the Third Edition cover a summary of a portion of this third course.

The coverage of power semiconductor devices in Chap. 4 has been bolstered and updated. The discussion of power diode switching has been significantly expanded, leading into averaged modeling of diode-induced switching loss. New material on wide bandgap devices and on MOSFET gate drivers has been added. The discussion of switching loss mechanisms has been updated and reorganized, and the MCT section is removed.

The Third Edition adopts a more mature viewpoint of averaging, based on the trapezoidal moving average defined in Eq. (7.3). The waveforms of the averaged model become true continuous quantities, with the approximations and logical steps clearly defined. New material in

Chap. 7 includes a section on the averaging operator, and a new treatment of how the small-ripple approximation works with the trapezoidal moving average. Additionally, the logical flow of Chap. 7 has been significantly revised to conform to how we now teach this material in our on-campus courses, and new material on state-space averaging has been added. This new viewpoint of averaging then is followed throughout the remainder of the book. Of most note, this viewpoint leads to the current-programmed control model of Tan and Middlebrook. The current-programmed control Chap. 18 has been significantly revised and updated accordingly. The high-frequency effects of sampling are discussed as well, in connection with current-programmed control and also with ac modeling of the discontinuous conduction mode.

The previous treatment of stability and phase margin would leave some students with misconceptions; to alleviate this, we have introduced a new section on Nyquist stability. Instructors may choose whether there is time to cover this material in a power electronics course, but the explanation is available as a reference in the text. The origin of the phase margin text is rigorously explained, and special cases such as conditionally stable systems or those with multiple crossover frequencies are adjudicated. A new section in the chapter on input filters has been added, which relies on the Nyquist stability criterion to determine the exact stability boundary in the presence of an input filter.

An all-new Part IV *Advanced Modeling, Analysis, and Control Techniques* has been organized to follow the logical flow of our advanced converter control course, and incorporates new chapters on null double injection techniques (Middlebrook's feedback theorem and extra element theorem) and on digital control of switching converters. The topics of circuit averaging, average switch modeling, and averaged simulation are consolidated into a single logical chapter. New examples of the extra element theorem include solution of the SEPIC averaged switch model, and damping the internal resonances of the SEPIC.

Chapter 18 on current-programmed control has been significantly revised and reorganized. As noted above, it now employs the model of Tan and Middlebrook, using the trapezoidal moving average. New sections on simulation, sampling and high-frequency dynamics, and input filters are incorporated into the chapter. A new section on average current-mode control has also been added.

The new Chap. 19 on digital control of switching converters extends the analog control techniques of earlier chapters, to address the relevant issues of digital controllers. Quantization, sampling, and controller delays are modeled. The \mathcal{Z} -transform is employed to model the discrete-time portion of the feedback loop, with the Laplace transform used as usual for the remaining analog system. Digital compensator design and realization is then addressed.

This text has evolved from courses developed over thirty-five years of teaching power electronics at the University of Colorado. These courses, in turn, were heavily influenced by our previous experiences as graduate students at the California Institute of Technology, under the direction of Profs. Slobodan Ćuk and R. D. Middlebrook, to whom we are grateful. We would also like to thank the many readers of the First and Second Editions, students, and instructors who offered their comments and suggestions, or who pointed out errata. We have attempted to incorporate these suggestions wherever possible.

Boulder, CO, USA
Boulder, CO, USA

Robert W. Erickson
Dragan Maksimović

Contents

1	Introduction	1
1.1	Introduction to Power Processing	1
1.2	Several Applications of Power Electronics	8
1.3	Elements of Power Electronics	10

Part I Converters in Equilibrium

2	Principles of Steady-State Converter Analysis	15
2.1	Introduction	15
2.2	Volt-Second and Charge Balance, Small-Ripple Approximation	18
2.3	Boost Converter Example	24
2.4	Ćuk Converter Example	30
2.5	Estimating the Output Voltage Ripple in Converters Containing Two-Pole Low-Pass Filters	35
2.6	Summary of Key Points	37
Problems		38
3	Steady-State Equivalent Circuit Modeling, Losses, and Efficiency	43
3.1	The DC Transformer Model	43
3.2	Inclusion of Inductor Copper Loss	46
3.3	Construction of Equivalent Circuit Model	49
3.3.1	Inductor Voltage Equation	50
3.3.2	Capacitor Current Equation	50
3.3.3	Complete Circuit Model	51
3.3.4	Efficiency	52
3.4	How to Obtain the Input Port of the Model	54
3.5	Example: Inclusion of Semiconductor Conduction Losses in the Boost Converter Model	56
3.6	Summary of Key Points	60
Problems		61

4	Switch Realization	67
4.1	Switch Applications	69
4.1.1	Single-Quadrant Switches	69
4.1.2	Current-Bidirectional Two-Quadrant Switches	72
4.1.3	Voltage-Bidirectional Two-Quadrant Switches	75
4.1.4	Four-Quadrant Switches	76
4.1.5	Synchronous Rectifiers	78
4.2	Introduction to Power Semiconductors	79
4.2.1	Breakdown Voltage, Forward Voltage, and Switching Speed	79
4.2.2	Transistor Switching Loss with Clamped Inductive Load	80
4.3	The Power Diode	82
4.3.1	Introduction to Power Diodes	82
4.3.2	Discussion: Power Diodes	87
4.3.3	Modeling Diode-Induced Switching Loss	90
4.3.4	Boost Converter Example	94
4.4	Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)	99
4.4.1	Introduction to the Power MOSFET	99
4.4.2	Wide-Bandgap FETs	103
4.4.3	MOSFET Gate Drivers	107
4.5	Minority-Carrier Transistors	111
4.5.1	Bipolar Junction Transistor (BJT)	111
4.5.2	Insulated-Gate Bipolar Transistor (IGBT)	115
4.5.3	Thyristors (SCR, GTO)	119
4.6	Additional Sources of Switching Loss	122
4.6.1	Device Capacitances, and Leakage, Package, and Stray Inductances	122
4.6.2	Inducing Switching Loss in Other Elements	124
4.6.3	Efficiency vs. Switching Frequency	126
4.7	Summary of Key Points	126
	Problems	128
5	The Discontinuous Conduction Mode	135
5.1	Origin of the Discontinuous Conduction Mode, and Mode Boundary	135
5.2	Analysis of the Conversion Ratio $M(D, K)$	140
5.3	Boost Converter Example	145
5.4	Summary of Results and Key Points	152
	Problems	154
6	Converter Circuits	163
6.1	Circuit Manipulations	164
6.1.1	Inversion of Source and Load	164
6.1.2	Cascade Connection of Converters	166
6.1.3	Rotation of Three-Terminal Cell	169
6.1.4	Differential Connection of the Load	170
6.2	A Short List of Converters	174
6.3	Transformer Isolation	178
6.3.1	Full-Bridge and Half-Bridge Isolated Buck Converters	181
6.3.2	Forward Converter	187

6.3.3	Push-Pull Isolated Buck Converter	192
6.3.4	Flyback Converter	194
6.3.5	Boost-Derived Isolated Converters	198
6.3.6	Isolated Versions of the SEPIC and the Ćuk Converter	201
6.4	Summary of Key Points	203
	Problems	205

Part II Converter Dynamics and Control

7	AC Equivalent Circuit Modeling	215
7.1	Introduction	215
7.2	The Basic AC Modeling Approach	220
7.2.1	Averaging the Inductor and Capacitor Waveforms	221
7.2.2	The Average Inductor Voltage and the Small-Ripple Approximation	222
7.2.3	Discussion of the Averaging Approximation	223
7.2.4	Averaging the Capacitor Waveforms	225
7.2.5	The Average Input Current	226
7.2.6	Perturbation and Linearization	227
7.2.7	Construction of the Small-Signal Equivalent Circuit Model	230
7.2.8	Discussion of the Perturbation and Linearization Step	232
7.2.9	Results for Several Basic Converters	233
7.2.10	Example: A Nonideal Flyback Converter	234
7.3	Modeling the Pulse-Width Modulator	242
7.4	The Canonical Circuit Model	245
7.4.1	Development of the Canonical Circuit Model	245
7.4.2	Example: Manipulation of the Buck–Boost Converter Model into Canonical Form	248
7.4.3	Canonical Circuit Parameter Values for Some Common Converters	250
7.5	State-Space Averaging	251
7.5.1	The State Equations of a Network	252
7.5.2	The Basic State-Space Averaged Model	255
7.5.3	Discussion of the State-Space Averaging Result	256
7.5.4	Example: State-Space Averaging of a Nonideal Buck–Boost Converter	259
7.5.5	Example: State-Space Averaging of a Boost Converter with ESR	264
7.6	Summary of Key Points	271
	Problems	272
8	Converter Transfer Functions	277
8.1	Review of Bode Plots	279
8.1.1	Single-Pole Response	281
8.1.2	Single Zero Response	287
8.1.3	Right Half-Plane Zero	288
8.1.4	Frequency Inversion	289
8.1.5	Combinations	290
8.1.6	Quadratic Pole Response: Resonance	294
8.1.7	The Low- <i>Q</i> Approximation	298

8.1.8	The High- <i>Q</i> Approximation	301
8.1.9	Approximate Roots of an Arbitrary-Degree Polynomial	304
8.2	Analysis of Converter Transfer Functions	309
8.2.1	Example: Transfer Functions of the Buck-Boost Converter	309
8.2.2	Transfer Functions of Some Basic CCM Converters	315
8.2.3	Physical Origins of the RHP Zero in Converters	316
8.3	Graphical Construction of Impedances and Transfer Functions	317
8.3.1	Series Impedances: Addition of Asymptotes	318
8.3.2	Series Resonant Circuit Example	320
8.3.3	Parallel Impedances: Inverse Addition of Asymptotes	322
8.3.4	Parallel Resonant Circuit Example	323
8.3.5	Voltage Divider Transfer Functions: Division of Asymptotes	325
8.4	Graphical Construction of Converter Transfer Functions	327
8.5	Measurement of AC Transfer Functions and Impedances	332
8.6	Summary of Key Points	336
	Problems	337
9	Controller Design	347
9.1	Introduction	347
9.2	Effect of Negative Feedback on the Network Transfer Functions	350
9.2.1	Feedback Reduces the Transfer Functions from Disturbances to the Output	351
9.2.2	Feedback Causes the Transfer Function from the Reference Input to the Output to Be Insensitive to Variations in the Gains in the Forward Path of the Loop	353
9.3	Construction of $1/(1 + T)$ and $T/(1 + T)$	353
9.4	Stability	358
9.4.1	The Phase Margin Test	359
9.4.2	The Nyquist Stability Criterion	360
9.4.3	The Relationship Between Phase Margin and Closed-Loop Damping Factor	370
9.4.4	Transient Response vs. Damping Factor	373
9.4.5	Load Step Response vs. Damping Factor	375
9.5	Regulator Design	376
9.5.1	Lead (<i>PD</i>) compensator	377
9.5.2	Lag (<i>PI</i>) Compensator	380
9.5.3	Combined (<i>PID</i>) Compensator	382
9.5.4	Design Example	383
9.6	Measurement of Loop Gains	392
9.6.1	Voltage Injection	394
9.6.2	Current Injection	396
9.6.3	Measurement of Unstable Systems	397
9.7	Summary of Key Points	398
	Problems	399

Part III Magnetics

10 Basic Magnetics Theory	409
10.1 Review of Basic Magnetics	409
10.1.1 Basic Relationships	409
10.1.2 Magnetic Circuits	415
10.2 Transformer Modeling	418
10.2.1 The Ideal Transformer	419
10.2.2 The Magnetizing Inductance	420
10.2.3 Leakage Inductances	421
10.3 Loss Mechanisms in Magnetic Devices	423
10.3.1 Core Loss	423
10.3.2 Low-Frequency Copper Loss	426
10.4 Eddy Currents in Winding Conductors	426
10.4.1 Introduction to the Skin and Proximity Effects	426
10.4.2 Leakage Flux in Windings	431
10.4.3 Foil Windings and Layers	432
10.4.4 Power Loss in a Layer	434
10.4.5 Example: Power Loss in a Transformer Winding	436
10.4.6 Interleaving the Windings	438
10.4.7 PWM Waveform Harmonics	441
10.5 Several Types of Magnetic Devices, Their B - H Loops, and Core vs. Copper Loss	444
10.5.1 Filter Inductor	444
10.5.2 AC Inductor	446
10.5.3 Transformer	447
10.5.4 Coupled Inductor	448
10.5.5 Flyback Transformer	449
10.6 Summary of Key Points	450
Problems	451
11 Inductor Design	459
11.1 Filter Inductor Design Constraints	459
11.1.1 Maximum Flux Density	461
11.1.2 Inductance	462
11.1.3 Winding Area	462
11.1.4 Winding Resistance	463
11.1.5 The Core Geometrical Constant K_g	463
11.2 The K_g Method: A First-Pass Design	464
11.3 Multiple-Winding Magnetics Design via the K_g Method	465
11.3.1 Window Area Allocation	465
11.3.2 Coupled Inductor Design Constraints	470
11.3.3 First-Pass Design Procedure	472
11.4 Examples	474
11.4.1 Coupled Inductor for a Two-Output Forward Converter	474

11.4.2 CCM Flyback Transformer	476
11.5 Summary of Key Points	481
Problems	482
12 Transformer Design	485
12.1 Transformer Design: Basic Constraints	486
12.1.1 Core Loss	486
12.1.2 Flux Density	486
12.1.3 Copper Loss	487
12.1.4 Total Power Loss vs. ΔB	488
12.1.5 Optimum Flux Density	488
12.2 A First-Pass Transformer Design Procedure	490
12.2.1 Procedure	490
12.3 Examples	492
12.3.1 Example 1: Single-Output Isolated Ćuk Converter	492
12.3.2 Example 2: Multiple-Output Full-Bridge Buck Converter	496
12.4 AC Inductor Design	499
12.4.1 Outline of Derivation	500
12.4.2 First-Pass AC Inductor Design Procedure	501
12.5 Summary	502
Problems	502

Part IV Advanced Modeling, Analysis, and Control Techniques

13 Techniques of Design-Oriented Analysis: The Feedback Theorem	509
13.1 Introduction to Part IV	509
13.2 The Feedback Theorem	510
13.2.1 Basic Result	510
13.2.2 Derivation	513
13.3 Example: Op Amp PD Compensator Circuit	519
13.4 Example: Closed-Loop Regulator	528
13.5 Summary of Key Points	540
Problems	540
14 Circuit Averaging, Averaged Switch Modeling, and Simulation	547
14.1 Circuit Averaging and Averaged Switch Modeling	548
14.1.1 Obtaining a Time-Invariant Circuit	550
14.1.2 Circuit Averaging	550
14.1.3 Perturbation and Linearization	552
14.1.4 Indirect Power	555
14.2 Additional Configurations of Switch Networks	558
14.3 Simulation of Averaged Circuit Models	566
14.3.1 Simulation Model of the Ideal CCM Averaged Switch Network	568
14.3.2 Averaged Switch Modeling and Simulation of Conduction Losses	569
14.3.3 Inclusion of Switch Conduction Losses in Simulations	571
14.3.4 Example: SEPIC DC Conversion Ratio and Efficiency	572

14.3.5 Example: Transient Response of a Buck–Boost Converter	575
14.4 Summary of Key Points	579
Problems	580
15 Equivalent Circuit Modeling of the Discontinuous Conduction Mode	585
15.1 Introduction to DCM Converter Dynamics	586
15.2 DCM Averaged Switch Model	589
15.3 Small-Signal AC Modeling of the DCM Switch Network	600
15.3.1 Example: Control-to-Output Frequency Response of a DCM Boost Converter	607
15.4 Combined CCM/DCM Averaged Switch Simulation Model	608
15.4.1 Example: CCM/DCM SEPIC Frequency Responses	611
15.4.2 Example: Loop Gain and Closed-Loop Responses of a Buck Voltage Regulator	614
15.5 High-Frequency Dynamics of Converters in DCM	618
15.6 Summary of Key Points	622
Problems	622
16 Techniques of Design-Oriented Analysis: Extra Element Theorems	625
16.1 Extra Element Theorem	625
16.1.1 Basic Result	626
16.1.2 Derivation	628
16.1.3 Discussion	631
16.2 EET Examples	632
16.2.1 A Simple Transfer Function	632
16.2.2 An Unmodeled Element	637
16.2.3 SEPIC Example	640
16.2.4 Damping the SEPIC Internal Resonances	644
16.3 The n -Extra Element Theorem	648
16.3.1 Introduction to the n -EET	649
16.3.2 Procedure for DC-Referenced Functions	653
16.4 n -EET Examples	654
16.4.1 Two-Section L – C Filter	654
16.4.2 Bridge-T Filter Example	658
16.5 Frequency Inversion	661
16.5.1 Example: Damped Input Filter	662
16.5.2 Other Special Cases	668
Problems	669
17 Input Filter Design	675
17.1 Introduction	675
17.1.1 Conducted EMI	675
17.1.2 The Input Filter Design Problem	676
17.2 Effect of an Input Filter on Converter Transfer Functions	679
17.2.1 Modified Transfer Functions	679
17.2.2 Discussion	682
17.2.3 Impedance Inequalities	684

17.3	Buck Converter Example	685
17.3.1	Effect of Undamped Input Filter	686
17.3.2	Damping the Input Filter	691
17.4	Design of a Damped Input Filter	693
17.4.1	R_f-C_b Parallel Damping	694
17.4.2	R_f-L_b Parallel Damping	696
17.4.3	R_f-L_b Series Damping	698
17.4.4	Cascading Filter Sections	699
17.4.5	Example: Two Stage Input Filter	700
17.5	Stability Criteria	704
17.5.1	Modified Phase Margin	706
17.5.2	Closed-Loop Input Impedance	711
17.5.3	Discussion	720
17.6	Summary of Key Points	720
	Problems	721
18	Current-Programmed Control	725
18.1	A Simple First-Order Model	728
18.1.1	Simple Model via Algebraic Approach: Buck–Boost Example	729
18.1.2	Averaged Switch Modeling	733
18.2	Oscillation for $D > 0.5$	738
18.3	A More Accurate Model	746
18.3.1	Current-Programmed Controller Model	746
18.3.2	Small-Signal Averaged Model	748
18.4	Current-Programmed Transfer Functions	752
18.4.1	Discussion	754
18.4.2	Current-Programmed Transfer Functions of the CCM Buck Converter	755
18.4.3	Results for Basic Converters	758
18.4.4	Addition of an Input Filter to a Current-Programmed Converter	760
18.5	Simulation of CPM Controlled Converters	763
18.5.1	Simulation Model for CPM Controlled Converters in CCM	764
18.5.2	Combined CCM/DCM Simulation Model	765
18.5.3	Simulation Example: Frequency Responses of a Buck Converter with Current-Programmed Control	766
18.6	Voltage Feedback Loop Around a Current-Programmed Converter	769
18.6.1	System Model	769
18.6.2	Design Example	770
18.7	High-Frequency Dynamics of Current-Programmed Converters	772
18.7.1	Sampled-Data Model	773
18.7.2	First-Order Approximation	776
18.7.3	Second-Order Approximation	778
18.8	Discontinuous Conduction Mode	779
18.9	Average Current-Mode Control	786
18.9.1	System Model and Transfer Functions	788
18.9.2	Design Example: ACM Controlled Boost Converter	791
18.10	Summary of Key Points	798
	Problems	799

19	Digital Control of Switched-Mode Power Converters	805
19.1	Digital Control Loop	806
19.1.1	A/D and DPWM Quantization	807
19.1.2	Sampling and Delays in the Control Loop	810
19.2	Introduction to Discrete-Time Systems	812
19.2.1	Integration in Continuous Time and in Discrete Time	812
19.2.2	z -Transform and Frequency Responses of Discrete-Time Systems	814
19.2.3	Continuous Time to Discrete Time Mapping	817
19.3	Discrete-Time Compensator Design	822
19.3.1	Design Procedure	823
19.3.2	Design Example	824
19.4	Digital Controller Implementation	827
19.4.1	Discrete-Time Compensator Realization	828
19.4.2	Quantization Effects, Digital Pulse-Width Modulators and A/D Converters	830
19.5	Summary of Key Points	838
	Problems	838

Part V Modern Rectifiers and Power System Harmonics

20	Power and Harmonics in Nonsinusoidal Systems	849
20.1	Average Power	850
20.2	Root-Mean-Square (RMS) Value of a Waveform	853
20.3	Power Factor	854
20.3.1	Linear Resistive Load, Nonsinusoidal Voltage	854
20.3.2	Nonlinear Dynamic Load, Sinusoidal Voltage	855
20.4	Power Phasors in Sinusoidal Systems	858
20.5	Harmonic Currents in Three-Phase Systems	859
20.5.1	Harmonic Currents in Three-Phase Four-Wire Networks	859
20.5.2	Harmonic Currents in Three-Phase Three-Wire Networks	861
20.5.3	Harmonic Current Flow in Power Factor Correction Capacitors	862
	Problems	863
21	Pulse-Width Modulated Rectifiers	867
21.1	Properties of the Ideal Rectifier	868
21.2	Realization of a Near-Ideal Rectifier	870
21.2.1	CCM Boost Converter	872
21.2.2	Simulation Example: DCM Boost Rectifier	876
21.2.3	DCM Flyback Converter	878
21.3	Control of the Current Waveform	880
21.3.1	Average Current Control	881
21.3.2	Current-Programmed Control	886
21.3.3	Critical Conduction Mode and Hysteretic Control	889
21.3.4	Nonlinear Carrier Control	892
21.4	Single-Phase Converter Systems Incorporating Ideal Rectifiers	895
21.4.1	Energy Storage	895

21.4.2	Modeling the Outer Low-Bandwidth Control System	900
21.5	RMS Values of Rectifier Waveforms	905
21.5.1	Boost Rectifier Example	906
21.5.2	Comparison of Single-Phase Rectifier Topologies	908
21.6	Modeling Losses and Efficiency in CCM High-Quality Rectifiers	910
21.6.1	Expression for Controller Duty Cycle $d(t)$	913
21.6.2	Expression for the DC Load Current	913
21.6.3	Solution for Converter Efficiency η	915
21.6.4	Design Example	916
21.7	Ideal Three-Phase Rectifiers	917
21.8	Summary of Key Points	923
	Problems	925

Part VI Resonant Converters

22	Resonant Conversion	933
22.1	Sinusoidal Analysis of Resonant Converters	938
22.1.1	Controlled Switch Network Model	938
22.1.2	Modeling the Rectifier and Capacitive Filter Networks	940
22.1.3	Resonant Tank Network	942
22.1.4	Solution of Converter Voltage Conversion Ratio $M = V/V_g$	943
22.2	Examples	944
22.2.1	Series Resonant DC–DC Converter Example	944
22.2.2	Subharmonic Modes of the Series Resonant Converter	946
22.2.3	Parallel Resonant DC–DC Converter Example	947
22.3	Soft Switching	951
22.3.1	Operation of the Full Bridge Below Resonance: Zero-Current Switching	951
22.3.2	Operation of the Full-Bridge Above Resonance: Zero-Voltage Switching	954
22.4	Load-Dependent Properties of Resonant Converters	957
22.4.1	Inverter Output Characteristics	958
22.4.2	Dependence of Transistor Current on Load	960
22.4.3	Dependence of the ZVS/ZCS Boundary on Load Resistance	965
22.4.4	Another Example	967
22.4.5	LLC Example	972
22.4.6	Results for Basic Tank Networks	973
22.5	Exact Characteristics of the Series and Parallel Resonant Converters	976
22.5.1	Series Resonant Converter	977
22.5.2	Parallel Resonant Converter	983
22.6	Summary of Key Points	988
	Problems	988

23 Soft Switching	995
23.1 Soft-Switching Mechanisms of Semiconductor Devices	996
23.1.1 Diode Switching	996
23.1.2 MOSFET Switching	1000
23.1.3 IGBT Switching	1003
23.2 The Zero-Current-Switching Quasi-Resonant Switch Cell	1003
23.2.1 Waveforms of the Half-Wave ZCS Quasi-Resonant Switch Cell	1005
23.2.2 The Average Terminal Waveforms	1009
23.2.3 The Full-Wave ZCS Quasi-Resonant Switch Cell	1014
23.3 Resonant Switch Topologies	1016
23.3.1 The Zero-Voltage-Switching Quasi-Resonant Switch	1017
23.3.2 The Zero-Voltage-Switching Multiresonant Switch	1019
23.3.3 Quasi-Square-Wave Resonant Switches	1020
23.4 Soft Switching in PWM Converters	1025
23.4.1 The Zero-Voltage Transition Full-Bridge Converter	1025
23.4.2 The Auxiliary Switch Approach	1029
23.4.3 Auxiliary Resonant Commutated Pole	1031
23.5 Summary of Key Points	1033
Problems	1034

Appendices

RMS Values of Commonly Observed Converter Waveforms	1037
A.1 Some Common Waveforms	1037
A.2 General Piecewise Waveform	1040
Magnetics Design Tables	1043
B.1 Pot Core Data	1044
B.2 EE Core Data	1045
B.3 EC Core Data	1046
B.4 ETD Core Data	1047
B.5 PQ Core Data	1048
B.6 American Wire Gauge Data	1049
References	1051
Index	1071



1

Introduction

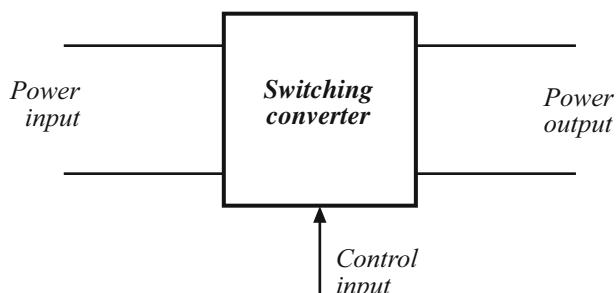
1.1 Introduction to Power Processing

The field of power electronics is concerned with the processing of electrical power using electronic devices [1–7]. The key element is the *switching converter*, illustrated in Fig. 1.1. In general, a switching converter contains power input and control input ports, and a power output port. The raw input power is processed as specified by the control input, yielding the conditioned output power. One of several basic functions can be performed [2]. In a *dc–dc converter*, the dc input voltage is converted to a dc output voltage having a larger or smaller magnitude, possibly with opposite polarity or with isolation of the input and output ground references. In an *ac–dc rectifier*, an ac input voltage is rectified, producing a dc output voltage. The dc output voltage and/or ac input current waveform may be controlled. The inverse process, *dc–ac inversion*, involves transforming a dc input voltage into an ac output voltage of controllable magnitude and frequency. *Ac–ac cycloconversion* involves converting an ac input voltage to a given ac output voltage of controllable magnitude and frequency.

Control is invariably required. It is nearly always desired to produce a well-regulated output voltage, in the presence of variations in the input voltage and load current. As illustrated in Fig. 1.2, a controller block is an integral part of any power processing system.

High efficiency is essential in any power processing application. The primary reason for this is usually not the desire to save money on one's electric bills, nor to conserve energy, in spite of the nobility of such pursuits. Rather, high efficiency converters are necessary because construction of low-efficiency converters, producing substantial output power, is impractical. The efficiency of a converter having output power P_{out} and input power P_{in} is

Fig. 1.1 The switching converter, a basic power processing block



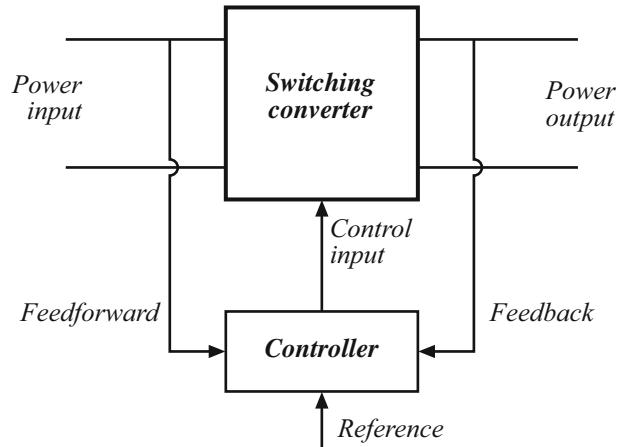


Fig. 1.2 A controller is generally required

$$\eta = \frac{P_{out}}{P_{in}} \quad (1.1)$$

The power lost in the converter $P_{loss} = P_{in} - P_{out}$ can be related to the output power as:

$$Q = \frac{P_{out}}{P_{loss}} = \frac{\eta}{1 - \eta} \quad (1.2)$$

Equation (1.2) is plotted in Fig. 1.3. The quantity $Q = P_{out}/P_{loss}$ is a fundamental measure of the quality of the power converter. The loss P_{loss} is converted into heat by the converter circuit elements and must be removed by a cooling system. In most applications, the maximum output power is limited by the capacity of the cooling system to remove this heat, and this limits the maximum allowable output power. If the loss power is substantial, then a large and expensive cooling system is needed, the circuit elements within the converter may operate at high temperature, and the system reliability may be reduced. Indeed, at high output powers, it may be impossible to adequately cool the converter elements using a given cooling technology.

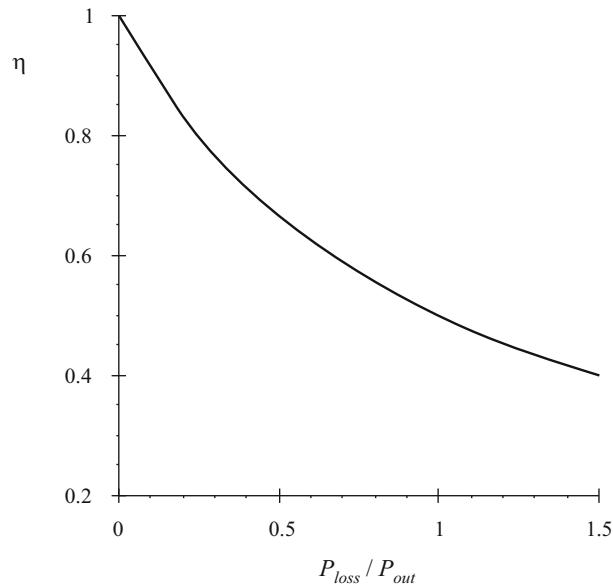


Fig. 1.3 Converter power loss vs. efficiency

Increasing the efficiency is the key to obtaining higher output powers. For example, if the converter efficiency is 90%, then the converter loss power is equal to only 11% of the output power and $P_{out}/P_{loss} = 9$. For a given cooling system technology and size, there is a maximum amount of P_{loss} that can be handled. With this maximum loss, the maximum output power then depends on the converter Q and efficiency according to Fig. 1.3. It can be seen that the output power can be increased if the efficiency is increased. In this way, Q (and, less directly, efficiency η) is a good measure of the success of a given converter technology. Figure 1.4 illustrates a converter that processes a large amount of power, with very high Q . Since very little power is lost, the converter elements can be packaged with high density and a small cooling system, leading to a converter of small size and weight, and of low temperature rise.

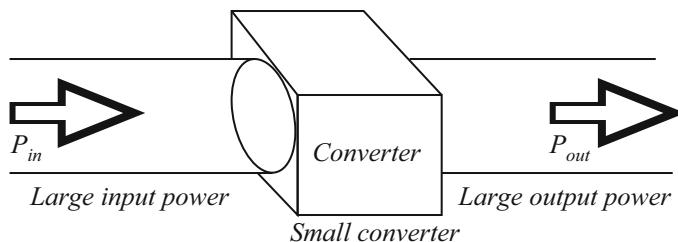


Fig. 1.4 A goal of current technology is to construct converters of small size and weight, which process substantial power at high efficiency

How can we build a circuit that changes the voltage, yet dissipates negligible power? The various conventional circuit elements are illustrated in Fig. 1.5. The available circuit elements fall broadly into the classes of resistive elements, capacitive elements, magnetic devices including inductors and transformers, semiconductor devices operated in the linear mode (for example, as class A or class B amplifiers), and semiconductor devices operated in the switched mode (such as in logic devices where transistors operate in either the fully on or fully off states). In conventional signal processing applications, where efficiency is not the primary concern, magnetic devices are usually avoided wherever possible, because of their large size and the difficulty

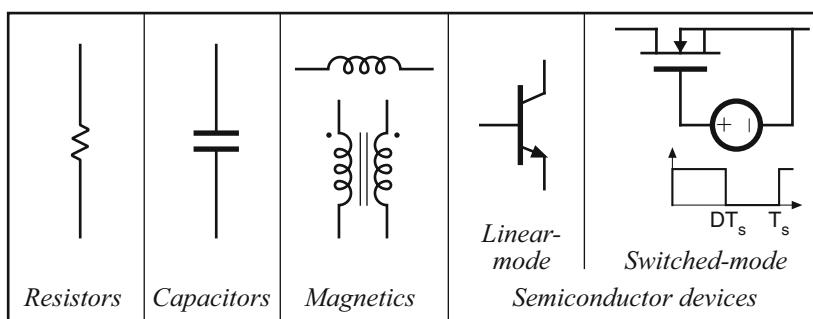


Fig. 1.5 Devices available to the circuit designer [2]

of incorporating them into integrated circuits. In contrast, capacitors and magnetic devices are important elements of switching converters, because ideally they do not consume power. It is the resistive element, as well as the linear-mode semiconductor device, that is avoided [2]. Switched-mode semiconductor devices are also employed. When a semiconductor device operates in the off state, its current is zero and hence its power dissipation is zero. When the semiconductor device operates in the on (saturated) state, its voltage drop is small and hence its power dissipation is also small. In either event, the power dissipated by the semiconductor device is low. So capacitive and inductive elements, as well as switched-mode semiconductor devices, are available for synthesis of high-efficiency converters.

Let us now consider how to construct the simple dc–dc converter example illustrated in Fig. 1.6. The input voltage V_g is 100 V. It is desired to supply 50 V to an effective 5Ω load, such that the dc load current is 10 A.

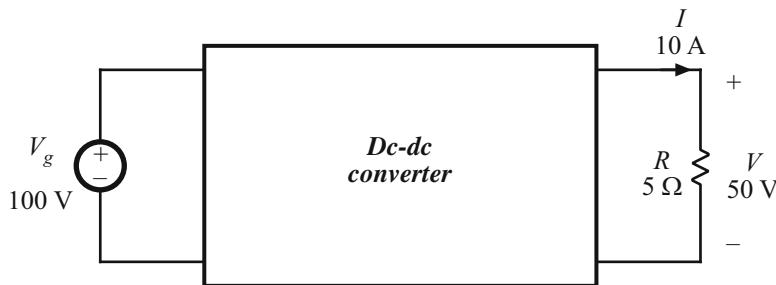


Fig. 1.6 A simple power processing example: construction of a 500 W dc–dc converter

Introductory circuits textbooks describe a low-efficiency method to perform the required function: the voltage divider circuit illustrated in Fig. 1.7a. The dc–dc converter then consists simply of a variable resistor, whose value is adjusted such that the required output voltage is obtained. The load current flows through the variable resistor. For the specified voltage and current levels, the power P_{loss} dissipated in the variable resistor equals the load power $P_{out} = 500$ W. The source V_g supplies power $P_{in} = 1000$ W. Figure 1.7b illustrates a more practical implementation known as the linear series-pass regulator. The variable resistor of Fig. 1.7a is replaced by a linear-mode power transistor, whose base current is controlled by a feedback system such that the desired output voltage is obtained. The power dissipated by the linear-mode transistor of Fig. 1.7b is approximately the same as the 500 W lost by the variable resistor in Fig. 1.7a. Series-pass linear regulators generally find modern application only at low power levels of a few watts.

Figure 1.8 illustrates another approach. A single-pole double-throw (SPDT) switch is connected as shown. The switch output voltage $v_s(t)$ is equal to the converter input voltage V_g when the switch is in position 1, and is equal to zero when the switch is in position 2. The switch position is varied periodically, as illustrated in Fig. 1.9, such that $v_s(t)$ is a rectangular waveform having frequency f_s and period $T_s = 1/f_s$. The duty cycle D is defined as the fraction of time in which the switch occupies position 1. Hence, $0 \leq D \leq 1$. In practice, the SPDT switch is realized using switched-mode semiconductor devices, which are controlled such that the SPDT switching function is attained.

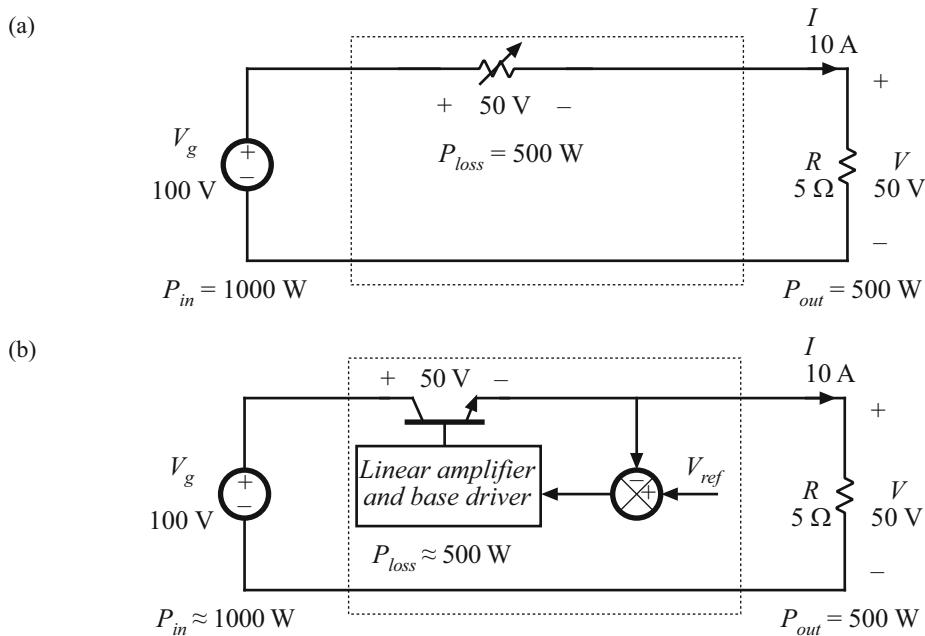


Fig. 1.7 Changing the dc voltage via dissipative means: (a) voltage divider, (b) series pass regulator

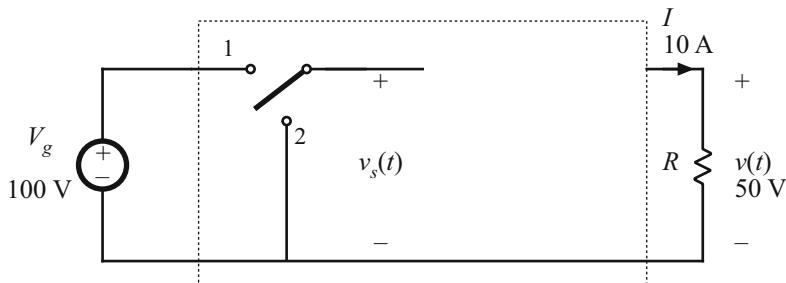


Fig. 1.8 Insertion of SPDT switch which changes the dc component of the voltage

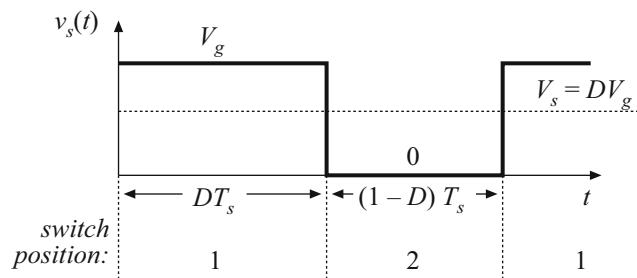


Fig. 1.9 Switch output voltage waveform $v_s(t)$

The switch changes the dc component of the voltage. Recall from Fourier analysis that the dc component of a periodic waveform is equal to its average value. Hence, the dc component of $v_s(t)$ is

$$V_s = \frac{1}{T_s} \int_0^{T_s} v_s(t) dt = DV_g \quad (1.3)$$

Thus, the switch changes the dc voltage, by a factor equal to the duty cycle D . To convert the input voltage $V_g = 100$ V into the desired output voltage of $V = 50$ V, a duty cycle of $D = 0.5$ is required.

Again, the power dissipated by the switch is ideally zero. When the switch contacts are closed, then their voltage is zero and hence the power dissipation is zero. When the switch contacts are open, then the current is zero and again the power dissipation is zero. So we have succeeded in changing the dc voltage component, using a device that is ideally lossless.

In addition to the desired dc component V_s , the switch output voltage waveform $v_s(t)$ also contains undesirable harmonics of the switching frequency. In most applications, these harmonics must be removed, such that the output voltage $v(t)$ is essentially equal to the dc component $V = V_s$. A low-pass filter can be employed for this purpose. Figure 1.10 illustrates the introduction of a single-section $L-C$ low-pass filter. If the filter corner frequency f_0 is sufficiently less than the switching frequency f_s , then the filter essentially passes only the dc component of $v_s(t)$. To the extent that the switch, inductor, and capacitor elements are ideal, the efficiency of this dc–dc converter can approach 100%.

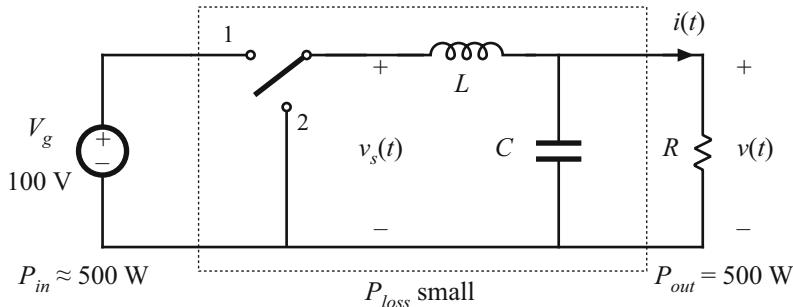


Fig. 1.10 Addition of $L-C$ low-pass filter, for removal of switching harmonics

In Fig. 1.11, a control system is introduced for regulation of the output voltage. Since the output voltage is a function of the switch duty cycle, a control system can be constructed that varies the duty cycle to cause the output voltage to follow a given reference. Figure 1.11 also illustrates a typical way in which the SPDT switch is realized using switched-mode semiconductor devices. The converter power stage developed in Figs. 1.8, 1.9, 1.10, 1.11 is called the *buck converter*, because it reduces the dc voltage.

Converters can be constructed that perform other power processing functions. For example, Fig. 1.12 illustrates a circuit known as the *boost converter*, in which the positions of the inductor and SPDT switch are interchanged. This converter is capable of producing output voltages that are greater in magnitude than the input voltage. In general, any given input voltage can be converted into any desired output voltage, using a converter containing switching devices embedded within a network of reactive elements.

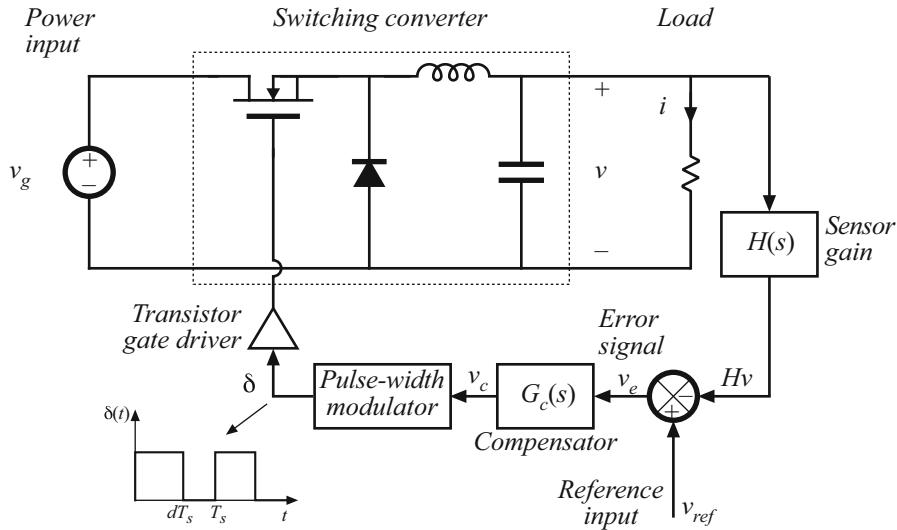


Fig. 1.11 Addition of control system to regulate the output voltage

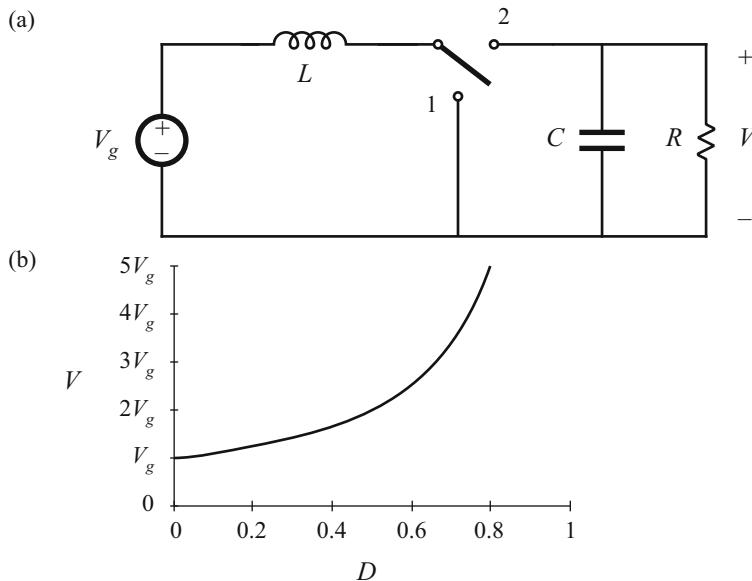


Fig. 1.12 The boost converter: (a) ideal converter circuit, (b) output voltage V vs. transistor duty cycle D

Figure 1.13a illustrates a simple dc-1Øac inverter circuit. As illustrated in Fig. 1.13b, the switch duty cycle is modulated sinusoidally. This causes the switch output voltage $v_s(t)$ to contain a low-frequency sinusoidal component. The $L-C$ filter cutoff frequency f_0 is selected to pass the desired low-frequency components of $v_s(t)$, but to attenuate the high-frequency switch-

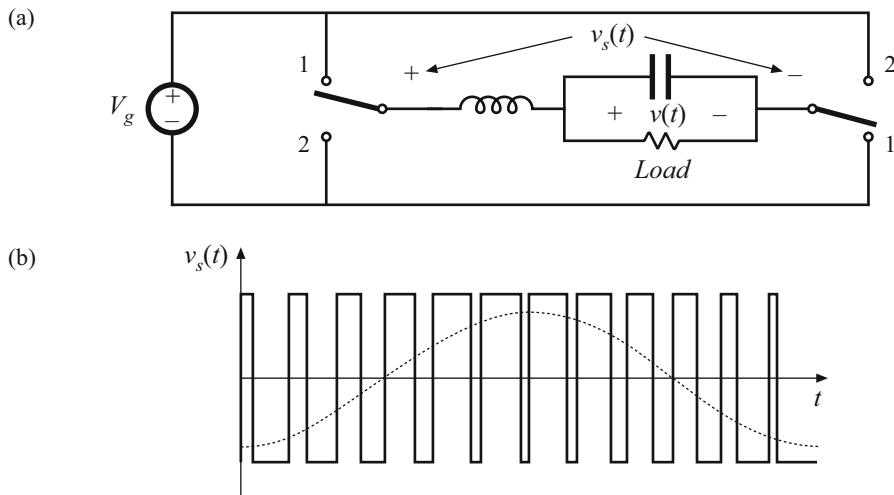


Fig. 1.13 A bridge-type dc-1φac inverter: (a) ideal inverter circuit, (b) typical pulse-width-modulated switch voltage waveform $v_s(t)$, and its low-frequency component

ing harmonics. The controller modulates the duty cycle such that the desired output frequency and voltage magnitude are obtained.

1.2 Several Applications of Power Electronics

The power levels encountered in high-efficiency switching converters range from (1) less than one watt, in dc–dc converters within battery-operated portable equipment, to (2) tens, hundreds, or thousands of watts in power supplies for computers and office equipment, to (3) kilowatts to megawatts, in variable-speed motor drives, to (4) roughly 1000 megawatts in the rectifiers and inverters that interface dc transmission lines to the ac utility power system. The converter systems of several applications are illustrated in this section.

A power supply system for a laptop computer is illustrated in Fig. 1.14. A lithium battery powers the system, and several dc–dc converters change the battery voltage into the voltages required by the loads. A buck converter produces the low-voltage dc required by the microprocessor. A boost converter increases the battery voltage to the level needed by the disk drive. An inverter produces high-voltage high-frequency ac to drive lamps that light the display. A charger with transformer isolation converts the ac line voltage into dc to charge the battery. The converter switching frequencies are typically in the vicinity of several hundred kilohertz; this leads to substantial reductions in the size and weight of the reactive elements. *Power management* is used, to control sleep modes in which power consumption is reduced and battery life is extended. In a *distributed power system*, an intermediate dc voltage appears at the computer backplane. Each printed circuit card contains high-density dc–dc converters that produce locally regulated low voltages. Commercial applications of power electronics include off-line power systems for computers, office and laboratory equipment, uninterruptable ac power supplies, and electronic ballasts for gas discharge lighting.

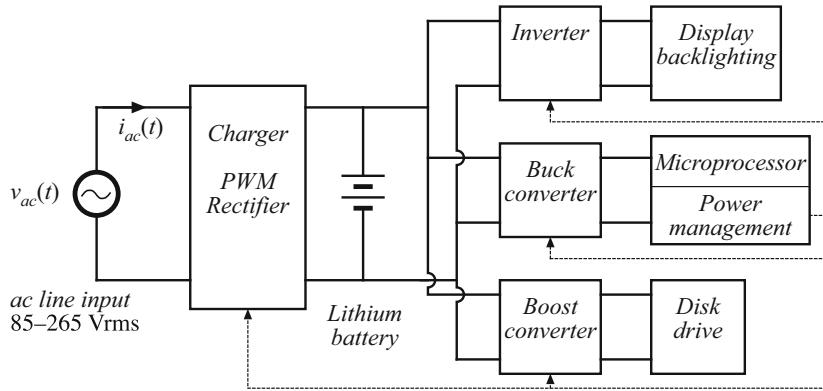


Fig. 1.14 A laptop computer power supply system

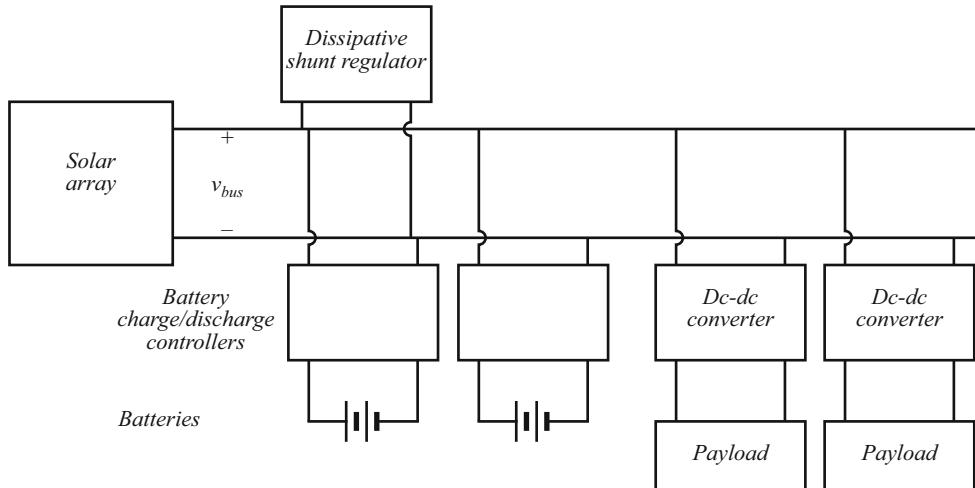


Fig. 1.15 Power system of an earth-orbiting spacecraft

Figure 1.15 illustrates a power system of an earth-orbiting spacecraft. A solar array produces the main power bus voltage V_{bus} . DC-DC converters convert V_{bus} to the regulated voltages required by the spacecraft payloads. Battery charge/discharge controllers interface the main power bus to batteries; these controllers may also contain dc-dc converters. Aerospace applications of power electronics include the power systems of aircraft, spacecraft, and other aerospace vehicles.

Figure 1.16 illustrates an electric vehicle power and drive system. Batteries are charged by a converter that draws high power-factor sinusoidal current from a single-phase or three-phase ac line. The batteries supply power to variable-speed ac motors to propel the vehicle. The speeds of the ac motors are controlled by variation of the electrical input frequency. Inverters produce three-phase ac output voltages of variable frequency and variable magnitude, to control the speed of the ac motors and the vehicle. A dc-dc converter steps down the battery voltage

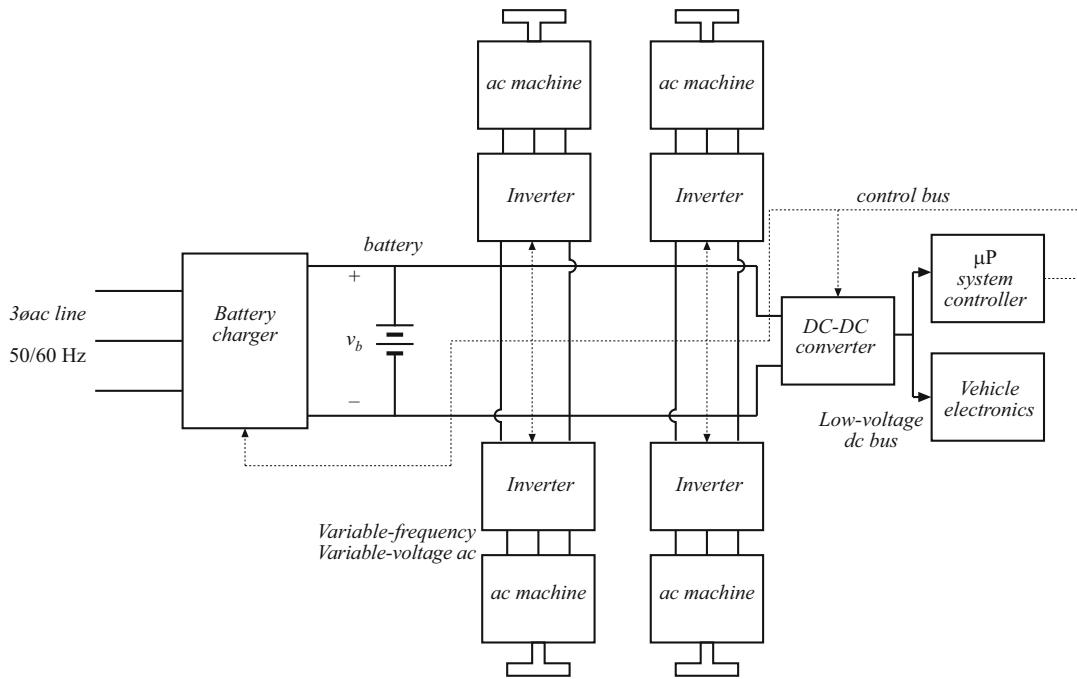


Fig. 1.16 An electric vehicle power and drive system

to the lower dc levels required by the electronics of the system. Applications of motor drives include speed control of industrial processes, such as control of compressors, fans, and pumps; transportation applications such as electric vehicles, subways, and locomotives; and motion control applications in areas such as computer peripherals and industrial robots.

Power electronics also finds application in other diverse industries, including dc power supplies, uninterruptable power supplies, and battery chargers for portable electronics, electric vehicles, and the telecommunications industry; inverter systems for renewable energy generation applications such as wind and photovoltaic power; and utility power systems applications including high-voltage dc transmission and static VAR (reactive volt-ampere) compensators.

1.3 Elements of Power Electronics

One of the things that makes the power electronics field interesting is its incorporation of concepts from a diverse set of fields, including:

- analog circuits
- electronic devices
- control systems
- power systems
- magnetics
- electric machines
- numerical simulation

Thus, the practice of power electronics requires a broad electrical engineering background. In addition, there are fundamental concepts that are unique to the power electronics field, and that require specialized study.

The presence of high-frequency switching makes the understanding of switched-mode converters not straightforward. Hence, converter modeling is central to the study of power electronics. As introduced in Eq. (1.3), the dc component of a periodic waveform is equal to its average value. This ideal can be generalized, to predict the dc components of all converter waveforms via averaging. In Part I of this book, averaged equivalent circuit models of converters operating in steady state are derived. These models not only predict the basic ideal behavior of switched-mode converters, but also model efficiency and losses. Realization of the switching elements, using power semiconductor devices, is also discussed.

Design of the converter control system requires models of the converter dynamics. In Part II of this book, the averaging technique is extended, to describe low-frequency variations in the converter waveforms. Small-signal equivalent circuit models are developed, which predict the control-to-output and line-to-transfer functions, as well as other ac quantities of interest. These models are then employed to design converter control systems and to lend an understanding of the well-known current-programmed control technique.

The magnetic elements are key components of any switching converter. The design of high-power high-frequency magnetic devices having high efficiency and small size and weight is central to most converter technologies. High-frequency power magnetics design is discussed in Part III.

More advanced control, design-oriented analysis, and simulation are the topics of Part IV. The Feedback Theorem, Extra Element Theorem, and n -Extra Element Theorem are techniques of design-oriented analysis that enable analytical solution and design of complex systems, based on the ideas of null double injection. These techniques are applied to converter control systems, damping internal resonances, designing input filters, and analyzing peak- and average-current mode control. The average switch modeling approach to converter modeling is developed, and is employed to model converter dynamics in the discontinuous conduction mode and to perform SPICE-based averaged simulations of converters. High-frequency converter dynamics are considered based on the ideas of converter sampled-data modeling; this explains observed behavior of discontinuous conduction mode converters and of current programmed converters at frequencies approaching half of the switching frequency. Digital control of switching converters is now implemented in a variety of converter applications; analog-to-digital converters, digital pulse-width modulators, and digital compensators are modeled and discussed.

Pollution of the ac power system by rectifier harmonics is a recognized problem. As a result, many converter systems now incorporate low-harmonic rectifiers, which draw sinusoidal currents from the utility system. These modern rectifiers are considerably more sophisticated than the conventional diode bridge: they may contain high-frequency switched-mode converters, with control systems that regulate the ac line current waveform. Modern rectifier technology is treated in Part V.

Resonant converters employ quasi-sinusoidal waveforms, as opposed to the rectangular waveforms of the buck converter illustrated in Fig. 1.9. These resonant converters find application where high-frequency inverters and converters are needed. Resonant converters are modeled in Part VI. Their loss mechanisms, including the processes of zero-voltage switching and zero-current switching, are discussed.

Part I

Converters in Equilibrium



Principles of Steady-State Converter Analysis

2.1 Introduction

In the previous chapter, the buck converter was introduced as a means of reducing the dc voltage, using only nondissipative switches, inductors, and capacitors. The switch produces a rectangular waveform $v_s(t)$ as illustrated in Fig. 2.1. The voltage $v_s(t)$ is equal to the dc input voltage V_g when the switch is in position 1, and is equal to zero when the switch is in position 2. In practice, the switch is realized using power semiconductor devices, such as transistors and diodes, which are controlled to turn on and off as required to perform the function of the ideal switch. The switching frequency f_s , equal to the inverse of the switching period T_s , generally lies in the range of 1 kHz–1 MHz, depending on the switching speed of the semiconductor devices. The

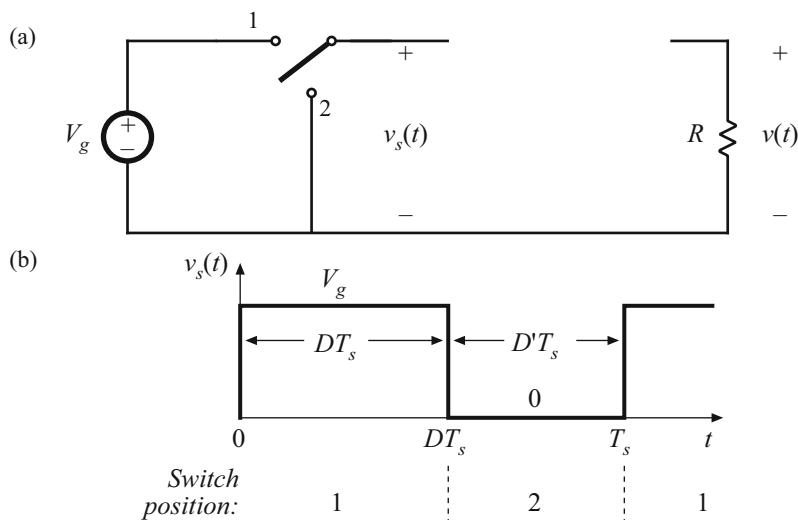
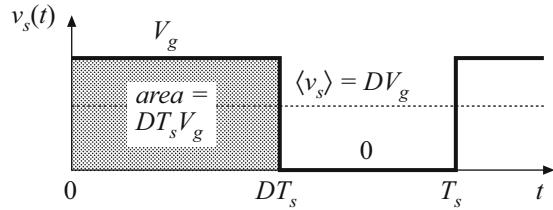


Fig. 2.1 Ideal switch, (a), used to reduce the voltage dc component, and (b) its output voltage waveform $v_s(t)$

Fig. 2.2 Determination of the switch output voltage dc component, by integrating and dividing by the switching period



duty ratio D is the fraction of time that the switch spends in position 1, and is a number between zero and one. The complement of the duty ratio, D' , is defined as $(1 - D)$.

The switch reduces the dc component of the voltage: the switch output voltage $v_s(t)$ has a dc component that is less than the converter dc input voltage V_g . From Fourier analysis, we know that the dc component of $v_s(t)$ is given by its average value $\langle v_s \rangle$, or

$$\langle v_s \rangle = \frac{1}{T_s} \int_0^{T_s} v_s(t) dt \quad (2.1)$$

As illustrated in Fig. 2.2, the integral is given by the area under the curve, or $DT_s V_g$. The average value is therefore

$$\langle v_s \rangle = \frac{1}{T_s} (DT_s V_g) = DV_g \quad (2.2)$$

So the average value, or dc component, of $v_s(t)$ is equal to the duty cycle times the dc input voltage V_g . The switch reduces the dc voltage by a factor of D .

What remains is to insert a low-pass filter as shown in Fig. 2.3. The filter is designed to pass the dc component of $v_s(t)$, but to reject the components of $v_s(t)$ at the switching frequency and its harmonics. To accomplish this, we design the filter such that its cutoff frequency is much lower than the switching frequency. The output voltage $v(t)$ is then essentially equal to the dc component of $v_s(t)$:

$$v \approx \langle v_s \rangle = DV_g \quad (2.3)$$

The converter of Fig. 2.3 has been realized using lossless elements. To the extent that they are ideal, the inductor, capacitor, and switch do not dissipate power. For example, when the switch is closed, its voltage drop is zero, and the current is zero when the switch is open. In either

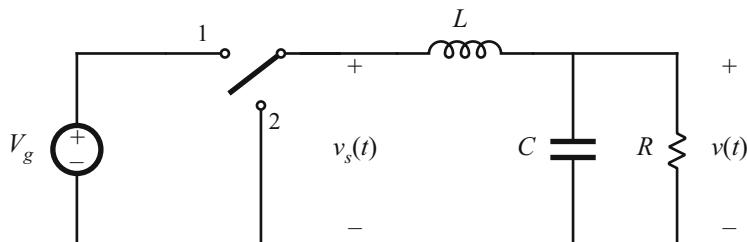


Fig. 2.3 Insertion of low-pass filer, to remove the switching harmonics and pass only the dc component of $v_s(t)$ to the output

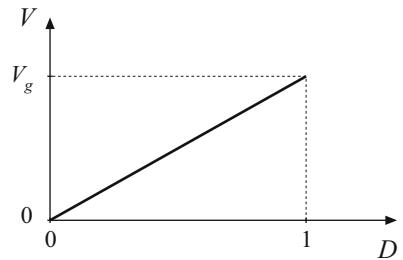


Fig. 2.4 Buck converter dc output voltage V vs. duty cycle D

case, the power dissipated by the switch is zero. Hence, efficiencies approaching 100% can be obtained. So to the extent that the components are ideal, we can realize our objective of changing dc voltage levels using a lossless network.

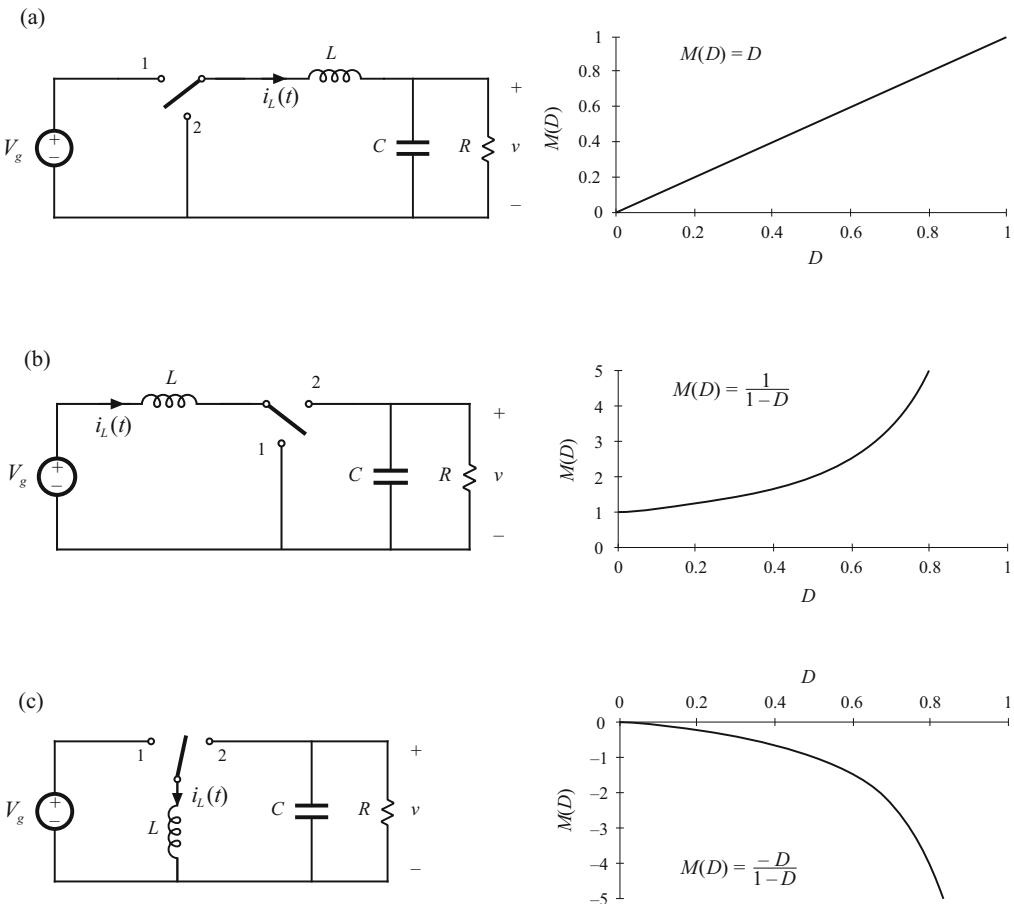


Fig. 2.5 Three basic converters and their dc conversion ratios $M(D) = V/V_g$: (a) buck, (b) boost, (c) buck-boost

The network of Fig. 2.3 also allows control of the output. Figure 2.4 is the control characteristic of the converter. The output voltage, given by Eq. (2.3), is plotted vs. duty cycle. The buck converter has a linear control characteristic. Also, the output voltage is less than or equal to the input voltage, since $0 \leq D \leq 1$. Feedback systems are often constructed that adjust the duty cycle D to regulate the converter output voltage. Inverters or power amplifiers can also be built, in which the duty cycle varies slowly with time and the output voltage follows.

The buck converter is just one of many possible switching converters. Two other commonly used converters, which perform different voltage conversion functions, are illustrated in Fig. 2.5. In the boost converter, the positions of the inductor and switch are reversed. It is shown later in this chapter that the boost converter steps the voltage up: $V \geq V_g$. Another converter, the buck-boost converter, can either increase or decrease the magnitude of the voltage, but the polarity is inverted. So with a positive input voltage, the ideal buck-boost converter can produce a negative output voltage of any magnitude. It may at first be surprising that dc output voltages can be produced that are greater in magnitude than the input, or that have opposite polarity. But it is indeed possible to produce any desired dc output voltage using a passive network of only inductors, capacitors, and embedded switches.

In the above discussion, it was possible to derive an expression for the output voltage of the buck converter, Eq. (2.3), using some simple arguments based on Fourier analysis. However, it may not be immediately obvious how to directly apply these arguments to find the dc output voltage of the boost, buck-boost, or other converters. The objective of this chapter is the development of a more general method for analyzing any switching converter comprised of a network of inductors, capacitors, and switches [4, 8–13].

The principles of *inductor volt-second balance* and *capacitor charge balance* are derived; these can be used to solve for the inductor currents and capacitor voltages of switching converters. A useful approximation, the *small-ripple* or *linear-ripple approximation*, greatly facilitates the analysis. Some simple methods for selecting the filter element values are also discussed.

2.2 Inductor Volt-Second Balance, Capacitor Charge Balance, and the Small-Ripple Approximation

Let us more closely examine the inductor and capacitor waveforms in the buck converter of Fig. 2.6. It is impossible to build a perfect low-pass filter that allows the dc component to pass but completely removes the components at the switching frequency and its harmonics. So the

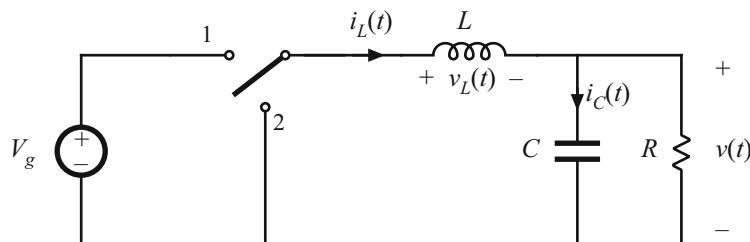


Fig. 2.6 Buck converter circuit, with the inductor voltage $v_L(t)$ and capacitor voltage $v_C(t)$ waveforms specifically identified

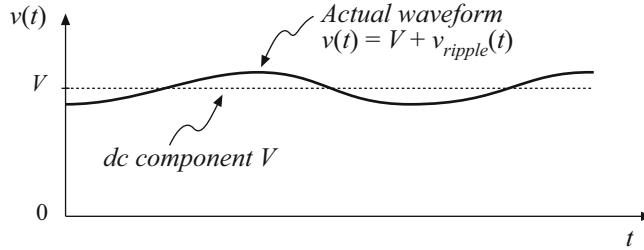


Fig. 2.7 Output voltage waveform $v(t)$, consisting of dc component V and switching ripple $v_{\text{ripple}}(t)$

low-pass filter must allow at least some small amount of the high-frequency harmonics generated by the switch to reach the output. Hence, in practice the output voltage waveform $v(t)$ appears as illustrated in Fig. 2.7, and can be expressed as

$$v(t) = V + v_{\text{ripple}}(t) \quad (2.4)$$

So the actual output voltage $v(t)$ consists of the desired dc component V , plus a small undesired ac component $v_{\text{ripple}}(t)$ arising from the incomplete attenuation of the switching harmonics by the low-pass filter. The magnitude of $v_{\text{ripple}}(t)$ has been exaggerated in Fig. 2.7.

The output voltage switching ripple should be small in any well-designed converter, since the object is to produce a dc output. For example, in a computer power supply having a 3.3 V output, the switching ripple is normally required to be less than a few tens of millivolts, or less than 1% of the dc component V . So it is nearly always a good approximation to assume that the magnitude of the switching ripple is much smaller than the dc component:

$$\|v_{\text{ripple}}\| \ll V \quad (2.5)$$

Therefore, the output voltage $v(t)$ is well approximated by its dc component V , with the small-ripple term $v_{\text{ripple}}(t)$ neglected:

$$v(t) \approx V \quad (2.6)$$

This approximation, known as the *small-ripple approximation*, or the *linear-ripple approximation*, greatly simplifies the analysis of the converter waveforms and is used throughout this book. With this approximation, we replace the exponential or damped sinusoidal expressions for the inductor and capacitor waveforms with simpler linear waveforms; this approximation is justified provided that the switching period is much shorter than the natural time constants of the circuit. The small-ripple approximation is applied to the inductor currents and capacitor voltages of the converter, which are continuous variables. It must not be applied to discontinuous waveforms of the converter, such as the switch voltage, switch current, or inductor voltage.

Next let us analyze the inductor current waveform. We can find the inductor current by integrating the inductor voltage waveform. With the switch in position 1, the left side of the inductor is connected to the input voltage V_g , and the circuit reduces to Fig. 2.8a. It should be noted here that the reference polarities of $v_L(t)$ and $i_L(t)$ have been carefully defined in Fig. 2.6, and these reference polarities are consistently followed in the circuits of Fig. 2.8a,b. The inductor voltage $v_L(t)$ is given by

$$v_L = V_g - v(t) \quad (2.7)$$

As described above, the output voltage $v(t)$ consists of the dc component V , plus a small ac ripple term $v_{\text{ripple}}(t)$. We can make the small-ripple approximation here, Eq. (2.6), to replace $v(t)$ with its dc component V :

$$v_L \approx V_g - V \quad (2.8)$$

So with the switch in position 1, the inductor voltage is essentially constant and equal to $V_g - V$, as shown in Fig. 2.9. By knowledge of the inductor voltage waveform, the inductor current can be found by use of the definition

$$v_L(t) = L \frac{di_L(t)}{dt} \quad (2.9)$$

Thus, during the first interval, when $v_L(t)$ is approximately $(V_g - V)$, the slope of the inductor current waveform is

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} \approx \frac{V_g - V}{L} \quad (2.10)$$

which follows by dividing Eq. (2.9) by L , and substituting Eq. (2.8). Since the inductor voltage $v_L(t)$ is essentially constant while the switch is in position 1, the inductor current slope is also essentially constant and the inductor current increases linearly.

Similar arguments apply during the second subinterval, when the switch is in position 2. The left side of the inductor is then connected to ground, leading to the circuit of Fig. 2.8b. It is important to consistently define the polarities of the inductor current and voltage; in particular, the polarity of $v_L(t)$ is defined consistently in Figs. 2.7, 2.8a,b. So the inductor voltage during the second subinterval is given by

$$v_L(t) = -v(t) \quad (2.11)$$

Use of the small-ripple approximation, Eq. (2.6), leads to

$$v_L(t) \approx -V \quad (2.12)$$

So the inductor voltage is also essentially constant while the switch is in position 2, as illustrated in Fig. 2.9. Substitution of Eq. (2.12) into Eq. (2.9) and solution for the slope of the inductor current yields

$$\frac{di_L(t)}{dt} \approx -\frac{V}{L} \quad (2.13)$$

Hence, during the second subinterval the inductor current changes with a negative and essentially constant slope.

We can now sketch the inductor current waveform (Fig. 2.10). The inductor current begins at some initial value $i_L(0)$. During the first subinterval, with the switch in position 1, the inductor

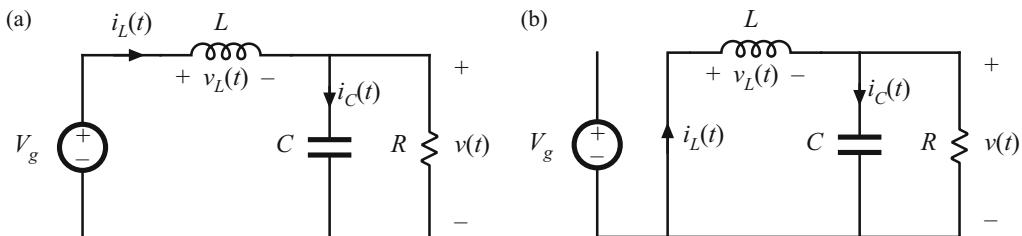


Fig. 2.8 Buck converter circuit: (a) while the switch is in position 1, (b) while the switch is in position 2

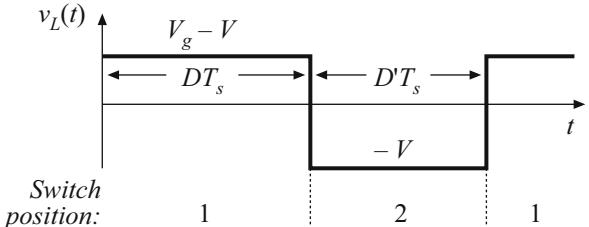
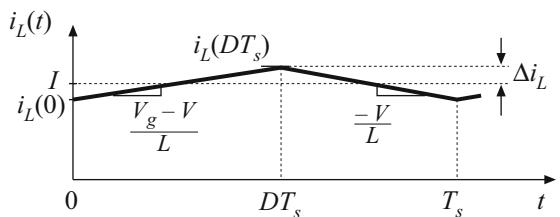


Fig. 2.9 Steady-state inductor voltage waveform, buck converter



current increases with the slope given in Eq. (2.10). At time $t = DT_s$, the switch changes to position 2. The current then decreases with the constant slope given by Eq. (2.13). At time $t = T_s$, the switch changes back to position 1, and the process repeats.

It is of interest to calculate the inductor current ripple Δi_L . As illustrated in Fig. 2.10, the peak inductor current is equal to the dc component I plus the peak-to-average ripple Δi_L . This peak current flows through not only the inductor, but also through the semiconductor devices that comprise the switch. Knowledge of the peak current is necessary when specifying the ratings of these devices.

Since we know the slope of the inductor current during the first subinterval, and we also know the length of the first subinterval, we can calculate the ripple magnitude. The $i_L(t)$ waveform is symmetrical about I , and hence during the first subinterval the current increases by $2\Delta i_L$ (since Δi_L is the peak ripple, the peak-to-peak ripple is $2\Delta i_L$). So the change in current, $2\Delta i_L$, is equal to the slope (the applied inductor voltage divided by L) times the length of the first subinterval (DT_s):

$$\begin{aligned} \text{(change in } i_L) &= \text{(slope)}(\text{length of subinterval}) \\ (2\Delta i_L) &= \left(\frac{V_g - V}{L} \right) (DT_s) \end{aligned} \quad (2.14)$$

Solution for Δi_L yields

$$\Delta i_L = \frac{V_g - V}{2L} DT_s \quad (2.15)$$

Typical values of Δi_L lie in the range of 10%–20% of the full-load value of the dc component I . It is undesirable to allow Δi_L to become too large; doing so would increase the peak currents of the inductor and of the semiconductor switching devices, and would increase their size and cost. So by design the inductor current ripple is also usually small compared to the dc component I . The small-ripple approximation $i_L(t) \approx I$ is usually justified for the inductor current.

The inductor value can be chosen such that a desired current ripple Δi_L is attained. Solution of Eq. (2.15) for the inductance L yields

$$L = \frac{V_g - V}{2\Delta i_L} DT_s \quad (2.16)$$

This equation is commonly used to select the value of inductance in the buck converter.

It is entirely possible to solve converters exactly, without use of the small-ripple approximation. For example, one could use the Laplace transform to write expressions for the waveforms of the circuits of Fig. 2.8a,b. One could then invert the transforms, match boundary conditions, and find the periodic steady-state solution of the circuit. Having done so, one could then find the dc components of the waveforms and the peak values. But this is a great deal of work, and the results are nearly always intractable. Besides, the extra work involved in writing equations that exactly describe the ripple is a waste of time, since the ripple is small and is undesired. The small-ripple approximation is easy to apply, and quickly yields simple expressions for the dc components of the converter waveforms.

The inductor current waveform of Fig. 2.10 is drawn under steady-state conditions, with the converter operating in equilibrium. Let us consider next what happens to the inductor current when the converter is first turned on. Suppose that the inductor current and output voltage are initially zero, and an input voltage V_g is then applied. As shown in Fig. 2.11, $i_L(0)$ is zero. During the first subinterval, with the switch in position 1, we know that the inductor current will increase, with a slope of $(V_g - v)/L$ and with v initially zero. Next, with the switch in position 2, the inductor current will change with a slope of $-v/L$; since v is initially zero, this slope is essentially zero. It can be seen that there is a net increase in inductor current over the first switching period, because $i_L(T_s)$ is greater than $i_L(0)$. Since the inductor current flows to the output, the output capacitor will charge slightly, and v will increase slightly. The process repeats during the second and succeeding switching periods, with the inductor current increasing during each subinterval 1 and decreasing during each subinterval 2.

As the output capacitor continues to charge and v increases, the slope during subinterval 1 decreases while the slope during subinterval 2 becomes more negative. Eventually, the point is reached where the increase in inductor current during subinterval 1 is equal to the decrease in inductor current during subinterval 2. There is then no net change in inductor current over a

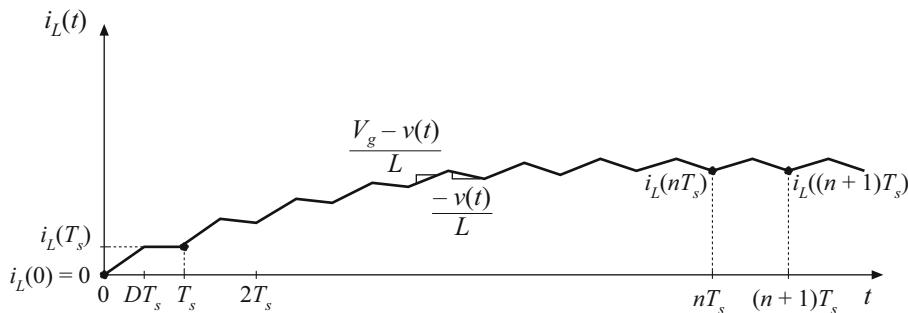


Fig. 2.11 Inductor current waveform during converter turn-on transient

complete switching period, and the converter operates in steady state. The converter waveforms are periodic: $i_L(nT_s) = i_L((n+1)T_s)$. From this point on, the inductor current waveform appears as in Fig. 2.10.

The requirement that, in equilibrium, the net change in inductor current over one switching period be zero leads us to a way to find steady-state conditions in any switching converter: the principle of *inductor volt-second balance*. Given the defining relation of an inductor:

$$v_L(t) = L \frac{di_L(t)}{dt} \quad (2.17)$$

Integration over one complete switching period, say from $t = 0$ to T_s , yields

$$i_L(T_s) - i_L(0) = \frac{1}{L} \int_0^{T_s} v_L(t) dt \quad (2.18)$$

This equation states that the net change in inductor current over one switching period, given by the left-hand side of Eq. (2.18), is proportional to the integral of the applied inductor voltage over the interval. In steady state, the initial and final values of the inductor current are equal, and hence the left-hand side of Eq. (2.18) is zero. Therefore, in steady state the integral of the applied inductor voltage must be zero:

$$0 = \int_0^{T_s} v_L(t) dt \quad (2.19)$$

The right-hand side of Eq. (2.19) has the units of volt-seconds or flux-linkages. Equation (2.19) states that the total area, or net volt-seconds, under the $v_L(t)$ waveform must be zero.

An equivalent form is obtained by dividing both sides of Eq. (2.19) by the switching period T_s :

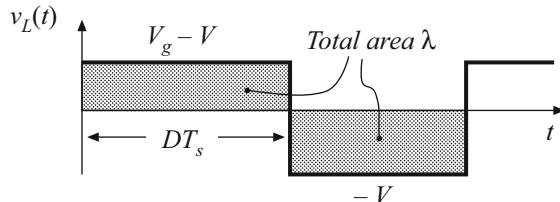
$$0 = \frac{1}{T_s} \int_0^{T_s} v_L(t) dt = \langle v_L \rangle \quad (2.20)$$

The right-hand side of Eq. (2.20) is recognized as the average value, or dc component, of $v_L(t)$. Equation (2.20) states that, in equilibrium, the applied inductor voltage must have zero dc component.

The inductor voltage waveform of Fig. 2.9 is reproduced in Fig. 2.12, with the area under the $v_L(t)$ curve specifically identified. The total area λ is given by the areas of the two rectangles, or

$$\lambda = \int_0^{T_s} v_L(t) dt = (V_g - V)(DT_s) + (-V)(D'T_s) \quad (2.21)$$

Fig. 2.12 The principle of inductor volt-second balance: in steady state, the net volt-seconds applied to an inductor (*i.e.*, the total area λ) must be zero



The average value is therefore

$$\langle v_L \rangle = \frac{\lambda}{T_s} = D(V_g - V) + D'(-V) \quad (2.22)$$

By equating $\langle v_L \rangle$ to zero, and noting that $D + D' = 1$, one obtains

$$0 = DV_g - (D + D')V = DV_g - V \quad (2.23)$$

Solution for V yields

$$V = DV_g \quad (2.24)$$

which coincides with the result obtained previously, Eq. (2.3). So the principle of inductor volt-second balance allows us to derive an expression for the dc component of the converter output voltage. An advantage of this approach is its generality—it can be applied to any converter. One simply sketches the applied inductor voltage waveform, and equates the average value to zero. This method is used later in this chapter, to solve several more complicated converters.

Similar arguments can be applied to capacitors. The defining equation of a capacitor is

$$i_C(t) = C \frac{dv_C(t)}{dt} \quad (2.25)$$

Integration of this equation over one switching period yields

$$v_C(T_s) - v_C(0) = \frac{1}{C} \int_0^{T_s} i_C(t) dt \quad (2.26)$$

In steady state, the net change over one switching period of the capacitor voltage must be zero, so that the left-hand side of Eq. (2.26) is equal to zero. Therefore, in equilibrium the integral of the capacitor current over one switching period (having the dimensions of amp-seconds, or charge) should be zero. There is no net change in capacitor charge in steady state. An equivalent statement is

$$0 = \frac{1}{T_s} \int_0^{T_s} i_C(t) dt = \langle i_C \rangle \quad (2.27)$$

The average value, or dc component, of the capacitor current must be zero in equilibrium.

This should be an intuitive result. If a dc current is applied to a capacitor, then the capacitor will charge continually and its voltage will increase without bound. Likewise, if a dc voltage is applied to an inductor, then the flux will increase continually and the inductor current will increase without bound. Equation (2.27), called the principle of *capacitor amp-second balance* or *capacitor charge balance*, can be used to find the steady-state currents in a switching converter.

2.3 Boost Converter Example

The boost converter, Fig. 2.13a, is another well-known switched-mode converter that is capable of producing a dc output voltage greater in magnitude than the dc input voltage. A practical realization of the switch, using a MOSFET and diode, is shown in Fig. 2.13b. Let us apply the small-ripple approximation and the principles of inductor volt-second balance and capacitor charge balance to find the steady-state output voltage and inductor current for this converter.

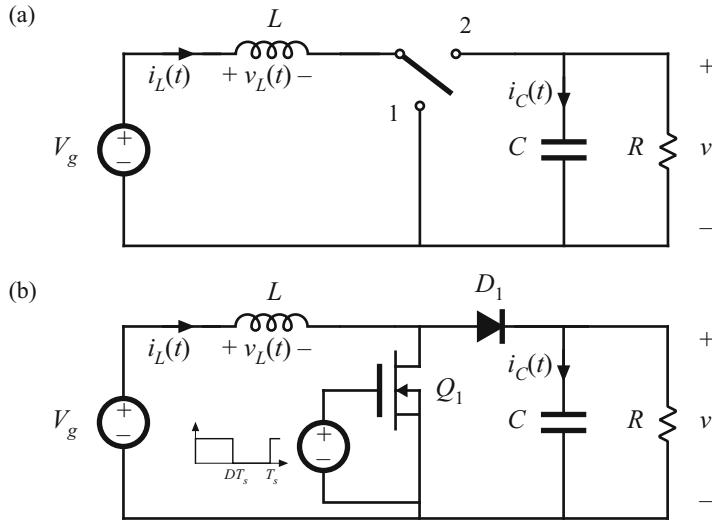


Fig. 2.13 Boost converter: (a) with ideal switch, (b) practical realization using MOSFET and diode

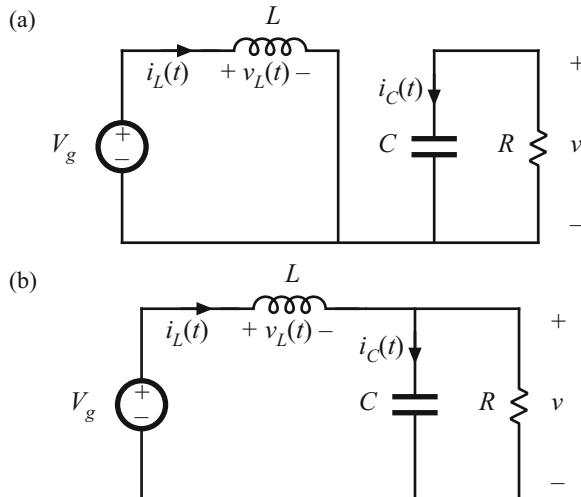


Fig. 2.14 Boost converter circuit, (a) while the switch is in position 1, (b) while the switch is in position 2

With the switch in position 1, the right-hand side of the inductor is connected to ground, resulting in the network of Fig. 2.14a. The inductor voltage and capacitor current for this subinterval are given by

$$\begin{aligned} v_L &= V_g \\ i_C &= -\frac{v}{R} \end{aligned} \tag{2.28}$$

Use of the linear-ripple approximation, $v \approx V$, leads to

$$\begin{aligned} v_L &= V \\ i_C &= -\frac{V}{R} \end{aligned} \quad (2.29)$$

With the switch in position 2, the inductor is connected to the output, leading to the circuit of Fig. 2.14b. The inductor voltage and capacitor current are then

$$\begin{aligned} v_L &= V_g - v \\ i_C &= i_L - \frac{v}{R} \end{aligned} \quad (2.30)$$

Use of the small-ripple approximation, $v \approx V$ and $i_L \approx I$, leads to

$$\begin{aligned} v_L &= V_g - V \\ i_C &= I - \frac{V}{R} \end{aligned} \quad (2.31)$$

Equations (2.29) and (2.31) are used to sketch the inductor voltage and capacitor current waveforms of Fig. 2.15.

It can be inferred from the inductor voltage waveform of Fig. 2.15a that the dc output voltage V is greater than the input voltage V_g . During the first subinterval, $v_L(t)$ is equal to the dc input voltage V_g , and positive volt-seconds are applied to the inductor. Since, in steady-state, the total volt-seconds applied over one switching period must be zero, negative volt-seconds must be applied during the second subinterval. Therefore, the inductor voltage during the second subinterval, $(V_g - V)$, must be negative. Hence, V is greater than V_g .

The total volt-seconds applied to the inductor over one switching period are

$$\int_0^{T_s} v_L(t) dt = (V_g)DT_s + (V_g - V)D'T_s \quad (2.32)$$

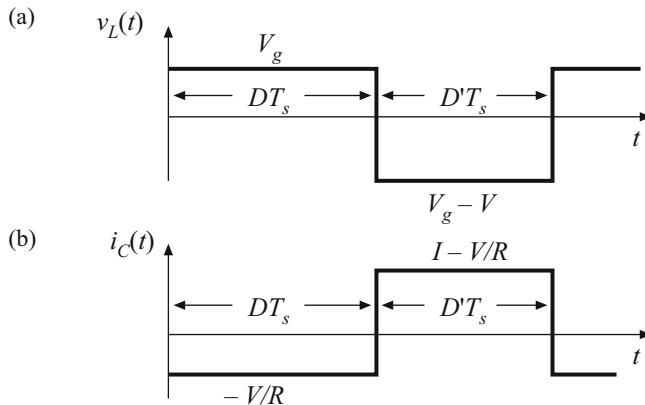


Fig. 2.15 Boost converter voltage and current waveforms

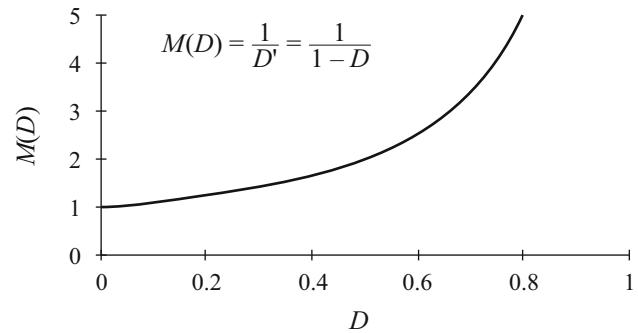


Fig. 2.16 Dc conversion ratio $M(D)$ of the boost converter

By equating this expression to zero and collecting terms, one obtains

$$V_g(D + D') - VD' = 0 \quad (2.33)$$

Solution for V , and by noting that $(D + D') = 1$, yields the expression for the output voltage,

$$V = \frac{V_g}{D'} \quad (2.34)$$

The voltage conversion ratio $M(D)$ is the ratio of the output to the input voltage of a dc-dc converter. Equation (2.34) predicts that the voltage conversion ratio is given by

$$M(D) = \frac{V}{V_g} = \frac{1}{D'} = \frac{1}{1-D} \quad (2.35)$$

This equation is plotted in Fig. 2.16. At $D = 0$, $V = V_g$. The output voltage increases as D increases, and in the ideal case tends to infinity as D tends to 1. So the ideal boost converter is capable of producing any output voltage greater than the input voltage. There are, of course, limits to the output voltage that can be produced by a practical boost converter. In the next chapter, component nonidealities are modeled, and it is found that the maximum output voltage of a practical boost converter is indeed limited. Nonetheless, very large output voltages can be produced if the nonidealities are sufficiently small.

The dc component of the inductor current is derived by use of the principle of capacitor charge balance. During the first subinterval, the capacitor supplies the load current, and the capacitor is partially discharged. During the second subinterval, the inductor current supplies the load and, additionally, recharges the capacitor. The net change in capacitor charge over one switching period is found by integrating the $i_C(t)$ waveform of Fig. 2.15b,

$$\int_0^{T_s} i_C(t) dt = \left(-\frac{V}{R} \right) DT_s + \left(I - \frac{V}{R} \right) D'T_s \quad (2.36)$$

Collecting terms, and equating the result to zero, leads to the steady-state result

$$-\frac{V}{R}(D + D') + ID' = 0 \quad (2.37)$$

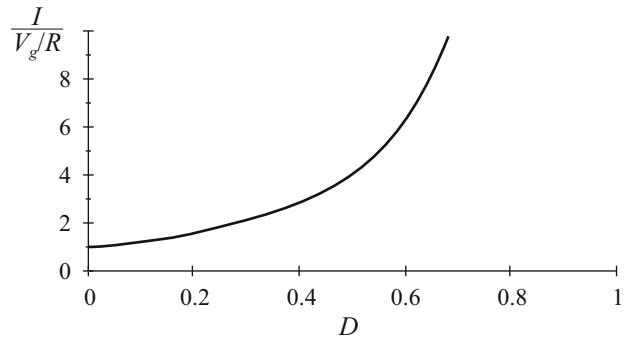


Fig. 2.17 Variation of inductor current dc component I with duty cycle D , boost converter

By noting that $(D+D') = 1$, and by solving for the inductor current dc component I , one obtains

$$I = \frac{V}{D'R} \quad (2.38)$$

So the inductor current dc component I is equal to the load current, V/R , divided by D' . Substitution of Eq. (2.34) to eliminate V yields

$$I = \frac{V_g}{D'^2 R} \quad (2.39)$$

This equation is plotted in Fig. 2.17. It can be seen that the inductor current becomes large as D approaches 1.

This inductor current, which coincides with the dc input current in the boost converter, is greater than the load current. Physically, this must be the case: to the extent that the converter elements are ideal, the converter input and output powers are equal. Since the converter output voltage is greater than the input voltage, the input current must likewise be greater than the output current. In practice, the inductor current flows through the semiconductor forward voltage drops, the inductor winding resistance, and other sources of power loss. As the duty cycle approaches one, the inductor current becomes very large and these component nonidealities lead to large power losses. In consequence, the efficiency of the boost converter decreases rapidly at high duty cycle.

Next, let us sketch the inductor current $i_L(t)$ waveform and derive an expression for the inductor current ripple Δi_L . The inductor voltage waveform $v_L(t)$ has been already found (Fig. 2.15), so we can sketch the inductor current waveform directly. During the first subinterval, with the switch in position 1, the slope of the inductor current is given by

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g}{L} \quad (2.40)$$

Likewise, when the switch is in position 2, the slope of the inductor current waveform is

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g - V}{L} \quad (2.41)$$

The inductor current waveform is sketched in Fig. 2.18. During the first subinterval, the change in inductor current, $2\Delta i_L$, is equal to the slope multiplied by the length of the subinterval, or

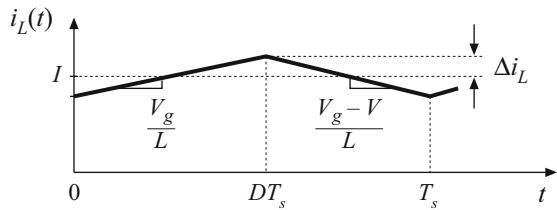


Fig. 2.18 Boost converter inductor current waveform $i_L(t)$

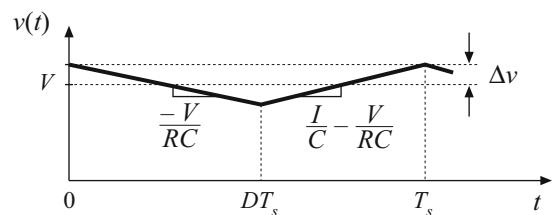


Fig. 2.19 Boost converter output voltage waveform $v(t)$

$$2\Delta i_L = \frac{V_g}{L}DT_s \quad (2.42)$$

Solution for Δi_L leads to

$$\Delta i_L = \frac{V_g}{2L}DT_s \quad (2.43)$$

This expression can be used to select the inductor value L such that a given value of Δi_L is obtained.

Likewise, the capacitor voltage $v(t)$ waveform can be sketched, and an expression derived for the output voltage ripple peak magnitude Δv . The capacitor current waveform $i_C(t)$ is given in Fig. 2.15. During the first subinterval, the slope of the capacitor voltage waveform $v(t)$ is

$$\frac{dv_C(t)}{dt} = \frac{i_C(t)}{C} = \frac{-V}{RC} \quad (2.44)$$

During the second subinterval, the slope is

$$\frac{dv_C(t)}{dt} = \frac{i_C(t)}{C} = \frac{I}{C} - \frac{V}{RC} \quad (2.45)$$

The capacitor voltage waveform is sketched in Fig. 2.19. During the first subinterval, the change in capacitor voltage, $-2\Delta v$, is equal to the slope multiplied by the length of the subinterval:

$$-2\Delta v = \frac{-V}{RC}DT_s \quad (2.46)$$

Solution for Δv yields

$$\Delta v = \frac{V}{2RC}DT_s \quad (2.47)$$

This expression can be used to select the capacitor value C to obtain a given output voltage ripple peak magnitude Δv .

2.4 Ćuk Converter Example

As a second example, consider the Ćuk converter of Fig. 2.20a. This converter performs a dc conversion function similar to the buck–boost converter: it can either increase or decrease the magnitude of the dc voltage, and it inverts the polarity. A practical realization using a transistor and diode is illustrated in Fig. 2.20b.

This converter operates via capacitive energy transfer. As illustrated in Fig. 2.21, capacitor C_1 is connected through L_1 to the input source while the switch is in position 2, and source energy is stored in C_1 . When the switch is in position 1, this energy is released through L_2 to the load.

The inductor currents and capacitor voltages are defined, with polarities assigned somewhat arbitrarily, in Fig. 2.20a. In this section, the principles of inductor volt-second balance and capacitor charge balance are applied to find the dc components of the inductor currents and capacitor voltages. The voltage and current ripple magnitudes are also found.

During the first subinterval, while the switch is in position 1, the converter circuit reduces to Fig. 2.21a. The inductor voltages and capacitor currents are

$$\begin{aligned} v_{L1} &= V_g \\ v_{L2} &= -v_1 - v_2 \\ i_{C1} &= i_2 \\ i_{C2} &= i_2 - \frac{v_2}{R} \end{aligned} \quad (2.48)$$

We next assume that the switching ripple magnitudes in $i_1(t)$, $i_2(t)$, $v_1(t)$, and $v_2(t)$ are small compared to their respective dc components I_1 , I_2 , V_1 , and V_2 . We can therefore make the small-ripple approximation, and Eq. (2.48) becomes

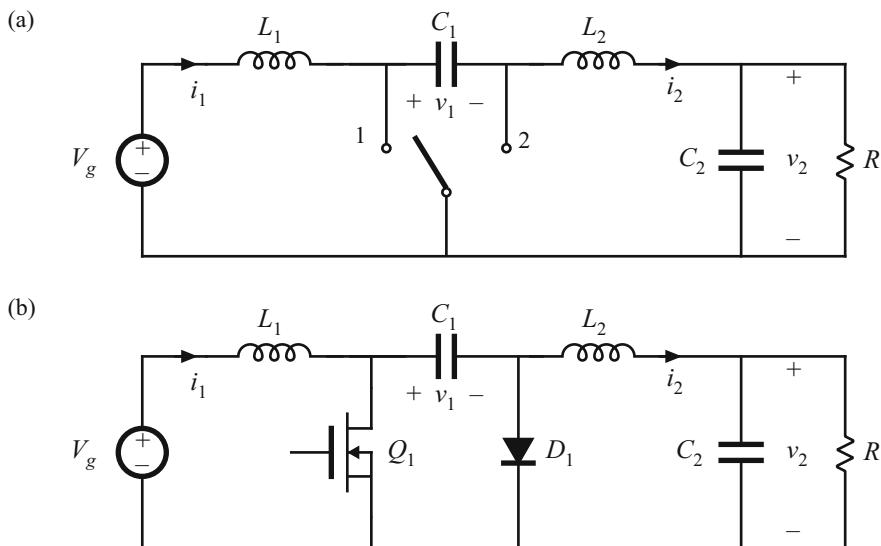


Fig. 2.20 Ćuk converter: (a) with ideal switch, (b) practical realization using MOSFET and diode

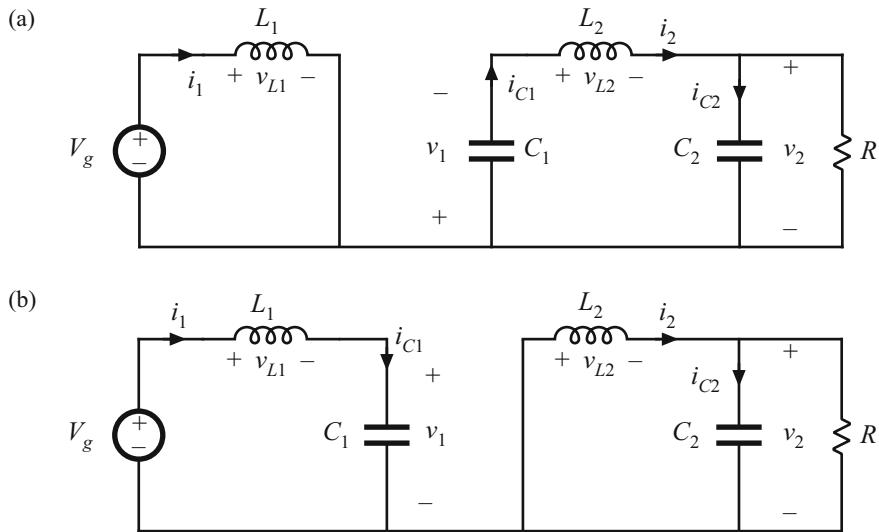


Fig. 2.21 Ćuk converter circuit: (a) while switch is in position 1, (b) while switch is in position 2

$$\begin{aligned}
 v_{L1} &= V_g \\
 v_{L2} &= -V_1 - V_2 \\
 i_{C1} &= I_2 \\
 i_{C2} &= I_2 - \frac{V_2}{R}
 \end{aligned} \tag{2.49}$$

During the second subinterval, with the switch in position 2, the converter circuit elements are connected as in Fig. 2.21b. The inductor voltages and capacitor currents are:

$$\begin{aligned}
 v_{L1} &= V_g - v_1 \\
 v_{L2} &= -v_2 \\
 i_{C1} &= i_1 \\
 i_{C2} &= i_2 - \frac{V_2}{R}
 \end{aligned} \tag{2.50}$$

We again make the small-ripple approximation, and hence Eq. (2.50) becomes

$$\begin{aligned}
 v_{L1} &= V_g - V_1 \\
 v_{L2} &= -V_2 \\
 i_{C1} &= I_1 \\
 i_{C2} &= I_2 - \frac{V_2}{R}
 \end{aligned} \tag{2.51}$$

Equations (2.49) and (2.51) are used to sketch the inductor voltage and capacitor current waveforms in Fig. 2.22.

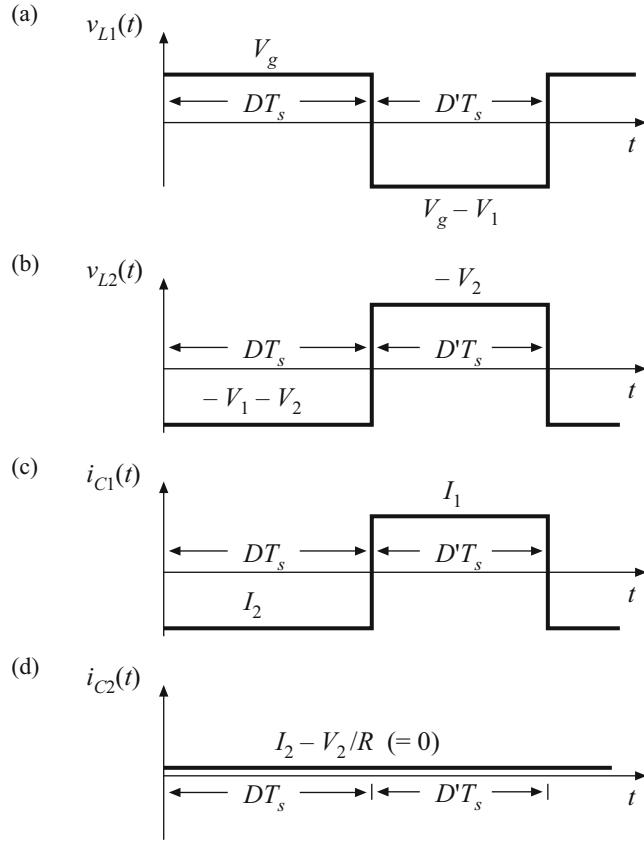


Fig. 2.22 Cuk converter waveforms: (a) inductor voltage $v_{L1}(t)$, (b) inductor voltage $v_{L2}(t)$, (c) capacitor current $i_{C1}(t)$, (d) capacitor current $i_{C2}(t)$

The next step is to equate the dc components, or average values, of the waveforms of Fig. 2.22 to zero, to find the steady-state conditions in the converter. The results are

$$\begin{aligned}\langle v_{L1} \rangle &= DV_g + D' (V_g - V_1) = 0 \\ \langle v_{L2} \rangle &= D (-V_1 - V_2) + D' (-V_2) = 0 \\ \langle i_{C1} \rangle &= DI_2 + D'I_1 = 0 \\ \langle i_{C2} \rangle &= I_2 - \frac{V_2}{R} = 0\end{aligned}\tag{2.52}$$

Solution of this system of equations for the dc components of the capacitor voltages and inductor currents leads to

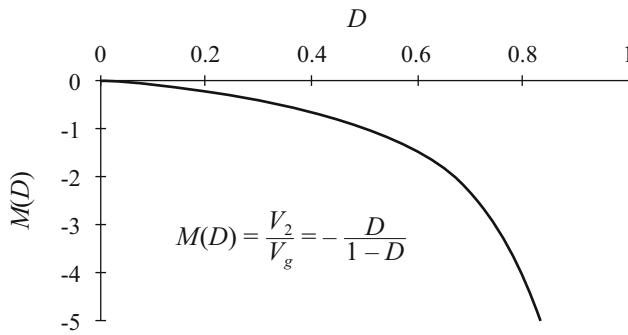


Fig. 2.23 Dc conversion ratio $M(D) = -V/V_g$ of the Ćuk converter

$$\begin{aligned}
 V_1 &= \frac{V_g}{D'} \\
 V_2 &= -\frac{D}{D'} V_g \\
 I_1 &= -\frac{D}{D'} I_2 = \left(\frac{D}{D'}\right)^2 \frac{V_g}{R} \\
 I_2 &= \frac{V_2}{R} = -\frac{D}{D'} \frac{V_g}{R}
 \end{aligned} \tag{2.53}$$

The dependence of the dc output voltage V_2 on the duty cycle D is sketched in Fig. 2.23.

The inductor current waveforms are sketched in Fig. 2.24a,b, and the capacitor C_1 voltage waveform $v_1(t)$ is sketched in Fig. 2.24c. During the first subinterval, the slopes of the waveforms are given by

$$\begin{aligned}
 \frac{di_1(t)}{dt} &= \frac{v_{L1}(t)}{L_1} = \frac{V_g}{L_1} \\
 \frac{di_2(t)}{dt} &= \frac{v_{L2}(t)}{L_2} = \frac{-V_1 - V_2}{L_2} \\
 \frac{dv_1(t)}{dt} &= \frac{i_{C1}(t)}{C_1} = \frac{I_2}{C_1}
 \end{aligned} \tag{2.54}$$

Equation (2.49) has been used here to substitute for the values of v_{L1} , v_{L2} , and i_{C1} during the first subinterval. During the second interval, the slopes of the waveforms are given by

$$\begin{aligned}
 \frac{di_1(t)}{dt} &= \frac{v_{L1}(t)}{L_1} = \frac{V_g - V_1}{L_1} \\
 \frac{di_2(t)}{dt} &= \frac{v_{L2}(t)}{L_2} = \frac{-V_2}{L_2} \\
 \frac{dv_1(t)}{dt} &= \frac{i_{C1}(t)}{C_1} = \frac{I_1}{C_1}
 \end{aligned} \tag{2.55}$$

Equation (2.51) was used to substitute for the values of v_{L1} , v_{L2} , and i_{C1} during the second subinterval.

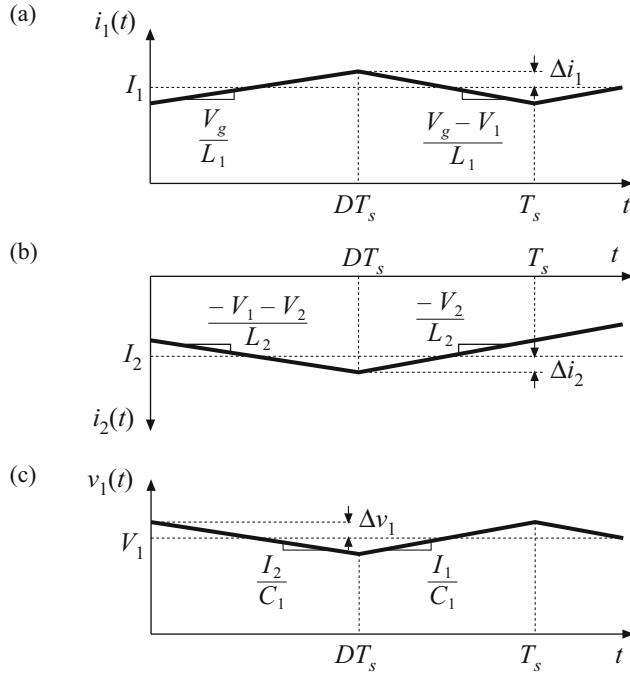


Fig. 2.24 Cuk converter waveforms: (a) inductor current $i_1(t)$, (b) inductor current $i_2(t)$, (c) capacitor voltage $v_1(t)$

During the first subinterval, the quantities $i_1(t)$, $i_2(t)$, and $v_1(t)$ change by $2\Delta i_1$, $-2\Delta i_2$, and $-2\Delta v_1$, respectively. These changes are equal to the slopes given in Eq. (2.54), multiplied by the subinterval length DT_s , yielding

$$\begin{aligned}\Delta i_1 &= \frac{V_g DT_s}{2L_1} \\ \Delta i_2 &= \frac{V_1 + V_2}{2L_2} DT_s \\ \Delta v_1 &= \frac{-I_2 DT_s}{2C_1}\end{aligned}\quad (2.56)$$

The dc relationships, Eq. (2.53), can now be used to simplify these expressions and eliminate V_1 , V_2 , and I_1 , leading to

$$\begin{aligned}\Delta i_1 &= \frac{V_g DT_s}{2L_1} \\ \Delta i_2 &= \frac{V_g DT_s}{2L_2} \\ \Delta v_1 &= \frac{V_g D^2 T_s}{2D'RC_1}\end{aligned}\quad (2.57)$$

These expressions can be used to select values of L_1 , L_2 , and C_1 , such that desired values of switching ripple magnitudes are obtained.

Similar arguments cannot be used to estimate the switching ripple magnitude in the output capacitor voltage $v_2(t)$. According to Fig. 2.22d, the current $i_{C2}(t)$ is continuous: unlike v_{L1} , v_{L2} , and i_{C1} , the capacitor current $i_{C2}(t)$ is nonpulsating. If the switching ripple of $i_2(t)$ is neglected, then the capacitor current $i_{C2}(t)$ does not contain an ac component. The small-ripple approximation then leads to the conclusion that the output switching ripple Δv is zero.

Of course, the output voltage switching ripple is not zero. To estimate the magnitude of the output voltage ripple in this converter, we must not neglect the switching ripple present in the inductor current $i_2(t)$, since this current ripple is the only source of ac current driving the output capacitor C_2 . A simple way of doing this in the Ćuk converter and in other similar converters is discussed in the next section.

2.5 Estimating the Output Voltage Ripple in Converters Containing Two-Pole Low-Pass Filters

A case where the small-ripple approximation is not useful is in converters containing two-pole low-pass filters, such as in the output of the Ćuk converter (Fig. 2.20) or the buck converter (Fig. 2.25). For these converters, the small-ripple approximation predicts zero output voltage ripple, regardless of the value of the output filter capacitance. The problem is that the only component of output capacitor current in these cases is that arising from the inductor current ripple. Hence, inductor current ripple cannot be neglected when calculating the output capacitor voltage ripple, and a more accurate approximation is needed.

An improved approach that is useful for this case is to estimate the capacitor current waveform $i_C(t)$ more accurately, accounting for the inductor current ripple. The capacitor voltage ripple can then be related to the total charge contained in the positive portion of the $i_C(t)$ waveform.

Consider the buck converter of Fig. 2.25. The inductor current waveform $i_L(t)$ contains a dc component I and linear ripple of peak magnitude Δi_L , as shown in Fig. 2.10. The dc component I must flow entirely through the load resistance R (why?), while the ac switching ripple divides between the load resistance R and the filter capacitor C . In a well-designed converter, in which the capacitor provides significant filtering of the switching ripple, the capacitance C is chosen large enough that its impedance at the switching frequency is much smaller than the load impedance R . Hence nearly all of the inductor current ripple flows through the capacitor, and

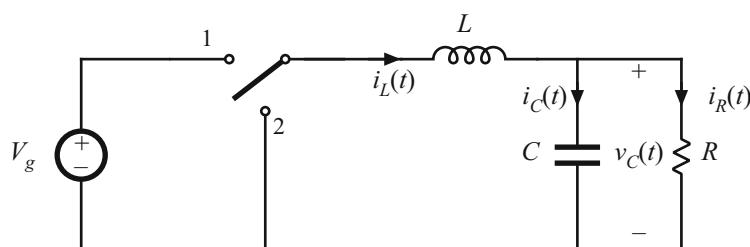


Fig. 2.25 The buck converter contains a two-pole output filter

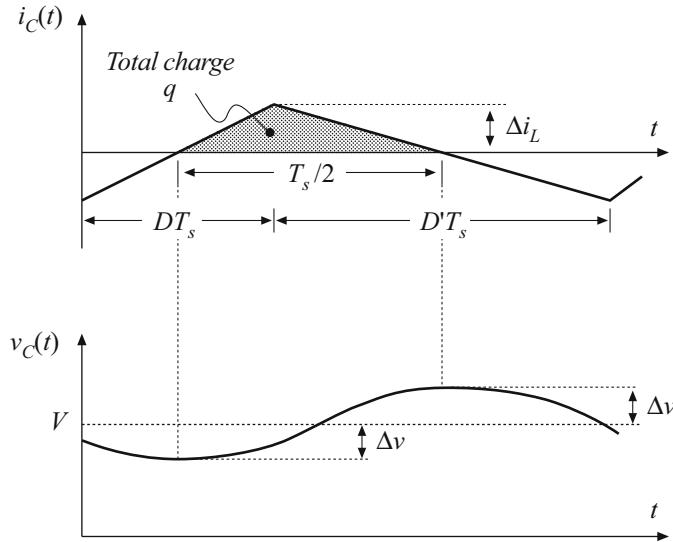


Fig. 2.26 Output capacitor voltage and current waveforms, for the buck converter in Fig. 2.25

very little flows through the load. As shown in Fig. 2.26, the capacitor current waveform $i_C(t)$ is then equal to the inductor current waveform with the dc component removed. The current ripple is linear, with peak value Δi_L .

When the capacitor current $i_C(t)$ is positive, charge is deposited on the capacitor plates and the capacitor voltage $v_C(t)$ increases. Therefore, between the two zero crossings of the capacitor current waveform, the capacitor voltage changes between its minimum and maximum extrema. The waveform is symmetrical, and the total change in v_C is the peak-to-peak output voltage ripple, or $2\Delta v$.

This change in capacitor voltage can be related to the total charge q contained in the positive portion of the capacitor current waveform. By the capacitor relation $Q = CV$,

$$q = C(2\Delta v) \quad (2.58)$$

As illustrated in Fig. 2.26, the charge q is the integral of the current waveform between its zero crossings. For this example, the integral can be expressed as the area of the shaded triangle, having a height Δi_L . Owing to the symmetry of the current waveform, the zero crossings occur at the centerpoints of the DT_s and $D'T_s$ subintervals. Hence, the base dimension of the triangle is $T_s/2$. So the total charge q is given by

$$q = \frac{1}{2}\Delta i_L \frac{T_s}{2} \quad (2.59)$$

Substitution of Eq. (2.58) into Eq. (2.59), and solution for the voltage ripple peak magnitude Δv yields

$$\Delta v = \frac{\Delta i_L T_s}{8C} \quad (2.60)$$

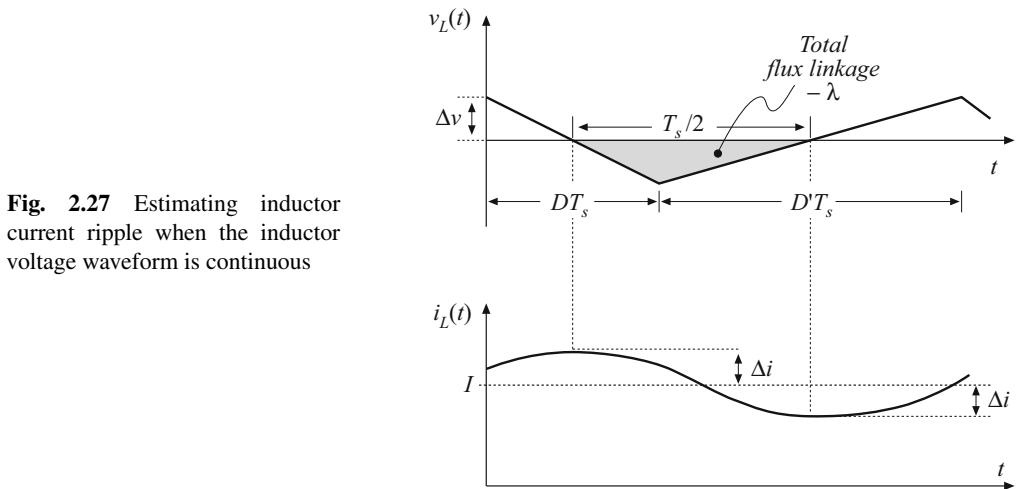


Fig. 2.27 Estimating inductor current ripple when the inductor voltage waveform is continuous

This expression can be used to select a value for the capacitance C such that a given voltage ripple Δv is obtained. In practice, the additional voltage ripple caused by the capacitor equivalent series resistance (ESR) must also be included.

Similar arguments can be applied to inductors. An example is considered in Problem 2.10, in which a two-pole input filter is added to a buck converter as in Fig. 2.33. The capacitor voltage ripple cannot be neglected; doing so would lead to the conclusion that no ac voltage is applied across the input filter inductor, resulting in zero input current ripple. The actual inductor voltage waveform is identical to the ac portion of the input filter capacitor voltage, with linear ripple and with peak value Δv as illustrated in Fig. 2.27. By use of the inductor relation $\lambda = Li$, a result similar to Eq. (2.60) can be derived. The derivation is left as a problem for the student.

2.6 Summary of Key Points

1. The dc component of a converter waveform is given by its average value, or the integral over one switching period, divided by the switching period. Solution of a dc-dc converter to find its dc, or steady state, voltages and currents therefore involves averaging the waveforms.
2. The linear- (or small-) ripple approximation greatly simplifies the analysis. In a well-designed converter, the switching ripples in the inductor currents and capacitor voltages are small compared to the respective dc components, and can be neglected.
3. The small-ripple approximation is properly applied only to inductor currents and capacitor voltages, which are continuous waveforms. Attempts to apply the small-ripple approximation to switched (discontinuous) waveforms lead to erroneous results.
4. The principle of inductor volt-second balance allows determination of the dc voltage components in any switching converter. In steady state, the average voltage applied to an inductor must be zero.
5. The principle of capacitor charge balance allows determination of the dc components of the inductor currents in a switching converter. In steady state, the average current applied to a capacitor must be zero.

6. By knowledge of the slopes of the inductor current and capacitor voltage waveforms, the ac switching ripple magnitudes may be computed. Inductance and capacitance values can then be chosen to obtain desired ripple magnitudes.
7. In converters containing multiple-pole filters, continuous (nonpulsating) voltages and currents are applied to one or more of the inductors or capacitors. Computation of the ac switching ripple in these elements can be done using capacitor charge and/or inductor flux-linkage arguments, without use of the small-ripple approximation.
8. Converters capable of increasing (boost), decreasing (buck), and inverting the voltage polarity (buck-boost and Ćuk) have been described. Converter circuits are explored more fully in the problems and in a later chapter.

PROBLEMS

- 2.1** Analysis and design of a buck-boost converter: A buck-boost converter is illustrated in Fig. 2.28a, and a practical implementation using a transistor and diode is shown in Fig. 2.28b.

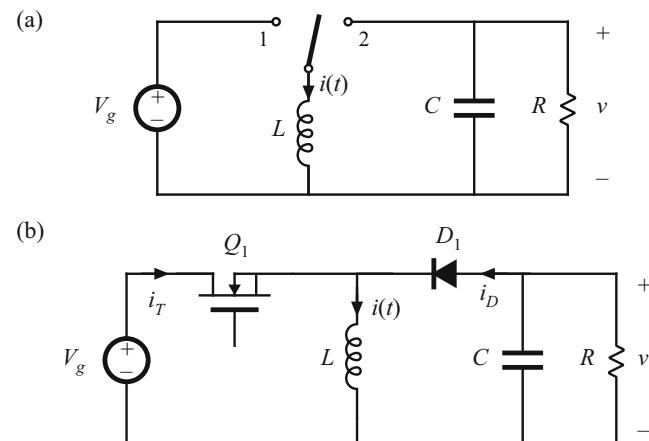


Fig. 2.28 Buck-boost converter of Problem 2.1: (a) ideal converter circuit, (b) implementation using MOSFET and diode

- (a) Find the dependence of the equilibrium output voltage V and inductor current I on the duty ratio D , input voltage V_g , and load resistance R . You may assume that the inductor current ripple and capacitor voltage ripple are small.
- (b) Plot your results of part (a) over the range $0 \leq D \leq 1$.
- (c) Dc design: for the specifications

$$\begin{aligned} V_g &= 30 \text{ V} & V &= -20 \text{ V} \\ R &= 4\Omega & f_s &= 40 \text{ kHz} \end{aligned}$$

- (i) Find D and I
- (ii) Calculate the value of L that will make the peak inductor current ripple Δi equal to ten percent of the average inductor current I .
- (iii) Choose C such that the peak output voltage ripple Δv is 0.1 V.

- (d) Sketch the transistor drain current waveform $i_T(t)$ for your design of part (c). Include the effects of inductor current ripple. What is the peak value of i_T ? Also sketch $i_T(t)$ for the case when L is decreased such that Δi is 50% of I . What happens to the peak value of i_T in this case?
- (e) Sketch the diode current waveform $i_D(t)$ for the two cases of part (d).
- 2.2** The boost converter illustrated in Fig. 2.29 operates with the following conditions:

Input voltage	$V_g = 3.3 \text{ V}$
Output voltage	$V = 5 \text{ V}$
Switching frequency f_s	$= 500 \text{ kHz}$

All elements are ideal, and the converter operates in steady state with waveforms similar to those illustrated in Fig. 2.15.

- (a) What is the duty cycle?

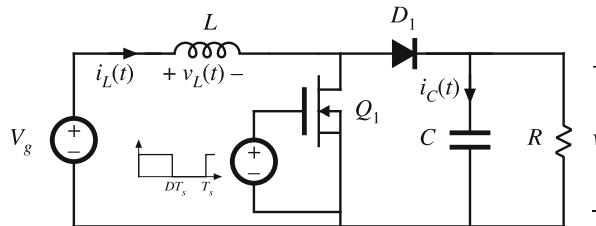


Fig. 2.29 Boost converter of Problem 2.2

- (b) Sketch the waveform of the MOSFET drain-to-source voltage. Label the numerical values of all relevant times and voltages.
- (c) Find the dc component of the voltage waveform of Part (b).
- 2.3** In a certain application, an unregulated dc input voltage can vary between 18 and 36 V. It is desired to produce a regulated output of 28 V to supply a 2 A load. Hence, a converter is needed that is capable of both increasing and decreasing the voltage. Since the input and output voltages are both positive, converters that invert the voltage polarity (such as the basic buck-boost converter) are not suited for this application.
- One converter that is capable of performing the required function is the nonisolated SEPIC (single-ended primary inductance converter) shown in Fig. 2.30. This converter has a con-

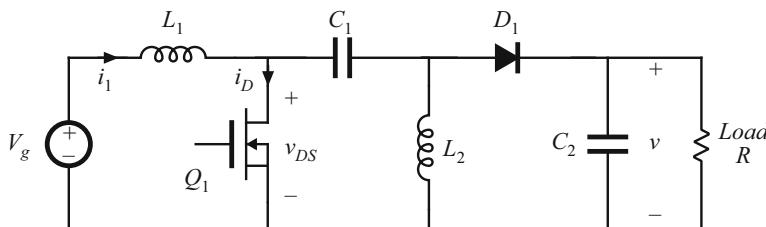


Fig. 2.30 SEPIC of Problems 2.3 and 2.4

version ratio $M(D)$ that can both buck and boost the voltage, but the voltage polarity is not inverted. In the normal converter operating mode, the transistor conducts during the first subinterval ($0 < t < DT_s$), and the diode conducts during the second subinterval ($DT_s < t < T_s$). You may assume that all elements are ideal.

- (a) Derive expressions for the dc components of each capacitor voltage and inductor current, as functions of the duty cycle D , the input voltage V_g , and the load resistance R .
- (b) A control circuit automatically adjusts the converter duty cycle D , to maintain a constant output voltage of $V = 28$ V. The input voltage slowly varies over the range $18 \text{ V} \leq V_g \leq 36 \text{ V}$. The load current is constant and equal to 2 A. Over what range will the duty cycle D vary? Over what range will the input inductor current dc component I_1 vary?

2.4 For the SEPIC of Problem 2.3,

- (a) Derive expressions for each inductor current ripple and capacitor voltage ripple. Express these quantities as functions of the switching period T_s ; the component values L_1, L_2, C_1, C_2 ; the duty cycle D ; the input voltage V_g ; and the load resistance R .
- (b) Sketch the waveforms of the transistor voltage $v_{DS}(t)$ and transistor current $i_D(t)$, and give expressions for their peak values.

2.5 The switches in the converter of Fig. 2.31 operate synchronously: each is in position 1 for $0 < t < DT_s$, and in position 2 for $DT_s < t < T_s$. Derive an expression for the voltage conversion ratio $M(D) = V/V_g$. Sketch $M(D)$ vs. D .

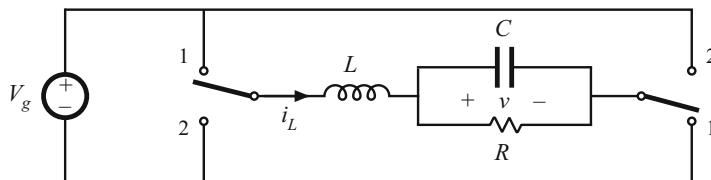


Fig. 2.31 H-bridge converter of Problems 2.5 and 2.7

2.6 The switches in the converter of Fig. 2.32 operate synchronously: each is in position 1 for $0 < t < DT_s$, and in position 2 for $DT_s < t < T_s$. Derive an expression for the voltage conversion ratio $M(D) = V/V_g$. Sketch $M(D)$ vs. D .

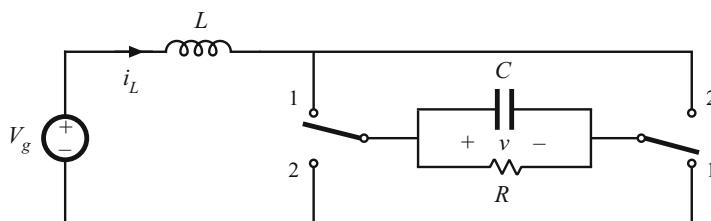


Fig. 2.32 Current-fed bridge converter of Problems 2.6, 2.8, and 2.9

- 2.7** For the converter of Fig. 2.31, derive expressions for the inductor current ripple Δi_L and the capacitor voltage ripple Δv_C .
- 2.8** For the converter of Fig. 2.32, derive an analytical expression for the dc component of the inductor current, I , as a function of D , V_g , and R . Sketch your result vs. D .
- 2.9** For the converter of Fig. 2.32, derive expressions for the inductor current ripple Δi_L and the capacitor voltage ripple Δv_C .
- 2.10** To reduce the switching harmonics present in the input current of a certain buck converter, an input filter consisting of inductor L_1 and capacitor C_1 is added as shown in Fig. 2.33. Such filters are commonly used to meet regulations limiting conducted electromagnetic interference (EMI). For this problem, you may assume that all inductance and capacitance values are sufficiently large, such that all ripple magnitudes are small.

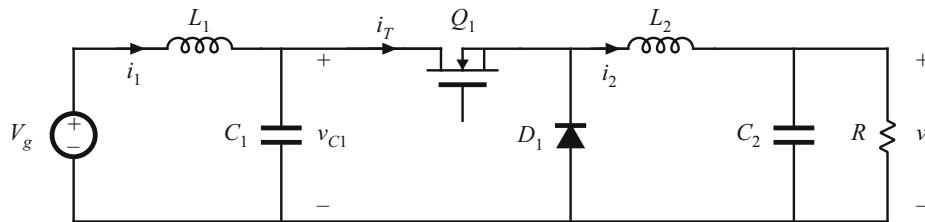


Fig. 2.33 Addition of $L-C$ input filter to buck converter, Problem 2.10

- (a) Sketch the transistor current waveform $i_T(t)$.
- (b) Derive analytical expressions for the dc components of the capacitor voltages and inductor currents.
- (c) Derive analytical expressions for the peak ripple magnitudes of the input filter inductor current and capacitor voltage.
- (d) Given the following values:

Input voltage	$V_g = 48 \text{ V}$
Output voltage	$V = 36 \text{ V}$
Switching frequency f_s	100 kHz
Load resistance	$R = 6 \Omega$

Select values for L_1 and C_1 such that (i) the peak voltage ripple on C_1 , Δv_{C1} , is two percent of the dc component V_{C1} , and (ii) the input peak current ripple Δi_1 is 20 mA.

- 2.11** An ideal boost converter is shown in Fig. 2.13a. For the converter operating in steady state, derive exact analytical expressions for:
- (a) the dc component of the output voltage,
 (b) the peak-to-peak inductor current ripple, and
 (c) the peak-to-peak capacitor voltage ripple.

Your expressions should be written in terms of the circuit parameters V_g , R , T_s , L , C , and duty cycle D .



Steady-State Equivalent Circuit Modeling, Losses, and Efficiency

Let us now consider the basic functions performed by a switching converter, and attempt to represent these functions by a simple equivalent circuit. The designer of a converter power stage must calculate the network voltages and currents, and specify the power components accordingly. Losses and efficiency are of prime importance. The use of equivalent circuits is a physical and intuitive approach which allows the well-known techniques of circuit analysis to be employed. As noted in the previous chapter, it is desirable to ignore the small but complicated switching ripple, and model only the important dc components of the waveforms.

The dc transformer is used to model the ideal functions performed by a dc-dc converter [14–17]. This simple model correctly represents the relationships between the dc voltages and currents of the converter. The model can be refined by including losses, such as semiconductor forward voltage drops and on-resistances, inductor core and copper losses, etc. The resulting model can be directly solved, to find the voltages, currents, losses, and efficiency in the actual nonideal converter.

3.1 The DC Transformer Model

As illustrated in Fig. 3.1, any switching converter contains three ports: a power input, a power output, and a control input. The input power is processed as specified by the control input, and then is output to the load. Ideally, these functions are performed with 100% efficiency, and hence

$$P_{in} = P_{out} \quad (3.1)$$

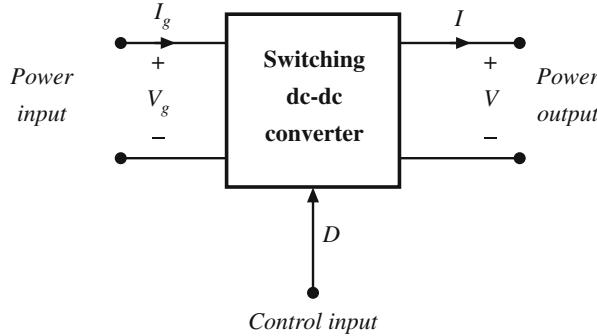
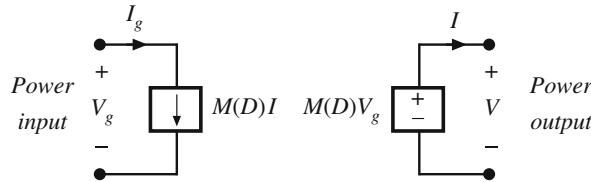
or,

$$V_g I_g = VI \quad (3.2)$$

These relationships are valid only under equilibrium (dc) conditions: during transients, the net stored energy in the converter inductors and capacitors may change, causing Eqs. (3.1) and (3.2) to be violated.

In the previous chapter, we found that we could express the converter output voltage in an equation of the form

$$V = M(D)V_g \quad (3.3)$$

**Fig. 3.1** Switching converter terminal quantities**Fig. 3.2** A switching converter equivalent circuit using dependent sources, corresponding to Eqs. (3.3) and (3.4)

where $M(D)$ is the equilibrium conversion ratio of the converter. For example, $M(D) = D$ for the buck converter, and $M(D) = 1/(1 - D)$ for the boost converter. In general, for ideal PWM converters operating in the continuous conduction mode and containing an equal number of independent inductors and capacitors, it can be shown that the equilibrium conversion ratio M is a function of the duty cycle D and is independent of load.

Substitution of Eq. (3.3) into Eq. (3.2) yields

$$I_g = M(D)I \quad (3.4)$$

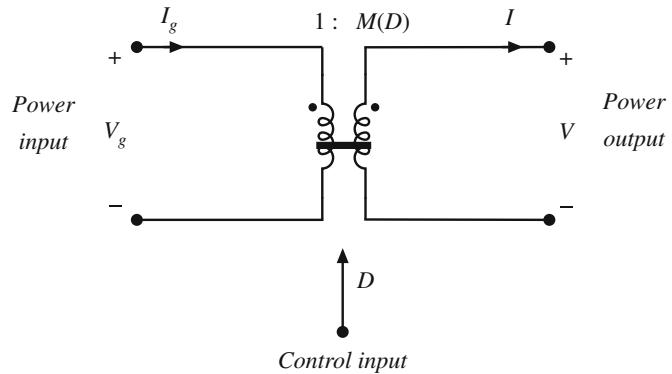
Hence, the converter terminal currents are related by the same conversion ratio.

Equations (3.3) and (3.4) suggest that the converter could be modeled using dependent sources, as in Fig. 3.2. An equivalent but more physically meaningful model (Fig. 3.3) can be obtained through the realization that Eqs. (3.1) to (3.4) coincide with the equations of an ideal transformer. In an ideal transformer, the input and output powers are equal, as stated in Eqs. (3.1) and (3.2). Also, the output voltage is equal to the turns ratio times the input voltage. This is consistent with Eq. (3.3), with the turns ratio taken to be the equilibrium conversion ratio $M(D)$. Finally, the input and output currents should be related by the same turns ratio, as in Eq. (3.4).

Thus, we can model the ideal dc-dc converter using the ideal dc transformer model of Fig. 3.3.

This symbol represents the first-order dc properties of any switching dc-dc converter: transformation of dc voltage and current levels, ideally with 100% efficiency, controllable by the duty cycle D . The solid horizontal line indicates that the element is ideal and capable of passing dc voltages and currents. It should be noted that, although standard magnetic core transformers

Fig. 3.3 Ideal dc transformer model of a dc-dc converter operating in continuous conduction mode, corresponding to Eqs. (3.1) to (3.4)



cannot transform dc signals (they saturate when a dc voltage is applied), we are nonetheless free to define the idealized model of Fig. 3.3 for the purpose of modeling dc-dc converters. Indeed, the absence of a physical dc transformer is one of the reasons for building a dc-dc switching converter. So the properties of the dc-dc converter of Fig. 3.1 can be modeled using the equivalent circuit of Fig. 3.3. An advantage of this equivalent circuit is that, for constant duty cycle, it is time invariant: there is no switching or switching ripple to deal with, and only the important dc components of the waveforms are modeled.

The rules for manipulating and simplifying circuits containing transformers apply equally well to circuits containing dc-dc converters. For example, consider the network of Fig. 3.4a, in which a resistive load is connected to the converter output, and the power source is modeled by a Thevenin-equivalent voltage source V_1 and resistance R_1 . The converter is replaced by the dc transformer model in Fig. 3.3. An advantage of this equivalent circuit is that, for constant duty cycle, it is time invariant: there is no switching or switching ripple to deal with, and only the important dc components of the waveforms are modeled.

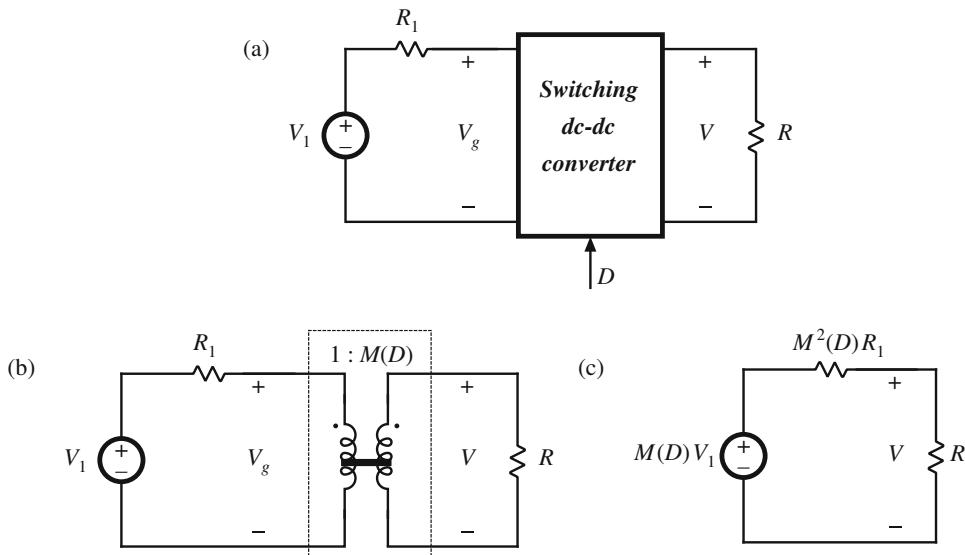


Fig. 3.4 Example of the use of the dc transformer model: (a) original circuit; (b) substitution of switching converter dc transformer model; (c) simplification by referring all elements to secondary side

transformer as in Fig. 3.4c; the voltage source V_1 is multiplied by the conversion ratio $M(D)$, and the resistor R_1 is multiplied by $M^2(D)$. This circuit can now be solved using the voltage divider formula to find the output voltage:

$$V = M(D)V_1 \frac{R}{R + M^2(D)R_1} \quad (3.5)$$

It should be apparent that the dc transformer/equivalent circuit approach is a powerful tool for understanding networks containing converters.

3.2 Inclusion of Inductor Copper Loss

The dc transformer model of Fig. 3.3 can be extended, to model other properties of the converter. Nonidealities, such as sources of power loss, can be modeled by adding resistors as appropriate. In later chapters, we will see that converter dynamics can be modeled as well, by adding inductors and capacitors to the equivalent circuit.

Let us consider the inductor copper loss in a boost converter.

Practical inductors exhibit power loss of two types: (1) *copper loss*, originating in the resistance of the wire, and (2) *core loss*, due to hysteresis and eddy current losses in the magnetic core. A suitable model that describes the inductor copper loss is given in Fig. 3.5, in which a resistor R_L is placed in series with the inductor. The actual inductor then consists of an ideal inductor, L , in series with the copper loss resistor R_L .



Fig. 3.5 Modeling inductor copper loss via series resistor R_L

The inductor model of Fig. 3.5 is inserted into the boost converter circuit in Fig. 3.6. The circuit can now be analyzed in the same manner as used for the ideal lossless converter, using the principles of inductor volt-second balance, capacitor charge balance, and the small-ripple approximation. First, we draw the converter circuits during the two subintervals, as in Fig. 3.7.

For $0 < t < DT_s$, the switch is in position 1 and the circuit reduces to Fig. 3.7a. The inductor voltage $v_L(t)$, across the ideal inductor L , is given by

$$v_L(t) = V_g - i(t)R_L \quad (3.6)$$

and the capacitor current $i_C(t)$ is

$$i_C(t) = -\frac{v(t)}{R} \quad (3.7)$$

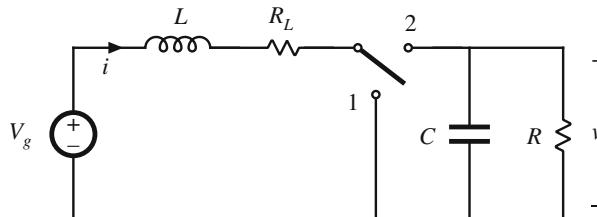


Fig. 3.6 Boost converter circuit, including inductor copper resistance R_L

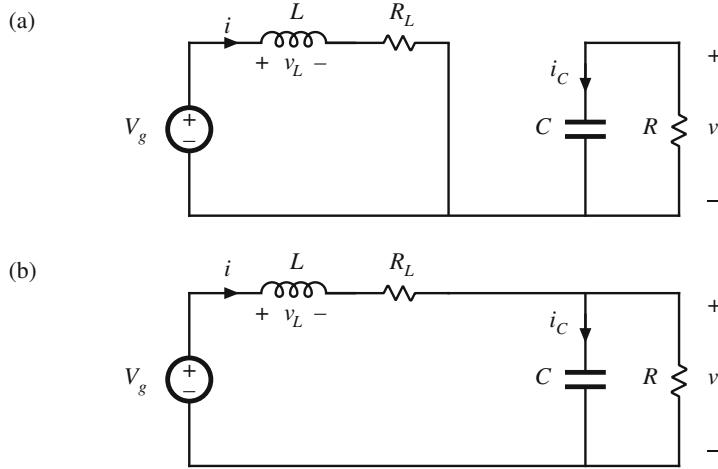


Fig. 3.7 Boost converter circuits during the two subintervals, including inductor copper loss resistance R_L : (a) with the switch in position 1, (b) with the switch in position 2

Next, we simplify these equations by assuming that the switching ripples in $i(t)$ and $v(t)$ are small compared to their respective dc components I and V . Hence, $i(t) \approx I$ and $v(t) \approx V$, and Eqs. (3.6) and (3.7) become

$$v_L(t) = V_g - IR_L \quad (3.8)$$

$$i_C(t) = -\frac{V}{R}$$

For $DT_s < t < T_s$, the switch is in position 2 and the circuit reduces to Fig. 3.7b. The inductor current and capacitor voltage are then given by

$$\begin{aligned} v_L(t) &= V_g - i(t)R_L - v(t) \approx V_g - IR_L - V \\ i_C(t) &= i(t) - \frac{v(t)}{R} \approx I - \frac{V}{R} \end{aligned} \quad (3.9)$$

We again make the small-ripple approximation.

The principle of inductor volt-second balance can now be invoked. Equations (3.8) and (3.9) are used to construct the inductor voltage waveform $v_L(t)$ in Fig. 3.8. The dc component, or average value, of the inductor voltage $v_L(t)$ is

$$\langle v_L(t) \rangle = \frac{1}{T_s} \int_0^{T_s} v_L(t) dt = D(V_g - IR_L) + D'(V_g - IR_L - V) \quad (3.10)$$

By setting $\langle v_L \rangle$ to zero and collecting terms, one obtains

$$0 = V_g - IR_L - D'V \quad (3.11)$$

(recall that $D + D' = 1$). It can be seen that the inductor winding resistance R_L adds another term to the inductor volt-second balance equation. In the ideal boost converter ($R_L = 0$) example

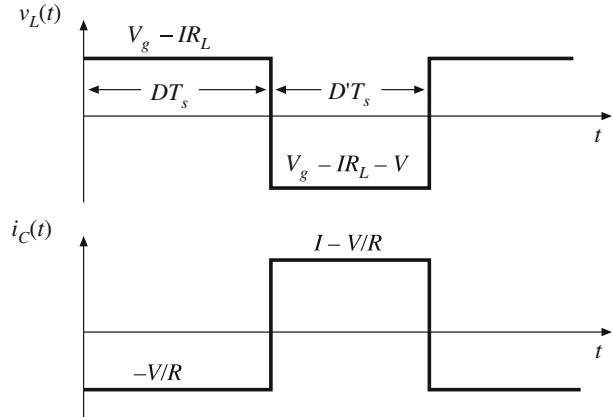


Fig. 3.8 Inductor voltage and capacitor current waveforms, for the nonideal boost converter of Fig. 3.6

of Chap. 2, we were able to solve this equation directly for the voltage conversion ratio V/V_g . Equation (3.11) cannot be immediately solved in this manner, because the inductor current I is unknown. A second equation is needed, to eliminate I .

The second equation is obtained using capacitor charge balance. The capacitor current $i_C(t)$ waveform is given in Fig. 3.8. The dc component, or average value, of the capacitor current waveform is

$$\langle i_C(t) \rangle = D \left(-\frac{V}{R} \right) + D' \left(I - \frac{V}{R} \right) \quad (3.12)$$

By setting $\langle i_C \rangle$ to zero and collecting terms, one obtains

$$0 = D'I - \frac{V}{R} \quad (3.13)$$

We now have two equations, Eqs. (3.11) and (3.13), and two unknowns, V and I . Elimination of I and solution for V yields

$$\frac{V}{V_g} = \frac{1}{D'} \frac{1}{\left(1 + \frac{R_L}{D'^2 R} \right)} \quad (3.14)$$

This is the desired solution for the converter output voltage V . It is plotted in Fig. 3.9 for several values of R_L/R . It can be seen that Eq. (3.14) contains two terms. The first, $1/D'$, is the ideal conversion ratio, with $R_L = 0$. The second term, $1/(1 + R_L/D'^2 R)$, describes the effect of the inductor winding resistance. If R_L is much less than $D'^2 R$, then the second term is approximately equal to unity and the conversion ratio is approximately equal to the ideal value $1/D'$. However, as R_L is increased in relation to $D'^2 R$, then the second term is reduced in value, and V/V_g is reduced as well.

As the duty cycle D approaches one, the inductor winding resistance R_L causes a major qualitative change in the V/V_g curve. Rather than approaching infinity at $D = 1$, the curve tends to zero. Of course, it is unreasonable to expect that the converter can produce infinite voltage, and it should be comforting to the engineer that the prediction of the model is now more realistic. What happens at $D = 1$ is that the switch is always in position 1. The inductor is never connected to the output, so no energy is transferred to the output and the output voltage tends to zero. The inductor current tends to a large value, limited only by the inductor resistance R_L . A large amount of power is lost in the inductor winding resistance, equal to V_g^2/R_L , while

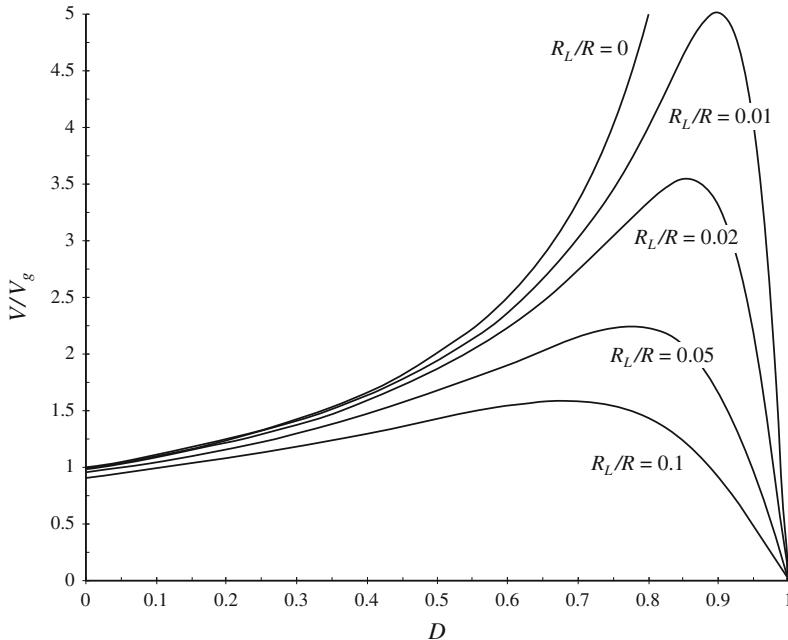


Fig. 3.9 Output voltage vs. duty cycle, boost converter with inductor copper loss

no power is delivered to the load; hence, we can expect that the converter efficiency tends to zero at $D = 1$.

Another implication of Fig. 3.9 is that the inductor winding resistance R_L limits the maximum voltage that the converter can produce. For example, with $R_L/R = 0.02$, it can be seen that the maximum V/V_g is approximately 3.5. If it is desired to obtain $V/V_g = 5$, then according to Fig. 3.9 the inductor winding resistance R_L must be reduced to less than 1% of the load resistance R . The only problem is that decreasing the inductor winding resistance requires building a larger, heavier, more expensive inductor. So it is usually important to optimize the design, by correctly modeling the effects of loss elements such as R_L , and choosing the smallest inductor that will do the job. We now have the analytical tools needed to do this.

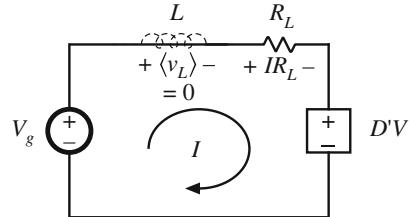
3.3 Construction of Equivalent Circuit Model

Next, let us refine the dc transformer model, to account for converter losses. This will allow us to determine the converter voltages, currents, and efficiency using well-known techniques of circuit analysis.

In the previous section, we used the principles of inductor volt-second balance and capacitor charge balance to write Eqs. (3.11) and (3.13), repeated here:

$$\begin{aligned}\langle v_L \rangle &= 0 = V_g - IR_L - D'V \\ \langle i_C \rangle &= 0 = D'I - \frac{V}{R}\end{aligned}\tag{3.15}$$

Fig. 3.10 Circuit whose loop equation is identical to Eq. (3.16), obtained by equating the average inductor voltage $\langle v_L \rangle$ to zero



These equations state that the dc components of the inductor voltage and capacitor current are equal to zero. Rather than algebraically solving the equations as in the previous section, we can reconstruct a circuit model based on these equations, which describes the dc behavior of the boost converter with inductor copper loss. This is done by constructing a circuit whose Kirchhoff loop and node equations are identical to Eqs. (3.15).

3.3.1 Inductor Voltage Equation

$$\langle v_L \rangle = 0 = V_g - IR_L - D'V \quad (3.16)$$

This equation was derived by use of Kirchhoff's voltage law to find the inductor voltage during each subinterval. The results were averaged and set to zero. Equation (3.16) states that the sum of three terms having the dimensions of voltage are equal to $\langle v_L \rangle$, or zero. Hence, Eq. (3.16) is of the same form as a loop equation; in particular, it describes the dc components of the voltages around a loop containing the inductor, with loop current equal to the dc inductor current I .

So let us construct a circuit containing a loop with current I , corresponding to Eq. (3.16). The first term in Eq. (3.16) is the dc input voltage V_g , so we should include a voltage source of value V_g as shown in Fig. 3.10. The second term is a voltage drop of value IR_L , which is proportional to the current I in the loop. This term corresponds to a resistance of value R_L . The third term is a voltage $D'V$, dependent on the converter output voltage. For now, we can model this term using a dependent voltage source, with polarity chosen to satisfy Eq. (3.16).

3.3.2 Capacitor Current Equation

$$\langle i_C \rangle = 0 = D'I - \frac{V}{R} \quad (3.17)$$

This equation was derived using Kirchhoff's current law to find the capacitor current during each subinterval. The results were averaged, and the average capacitor current was set to zero.

Equation (3.17) states that the sum of two dc currents is equal to $\langle i_C \rangle$, or zero. Hence, Eq. (3.17) is of the same form as a node equation; in particular, it describes the dc components of currents flowing into a node connected to the capacitor. The dc capacitor voltage is V .

So now let us construct a circuit containing a node connected to the capacitor, as in Fig. 3.11, whose node equation satisfies Eq. (3.17). The second term in Eq. (3.17) is a current of magnitude V/R , proportional to the dc capacitor voltage V . This term corresponds to a resistor of value R , connected in parallel with the capacitor so that its voltage is V and hence its current is V/R . The first term is a current $D'I$, dependent on the dc inductor current I . For now, we can model this term using a dependent current source as shown. The polarity of the source is chosen to satisfy Eq. (3.17).

3.3.3 Complete Circuit Model

The next step is to combine the circuits of Figs. 3.10 and 3.11 into a single circuit, as in Fig. 3.12. This circuit can be further simplified by recognizing that the dependent voltage and current sources constitute an ideal dc transformer, as discussed in Sect. 3.1. The $D'V$ dependent voltage source depends on V , the voltage across the dependent current source. Likewise, the $D'I$ dependent current source depends on I , the current flowing through the dependent voltage source. In each case, the coefficient is D' . Hence, the dependent sources form a circuit similar to Fig. 3.2; the fact that the voltage source appears on the primary rather than the secondary side is irrelevant, owing to the symmetry of the transformer. They are therefore equivalent to the dc transformer model of Fig. 3.3, with turns ratio $D' : 1$. Substitution of the ideal dc transformer model for the dependent sources yields the equivalent circuit of Fig. 3.13.

The equivalent circuit model can now be manipulated and solved to find the converter voltages and currents. For example, we can eliminate the transformer by referring the V_g voltage source and R_L resistance to the secondary side. As shown in Fig. 3.14, the voltage source value is divided by the effective turns ratio D' , and the resistance R_L is divided by the square of the turns ratio, D'^2 . This circuit can be solved directly for the output voltage V , using the voltage divider formula:

$$V = \frac{V_g}{D'} \frac{R}{R + \frac{R_L}{D'^2}} = \frac{V_g}{D'} \frac{1}{1 + \frac{R_L}{D'^2 R}} \quad (3.18)$$

This result is identical to Eq. (3.14). The circuit can also be solved directly for the inductor current I , by referring all elements to the transformer primary side. The result is

Fig. 3.11 Circuit whose node equation is identical to Eq. (3.17), obtained by equating the average capacitor current $\langle i_C \rangle$ to zero

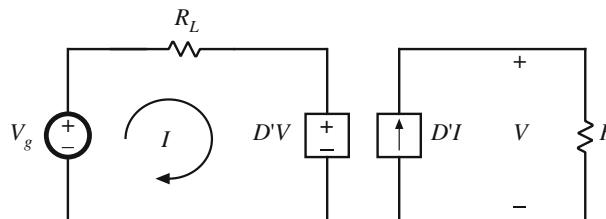
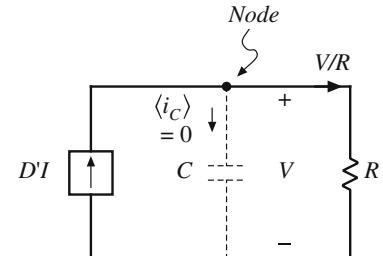


Fig. 3.12 The circuits of Figs. 3.10 and 3.11, drawn together

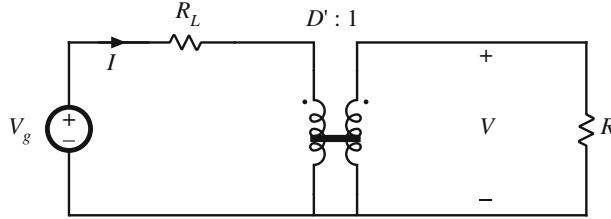
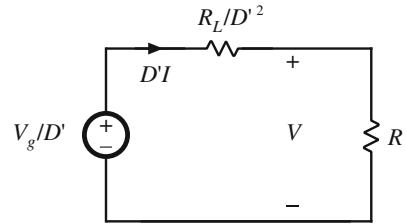


Fig. 3.13 Equivalent circuit model of the boost converter, including a $D' : 1$ dc transformer and the inductor winding resistance R_L

Fig. 3.14 Simplification of the equivalent circuit of Fig. 3.13, by referring all elements to the secondary side of the transformer



$$I = \frac{V_g}{D'^2R + R_L} = \frac{V_g}{D'^2R} \frac{1}{1 + \frac{R_L}{D'^2R}} \quad (3.19)$$

3.3.4 Efficiency

The equivalent circuit model also allows us to compute the converter efficiency η . Figure 3.13 predicts that the converter input power is

$$P_{in} = (V_g)(I) \quad (3.20)$$

The load current is equal to the current in the secondary of the ideal dc transformer, or $D'I$. Hence, the model predicts that the converter output power is

$$P_{out} = (V)(D'I) \quad (3.21)$$

Therefore, the converter efficiency is

$$\eta = \frac{P_{out}}{P_{in}} = \frac{(V)(D'I)}{(V_g)(I)} = \frac{V}{V_g} D' \quad (3.22)$$

Substitution of Eq. (3.18) into Eq. (3.22) to eliminate V yields

$$\eta = \frac{1}{1 + \frac{R_L}{D'^2R}} \quad (3.23)$$

This equation is plotted in Fig. 3.15, for several values of R_L/R . It can be seen from Eq. (3.23) that, to obtain high efficiency, the inductor winding resistance R_L should be much smaller than

D'^2R , the load resistance referred to the primary side of the ideal dc transformer. This is easier to do at low duty cycle, where D' is close to unity, than at high duty cycle where D' approaches zero. It can be seen from Fig. 3.15 that the efficiency is typically high at low duty cycles, but decreases rapidly to zero near $D = 1$.

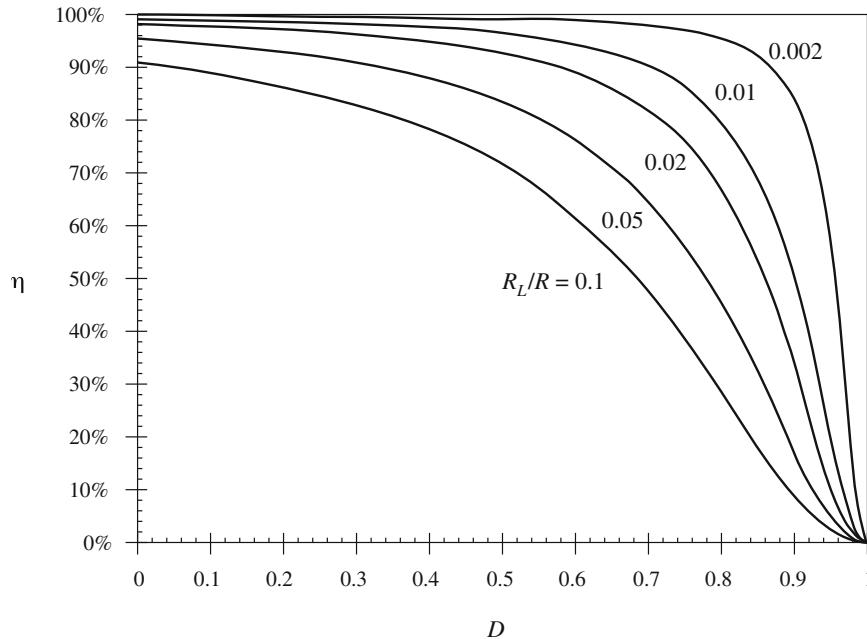


Fig. 3.15 Efficiency vs. duty cycle, boost converter with inductor copper loss

Thus, the basic dc transformer model can be refined to include other effects, such as the inductor copper loss. The model describes the basic properties of the converter, including (a) transformation of dc voltage and current levels, (b) second-order effects such as power losses, and (c) the conversion ratio M . The model can be solved to find not only the output voltage V , but also the inductor current I and the efficiency η . All of the well-known techniques of circuit analysis can be employed to solve the model, making this a powerful and versatile approach.

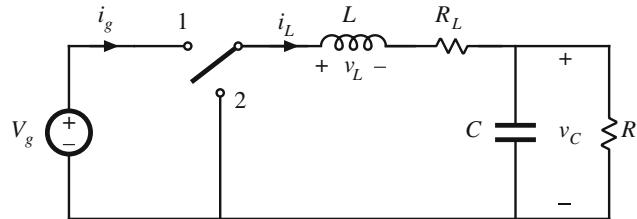
The example considered so far is a relatively simple one, in which there is only a single loss element, R_L . Of course, real converters are considerably more complicated, and contain a large number of loss elements. When solving a complicated circuit to find the output voltage and efficiency, it behooves the engineer to use the simplest and most physically meaningful method possible. Writing a large number of simultaneous loop or node equations is not the best approach, because its solution typically requires several pages of algebra, and the engineer usually makes algebra mistakes along the way. The practicing engineer often gives up before finding the correct solution. The equivalent circuit approach avoids this situation, because one can simplify the circuit via well-known circuit manipulations such as pushing the circuit elements to the secondary side of the transformer. Often the answer can then be written by inspection, using

the voltage divider rule or other formulas. The engineer develops confidence that the result is correct, and does not contain algebra mistakes.

3.4 How to Obtain the Input Port of the Model

Let us try to derive the model of the buck converter of Fig. 3.16, using the procedure of Sect. 3.3. The inductor winding resistance is again modeled by a series resistor R_L .

Fig. 3.16 Buck converter example



The average inductor voltage can be shown to be

$$\langle v_L \rangle = 0 = DV_g - I_L R_L - V_C \quad (3.24)$$

This equation describes a loop with the dc inductor current I_L . The dc components of the voltages around this loop are: (i) the DV_g term, modeled as a dependent voltage source, (ii) a voltage drop $I_L R_L$, modeled as resistor R_L , and (iii) the dc output voltage V_C .

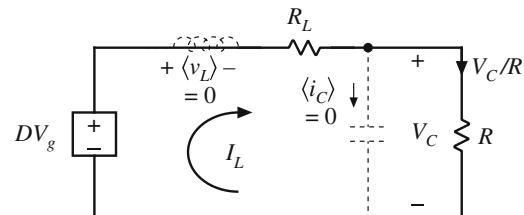
The average capacitor current is

$$\langle i_C \rangle = 0 = I_L - \frac{V_C}{R} \quad (3.25)$$

This equation describes the dc currents flowing into the node connected to the capacitor. The dc component of inductor current, I_L , flows into this node. The dc load current V_C/R (i.e., the current flowing through the load resistor R) flows out of this node. An equivalent circuit that models Eqs. (3.24) and (3.25) is given in Fig. 3.17. This circuit can be solved to determine the dc output voltage V_C .

What happened to the dc transformer in Fig. 3.17? We expect the buck converter model to contain a dc transformer, with turns ratio equal to the dc conversion ratio, or 1:D. According to Fig. 3.2, the secondary of this transformer is equivalent to a dependent voltage source, of value DV_g . Such a source does indeed appear in Fig. 3.17. But where is the primary? From Fig. 3.2, we expect the primary of the dc transformer to be equivalent to a dependent current source. In

Fig. 3.17 Equivalent circuit derived from Eqs. (3.24) and (3.25)



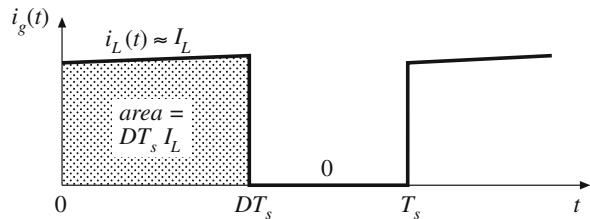


Fig. 3.18 Converter input current waveform $i_g(t)$

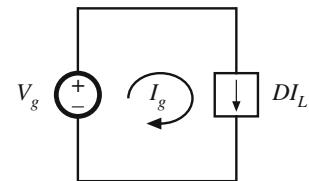
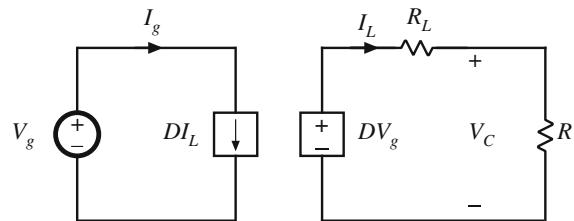


Fig. 3.19 Converter input port dc equivalent circuit



general, to derive this source, it is necessary to find the dc component of the converter input current $i_g(t)$.

The converter input current waveform $i_g(t)$ is sketched in Fig. 3.18. When the switch is in position 1, $i_g(t)$ is equal to the inductor current. Neglecting the inductor current ripple, we have $i_g(t) \approx I_L$. When the switch is in position 2, $i_g(t)$ is zero. The dc component, or average value, of $i_g(t)$ is

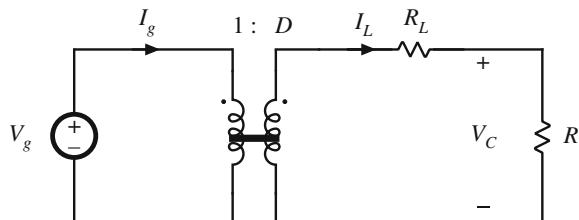
$$I_g = \frac{1}{T_s} \int_0^{T_s} i_g(t) dt = D I_L \quad (3.26)$$

The integral of $i_g(t)$ is equal to the area under the $i_g(t)$ curve, or $D T_s I_L$ according to Fig. 3.18. The dc component I_g is therefore $(D T_s I_L)/T_s = D I_L$. Equation (3.26) states that I_g , the dc component of current drawn by the converter out of the V_g source, is equal to $D I_L$. An equivalent circuit is given in Fig. 3.19.

A complete model for the buck converter can now be obtained by combining Figs. 3.17 and 3.19 to obtain Fig. 3.20. The dependent current and voltage sources can be combined into a dc transformer, since the DV_g dependent voltage source has value D times the voltage V_g across the dependent current source, and the current source is the same constant D times the current I_L through the dependent voltage source. So, according to Fig. 3.2, the sources are equivalent to a dc transformer with turns ratio $1:D$, as shown in Fig. 3.21.

In general, to obtain a complete dc equivalent circuit that models the converter input port, it is necessary to write an equation for the dc component of the converter input current. An equivalent circuit corresponding to this equation is then constructed. In the case of the buck converter, as well as in other converters having pulsating input currents, this equivalent circuit contains a dependent current source which becomes the primary of a dc transformer model. In the boost

Fig. 3.21 Equivalent circuit of the buck converter, including a $1 : D$ dc transformer and the inductor winding resistance R_L



converter example of Sect. 3.3, it was unnecessary to explicitly write this equation, because the input current $i_g(t)$ coincided with the inductor current $i(t)$, and hence a complete equivalent circuit could be derived using only the inductor voltage and capacitor current equations.

3.5 Example: Inclusion of Semiconductor Conduction Losses in the Boost Converter Model

As a final example, let us consider modeling semiconductor conduction losses in the boost converter of Fig. 3.22. Another major source of power loss is the conduction loss due to semiconductor device forward voltage drops. The forward voltage of a metal oxide semiconductor field-effect transistor (MOSFET) or bipolar junction transistor (BJT) can be modeled with reasonable accuracy as an on-resistance R_{on} . In the case of a diode, insulated-gate bipolar transistor (IGBT), or thyristor, a voltage source plus an on-resistance yields a model of good accuracy; the on-resistance may be omitted if the converter is being modeled at a single operating point.

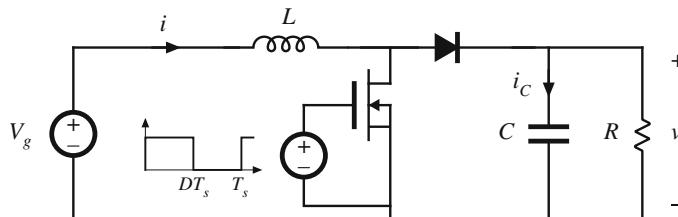


Fig. 3.22 Boost converter example

When the gate drive signal is high, the MOSFET turns on and the diode is reverse-biased. The circuit then reduces to Fig. 3.23a. In the conducting state, the MOSFET is modeled by the on-resistance R_{on} . The inductor winding resistance is again represented as in Fig. 3.5. The inductor voltage and capacitor current are given by

$$v_L(t) = V_g - iR_L - iR_{on} \approx V_g - IR_L - IR_{on} \quad (3.27)$$

$$i_C(t) = -\frac{v}{R} \approx -\frac{V}{R}$$

The inductor current and capacitor voltage have again been approximated by their dc components.

When the gate drive signal is low, the MOSFET turns off. The diode becomes forward-biased by the inductor current, and the circuit reduces to Fig. 3.23b. In the conducting state, the diode is modeled in this example by voltage source V_D and resistance R_D . The inductor winding

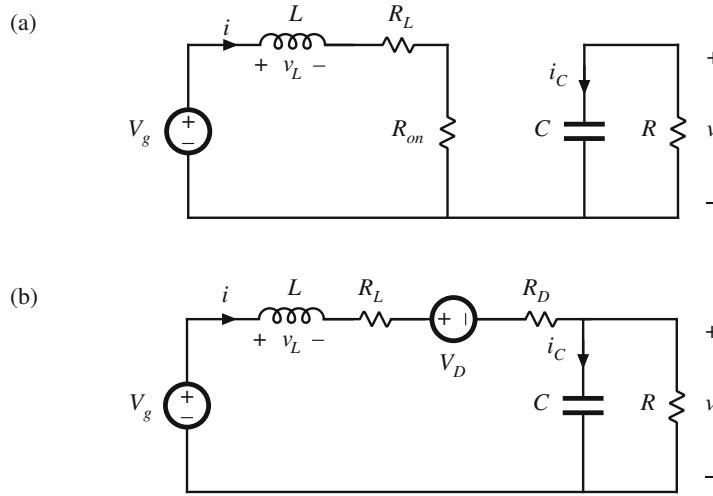


Fig. 3.23 Boost converter circuits: (a) when MOSFET conducts, (b) when diode conducts

resistance is again modeled by resistance \$R_L\$. The inductor voltage and capacitor current for this subinterval are

$$\begin{aligned} v_L(t) &= V_g - iR_L - V_D - iR_D - v \approx V_g - IR_L - V_D - IR_D - V \\ i_C(t) &= i - \frac{v}{R} \approx I - \frac{V}{R} \end{aligned} \quad (3.28)$$

The inductor voltage and capacitor current waveforms are sketched in Fig. 3.24.

The dc component of the inductor voltage is given by

$$\langle v_L \rangle = D(V_g - IR_L - IR_{on}) + D'(V_g - IR_L - V_D - IR_D - V) = 0 \quad (3.29)$$

By collecting terms and noting that \$D + D' = 1\$, one obtains

$$V_g - IR_L - IDR_{on} - D'V_D - ID'R_D - D'V = 0 \quad (3.30)$$

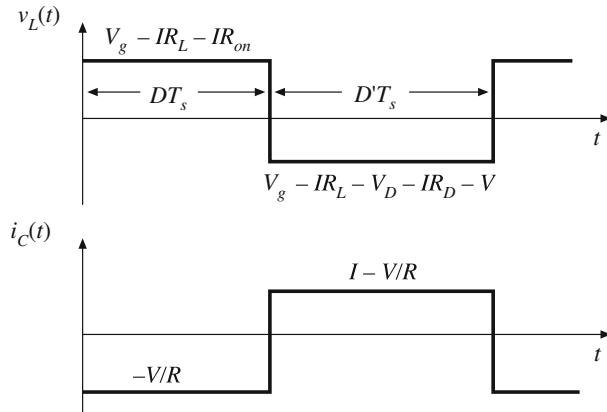


Fig. 3.24 Inductor voltage \$v_L(t)\$ and capacitor current \$i_C(t)\$ waveforms, for the converter of Fig. 3.22

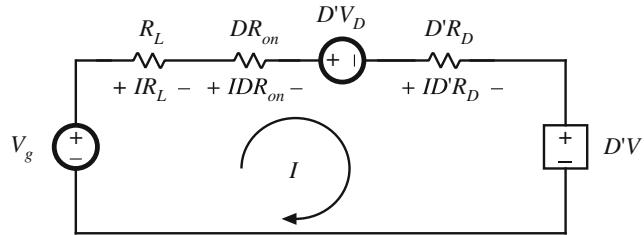


Fig. 3.25 Equivalent circuit corresponding to Eq. (3.30)

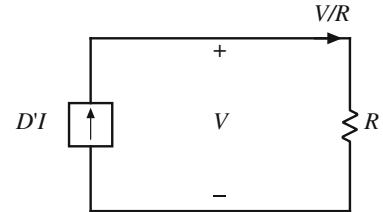


Fig. 3.26 Equivalent circuit corresponding to Eq. (3.32)

This equation describes the dc components of the voltages around a loop containing the inductor, with loop current equal to the dc inductor current I . The resistive terms (for example, IDR_{on}) are interpreted as the voltage drop across resistive elements having current I and resistance equal to the remaining terms (for the example, the effective resistance is DR_{on}). An equivalent circuit is given in Fig. 3.25.

The dc component of the capacitor current is

$$\langle i_C \rangle = D\left(-\frac{V}{R}\right) + D'\left(I - \frac{V}{R}\right) = 0 \quad (3.31)$$

Upon collecting terms, one obtains

$$D'I - \frac{V}{R} = 0 \quad (3.32)$$

This equation describes the dc components of the currents flowing into a node connected to the capacitor, with dc capacitor voltage equal to V . An equivalent circuit is given in Fig. 3.26.

The two circuits are drawn together in Fig. 3.27. The dependent sources are combined into an ideal $D':1$ transformer in Fig. 3.28, yielding the complete dc equivalent circuit model.

Solution of Fig. 3.28 for the output voltage V yields

$$V = \left(\frac{1}{D'}\right)(V_g - D'V_D)\left(\frac{D'^2R}{D'^2R + R_L + DR_{on} + D'R_D}\right) \quad (3.33)$$

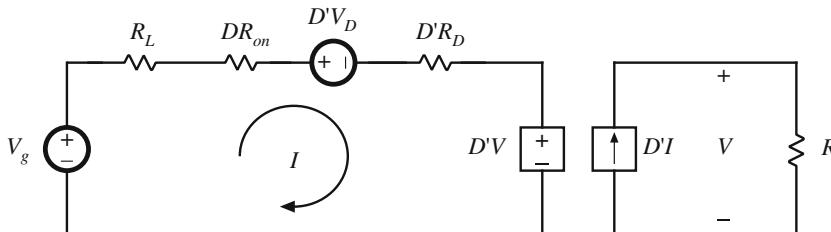


Fig. 3.27 The circuits of Figs. 3.25 and 3.26, drawn together

Dividing by V_g gives the voltage conversion ratio:

$$\frac{V}{V_g} = \left(\frac{1}{D'} \right) \left(1 - \frac{D'V_D}{V_g} \right) \left(\frac{1}{1 + \frac{R_L + DR_{on} + D'R_D}{D'^2 R}} \right) \quad (3.34)$$

It can be seen that the effect of the loss elements V_D , R_L , R_{on} , and R_D is to decrease the voltage conversion ratio below the ideal value ($1/D'$).

The efficiency is given by $\eta = P_{out}/P_{in}$. From Fig. 3.28, $P_{in} = V_g I$ and $P_{out} = VD'I$. Hence,

$$\eta = D' \frac{V}{V_g} = \frac{\left(1 - \frac{D'V_D}{V_g} \right)}{\left(1 + \frac{R_L + DR_{on} + D'R_D}{D'^2 R} \right)} \quad (3.35)$$

For high efficiency, we require

$$\begin{aligned} V_g/D' &\gg V_D \\ D'^2 R &\gg R_L + DR_{on} + D'R_D \end{aligned} \quad (3.36)$$

It may seem strange that the equivalent circuit model of Fig. 3.28 contains effective resistances DR_{on} and $D'R_D$, whose values vary with duty cycle. The reason for this dependence is that the semiconductor on-resistances are connected in the circuit only when their respective semiconductor devices conduct. For example, at $D = 0$, the MOSFET never conducts, and the effective resistance DR_{on} disappears from the model. These effective resistances correctly model the average power losses in the elements. For instance, the equivalent circuit predicts that the power loss in the MOSFET on-resistance is $I^2 DR_{on}$. In the actual circuit, the MOSFET conduction loss is $I^2 R_{on}$ while the MOSFET conducts, and zero while the MOSFET is off. Since the MOSFET conducts with duty cycle D , the average conduction loss is $DI^2 R_{on}$, which coincides with the prediction of the model.

In general, to predict the power loss in a resistor R , we must calculate the root-mean-square current I_{rms} through the resistor, rather than the average current. The average power loss is then

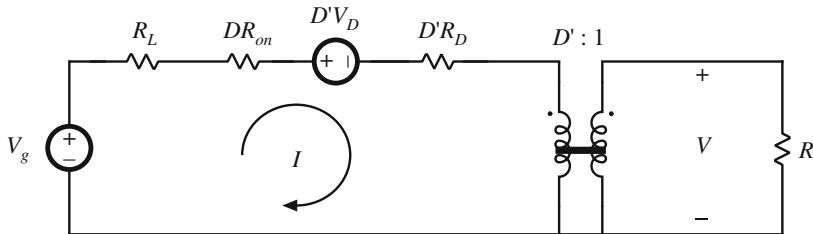


Fig. 3.28 Equivalent circuit model of the boost converter of Fig. 3.22, including ideal dc transformer, inductor winding resistance, and MOSFET and diode conduction losses

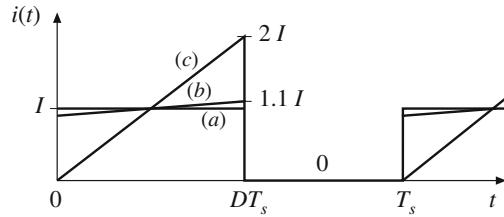


Fig. 3.29 Transistor current waveform, for various filter inductor values: (a) with a very large inductor, such that $\Delta i \approx 0$; (b) with a typical inductor value, such that $\Delta i = 0.1I$; (c) with a small inductor value, chosen such that $\Delta i = I$

given by $I_{rms}^2 R$. Nonetheless, the average model of Fig. 3.28 correctly predicts average power loss, provided that the inductor current ripple is small. For example, consider the MOSFET conduction loss in the buck converter. The actual transistor current waveform is sketched in Fig. 3.29, for several values of inductor current ripple Δi . Case (a) corresponds to use of an infinite inductance L , leading to zero inductor current ripple. As shown in Table 3.1, the MOSFET conduction loss is then given by $I_{rms}^2 R_{on} = DI^2 R_{on}$, which agrees exactly with the prediction of the average model. Case (b) is a typical choice of inductance L , leading to an inductor current ripple of $\Delta i = 0.1I$. The exact MOSFET conduction loss, calculated using the rms value of MOSFET current, is then only 0.33% greater than the prediction of the average model. In the extreme case (c) where $\Delta i = I$, the actual conduction loss is 33% greater than that predicted by the average model. Thus, the dc (average) model correctly predicts losses in the component nonidealities, even though rms currents are not calculated. The model is accurate provided that the inductor current ripple is small.

Table 3.1 Effect of inductor current ripple on MOSFET conduction loss

Inductor current ripple	MOSFET rms current	Average power loss in R_{on}
(a) $\Delta i = 0$	$I\sqrt{D}$	$DI^2 R_{on}$
(b) $\Delta i = 0.1i$	$(1.00167)I\sqrt{D}$	$(1.0033)DI^2 R_{on}$
(c) $\Delta i = I$	$(1.155)I\sqrt{D}$	$(1.3333)DI^2 R_{on}$

3.6 Summary of Key Points

1. The dc transformer model represents the primary functions of any dc-dc converter: transformation of dc voltage and current levels, ideally with 100% efficiency, and control of the conversion ratio M via the duty cycle D . This model can be easily manipulated and solved using familiar techniques of conventional circuit analysis.
2. The model can be refined to account for loss elements such as inductor winding resistance and semiconductor on-resistances and forward voltage drops. The refined model predicts the voltages, currents, and efficiency of practical nonideal converters.

3. In general, the dc equivalent circuit for a converter can be derived from the inductor volt-second balance and capacitor charge balance equations. Equivalent circuits are constructed whose loop and node equations coincide with the volt-second and charge balance equations. In converters having a pulsating input current, an additional equation is needed to model the converter input port; this equation may be obtained by averaging the converter input current.

PROBLEMS

- 3.1** In the buck-boost converter of Fig. 3.30, the inductor has winding resistance R_L . All other losses can be ignored.

- (a) Derive an expression for the nonideal voltage conversion ratio V/V_g .
- (b) Plot your result of part (a) over the range $0 \leq D \leq 1$, for $R_L/R = 0, 0.01$, and 0.05 .
- (c) Derive an expression for the efficiency. Manipulate your expression into a form similar to Eq. (3.35)

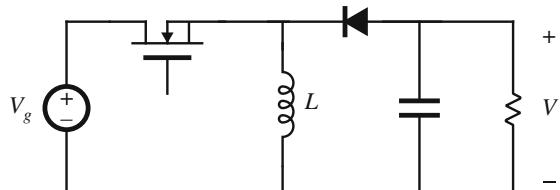


Fig. 3.30 Nonideal buck-boost converter, Problems 3.1 and 3.2

- 3.2** The inductor in the buck-boost converter of Fig. 3.30 has winding resistance R_L . All other losses can be ignored. Derive an equivalent circuit model for this converter. Your model should explicitly show the input port of the converter, and should contain two dc transformers.

- 3.3** In the converter of Fig. 3.31, the inductor has winding resistance R_L . All other losses can be ignored. The switches operate synchronously: each is in position 1 for $0 < t < DT_s$, and in position 2 for $DT_s < t < T_s$.

- (a) Derive an expression for the nonideal voltage conversion ratio V/V_g .

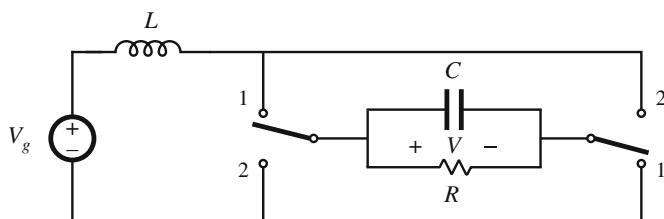


Fig. 3.31 Nonideal current-fed bridge converter, Problems 3.3 and 3.4

- (b) Plot your result of part (a) over the range $0 \leq D \leq 1$, for $R_L/R = 0, 0.01$, and 0.05 .
 (c) Derive an expression for the efficiency. Manipulate your expression into a form similar to Eq. (3.35)

3.4 The inductor in the converter of Fig. 3.31 has winding resistance R_L . All other losses can be ignored. Derive an equivalent circuit model for this converter.

3.5 In the buck converter of Fig. 3.32, the MOSFET has on-resistance R_{on} and the diode forward voltage drop can be modeled by a constant voltage source V_D . All other losses can be neglected.

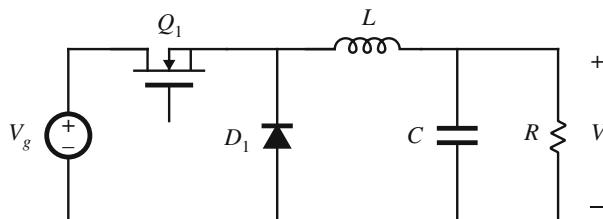


Fig. 3.32 Nonideal buck converter, Problem 3.5

- (a) Derive a complete equivalent circuit model for this converter.
 (b) Solve your model to find the output voltage V .
 (c) Derive an expression for the efficiency. Manipulate your expression into a form similar to Eq. (3.35).

3.6 A single-cell lithium-polymer battery is to be used to power a 3.3 V load. The battery voltage can vary over the usable range $3.0 \text{ V} \leq V_{batt} \leq 4.2 \text{ V}$. It has been decided to use a buck-boost converter for this application, as illustrated in Fig. 3.33 below. A suitable MOSFET transistor has been found for Q_1 , having an on-resistance of $R_{on} = 50 \text{ m}\Omega$. A low- V_F (low forward voltage) Schottky diode is employed for D_1 ; this diode can be modeled as a fixed voltage drop of $V_D = 0.2 \text{ V}$, in series with an effective resistance of $R_D = 0.1 \Omega$. The inductor has winding resistance R_L . All other sources of loss can be neglected.

- (a) Derive an equivalent circuit that models the dc properties of this converter. Include the transistor, diode, and inductor conduction losses as described above. Your equivalent circuit model should correctly describe the converter dc input port. Give analytical expressions for all elements in your model.

“Analytical expressions” are equations or expressions that are written in terms of variable names such as D , R_{on} , V_D , etc., and that do not have numerical values substituted.

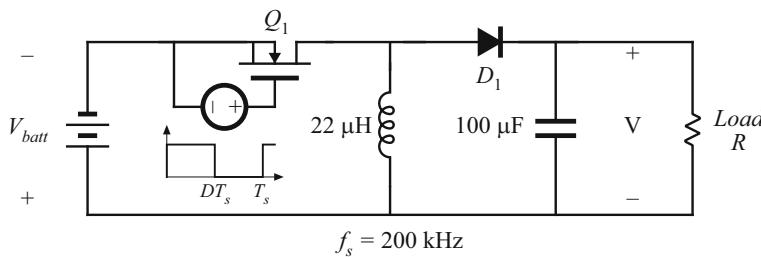


Fig. 3.33 Nonideal buck-boost converter powering a 3.3 V load from a lithium-polymer battery, Problem 3.6

- (b) Solve your model to find analytical expressions for the converter output voltage and efficiency.
- (c) It is decided that the converter must operate with an efficiency of at least 80% under the following operating condition:

Input voltage $V_{batt} = 4.0 \text{ V}$

Output voltage $V = 3.3 \text{ V}$

Load current $I = 2 \text{ A}$

You should assume that a controller system (not shown in Fig. 3.33) adjusts the duty cycle as necessary to regulate the output voltage to be $V = 3.3 \text{ V}$. To meet the above requirements, how large can the inductor winding resistance R_L be? At what duty cycle will the converter then operate? *Note:* there is an easy way and a not-so-easy way to solve this part.

- (d) For your design of Part (c), compute the power loss in each element.
- (e) Accurately plot the converter output voltage and efficiency over the complete range $0 \leq D \leq 1$, using the value of inductor winding resistance R_L computed in Part (c).
- (f) Discuss your plot of Part (e). Does it behave as you expect? Explain.
- 3.7** To reduce the switching harmonics present in the input current of a certain buck converter, an input filter is added as shown in Fig. 3.34. Inductors L_1 and L_2 contain winding resistances R_{L1} and R_{L2} , respectively. The MOSFET has on-resistance R_{on} , and the diode forward voltage drop can be modeled by a constant voltage V_D plus a resistor R_D . All other losses can be ignored.

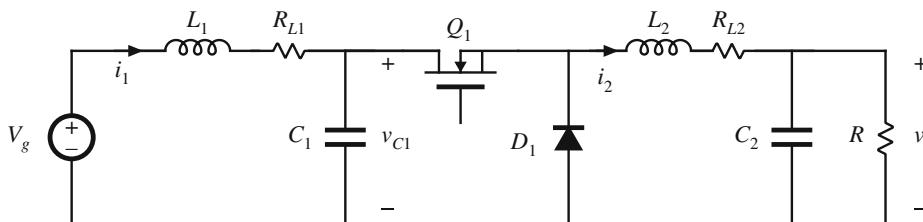


Fig. 3.34 Buck converter with input filter, Problem 3.7

- (a) Derive a complete equivalent circuit model for this circuit.
- (b) Solve your model to find the dc output voltage V .
- (c) Derive an expression for the efficiency. Manipulate your expression into a form similar to Eq. (3.35).
- 3.8** A 1.5 V battery is to be used to power a 5 V, 1 A load. It has been decided to use a buck-boost converter in this application. A suitable transistor is found with an on-resistance of $35 \text{ m}\Omega$, and a Schottky diode is found with a forward drop of 0.5 V. The on-resistance of the Schottky diode may be ignored. The power stage schematic is shown in Fig. 3.35.
- (a) Derive an equivalent circuit that models the dc properties of this converter. Include the transistor and diode conduction losses, as well as the inductor copper loss, but ignore all other sources of loss. Your model should correctly describe the converter dc input port.
- (b) It is desired that the converter operates with at least 70% efficiency under nominal conditions (i.e., when the input voltage is 1.5 V and the output is 5 V at 1 A). How

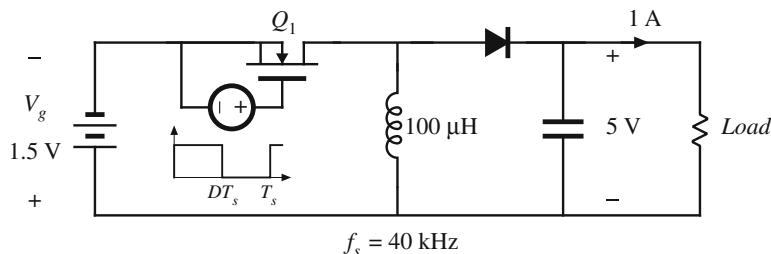


Fig. 3.35 Nonideal buck-boost converter powering a 5 V load from a 1.5 V battery, Problem 3.8

large can the inductor winding resistance be? At what duty cycle will the converter then operate? Note: there is an easy way and a not-so-easy way to analytically solve this part.

- (c) For your design of part (b), compute the power loss in each element.
- (d) Plot the converter output voltage and efficiency over the range $0 \leq D \leq 1$, using the value of inductor winding resistance which you selected in part (b).
- (e) Discuss your plot of part (d). Does it behave as you expect? Explain.

For Problems 3.9 and 3.10, a transistor having an on-resistance of 0.5Ω is used. To simplify the problems, you may neglect all losses other than the transistor conduction loss. You may also neglect the dependence of MOSFET on-resistance on rated blocking voltage. These simplifying assumptions reduce the differences between converters, but do not change the conclusions regarding which converter performs best in the given situations.

- 3.9** It is desired to interface a 500 V dc source to a 400 V, 10 A load using a dc-dc converter. Two possible approaches, using buck and buck-boost converters, are illustrated in Fig. 3.36. Use the assumptions described above to:

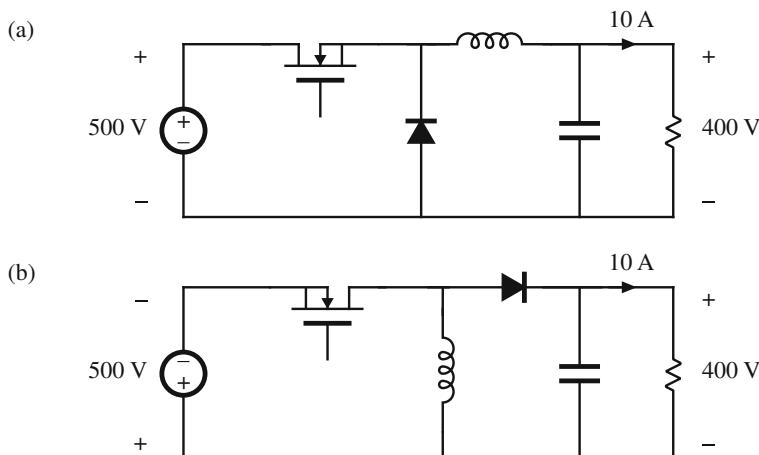


Fig. 3.36 Problem 3.9: interfacing a 500 V source to a 400 V load, using: (a) a buck converter, (b) a buck-boost converter

- (a) Derive equivalent circuit models for both converters, which model the converter input and output ports as well as the transistor conduction loss.
- (b) Determine the duty cycles that cause the converters to operate with the specified conditions.
- (c) Compare the transistor conduction losses and efficiencies of the two approaches, and conclude which converter is better suited to the specified application.
- 3.10** It is desired to interface a 300 V battery to a 400 V, 10 A load using a dc-dc converter. Two possible approaches, using boost and buck-boost converters, are illustrated in Fig. 3.37. Using the assumptions described above (before Problem 3.9), determine the efficiency and power loss of each approach. Which converter is better for this application?

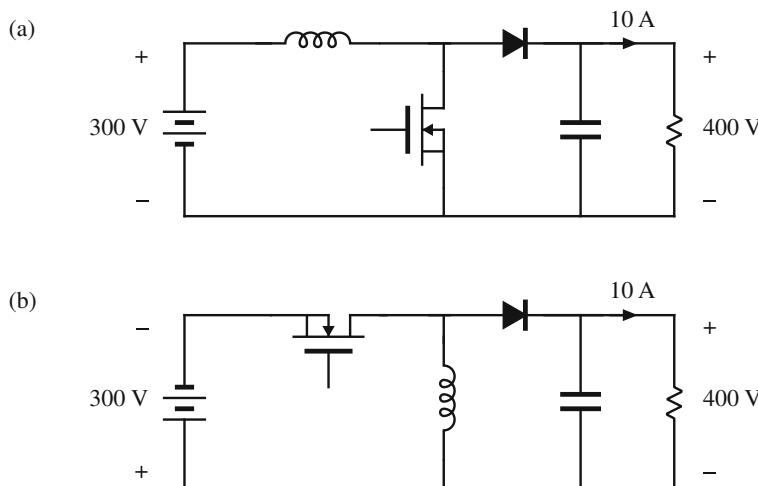


Fig. 3.37 Problem 3.10: interfacing a 300 V battery to a 400 V load, using: (a) a boost converter, (b) a buck-boost converter

- 3.11** A buck converter is operated from the rectified 230 V ac mains, such that the converter dc input voltage is

$$V_g = 325 \text{ V} \pm 20\%$$

A control circuit automatically adjusts the converter duty cycle D , to maintain a constant dc output voltage of $V = 240 \text{ V}$ dc. The dc load current I can vary over a 10: 1 range:

$$10 \text{ A} \leq I \leq 1 \text{ A}$$

The MOSFET has an on-resistance of 0.8Ω . The diode conduction loss can be modeled by a 0.7 V source in series with a 0.2Ω resistor. All other losses can be neglected.

- (a) Derive an equivalent circuit that models the converter input and output ports, as well as the loss elements described above.
- (b) Given the range of variation of V_g and I described above, over what range will the duty cycle vary?

- (c) At what operating point (i.e., at what value of V_g and I) is the converter power loss the largest? What is the value of the efficiency at this operating point?

3.12 In the Ćuk converter of Fig. 3.38, the MOSFET has on-resistance R_{on} and the diode has a constant forward voltage drop V_D . All other losses can be neglected.

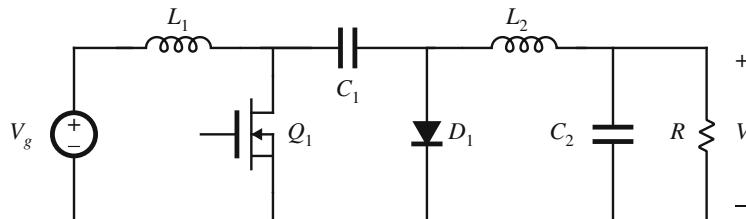


Fig. 3.38 Ćuk converter, Problem 3.12

- (a) Derive an equivalent circuit model for this converter. *Suggestion:* if you do not know how to handle some of the terms in your dc equations, then temporarily leave them as dependent sources. A more physical representation of these terms may become apparent once dc transformers are incorporated into the model.
- (b) Derive analytical expressions for the converter output voltage and for the efficiency.
- (c) For $V_D = 0$, plot V/V_g vs. D over the range $0 \leq D \leq 1$, for (i) $R_{on}/R = 0.01$, and (ii) $R_{on}/R = 0.05$.
- (d) For $V_D = 0$, plot the converter efficiency over the range $0 \leq D \leq 1$, for (i) $R_{on}/R = 0.01$, and (ii) $R_{on}/R = 0.05$.



Switch Realization

We have seen in previous chapters that the switching elements of the buck, boost, and several other dc–dc converters can be implemented using a transistor and diode. One might wonder why this is so, and how to realize semiconductor switches in general. These are worthwhile questions to ask, and switch implementation can depend on the power processing function being performed. The switches of inverters and cycloconverters require more complicated implementations than those of dc–dc converters. Also, the way in which a semiconductor switch is implemented can alter the behavior of a converter in ways not predicted by the ideal-switch analysis of the previous chapters—an example is the discontinuous conduction mode treated in the next chapter. The realization of switches using transistors and diodes is the subject of this chapter.

Semiconductor power devices behave as single-pole single-throw (SPST) switches, represented ideally in Fig. 4.1. So, although we often draw converter schematics using ideal single-pole double-throw (SPDT) switches as in Fig. 4.2a, the schematic of Fig. 4.2b containing SPST switches is more realistic. The realization of a SPDT switch using two SPST switches is not as trivial as it might at first seem, because Fig. 4.2a,b are not exactly equivalent. It is possible for both SPST switches to be simultaneously in the on state or in the off state, leading to behavior not predicted by the SPDT switch of Fig. 4.2a. In addition, it is possible for the switch state to depend on the applied voltage or current waveforms—a familiar example is the diode. Indeed, and it is common for these phenomena to occur in converters operating at light load, or occasionally at heavy load, leading to the discontinuous conduction mode previously mentioned. The converter properties are then significantly modified.

How an ideal switch can be realized using semiconductor devices depends on the polarity of the voltage that the devices must block in the off state, and on the polarity of the current that the devices must conduct in the on state. For example, in the dc–dc buck converter of Fig. 4.2b, switch A must block positive voltage V_g when in the off state, and must conduct positive current i_L when in the on state. If, for all intended converter operating points, the current and blocking voltage lie in a single quadrant of the plane as illustrated in Fig. 4.3, then the switch can be implemented in a simple manner using a transistor or a diode. Use of single-quadrant switches is common in dc–dc converters. Their operation is discussed briefly here.

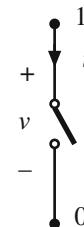


Fig. 4.1 SPST switch, with defined voltage and current polarities

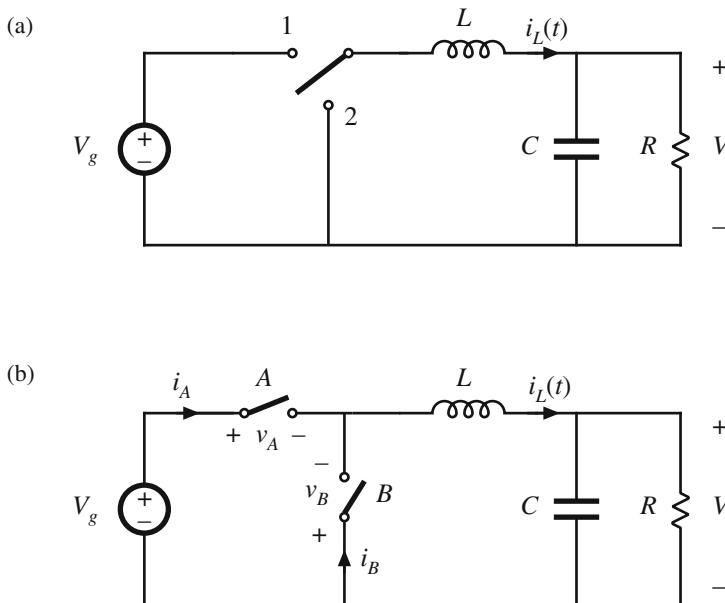


Fig. 4.2 Buck converter: (a) containing SPDT switch, (b) containing two SPST switches

In inverter circuits, two-quadrant switches are required. The output current is ac, and hence is sometimes positive and sometimes negative. If this current flows through the switch, then its current is ac, and the semiconductor switch realization is more complicated. A two-quadrant SPST switch can be realized using a transistor and diode. The dual case also sometimes occurs, in which the switch current is always positive, but the blocking voltage is ac. This type of two-quadrant switch can be constructed using a different arrangement of a transistor and diode. Cycloconverters generally require four-quadrant switches, which are capable of blocking ac voltages and conducting ac currents. Realizations of these elements are also discussed in this chapter.

Next, the synchronous rectifier is examined. The reverse-conducting capability of the metal-oxide-semiconductor field-effect transistor (MOSFET) allows it to be used where a diode would normally be required. If the MOSFET on-resistance is sufficiently small, then its conduction loss is less than that obtained using a diode. Synchronous rectifiers are sometimes used in low-voltage high-current applications to obtain improved efficiency. Several basic references treating single-, two-, and four-quadrant switches are listed in the bibliography [4, 18–25].

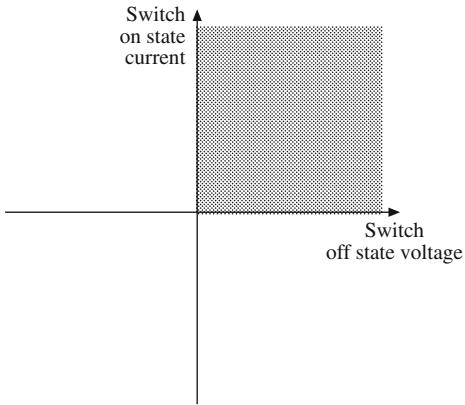


Fig. 4.3 A single-quadrant switch is capable of conducting currents of a single polarity, and of blocking voltages of a single polarity

Several power semiconductor devices are briefly discussed in Sect. 4.2. Majority-carrier devices, including the MOSFET and Schottky diode, exhibit very fast switching times, and hence are preferred when the off-state voltage levels are not too high. Minority-carrier devices, including the bipolar junction transistor (BJT), insulated-gate bipolar transistor (IGBT), and thyristors [silicon-controlled rectifier (SCR) and gate turn-off thyristor (GTO)] exhibit high breakdown voltages with low forward voltage drops, at the expense of reduced switching speed. Recent diodes and FET devices based on wide-bandgap semiconductors (SiC and GaN) represent a significant advance in the tradeoff between breakdown voltage, forward voltage drop, and switching times.

Having realized the switches using semiconductor devices, switching loss can next be discussed. There are a number of mechanisms that cause energy to be lost during the switching transitions [26]. When a transistor drives a clamped inductive load, it experiences high instantaneous power loss during the switching transitions. Diode stored charge further increases this loss, during the transistor turn-on transition. Energy stored in certain parasitic capacitances and inductances is lost during switching. Parasitic ringing, which decays before the end of the switching period, also indicates the presence of switching loss. Switching loss increases directly with switching frequency, and imposes a maximum limit on the operating frequencies of practical converters.

4.1 Switch Applications

4.1.1 Single-Quadrant Switches

The ideal SPST switch is illustrated in Fig. 4.1. The switch contains power terminals 1 and 0, with current and voltage polarities defined as shown. In the on state, the voltage v is zero, while the current i is zero in the off state. There is sometimes a third terminal C , where a control signal is applied. Distinguishing features of the SPST switch include the control method (active vs. passive) and the region of the i - v plane in which they can operate.

A passive switch does not contain a control terminal C . The state of the switch is determined by the waveforms $i(t)$ and $v(t)$ applied to terminals 0 and 1. The most common example is the diode, illustrated in Fig. 4.4. The ideal diode requires that $v(t) \leq 0$ and $i(t) \geq 0$. The diode is off ($i = 0$) when $v < 0$, and is on ($v = 0$) when $i > 0$. It can block negative voltage but not positive voltage. A passive SPST switch can be realized using a diode provided that the intended operating points [i.e., the values of $v(t)$ and $i(t)$ when the switch is in the on and off states] lie on the diode characteristic of Fig. 4.4b.

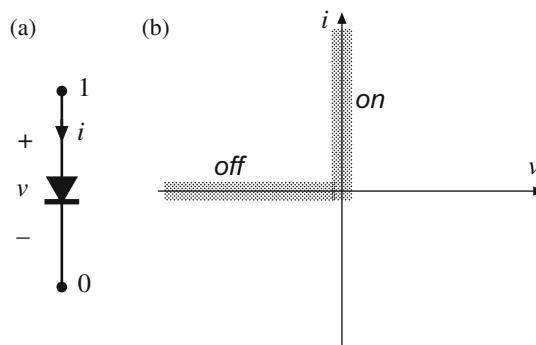


Fig. 4.4 Diode symbol (a), and its ideal characteristic (b)

The conducting state of an active switch is determined by the signal applied to the control terminal C . The state does not directly depend on the waveforms $v(t)$ and $i(t)$ applied to terminals 0 and 1. The BJT, MOSFET, IGBT, GTO, and MCT are examples of active switches. Idealized characteristics $i(t)$ vs. $v(t)$ for the BJT and IGBT are sketched in Fig. 4.5. When the

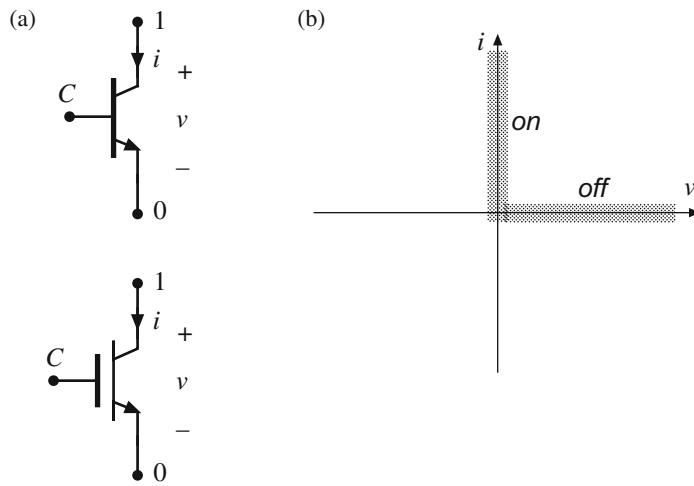


Fig. 4.5 Bipolar junction transistor (BJT) and insulated-gate bipolar transistor (IGBT) symbols (a), and their idealized switch characteristics (b)

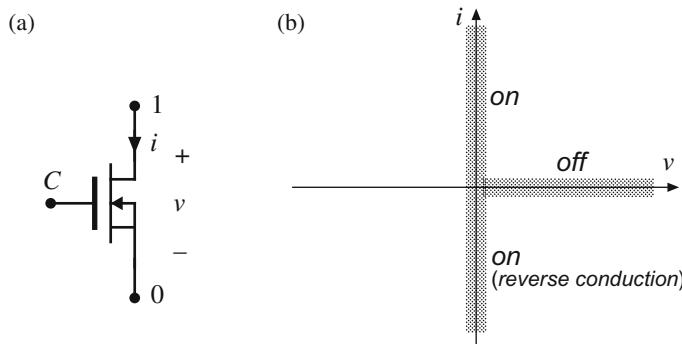


Fig. 4.6 Power MOSFET symbol (a), and its idealized switch characteristic (b)

control terminal causes the transistor to be in the off state, $i = 0$ and the device is capable of blocking positive voltage: $v \geq 0$. When the control terminal causes the transistor to be in the on state, $v = 0$ and the device is capable of conducting positive current: $i \geq 0$. The reverse-conducting and reverse-blocking characteristics of the BJT and IGBT are poor or nonexistent, and have essentially no application in the power converter area. The power MOSFET (Fig. 4.6) has similar characteristics, except that it is able to conduct current in the reverse direction. With one notable exception (the synchronous rectifier discussed later), the MOSFET is normally operated with $i \geq 0$, in the same manner as the BJT and IGBT. So an active SPST switch can be realized using a BJT, IGBT, or MOSFET, provided that the intended operating points lie on the transistor characteristic of Fig. 4.5b.

To determine how to implement an SPST switch using a transistor or diode, one compares the switch operating points with the $i - v$ characteristics of Figs. 4.4b, 4.5b, and 4.6b. For example, when it is intended that the SPDT switch of Fig. 4.2a be in position 1, SPST switch A of

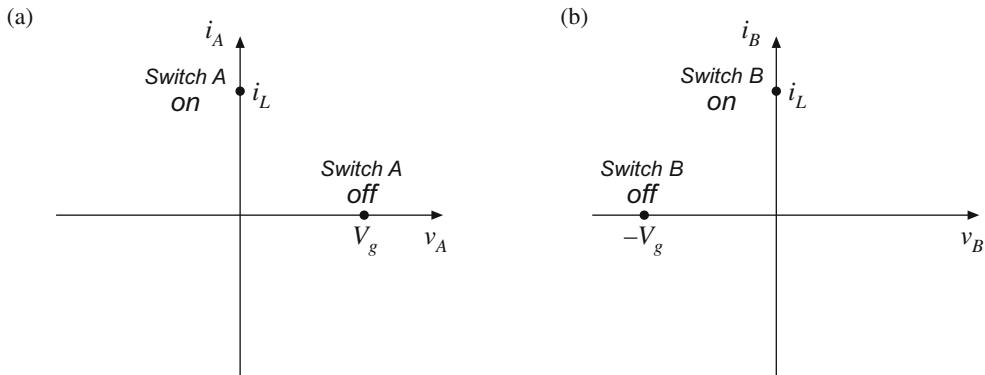


Fig. 4.7 Operating points of switch A, (a), and switch B, (b), in the buck converter of Fig. 4.2b

Fig. 4.2b is closed, and SPST switch B is opened. Switch A then conducts the positive inductor current, $i_A = i_L$, and switch B must block negative voltage, $v_B = -V_g$. These switch operating points are illustrated in Fig. 4.7. Likewise, when it is intended that the SPDT switch of Fig. 4.2a be in position 2, then SPST switch A is opened and switch B is closed. Switch B then conducts the positive inductor current, $i_B = i_L$, while switch A blocks positive voltage, $v_A = V_g$.

By comparison of the switch A operating points of Fig. 4.7a with Figs. 4.5b and 4.6b, it can be seen that a transistor (BJT, IGBT, or MOSFET) could be used, since switch A must block positive voltage and conduct positive current. Likewise, comparison of Fig. 4.7b with Fig. 4.4b reveals that switch B can be implemented using a diode, since switch B must block negative voltage and conduct positive current. Hence a valid switch realization is given in Fig. 4.8.

Figure 4.8 is an example of a single-quadrant switch realization: the devices are capable of conducting current of only one polarity, and blocking voltage of only one polarity. When the controller turns the transistor on, the diode becomes reverse-biased since $v_B = -V_g$. It is required that V_g be positive; otherwise, the diode will be forward-biased. The transistor conducts current i_L . This current should also be positive, so that the transistor conducts in the forward direction.

When the controller turns the transistor off, the diode must turn on so that the inductor current can continue to flow. Turning the transistor off causes the inductor current $i_L(t)$ to decrease. Since $v_L(t) = Ldi_L(t)/dt$, the inductor voltage becomes sufficiently negative to forward-bias the diode, and the diode turns on. Diodes that operate in this manner are sometimes called *freewheeling diodes*. It is required that i_L be positive; otherwise, the diode cannot be forward-

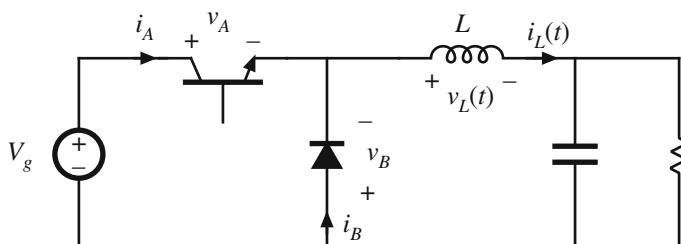


Fig. 4.8 Implementation of SPST switches of Fig. 4.2b using a transistor and diode

biased since $i_B = i_L$. The transistor blocks voltage V_g ; this voltage should be positive to avoid operating the transistor in the reverse blocking mode.

4.1.2 Current-Bidirectional Two-Quadrant Switches

In any number of applications such as dc-ac inverters and servo amplifiers, it is required that the switching elements conduct currents of both polarities, but block only positive voltages. A current-bidirectional two-quadrant SPST switch of this type can be realized using a transistor and diode, connected in an antiparallel manner as in Fig. 4.9.

The MOSFET of Fig. 4.6 is also a two-quadrant switch. However, it should be noted here that practical power MOSFETs inherently contain a built-in diode, often called the *body diode*, as illustrated in Fig. 4.10a. The switching speed of the body diode typically is slower than that of the MOSFET. If the body diode is allowed to conduct, then high peak currents can occur during the diode turn-off transition. Some MOSFETs are not rated to handle these currents, and device failure can occur. To avoid this situation, external series and antiparallel diodes can be added as

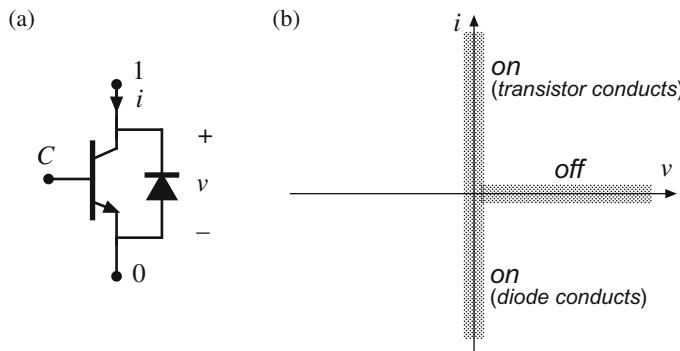


Fig. 4.9 A current-bidirectional two-quadrant SPST switch: (a) implementation using a transistor and antiparallel diode, (b) idealized switch characteristics

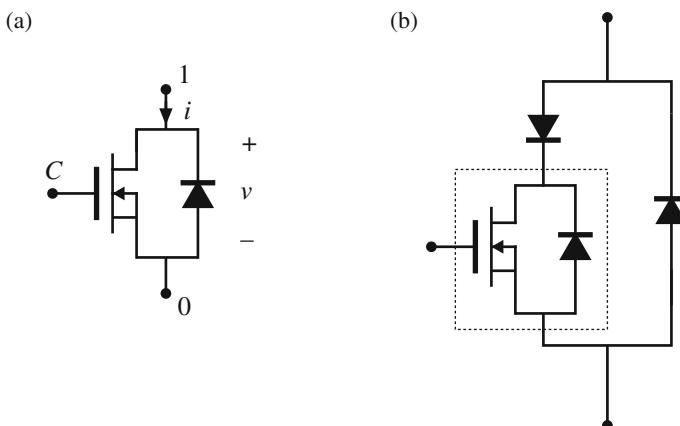


Fig. 4.10 The power MOSFET inherently contains a built-in body diode: (a) equivalent circuit, (b) addition of external diodes to prevent conduction of body diode

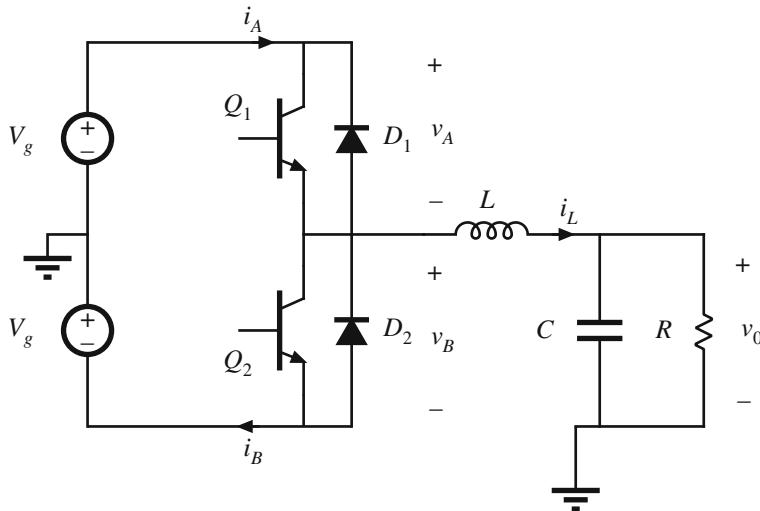
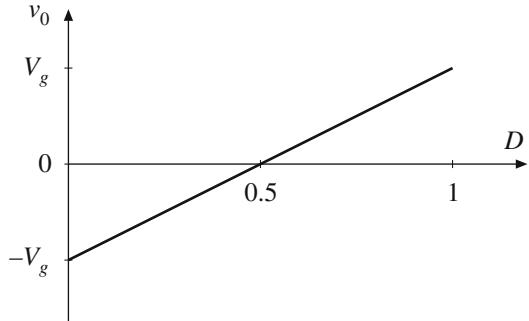


Fig. 4.11 Inverter circuit using two-quadrant switches

Fig. 4.12 Output voltage vs. duty cycle, for the inverter of Fig. 4.11. This converter can produce both positive and negative output voltages



in Fig. 4.10b. Power MOSFETs can be specifically designed to have a fast recovery body diode, and to operate reliably when the body diode is allowed to conduct the rated MOSFET current. However, significant switching loss induced by the diode reverse-recovery process (discussed later in this chapter) may occur, depending on the switching speed and stored charge of the body diode.

A SPDT current-bidirectional two-quadrant switch can again be derived using two SPST switches as in Fig. 4.2b. An example is given in Fig. 4.11. This converter operates from positive and negative dc supplies, and can produce an ac output voltage $v(t)$ having either polarity. Transistor Q_2 is driven with the complement of the Q_1 drive signal, so that Q_1 conducts during the first subinterval $0 < t < DT_s$, and Q_2 conducts during the second subinterval $DT_s < t < T_s$.

It can be seen from Fig. 4.11 that the switches must block voltage $2V_g$. It is required that V_g be positive; otherwise, diodes D_1 and D_2 will conduct simultaneously, shorting out the source.

It can be shown via inductor volt-second balance that

$$v_0 = (2D - 1)V_g \quad (4.1)$$

This equation is plotted in Fig. 4.12. The converter output voltage v_0 is positive for $D > 0.5$, and negative for $D < 0.5$. By sinusoidal variation of the duty cycle,

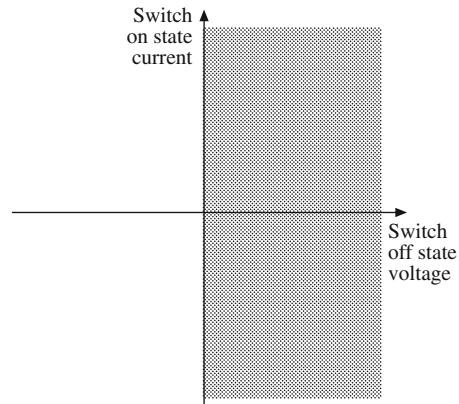


Fig. 4.13 The switches in the inverter of Fig. 4.11 must be capable of conducting both positive and negative current, but need block only positive voltage

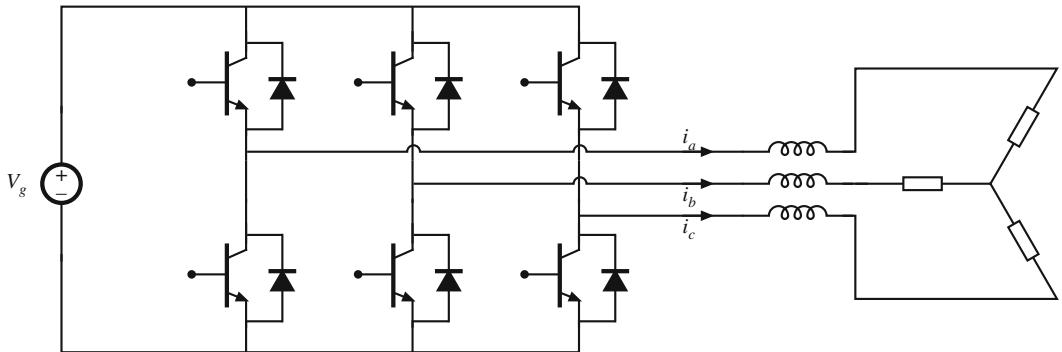


Fig. 4.14 The dc-3 ϕ ac voltage-source inverter requires two-quadrant switches

$$D(t) = 0.5 + D_m \sin(\omega t) \quad (4.2)$$

with D_n being a constant less than 0.5, the output voltage becomes sinusoidal. Hence this converter could be used as a dc-ac inverter.

The load current is given by v_0/R ; in equilibrium, this current coincides with the inductor current i_L ,

$$i_L = \frac{v_0}{R} = (2D - 1) \frac{V_g}{R} \quad (4.3)$$

The switches must conduct this current. So the switch current is also positive when $D > 0.5$, and negative when $D < 0.5$. With high-frequency duty-cycle variations, the $L - C$ filter may introduce a phase lag into the inductor current waveform, but it is nonetheless true that switch currents of both polarities occur. So the switch must operate in two quadrants of the plane, as illustrated in Fig. 4.13. When i_L is positive, Q_1 and D_2 alternately conduct. When i_L is negative, Q_2 and D_1 alternately conduct.

A well-known dc-3 ϕ ac inverter circuit, the *voltage-source inverter* (VSI), operates in a similar manner. As illustrated in Fig. 4.14, the VSI contains three two-quadrant SPDT switches, one per phase. These switches block the dc input voltage V_g , and must conduct the output ac phase currents i_a , i_b , and i_c , respectively. Figure 4.14 illustrates realization of the current-bidirectional switches using IGBTs with antiparallel diodes.

Another current-bidirectional two-quadrant switch example is the bidirectional battery charger/discharger illustrated in Fig. 4.15. This converter can be used, for example, to inter-

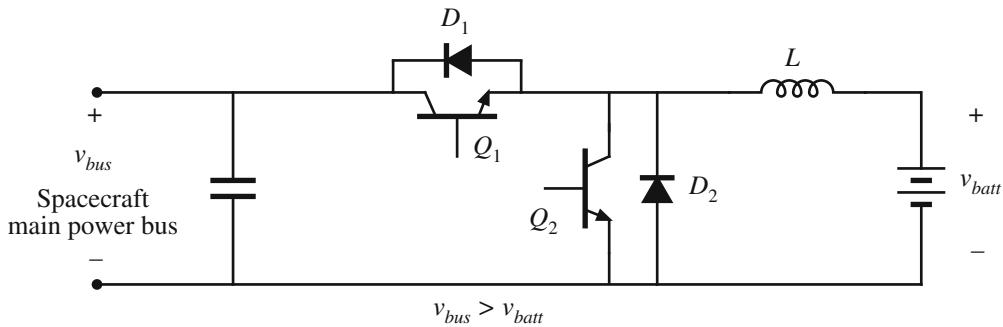


Fig. 4.15 Bidirectional battery charger/discharger, based on the dc–dc buck converter

face a battery to the main power bus of a spacecraft. Both the dc bus voltage v_{bus} and the battery voltage v_{batt} are always positive. The semiconductor switch elements block positive voltage v_{bus} . When the battery is being charged, i_L is positive, and Q_1 and D_2 alternately conduct current. When the battery is being discharged, i_L is negative, and Q_2 and D_1 alternately conduct. At the time a diode would conduct, it is possible for the gate driver to turn on its antiparallel MOSFET; the MOSFET then operates as a *synchronous rectifier* as described in Sect. 4.1.5. Although this is a dc–dc converter, it requires two-quadrant switches because the power can flow in either direction. Figure 4.15 illustrates realization of the current-bidirectional switches using MOSFETs having fast-recovery body diodes.

Converters performing battery charging and battery discharging functions now find significant application in portable electronic devices such as cell phones and laptop computers. When the battery is being charged, the converter controller implements algorithms that control the charging profile needed by the battery. While the battery is being discharged, the converter controller regulates the bus voltage.

4.1.3 Voltage-Bidirectional Two-Quadrant Switches

Another type of two-quadrant switch, having the voltage-bidirectional properties illustrated in Fig. 4.16, is sometimes required. In applications where the switches must block both positive and negative voltages, but conduct only positive current, an SPST switch can be constructed using a series-connected transistor and diode as in Fig. 4.17. When it is intended that the switch be in the off state, the controller turns the transistor off. The diode then blocks negative voltage, and the transistor blocks positive voltage. The series connection can block negative voltages up to the diode voltage rating, and positive voltages up to the transistor voltage rating. The silicon-controlled rectifier is another example of a voltage-bidirectional two-quadrant switch.

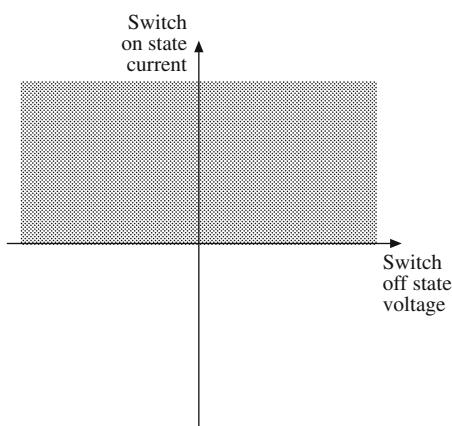


Fig. 4.16 Voltage-bidirectional two-quadrant switch properties

Fig. 4.17 A voltage-bidirectional two-quadrant SPST switch: (a) implementation using a transistor and series diode, (b) idealized switch characteristics

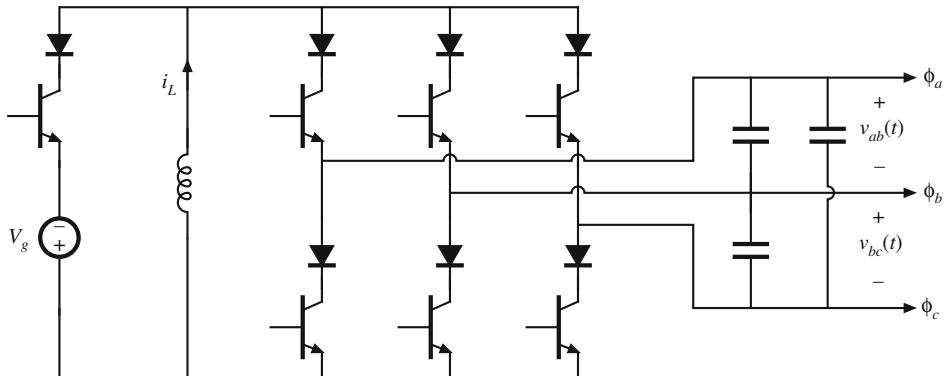
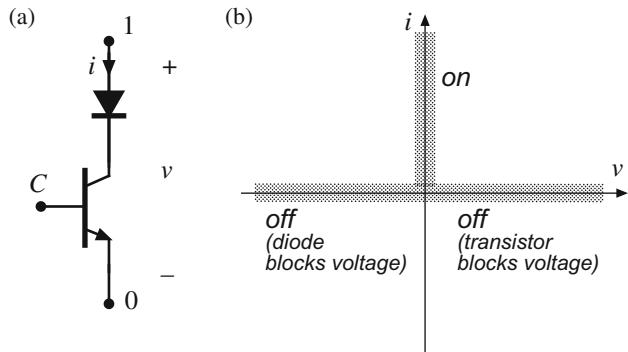


Fig. 4.18 Dc- 3ϕ buck-boost inverter

A converter that requires this type of two-quadrant switch is the dc- 3ϕ ac buck-boost inverter shown in Fig. 4.18 [22]. If the converter functions in inverter mode, so that the inductor current $i_L(t)$ is always positive, then all switches conduct only positive current. But the switches must block the output ac line-to-line voltages, which are sometimes positive and sometimes negative. Hence voltage-bidirectional two-quadrant switches are required.

4.1.4 Four-Quadrant Switches

The most general type of switch is the four-quadrant switch, capable of conducting currents of either polarity and blocking voltages of either polarity, as in Fig. 4.19. There are several ways of constructing a four-quadrant switch. As illustrated in Fig. 4.20b, two current-bidirectional two-quadrant switches described in Sect. 4.1.2 can be connected back-to-back. The transistors are driven on and off simultaneously. Another approach is the antiparallel connection of two voltage-bidirectional two-quadrant switches described in Sect. 4.1.3, as in Fig. 4.20a. A third approach, using only one transistor but additional diodes, is given in Fig. 4.20c.

Cycloconverters are a class of converters requiring four-quadrant switches. For example, a 3ϕ ac-to- 3ϕ ac matrix converter is illustrated in Fig. 4.21. Each of the nine SPST switches is realized using one of the semiconductor networks of Fig. 4.20. With proper control of the switches, this converter can produce a three-phase output of variable frequency and voltage, from a given three-phase ac input. Note that there are no dc signals in this converter: all of the input and output voltages and currents are ac, and hence four-quadrant switches are necessary.

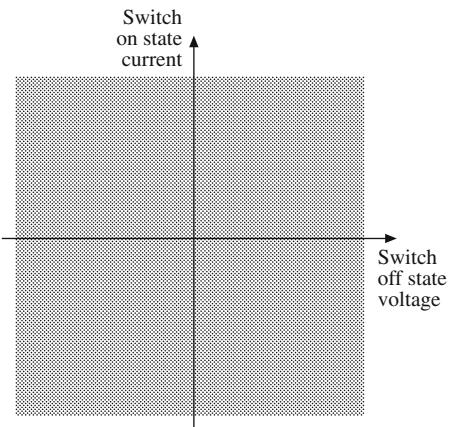


Fig. 4.19 A four-quadrant switch can conduct either polarity of current, and can block either polarity of voltage

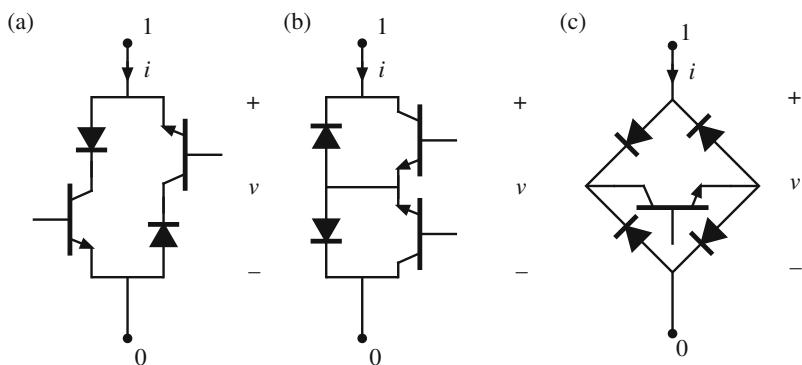


Fig. 4.20 Three ways of implementing a four-quadrant SPST switch

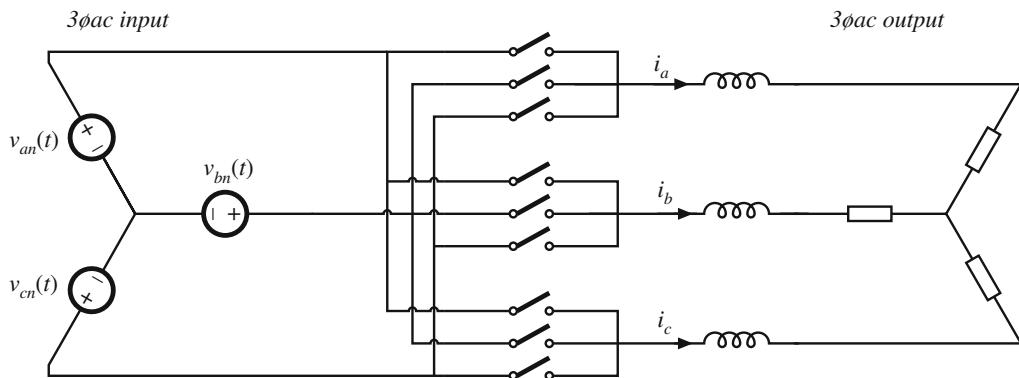


Fig. 4.21 A 3ϕ ac– 3ϕ ac matrix converter, which requires nine SPST four-quadrant switches

4.1.5 Synchronous Rectifiers

The ability of the MOSFET channel to conduct current in the reverse direction makes it possible to employ a MOSFET where a diode would otherwise be required. When the MOSFET is connected as in Fig. 4.22a [note that the source and drain connections are reversed from the connections of Fig. 4.6a], the characteristics of Fig. 4.22b are obtained. The device can now block negative voltage and conduct positive current, with properties similar to those of the diode in Fig. 4.4. The MOSFET must be controlled such that it operates in the on state when the diode would normally conduct, and in the off state when the diode would be reverse-biased.

Thus, we could replace the diode in the buck converter of Fig. 4.8 with a MOSFET, as in Fig. 4.23. The BJT has also been replaced with a MOSFET in the figure. MOSFET Q_2 is driven with the complement of the Q_1 control signal.

The trend in computer power supplies is reduction of output voltage levels, from 3.3 V to lower levels. As the output voltage is reduced, the diode conduction loss increases; in consequence, the diode conduction loss is easily the largest source of power loss in a sub-3.3 V power supply. Unfortunately, the diode junction contact potential limits what can be done to reduce the forward voltage drop of diodes. Schottky diodes having reduced junction potential can be employed; nonetheless, low-voltage power supplies containing diodes that conduct the output current must have low efficiency.

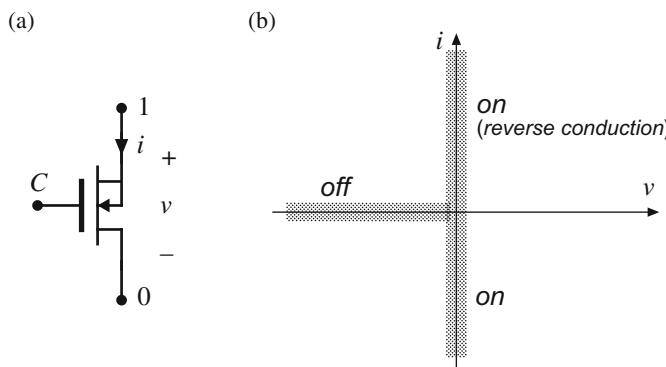


Fig. 4.22 Power MOSFET connected as a synchronous rectifier, (a), and its idealized switch characteristics, (b)

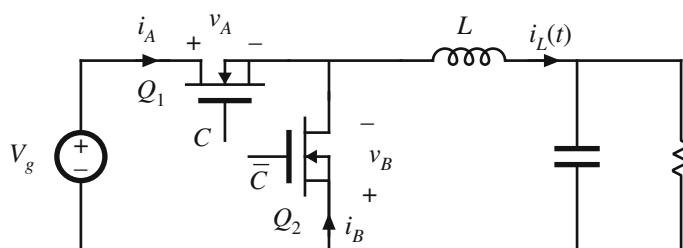


Fig. 4.23 Buck converter, implemented using a synchronous rectifier

A solution is to replace the diodes with MOSFETs operated as synchronous rectifiers. The conduction loss of a MOSFET having on-resistance R_{on} and operated with rms current is I_{rms} , is $I_{rms}^2 R_{on}$. The on-resistance can be decreased by use of a larger MOSFET. So the conduction loss can be reduced as low as desired, if one is willing to pay for a sufficiently large device. Synchronous rectifiers find widespread use in low-voltage power supplies.

The half-bridge MOSFET switches of Fig. 4.23 are also called *synchronous switches* and this buck converter is often called a *synchronous buck converter*. Most often, the synchronous rectifier Q_2 is driven with the complement of the gate drive signal that controls the main MOSFET Q_1 . Further details regarding gate drivers of synchronous buck converters are discussed in Sect. 4.4.3.

4.2 Introduction to Power Semiconductors

4.2.1 Breakdown Voltage, Forward Voltage, and Switching Speed

The most fundamental challenge in power semiconductor design is obtaining a high breakdown voltage, while maintaining low forward voltage drop and on-resistance [27, 28]. A closely related issue is the longer switching times of high-voltage low on-resistance devices; during these switching times, significant *switching loss* can be induced in the semiconductor devices. The tradeoff between breakdown voltage, on-resistance, and switching times is a key distinguishing feature of the various power devices.

The breakdown voltage of a reverse-biased $p-n$ junction and its associated depletion region is a function of doping level: obtaining a high breakdown voltage requires low doping concentration, and hence high resistivity, in the material on at least one side of the junction. This high-resistivity region is usually the dominant contributor to the on-resistance of the device, and hence high-voltage devices must have higher on-resistance than low-voltage devices. In *majority-carrier* devices, including the MOSFET and Schottky diode, this accounts for the first-order dependence of on-resistance on rated voltage. However, *minority-carrier* devices, including the diffused-junction $p-n$ diode, the bipolar junction transistor (BJT), the insulated-gate bipolar transistor (IGBT), and the thyristor family (SCR, GTO), exhibit another phenomenon known as *conductivity modulation*. When a minority-carrier device operates in the on state, minority carriers are injected into the lightly doped high-resistivity region by the forward-biased $p-n$ junction. The resulting high concentration of minority carriers effectively reduces the apparent resistivity of the region, reducing the on-resistance of the device. Hence, minority-carrier devices exhibit lower on-resistances than comparable majority-carrier devices.

However, the advantage of decreased on-resistance in minority-carrier devices comes with the disadvantage of decreased switching speed. The conducting state of any semiconductor device is controlled by the presence or absence of key charge quantities within the device, and the turn-on and turn-off switching times are equal to the times required to insert or remove this controlling charge. Devices operating with conductivity modulation are controlled by their injected minority carriers. The total amount of controlling minority charge in minority-carrier devices is much greater than the charge required to control an equivalent majority-carrier device. Although the mechanisms for inserting and removing the controlling charge of the various devices can differ, it is nonetheless true that, because of their large amounts of minority charge, minority-carrier devices exhibit switching times that are significantly longer than those

of majority-carrier devices. In consequence, majority-carrier devices find application at lower voltage levels and higher switching frequencies, while the reverse is true of minority-carrier devices.

The fundamental relationship between breakdown voltage, on-resistance, and switching speed, is a function of the energy *bandgap* of the semiconductor material. Electrons having low energy (in the *valence band*) are tightly bound to their atoms and do not participate in the conduction of electrical current. Electrons having sufficiently high energy (in the *conduction band*) are easily able to move from one atom to the next, and hence can participate in the conduction of current. The band gap of a semiconductor material is the energy difference between the highest energy state of the valence band and the lowest energy state of the conduction band. The bandgap of Silicon (Si) is approximately 1.1 eV.

Use of a *wide-bandgap* (WBG) semiconductor material can lead to a very significant improvement in this tradeoff between voltage breakdown, on-resistance, and switching time. Power diodes and transistors based on Silicon Carbide (SiC, bandgap approximately 3.2 eV) or Gallium Nitride (GaN, bandgap 3.4 eV) materials are now becoming commercially significant. These devices exhibit high-voltage characteristics that are superior to Silicon devices. Schottky diodes based on SiC technology are widely available at 600 to 1700 V, and can significantly improve converter efficiency relative to Si technology. Commercial power MOSFET devices based on SiC technology are available or have been announced at voltages of 600 V to 10 kV, and exhibit on-resistance and switching time far superior to what can be achieved with Si. Power transistors based on GaN technology are also available at voltages up to 650 V; these also exhibit significantly better switching time and on-resistance.

A detailed description of power semiconductor device physics and switching mechanisms is beyond the scope of this book. Selected references on power semiconductor devices are listed in the reference section [8, 11, 26, 28–40]. Rather, this and the following sections discuss the origins of switching times and forward voltage drop in power semiconductor devices at a high level. The averaged models of Chap. 3 are then extended to include switching losses. How the different types of power semiconductor switches address the tradeoff between forward voltage drop and switching speed is also considered.

4.2.2 Transistor Switching Loss with Clamped Inductive Load

The nonzero switching times of practical semiconductor devices lead to power loss during the switching transitions. This loss, called *switching loss*, can significantly reduce the efficiency of a switching converter. Multiple physical mechanisms induce switching loss; the most significant are discussed throughout this chapter.

Consider first the switching waveforms in the buck converter of Fig. 4.24. Let us treat the diode as ideal, and investigate only the switching loss due to the transistor switching times. Semiconductor output capacitances, transformer leakage inductances, diode reverse recovery, and other sources of switching loss are neglected in this first example. A MOSFET is illustrated in Fig. 4.24, but the introductory arguments of this section could apply to any power transistor.

The diode and inductor present a *clamped inductive load* to the transistor. With such a load, the transistor voltage $v_A(t)$ and current $i_A(t)$ do not change simultaneously. For example, a magnified view of the transistor turn-off-transition waveforms is given in Fig. 4.25. For simplicity, the waveforms are approximated as piecewise linear. The switching times are short, such that the inductor current $i_L(t)$ is essentially constant during the entire switching transition $t_0 < t < t_2$.

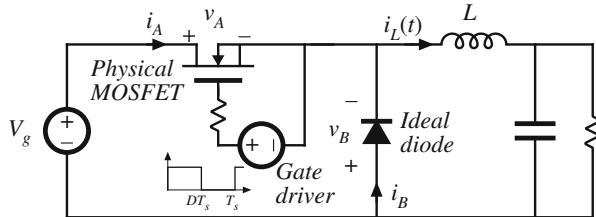


Fig. 4.24 MOSFET driving a clamped inductive load, buck converter example

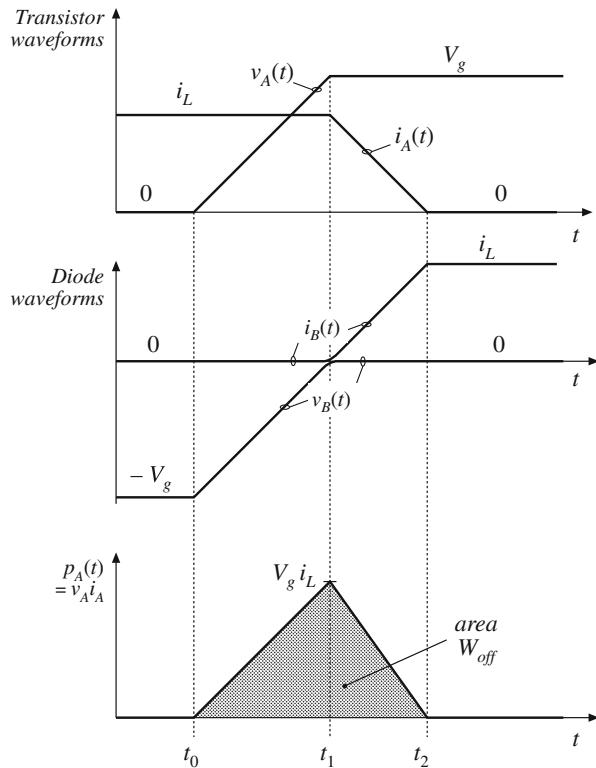


Fig. 4.25 Magnified view of transistor turn-off transition waveforms for the circuit of Fig. 4.24

No current flows through the diode while the diode is reverse-biased, and the diode cannot become forward-biased while its voltage $v_B(t)$ is negative. So first, the voltage $v_A(t)$ across the transistor must rise from zero to V_g . The interval length ($t_1 - t_0$) is essentially the time required for the gate driver to charge the MOSFET gate-to-drain capacitance. The transistor current $i_A(t)$ is constant and equal to i_L during this interval.

The diode voltage $v_B(t)$ and current $i_B(t)$ are given by

$$\begin{aligned} v_B(t) &= v_A(t) - V_g \\ i_A(t) + i_B(t) &= i_L \end{aligned} \quad (4.4)$$

At time $t = t_1$, when $v_A = V_g$, the diode becomes forward-biased. The current i_L now begins to commute from the transistor to the diode. The interval length $(t_2 - t_1)$ is the time required for the gate driver to discharge the MOSFET gate-to-source capacitance down to the threshold voltage which causes the MOSFET to be in the off state.

The instantaneous power $p_A(t)$ dissipated by the transistor is equal to $v_A(t)i_A(t)$. This quantity is also sketched in Fig. 4.25. The energy W_{off} lost during the transistor turn-off transition is the area under this waveform. With the simplifying assumption that the waveforms are piecewise-linear, then the energy lost is the area of the shaded triangle:

$$W_{off} = \frac{1}{2}V_g i_L(t_2 - t_1) \quad (4.5)$$

This is the energy lost during each transistor turn-off transition in the simplified circuit of Fig. 4.24. A transistor having shorter switching time $(t_2 - t_1)$ would be expected to exhibit lower energy lost during this switching transition.

The transistor turn-on waveforms of the simplified circuit of Fig. 4.24 are qualitatively similar to those of Fig. 4.25, with the time axis reversed. The transistor current must first rise from 0 to i_L . The diode then becomes reverse-biased, and the transistor voltage can fall from V_g to zero. The instantaneous transistor power dissipation again has peak value $V_g i_L$, and if the waveforms are piecewise linear, then the energy lost during the turn-on transition W_{on} is given by $0.5 V_g i_L$ multiplied by the transistor turn-on time.

Thus, during one complete switching period, the total energy lost during the turn-on and turn-off transitions is $(W_{on} + W_{off})$. If the switching frequency is f_s , then the average power loss incurred due to switching is

$$P_{sw} = \frac{1}{T_s} \int_{\text{switching transitions}} p_A(t)dt = (W_{on} + W_{off})f_s \quad (4.6)$$

So the switching loss P_{sw} is directly proportional to the switching frequency. This loss is also directly proportional to the energy losses W_{on} and W_{off} ; transistors having faster switching speeds are expected to exhibit lower switching loss.

The above arguments constitute a simplified and highly idealized view of switching loss. Unfortunately, often they are insufficient to explain the observed converter behavior related to switching loss; for example, they do not explain why zero-current switching of converters incorporating MOSFETs and diodes is inferior to zero-voltage switching (converters that employ these *soft-switching* phenomena are the subject of Chaps. 22 and 23). Hence, the sections that follow refine these arguments to account for the effects of diode reverse recovery, device output capacitances, and similar phenomena.

4.3 The Power Diode

4.3.1 Introduction to Power Diodes

A *p–n* diode is illustrated in Fig. 4.26. The right side of the *p–n* junction is doped with donor atoms that contribute weakly bound electrons to the semiconductor lattice, which can easily move from atom to atom. The left side of the junction is doped with acceptor atoms that create



Fig. 4.26 A *p-n* junction diode

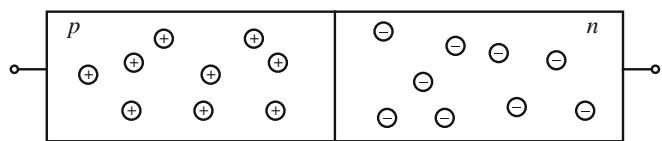
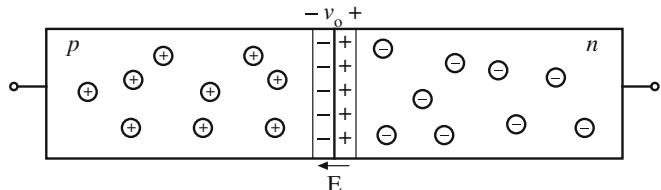


Fig. 4.27 Creation of depletion region at the *p-n* junction



holes, which can also easily move from atom to atom and effectively act as positive charge carriers. At the normal operating temperatures of the diode, these majority carriers exhibit thermally induced vibrations that cause them to move randomly around the semiconductor lattice.

At the *p-n* junction, a depletion region forms. This occurs because the thermally induced motion of the charge carriers causes them to diffuse in the direction of decreasing carrier concentration. As illustrated in Fig. 4.27, the concentration of mobile electrons is high on the right side of the junction, and low on the left side, and hence electrons diffuse to the left. These electrons become mobile minority carriers in the *p* region, having an energy state sufficient to continue to easily move from atom to atom within the semiconductor lattice. In a similar manner, holes diffuse into the *n* region, where they become minority carriers as well.

These mobile carriers leave behind ionized dopant atoms near the junction, causing an electric field to form. For example, when a majority-carrier electron from the *n* region diffuses into the *p* region, it leaves behind an ionized atom in the *n* region that is missing an electron and therefore has net positive charge. Likewise, when holes from the *p* region diffuse into the *n* region, they leave behind ionized atoms having net negative charge. This region of ionized atoms near the junction is called the *space-charge layer*, or *depletion region*. These ionized atoms within this region lead to an electric field E , with net voltage v_o , as illustrated in Fig. 4.27. The voltage v_o constitutes an energy barrier which tends to oppose the diffusion of the mobile carriers: it causes carriers to drift in the opposite direction. As more mobile carriers diffuse across the junction, the field continues to build. The device comes to equilibrium when the voltage and the electric field strength are large enough to counteract the net diffusion of mobile charges across the junction.

Figure 4.28 illustrates the situation in which an external voltage is applied that reverse-biases the *p-n* junction. This external voltage causes the further ionization of dopant atoms near the junction, and increases the size of the depletion region. Effectively, the applied voltage appears across the depletion region and the electric field within this region is increased. Increasing the reverse voltage requires that additional charge (from the external circuit) be added to the depletion region; this is a capacitive effect that leads to the *junction capacitance* of the diode.

Figure 4.29 illustrates the situation in which an external source forward-biases the *p-n* junction. This external source reduces the voltage across the *p-n* junction, such that the depletion

Fig. 4.28 The diode under reverse-bias conditions

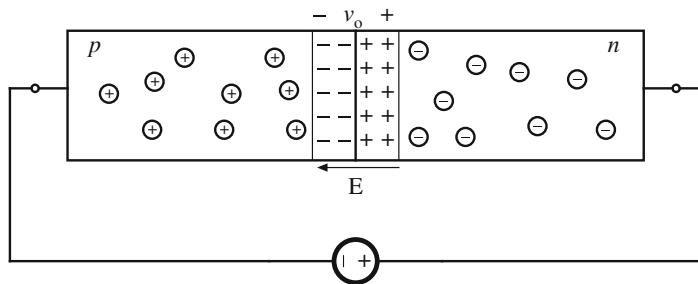


Fig. 4.29 The diode under forward-bias conditions

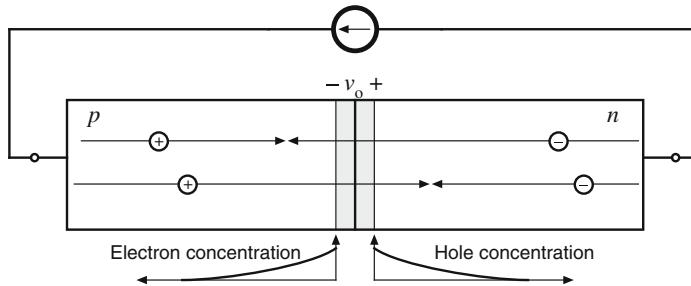
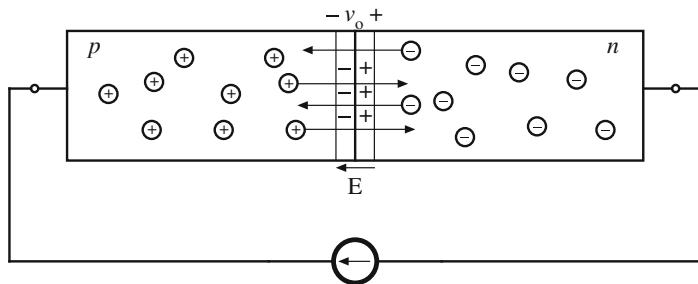


Fig. 4.30 Minority-carrier concentrations and recombination under forward-bias conditions

region electric field is not large enough to counteract diffusion of carriers across the junction. Under these forward-bias conditions, holes from the p -region diffuse across the junction, and become minority carriers in the n -region whose energy state is high enough to enable them to be mobile carriers. Similarly, electrons from the n -region diffuse across the junction and become mobile minority carriers in the p -region.

Figure 4.30 illustrates the mechanisms for conduction of current under forward-bias conditions. Electrons enter the n -region from the external circuit, through the contact at the right edge of the n -region. These electrons become majority carriers in the n -region. Likewise, electrons leave the p -region through the contact at the left side of the p -region, creating majority-carrier holes in the p -region. Some of these majority carriers diffuse across the forward-biased $p-n$ junction, and become minority carriers.

A number of processes cause minority carriers to lose their energy and *recombine* with majority carriers. This occurs at some rate, and therefore the minority carriers last for an effective *lifetime* τ_L before recombination. As the minority carriers diffuse away from the junction, their

concentration diminishes through recombination as illustrated in Fig. 4.30. The slope of this concentration curve determines the rate at which the minority carriers diffuse.

Under forward-bias conditions, the forward current consists entirely of recombination. A majority carrier from the external circuit enters the semiconductor at one of the contacts. This majority carrier may recombine with a minority carrier. Alternatively, it may diffuse across the junction, become a minority carrier, and then recombine.

Under forward-bias conditions, the diode is *charge controlled*. It can be shown that the voltage v across the depletion region is related to the minority charge concentrations p_s and n_s at the edge of the depletion region according to the diode equation (written below as a function of the hole concentration at the right edge of the depletion region of Fig. 4.30):

$$p_s(t) = Q_{s0} \left(e^{\lambda v(t)} - 1 \right) \quad (4.7)$$

The quantity λ is kT/q_e where k is Boltzmann's constant, T is the Kelvin temperature, and q_e is the charge of the electron. This equation states that greater forward-bias leads to greater minority charge injected across the junction. It also implies that the junction voltage cannot be decreased unless the minority charge at the edge of the depletion region is decreased.

We can model the switching behavior using a lumped-element model of the minority charge. In the simplest single-lump model, we let $q(t)$ be equal to the total minority charge on one side of the junction. This charge can reduce by recombination, and it can increase through application of positive terminal current $i(t)$. Hence we can write

$$\frac{dq(t)}{dt} = i(t) - \frac{q(t)}{\tau_L} \quad (4.8)$$

In this equation, q/τ_L is the rate at which the minority carriers recombine. In equilibrium, the total stored minority charge $q(t)$ is related to the charge concentration $p_s(t)$ or $n_s(t)$ at the edge of the depletion region.

In equilibrium, the net stored minority charge does not change: $dq(t)/dt = 0$. Equations (4.7) and (4.8) then predict

$$i(t) = \frac{q(t)}{\tau_L} = \frac{Q_0}{\tau_L} \left(e^{\lambda v(t)} - 1 \right) = I_0 \left(e^{\lambda v(t)} - 1 \right) \quad (4.9)$$

This is the traditional exponential diode equation. It can be seen that this is an equilibrium expression, and it does not hold during transient conditions (*i.e.* during the diode switching times). In particular, during the diode turn-off switching transition, the voltage $v(t)$ is determined by the stored minority charge concentration according to Eq. (4.7). To reduce this voltage, the stored minority charge must be removed. During the turn-off switching transition, the current can deviate from Eq. (4.9); Eq. (4.8) predicts that negative current can actively reduce the stored minority charge.

Figure 4.31 illustrates typical diode waveforms and stored minority charge concentration profiles during the turn-off transient. Initially (for $t \leq t_0$), the diode is in the on state, with a forward voltage $v(t_0) > 0$ and conducting current $i(t_0) = I_{on}$. The depletion region extends some distance x_0 from the $p-n$ junction; the shaded region illustrated in Fig. 4.31b denotes the depletion region at $t = t_0$. For $x > x_0$, there is a distribution of stored minority charge as illustrated in Fig. 4.31b for $t = t_0$. The slope of this minority charge curve is proportional to the rate at which the minority carriers diffuse; this slope at $x = x_0$ is proportional to I_{on} .

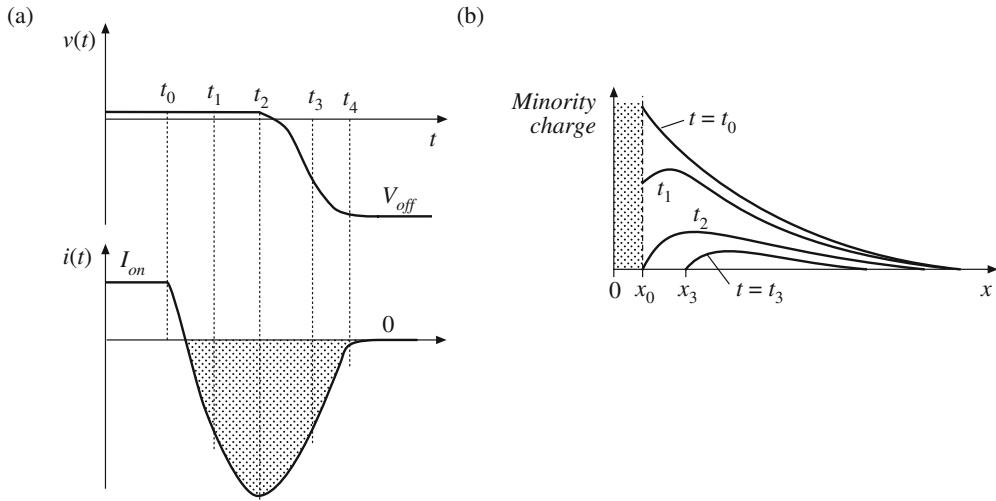


Fig. 4.31 The diode reverse-recovery process: (a) waveforms of diode voltage v and diode current i ; (b) minority charge concentration on one side of the $p-n$ junction

At time $t = t_0$, the external circuit begins to reverse the direction of the applied current $i(t)$. The rate di/dt at which the current changes is determined by the external circuit, and typically is limited by wiring and package inductances, transistor driver circuitry, etc.

The current has become negative at time $t = t_1$. The total stored charge, which is the area under the minority charge concentration curve of Fig. 4.31b, has been reduced by both negative current and by recombination according to Eq. 4.8. The slope of the charge concentration curve at the edge of the depletion region is negative, reflecting the reversal of current across the junction. Because of its polarity, the electric field within the depletion region does not oppose the flow of minority carriers in the reverse direction, and the current $i(t)$ now includes minority carriers flowing backwards across the depletion region. Since the minority charge concentration at $x = x_0$ is still substantial, Eq. (4.7) predicts that the voltage across the depletion region remains positive. Because of the exponential nature of the diode equation, the voltage $v(t)$ at $t = t_1$ is only slightly reduced from its initial value, and the diode remains forward-biased.

At time $t = t_2$, the stored minority charge at $x = x_0$ has been removed. Equation (4.7) now predicts that the voltage across the depletion region can become negative. However, stored minority charge remains for $x > x_0$, as illustrated in Fig. 4.31b. For $t > t_2$, this minority charge continues to be removed, while the voltage becomes more negative. At time $t = t_3$, the depletion region has increased in size, and extends to $x = x_3$ [not shown in Fig. 4.31b]. Finally, at time $t = t_4$, all of the minority stored charge has been removed. The diode now blocks the full reverse voltage V_{off} , with no substantial reverse current.

Let us consider the power consumption of the diode during the reverse-recovery process, as predicted by the waveforms of Fig. 4.31a. For $t < t_0$, the power flowing into the diode is

$$p(t) = v(t)i(t) = V_F I_{on} \quad (4.10)$$

where V_F is the forward voltage drop of the diode given by Eq. (4.9). This is the conduction loss of the diode. At time $t = t_1$, the current has reversed while the voltage remains positive;

the diode then supplies power (but in a typical converter, this power is lost elsewhere in the converter, usually in a transistor). For $t_2 < t < t_4$, both voltage and current are negative, and the diode again consumes power. In addition to the negative current arising from minority charge flowing across the depletion region, additional current is caused by charging the capacitance of the depletion region. This capacitive component of current does not constitute power loss within the diode. Nonetheless, the power lost at this time can be quite substantial, since both the voltage and current are large, and this component of power loss can lead to substantial switching loss within the diode. We will see soon that the total switching loss within the diode plus the associated switching transistor is substantial for the entire time from t_0 to t_4 .

The time extending from t_0 to t_4 is called the *reverse recovery time*, denoted t_r . The charge contained in the negative portion of the current $i(t)$ waveform is called the *recovered charge*, denoted Q_r . This charge consists of the stored minority charge that is actively removed through negative $i(t)$, as well as changes in the capacitive charge of the reverse-biased depletion region. The peak negative current at time $t = t_2$ can be substantial, and may be several times larger than the on-state current I_{on} , depending on the construction of the diode. This can cause significant instantaneous power dissipation during the reverse recovery, with significant magnitude of Q_r .

The magnitude of Q_r can be reduced if the switching time is slow; this then causes more of the stored minority charge to recombine rather than being actively removed through negative $i(t)$. If the slope di/dt for $t_0 < t < t_2$ is reduced, then Q_r is observed to be reduced as well.

The *softness factor* S is defined as

$$S = \frac{t_4 - t_2}{t_2 - t_0} \quad (4.11)$$

A diode whose turn-off transient is characterized by relatively large S is called a *soft recovery* diode; conversely, a diode having a small value of S is called a *snappy* diode. The reduced dv/dt of soft recovery diodes can aid in the turn-on process of the associated power transistor, and can also lead to reduced generation of electromagnetic interference. Semiconductor manufacturers are able to adjust S through device design.

Thus, the familiar exponential $i-v$ curve of the diode is an equilibrium relationship that can be violated during transient conditions. During the turn-on and turn-off switching transients, the current may deviate substantially from the equilibrium $i-v$ curve, because of changes in the stored minority charge and changes within the reverse-biased depletion region. The reverse recovery time t_r is the time required to remove the stored charge in the diode and enable it to block the full applied negative voltage. The area of the negative diode current during reverse recovery is the recovered charge Q_r .

4.3.2 Discussion: Power Diodes

As noted in Sect. 4.2, the diffused-junction $p-n$ power diode contains a lightly doped epitaxial or intrinsic high-resistivity region, which allows a high breakdown voltage to be obtained. This region is often called the *drift region*. As illustrated in Fig. 4.32a, this region comprises one side of the $p-n^-$ junction (denoted n^-); under reverse-biased conditions, essentially all of the applied voltage appears across the depletion region inside the n^- region. Figure 4.32a illustrates the off state of a *punch-through* design, in which the depletion region extends all of the way across the n^- region. The high electric field is supported without breakdown by the lightly doped n^- material.

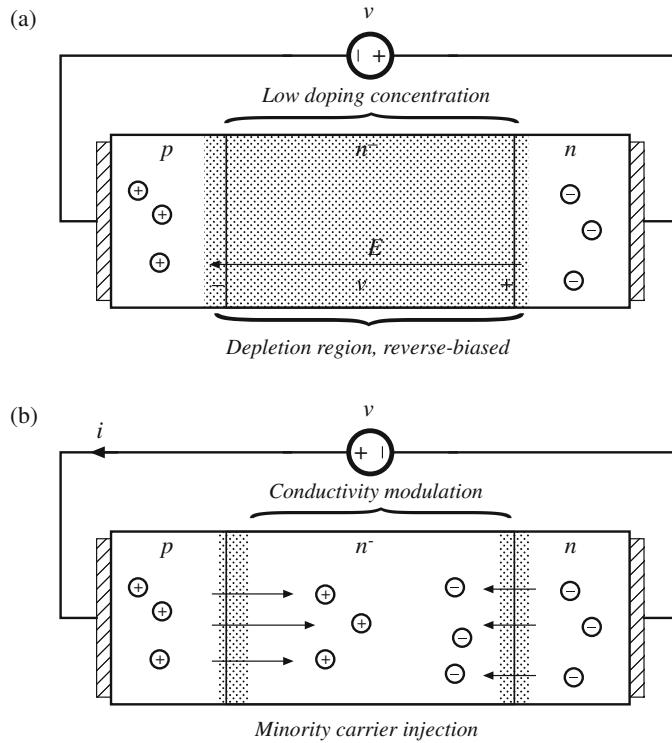


Fig. 4.32 Power diode: (a) under reverse-bias conditions, (b) under forward-bias conditions

On-state conditions are illustrated in Fig. 4.32b. Holes are injected across the forward-biased junction, and become minority carriers in the n⁻ region. In addition, electrons are injected across the forward-biased n⁻-n junction, which increases the concentration of electron carriers in the n⁻ region. These hole and electron carriers effectively reduce the apparent resistivity of the n⁻ region via conductivity modulation. Essentially all of the forward current $i(t)$ is comprised of recombination of minority carriers: either the recombination of holes and electrons within the n⁻ region, the recombination of minority holes with majority electrons within the n region, or the recombination of minority electrons with majority holes within the p region.

Diodes are rated according to the length of their reverse recovery time t_r . *Standard recovery* rectifiers are intended for 50 Hz or 60 Hz operation; reverse recovery times of these devices are usually not specified. *Fast recovery* rectifiers and *ultrafast recovery* rectifiers are intended for use in converter applications. The reverse recovery time t_r , and sometimes also the recovered charge Q_r , are specified by manufacturers of these devices. Ratings of several commercial devices are listed in Table 4.1.

Schottky diodes are essentially majority-carrier devices whose operation is based on the rectifying characteristic of a metal-semiconductor junction. These devices exhibit negligible minority stored charge, and their switching behavior can be adequately modeled simply by their depletion region capacitance and equilibrium exponential i-v characteristic. Hence, an advantage of the Schottky diode is its fast switching speed. An even more important advantage

Table 4.1 Characteristics of several commercial power rectifier diodes

Part number	Rated maximum voltage	Rated average current	V_F (typical)	t_r (max)
Fast recovery rectifiers				
IN3913	400 V	30 A	1.1 V	400 ns
SD453N2S20PC	2500 V	400 A	2.2 V	3 μ s
Ultrafast recovery rectifiers				
MUR815	150 V	8 A	0.975 V	35 ns
RHRD660	600 V	6 A	1.7 V	35 ns
RHRU100120	1200 V	100 A	2.6 V	60 ns
Schottky rectifiers				
MBR6030L	30 V	60 A	0.48 V	
444CNQ045	45 V	440 A	0.69 V	
30CPQ150	150 V	30 A	1.19 V	
SiC Schottky rectifiers				
C4D10120E	1200 V	10 A	1.8 V	
C3D3060F	600 V	3 A	1.7 V	

of Schottky diodes is their low forward voltage drops, especially in devices rated 45 V or less. Silicon Schottky diodes are restricted to low breakdown voltages; very few commercial devices are rated to block 100 V or more. Their off-state reverse currents are considerably higher than those of $p-n$ junction diodes. Characteristics of several commercial Schottky rectifiers are also listed in Table 4.1.

Wide-bandgap semiconductor materials have recently become commercially significant. Silicon carbide (SiC) and, more recently, gallium nitride (GaN) materials exhibit an improved tradeoff between blocking voltage, on-resistance, and switching speed. Schottky barrier diodes based on SiC are available with 600 V and 1200 V ratings; these exhibit much faster switching speeds and much lower Q_r than comparable silicon $p-n$ devices. Although the built-in diode drop is larger, the switching loss is much smaller; hence, overall efficiency improvements are observed. Because of the difficulties in producing high-quality compound semiconductor material, wide-bandgap power devices are more expensive than traditional silicon devices.

Another important characteristic of a power semiconductor device is whether its on-resistance and forward voltage drop exhibit a positive temperature coefficient. Such devices, including the MOSFET and IGBT, are advantageous because multiple chips can be easily paralleled, to obtain high-current modules. These devices also tend to be more rugged and less susceptible to hot-spot formation and second-breakdown problems. Diodes cannot be easily connected in parallel, because of their negative temperature coefficients: an imbalance in device characteristics may cause one diode to conduct more current than the others. This diode becomes hotter, which causes it to conduct even more of the total current. In consequence, the current does not divide evenly between the paralleled devices, and the current rating of one of the devices may be exceeded. Since BJTs and thyristors are controlled by a diode junction, these devices also exhibit negative temperature coefficients and have similar problems when operated in parallel. Of course, it is possible to parallel any type of semiconductor device; however, use of matched devices, a common thermal substrate, and/or external circuitry may be required to cause the on-state currents of the devices to be equal.

4.3.3 Modeling Diode-Induced Switching Loss

Diode-induced switching loss is often one of the largest sources of power loss in a PWM switching converter. In this section, the equivalent circuit models of Chap. 3 are extended to include the switching loss induced by the diode reverse-recovery process. The diode reverse recovery time t_r and recovered charge Q_r are included in the transistor and diode waveforms, and then these waveforms are related to the inductor and capacitor waveforms. The principles of inductor volt-second balance and capacitor charge balance are applied, along with the other techniques of Chap. 3. Equivalent circuits are then constructed, which include the effects of diode-induced switching loss, that can be employed to predict efficiency and dc components of the converter waveforms.

The discussion of this section employs the buck converter example illustrated in Fig. 4.33. An ideal MOSFET is assumed, which is driven by a control signal $c(t)$ having a duty cycle D_c . The diode is taken to be a $p-n$ diode having reverse recovery time t_r and recovered charge Q_r . Other nonidealities are neglected in this example, including conduction losses, switching ripple, etc.

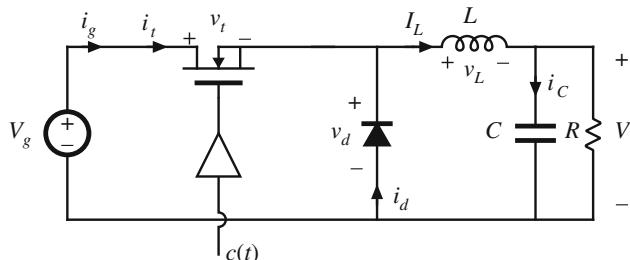


Fig. 4.33 Buck converter example: modeling switching loss

The assumed transistor and diode waveforms are illustrated in Fig. 4.34. In these idealized waveforms, the diode softness factor is taken to be $S = 0$. The switching ripple in the inductor current and capacitor voltage are assumed to be small. Additionally, the power stage duty cycle D is defined according to the transistor voltage waveform $v_t(t)$: the transistor voltage is zero for the interval $0 \leq t \leq DT_s$. This definition causes the inductor volt-second balance equation to coincide with the results for the ideal case, and leads to an equivalent circuit having a dc transformer with turns ratio $1 : D$.

It can be noted that the diode reverse recovery time t_r distorts the duty cycle, and causes the effective power stage duty cycle D to be smaller than the duty cycle D_c produced by the control circuit:

$$D = D_c - \frac{t_r}{T_s} \quad (4.12)$$

Switching times, as well as phenomena such as gate driver delays, can create some ambiguity in determination of the duty cycle. In this discussion, the power stage duty cycle D is defined according to the transistor voltage waveform.

We can relate these waveforms to the inductor voltage, capacitor current, and converter input current. The inductor voltage $v_L(t)$ is related to the diode voltage $v_d(t)$ as follows:

$$v_L(t) = v_d(t) - V \quad (4.13)$$

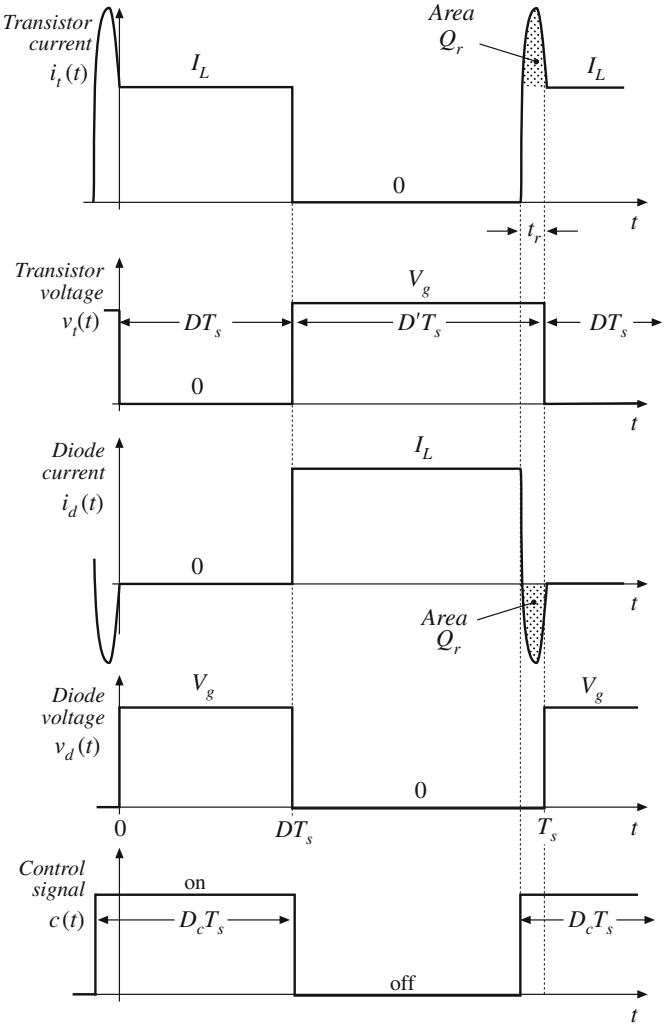
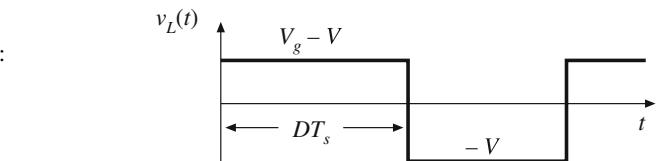


Fig. 4.34 Assumed waveforms for the buck converter with diode reverse recovery, Fig. 4.33



Subtraction of the output voltage V from the diode voltage waveform $v_d(t)$ illustrated in Fig. 4.34 leads to the inductor voltage waveform of Fig. 4.35. It can be seen that, with the definition of D as in Eq. (4.12), we obtain the usual inductor voltage waveform. Application of inductor volt-second balance to this waveform leads to

$$\langle v_L \rangle = 0 = DV_g - V \quad (4.14)$$

The capacitor current $i_C(t)$ is related to the inductor and load currents in the usual manner. Capacitor charge balance leads to

$$\langle i_C \rangle = 0 = I_L - \frac{V}{R} \quad (4.15)$$

Construction of an equivalent circuit corresponding to these two equations, according to the methods of Sect. 3.3, leads to the equivalent circuit of Fig. 4.36.

To complete the equivalent circuit model of the buck converter, an equation for the average input current I_g must be derived, as discussed in Sect. 3.4. It can be seen from Fig. 4.33 that the input current $i_g(t)$ coincides with the transistor current $i_t(t)$. The transistor current waveform is sketched in Fig. 4.34; its average is

$$I_g = \langle i_t(t) \rangle = \frac{1}{T_s} \int_0^{T_s} i_t(t) dt \quad (4.16)$$

$$= \frac{1}{T_s} (DT_s I_L + t_r I_L + Q_r) \quad (4.17)$$

$$= DI_L + \frac{t_r}{T_s} I_L + \frac{Q_r}{T_s} \quad (4.18)$$

Fig. 4.36 Buck converter example: equivalent circuit corresponding to Eqs. (4.14) and (4.15)

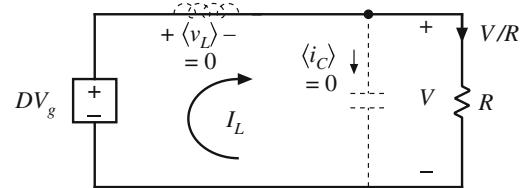
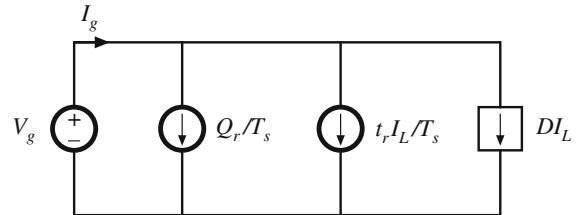


Fig. 4.37 Buck converter example: equivalent circuit corresponding to Eq. (4.18)



Equation (4.18) can be viewed as a node equation describing the dc current drawn out of the source V_g . The corresponding equivalent circuit is constructed in Fig. 4.37.

A complete model of the buck converter with switching loss can now be obtained by combining Figs. 4.36 and 4.37 to obtain Fig. 4.38. The dependent sources are combined into a $1 : D$ dc transformer. In addition, the model includes two current sources that model the dc components of input current that are induced by the diode recovered charge Q_r and reverse recovery time t_r .

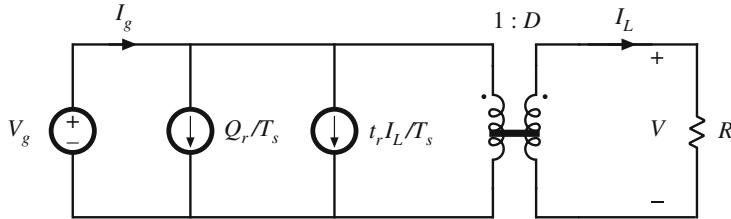


Fig. 4.38 Complete model of the buck converter with diode-induced switching loss

In the model of Fig. 4.38, the current sources consume power equal to

$$P_{sw} = V_g \left(\frac{Q_r}{T_s} + I_L \frac{t_r}{T_s} \right) \quad (4.19)$$

This is the switching loss induced by the diode reverse-recovery process. For the case \$S = 0\$, this power is dissipated in the transistor. For \$S > 0\$, this switching loss is dissipated partly in the diode and partly in the transistor.

We can now solve the model of Fig. 4.38, to derive expressions for the conversion ratio and efficiency. The conversion ratio \$M\$ is equal to the turns ratio of the dc transformer:

$$M = \frac{V}{V_g} = D \quad (4.20)$$

The output power is

$$P_{out} = VI_L \quad (4.21)$$

The input power is

$$P_{in} = V_g \left(DI_L + \frac{Q_r}{T_s} + I_L \frac{t_r}{T_s} \right) \quad (4.22)$$

The following equation for efficiency can be derived by taking the ratio of Eqs. (4.21) and (4.22), and simplifying:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{1}{1 + f_s \left(\frac{t_r}{D} + \frac{Q_r R}{D^2 V_g} \right)} \quad (4.23)$$

It can be seen that the efficiency is dependent on the switching frequency.

Equation (4.23) is plotted in Fig. 4.39, for the values \$V_g = 24\$ V, \$f_s = 100\$ kHz, \$R = 15\$ \$\Omega\$, \$Q_r = 0.75\$ \$\mu\$coul, \$t_r = 75\$ nsec. It can be seen that the switching loss causes the efficiency to tend to zero at low duty cycle. This occurs because the output power goes to zero but switching loss remains. This model assumes that the switching ripple is negligible, and no attempt has been made to model how \$Q_r\$ and \$t_r\$ vary with current; in practice these quantities do vary with current, but somewhat weakly. It is found experimentally that switching loss does indeed cause the efficiency of constant-frequency converters to degrade substantially as the output power is reduced.

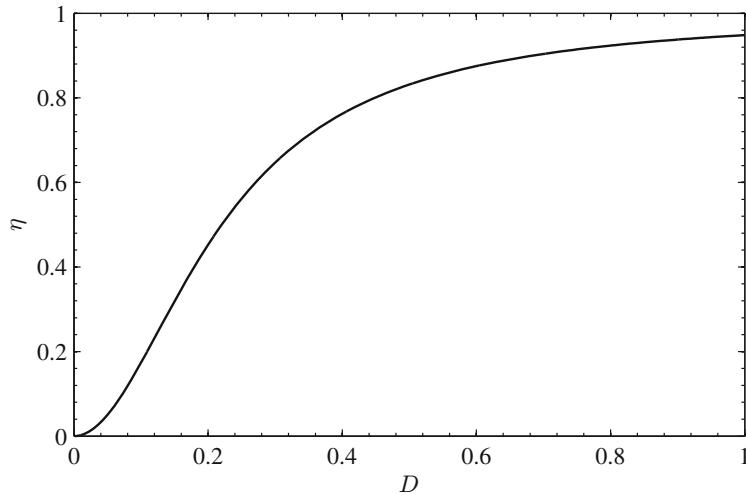


Fig. 4.39 Buck converter efficiency predicted by Eq. (4.23)

4.3.4 Boost Converter Example

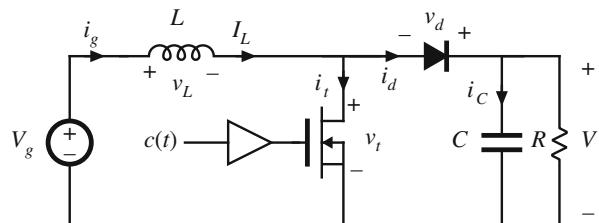
As another example of modeling switching loss, the boost converter of Fig. 4.40 is considered. Again, the switching loss induced by the diode reverse recovery is considered, including the effects of reverse recovery time t_r and recovered charge Q_r . Additionally, the loss induced by the inductor dc winding resistance R_L is modeled, but all other sources of loss are neglected. Also, the inductor current and capacitor voltage ripples are taken to be small.

The transistor and diode waveforms are sketched in Fig. 4.41; these are similar to the buck waveforms of Fig. 4.34 with the exception of the voltage amplitudes. Again, the converter power stage duty cycle D is defined with respect to the transistor voltage waveform $v_t(t)$; this duty cycle differs from the duty cycle D_c of the controller gate drive signal $c(t)$ because of the diode reverse recovery time t_r . We will see that this definition leads to an equivalent circuit having a dc transformer with turns ratio $D' : 1$.

To apply the principle of inductor volt-second balance, we first construct the waveform of $v_L(t)$. In the boost converter, the inductor voltage $v_L(t)$ is related to the transistor voltage $v_t(t)$ and inductor current $i_L(t)$ according to

$$v_L(t) = V_g - i_L(t)R_L - v_t(t) \quad (4.24)$$

Fig. 4.40 Boost converter example: modeling switching loss



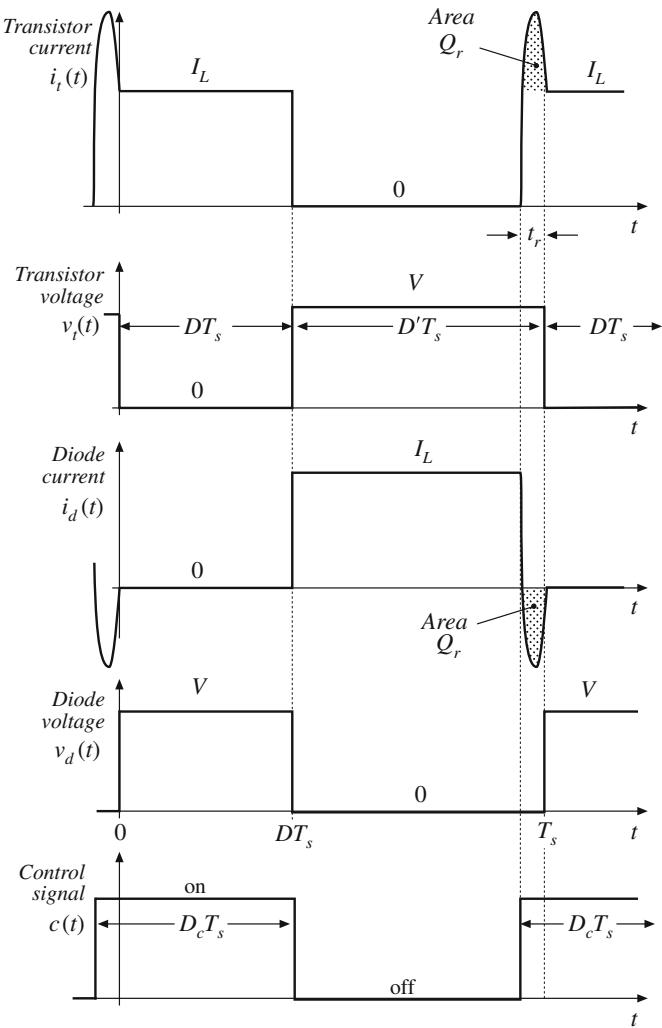
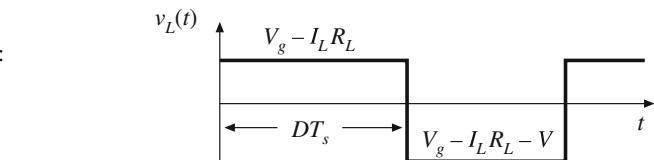


Fig. 4.41 Assumed waveforms for the boost converter with diode reverse recovery, Fig. 4.40



By subtraction of the transistor voltage waveform of Fig. 4.41 from V_g , and with use of the small-ripple approximation, the inductor voltage waveform of Fig. 4.42 is obtained. The dc component of this waveform is

$$\begin{aligned} \langle v_L \rangle &= 0 = D(V_g - I_L R_L) - D'(V_g - I_L R_L - V) \\ &= V_g - I_L R_L - D'V \end{aligned} \quad (4.25)$$

In the boost converter, the capacitor current i_C is related to the diode current i_d and load current v/R according to the output node equation

$$i_C = i_d - \frac{v}{R} \quad (4.26)$$

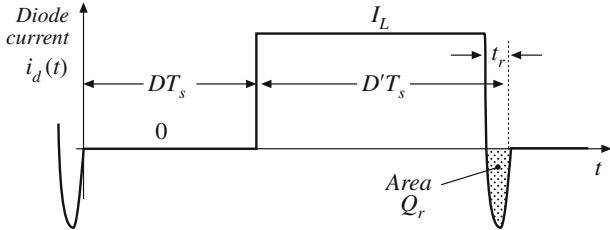
By capacitor charge balance, the average value of the capacitor current is zero. We can therefore use Eq. (4.26) to write

$$\langle i_C \rangle = 0 = \langle i_d \rangle - \frac{V}{R} \quad (4.27)$$

The dc component of the diode current is found by integration of the waveform of Fig. 4.43:

$$\begin{aligned} \langle i_d \rangle &= \frac{1}{T_s} \int_0^{T_s} i_d(\tau) d\tau \\ &= \frac{1}{T_s} (I_L(D'T_s - t_r) - Q_r) \\ &= D'I_L - \frac{t_r I_L}{T_s} - \frac{Q_r}{T_s} \end{aligned} \quad (4.28)$$

Fig. 4.43 Boost converter example: diode current waveform



By convention in these equations, the recovered charge Q_r is taken to be a positive quantity. Hence, the output node equation (4.27) becomes

$$0 = D'I_L - \frac{t_r I_L}{T_s} - \frac{Q_r}{T_s} - \frac{V}{R} \quad (4.29)$$

Finally, we note that the input current $i_g(t)$ coincides with the inductor current $i_L(t)$, and hence the dc component of input current is

$$I_g = I_L \quad (4.30)$$

Hence, the equations that describe the dc model of this converter are

$$\begin{aligned} 0 &= V_g - I_L R_L - D'V \\ 0 &= D'I_L - \frac{t_r I_L}{T_s} - \frac{Q_r}{T_s} - \frac{V}{R} \\ I_g &= I_L \end{aligned} \quad (4.31)$$

These equations follow from Eqs. (4.25), (4.29), and (4.30). An equivalent circuit corresponding to Eqs. (4.31) is given in Fig. 4.44. This dc circuit model accounts for diode-induced switching loss and for inductor dc winding resistance in the boost converter; other conduction losses could have been included as well, following the approach of Chap. 3.

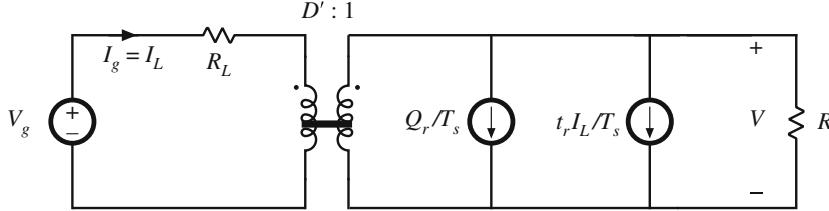


Fig. 4.44 Complete model of the boost converter with diode-induced switching loss

The two independent sources of Fig. 4.44 consume power

$$P_{sw} = V \left(\frac{t_r I_L}{T_s} + \frac{Q_r}{T_s} \right) \quad (4.32)$$

This power is equal to the switching loss within the MOSFET and diode induced by diode reverse recovery. In the model, these sources appear in parallel with the load and effectively behave as an additional load on the converter. Indeed, in the actual converter, the diode reverse recovery current flows out of the output filter capacitor C and through the semiconductor devices.

The model of Fig. 4.44 can now be solved, to find the conversion ratio $M = V/V_g$. The result can be shown to be

$$M = \frac{V}{V_g} = \left(\frac{1}{D'} \right) \frac{\left(1 - \frac{Q_r}{T_s} \frac{R_L}{D'V_g (1 - t_r/D'T_s)} \right)}{\left(1 + \frac{R_L}{D'^2 R (1 - t_r/D'T_s)} \right)} \quad (4.33)$$

This equation is plotted vs. duty cycle in Fig. 4.45, for the values $f_s = 100$ kHz, $V_g = 24$ V, $R = 15 \Omega$, $R_L = 0.15 \Omega$, $Q_r = 1 \mu\text{Coul}$, and $t_r = 50$ nsec. The conversion ratio with switching loss (thick, lower line) is compared to the result with inductor winding resistance only (thin, upper line). It can be seen that the two curves are qualitatively similar, and the effect of switching loss is more pronounced at high duty cycles.

We can also evaluate the equivalent circuit model of Fig. 4.44 to find the converter efficiency. The input power is given by

$$P_{in} = V_g I_g \quad (4.34)$$

The output power is equal to

$$P_{out} = V \left(D' I_g - \frac{Q_r}{T_s} - \frac{t_r I_L}{T_s} \right) \quad (4.35)$$

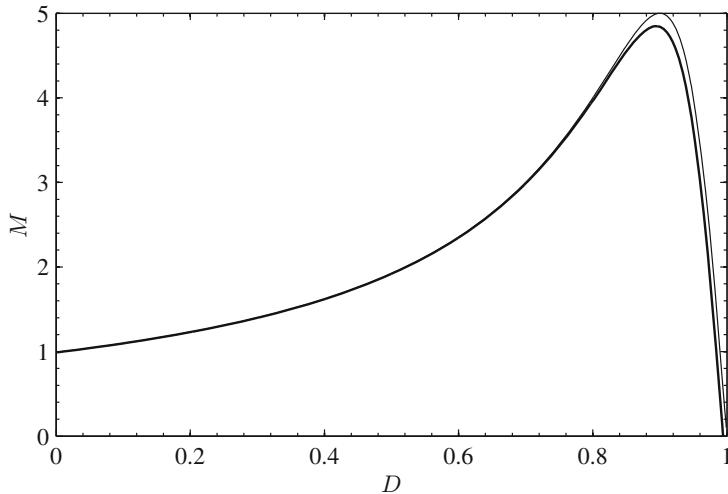


Fig. 4.45 Conversion ratio V/V_g , boost converter with switching loss and inductor dc winding resistance. The lower (thick) line includes switching loss terms and dc winding resistance. The upper (thin) line includes dc winding resistance only, with no switching loss

By taking the ratio of these two expressions and simplifying, we can show that the efficiency is given by

$$\eta = \frac{V}{V_g} \left(D' - \frac{Q_r}{T_s I_L} - \frac{t_r}{T_s} \right) \quad (4.36)$$

Additionally, the equivalent circuit model of Fig. 4.44 can be solved for the inductor current I_L , yielding

$$I_L = \frac{\left(\frac{V_g}{D'^2 R} + \frac{Q_r}{T_s D'} \right)}{\left(1 - \frac{t_r}{D' T_s} + \frac{R_L}{D'^2 R} \right)} \quad (4.37)$$

Equations (4.36) and (4.37) can be used to plot the converter efficiency. The result is shown in Fig. 4.46, for the same parameter values of Fig. 4.45. Again, the result with switching loss (lower thick line) and without switching loss but with inductor winding resistance only (upper, thin line) are compared. It can be seen that these values of diode reverse recovery time and diode recovered charge lead to substantial reductions in efficiency, even at low duty cycles where the diode reverse recovery causes negligible change in the conversion ratio V/V_g . The term multiplying $1/D'$ on the right-hand side of Eq. (4.33) is not equal to the efficiency, and instead simply accounts for how the loss elements affect the conversion ratio.

The plot of Fig. 4.46 predicts that the efficiency tends to a value slightly less than 93% as the duty cycle tends to zero. It should be noted that the boost converter can be operated in *passthrough mode* at $D = 0$, where the MOSFET is always off and never switches. In this case, there is no switching loss and the efficiency will jump to the upper curve that includes inductor dc copper loss only.

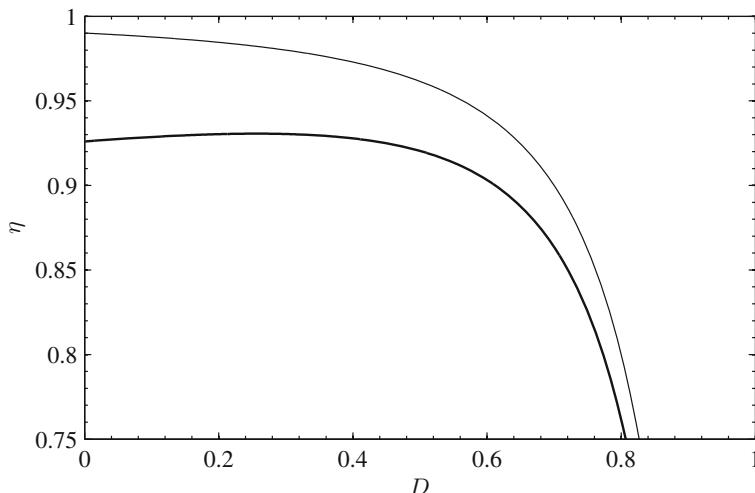


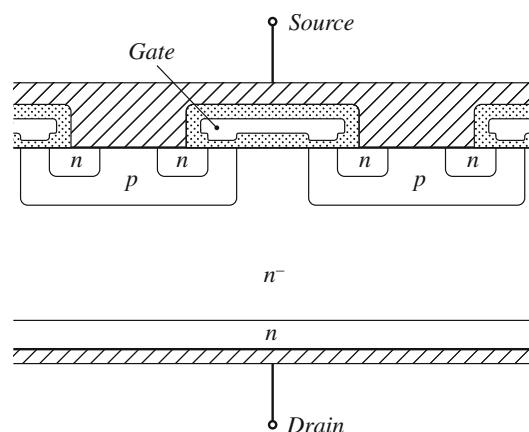
Fig. 4.46 Efficiency of the boost converter with diode-induced switching loss. The lower (thick) line includes switching loss terms and dc winding resistance. The upper (thin) line includes dc winding resistance only, with no switching loss

4.4 Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

4.4.1 Introduction to the Power MOSFET

The power MOSFET is a modern power semiconductor device having gate lengths close to one micron. The power device is comprised of many small parallel-connected enhancement-mode MOSFET cells, which cover the surface of the silicon die. A cross-section of one cell is illustrated in Fig. 4.47. Current flows vertically through the silicon wafer: the metallized drain connection is made on the bottom of the chip, while the metallized source connection and polysilicon gate are on the top surface. Under normal operating conditions, in which $v_{ds} \geq 0$, both the $p-n$ and $p-n^-$ junctions are reverse-biased. Figure 4.48a illustrates operation of the

Fig. 4.47 Cross-section of DMOS n -channel power MOSFET structure. Crosshatched regions are metallized contacts. Shaded regions are insulating silicon dioxide layers



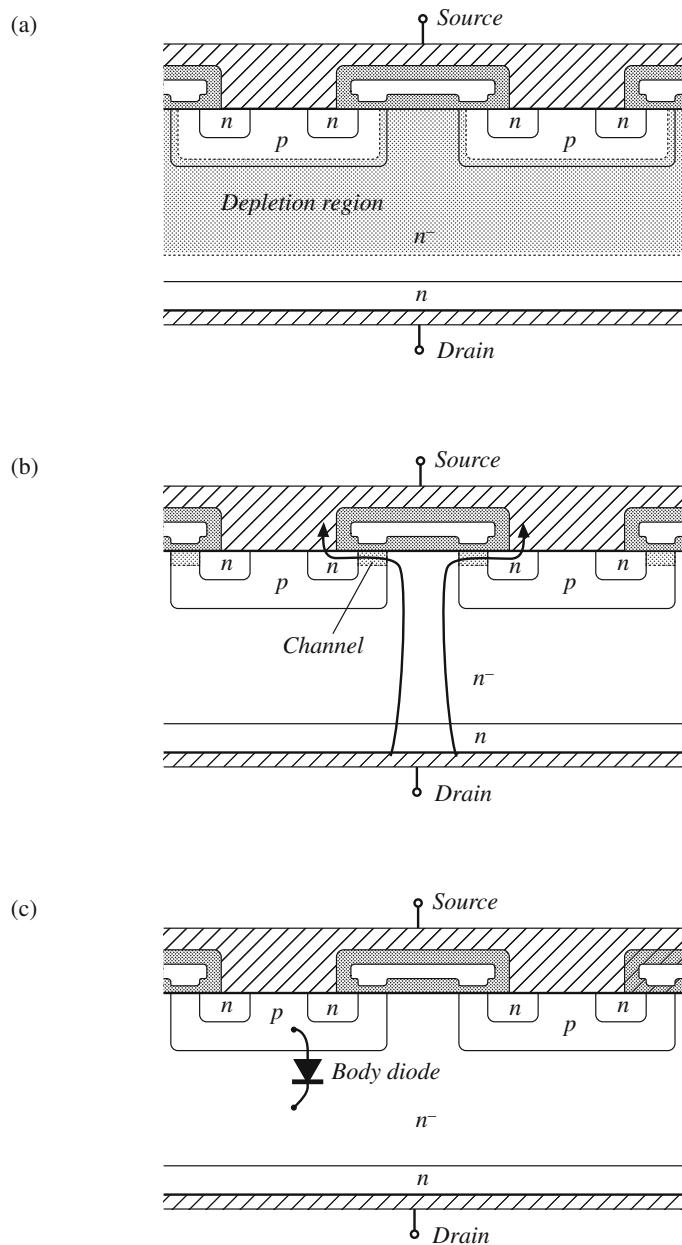


Fig. 4.48 Operation of the power MOSFET: (a) in the off state, v_{ds} across the depletion region in the n^- region; (b) current flow through the conducting channel in the on state; (c) body diode due to the $p - n^-$ junction

device in the off state. The applied drain-to-source voltage then appears across the depletion region of the $p-n^-$ junction. The n^- region is lightly doped, such that the desired breakdown voltage rating is attained. Figure 4.48b illustrates operation in the on state, with a sufficiently large positive gate-to-source voltage. A channel then forms at the surface of the p region, underneath the gate. This channel is called an *inversion region*, it contains mobile electrons that are able to conduct current between the drain and source. The drain current flows through the n^- drift region, channel, n region, and out through the source contact. The on-resistance of the device is the sum of the resistances of the n^- region, the channel, the source and drain contacts, etc. As the breakdown voltage is increased, the on-resistance becomes dominated by the resistance of the n^- drift region. Since there are no minority carriers to cause conductivity modulation, the on-resistance increases rapidly as the breakdown voltage is increased to several hundred volts and beyond.

The $p-n^-$ junction is called the *body diode*; as illustrated in Fig. 4.48c, this junction forms an effective diode in parallel with the MOSFET channel. The body diode can become forward-biased when the drain-to-source voltage $v_{ds}(t)$ is negative. This diode is capable of conducting the full rated current of the MOSFET. However, many MOSFETs are not optimized with respect to the speed of their body diodes, and the large peak currents that flow during the reverse recovery transition of the body diode can cause device failure as described below. Most recent MOSFETs contain fast recovery body diodes; these devices are rated to withstand the peak currents during the body diode reverse recovery transition.

The MOSFET structure of Fig. 4.48 also includes a *parasitic BJT* structure, formed by the source n region (emitter), substrate p region (base), and drift n^- region (collector). Since the n and p regions are shorted by the source contact, this parasitic BJT is normally off. However, if a sufficiently large current flows through the bulk resistance of the p region, it is possible to forward-bias the $p-n$ base-emitter junction. This situation may be observed during the reverse recovery transition of the body diode, and it can lead to latchup and failure of the MOSFET. Recent MOSFET designs are less prone to this failure mechanism.

Typical n -channel MOSFET static switch characteristics are illustrated in Fig. 4.49. The drain current is plotted as a function of the gate-to-source voltage, for various values of drain-to-source voltage. When the gate-to-source voltage is less than the threshold voltage V_{th} , the device operates in the off state. A typical value of V_{th} is 3 V. When the gate-to-source voltage is greater than 6 or 7 V, the device operates in the on state; typically, the gate is driven to 12 or 15 V to ensure minimization of the forward voltage drop. In the on state, the drain-to-source voltage V_{DS} is roughly proportional to the drain current I_D . The MOSFET is able to conduct peak currents well in excess of its average current rating, and the nature of the static characteristics is unchanged at high current levels. Logic-level power MOSFETs are also available, which operate in the on state with a gate-to-source voltage of 5 V. Some p -channel devices can be obtained, but their properties are inferior to those of equivalent n -channel devices.

The on-resistance and forward voltage drop of the MOSFET have a positive temperature coefficient. This property makes it relatively easy to parallel devices. High-current MOSFET modules are available, containing several parallel-connect chips.

The major capacitances of the MOSFET are illustrated in Fig. 4.50. This model is sufficient for qualitative understanding of the MOSFET switching behavior; more accurate models account for the parasitic junction field-effect transistor inherent in the DMOS geometry. Switching times of the MOSFET are determined essentially by the times required for the gate driver to charge these capacitances. Since the drain current is a function of the gate-to-source voltage,

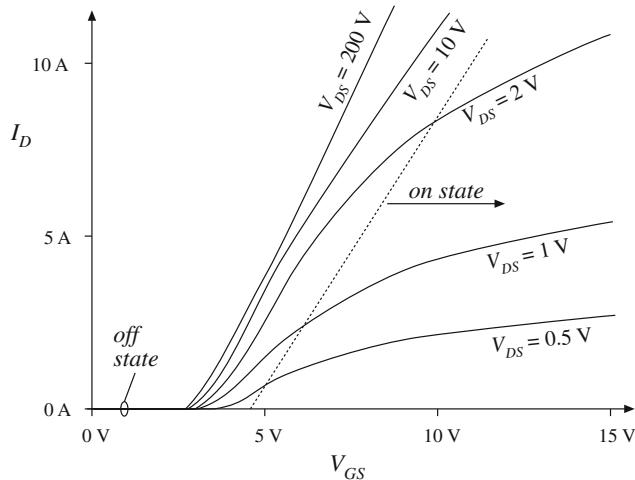
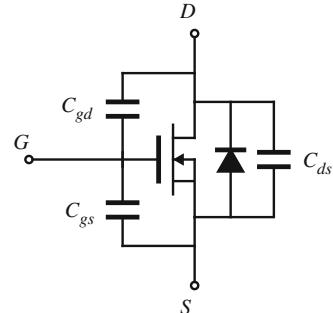


Fig. 4.49 Typical static characteristics of a power MOSFET. Drain current I_D is plotted vs. gate-to-source voltage V_{GS} , for various values of drain-to-source voltage V_{DS}

Fig. 4.50 MOSFET equivalent circuit which accounts for the body diode and effective terminal capacitances



the rate at which the drain current changes is dependent on the rate at which the gate-to-source capacitance is charged by the gate drive circuit. Likewise, the rate at which the drain voltage changes is a function of the rate at which the gate-to-drain capacitance is charged. The drain-to-source capacitance leads directly to switching loss in PWM converters, since the energy stored in this capacitance is lost during the transistor turn-on transition. Switching loss is discussed in Sect. 4.6.

The gate-to-source capacitance is essentially linear. However, the drain-to-source and gate-to-drain capacitances are strongly nonlinear: these incremental capacitances vary as the inverse square root of the applied capacitor voltage. For example, the dependence of the incremental drain-to-source capacitance can be written in the form

$$C_{ds}(v_{ds}) = \frac{C_0}{\sqrt{1 + \frac{v_{ds}}{V_0}}} \quad (4.38)$$

where C_0 and V_0 are constants that depend on the construction of the device. These capacitances can easily vary by several orders of magnitude as v_{ds} varies over its normal operating range. For $v_{ds} \gg V_0$, Eq. (4.38) can be approximated as

$$C_{ds}(v_{ds}) \approx C_0 \sqrt{\frac{V_0}{v_{ds}}} = \frac{c'_0}{\sqrt{v_{ds}}} \quad (4.39)$$

These expressions are used in Sect. 4.6.1 to determine the switching loss due to energy stored in C_{ds} .

Table 4.2 Characteristics of several commercial n -channel power MOSFETs

Part number	Rated maximum voltage	Rated average current	R_{on}	Q_g (typical)
SiSS64DN	30 V	40 A	2.1 mΩ	21 nC
CSD18512Q5B	40 V	100 A	1.3 mΩ	75 nC
NTMFS6H800N	80 V	203 A	1.8 mΩ	85 nC
IXFH80N25X3	250 V	80 A	13 mΩ	83 nC
IPL60R065P7	650 V	41 A	53 mΩ	67 nC

Characteristics of several commercially available power MOSFETs are listed in Table 4.2. The gate charge Q_g is the charge that the gate drive circuit must supply to the MOSFET to raise the gate voltage from zero to some specified value (typically 10 V), with a specified value of off-state drain-to-source voltage (typically 80% of the rated V_{DS}). The total gate charge is the sum of the charges on the gate-to-drain and the gate-to-source capacitance. The total gate charge is to some extent a measure of the size and switching speed of the MOSFET. A figure of merit is the product of on-resistance R_{on} and gate charge Q_g ; a device exhibiting lower $R_{on} Q_g$ is expected to operate with higher efficiency. The on-resistances listed in Table 4.2 are typical values specified at 25°C; the on-resistance increases significantly at elevated temperature.

Unlike other power devices, MOSFETs are usually not selected on the basis of their rated average current. Rather, on-resistance and its influence on conduction loss are the limiting factors, and MOSFETs typically operate at average currents somewhat less than the rated value.

Majority-carrier silicon MOSFETs are usually the device of choice at voltages up to approximately 600 V. At these voltages, the forward voltage drop is competitive or superior to the forward voltage drops of minority-carrier devices, and the switching speed is significantly faster. Typical switching times are below 100 ns. At voltages greater than 600 V, minority-carrier devices having lower forward voltage drops, such as the IGBT, usually have been preferred. These minority-carrier devices are discussed in Sect. 4.5.

The *superjunction* MOSFET [41] employs alternate heavily doped n and p layers within the drift region, to carefully control the electric field under off-state conditions. This enables better optimization of the tradeoff between on-resistance and blocking voltage, leading to significantly better on-resistance, capacitance, and die area in MOSFETs at voltages of 500–800 V. The IPL60R06SP7 device listed in Table 4.2 is an example of a superjunction MOSFET.

4.4.2 Wide-Bandgap FETs

Power transistors based on *wide-bandgap* (WBG) materials have recently emerged as commercially significant switching devices. In comparison with conventional silicon-based power

transistors, these wide-bandgap transistors can achieve higher breakdown voltage with lower on-resistance and faster switching times. Power MOSFETs based on Silicon Carbide (SiC) find application at voltages above 600 V, and FET devices based on Gallium Nitride (GaN) currently find application at voltages of 600 V and below.

For a majority-carrier device having no conductivity modulation, the resistance R_{on} of the drift region can be expressed as

$$AR_{on} = \frac{k}{\mu_n \epsilon_s E_c^3} V_B^2 \quad (4.40)$$

where R_{on} is the resistance of the drift region, A is the device area, k is a constant dependent on the process and other factors, μ_n is the electron mobility, ϵ_s is the semiconductor permittivity, E_c is the critical field for avalanche breakdown, and V_B is the device breakdown voltage. The right-hand side of Eq. (4.40) is known as the *specific on-resistance* of a power transistor technology, having units of transistor on-resistance per unit area. Wide-bandgap devices take advantage of this basic relationship to make significant advances in performance. These parameters are listed in Table 4.3 for selected semiconductor materials. The electron mobility listed for GaN material is for a high electron mobility transistor (HEMT), for the two-dimensional electron gas induced at the junction between AlGaN and GaN materials. Different crystalline structures are possible in these materials, which can lead to a range of values.

Table 4.3 Comparison of Power Semiconductor Materials [42]

Material	Bandgap [eV]	Electron mobility μ_n [cm ² /Vs]	Permittivity ϵ_s	Critical field E_c [V/cm]	Thermal conductivity [W/m°K]
Si	1.1	1350	11.8	$3 \cdot 10^5$	150
SiC (4H)	3.26	720	10	$2 \cdot 10^6$	450
GaN	3.44	1500–2000 (2DEG)	9	$3.3 \cdot 10^6$	130

The wide-bandgap energies of SiC and GaN materials lead to significant increases in the critical field E_c , approximately an order-of-magnitude improvement. Equation (4.40) predicts that an order-of-magnitude improvement in E_c leads to a three orders-of-magnitude improvement in on-resistance R_{on} . Hence, wide-bandgap materials can potentially achieve a major improvement in the relationship between on-resistance and breakdown voltage.

Additionally, a wide bandgap directly influences the impact on switching time because improvement in specific on-resistance allows a reduction in device area while maintaining the same on-resistance. Reduction in device area reduces its capacitance, and hence also switching loss. Further, wide-bandgap materials enable the use of majority-carrier devices in much higher voltage applications, with no current tail, no reverse recovery, and other advantages of majority-carrier device technology. Hence a technological improvement in Eq. (4.40) represents an improvement in a combination of on-resistance, switching time, and voltage breakdown.

Native oxide layers can be grown on SiC, and manufacturers have developed vertical power MOSFETs in SiC having structures similar to Fig. 4.47. The properties of several commercial SiC power MOSFETs are listed in Table 4.4. Relative to Si MOSFET technology, these SiC MOSFETs achieve significantly higher breakdown voltages, lower on-resistances, and lower gate charge. Silicon Carbide MOSFETs rated at 10 kV [43] and higher are feasible.

Table 4.4 Characteristics of several commercial SiC MOSFETs

Part number	Rated maximum voltage	Rated average current	R_{on}	Q_g (typical)
C3M0030090K	900 V	63 A	30 mΩ	87 nC
C3M0075120K	1200 V	30 A	75 mΩ	51 nC
C2M0045170D	1700 V	72 A	45 mΩ	188 nC
SCT3022AL	650 V	93 A	22 mΩ	133 nC
CPM3-0900-0010A	900 V	196 A	10 mΩ	68 nC

Table 4.3 notes that SiC exhibits significantly lower electron mobility than Si. Since on-resistance depends on mobility, low-voltage SiC MOSFETs exhibit inferior on-resistance in low-voltage devices. The advantage of wide bandgap in SiC causes SiC devices to be superior to Si devices only at rated voltages above 600 V. At lower rated voltages, SiC MOSFETs exhibits lower specific resistance than Si MOSFETs.

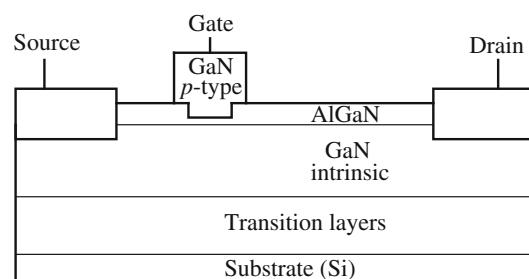
Silicon carbide exhibits high thermal conductivity and low thermal coefficient of expansion. Bulk devices are able to operate at very high temperatures, possibly up to 300°C. However, the packaging of these devices generally is limited to lower temperatures. Additionally, the reliability of oxide layers is compromised above 175°C, which limits the maximum temperatures of SiC MOSFETs.

The SiC MOSFET includes a body diode, as in Fig. 4.48c. The forward voltage drop of this SiC $p-n$ diode is 3–4 volts, and its reverse recovery time typically is several tens of nanoseconds. If reverse current conduction is required, the MOSFET can be turned on and operated as a synchronous rectifier, to reduce conduction loss.

As noted earlier, the SiC Schottky diode finds application as a replacement for high voltage Si $p-n$ diodes, at 600 V and above. The SiC MOSFET may find application as a replacement for the Si IGBT at 600 V and above, enabling higher switching frequencies and smaller reactive element size.

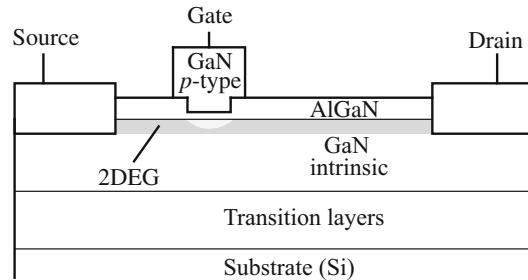
Gallium Nitride (GaN) is a second wide-bandgap material finding significant application in power electronics. The bandgap energy and critical field of GaN is even higher than SiC, and Eq. (4.40) again predicts that GaN can potentially achieve a major improvement in the relationship between on-resistance and breakdown voltage. Thin-film lateral GaN devices are deposited on a Si or SiC substrate. Since no native oxide is available in GaN, these transistors are heterostructure field-effect devices. Early devices were depletion-mode field-effect transistors, but enhancement-mode FETs now are offered commercially [38].

The structure of a simple enhancement-mode GaN FET is diagrammed in Fig. 4.51. The device may be fabricated on a silicon substrate, or possible another substrate material such as SiC

**Fig. 4.51** Basic structure of enhancement-mode GaN FET

or sapphire. Since the coefficients of thermal expansion of the substrate and the GaN materials differ, transition layers are needed for improvement of reliability under thermal cycling. Intrinsic GaN is deposited next. A layer of AlGaN is then deposited. The crystalline structures and bandgaps of AlGaN and GaN differ, and hence the AlGaN–GaN interface is known as a *heterojunction*. In the GaN FET, a two-dimensional electron gas (2DEG) forms at the heterojunction as illustrated in Fig. 4.52; the 2DEG contains high-mobility electrons within the GaN material at the heterojunction. This type of device is also called a *high electron mobility transistor* (HEMT).

Fig. 4.52 Formation of a two-dimensional electron gas (2DEG) at the heterojunction, comprised of high-mobility electrons



The electrons within the 2DEG form a channel that can conduct current between the source and drain; because of their high mobility, the device exhibits low on-resistance. The gate forms a GaN diode between the gate terminal and the channel. The 2DEG can be controlled by the gate voltage: at zero gate voltage, the gate diode is reverse-biased, and its depletion region extends into the GaN region sufficient to deplete the 2DEG. With positive gate voltage, the 2DEG forms a complete conducting channel between drain and source. It is important to limit the on-state gate current to a value that does not exceed what the gate diode can handle. The $i-v$ characteristics of the gate GaN diode vary with temperature and drain current; depending on the manufacturer, a typical on-state gate-to-source voltage may be 3–5 V.

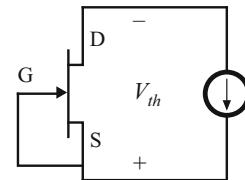
The high electron mobility of these devices yields competitive on-resistance at voltages below 600 V. GaN FETs are available at rated voltages of tens of volts up to 650 V, and devices at much higher voltages are described in the literature. In comparison with Si MOSFETs, the GaN FET can achieve similar on-resistance with smaller area, smaller capacitances, and faster switching times. Table 4.5 contains a comparison of a 650 V GaN FET with a 650 V Si superjunction MOSFET, having similar on-resistance. The gate charge of the GaN FET is roughly an order-of-magnitude smaller than the Si MOSFET. For reverse conduction with zero gate bias, the Si MOSFET body diode exhibits a voltage drop of approximately 0.8 V, while the GaN FET exhibits a drop of approximately 4 V. The Si MOSFET body diode exhibits significant reverse recovery, while the GaN FET does not.

The GaN FET structure of Fig. 4.51 does not contain a body diode. Nonetheless, the device is able to conduct both positive and negative current between drain and source when the device is on. Further, when $v_{gs} = 0$, the GaN FET will conduct when v_{ds} is sufficiently negative such that v_{gd} is positive enough to turn on the device, as illustrated in Fig. 4.53. Hence, the GaN FET cannot block negative voltage, but it is a current-bidirectional two-quadrant switch.

Table 4.5 Comparison of Si Superjunction MOSFET and GaN FET

	Si SJ MOSFET	GaN FET
Voltage rating	650 V	650 V
R_{on} , 25–150°C	24–60 mΩ	25–50 mΩ
Q_g at $V_{DS} = 400\text{V}$	123 nC (10 V)	12 nC (6 V)
V_{SD}	0.8 V	4 V
Q_{rr}	8.7 μC	—
t_{rr}	440 ns	—

Fig. 4.53 Reverse conduction through a FET such as a GaN device, when the gate is shorted to the source. The FET becomes forward-biased when $v_{ds} \leq -V_{th}$



4.4.3 MOSFET Gate Drivers

Now let us discuss some practical circuitry and basic considerations for driving power MOSFETs. Figure 4.54 contains a synchronous buck converter; in which the main switch Q_1 and the synchronous rectifier Q_2 are both realized using power MOSFETs. This configuration is found in quite a few examples, including not only low-voltage dc–dc buck converters, but also dc–ac inverter circuits and converters having bidirectional power flow. The transistor configuration is also called a *half-bridge* circuit, and the gate driver circuitry illustrated in this figure is called a *half-bridge gate driver*. The fundamentals of driving the MOSFETs in these applications are nearly the same, and are discussed in this section in the context of the synchronous buck converter.

In Fig. 4.54, MOSFET Q_2 is driven by low-side driver DR_{LS} . Since the source of Q_2 is connected to ground, the gate is driven at zero volts to turn Q_2 off, and at 12 V to turn Q_2 on.

The source of MOSFET Q_1 is connected to the switch node voltage $v_s(t)$; this voltage is approximately zero when Q_2 is on, but is approximately equal to the input voltage V_g when Q_1 is on. The high-side driver DR_{HS} must drive the gate of Q_1 to 0 V with respect to $v_s(t)$ to turn Q_1 off, and to +12 V with respect to $v_s(t)$ to turn Q_1 on. To drive Q_1 in this manner, the high-side driver circuit is referenced to the switch node voltage $v_s(t)$, and a level shifter circuit converts the ground-referenced control signal to a v_s -referenced signal as needed to drive the input of DR_{HS} .

A *bootstrap power supply* provides 12 V power to DR_{HS} that is referenced to v_s . When MOSFET Q_2 conducts, then capacitor C_{boot} charges to 12 V through diode D_{boot} and Q_2 . While Q_1 conducts, capacitor C_{boot} supplies power to DR_{HS} , that is approximately +12 V with respect to v_s . It is necessary to periodically turn Q_2 on, to recharge C_{boot} to 12 V and maintain power to DR_{HS} .

Up-to-date gate driver ICs contain *undervoltage lockout* (UVLO) circuitry that reliably turns off both MOSFETs when the 12 V power supply voltage is less than an UVLO threshold. This forces the MOSFETs into a known safe OFF-state while the 12 V power supply starts up. For

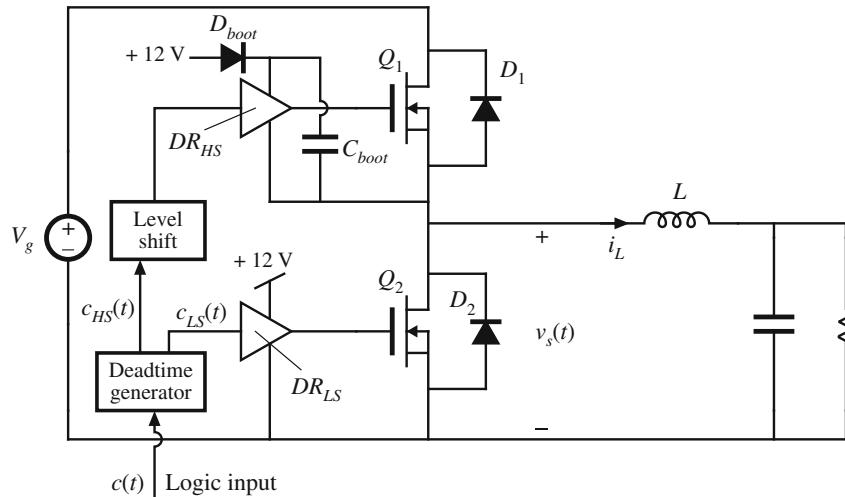


Fig. 4.54 Buck converter with MOSFET synchronous rectifier and half-bridge gate driver

reliable operation of the high-side bootstrap power supply, the voltage across capacitor C_{boot} must be higher than this UVLO threshold.

The control signal $c(t)$ is a logic signal that commands switching of the transistors, with switching frequency f_s and duty cycle D_c . This signal drives a *deadtime generator* that produces signals that drive the driver circuits DR_{LS} and DR_{HS} . It is necessary to make sure that Q_1 and Q_2 do not simultaneously conduct, even for a few nanoseconds—simultaneous conduction leads to very large current spikes drawn out of the source V_g , which can damage the MOSFETs or at least substantially reduce the efficiency. The function of the deadtime generator is to insert small delays, or *deadtimes*, that implement *break-before-make* switching, in which one transistor is fully turned off before the next transistor begins to turn on. Typical waveforms of the control signals $c(t)$, $c_{HS}(t)$, and $c_{LS}(t)$ are illustrated in Fig. 4.55.

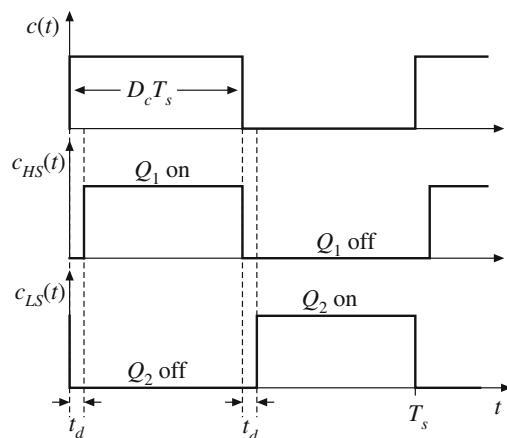


Fig. 4.55 Control waveforms of the deadtime generator block of Fig. 4.54

Let us consider next the details of the switching transition in which the synchronous rectifier Q_2 turns off, and then the main switch Q_1 turns on. In Fig. 4.56, the low-side driver DR_{LS} and MOSFET Q_2 are replaced by equivalent circuit models that aid in understanding the waveforms observed during this switching transition. The driver DR_{LS} is replaced by a Thevenin-equivalent model consisting of a voltage source $v_{thev}(t)$ and a resistance R_{thev} . The voltage source v_{thev} is the open-circuit output voltage of the driver, and can be assumed to be proportional to the control signal $c_{LS}(t)$ of Fig. 4.55. The resistance R_{thev} can be viewed, to first order, as arising from the on-resistance of the output driver stage MOSFETs of the driver DR_{LS} . It is traditional to rate gate drivers according to their peak current capability; so, for example, a driver rated at 12 V and 1 A would exhibit $R_{thev} = (12 \text{ V})/(1 \text{ A}) = 12 \Omega$. Additionally, in Fig. 4.56, MOSFET Q_2 is replaced with an equivalent circuit model consisting of the device capacitances C_{gs} , C_{gd} , and C_{ds} , body diode D_2 , and a dependent current source that models the dependence of the drain current on v_{gs} and v_s .

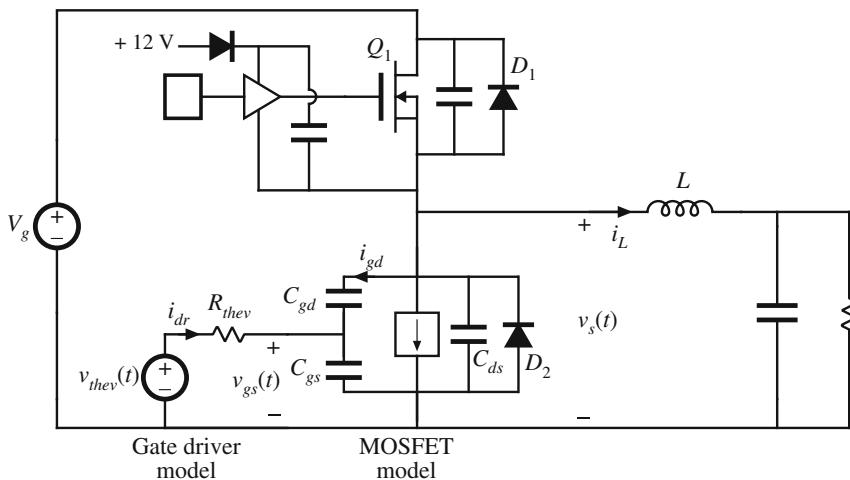


Fig. 4.56 Detail of half-bridge gate driver of Fig. 4.54, with low-side driver modeled by Thevenin-equivalent network, and with MOSFET Q_2 replaced by its equivalent circuit model

Waveforms of the switching transition are illustrated in Fig. 4.57. Initially, Q_2 is on, and its gate-to-source voltage $v_{gs}(t)$ is high. The switch node voltage $v_s(t)$ is approximately zero, and transistor Q_1 is off. When the control signal $c_{LS}(t)$ commands the low-side driver to turn Q_2 off, then the Q_2 gate capacitances begin to discharge through the driver resistance R_{thev} . When the Q_2 gate voltage $v_{gs}(t)$ falls below the Q_2 threshold voltage V_{th} , then MOSFET Q_2 is fully off. With a properly chosen deadtime t_d , this happens before Q_1 begins to turn on.

After Q_2 has turned off, but before Q_1 turns on, where does the inductor current $i_L(t)$ flow? It is assumed that the inductor current has small ripple, and does not significantly change over the switching times illustrated in Fig. 4.57. With both Q_1 and Q_2 in the off state, and with positive inductor current in the direction illustrated, the inductor current will forward-bias the body diode D_2 . This body diode will continue to conduct for the remainder of the deadtime.

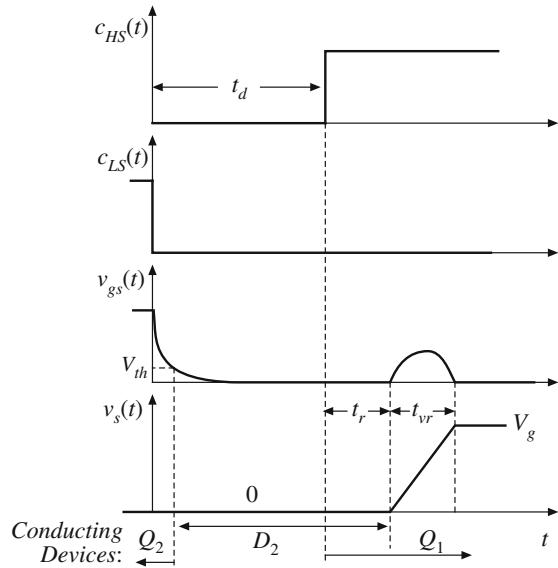


Fig. 4.57 Waveforms for the switching transition where Q_2 turns off and then Q_1 turns on

At the conclusion of the deadtime, the control signal $c_{HS}(t)$ commands the high-side driver to turn Q_1 on. Since body diode D_2 is conducting, it must undergo a reverse-recovery process, and hence reverse current flows through D_2 (also flowing through Q_1 and V_g). Consequently, D_2 induces switching loss in Q_1 , as described in Sect. 4.3. In Fig. 4.57, the D_2 reverse recovery time is labeled t_r .

When the reverse recovery of D_2 has progressed enough to allow the diode voltage to change, then the switch node voltage $v_s(t)$ will rise. Figure 4.57 is sketched for the case that the body diode softness factor is $S = 0$, so that the voltage $v_s(t)$ changes after the reverse recovery has concluded. During the interval of length t_{vr} , the switch node voltage rises from zero to V_g . During this interval, the energy stored in the output capacitances C_{ds} of MOSFETs Q_1 and Q_2 is dissipated as switching loss in Q_1 . Switching loss as described in Sect. 4.2.2 is also induced in Q_1 .

It can be observed from Fig. 4.56 that when $v_{gs}(t)$ and $v_{thev}(t)$ are both zero, there is zero voltage across R_{thev} , and hence i_{dr} is zero. This is what happens at the beginning of the t_{vr} interval of Fig. 4.57. But since $v_s(t)$ is rising, current $i_{gd} = C_{gd} dv_s/dt$ is induced in capacitance C_{gd} . This current must flow into C_{gs} since $i_{dr} = 0$. Hence, $v_{gs}(t)$ must increase as shown. For v_{gs} greater than zero, some negative driver current i_{dr} will occur, limited by the Thevenin resistance R_{thev} .

How high does $v_{gs}(t)$ become during the t_{vr} interval? It is important that v_{gs} remain less than V_{th} for the entire interval, so that MOSFET Q_2 remains off. If v_{gs} rises above V_{th} , then Q_2 will begin to turn on, leading to oscillations and additional switching loss. It is important to maintain $v_{gs} < V_{th}$ for the entire Q_1 turn-on interval.

A commonly used solution for reducing the rise of $V_{gs}(t)$ is illustrated in Fig. 4.58. A small-value resistor R_{g1} is connected between the high-side driver DR_{HS} and the gate of MOSFET Q_1 . This slows down the turn-on of Q_1 , reducing the rate at which the switch node voltage $v_s(t)$ rises. Hence the current i_{gd} of the Q_2 gate-to-drain capacitance is reduced, and $v_{gs}(t)$ increases more slowly. If R_{g1} is large enough, then the low-side driver DR_{LS} is able to maintain $v_{gs}(t)$ less than

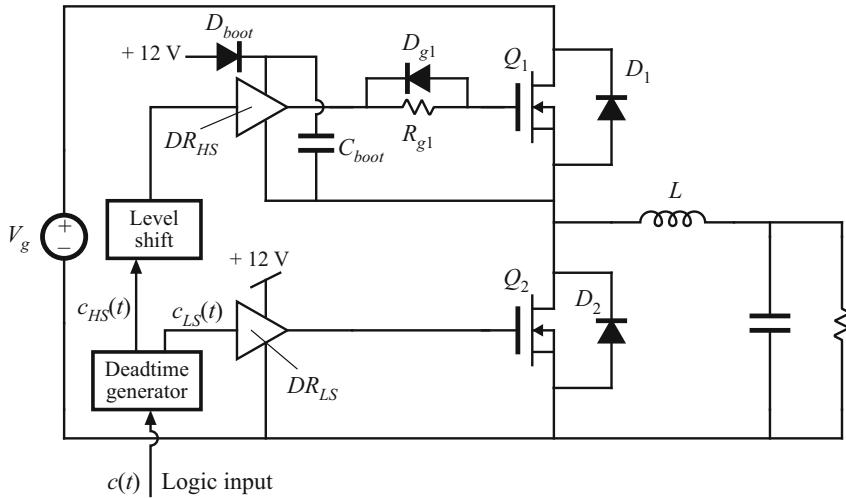


Fig. 4.58 Addition of resistor R_{g1} and diode D_{g1} between high-side driver and gate of Q_1 , to slow down the turn-on of Q_1 and maintain the V_{gs} of Q_2 below V_{th} during the Q_1 turn-on transition

V_{th} . Diode D_{g1} bypasses R_{g1} during the turn-off transition of Q_1 , so that R_{g1} reduces the turn-on speed but does not affect the turn-off speed. If the inductor current i_L can reverse polarity, then it may be desirable to insert a similar R_{g2} and D_{g2} network at the gate of Q_2 .

4.5 Minority-Carrier Transistors

4.5.1 Bipolar Junction Transistor (BJT)

A cross-section of an NPN power BJT is illustrated in Fig. 4.59. As with other power devices, current flows vertically through the silicon wafer. A lightly doped n^- region is inserted in the collector, to obtain the desired voltage breakdown rating. The transistor operates in the off state

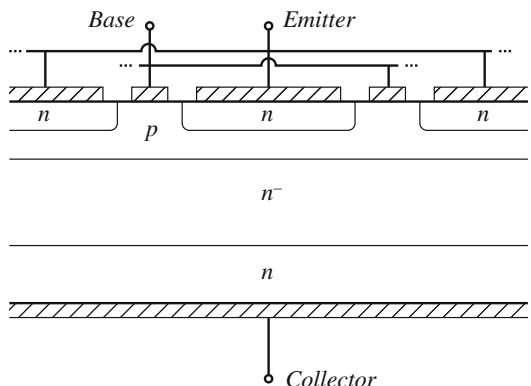


Fig. 4.59 Power BJT structure. Crosshatched regions are metallized contacts

(cutoff) when the $p-n$ base-emitter junction and the $p-n^-$ base-collector junction are reverse-biased; the applied collector-to-emitter voltage then appears essentially across the depletion region of the $p-n^-$ junction. The transistor operates in the on state (saturation) when both junctions are forward-biased; substantial minority charge is then present in the p and n^- regions. This minority charge causes the n^- region to exhibit a low on-resistance via the conductivity modulation effect. Between the off state and the on state is the familiar active region, in which the $p-n$ base-emitter junction is forward-biased and the $p-n^-$ base-collector junction is reverse-biased. When the BJT operates in the active region, the collector current is proportional to the base region minority charge, which in turn is proportional (in equilibrium) to the base current. There is in addition a fourth region of operation known as *quasi-saturation*, occurring between the active and saturation regions. Quasi-saturation occurs when the base current is insufficient to fully saturate the device; hence, the minority charge present in the n^- region is insufficient to fully reduce the n^- region resistance, and high transistor on-resistance is observed.

Consider the simple switching circuit of Fig. 4.60. Figure 4.61 contains waveforms illustrating the BJT turn-on and turn-off transitions. The transistor operates in the off state during interval (1), with the base-emitter junction reverse-biased by the source voltage $v_s(t) = -V_{s1}$. The turn-on transition is initiated at the beginning of interval (2), when the source voltage changes to $v_s(t) = +V_{s2}$. Positive current is then supplied by source v_s to the base of the BJT. This current first charges the capacitances of the depletion regions of the reverse-biased base-emitter and base-collector junctions. At the end of interval (2), the base-emitter voltage exceeds zero sufficiently for the base-emitter junction to become forward-biased. The length of interval (2) is called the *turn-on delay time*. During interval (3), minority charge is injected across the base-emitter junction from the emitter into the base region; the collector current is proportional to this minority base charge. Hence during interval (3), the collector current increases. Since the transistor drives a resistive load R_L , the collector voltage also decreases during interval (3). This causes the voltage to reduce across the reverse-biased base-collector depletion region (Miller) capacitance. Increasing the base current I_{B1} (by reducing R_B or increasing V_{s2}) increases the rate of change of both the base region minority charge and the charge in the Miller capacitance. Hence, increased I_{B1} leads to a decreased turn-on switching time.

Near or at the end of interval (3), the base-collector $p-n^-$ junction becomes forward-biased. Minority carriers are then injected into the n^- region, reducing its effective resistivity. Depending on the device geometry and the magnitude of the base current, a *voltage tail* [interval (4)] may be observed as the apparent resistance of the n^- region decreases via conductivity modulation. The BJT reaches on-state equilibrium at the beginning of interval (5), with low on-resistance and with substantial minority charge present in both the n^- and p regions. This minority charge significantly exceeds the amount necessary to support the active region conduction of the collector current I_{Con} ; its magnitude is a function of $I_{B1} - I_{Con}/\beta$, where β is the active-region current gain.

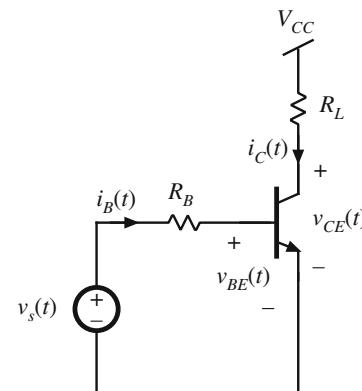


Fig. 4.60 Circuit for BJT switching time example

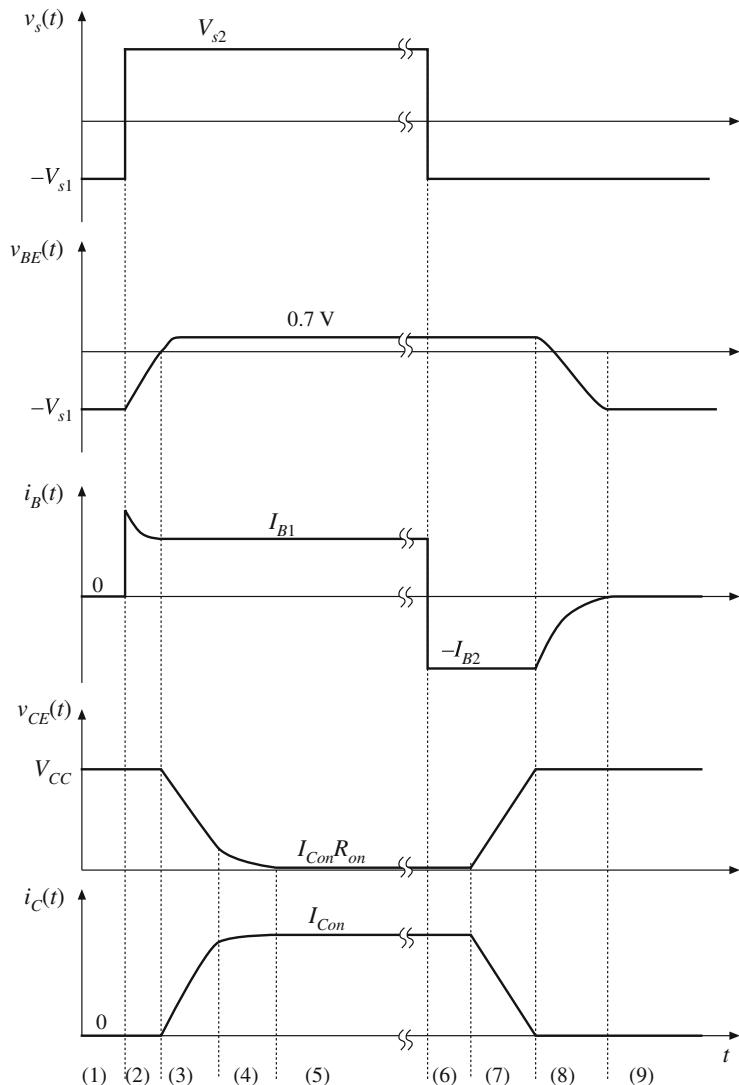


Fig. 4.61 BJT turn-on and turn-off transition waveforms

The turn-off process is initiated at the beginning of interval (6), when the source voltage changes to $v_s(t) = -V_{s1}$. The base-emitter junction remains forward-biased as long as minority carriers are present in its vicinity. Also, the collector current continues to be $i_C(t) = I_{Con}$ as long as the minority charge exceeds the amount necessary to support the active region conduction of I_{Con} , that is, as long as *excess charge* is present. So during interval (6), a negative base current flows equal to $-I_{B2} = (-V_{s1} - v_{BE}(t))/R_B$. This negative base current actively removes the total stored minority charge. Recombination further reduces the stored minority charge. Interval (6) ends when all of the excess minority charge has been removed. The length of interval (6)

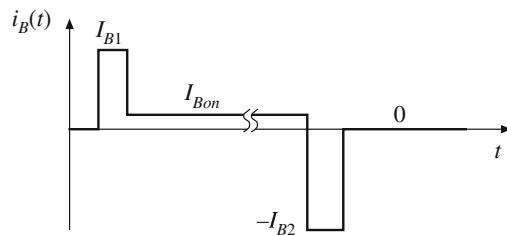


Fig. 4.62 Ideal base current waveform for minimization of switching times

is called the *storage time*. During interval (7), the transistor operates in the active region. The collector current $i_C(t)$ is now proportional to the stored minority charge. Recombination and the negative base current continue to reduce the minority base charge, and hence the collector current decreases. In addition, the collector voltage increases, and hence the base current must charge the Miller capacitance. At the end of interval (7), the minority stored charge is equal to zero, and the base-emitter junction can become reverse-biased. The length of interval (7) is called the turn-off time or *fall time*. During interval (8), the reverse-biased base-emitter junction capacitance is discharged to voltage $-V_{s1}$. During interval (9), the transistor operates in equilibrium, in the off state.

It is possible to turn the transistor off using $I_{B2} = 0$; for example, we could let V_{s1} be approximately zero. However, this leads to very long storage and turn-off switching times. If $I_{B2} = 0$, then all of the stored minority charge must be removed passively, via recombination. From the standpoint of minimizing switching times, the base current waveform of Fig. 4.62 is ideal. The initial base current I_{B1} is large in magnitude, such that charge is inserted quickly into the base, and the turn-on switching times are short. A compromise value of equilibrium on-state current I_{Bon} is chosen, to yield a reasonably low collector-to-emitter forward voltage drop, while maintaining moderate amounts of excess stored minority charge and hence keeping the storage time reasonably short. The current $-I_{B2}$ is large in magnitude, such that charge is removed quickly from the base and hence the storage and turn-off switching times are minimized.

Unfortunately, in most BJTs, the magnitudes of I_{B1} and I_{B2} must be limited because excessive values lead to device failure. As illustrated in Fig. 4.63, the base current flows laterally through the p region. This current leads to a voltage drop in the resistance of the p material, which influences the voltage across the base-emitter junction. During the turn-off transition, the base current $-I_{B2}$ causes the base-emitter junction voltage to be greater in the center of the base

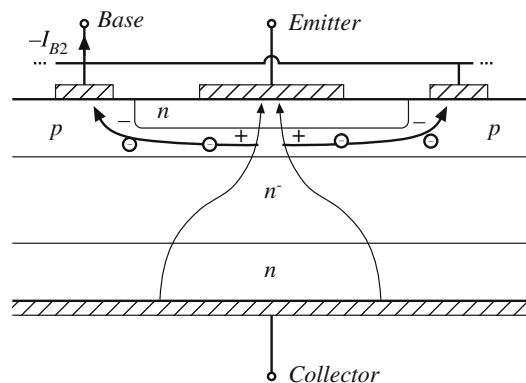


Fig. 4.63 A large I_{B2} leads to focusing of the emitter current away from the base contacts, due to the voltage induced by the lateral base region current

region, and smaller at the edges near the base contacts. This causes the collector current to focus near the center of the base region. In a similar fashion, a large I_{B1} causes the collector current to crowd near the edges of the base region during the turn-on transition. Since the collector-to-emitter voltage and collector current are simultaneously large during the switching transitions, substantial power loss can be associated with current focusing. Hence hot spots are induced at the center or edge of the base region. The positive temperature coefficient of the base-emitter junction current (corresponding to a negative temperature coefficient of the junction voltage) can then lead to thermal runaway and device failure. Thus, to obtain reliable operation, it may be necessary to limit the magnitudes of I_{B1} and I_{B2} . It may also be necessary to add external *snubber* networks which reduce the instantaneous transistor power dissipation during the switching transitions.

Steady-state characteristics of the BJT are illustrated in Fig. 4.64. In Fig. 4.64a, the collector current I_C is plotted as a function of the base current I_B , for various values of collector-to-emitter voltage V_{CE} . The cutoff, active, quasi-saturation, and saturation regions are identified. At a given collector current I_c , to operate in the saturation region with minimum forward voltage drop, the base current I_B must be sufficiently large. The slope dI_C/dI_B in the active region is the current gain β . It can be seen that β decreases at high current—near the rated current of the BJT, the current gain decreases rapidly and hence it is difficult to fully saturate the device. Collector current I_C is plotted as a function of collector-to-emitter voltage V_{CE} in Fig. 4.64b, for various values of I_B . The breakdown voltages BV_{SUS} , BV_{CEO} , and BV_{CBO} are illustrated. BV_{CBO} is the avalanche breakdown voltage of the base-collector junction, with the emitter open circuited or with sufficiently negative base current. BV_{CBO} is the somewhat smaller collector-emitter breakdown voltage observed when the base current is zero; as avalanche breakdown is approached, free carriers are created that have the same effect as a positive base current and that cause the breakdown voltage to be reduced. BV_{SUS} is the breakdown voltage observed with positive base current. Because of the high instantaneous power dissipation, breakdown usually results in destruction of the BJT. In most applications, the off-state transistor voltage must not exceed BV_{CBO} .

At voltage levels up to 600 V, the BJT has been replaced by the MOSFET in power applications. At 600 V and above, the BJT has been displaced by a more recent minority-carrier device, the IGBT.

4.5.2 Insulated-Gate Bipolar Transistor (IGBT)

A cross-section of the IGBT is illustrated in Fig. 4.65. Comparison with Fig. 4.47 reveals that the IGBT and power MOSFET are very similar in construction. The key difference is the p region connected to the collector of the IGBT. So the IGBT is a modern four-layer power semiconductor device having a MOS gate.

The function of the added p region is to inject minority charges into the n^- region while the device operates in the on state, as illustrated in Fig. 4.65. When the IGBT conducts, the $p-n^-$ junction is forward-biased, and the minority charges injected into the n^- region cause conductivity modulation. This reduces the on-resistance of the n^- region, and allows high-voltage IGBTs to be constructed which have low forward voltage drops. IGBTs rated as low as 600 V and as high as 6500 V are readily available. The forward voltage drops of these devices are typically 2 to 4 V, much lower than would be obtained in equivalent MOSFETs of the same silicon area.

Several schematic symbols for the IGBT are in current use; the symbol illustrated in Fig. 4.66a is the most popular. A two-transistor equivalent circuit for the IGBT is illustrated

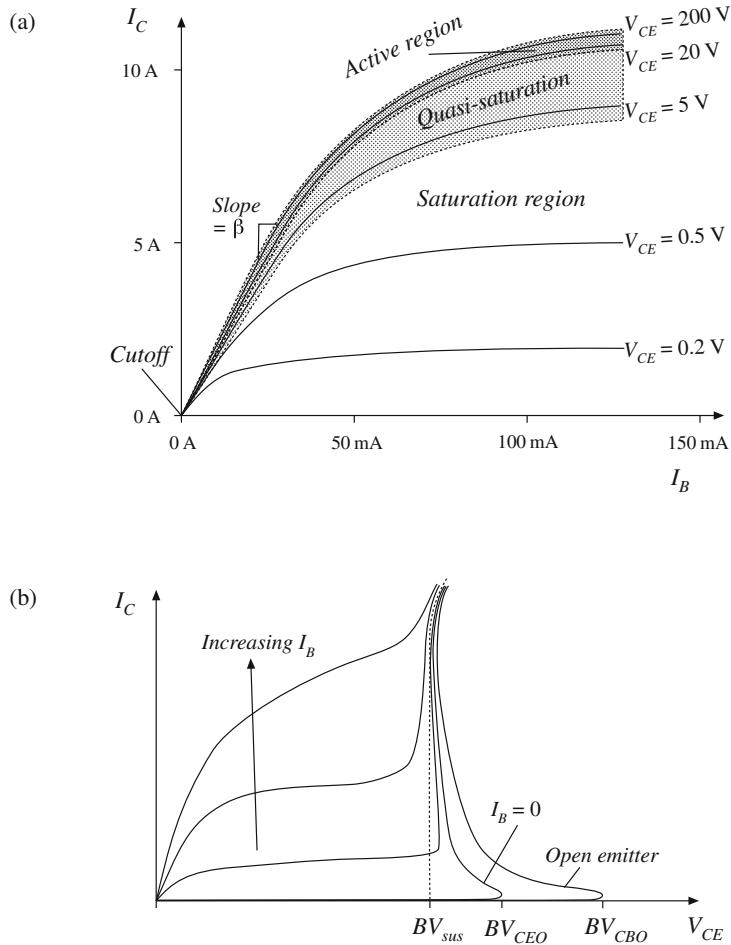


Fig. 4.64 BJT static characteristics: (a) I_C vs. I_B , illustrating the regions of operation; (b) I_C vs. V_{CE} , illustrating voltage breakdown characteristics

in Fig. 4.66b. The IGBT functions effectively as an n -channel power MOSFET, cascaded by a PNP emitter-follower BJT. The physical locations of the two effective devices are illustrated in Fig. 4.67. It can be seen that there are two effective currents: the effective MOSFET channel current i_1 , and the effective PNP collector current i_2 .

The price paid for the reduced voltage drop of the IGBT is its increased switching times, especially during the turn-off transition. In particular, the IGBT turn-off transition exhibits a phenomenon known as *current tailing*. The effective MOSFET can be turned off quickly, by removing the gate-to-emitter voltage such that the gate-to-emitter voltage is negative. This causes the channel current i_1 to quickly become zero. However, the PNP collector current i_2 continues to flow as long as minority charge is present in the n^- region. Since there is no way to actively remove the stored minority charge, it slowly decays via recombination. So i_2 slowly decays in proportion

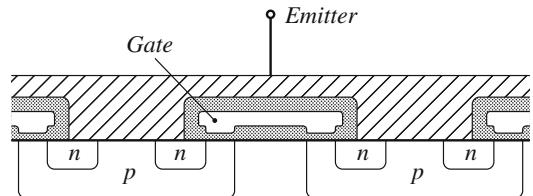


Fig. 4.65 IGBT structure. Crosshatched regions are metallized contacts. Shaded regions are insulating silicon dioxide layers

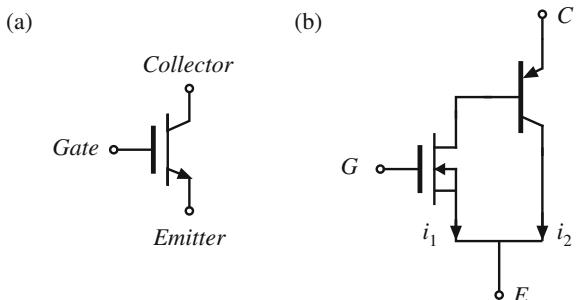
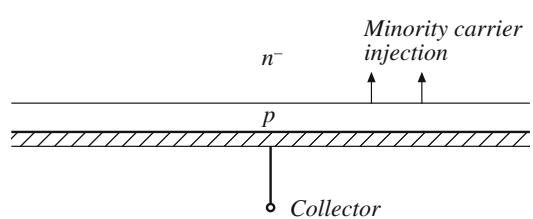


Fig. 4.66 The IGBT: (a) schematic symbol, (b) equivalent circuit

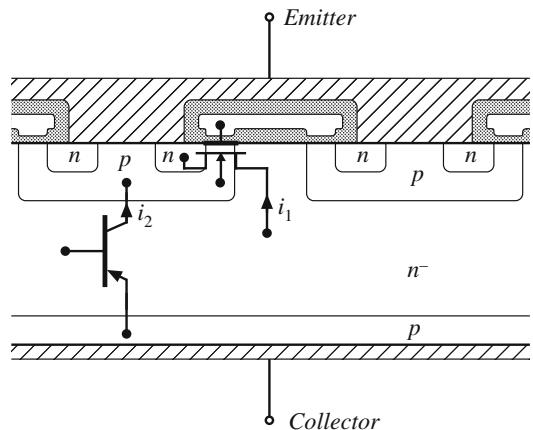


Fig. 4.67 Physical locations of the effective MOSFET and PNP components of the IGBT

to the minority charge, and a current tail is observed. The length of the current tail can be reduced by introduction of recombination centers in the n^- region, at the expense of a somewhat increased on-resistance. The current gain of the effective PNP transistor can also be minimized, causing i_1 to be greater than i_2 . Nonetheless, the turn-off switching time of the IGBT is significantly longer than that of the MOSFET, with typical turn-off times in the range $0.5\ \mu s$ to $5\ \mu s$.

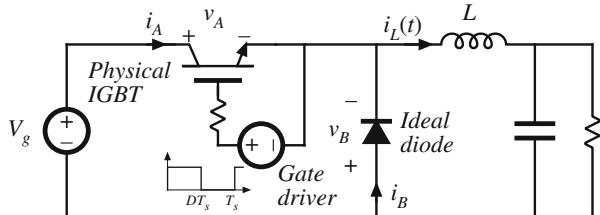


Fig. 4.68 IGBT switching loss example

A buck converter circuit containing an ideal diode and nonideal (physical) IGBT is illustrated in Fig. 4.68. Turn-off transition waveforms are illustrated in Fig. 4.69; these waveforms are similar to the MOSFET waveforms of Fig. 4.25. The diode is initially reverse-biased, and the voltage $v_A(t)$ rises from approximately zero to V_g . The interval length $(t_1 - t_0)$ is the time required for the gate drive circuit to charge the IGBT gate-to-collector capacitance. At time $t = t_1$, the diode becomes forward-biased, and current begins to commute from the IGBT to the diode. The interval $(t_2 - t_1)$ is the time required for the gate drive circuit to discharge the IGBT gate-to-emitter capacitance to the threshold value which causes the effective MOSFET in Fig. 4.66b to be in the off state. This time can be minimized by use of a high-current gate drive circuit which discharges the gate capacitance quickly. However, switching off the effective MOSFET does not completely interrupt the IGBT current $i_A(t)$: current $i_2(t)$ continues to flow through the effective PNP bipolar junction transistor of Fig. 4.66b as long as minority carriers continue to

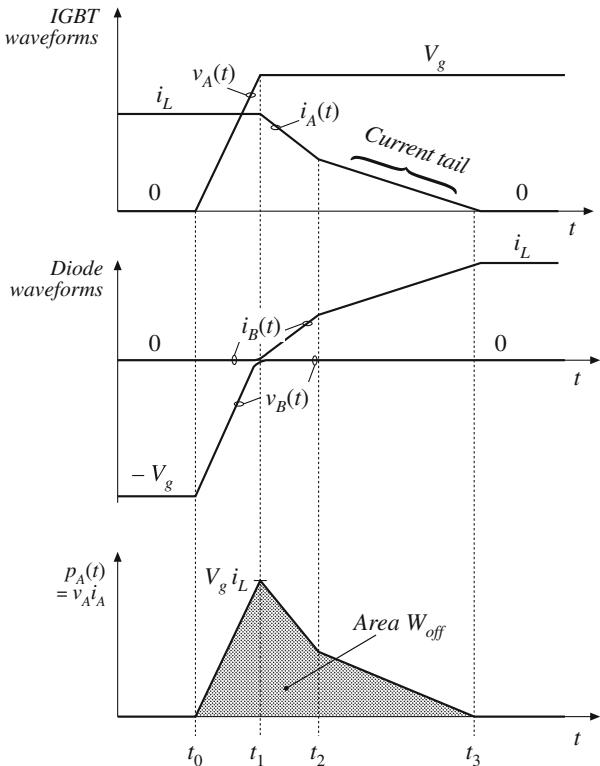


Fig. 4.69 IGBT turn-off transition waveforms for the circuit of Fig. 4.68

exist within its base region. During the interval $t_2 < t < t_3$, the current is proportional to this stored minority charge, and the current tail interval length ($t_3 - t_2$) is equal to the time required for this remaining stored minority charge to recombine.

The energy W_{off} lost during the turn-off transition of the IGBT is again the area under the instantaneous power waveform, as illustrated in Fig. 4.69. The switching loss can again be evaluated using Eq. (4.6). Switching loss typically limits the maximum switching frequencies of conventional PWM converters employing IGBTs to roughly 1 to 30 kHz.

The added $p-n^-$ diode junction of the IGBT is not normally designed to block significant voltage. Hence, the IGBT has negligible reverse voltage-blocking capability.

Since the IGBT is a four-layer device, there is the possibility of SCR-type latchup, in which the IGBT cannot be turned off by gate voltage control. Recent devices are not susceptible to this problem. These devices are quite robust, hot spot and current crowding problems are nonexistent, and the need for external snubber circuits is minimal.

The on-state forward voltage drop of the IGBT can be modeled by a forward-biased diode junction, in series with an effective on-resistance. The temperature coefficient of the IGBT forward voltage drop is complicated by the fact that the diode junction voltage has a negative temperature coefficient, while the on-resistance has a positive temperature coefficient. Fortunately, near rated current the on-resistance dominates, leading to an overall positive temperature coefficient. In consequence, IGBTs can be easily connected in parallel, with a modest current derating. Large modules are commercially available, containing multiple parallel-connected chips.

Characteristics of several commercially available single-chip IGBTs and multiple-chip IGBT modules are listed in Table 4.6.

4.5.3 Thyristors (SCR, GTO)

Of all conventional semiconductor power devices, the silicon-controlled rectifier (SCR) is the oldest, has the lowest cost per rated kVA, and is capable of controlling the greatest amount of power. Devices having voltage ratings of 5000 to 7000 V and current ratings of several thousand amperes are available. In utility dc transmission line applications, series-connected light-triggered SCRs are employed in inverters and rectifiers that interface the ac utility system

Table 4.6 Characteristics of several commercial IGBTs

Part number	Rated maximum voltage	Rated average current	V_F (typical)	t_f (typical)
Single-chip devices				
HGTP12N60A4	600 V	23 A	2.0 V	70 ns
HGTG32N60E2	600 V	32 A	2.4 V	0.62 μ s
HGTG30N120D2	1200 V	30 A	3.2 V	0.58 μ s
Multiple-chip modules				
CM400HA-12E	600 V	400 A	2.7 V	0.3 μ s
CM300HA-24E	1200 V	300 A	2.7 V	0.3 μ s
CM800HA-34H	1700 V	800 A	3.3 V	0.6 μ s
High voltage modules				
CM 800HB-50H	2500 V	800 A	3.15 V	1.0 μ s
CM 600HB-90H	4500 V	900 A	3.3 V	1.2 μ s

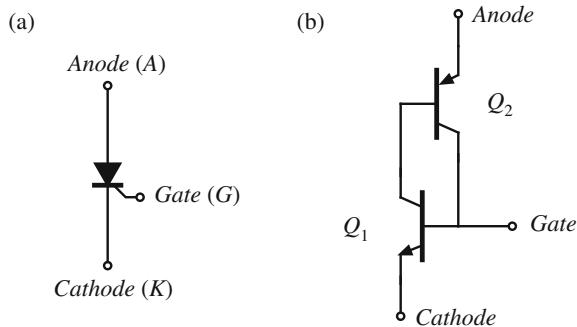
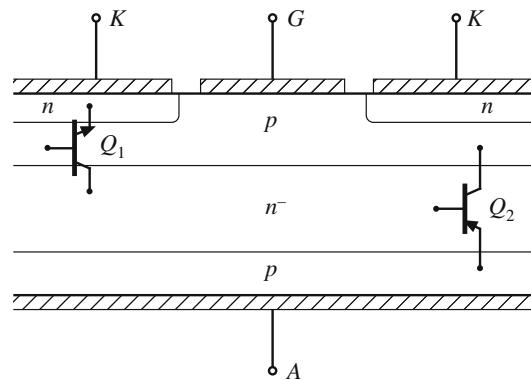


Fig. 4.70 The SCR: (a) schematic symbol, (b) equivalent circuit



to dc transmission lines which carry roughly 1 kA and 1 MV. A single large SCR fills a silicon wafer that is several inches in diameter, and is mounted in a hockey-puck-style case.

The schematic symbol of the SCR is illustrated in Fig. 4.70a, and an equivalent circuit containing NPN and PNP BJT devices is illustrated in Fig. 4.70b. A cross-section of the silicon chip is illustrated in Fig. 4.71. Effective transistor Q_1 is composed of the n , p , and n^- regions, while effective transistor Q_2 is composed of the p , n^- , and p regions as illustrated.

The device is capable of blocking both positive and negative anode-to-cathode voltages. Depending on the polarity of the applied voltage, one of the $p-n^-$ junctions is reverse-biased. In either case, the depletion region extends into the lightly doped n^- region. As with other devices, the desired voltage breakdown rating is obtained by proper design of the n^- region thickness and doping concentration.

The SCR can enter the on state when the applied anode-to-cathode voltage v_{AK} is positive. Positive gate current i_G then causes effective transistor Q_1 to turn on; this in turn supplies base current to effective transistor Q_2 , and causes it to turn on as well. The effective connections of the base and collector regions of transistors Q_1 and Q_2 constitute a positive feedback loop. Provided that the product of the current gains of the two transistors is greater than one, then the currents of the transistors will increase regeneratively. In the on state, the anode current is limited by the external circuit, and both effective transistors operate fully saturated. Minority carriers are injected into all four regions, and the resulting conductivity modulation leads to very low forward voltage drop. In the on state, the SCR can be modeled as a forward-biased diode junction in series with a low-value on-resistance. Regardless of the gate current, the SCR is latched in the on state: it cannot be turned off except by application of negative anode current

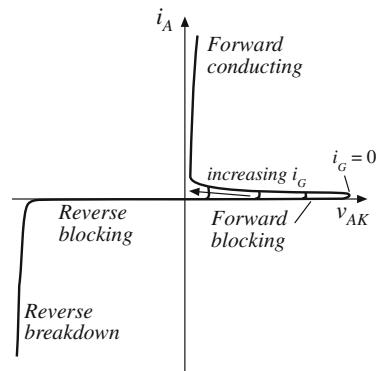


Fig. 4.72 Static $i_A - v_{AK}$ characteristics of the SCR

or negative anode-to-cathode voltage. In phase-controlled converters, the SCR turns off at the zero crossing of the converter ac input or output waveform. In forced commutation converters, external commutation circuits force the controlled turn-off of the SCR, by reversing either the anode current or the anode-to-cathode voltage.

Static $i_A - v_{AK}$ characteristics of the conventional SCR are illustrated in Fig. 4.72. It can be seen that the SCR is a voltage-bidirectional two-quadrant switch. The turn-on transition is controlled actively via the gate current. The turn-off transition is passive.

During the turn-off transition, the rate at which forward anode-to-cathode voltage is reapplied must be limited, to avoid retriggering the SCR. The turn-off time t_q is the time required for minority stored charge to be actively removed via negative anode current, and for recombination of any remaining minority charge. During the turn-off transition, negative anode current actively removes stored minority charge, with waveforms similar to diode turn-off transition waveforms of Fig. 4.31. Thus, after the first zero crossing of the anode current, it is necessary to wait for time t_q before reapplying positive anode-to-cathode voltage. It is then necessary to limit the rate at which the anode-to-cathode voltage increases, to avoid retriggering the device. Inverter-grade SCRs are optimized for faster switching times, and exhibit smaller values of t_q .

Conventional SCR wafers have large feature size, with coarse or nonexistent interdigititation of the gate and cathode contacts. The parasitic elements arising from this large feature size lead to several limitations. During the turn-on transition, the rate of increase of the anode current must be limited to a safe value. Otherwise, cathode current focusing can occur, which leads to formation of hot spots and device failure.

The coarse feature size of the gate and cathode structure is also what prevents the conventional SCR from being turned off by active gate control. One might apply a negative gate current, in an attempt to actively remove all of the minority stored charge and to reverse-bias the $p-n$ gate-cathode junction. The reason that this attempt fails is illustrated in Fig. 4.73. The large negative gate current flows laterally through the adjoining the p region, inducing a voltage drop as shown. This causes the gate-cathode junction voltage to be smaller near the gate contact, and relatively larger away from the gate contact. The negative gate current is able to reverse-bias only the portion of the gate-cathode junction in the vicinity of the gate contact; the remainder of the gate-cathode junction continues to be forward-biased, and cathode current continues to flow. In effect, the gate contact is able to influence only the nearby portions of the cathode.

The gate turn off thyristor, or GTO, is a more recent power device having small feature size. The gate and cathode contacts highly interdigitated, such that the entire gate-cathode $p-n$

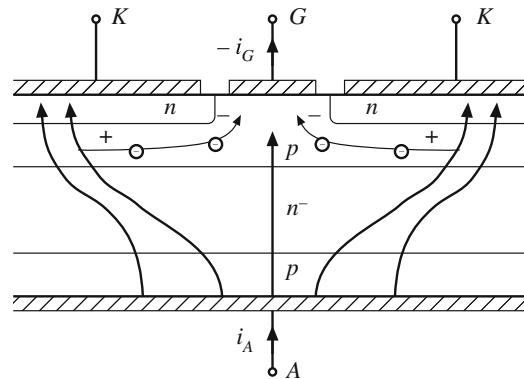


Fig. 4.73 Negative gate current is unable to completely reverse-bias the gate-cathode junction. The anode current focuses away from the gate contact

junction can be reverse-biased via negative gate current during the turn-off transition. Like the SCR, a single large GTO can fill an entire silicon wafer. Maximum voltage and current ratings of commercial GTOs are lower than those of SCRs.

The turn-off gain of a GTO is the ratio of on-state current to the negative gate current magnitude required to switch the device off. Typical values of this gain are 2 to 5, meaning that several hundred amperes of negative gate current may be required to turn off a GTO conducting 1000 A. Also of interest is the maximum controllable on-state current. The GTO is able to conduct peak currents significantly greater than the rated average current; however, it may not be possible to switch the device off under gate control while these high peak currents are present.

4.6 Additional Sources of Switching Loss

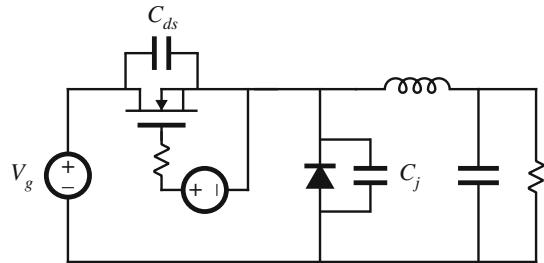
Switching loss caused by transistor switching times with a clamped inductive load is introduced in Sect. 4.2.2. Current tailing in IGBTs leads to this type of switching loss, as discussed in Sect. 4.5.2. Diode reverse recovery also induces switching loss as modeled in Sect. 4.3.3.

Several other sources of switching loss are discussed in this section. Semiconductor output capacitances store energy that is dissipated in the transistor at the transistor turn-on transition. Inductances that effectively are in series with the transistor store energy when the transistor conducts; when the transistor turns off and interrupts the inductor current, the stored energy is dissipated in the transistor. Diode reverse recovery can also induce switching loss in other circuit elements. These additional mechanisms of switching loss are discussed in this section.

4.6.1 Device Capacitances, and Leakage, Package, and Stray Inductances

Reactive elements can also lead to switching loss. Capacitances that are effectively in parallel with switching elements are shorted out when the switch turns on, and any energy stored in the capacitance is lost. The capacitances are charged without energy loss when the switching elements turn off, and the transistor turn-off loss W_{off} computed in Eq. (4.5) may be reduced.

Fig. 4.74 The energy stored in the semiconductor output capacitances is lost during the transistor turn-on transition



Likewise, inductances that are effectively in series with a switching element lose their stored energy when the switch turns off. Hence, series inductances lead to additional switching loss at turn-off, but can reduce the transistor turn-on loss.

The stored energies of the reactive elements can be summed to find the total energy loss per switching period due to these mechanisms. For linear capacitors and inductors, the stored energy is

$$W_C = \sum_{\text{capacitive elements}} \frac{1}{2} C_i V_i^2 \quad (4.41)$$

$$W_L = \sum_{\text{inductive elements}} \frac{1}{2} L_j I_j^2$$

A common source of this type of switching loss is the output capacitances of the semiconductor switching devices. The depletion layers of reverse-biased semiconductor devices exhibit capacitance which stores energy. When the transistor turns on, this stored energy is dissipated by the transistor. For example, in the buck converter of Fig. 4.74, the MOSFET exhibits drain-to-source capacitance C_{ds} , and the reverse-biased diode exhibits junction capacitance C_j . During the switching transitions these two capacitances are effectively in parallel, since the dc source V_g is effectively a short-circuit at high frequency. To the extent that the capacitances are linear, the energy lost when the MOSFET turns on is

$$W_C = \frac{1}{2} (C_{ds} + C_j) V_g^2 \quad (4.42)$$

Typically, this type of switching loss is significant at voltage levels above 100 V. The MOSFET gate drive circuit, which must charge and discharge the MOSFET gate capacitances, also exhibits this type of loss.

As noted in Sect. 4.4.1, the incremental drain-to-source capacitance C_{ds} of the power MOSFET is a strong function of the drain-to-source voltage v_{ds} . $C_{ds}(v_{ds})$ follows an approximate inverse-square root dependence of v_{ds} , as given by Eq. (4.39). The energy stored in C_{ds} at $v_{ds} = V_{DS}$ is

$$W_{Cds} = \int v_{ds} i_C dt = \int_0^{V_{DS}} v_{ds} C_{ds}(v_{ds}) dv_{ds} \quad (4.43)$$

where $i_C = C_{ds}(v_{ds})dv_{ds}/dt$ is the current in C_{ds} . Substitution of Eq. (4.39) into (4.43) yields

$$W_{Cds} = \int_0^{V_{DS}} C'_0(v_{ds}) \sqrt{v_{ds}} dv_{ds} = \frac{2}{3} C_{ds}(V_{DS}) V_{DS}^2 \quad (4.44)$$

This energy is lost each time the MOSFET switches on. From the standpoint of switching loss, the drain-to-source capacitance is equivalent to a linear capacitance having the value $\frac{4}{3}C_{ds}(V_{DS})$.

The Schottky diode is essentially a majority-carrier device, which does not exhibit a reverse-recovery transient such as in Fig. 4.31. Reverse-biased Schottky diodes do exhibit significant junction capacitance, however, which can be modeled with a parallel capacitor C_j as in Fig. 4.74, and which leads to energy loss at the transistor turn-on transition.

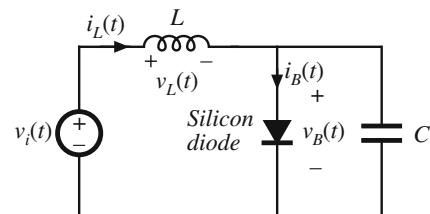
Common sources of series inductance are transformer leakage inductances in isolated converters (discussed in Chap. 6), as well as the inductances of interconnections and of semiconductor device packages. In addition to generating switching loss, these elements can lead to excessive peak voltage stress during the transistor turn-off transition. Interconnection and package inductances can lead to significant switching loss in high-current applications, and leakage inductance is an important source of switching loss in many transformer-isolated converters.

4.6.2 Inducing Switching Loss in Other Elements

Diode stored minority charge can induce switching loss in the (nonideal) converter reactive elements. As an example, consider the circuit of Fig. 4.75, containing an ideal voltage source $v_f(t)$, an inductor L , a capacitor C (which may represent the diode junction capacitance, or the junction capacitance in parallel with an external capacitor), and a silicon diode. The diode switching processes of many converter and rectifier circuits can be modeled by a circuit of this form. The voltage source produces the rectangular waveform $v_i(t)$ illustrated in Fig. 4.76. This voltage is initially positive, causing the diode to become forward-biased and the inductor current $i_L(t)$ to increase linearly with slope V_1/L . Since the current is increasing, the stored minority charge inside the diode also increases. At time $t = t_1$, the source voltage $v_i(t)$ becomes negative, and the inductor current decreases with slope $di_L/dt = -V_2/L$. The diode stored charge also decreases, but at a slower rate that depends not only on i_L but also on the minority-carrier recombination lifetime of the silicon material in the diode. Hence, at time $t = t_2$, when $i_L(t)$ reaches zero, some stored minority charge remains in the diode. So the diode continues to be forward-biased, and the inductor current continues to decrease with the same slope. The negative current for $t > t_2$ constitutes a reverse diode current, which actively removes diode stored charge. At some time later, $t = t_3$, the diode stored charge in the vicinity of the diode junction becomes zero, and the diode junction becomes reverse-biased. The inductor current is now negative, and must flow through the capacitor. The inductor and capacitor then form a series resonant circuit, which rings with decaying sinusoidal waveforms as shown. This ringing is eventually damped out by the parasitic loss elements of the circuit, such as the inductor winding resistance, inductor core loss, and capacitor equivalent series resistance.

The diode recovered charge induces loss in this circuit. During the interval $t_2 < t < t_3$, the minority stored charge Q_r recovered from the diode is

Fig. 4.75 A circuit in which the diode stored charge induces ringing, and ultimately switching loss, in (nonideal) reactive elements



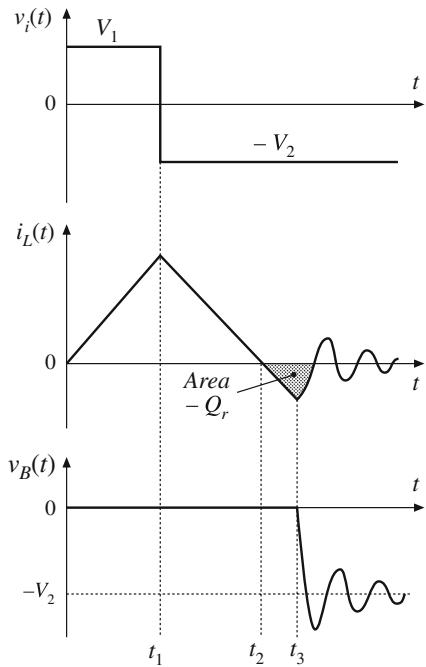


Fig. 4.76 Waveforms of the circuit of Fig. 4.75

$$Q_r = - \int_{t_2}^{t_3} i_L(t) dt \quad (4.45)$$

This charge is directly related to the energy stored in the inductor during this interval. The energy W_L stored in the inductor is the integral of the power flowing into the inductor:

$$W_L = \int_{t_2}^{t_3} v_L(t) i_L(t) dt \quad (4.46)$$

During this interval, the applied inductor voltage is

$$v_L(t) = L \frac{di_L(t)}{dt} = -V_2 \quad (4.47)$$

Substitution of Eq. (4.47) into Eq. (4.46) leads to

$$W_L = \int_{t_2}^{t_3} L \frac{di_L(t)}{dt} i_L(t) dt = \int_{t_2}^{t_3} (-V_2) i_L(t) dt \quad (4.48)$$

Evaluation of the integral on the left side yields the stored inductor energy at $t = t_3$, or $L i_L^2(t_3)/2$. The right-side integral is evaluated by noting that V_2 is constant and by substitution of Eq. (4.45), yielding $V_2 Q_r$. Hence, the energy stored in the inductor at $t = t_3$ is

$$W_L = \frac{1}{2} L i_L^2(t_3) = V_2 Q_r \quad (4.49)$$

or, the recovered charge multiplied by the source voltage. For $t > t_3$, the ringing of the resonant circuit formed by the inductor and capacitor causes this energy to be circulated back and forth

between the inductor and capacitor. If parasitic loss elements in the circuit cause the ringing amplitude to eventually decay to zero, then the energy becomes lost as heat in the parasitic elements.

So diode stored minority charge can lead to loss in circuits that do not contain an active switching element. Also, ringing waveforms that decay before the end of the switching period indicate the presence of switching loss.

4.6.3 Efficiency vs. Switching Frequency

Suppose next that we add up all of the energies lost due to switching, as discussed above:

$$W_{tot} = W_{on} + W_{off} + W_D + W_C + W_L + \dots \quad (4.50)$$

This is the energy lost in the switching transitions of one switching period. To obtain the average switching power loss, we must multiply by the switching frequency:

$$P_{sw} = W_{tot} f_{sw} \quad (4.51)$$

Other losses in the converter include the conduction losses P_{cond} , modeled and solved as in Chap. 3, and other frequency-independent fixed losses P_{fixed} , such as the power required to operate the control circuit. The total loss is therefore

$$P_{loss} = P_{cond} + P_{fixed} + W_{tot} f_{sw} \quad (4.52)$$

which increases linearly with frequency. At the critical frequency

$$f_{crit} = \frac{P_{cond} + P_{fixed}}{W_{tot}} \quad (4.53)$$

the switching losses are equal to the other converter losses. Below this critical frequency, the total loss is dominated by the conduction and fixed loss, and hence the total loss and converter efficiency are not strong functions of switching frequency. Above the critical frequency, the switching loss dominates the total loss, and the converter efficiency decreases rapidly with increasing switching frequency. Typical dependence of the full-load converter efficiency on switching frequency is plotted in Fig. 4.77, for an arbitrary choice of parameter values. The critical frequency f_{crit} can be taken as a rough upper limit on the switching frequency of a practical converter.

4.7 Summary of Key Points

1. How an SPST ideal switch can be realized using semiconductor devices depends on the polarity of the voltage that the devices must block in the off state, and on the polarity of the current which the devices must conduct in the on state.
2. Single-quadrant SPST switches can be realized using a single transistor or a single diode, depending on the relative polarities of the off-state voltage and on-state current.
3. Two-quadrant SPST switches can be realized using a transistor and diode, connected in series (bidirectional-voltage) or in antiparallel (bidirectional-current). Several four-quadrant schemes are also listed here.

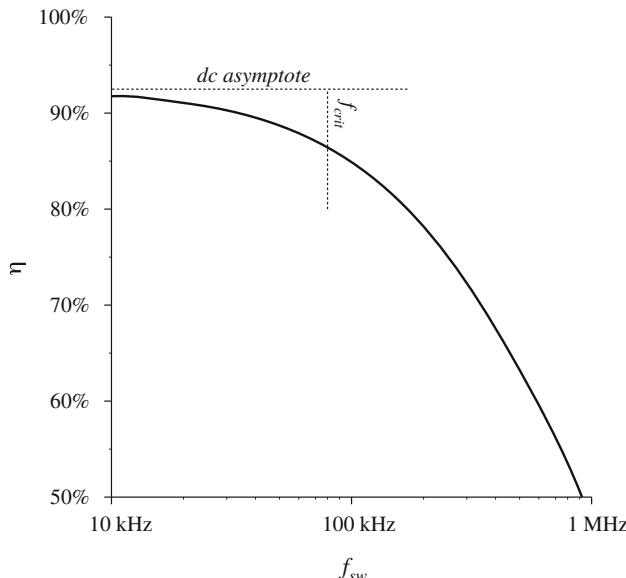


Fig. 4.77 Efficiency vs. switching frequency, based on Eq. (4.52), using arbitrary values for the choice of loss and load power. Switching loss causes the efficiency to decrease rapidly at high frequency

4. A “synchronous rectifier” is a MOSFET connected to conduct reverse current, with gate drive control as necessary. This device can be used where a diode would otherwise be required. If a MOSFET with sufficiently low R_{on} is used, reduced conduction loss is obtained.
5. Majority-carrier devices, including the MOSFET and Schottky diode, exhibit very fast switching times, controlled essentially by the charging of the device capacitances. However, the forward voltage drops of these devices increases quickly with increasing breakdown voltage.
6. Minority-carrier devices, including the BJT, IGBT, and thyristor family, can exhibit high breakdown voltages with relatively low forward voltage drop. However, the switching times of these devices are longer, and are controlled by the times needed to insert or remove stored minority charge.
7. Wide-bandgap semiconductor devices can significantly improve the tradeoff between breakdown voltage, on-resistance, and switching speed. Silicon carbide MOSFETs, SiC Schottky diodes, and GaN HEMTs have realized performance well beyond that achieved with silicon.
8. Energy is lost during switching transitions, owing to a variety of mechanisms. The resulting average power loss, or switching loss, is equal to this energy loss multiplied by the switching frequency. Switching loss imposes an upper limit on the switching frequencies of practical converters.
9. The diode and inductor present a “clamped inductive load” to the transistor. When a transistor drives such a load, it experiences high instantaneous power loss during the switching transitions. An example where this leads to significant switching loss is the IGBT and the “current tail” observed during its turn-off transition.

10. The familiar exponential $i-v$ characteristic of the $p-n$ diode is an equilibrium relationship that does not apply during switching transitions. To turn off the diode, its internal stored minority charge must be removed. During the reverse-recovery process, significant negative current can flow through the diode that induces switching loss in the transistor.
11. The equivalent circuit models of the previous chapter can be extended to model the switching loss caused by diode reverse recovery. Switching waveforms including the switching transitions are averaged, to find expressions for their dc components. These averaged expressions are employed in the construction of equivalent circuits.
12. Other significant sources of switching loss include diode stored charge and energy stored in certain parasitic capacitances and inductances. Parasitic ringing also indicates the presence of switching loss.

PROBLEMS

In Problems 4.1 to 4.6 and 4.10, the input voltage V_g is dc and positive with the polarity shown. Specify how to implement the switches using a minimal number of diodes and transistors, such that the converter operates over the entire range of duty cycles $0 \leq D \leq 1$. The switch states should vary as shown in Fig. 4.78. You may assume that the inductor current ripples and capacitor voltage ripples are small.

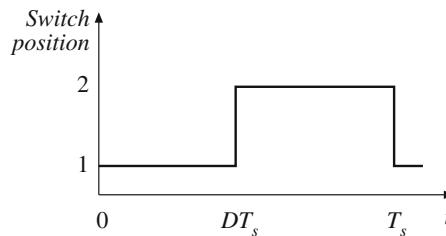


Fig. 4.78 Switch control method for Problems 4.1 to 4.6

For each problem, do the following:

- (a) Realize the switches using SPST ideal switches, and explicitly define the voltage and current of each switch.
- (b) Express the on-state current and off-state voltage of each SPST switch in terms of the converter inductor currents, capacitor voltages, and/or input source voltage.
- (c) Solve the converter to determine the inductor currents and capacitor voltages, as in Chap. 2.
- (d) Determine the polarities of the switch on-state currents and off-state voltages. Do the polarities vary with duty cycle?
- (e) State how each switch can be realized using transistors and/or diodes, and whether the realization requires single-quadrant, current-bidirectional two-quadrant, voltage-bidirectional two-quadrant, or four-quadrant switches.

- 4.1** Realize the switches in the converter of Fig. 4.79, following steps (a) to (e) described above.

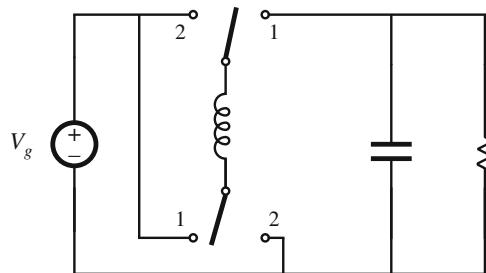


Fig. 4.79 Converter for Problem 4.1

- 4.2** Realize the switches in the converter of Fig. 4.80, following steps (a) to (e) described above.

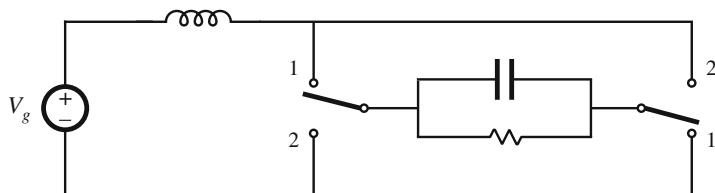


Fig. 4.80 Converter for Problem 4.2

- 4.3** Realize the switches in the converter of Fig. 4.81, following steps (a) to (e) described above.

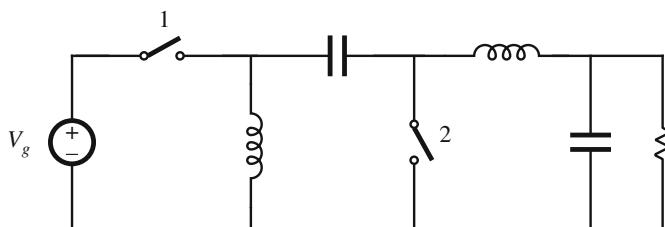
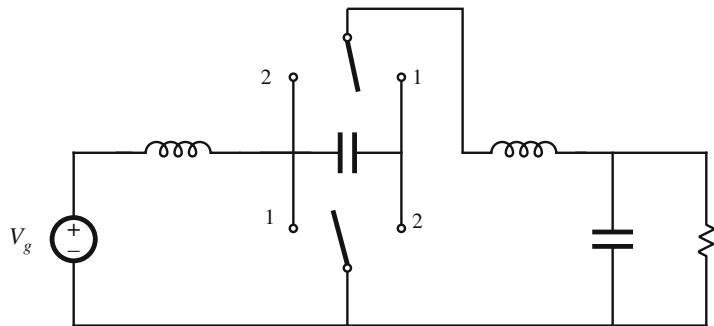
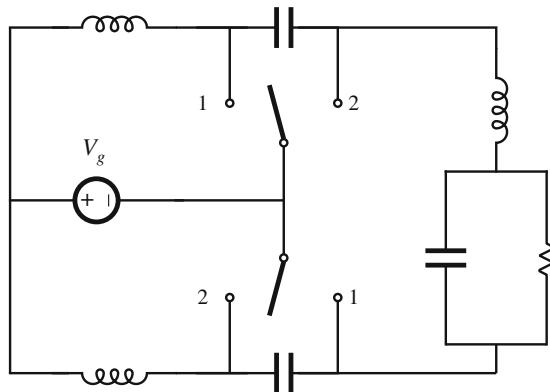


Fig. 4.81 Converter for Problem 4.3

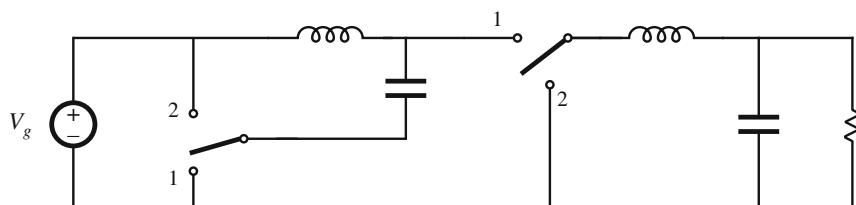
- 4.4** Realize the switches in the converter of Fig. 4.82, following steps (a) to (e) described above.

**Fig. 4.82** Converter for Problem 4.4

4.5 Realize the switches in the converter of Fig. 4.83, following steps (a) to (e) described above.

**Fig. 4.83** Converter for Problem 4.5

4.6 Realize the switches in the converter of Fig. 4.84, following steps (a) to (e) described above.

**Fig. 4.84** Converter for Problem 4.6

- 4.7** The buck-boost converter of Fig. 4.85 is implemented with a MOSFET and a *p-n* diode. The MOSFET can be modeled as ideal, but the diode exhibits a substantial reverse-recovery process, with reverse recovery time t_r and recovered charge Q_r . In addition, the inductor has winding resistance R_L . The converter operates in continuous conduction mode.

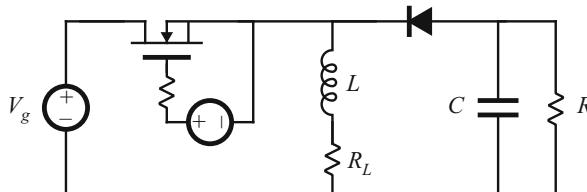
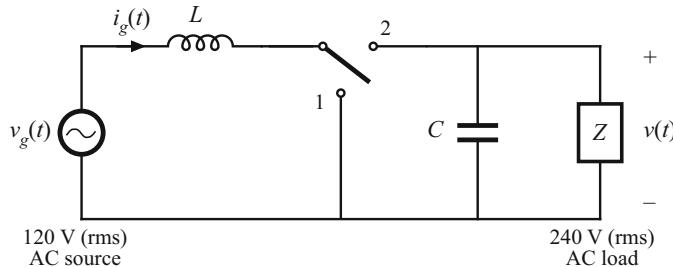
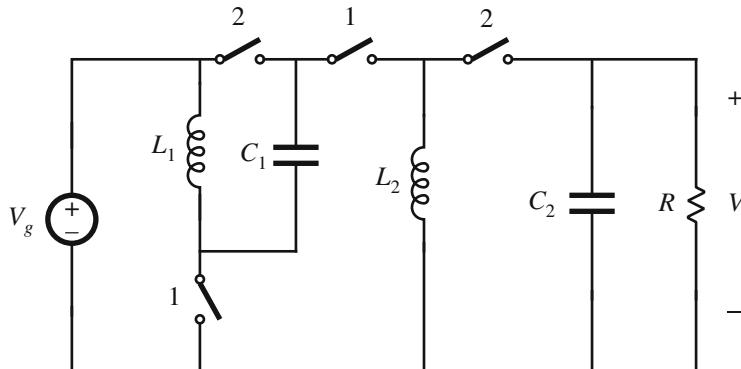


Fig. 4.85 Converter for Problem 4.7

Derive an equivalent circuit that models the dc components of the converter waveforms and that accounts for the loss mechanisms described above.

- 4.8** Solve the equivalent circuit model derived in Problem 4.7, to find closed-form expressions for the output voltage and inductor current.
- 4.9** A certain boost converter is implemented with a MOSFET and a *p-n* diode. The MOSFET can be modeled as ideal, but the diode exhibits a substantial reverse-recovery process, with reverse recovery time t_r and recovered charge Q_r . In addition, the inductor has winding resistance R_L .
- Derive an equivalent circuit that models the dc components of the converter waveforms and that accounts for the loss elements described above.
 - Solve your model to find an expression for the output voltage.
 - Plot the output voltage vs. duty cycle over the range $0 \leq D < 1$, for the following values: $R_L = 0.25 \Omega$, $f_s = 150 \text{ kHz}$, $Q_r = 5 \mu\text{coul}$, $t_r = 100 \text{ nsec}$, $R = 60 \Omega$, $V_g = 24 \text{ V}$.
- 4.10** It is desired to convert 60 Hz 120 VAC to 240 VAC, to power a 1 kW AC load. Although a conventional 60 Hz transformer could be used in this application, such a transformer is large and heavy. Instead, it is decided to use a boost converter switching at 100 kHz, as illustrated in Fig. 4.86. Potentially, this converter is small and lightweight. It operates at a constant duty cycle of approximately 0.5, so that $v(t) = 2v_g(t)$. The elements L and C are chosen to filter the switching harmonics and have small switching ripples; however, they have negligible effect on the 60 Hz components of the waveforms. The load is a linear impedance Z . Realize the switches in the converter of Fig. 4.86, following steps (a) to (e) listed above Problem 4.1.
- 4.11** The converter illustrated in Fig. 4.87 is sometimes employed in low-power applications requiring a wide range of conversion ratios. It is desired that all elements operate in the continuous conduction mode (CCM) over the range $0 \leq D < 1$. This mode is defined as follows: each switching period contains two subintervals numbered 1 and 2; in the schematic illustrated in Fig. 4.87, switches labeled “1” conduct during subinterval 1 for time DT_s , and switches labeled “2” conduct during subinterval 2 for time $(1 - D)T_s$.

**Fig. 4.86** Converter for Problem 4.10**Fig. 4.87** Double buck-boost converter of Problem 4.11

- (a) Solve the converter in steady state, to find the dc components of both capacitor voltages and both inductor currents. Your expressions should be functions of V_g , D , and R only. Clearly label the polarity or direction of each of these quantities on your schematic.
 - (b) Show how to realize the switches using BJTs and diodes, so that the converter operates in CCM over the range $0 \leq D < 1$. Document all steps in your derivation.
 - (c) How does your switch realization change if the duty cycle is restricted to the range $0 \leq D < 0.5$? Sketch the circuit and switch realization for this case.
- 4.12** An IGBT and a silicon diode operate in a buck converter, with the IGBT waveforms illustrated in Fig. 4.88. The converter operates with input voltage $V_g = 400$ V, output voltage $V = 200$ V, and load current $I = 10$ A.
- (a) Estimate the total energy lost during the switching transitions. You may graphically estimate the waveforms of Fig. 4.88.
 - (b) The forward voltage drop of the IGBT is 2.5 V, and the diode has forward voltage drop 1.5 V. All other sources of conduction loss and fixed loss can be neglected. Estimate the semiconductor conduction loss.
 - (c) Sketch the converter efficiency over the range of switching frequencies $1 \text{ kHz} \leq f_s \leq 100 \text{ kHz}$, and label numerical values.
- 4.13** Two MOSFETs are employed as current-bidirectional two-quadrant switches in a bidirectional battery charger/discharger based on the dc–dc buck converter, similar to Fig. 4.15.

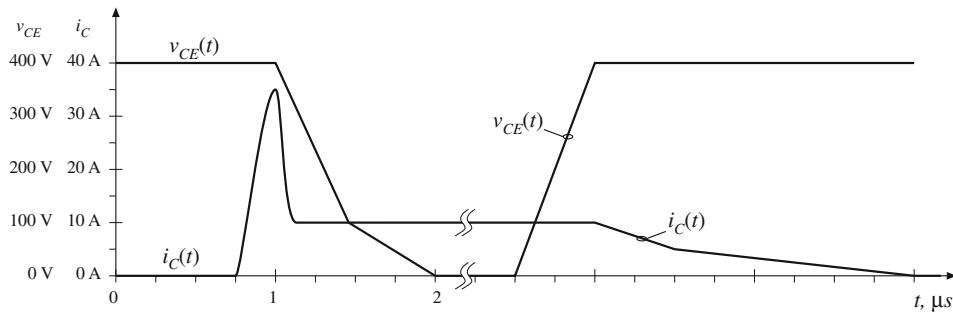


Fig. 4.88 IGBT voltage and current waveforms, Problem 4.12

This converter interfaces a 16 V battery to a 28 V main power bus. The maximum battery current is 40 A. The MOSFETs have on-resistances of $35\text{ m}\Omega$. Their body diodes have forward voltage drops of 1.0 V, and exhibit recovered charge Q_r of $25\text{ }\mu\text{C}$ and reverse recovery times t_r of 200 ns in the given circuit. You may assume that all diodes in this problem have “snappy” reverse recovery characteristics, and also assume that diode stored charge is the dominant cause of switching loss in this circuit. You may neglect all losses other than the semiconductor conduction losses and the switching loss induced by diode stored charge.

The current-bidirectional two-quadrant switches are realized as in Fig. 4.10a, utilizing the MOSFET body diodes.

- (a) Estimate the switching energy loss, conduction loss, and converter efficiency, when the battery is being charged at the maximum rate. The switching frequency is 100 kHz. External diodes are now added as illustrated in Fig. 4.10b. These diodes have forward voltage drops of 1.0 V, and exhibit recovered charge Q_r of $5\text{ }\mu\text{C}$ and reverse recovery times t_r of 40 ns in the given circuit.
- (b) Repeat the analysis of Part (a), for this case.
- (c) Over what range of switching frequencies does the addition of the external diodes improve the converter efficiency?

- 4.14** A switching converter operates with a switching frequency of 100 kHz. The converter waveforms exhibit damped sinusoidal ringing, initiated by the transistor turn-off transition, which decays slowly but eventually reaches zero before the end of the switching period. This ringing occurs in a series resonant circuit formed by parasitic inductances and capacitances in the circuit. The frequency of the ringing is 5 MHz. During the first period of sinusoidal ringing, the ac inductor current reaches a peak magnitude of 0.5 A, and the ac capacitor voltage reaches a peak magnitude of 200 V. Determine the following quantities:

- (a) the value of the total parasitic inductance,
- (b) the value of the total parasitic capacitance,
- (c) the energy lost per switching period, associated with this ringing, and
- (d) the switching loss associated with this ringing.
- (e) Derive a general expression for the switching loss, as a function of the switching frequency, ringing frequency, and the ringing voltage and current peak magnitudes during the first period of ringing.



The Discontinuous Conduction Mode

When the ideal switches of a dc–dc converter are implemented using current-unidirectional and/or voltage-unidirectional semiconductor switches, one or more new modes of operation known as *discontinuous conduction modes* (DCM) can occur. The discontinuous conduction mode arises when the switching ripple in an inductor current or capacitor voltage is large enough to cause the polarity of the applied switch current or voltage to reverse, such that the current- or voltage-unidirectional assumptions made in realizing the switch with semiconductor devices are violated. The DCM is commonly observed in dc–dc converters and rectifiers, and can also sometimes occur in inverters or in other converters containing two-quadrant switches.

The discontinuous conduction mode typically occurs with large inductor current ripple in a converter operating at light load and containing current-unidirectional switches. Since it is usually required that converters operate with their loads removed, DCM is frequently encountered. Indeed, some converters are purposely designed to operate in DCM for all loads.

The properties of converters change radically in the discontinuous conduction mode. The conversion ratio M becomes load-dependent, and the output impedance is increased. Control of the output may be lost when the load is removed. We will see in a later chapter that the converter dynamics are also significantly altered.

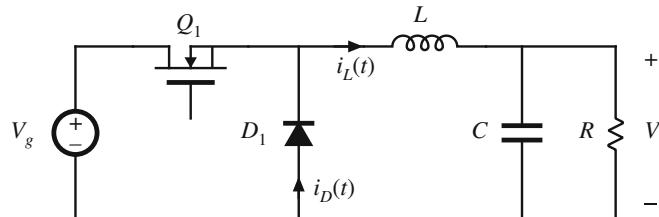
In this chapter, the origins of the discontinuous conduction mode are explained, and the mode boundary is derived. Techniques for solution of the converter waveforms and output voltage are also described. The principles of inductor volt-second balance and capacitor charge balance must always be true in steady state, regardless of the operating mode. However, application of the small-ripple approximation requires some care, since the inductor current ripple (or one of the inductor current or capacitor voltage ripples) is not small.

Buck and boost converters are solved as examples. Characteristics of the basic buck, boost, and buck-boost converters are summarized in tabular form.

5.1 Origin of the Discontinuous Conduction Mode, and Mode Boundary

Let us consider how the inductor and switch current waveforms change as the load power is reduced. Let us use the buck converter (Fig. 5.1) as a simple example. The inductor current $i_L(t)$ and diode current $i_D(t)$ waveforms are sketched in Fig. 5.2 for the continuous conduction

Fig. 5.1 Buck converter example



mode. As described in Chap. 2, the inductor current waveform contains a dc component I , plus switching ripple of peak amplitude Δi_L . During the second subinterval, the diode current is identical to the inductor current. The minimum diode current during the second subinterval is equal to $(I - \Delta i_L)$; since the diode is a single-quadrant switch, operation in the continuous conduction mode requires that this current remain positive. As shown in Chap. 2, the inductor current dc component I is equal to the load current:

$$I = \frac{V}{R} \quad (5.1)$$

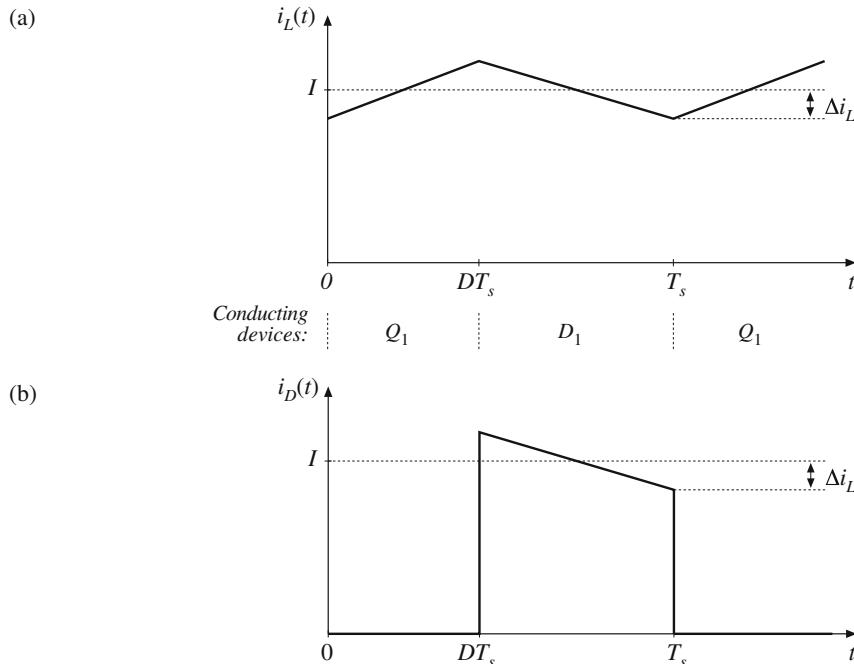


Fig. 5.2 Buck converter waveforms in the continuous conduction mode: (a) inductor current $i_L(t)$, (b) diode current $i_D(t)$

since no dc current flows through capacitor C . It can be seen that I depends on the load resistance R . The switching ripple peak amplitude is

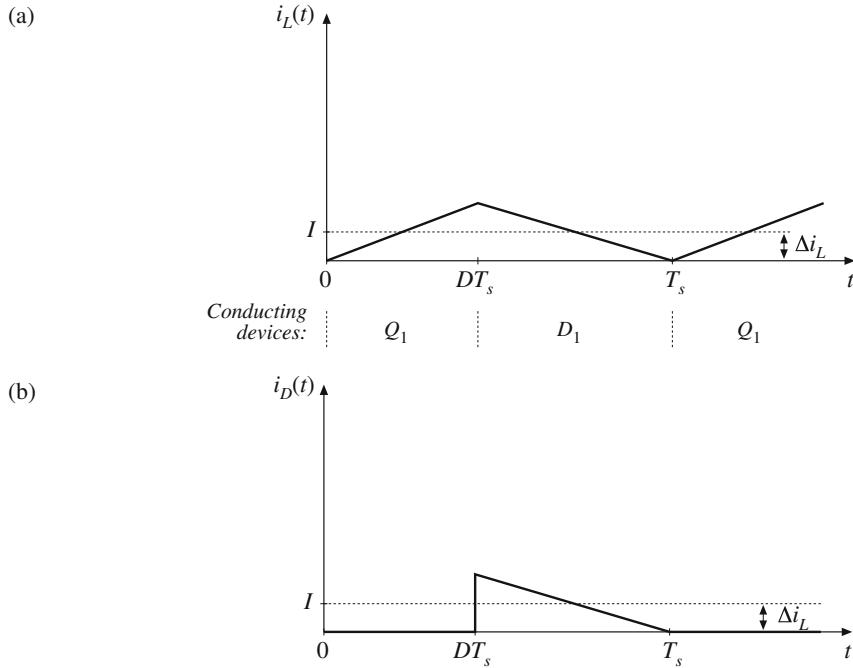


Fig. 5.3 Buck converter waveforms at the boundary between the continuous and discontinuous conduction modes: (a) inductor current $i_L(t)$, (b) diode current $i_D(t)$

$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD' T_s}{2L} \quad (5.2)$$

The ripple magnitude depends on the applied voltage ($V_g - V$), on the inductance L , and on the transistor conduction time DT_s . But it does not depend on the load resistance R . The inductor current ripple magnitude varies with the applied voltages rather than the applied currents.

Suppose now that the load resistance R is increased, so that the dc load current is decreased. The dc component of inductor current I will then decrease, but the ripple magnitude Δi_L will remain unchanged. If we continue to increase R , eventually the point is reached where $I = \Delta i_L$, illustrated in Fig. 5.3. It can be seen that the inductor current $i_L(t)$ and the diode current $i_D(t)$ are both zero at the end of the switching period. Yet the load current is positive and nonzero.

What happens if we continue to increase the load resistance R ? The diode current cannot be negative; therefore, the diode must become reverse-biased before the end of the switching period. As illustrated in Fig. 5.4, there are now three subintervals during each switching period T_s . During the first subinterval of length $D_1 T_s$ the transistor conducts, and the diode conducts during the second subinterval of length $D_2 T_s$. At the end of the second subinterval the diode current reaches zero, and for the remainder of the switching period neither the transistor nor the diode conduct. The converter operates in the discontinuous conduction mode.

Figure 5.3 suggests a way to find the boundary between the continuous and discontinuous conduction modes. It can be seen that, for this buck converter example, the diode current is positive over the entire interval $DT_s < t < T_s$ provided that $I > \Delta i_L$. Hence, the conditions for operation in the continuous and discontinuous conduction modes are

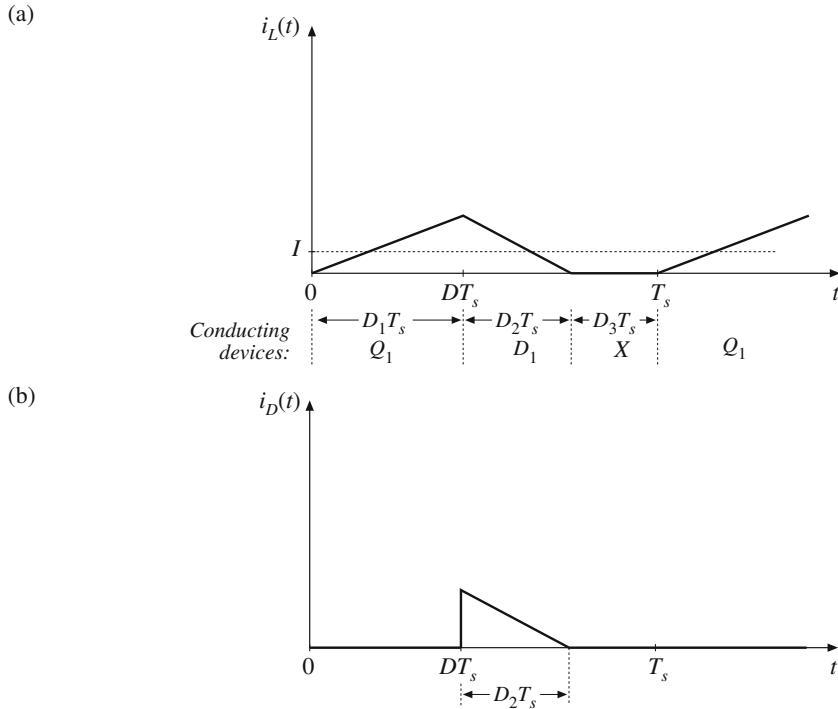


Fig. 5.4 Buck converter waveforms in the discontinuous conduction mode: (a) inductor current $i_L(t)$, (b) diode current $i_D(t)$

$$I > \Delta i_L \text{ for CCM} \quad (5.3)$$

$$I < \Delta i_L \text{ for DCM}$$

where I and Δi_L are found assuming that the converter operates in the continuous conduction mode. Insertion of Eqs. (5.1) and (5.2) into Eq. (5.3) yields the following condition for operation in the discontinuous conduction mode:

$$\frac{DV_g}{R} < \frac{DD'T_sV_g}{2L} \quad (5.4)$$

Simplification leads to

$$\frac{2L}{RT_s} < D' \quad (5.5)$$

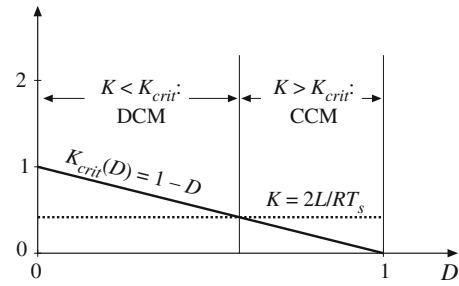
This can also be expressed

$$K < K_{crit}(D) \text{ for DCM} \quad (5.6)$$

where

$$K = \frac{2L}{RT_s} \quad \text{and} \quad K_{crit}(D) = D'$$

Fig. 5.5 Buck converter $K_{crit}(D)$ vs. D . The converter operates in CCM when $K > K_{crit}$, and in DCM when $K < K_{crit}$



The dimensionless parameter K is a measure of the tendency of a converter to operate in the discontinuous conduction mode. Large values of K lead to continuous mode operation, while small values lead to the discontinuous mode for some values of duty cycle. The critical value of K at the boundary between modes, $K_{crit}(D)$, is a function of duty cycle, and is equal to D' for the buck converter.

The critical value $K_{crit}(D)$ is plotted vs. duty cycle D in Fig. 5.5. An arbitrary choice of K is also illustrated. For the values shown, it can be seen that the converter operates in DCM at low duty cycle, and in CCM at high duty cycle. Figure 5.6 illustrates what happens with heavier loading. The load resistance R is reduced in value, such that K is larger. If K is greater than one, then the converter operates in the continuous conduction mode for all duty cycles.

It is natural to express the mode boundary in terms of the load resistance R , rather than the dimensionless parameter K . Equation (5.6) can be rearranged to directly expose the dependence of the mode boundary on the load resistance:

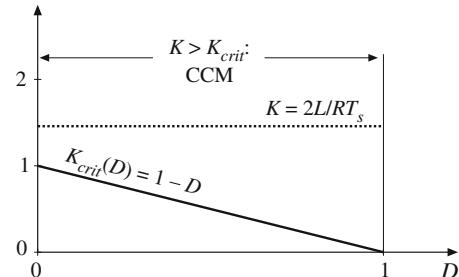
$$\begin{aligned} R &< R_{crit}(D) \text{ for CCM} \\ R &> R_{crit}(D) \text{ for DCM} \end{aligned} \quad (5.7)$$

where

$$R_{crit}(D) = \frac{2L}{D'T_s}$$

So the converter enters the discontinuous conduction mode when the load resistance R exceeds the critical value R_{crit} . This critical value depends on the inductance, the switching period, and the duty cycle. Note that, since $D' \leq 1$, the minimum value of R_{crit} is $2L/T_s$. Therefore, if $R < 2L/T_s$, then the converter will operate in the continuous conduction mode for all duty cycles.

Fig. 5.6 Comparison of K with $K_{crit}(D)$, for a larger value of K . Since $K > 1$, the converter operates in CCM for all D



These results can be applied to loads that are not pure linear resistors. An effective load resistance R is defined as the ratio of the dc output voltage to the dc load current: $R = V/I$. This effective load resistance is then used in the above equations.

Table 5.1 CCM-DCM mode boundaries for the buck, boost, and buck-boost converters

Converter	$K_{crit}(D)$	$\max_{0 \leq D \leq 1} (K_{crit})$	$R_{crit}(D)$	$\min_{0 \leq D \leq 1} (R_{crit})$
Buck	$(1 - D)$	1	$\frac{2L}{(1 - D)T_s}$	$\frac{2}{T_s} \frac{L}{R}$
Boost	$D(1 - D)^2$	$\frac{4}{27}$	$\frac{2L}{D(1 - D)^2 T_s}$	$\frac{27}{2} \frac{L}{T_s}$
Buck-boost	$(1 - D)^2$	1	$\frac{2L}{(1 - D)^2 T_s}$	$\frac{2}{T_s} \frac{L}{R}$

A similar mode boundary analysis can be performed for other converters. The boost converter is analyzed in Sect. 5.3, while analysis of the buck-boost converter is left as a homework problem. The results are listed in Table 5.1, for the three basic dc-dc converters. In each case, the dimensionless parameter K is defined as $K = 2L/RT_s$, and the mode boundary is given by

$$\begin{aligned} K > K_{crit}(D) \quad &\text{or} \quad R < R_{crit}(D) \text{ for CCM} \\ K < K_{crit}(D) \quad &\text{or} \quad R > R_{crit}(D) \text{ for DCM} \end{aligned} \quad (5.8)$$

5.2 Analysis of the Conversion Ratio $M(D, K)$

With a few modifications, the same techniques and approximations developed in Chap. 2 for the steady-state analysis of the continuous conduction mode may be applied to the discontinuous conduction mode.

- (a) *Inductor volt-second balance.* The dc component of the voltage applied to an inductor must be zero:

$$\langle v_L \rangle = \frac{1}{T_s} \int_0^{T_s} v_L(t) dt = 0 \quad (5.9)$$

- (b) *Capacitor charge balance.* The dc component of current applied to a capacitor must be zero:

$$\langle i_C \rangle = \frac{1}{T_s} \int_0^{T_s} i_C(t) dt = 0 \quad (5.10)$$

These principles must be true for any circuit that operates in steady state, regardless of the operating mode.

- (c) *The linear-ripple approximation.* Care must be used when employing the linear-ripple approximation in the discontinuous conduction mode.

- (i) *Output capacitor voltage ripple.* Regardless of the operating mode, it is required that the output voltage ripple be small. Hence, for a well-designed converter operating in the discontinuous conduction mode, the peak output voltage ripple Δv should be much smaller in magnitude than the output voltage dc component V . So the linear-ripple approximation applies to the output voltage waveform:

$$v(t) \approx V \quad (5.11)$$

- (ii) *Inductor current ripple.* By definition, the inductor current ripple is not small in the discontinuous conduction mode. Indeed, Eq. (5.3) states that the inductor current ripple Δi_L is greater in magnitude than the dc component I . So neglecting the inductor current ripple leads to inaccurate results. In other converters, several inductor currents, or a capacitor voltage, may contain large switching ripple which should not be neglected.

The equations necessary for solution of the voltage conversion ratio can be obtained by invoking volt-second balance for each inductor voltage, and charge balance for each capacitor current, in the network. The switching ripple is ignored in the output capacitor voltage, but the inductor current switching ripple must be accounted for in this buck converter example.

Let us analyze the conversion ratio $M = V/V_g$ of the buck converter of Eq. (5.1). When the transistor conducts, for $0 < t < D_1 T_s$, the converter circuit reduces to the network of Fig. 5.7a. The inductor voltage and capacitor current are given by

$$\begin{aligned} v_L(t) &= V_g - v(t) \\ i_C(t) &= i_L(t) - \frac{v(t)}{R} \end{aligned} \quad (5.12)$$

By making the linear-ripple approximation, to ignore the output capacitor voltage ripple, one obtains

$$\begin{aligned} v_L(t) &\approx V_g - V \\ i_C(t) &\approx i_L(t) - \frac{V}{R} \end{aligned} \quad (5.13)$$

Note that the inductor current ripple has not been ignored.

The diode conducts during subinterval 2, $D_1 T_s < t < (D_1 + D_2) T_s$. The circuit then reduces to Fig. 5.7b. The inductor voltage and capacitor current are given by

$$\begin{aligned} v_L(t) &= -v(t) \\ i_C(t) &= i_L(t) - \frac{v(t)}{R} \end{aligned} \quad (5.14)$$

By neglecting the ripple in the output capacitor voltage, one obtains

$$\begin{aligned} v_L(t) &\approx -V \\ i_C(t) &\approx i_L(t) - \frac{V}{R} \end{aligned} \quad (5.15)$$

The diode becomes reverse-biased at time $t = (D_1 + D_2) T_s$. The circuit is then as shown in Fig. 5.7c, with both transistor and diode in the off state. The inductor voltage and inductor

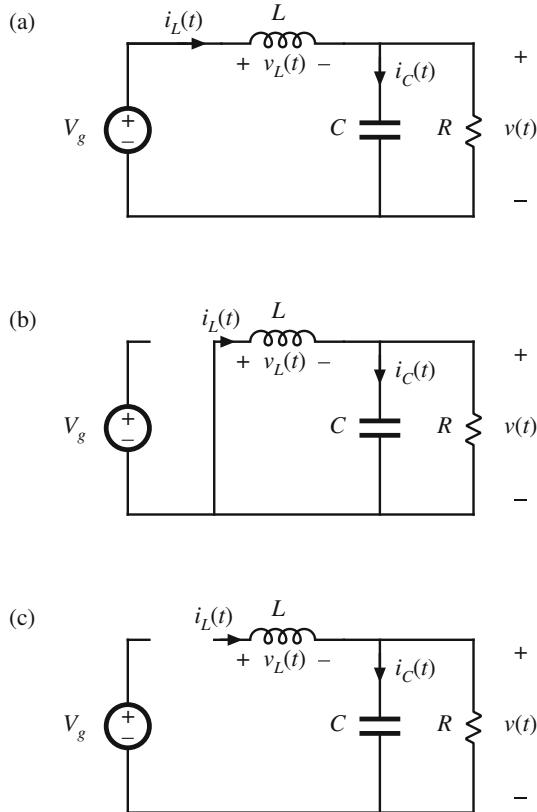


Fig. 5.7 Buck converter circuits for operation in the discontinuous conduction mode: (a) during subinterval 1, (b) during subinterval 2, (c) during subinterval 3

current are both zero for the remainder of the switching period $(D_1 + D_2)T_s < t < T_s$. The network equations for the third subinterval are given by

$$\begin{aligned} v_L &= 0, \quad i_L = 0 \\ i_C(t) &= i_L(t) - \frac{v(t)}{R} \end{aligned} \quad (5.16)$$

Note that the inductor current is constant and equal to zero during the third subinterval, and therefore the inductor voltage must also be zero in accordance with the relationship $v_L(t) = L di_L(t)/dt$. In practice, parasitic ringing is observed during this subinterval. This ringing occurs owing to the resonant circuit formed by the inductor and the semiconductor device capacitances, and typically has little influence on the converter steady-state properties. Again ignoring the output capacitor voltage ripple, one obtains

$$\begin{aligned} v_L(t) &= 0 \\ i_C(t) &= -\frac{V}{R} \end{aligned} \quad (5.17)$$

Equations (5.13), (5.15), and (5.17) can now be used to plot the inductor voltage waveform as in Fig. 5.8. According to the principle of inductor volt-second balance, the dc component of this waveform must be zero. Since the waveform is rectangular, its dc component (or average value)

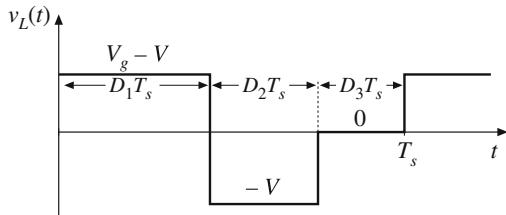


Fig. 5.8 Inductor voltage waveform $v_L(t)$, buck converter operating in discontinuous conduction mode

is easily evaluated:

$$\langle v_L(t) \rangle = D_1(V_g - V) + D_2(-V) + D_3(0) = 0 \quad (5.18)$$

Solution for the output voltage yields

$$V = V_g \frac{D_1}{D_1 + D_2} \quad (5.19)$$

The transistor duty cycle D (which coincides with the subinterval 1 duty cycle D_1) is the control input to the converter, and can be considered known. But the subinterval 2 duty cycle D_2 is unknown, and hence another equation is needed to eliminate D_2 and solve for the output voltage V .

The second equation is obtained by use of capacitor charge balance. The connection of the capacitor to its adjacent components is detailed in Fig. 5.9. The node equation of this network is

$$i_L(t) = i_C(t) + \frac{v(t)}{R} \quad (5.20)$$

By capacitor charge balance, the dc component of capacitor current must be zero:

$$\langle i_C \rangle = 0 \quad (5.21)$$

Therefore, the dc load current must be supplied entirely by the other elements connected to the node. In particular, for the case of the buck converter, the dc component of inductor current must be equal to the dc load current:

$$\langle i_L \rangle = \frac{V}{R} \quad (5.22)$$

So we need to compute the dc component of the inductor current.

Since the inductor current ripple is not small, determination of the inductor current dc component requires that we examine the current waveform in detail. The inductor current waveform is sketched in Fig. 5.10. The current begins the switching period at zero, and increases during

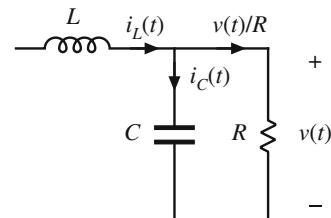


Fig. 5.9 Connection of the output capacitor to adjacent components in the buck converter

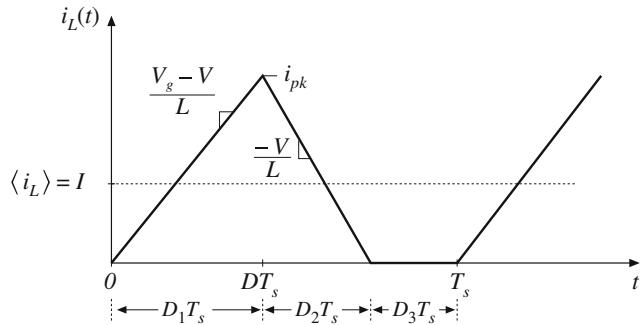


Fig. 5.10 Inductor current waveform $i_L(t)$, buck converter operating in discontinuous conduction mode

the first subinterval with a constant slope, given by the applied voltage divided by the inductance. The peak inductor current i_{pk} is equal to the constant slope, multiplied by the length of the first subinterval:

$$i_L(D_1T_s) = i_{pk} = \frac{V_g - V}{L} D_1 T_s \quad (5.23)$$

The dc component of the inductor current is again the average value:

$$\langle i_L \rangle = \frac{1}{T_s} \int_0^{T_s} i_L(t) dt \quad (5.24)$$

The integral, or area under the $i_L(t)$ curve, is the area of the triangle having height i_{pk} and base dimension $(D_1 + D_2)T_s$. Use of the triangle area formula yields

$$\int_0^{T_s} i_L(t) dt = \frac{1}{2} i_{pk} (D_1 + D_2) T_s \quad (5.25)$$

Substitution of Eqs. (5.23) and (5.25) into Eq. (5.24) leads to

$$\langle i_L \rangle = (V_g - V) \left(\frac{D_1 T_s}{2L} \right) (D_1 + D_2) \quad (5.26)$$

Finally, by equating this result to the dc load current, according to Eq. (5.22), we obtain

$$\frac{V}{R} = \frac{D_1 T_s}{2L} (D_1 + D_2) (V_g - V) \quad (5.27)$$

Thus, we have two unknowns, V and D_2 , and we have two equations. The first equation, Eq. (5.19), was obtained by inductor volt-second balance, while the second equation, Eq. (5.27), was obtained using capacitor charge balance. Elimination of D_2 from the two equations, and solution for the voltage conversion ratio $M(D_1, K) = V/V_g$, yields

$$\frac{V}{V_g} = \frac{2}{1 + \sqrt{1 + \frac{4K}{D_1^2}}} \quad (5.28)$$

where $K = 2L/RT_s$
valid for $K < K_{crit}$

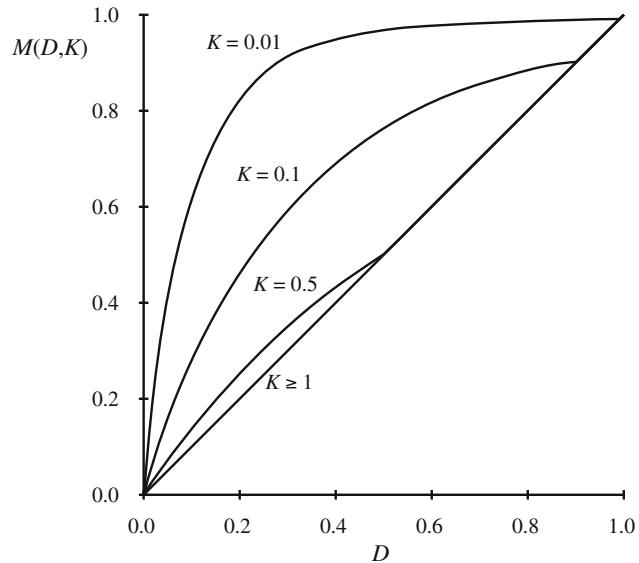


Fig. 5.11 Voltage conversion ratio $M(D, K)$, buck converter

This is the solution of the buck converter operating in discontinuous conduction mode.

The complete buck converter characteristics, including both continuous and discontinuous conduction modes, are therefore

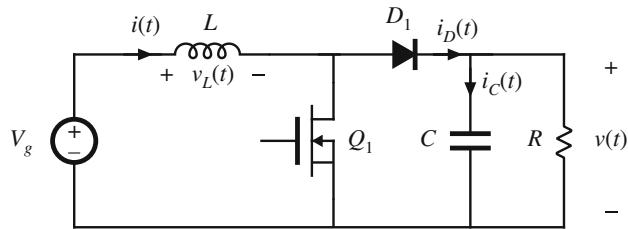
$$M = \begin{cases} D & \text{for } K > K_{crit} \\ \frac{2}{1 + \sqrt{1 + \frac{4K}{D^2}}} & \text{for } K < K_{crit} \end{cases} \quad (5.29)$$

where the transistor duty cycle D is identical to the subinterval 1 duty cycle D_1 of the above derivation. These characteristics are plotted in Fig. 5.11, for several values of K . It can be seen that the effect of the discontinuous conduction mode is to cause the output voltage to increase. As K tends to zero (the unloaded case), M tends to unity for all nonzero D . The characteristics are continuous, and Eq. (5.28) intersects the CCM characteristic $M = D$ at the mode boundary.

5.3 Boost Converter Example

As a second example, consider the boost converter of Fig. 5.12. Let us determine the boundary between modes, and solve for the conversion ratio in the discontinuous conduction mode. Behavior of the boost converter operating in the continuous conduction mode was analyzed previously, in Sect. 2.3, and expressions for the inductor current dc component I and ripple peak magnitude Δi_L were found.

When the diode conducts, its current is identical to the inductor current $i_L(t)$. As can be seen from Fig. 2.18, the minimum value of the inductor current during the diode conduction subinterval $DT_s < t < T_s$ is $(I - \Delta i_L)$. If this minimum current is positive, then the diode is

**Fig. 5.12** Boost converter example

forward-biased for the entire subinterval $DT_s < t < T_s$, and the converter operates in the continuous conduction mode. So the conditions for operation of the boost converter in the continuous and discontinuous conduction modes are

$$\begin{aligned} I &> \Delta i_L \text{ for CCM} \\ I &< \Delta i_L \text{ for DCM} \end{aligned} \quad (5.30)$$

which is identical to the results for the buck converter. Substitution of the CCM solutions for I and Δi_L , Eqs. (2.39) and (2.43), yields

$$\frac{V_g}{D'^2 R} > \frac{DT_s V_g}{2L} \quad \text{for CCM} \quad (5.31)$$

This equation can be rearranged to obtain

$$\frac{2L}{RT_s} > DD'^2 \quad \text{for CCM} \quad (5.32)$$

which is in the standard form

$$\begin{aligned} K &> K_{crit}(D) \text{ for CCM} \\ K &< K_{crit}(D) \text{ for DCM} \end{aligned} \quad (5.33)$$

where

$$K = \frac{2L}{RT_s} \text{ and } K_{crit}(D) = DD'^2$$

The conditions for operation in the continuous or discontinuous conduction modes are of similar form to those for the buck converter; however, the critical value $K_{crit}(D)$ is a different function of the duty cycle D . The dependence of $K_{crit}(D)$ on the duty cycle D is plotted in Fig. 5.13. $K_{crit}(D)$ is zero at $D = 0$ and at $D = 1$, and has a maximum value of $4/27$ at $D = 1/3$. Hence, if K is greater than $4/27$, then the converter operates in the continuous conduction mode for all D . Figure 5.14 illustrates what happens when K is less than $4/27$. The converter then operates in the discontinuous conduction mode for some intermediate range of values of D near $D = 1/3$. But the converter operates in the continuous conduction mode near $D = 0$ and $D = 1$. Unlike the buck converter, the boost converter must operate in the continuous conduction mode near $D = 0$ because the ripple magnitude approaches zero while the dc component I does not.

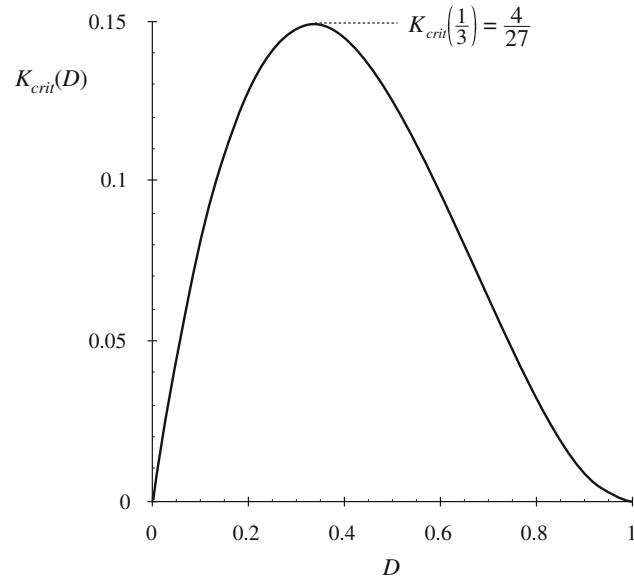


Fig. 5.13 Boost converter $K_{crit}(D)$ vs. D

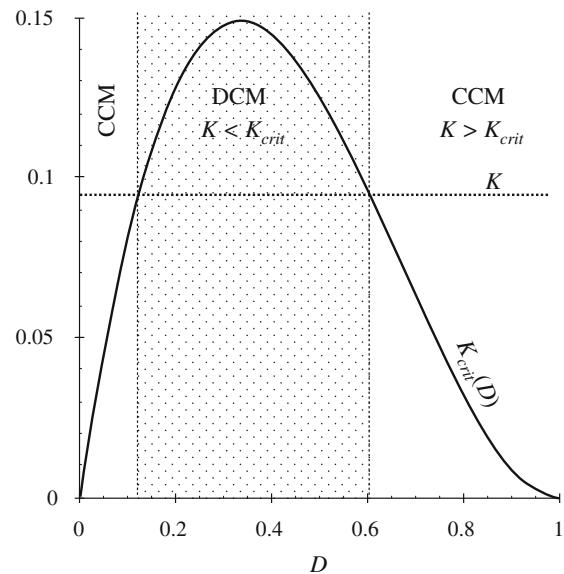


Fig. 5.14 Comparison of K with $K_{crit}(D)$

Next, let us analyze the conversion ratio $M = V/V_g$ of the boost converter. When the transistor conducts, for the subinterval $0 < t < D_1 T_s$, the converter circuit reduces to the circuit of Fig. 5.15a. The inductor voltage and capacitor current are given by

$$\begin{aligned} v_L(t) &= V_g & (5.34) \\ i_C(t) &= -\frac{v(t)}{R} \end{aligned}$$

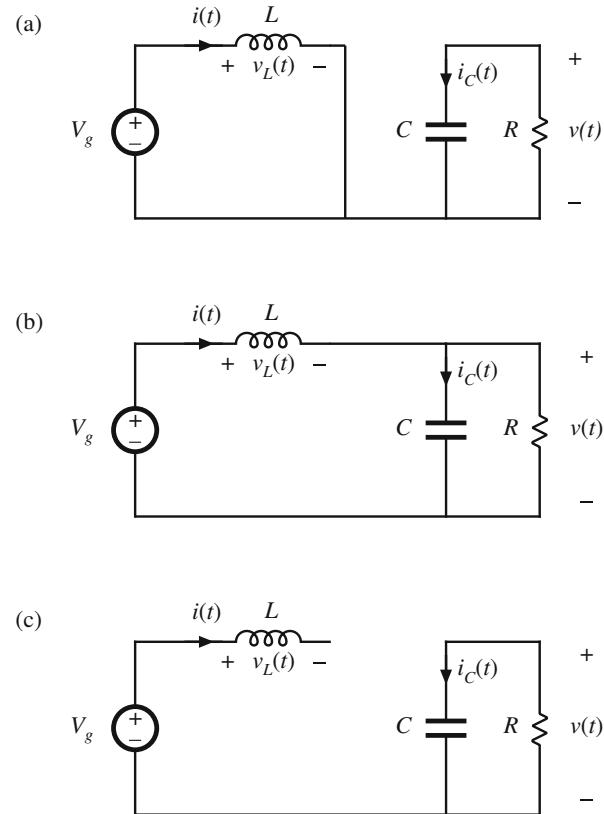


Fig. 5.15 Boost converter circuits for operation in the discontinuous conduction mode: (a) during subinterval 1, $0 < t < D_1 T_s$, (b) during subinterval 2, $D_1 T_s < t < (D_1 + D_2) T_s$, (c) during subinterval 3, $(D_1 + D_2) T_s < t < T_s$

Use of the linear-ripple approximation, to ignore the output capacitor voltage ripple, leads to

$$\begin{aligned} v_L(t) &\approx V_g \\ i_C(t) &\approx -\frac{V}{R} \end{aligned} \quad (5.35)$$

During the second subinterval $D_1 T_s < t < (D_1 + D_2) T_s$, the diode conducts. The circuit then reduces to Fig. 5.15b. The inductor voltage and capacitor current are given by

$$\begin{aligned} v_L(t) &= V_g - v(t) \\ i_C(t) &= i(t) - \frac{v(t)}{R} \end{aligned} \quad (5.36)$$

Neglect of the output capacitor voltage ripple yields

$$\begin{aligned} v_L(t) &\approx V_g - V \\ i_C(t) &\approx i(t) - \frac{V}{R} \end{aligned} \quad (5.37)$$

The inductor current ripple has not been neglected.

During the third subinterval, $(D_1 + D_2)T_s < t < T_s$, both transistor and diode are in the off state, and Fig. 5.15c is obtained. The network equations are

$$\begin{aligned} v_L &= 0, \quad i = 0 \\ i_C(t) &= -\frac{v(t)}{R} \end{aligned} \quad (5.38)$$

Use of the small-ripple approximation yields

$$\begin{aligned} v_L(t) &= 0 \\ i_C(t) &= -\frac{V}{R} \end{aligned} \quad (5.39)$$

Equations (5.35), (5.37), and (5.39) are now used to sketch the inductor voltage waveform as in Fig. 5.16. By volt-second balance, this waveform must have zero dc component when the converter operates in steady state. By equating the average value of this $v_L(t)$ waveform to zero, one obtains

$$D_1 V_g + D_2(V_g - V) + D_3(0) = 0 \quad (5.40)$$

Solution for the output voltage V yields

$$V = \frac{D_1 + D_2}{D_2} V_g \quad (5.41)$$

The diode duty cycle D_2 is again an unknown, and so a second equation is needed for elimination of D_2 before the output voltage V can be found.

We can again use capacitor charge balance to obtain the second equation. The connection of the output capacitor to its adjacent components is detailed in Fig. 5.17. Unlike the buck converter, the diode in the boost converter is connected to the output node. The node equation of Fig. 5.17 is

$$i_D(t) = i_C(t) + \frac{v(t)}{R} \quad (5.42)$$

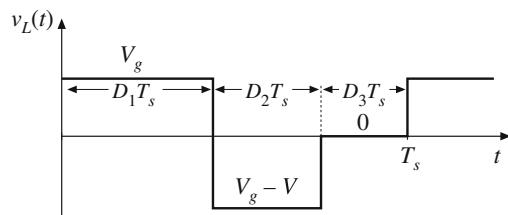


Fig. 5.16 Inductor voltage waveform $v_L(t)$, boost converter operating in discontinuous conduction mode

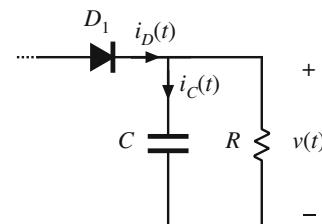


Fig. 5.17 Connection of the output capacitor to adjacent components in the boost converter

where $i_D(t)$ is the diode current. By capacitor charge balance, the capacitor current $i_C(t)$ must have zero dc component in steady state. Therefore, the diode current dc component $\langle i_D \rangle$ must be equal to the dc component of the load current:

$$\langle i_D \rangle = \frac{V}{R} \quad (5.43)$$

So we need to sketch the diode current waveform, and find its dc component.

The waveforms of the inductor current $i(t)$ and diode current $i_D(t)$ are illustrated in Fig. 5.18. The inductor current begins at zero, and rises to a peak value i_{pk} during the first subinterval. This peak value i_{pk} is equal to the slope V_g/L , multiplied by the length of the first subinterval, $D_1 T_s$:

$$i_{pk} = \frac{V_g}{L} D_1 T_s \quad (5.44)$$

The diode conducts during the second subinterval, and the inductor current then decreases to zero, where it remains during the third subinterval. The diode current $i_D(t)$ is identical to the inductor current $i(t)$ during the second subinterval. During the first and third subintervals, the diode is reverse-biased and hence $i_D(t)$ is zero.

The dc component of the diode current, $\langle i_D \rangle$, is

$$\langle i_D \rangle = \frac{1}{T_s} \int_0^{T_s} i_D(t) dt \quad (5.45)$$

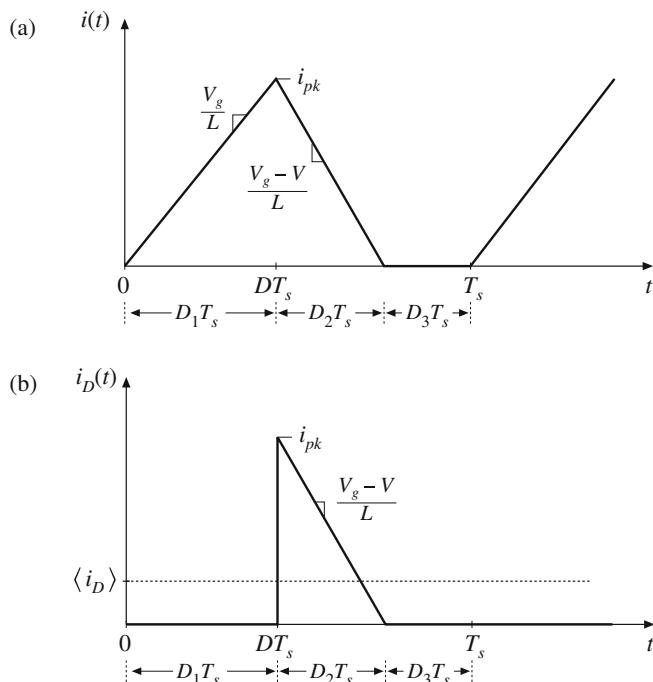


Fig. 5.18 Boost converter waveforms in the discontinuous conduction mode: (a) inductor current $i(t)$, (b) diode current $i_D(t)$

The integral is the area under the $i_D(t)$ waveform. As illustrated in Fig. 5.18b, this area is the area of the triangle having peak value i_{pk} and base dimension $D_2 T_s$:

$$\int_0^{T_s} i_D(t) dt = \frac{1}{2} i_{pk} D_2 T_s \quad (5.46)$$

Substitution of Eqs. (5.44) and (5.46) into Eq. (5.45) leads to the following expression for the dc component of the diode current:

$$\langle i_D \rangle = \frac{1}{T_s} \left(\frac{1}{2} i_{pk} D_2 T_s \right) = \frac{V_g D_1 D_2 T_s}{2L} \quad (5.47)$$

By equating this expression to the dc load current as in Eq. (5.43), one obtains the final result

$$\frac{V_g D_1 D_2 T_s}{2L} = \frac{V}{R} \quad (5.48)$$

So now we have two unknowns, V and D_2 . We have two equations: Eq. (5.41) obtained via inductor volt-second balance, and Eq. (5.48) obtained using capacitor charge balance. Let us now eliminate D_2 from this system of equations, and solve for the output voltage V . Solution of Eq. (5.41) for D_2 yields

$$D_2 = D_1 \frac{V_g}{V - V_g} \quad (5.49)$$

By inserting this result into Eq. (5.48), and rearranging terms, one obtains the following quadratic equation:

$$V^2 - VV_g - \frac{V_g^2 D_1^2}{K} = 0 \quad (5.50)$$

Use of the quadratic formula yields

$$\frac{V}{V_g} = \frac{1 \pm \sqrt{1 + \frac{4D_1^2}{K}}}{2} \quad (5.51)$$

The quadratic equation has two roots: one of the roots of Eq. (5.51) is positive, while the other is negative. We already know that the output voltage of the boost converter should be positive, and indeed, from Eq. (5.41), it can be seen that V/V_g must be positive since the duty cycles D_1 and D_2 are positive. So we should select the positive root:

$$\frac{V}{V_g} = M(D_1, K) = \frac{1 + \sqrt{1 + \frac{4D_1^2}{K}}}{2} \quad (5.52)$$

where $K = 2L/RT_s$

valid for $K < K_{crit}(D)$

This is the solution of the boost converter operating in the discontinuous conduction mode.

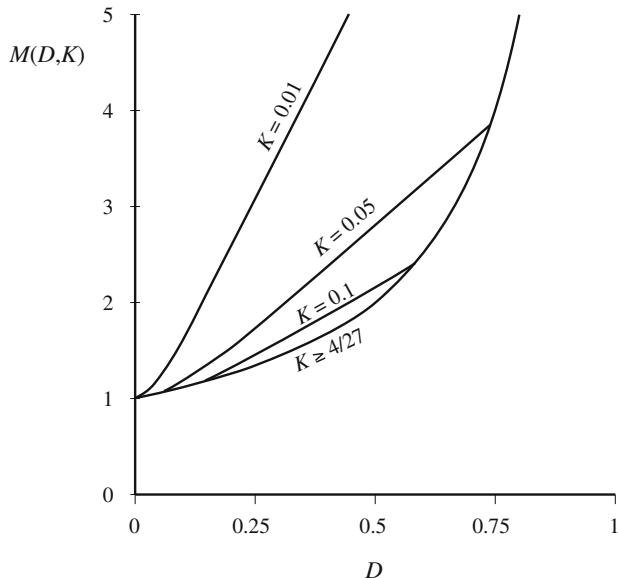


Fig. 5.19 Voltage conversion ratio $M(D, K)$ of the boost converter, including both continuous and discontinuous conduction modes

The complete boost converter characteristics, including both continuous and discontinuous conduction modes, are

$$M = \begin{cases} \frac{1}{1-D} & \text{for } K > K_{crit} \\ \frac{1 + \sqrt{1 + \frac{4D^2}{K}}}{2} & \text{for } K < K_{crit} \end{cases} \quad (5.53)$$

These characteristics are plotted in Fig. 5.19, for several values of K . As in the buck converter, the effect of the discontinuous conduction mode is to cause the output voltage to increase. The DCM portions of the characteristics are nearly linear, and can be approximated as

$$M \approx \frac{1}{2} + \frac{D}{\sqrt{K}} \quad (5.54)$$

5.4 Summary of Results and Key Points

The characteristics of the basic buck, boost, and buck-boost are summarized in Table 5.2. Expressions for $K_{crit}(D)$, as well as for the solutions of the dc conversion ratios in CCM and DCM, and for the DCM diode conduction duty cycle D_2 , are given.

The dc conversion ratios of the DCM buck, boost, and buck-boost converters are compared in Fig. 5.20. The buck-boost characteristic is a line with slope $1/\sqrt{K}$. The characteristics of the buck and the boost converters are both asymptotic to this line, as well as to the line $M = 1$. Hence, when operated deeply into the discontinuous conduction mode, the boost converter characteristic becomes nearly linear with slope $1/\sqrt{K}$, especially at high duty cycle. Likewise, the buck converter characteristic becomes nearly linear with the same slope, when operated deeply into discontinuous conduction mode at low duty cycle.

Table 5.2 Summary of CCM-DCM characteristics for the buck, boost, and buck-boost converters

Converter	$K_{crit}(D)$	DCM $M(D, K)$	DCM $D_2(D, K)$	CCM $M(D)$
Buck	$(1 - D)$	$\frac{2}{1 + \sqrt{1 + 4K/D^2}}$	$\frac{K}{D}M(D, K)$	D
Boost	$D(1 - D)^2$	$\frac{1 + \sqrt{1 + 4D^2/K}}{2}$	$\frac{K}{D}M(D, K)$	$\frac{1}{1 - D}$
Buck-boost	$(1 - D)^2$	$-\frac{D}{\sqrt{K}}$	\sqrt{K}	$-\frac{D}{1 - D}$

with $K = 2L/RT_s$. DCM occurs for $K < K_{crit}$.

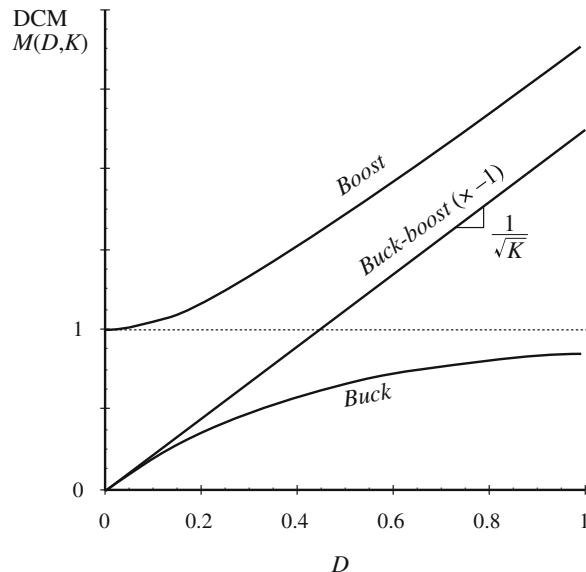


Fig. 5.20 Comparison of the dc conversion ratios of the buck-boost, buck, and boost converters operated in the discontinuous conduction mode

The following are the key points of this chapter:

1. The discontinuous conduction mode occurs in converters containing current- or voltage-unidirectional switches, when the inductor current or capacitor voltage ripple is large enough to cause the switch current or voltage to reverse polarity.
2. Conditions for operation in the discontinuous conduction mode can be found by determining when the inductor current or capacitor voltage ripples and dc components cause the switch on state current or off state voltage to reverse polarity.
3. The dc conversion ratio M of converters operating in the discontinuous conduction mode can be found by application of the principles of inductor volt-second and capacitor charge balance.
4. Extra care is required when applying the small-ripple approximation. Some waveforms, such as the output voltage, should have small ripple which can be neglected. Other waveforms, such as one or more inductor currents, may have large ripple that cannot be ignored.

5. The characteristics of a converter changes significantly when the converter enters DCM. The output voltage becomes load-dependent, resulting in an increase in the converter output impedance.

PROBLEMS

- 5.1** The elements of the buck-boost converter of Fig. 5.21 are ideal: all losses may be ignored. Your results for parts (a) and (b) should agree with Table 5.2.

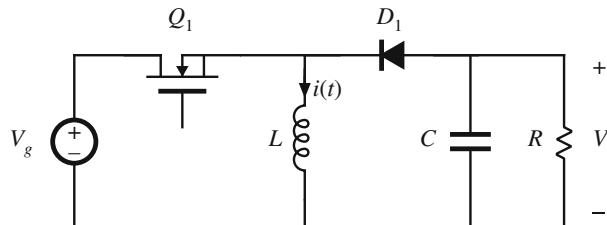


Fig. 5.21 Buck-boost converter of Problems 5.1, 5.2, and 5.16

- (a) Show that the converter operates in discontinuous conduction mode when $K < K_{crit}$, and derive expressions for K and K_{crit} .
- (b) Derive an expression for the dc conversion ratio V/V_g of the buck-boost converter operating in discontinuous conduction mode.
- (c) For $K = 0.1$, plot V/V_g over the entire range $0 \leq D \leq 1$.
- (d) Sketch the inductor voltage and current waveforms for $K = 0.1$ and $D = 0.3$. Label salient features.
- (e) What happens to V at no load ($R \rightarrow \infty$)? Explain why, physically.
- 5.2** For this problem, the buck-boost converter of Fig. 5.21 employs a diode having forward voltage drop V_D . All other elements should be modeled as ideal. Express your results in terms of the transistor duty cycle D , the input voltage V_g , the diode forward voltage drop V_D , and the dimensionless parameter $K = 2L/RT_s$ where T_s is the switching period.
- (a) Derive an expression for the conditions under which this converter operates in the discontinuous conduction mode. Express your result in the form $K < K_{crit}$, and give an expression for K_{crit} .
- (b) Derive an equation for the steady-state output voltage V . Manipulate your equation into the form
- $$V = f(D, K, V_g, V_D)$$
- 5.3** A certain buck converter contains a synchronous rectifier, as described in Sect. 4.1.5.
- (a) Does this converter operate in the discontinuous conduction mode at light load? Explain.
- (b) The load resistance is disconnected ($R \rightarrow \infty$), and the converter is operated with duty cycle 0.5. Sketch the inductor current waveform.

- 5.4** An unregulated dc input voltage V_g varies over the range $35 \text{ V} \leq V_g \leq 70 \text{ V}$. A buck converter reduces this voltage to 28 V; a feedback loop varies the duty cycle as necessary such that the converter output voltage is always equal to 28 V. The load power varies over the range $10 \text{ W} \leq P_{load} \leq 1000 \text{ W}$. The element values are

$$L = 22 \mu\text{H} \quad C = 470 \mu\text{F} \quad f_s = 75 \text{ kHz}$$

Losses may be ignored.

- Over what range of V_g and load current does the converter operate in CCM?
- Determine the maximum and minimum values of the steady-state transistor duty cycle.

- 5.5** The transistors in the converter of Fig. 5.22 are driven by the same gate drive signal, so that they turn on and off in synchronism with duty cycle D .

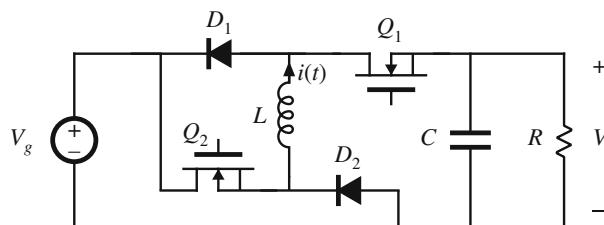


Fig. 5.22 Watkins-Johnson converter of Problem 5.5

- Determine the conditions under which this converter operates in the discontinuous conduction mode, as a function of the steady-state duty ratio D and the dimensionless parameter $K = 2L/RT_s$.
- What happens to your answer to Part (a) for $D < 0.5$?
- Derive an expression for the dc conversion ratio $M(D, K)$. Sketch M vs. D for $K = 10$ and for $K = 0.1$, over the range $0 \leq D \leq 1$.

- 5.6** In the buck converter illustrated in Fig. 5.23, the diode has forward voltage drop V_F . You may model this voltage as being independent of current. All other elements should be modeled as ideal. In this problem, you will show how this diode drop changes the equations of the discontinuous conduction mode.

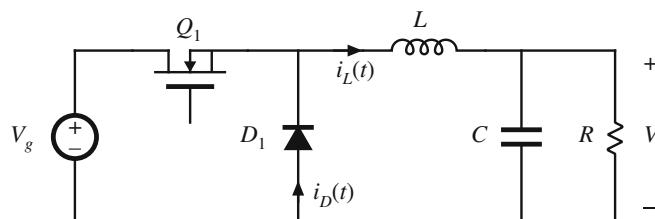


Fig. 5.23 Buck converter of Problem 5.6

- Derive the conditions under which the converter operates in the discontinuous conduction mode. Express your result in terms of the quantities $K = 2L/RT_s$ and K_{crit} . Note that K_{crit} may now depend not only on D , but also on other element values.

- (b) Derive closed-form analytical expressions for the conversion ratio $M = V/V_g$ for both continuous and discontinuous conduction modes.
 (c) The element values are

$$\begin{aligned}V_D &= 0.5 \text{ V} & f_s &= 250 \text{ kHz} \\V_g &= 5 \text{ V} & R &= 4 \Omega \\L_1 &= 2.2 \mu\text{H}\end{aligned}$$

C is large. Plot the conversion ratio $M = V/V_g$ for the entire range $0 \leq D \leq 1$.

- (d) What happens near $D = 0$? Does the converter operate in CCM or DCM? Compare with your result from part (a).

5.7 DCM mode boundary analysis of the Ćuk converter of Fig. 5.24. The capacitor voltage ripples are small.

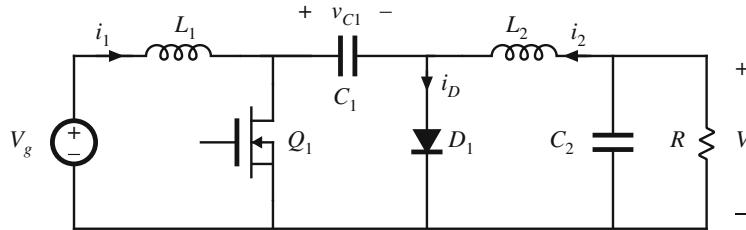


Fig. 5.24 Ćuk converter, Problems 5.7, 5.8, 5.14, and 5.15

- (a) Sketch the diode current waveform for CCM operation. Find its peak value, in terms of the ripple magnitudes Δi_{L1} , Δi_{L2} , and the dc components I_1 and I_2 , of the two inductor currents $i_{L1}(t)$ and $i_{L2}(t)$, respectively.
 (b) Derive an expression for the conditions under which the Ćuk converter operates in the discontinuous conduction mode. Express your result in the form $K < K_{crit}(D)$, and give formulas for K and $K_{crit}(D)$.

5.8 DCM conversion ratio analysis of the Ćuk converter of Fig. 5.24.

- (a) Suppose that the converter operates at the boundary between CCM and DCM, with the following element and parameter values:

$$\begin{aligned}D &= 0.4 & f_s &= 100 \text{ kHz} \\V_g &= 120 \text{ V} & R &= 10 \Omega \\L_1 &= 54 \mu\text{H} & L_2 &= 27 \mu\text{H} \\C_1 &= 47 \mu\text{F} & C_2 &= 100 \mu\text{F}\end{aligned}$$

Sketch the diode current waveform $i_D(t)$, and the inductor current waveforms $i_1(t)$ and $i_2(t)$. Label the magnitudes of the ripples and dc components of these waveforms.

- (b) Suppose next that the converter operates in the discontinuous conduction mode, with a different choice of parameter and element values. Derive an analytical expression for the dc conversion ratio $M(D, K)$.

- (c) Sketch the diode current waveform $i_D(t)$, and the inductor current waveforms $i_1(t)$ and $i_2(t)$, for operation in the discontinuous conduction mode.

5.9 DCM mode boundary analysis of the modified SEPIC of Fig. 5.25 The converter illustrated in Fig. 5.25 is similar to the SEPIC, except that an additional diode is placed in series with the input inductor L_1 . The objective of this problem is to analyze the discontinuous conduction mode associated with large ripple in the inductor current $i_1(t)$.

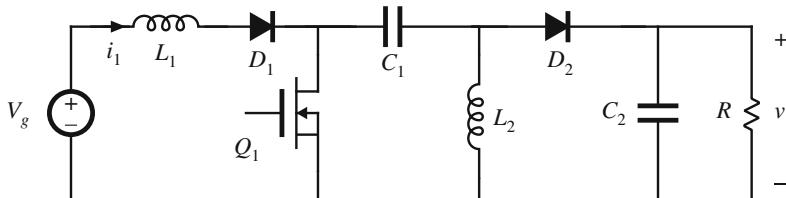


Fig. 5.25 Modified SEPIC for Problem 5.9

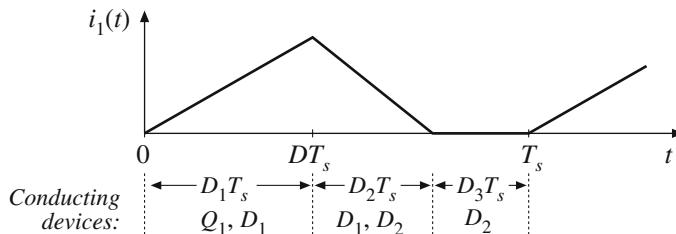


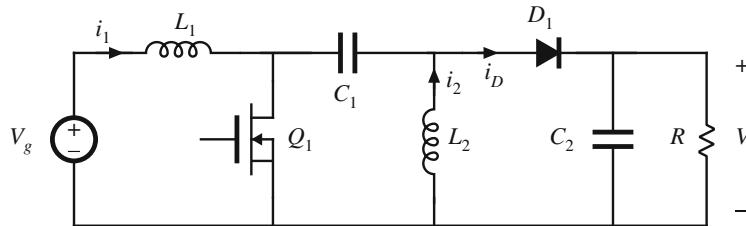
Fig. 5.26 Inductor current waveform $i_1(t)$

For this problem, you may assume that the switching ripples in the current of inductor L_2 , the voltage of capacitor C_1 , and the voltage of capacitor C_2 , are negligible. Figure 5.26 depicts the inductor current waveform $i_1(t)$ and the sequence of conducting devices for the discontinuous conduction mode that is the subject of this problem. Neglect all losses.

- Derive an expression for the boundary between the discontinuous conduction mode illustrated in Fig. 5.26 and the continuous conduction mode. Express your result in terms of the parameters K and $K_{crit}(D)$, in the usual manner, and give expressions for K and K_{crit} .
- Derive the system of equations that relate the dc components of the important waveforms of the circuit in the discontinuous conduction mode of Fig. 5.26. Solve to find the conversion ratio:

$$M(D, K) = \frac{V}{V_g}$$

Your result should be a function of D and K only, with other intermediate variables eliminated.

5.10 DCM mode boundary analysis of the SEPIC of Fig. 5.27**Fig. 5.27** SEPIC, Problems 5.10 and 5.11

- (a) Sketch the diode current waveform for CCM operation. Find its peak value, in terms of the ripple magnitudes Δi_{L1} , Δi_{L2} , and the dc components I_1 and I_2 , of the two inductor currents $i_{L1}(t)$ and $i_{L2}(t)$, respectively.
- (b) Derive an expression for the conditions under which the SEPIC operates in the discontinuous conduction mode. Express your result in the form $K < K_{crit}(D)$, and give formulas for K and $K_{crit}(D)$.

5.11 DCM conversion ratio analysis of the SEPIC of Fig. 5.27.

- (a) Suppose that the converter operates at the boundary between CCM and DCM, with the following element and parameter values:

$$\begin{aligned} D &= 0.225 & f_s &= 100 \text{ kHz} \\ V_g &= 120 \text{ V} & R &= 10\Omega \\ L_1 &= 50 \mu\text{H} & L_2 &= 75 \mu\text{H} \\ C_1 &= 47 \mu\text{F} & C_2 &= 200 \mu\text{F} \end{aligned}$$

Sketch the diode current waveform $i_D(t)$, and the inductor current waveforms $i_1(t)$ and $i_2(t)$. Label the magnitudes of the ripples and dc components of these waveforms.

- (b) Suppose next that the converter operates in the discontinuous conduction mode, with a different choice of parameter and element values. Derive an analytical expression for the dc conversion ratio $M(D, K)$.
- (c) Sketch the diode current waveform $i_D(t)$, and the inductor current waveforms $i_1(t)$ and $i_2(t)$, for operation in the discontinuous conduction mode.

5.12 An $L - C$ input filter is added to a buck converter as illustrated in Fig. 5.28. Inductors L_1 and L_2 and capacitor C_2 are large in value, such that their switching ripples are small. All losses can be neglected.

- (a) Sketch the capacitor C_1 voltage waveform $v_1(t)$, and derive expressions for its dc component V_1 and peak ripple magnitude Δv_1 .
- (b) The load current is increased (R is decreased in value) such that Δv_1 is greater than V_1 .
 - (i) Sketch the capacitor voltage waveform $v_1(t)$.
 - (ii) For each subinterval, determine which semiconductor devices conduct.

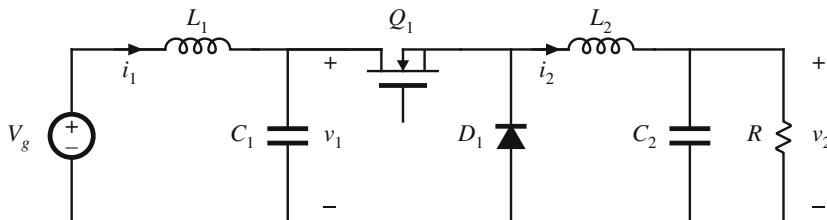


Fig. 5.28 Buck converter with input filter, Problems 5.12 and 5.13

- (iii) Determine the conditions under which the discontinuous conduction mode occurs. Express your result in the form $K < K_{crit}(D)$, and give formulas for K and $K_{crit}(D)$.

5.13 Derive an expression for the conversion ratio $M(D, K)$ of the DCM converter described in the previous problem. Note: D is the transistor duty cycle.

5.14 In the Cuk converter of Fig. 5.24, inductors L_1 and L_2 and capacitor C_2 are large in value, such that their switching ripples are small. All losses can be neglected.

- Assuming that the converter operates in CCM, sketch the capacitor C_1 voltage waveform $v_{C1}(t)$, and derive expressions for its dc component V_1 and peak ripple magnitude Δv_{C1} .
- The load current is increased (R is decreased in value) such that Δv_{C1} is greater than V_1 .
 - Sketch the capacitor voltage waveform $v_{C1}(t)$.
 - For each subinterval, determine which semiconductor devices conduct.
 - Determine the conditions under which the discontinuous conduction mode occurs. Express your result in the form $K < K_{crit}(D)$, and give formulas for K and $K_{crit}(D)$.

5.15 Derive an expression for the conversion ratio $M(D, K)$ of the DCM Cuk converter described in the previous problem. Note: D is the transistor duty cycle.

5.16 A DCM buck-boost converter as in Fig. 5.21 is to be designed to operate under the following conditions:

$$136 \text{ V} \leq V_g \leq 204 \text{ V}$$

$$5 \text{ W} \leq P_{load} \leq 100 \text{ W}$$

$$V = -150 \text{ V}$$

$$f_s = 100 \text{ kHz}$$

You may assume that a feedback loop will vary to transistor duty cycle as necessary to maintain a constant output voltage of -150 V .

Design the converter, subject to the following considerations:

- The converter should operate in the discontinuous conduction mode at all times
- Given the above requirements, choose the element values to minimize the peak inductor current
- The output voltage peak ripple should be less than 1V .

Specify:

- (a) The inductor value L
- (b) The output capacitor value C
- (c) The worst-case peak inductor current i_{pk}
- (d) The maximum and minimum values of the transistor duty cycle D

5.17 A DCM boost converter as in Fig. 5.12 is to be designed to operate under the following conditions:

$$\begin{aligned} 18 \text{ V} &\leq V_g \leq 36 \text{ V} \\ 5 \text{ W} &\leq P_{load} \leq 100 \text{ W} \\ V &= 48 \text{ V} \\ f_s &= 150 \text{ kHz} \end{aligned}$$

You may assume that a feedback loop will vary the transistor duty cycle as necessary to maintain a constant output voltage of 48 V.

Design the converter, subject to the following considerations:

- The converter should operate in the discontinuous conduction mode at all times. To ensure an adequate design margin, the inductance L should be chosen such that K is no greater than 75% of K_{crit} at all operating points.
- Given the above requirements, choose the element values to minimize the peak inductor current.
- The output voltage peak ripple should be less than 1V.

Specify:

- (a) The inductor value L
- (b) The output capacitor value C
- (c) The worst-case peak inductor current i_{pk}
- (d) The maximum and minimum values of the transistor duty cycle D .
- (e) The values of D , K , and K_{crit} at the following operating points: (i) $V_g = 18 \text{ V}$ and $P_{load} = 5 \text{ W}$; (ii) $V_g = 36 \text{ V}$ and $P_{load} = 5 \text{ W}$; (iii) $V_g = 18 \text{ V}$ and $P_{load} = 100 \text{ W}$; (iv) $V_g = 36 \text{ V}$ and $P_{load} = 100 \text{ W}$.

5.18 In dc–dc converters used in battery-powered portable equipment, it is sometimes required that the converter continue to regulate its load voltage with high efficiency while the load is in a low-power “sleep” mode. The power required by the transistor gate drive circuitry, as well as much of the switching loss, is dependent on the switching frequency but not on the load current. So to obtain high efficiency at very low load powers, a variable-frequency control scheme is used, in which the switching frequency is reduced in proportion to the load current.

Consider the boost converter system of Fig. 5.29a. The battery pack consists of two nickel-cadmium cells, which produce a voltage of $V_g = 2.4 \text{ V} \pm 0.4 \text{ V}$. The converter boosts this voltage to a regulated 5 V. As illustrated in Fig. 5.29b, the converter operates in the discontinuous conduction mode, with constant transistor on-time t_{on} . The transistor off-time t_{off} is varied by the controller to regulate the output voltage.

- (a) Write the equations for the CCM-DCM boundary and conversion ratio $M = V/V_g$, in terms of t_{on} , t_{off} , L , and the effective load resistance R .
For parts (b) and (c), the load current can vary between $100 \mu\text{A}$ and 1 A. The transistor on-time is fixed: $t_{on} = 10 \mu\text{s}$.
- (b) Select values for L and C such that:
 - The output voltage peak ripple is no greater than 50 mV,

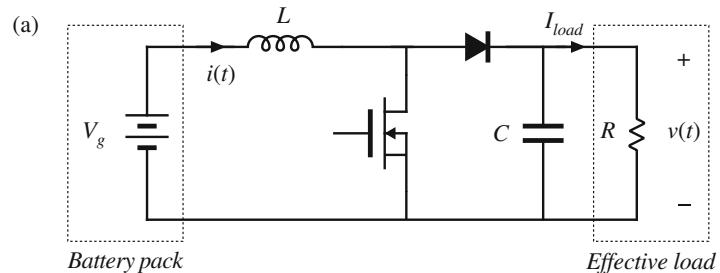
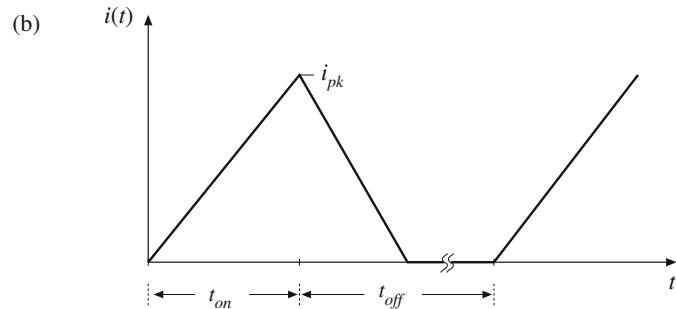


Fig. 5.29 Boost converter employed in portable battery-powered equipment with sleep mode, Problem 5.18:

- (a) converter circuit,
 (b) inductor current waveform



- The converter always operates in DCM, and
 - The peak inductor current is as small as possible.
- (c) For your design of part (b), what are the maximum and minimum values of the switching frequency?

- 5.19** An unregulated dc input voltage V_g varies over the range $35V \leq V_g \leq 70V$. A buck converter reduces this voltage to 28 V; a feedback loop varies the duty cycle as necessary such that the converter output voltage is always equal to 28 V. The load power varies over the range $10W \leq P_{load} \leq 1000W$. The buck converter elements are $L = 22\mu H$, $C = 470\mu F$, $f_s = 75kHz$. Losses may be ignored.

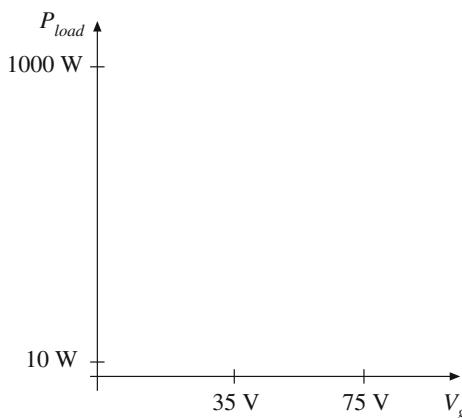


Fig. 5.30 V_g vs. P_{load} axes, Problem 5.19

- (a) Over what range of V_g and P_{load} does the converter operate in continuous conduction mode? Sketch the mode boundary on the axes of Fig. 5.30, and identify the region over which the converter operates in CCM.
- (b) Determine the maximum and minimum values of the steady-state transistor duty cycle.



Converter Circuits

We have already analyzed the operation of a number of different types of converters: buck, boost, buck-boost, Ćuk, voltage-source inverter, etc. With these converters, a number of different functions can be performed: step-down of voltage, step-up, inversion of polarity, and conversion of dc to ac or vice-versa.

It is natural to ask: Where do these converters come from? What other converters occur, and what other functions can be obtained? What are the basic relations between converters? In this chapter, several different circuit manipulations are explored, which explain the origins of the basic converters. Inversion of source and load transforms the buck converter into the boost converter. Cascade connection of converters, and simplification of the resulting circuit, shows how the buck-boost and Ćuk converters are based on the buck and the boost converters. Differential connection of the load between the outputs of two or more converters leads to a single-phase or polyphase inverter. A short list of some of the better known converter circuits follows this discussion.

Transformer-isolated dc–dc converters are also covered in this chapter. Use of a transformer allows isolation and multiple outputs to be obtained in a dc–dc converter, and can lead to better converter optimization when a very large or very small conversion ratio is required. The transformer is modeled as a magnetizing inductance in parallel with an ideal transformer; this allows the analysis techniques of the previous chapters to be extended to cover converters containing transformers. A number of well-known isolated converters, based on the buck, boost, buck-boost, single-ended primary inductance converter (SEPIC), and Ćuk, are listed and discussed.

Finally, the evaluation, selection, and design of converters to meet given requirements are considered. Important performance-related attributes of transformer-isolated converters include: whether the transformer reset process imposes excessive voltage stress on the transistors, whether the converter can supply a high-current output without imposing excessive current stresses on the secondary-side components, and whether the converter can be well-optimized to operate with a wide range of operating points, that is, with large tolerances in V_g and P_{load} . Switch utilization is a simplified figure-of-merit that measures the ratio of the converter output power to the total transistor voltage and current stress. As the switch utilization increases, the converter efficiency increases while its cost decreases. Isolated converters with large variations in operating point tend to utilize their power devices more poorly than nonisolated converters.

which function at a single operating point. Computer spreadsheets are a good tool for optimization of power-stage designs and for trade studies to select a converter topology for a given application.

6.1 Circuit Manipulations

The buck converter (Fig. 6.1) was developed in Chap. 1 using basic principles. The switch reduces the voltage dc component, and the low-pass filter removes the switching harmonics. In the continuous conduction mode, the buck converter has a conversion ratio of $M = D$. The buck converter is the simplest and most basic circuit, from which we will derive other converters.

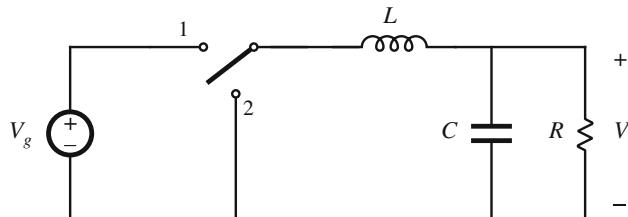


Fig. 6.1 The basic buck converter

6.1.1 Inversion of Source and Load

Let us consider first what happens when we interchange the power input and power output ports of a converter. In the buck converter of Fig. 6.2a, voltage V_1 is applied at port 1, and voltage V_2 appears at port 2. We know that

$$V_2 = DV_1 \quad (6.1)$$

This equation can be derived using the principle of inductor volt-second balance, with the assumption that the converter operates in the continuous conduction mode. Provided that the switch is realized such that this assumption holds, then Eq. (6.1) is true regardless of the direction of power flow.

So let us interchange the power source and load, as in Fig. 6.2b. The load, bypassed by the capacitor, is connected to converter port 1, while the power source is connected to converter port 2. Power now flows in the opposite direction through the converter. Equation (6.1) must still hold; by solving for the load voltage V_1 , one obtains

$$V_1 = \frac{1}{D} V_2 \quad (6.2)$$

So the load voltage is greater than the source voltage. Figure 6.2b is a boost converter, drawn backwards. Equation (6.2) nearly coincides with the familiar boost converter result, $M(D) = 1/D'$, except that D' is replaced by D .

Since power flows in the opposite direction, the standard buck converter unidirectional switch realization cannot be used with the circuit of Fig. 6.2b. By following the discussion of Chap. 4, one finds that the switch can be realized by connecting a transistor between the inductor and ground, and a diode from the inductor to the load, as shown in Fig. 6.2c. In consequence,

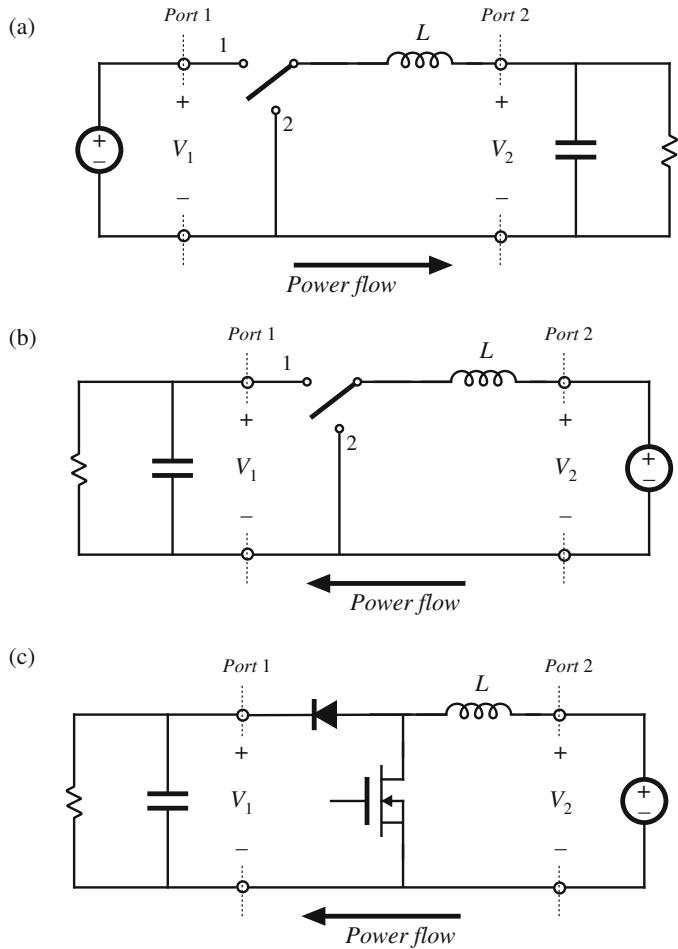
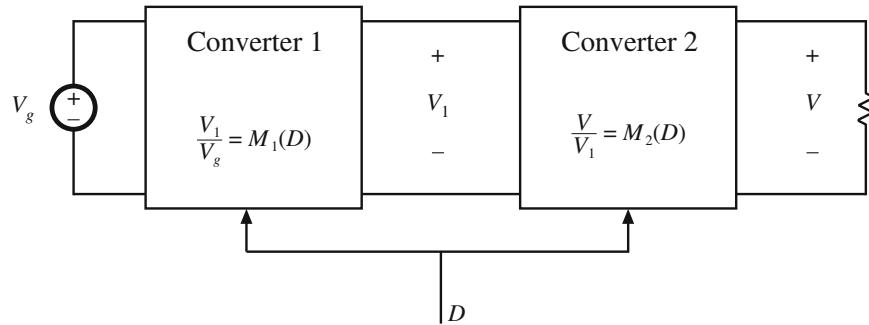


Fig. 6.2 Inversion of source and load transforms a buck converter into a boost converter: (a) buck converter, (b) inversion of source and load, (c) realization of switch

the transistor duty cycle D becomes the fraction of time which the single-pole double-throw (SPDT) switch of Fig. 6.2b spends in position 2, rather than in position 1. So we should interchange D with its complement D' in Eq. (6.2), and the conversion ratio of the converter of Fig. 6.2c is

$$V_1 = \frac{1}{D'} V_2 \quad (6.3)$$

Thus, the boost converter can be viewed as a buck converter having the source and load connections exchanged, and in which the switch is realized in a manner that allows reversal of the direction of power flow.

**Fig. 6.3** Cascade connection of converters

6.1.2 Cascade Connection of Converters

Converters can also be connected in cascade, as illustrated in Fig. 6.3 [15, 44]. Converter 1 has conversion ratio $M_1(D)$, such that its output voltage V_1 is

$$V_1 = M_1(D)V_g \quad (6.4)$$

This voltage is applied to the input of the second converter. Let us assume that converter 2 is driven with the same duty cycle D applied to converter 1. If converter 2 has conversion ratio $M_2(D)$, then the output voltage V is

$$V = M_2(D)V_1 \quad (6.5)$$

Substitution of Eq. (6.4) into Eq. (6.5) yields

$$\frac{V}{V_g} = M(D) = M_1(D)M_2(D) \quad (6.6)$$

Hence, the conversion ratio $M(D)$ of the composite converter is the product of the individual conversion ratios $M_1(D)$ and $M_2(D)$.

Let us consider the case where converter 1 is a buck converter, and converter 2 is a boost converter. The resulting circuit is illustrated in Fig. 6.4. The buck converter has conversion ratio

$$\frac{V_1}{V_g} = D \quad (6.7)$$

The boost converter has conversion ratio

$$\frac{V}{V_1} = \frac{1}{1 - D} \quad (6.8)$$

So the composite conversion ratio is

$$\frac{V}{V_g} = \frac{D}{1 - D} \quad (6.9)$$

The composite converter has a noninverting buck-boost conversion ratio. The voltage is reduced when $D < 0.5$, and increased when $D > 0.5$.

The circuit of Fig. 6.4 can be simplified considerably. Note that inductors L_1 and L_2 , along with capacitor C_1 , form a three-pole low-pass filter. The conversion ratio does not depend on the number of poles present in the low-pass filter, and so the same steady-state output voltage should be obtained when a simpler low-pass filter is used. In Fig. 6.5a, capacitor C_1 is removed. Inductors L_1 and L_2 are now in series, and can be combined into a single inductor as shown in Fig. 6.5b. This converter, the noninverting buck-boost converter, continues to exhibit the conversion ratio given in Eq. (6.9).

The switches of the converter of Fig. 6.5b can also be simplified, leading to a negative output voltage. When the switches are in position 1, the converter reduces to Fig. 6.6a. The inductor is connected to the input source V_g , and energy is transferred from the source to the inductor. When the switches are in position 2, the converter reduces to Fig. 6.6b. The inductor is then connected to the load, and energy is transferred from the inductor to the load. To obtain a negative output, we can simply reverse the polarity of the inductor during one of the subintervals (say, while

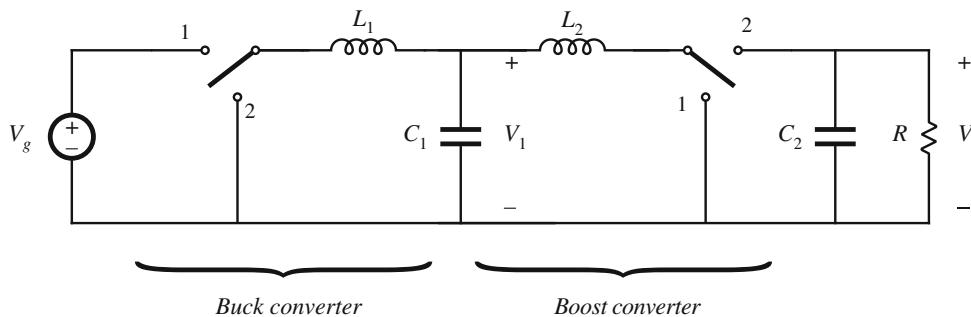


Fig. 6.4 Cascade connection of buck converter and boost converter

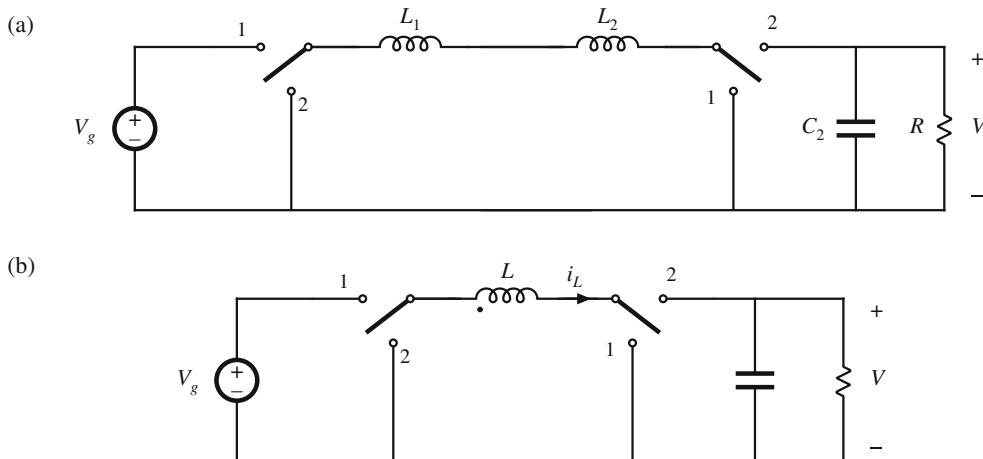


Fig. 6.5 Simplification of the cascaded buck and boost converter circuit of Fig. 6.4: (a) removal of capacitor C_1 , (b) combining of inductors L_1 and L_2

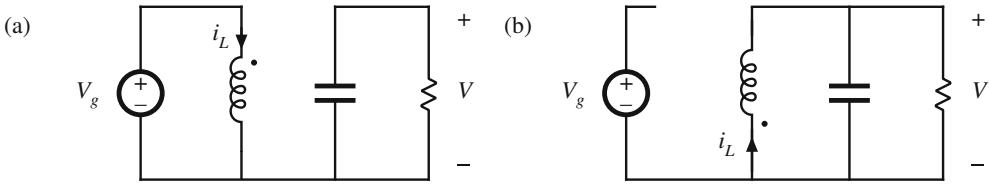


Fig. 6.6 Connections of the circuit of Fig. 6.5b: (a) while the switches are in position 1, (b) while the switches are in position 2

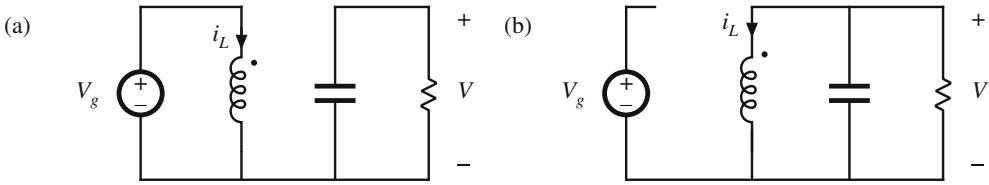


Fig. 6.7 Reversal of the output voltage polarity, by reversing the inductor connections while the switches are in position 2: (a) connections with the switches in position 1, (b) connections with the switches in position 2

the switches are in position 2). The individual circuits of Fig. 6.7 are then obtained, and the conversion ratio becomes

$$\frac{V}{V_g} = -\frac{D}{1-D} \quad (6.10)$$

Note that one side of the inductor is now always connected to ground, while the other side is switched between the input source and the load. Hence only one SPDT switch is needed, and the converter circuit of Fig. 6.8 is obtained. Figure 6.8 is recognized as the conventional buck-boost converter.

Thus, the buck-boost converter can be viewed as a cascade connection of buck and boost converters. The properties of the buck-boost converter are consistent with this viewpoint. Indeed, the equivalent circuit model of the buck-boost converter contains a 1:D (buck) dc transformer, followed by a D' : 1 (boost) dc transformer. The buck-boost converter inherits the pulsating input current of the buck converter, and the pulsating output current of the boost converter.

Other converters can be derived by cascade connections. The Ćuk converter (Fig. 2.20) was originally derived [15, 44] by cascading a boost converter (converter 1), followed by a buck (converter 2). A negative output voltage is obtained by reversing the polarity of the internal

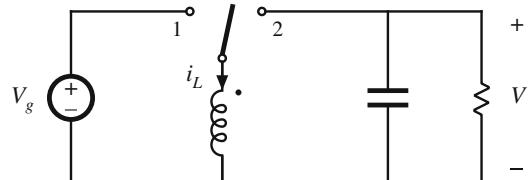


Fig. 6.8 Converter circuit obtained from the subcircuits of Fig. 6.7

capacitor connection during one of the subintervals; as in the buck-boost converter, this operation has the additional benefit of reducing the number of switches. The equivalent circuit model of the Ćuk converter contains a $D':1$ (boost) ideal dc transformer, followed by a $1:D$ (buck) ideal dc transformer. The Ćuk converter inherits the nonpulsating input current property of the boost converter, and the nonpulsating output current property of the buck converter.

6.1.3 Rotation of Three-Terminal Cell

The buck, boost, and buck-boost converters each contains an inductor that is connected to a SPDT switch. As illustrated in Fig. 6.9a, the inductor-switch network can be viewed as a basic cell having the three terminals labeled a , b , and c . It was first pointed out in [15, 44], and later in [45], that there are three distinct ways to connect this cell between the source and load. The connections $a-A$ $b-B$ $c-C$ lead to the buck converter. The connections $a-A$ $b-B$ $c-C$ amount to inversion of the source and load, and lead to the boost converter. The connections $a-A$ $b-B$ $c-C$ lead to the buck-boost converter. So the buck, boost, and buck-boost converters could be viewed as being based on the same inductor-switch cell, with different source and load connections.

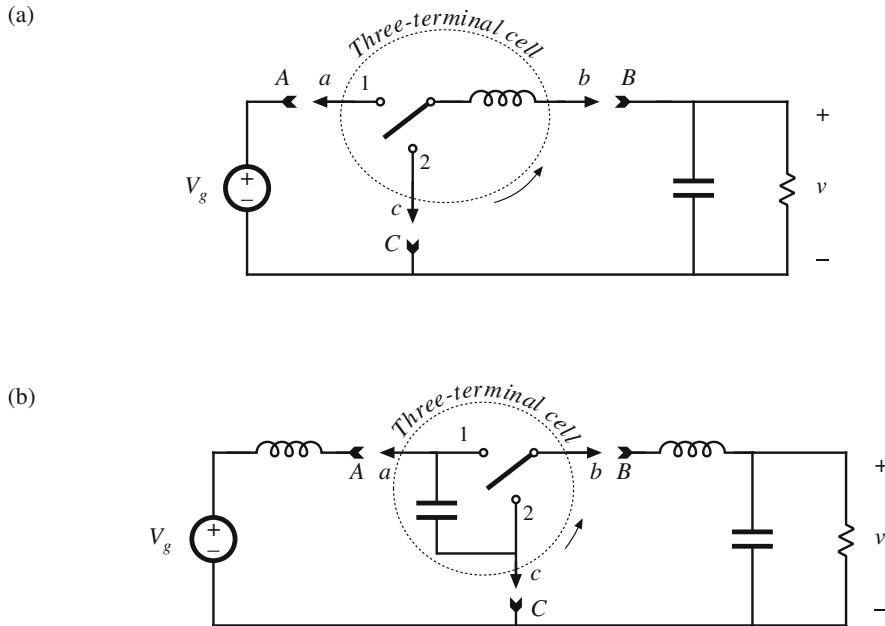


Fig. 6.9 Rotation of three-terminal switch cells: (a) switch/inductor cell, (b) switch/capacitor cell

A dual three-terminal network, consisting of a capacitor-switch cell, is illustrated in Fig. 6.9b. Filter inductors are connected in series with the source and load, such that the converter input and output currents are nonpulsating. There are again three possible ways to connect this cell

between the source and load. The connections a - A b - B c - C lead to a buck converter with L - C input low-pass filter. The connections a - A b - B c - C coincide with inversion of source and load, and lead to a boost converter with an added output L - C filter section. The connections a - A b - B c - C lead to the Ćuk converter.

Rotation of more complicated three-terminal cells is explored in [46].

6.1.4 Differential Connection of the Load

In inverter applications, where an ac output is required, a converter is needed that is capable of producing an output voltage of either polarity. By variation of the duty cycle in the correct manner, a sinusoidal output voltage having no dc bias can then be obtained. Of the converters studied so far in this chapter, the buck and the boost can produce only a positive unipolar output voltage, while the buck-boost and Ćuk converters produce only a negative unipolar output voltage. How can we derive converters that can produce bipolar output voltages?

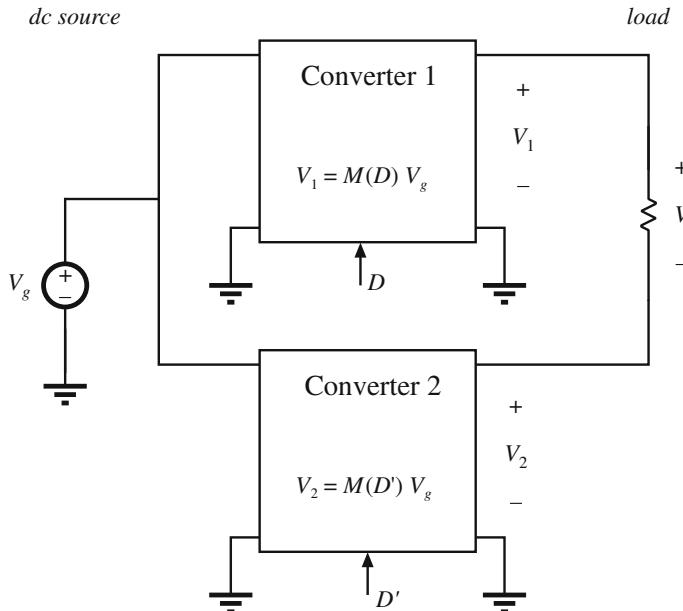


Fig. 6.10 Obtaining a bipolar output by differential connection of load

A well-known technique for obtaining a bipolar output is the differential connection of the load across the outputs of two known converters, as illustrated in Fig. 6.10. If converter 1 produces voltage V_1 , and converter 2 produces voltage V_2 , then the load voltage V is given by

$$V = V_1 - V_2 \quad (6.11)$$

Although V_1 and V_2 may both individually be positive, the load voltage V can be either positive or negative. Typically, if converter 1 is driven with duty cycle D , then converter 2 is driven with its complement, D' , so that when V_1 increases, V_2 decreases, and vice versa.

Several well-known inverter circuits can be derived using the differential connection. Let us realize converters 1 and 2 of Fig. 6.10 using buck converters. Figure 6.11a is obtained. Converter

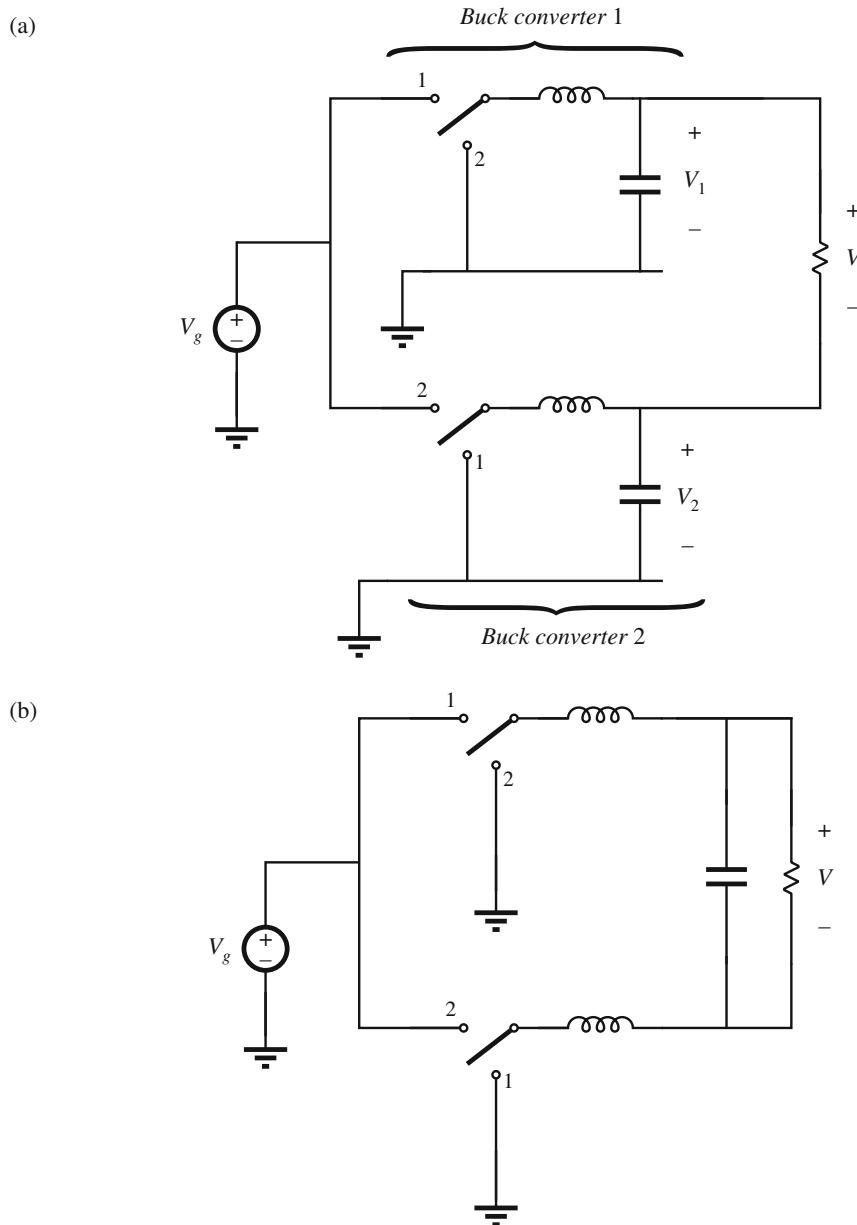


Fig. 6.11 Derivation of bridge inverter (H-bridge): (a) differential connection of load across outputs of buck converters, (b) bypassing load by capacitor, (c) combining series inductors, (d) circuit (c) redrawn in its usual form

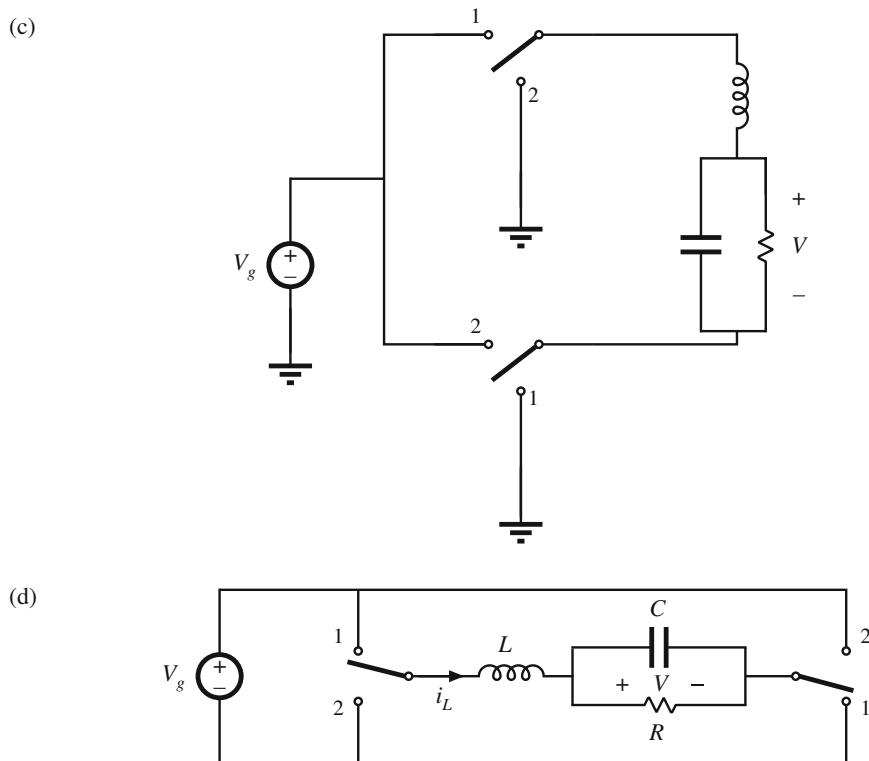
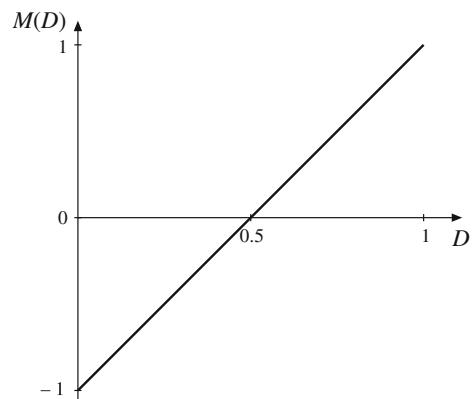


Fig. 6.11 (continued)

Fig. 6.12 Conversion ratio of the H-bridge inverter circuit



1 is driven with duty cycle D , while converter 2 is driven with duty cycle D' . So when the SPDT switch of converter 1 is in the upper position, then the SPDT switch of converter 2 is in the lower position, and vice-versa. Converter 1 then produces output voltage $V_1 = DV_g$, while converter 2 produces output voltage $V_2 = D'V_g$. The differential load voltage is

$$V = DV_g - D'V_g \quad (6.12)$$

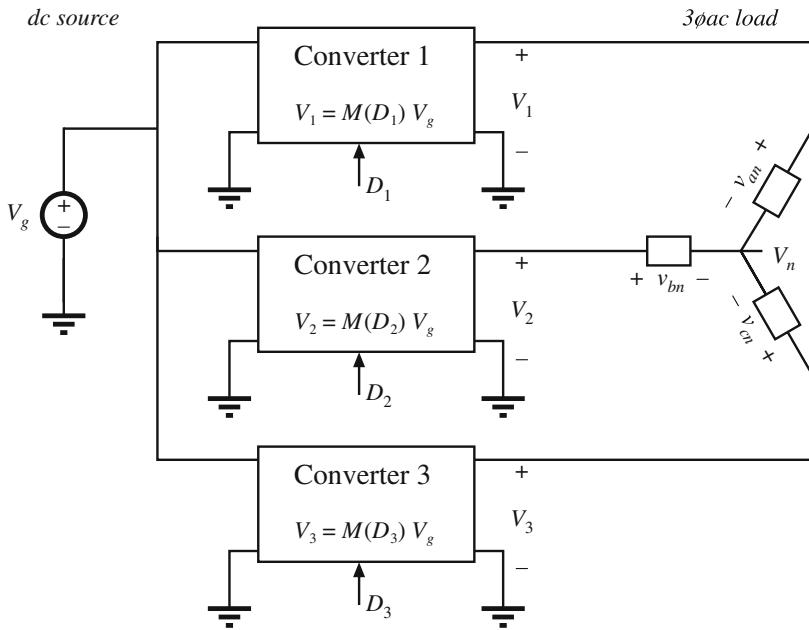


Fig. 6.13 Generation of dc–3φac inverter by differential connection of 3φ load

Simplification leads to

$$V = (2D - 1)V_g \quad (6.13)$$

This equation is plotted in Fig. 6.12. It can be seen the output voltage is positive for $D > 0.5$, and negative for $D < 0.5$. If the duty cycle is varied sinusoidally about a quiescent operating point of 0.5, then the output voltage will be sinusoidal, with no dc bias.

The circuit of Fig. 6.11a can be simplified. It is usually desired to bypass the load directly with a capacitor, as in Fig. 6.11b. The two inductors are now effectively in series, and can be combined into a single inductor as in Fig. 6.11c. Figure 6.11d is identical to Fig. 6.11c, but is redrawn for clarity. This circuit is commonly called the H-bridge, or bridge inverter circuit. Its use is widespread in servo amplifiers and single-phase inverters. Its properties are similar to those of the buck converter, from which it is derived.

Polyphase inverter circuits can be derived in a similar manner. A three-phase load can be connected differentially across the outputs of three dc–dc converters, as illustrated in Fig. 6.13. If the three-phase load is balanced, then the neutral voltage V_n will be equal to the average of the three converter output voltages:

$$V_n = \frac{1}{3} (V_1 + V_2 + V_3) \quad (6.14)$$

If the converter output voltages V_1 , V_2 , and V_3 contain the same dc bias, then this dc bias will also appear at the neutral point V_n . The phase voltages V_{an} , V_{bn} , and V_{cn} are given by

$$\begin{aligned}V_{an} &= V_1 - V_n \\V_{bn} &= V_2 - V_n \\V_{cn} &= V_3 - V_n\end{aligned}\tag{6.15}$$

It can be seen that the dc biases cancel out, and do not appear in V_{an} , V_{bn} , and V_{cn} .

Let us realize converters 1, 2, and 3 of Fig. 6.13 using buck converters. Figure 6.14a is then obtained. The circuit is redrawn in Fig. 6.14b for clarity. This converter is known by several names, including the *voltage-source inverter* and the buck-derived three-phase bridge.

Inverter circuits based on dc–dc converters other than the buck converter can be derived in a similar manner. Figure 6.14c contains a three-phase current-fed bridge converter having a boost-type voltage conversion ratio, also known as the *current source inverter*. Since most inverter applications require the capability to reduce the voltage magnitude, a dc–dc buck converter is usually cascaded at the dc input port of this inverter. Several other examples of three-phase inverters are given in [19, 22, 47], in which the converters are capable of both increasing and decreasing the voltage magnitude.

6.2 A Short List of Converters

An infinite number of converters are possible, and hence it is not feasible to list them all. A short list is given here.

Let us consider first the class of single-input single-output converters, containing a single inductor. There are a limited number of ways in which the inductor can be connected between the source and load. If we assume that the switching period is divided into two subintervals, then the inductor should be connected to the source and load in one manner during the first subinterval, and in a different manner during the second subinterval. One can examine all of the possible combinations, to derive the complete set of converters in this class [48–50]. By elimination of redundant and degenerate circuits, one finds that there are eight converters, listed in Fig. 6.15. How the converters are counted can actually be a matter of semantics and personal preference; for example, many people in the field would not consider the noninverting buck-boost converter as distinct from the inverting buck-boost. Nonetheless, it can be said that a converter is defined by the connections between its reactive elements, switches, source, and load; by how the switches are realized; and by the numerical range of reactive element values.

The first four converters of Fig. 6.15, the buck, boost, buck-boost, and the noninverting buck-boost, have been previously discussed. These converters produce a unipolar dc output voltage. With these converters, it is possible to increase, decrease, and/or invert a dc voltage.

Converters 5 and 6 are capable of producing a bipolar output voltage. Converter 5, the H-bridge, has previously been discussed. Converter 6 is a nonisolated version of the current-fed converter of Fig. 6.38b; this converter is denoted the *Watkins-Johnson converter* [51–55]. This converter can also produce a bipolar output voltage; however, its conversion ratio $M(D)$ is a nonlinear function of duty cycle. The number of switch elements can be reduced by using a two-winding inductor as shown. The function of the inductor is similar to that of the flyback converter, discussed in the next section. When switch 1 is closed the upper winding is used, while when switch 2 is closed, current flows through the lower winding. The current flows through only one winding at any given instant, and the total ampere-turns of the two windings are a continuous function of time. Advantages of this converter are its ground-referenced load and its ability to produce a bipolar output voltage using only two SPST current-bidirectional

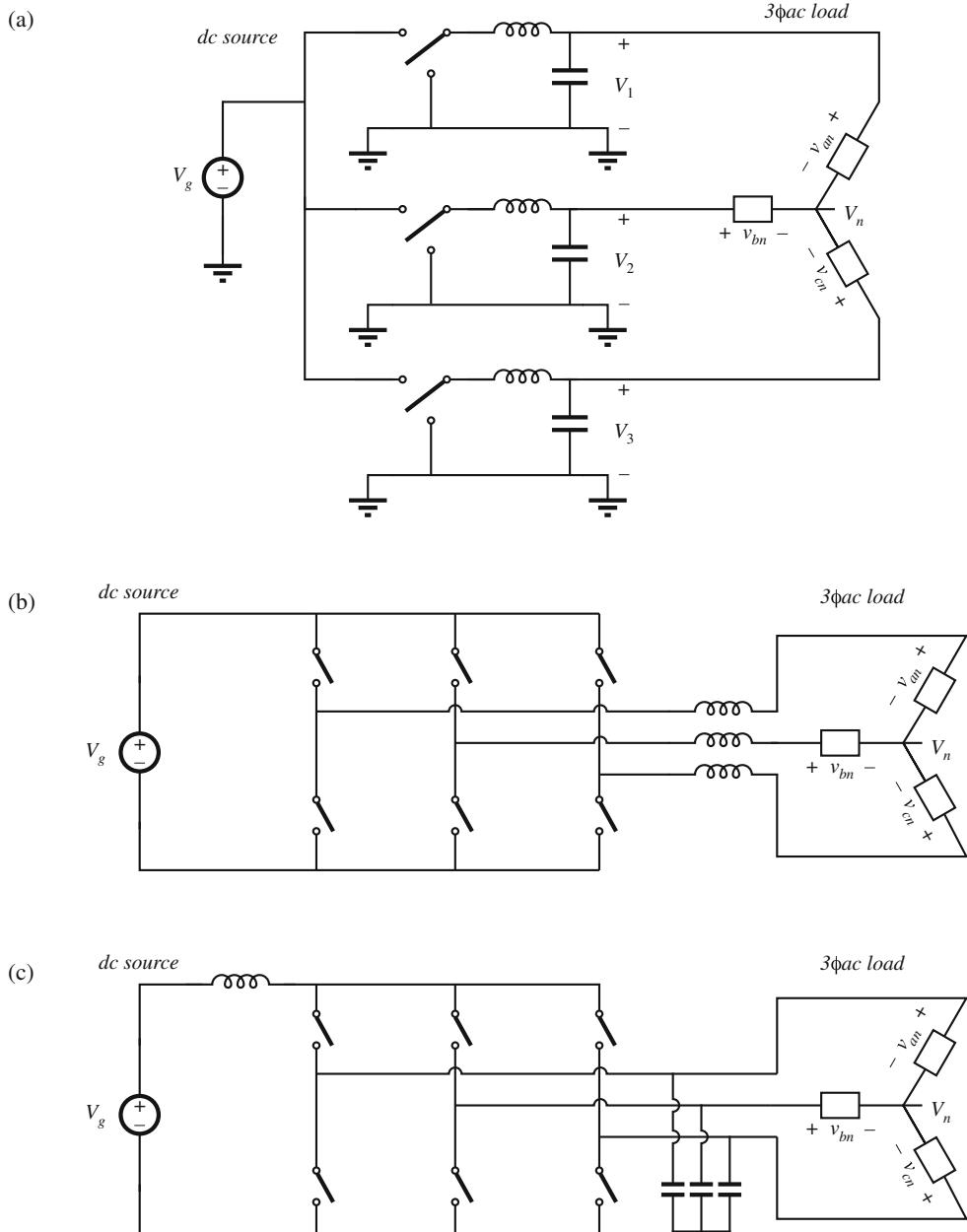
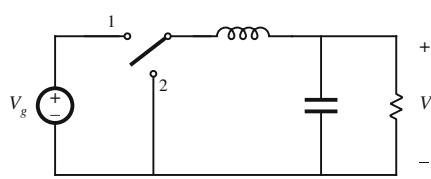
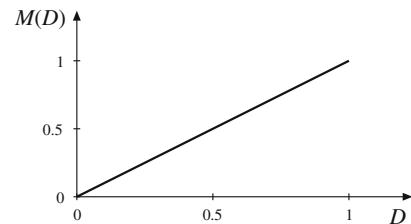


Fig. 6.14 Dc–3φac inverter topologies: (a) differential connection of 3φ load across outputs of buck converters; (b) simplification of low-pass filters to obtain the dc–3φac voltage-source inverter; (c) the dc–3φac current source inverter

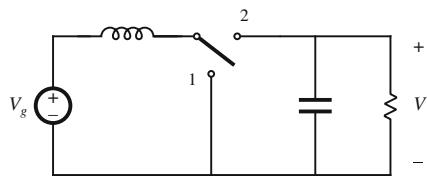
1. Buck



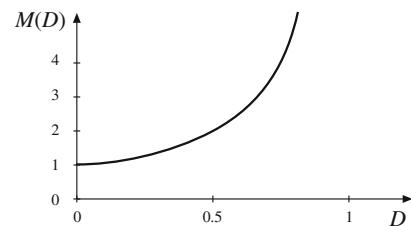
$$M(D) = D$$



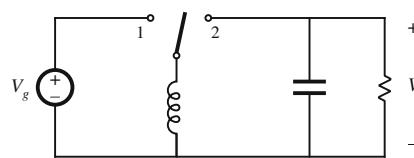
2. Boost



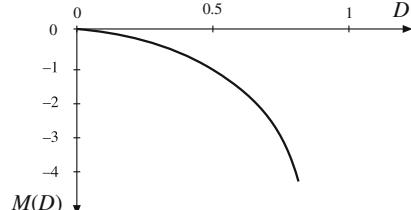
$$M(D) = \frac{1}{1-D}$$



3. Buck-boost



$$M(D) = -\frac{D}{1-D}$$



4. Noninverting buck-boost

$$M(D) = \frac{D}{1-D}$$

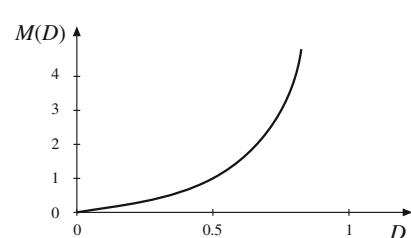
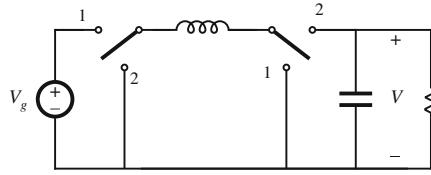


Fig. 6.15 Eight members of the basic class of single-input single-output converters containing a single inductor

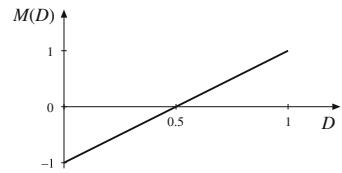
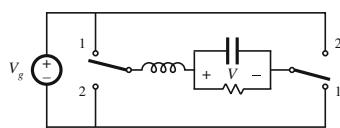
switches. The isolated version and its variants have found application in high-voltage dc power supplies.

Converters 7 and 8 can be derived as the inverses of converters 5 and 6. These converters are capable of interfacing an ac input to a dc output. The ac input current waveform can have arbitrary waveshape and power factor.

The class of single-input single-output converters containing two inductors is much larger. Several of its members are listed in Fig. 6.16. The Ćuk converter has been previously discussed and analyzed. It has an inverting buck-boost characteristic, and exhibits nonpulsating input and

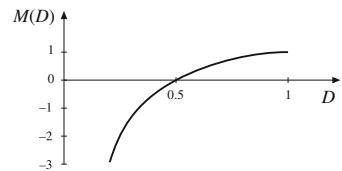
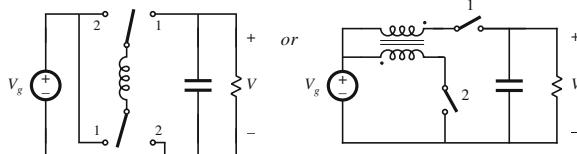
5. Bridge

$$M(D) = 2D - 1$$



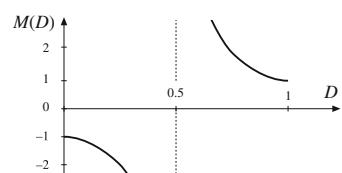
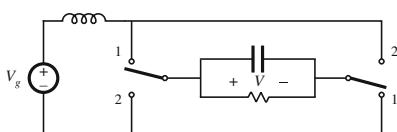
6. Watkins-Johnson

$$M(D) = \frac{2D-1}{D}$$



7. Current-fed bridge

$$M(D) = \frac{1}{2D-1}$$



8. Inverse of Watkins-Johnson

$$M(D) = \frac{D}{2D-1}$$

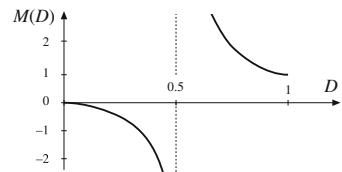
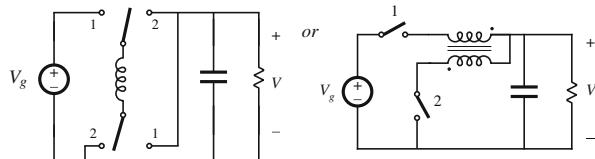
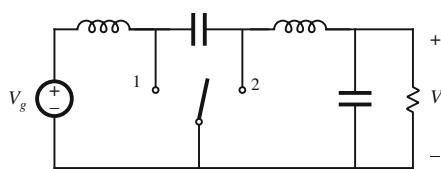
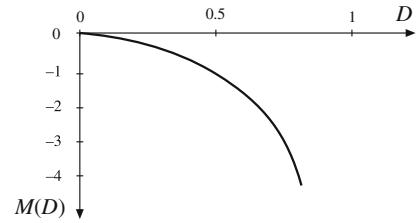
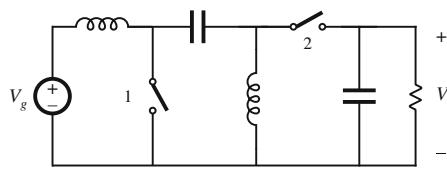


Fig. 6.15 (continued)

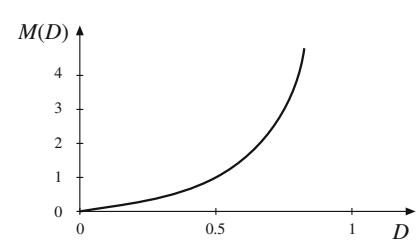
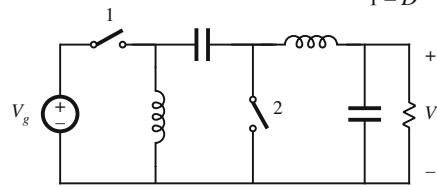
output terminal currents. The SEPIC (single-ended primary inductance converter) [56], and its inverse, have noninverting buck-boost characteristics. The Ćuk and SEPIC also exhibit the desirable feature that the MOSFET source terminal is connected to ground; this simplifies the construction of the gate drive circuitry. Two inductor converters having conversion ratios $M(D)$ that are biquadratic functions of the duty cycle D are also numerous. An example is converter 4 of Fig. 6.16 [57]. This converter can be realized using a single transistor and three diodes. Its conversion ratio is $M(D) = D^2$. This converter may find use in nonisolated applications that require a large step-down of the dc voltage, or in applications having wide variations in operating point.

1. *Cuk*

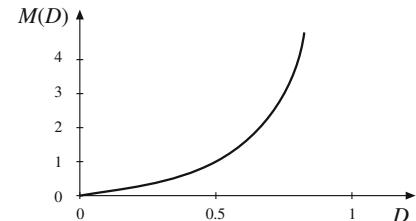
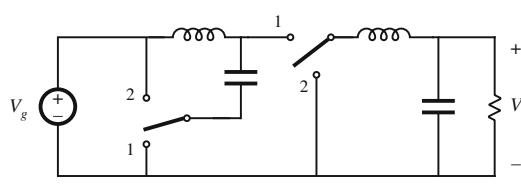
$$M(D) = -\frac{D}{1-D}$$

2. *SEPIC*

$$M(D) = \frac{D}{1-D}$$

3. *Inverse of SEPIC*

$$M(D) = \frac{D}{1-D}$$

4. *Buck*²

$$M(D) = D^2$$

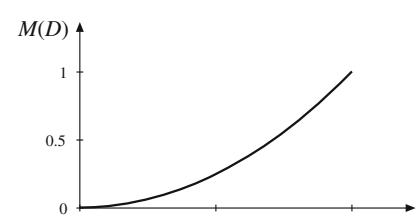


Fig. 6.16 Several members of the basic class of single-input single-output converters containing two inductors

6.3 Transformer Isolation

In a large number of applications, it is desired to incorporate a transformer into a switching converter, to obtain dc isolation between the converter input and output. For example, in off-line applications (where the converter input is connected to the ac utility system), isolation is usually required by regulatory agencies. Isolation could be obtained in these cases by simply connecting

a 50 Hz or 60 Hz transformer at the converter ac input. However, since transformer size and weight vary inversely with frequency, significant improvements can be made by incorporating the transformer into the converter, so that the transformer operates at the converter switching frequency of tens or hundreds of kilohertz.

When a large step-up or step-down conversion ratio is required, the use of a transformer can allow better converter optimization. By proper choice of the transformer turns ratio, the voltage or current stresses imposed on the transistors and diodes can be minimized, leading to improved efficiency and lower cost.

Multiple dc outputs can also be obtained in an inexpensive manner, by adding multiple secondary windings and converter secondary-side circuits. The secondary turns ratios are chosen to obtain the desired output voltages. Usually only one output voltage can be regulated via control of the converter duty cycle, so wider tolerances must be allowed for the auxiliary output voltages. *Cross regulation* is a measure of the variation in an auxiliary output voltage, given that the main output voltage is perfectly regulated [58–60].

A physical multiple-winding transformer having turns ratio $n_1:n_2:n_3:\dots$ is illustrated in Fig. 6.17, and the schematic symbol for this transformer is illustrated in Fig. 6.18a. A simple equivalent circuit is illustrated in Fig. 6.18b, which is sufficient for understanding the operation of most transformer-isolated converters. The model assumes perfect coupling between windings and neglects losses; more accurate models are discussed in a later chapter. The ideal transformer obeys the relationships

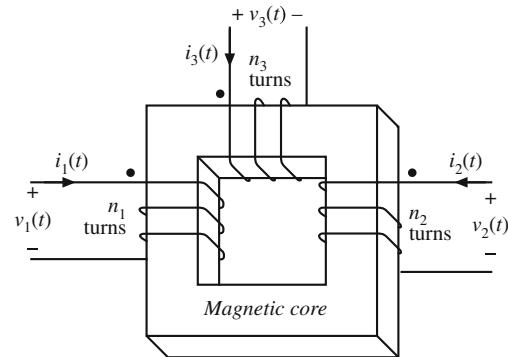


Fig. 6.17 Physical construction of a three-winding transformer

$$\frac{v_1(t)}{n_1} = \frac{v_2(t)}{n_2} = \frac{v_3(t)}{n_3} = \dots \quad (6.16)$$

$$0 = n_1 i'_1(t) + n_2 i_2(t) + n_3 i_3(t) + \dots$$

In parallel with the ideal transformer is an inductance L_M , called the *magnetizing inductance*, referred to the transformer primary in the figure.

Physical transformers must contain a magnetizing inductance. For example, suppose we disconnect all windings except for the primary winding. We are then left with a single winding on a magnetic core—an inductor. Indeed, the equivalent circuit of Fig. 6.18b predicts this behavior, via the magnetizing inductance.

The magnetizing current $i_M(t)$ is proportional to the magnetic field $H(t)$ inside the transformer core. The physical B - H characteristics of the transformer core material, illustrated in Fig. 6.19, govern the magnetizing current behavior. For example, if the magnetizing current $i_M(t)$ becomes too large, then the magnitude of the magnetic field $H(t)$ causes the core to saturate. The magnetizing inductance then becomes very small in value, effectively shorting out the transformer.

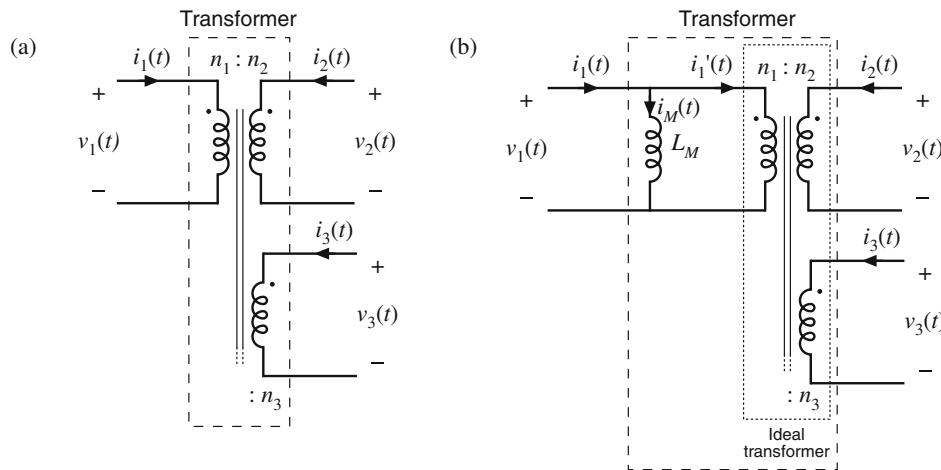
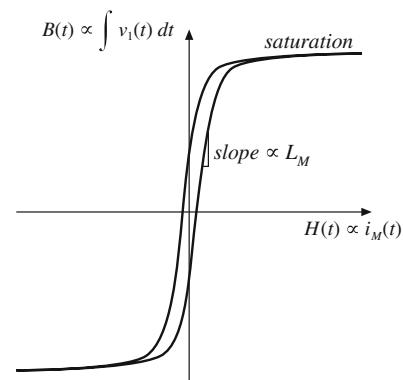


Fig. 6.18 A multiple-winding transformer: (a) schematic symbol, (b) equivalent circuit model containing a magnetizing inductance and ideal transformer

Fig. 6.19 B - H characteristics of transformer core



The presence of the magnetizing inductance explains why transformers do not work in dc circuits: at dc, the magnetizing inductance has zero impedance, and shorts out the windings. In a well-designed transformer, the impedance of the magnetizing inductance is large in magnitude

over the intended range of operating frequencies, such that the magnetizing current $i_M(t)$ has much smaller magnitude than $i_1(t)$. Then $i'_1(t) \approx i_1(t)$, and the transformer behaves nearly as an ideal transformer. It should be emphasized that the magnetizing current $i_M(t)$ and the primary winding current $i_1(t)$ are independent quantities.

The magnetizing inductance must obey all of the usual rules for inductors. In the model of Fig. 6.18b, the primary winding voltage $v_1(t)$ is applied across L_M , and hence

$$v_1(t) = L_M \frac{di_M(t)}{dt} \quad (6.17)$$

Integration leads to

$$i_M(t) - i_M(0) = \frac{1}{L_M} \int_0^t v_1(\tau) d\tau \quad (6.18)$$

So the magnetizing current is determined by the integral of the applied winding voltage. The principle of inductor volt-second balance also applies: when the converter operates in steady state, the dc component of voltage applied to the magnetizing inductance must be zero:

$$0 = \frac{1}{T_s} \int_0^{T_s} v_1(t) dt \quad (6.19)$$

Since the magnetizing current is proportional to the integral of the applied winding voltage, it is important that the dc component of this voltage be zero. Otherwise, during each switching period there will be a net increase in magnetizing current, eventually leading to excessively large currents and transformer saturation.

The operation of converters containing transformers may be understood by inserting the model of Fig. 6.18b in place of the transformer in the converter circuit. Analysis then proceeds as described in the previous chapters, treating the magnetizing inductance as any other inductor of the converter.

Practical transformers must also contain leakage inductance. A small part of the flux linking a winding may not link the other windings. In the two-winding transformer, this phenomenon may be modeled with small inductors in series with the windings. In most isolated converters, leakage inductance is a nonideality that leads to switching loss, increased peak transistor voltage, and that degrades cross-regulation, but otherwise has no influence on basic converter operation.

There are several ways of incorporating transformer isolation into a dc–dc converter. The full-bridge, half-bridge, forward, and push-pull converters are commonly used isolated versions of the buck converter. Similar isolated variants of the boost converter are known. The flyback converter is an isolated version of the buck–boost converter. These isolated converters, as well as isolated versions of the SEPIC and the Cuk converter, are discussed in this section.

6.3.1 Full-Bridge and Half-Bridge Isolated Buck Converters

The full-bridge transformer-isolated buck converter is sketched in Fig. 6.20a. A version containing a center-tapped secondary winding is shown; this circuit is commonly used in converters producing low output voltages. The two halves of the center-tapped secondary winding may be viewed as separate windings, and hence we can treat this circuit element as a three-winding

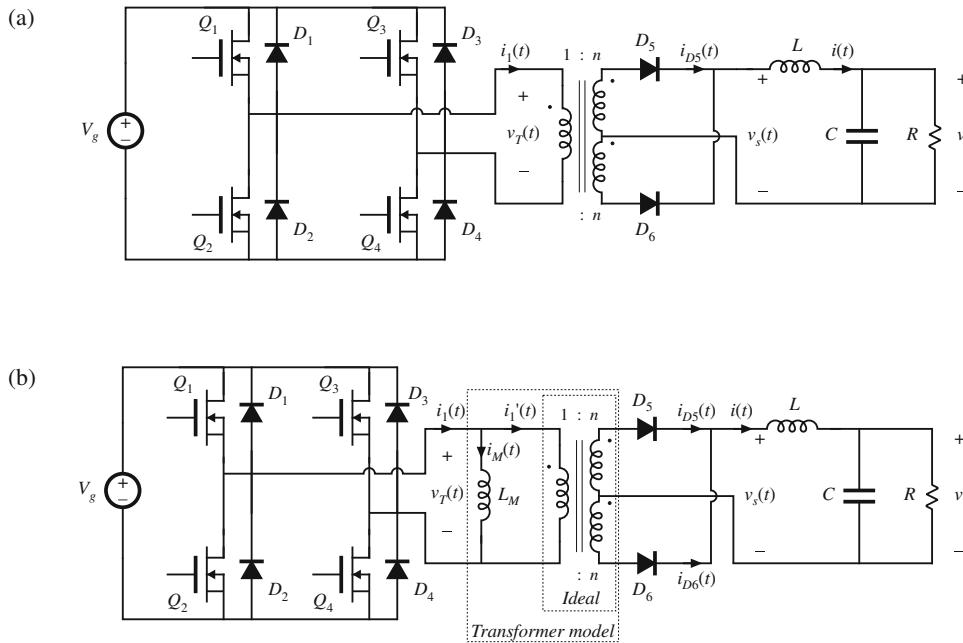


Fig. 6.20 Full-bridge transformer-isolated buck converter: (a) schematic diagram, (b) replacement of transformer with equivalent circuit model

transformer having turns ratio $1:n:n$. When the transformer is replaced by the equivalent circuit model of Fig. 6.18b, the circuit of Fig. 6.20b is obtained. Typical waveforms are illustrated in Fig. 6.21. The output portion of the converter is similar to the nonisolated buck converter—compare the $v_s(t)$ and $i(t)$ waveforms of Fig. 6.21 with Figs. 2.1b and 2.10.

During the first subinterval $0 < t < DT_s$, transistors Q_1 and Q_4 conduct, and the transformer primary voltage is $v_T = V_g$. This positive voltage causes the magnetizing current $i_M(t)$ to increase with a slope of V_g/L_M . The voltage appearing across each half of the center-tapped secondary winding is nV_g , with the polarity mark at positive potential. Diode D_5 is therefore forward-biased, and D_6 is reverse-biased. The voltage $v_s(t)$ is then equal to nV_g , and the output filter inductor current $i(t)$ flows through diode D_5 .

Several transistor control schemes are possible for the second subinterval $DT_s < t < T_s$. In the most common scheme, all four transistors are switched off, and hence the transformer voltage is $v_T = 0$. Alternatively, transistors Q_2 and Q_4 could conduct, or transistors Q_1 and Q_3 could conduct. In any event, diodes D_5 and D_6 are both forward-biased during this subinterval; each diode conducts approximately one-half of the output filter inductor current.

Actually, the diode currents i_{D5} and i_{D6} during the second subinterval are functions of both the output inductor current and the transformer magnetizing current. In the ideal case (no magnetizing current), the transformer causes $i_{D5}(t)$ and $i_{D6}(t)$ to be equal in magnitude since, if $i'_1(t) = 0$, then $ni_{D5}(t) = ni_{D6}(t)$. But the sum of the two diode currents is equal to the output inductor current:

$$i_{D5}(t) + i_{D6}(t) = i(t) \quad (6.20)$$

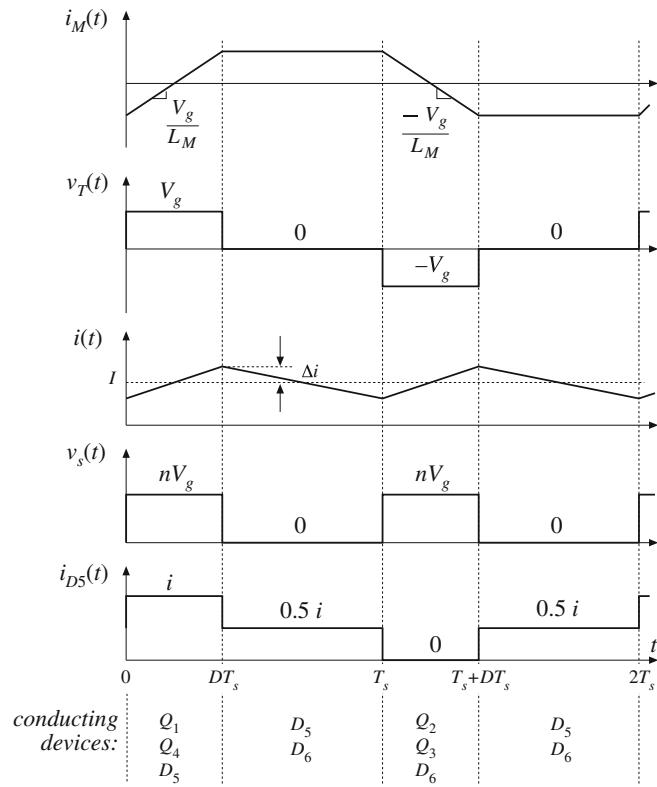


Fig. 6.21 Waveforms of the full-bridge transformer-isolated buck converter

Therefore, it must be true that $i_{D5} = i_{D6} = 0.5i$ during the second subinterval. In practice, the diode currents differ slightly from this result, because of the nonzero magnetizing current.

The ideal transformer currents in Fig. 6.20b obey

$$i'_1(t) - ni_{D5}(t) + ni_{D6}(t) = 0 \quad (6.21)$$

The node equation at the primary of the ideal transformer is

$$i_1(t) = i_M(t) + i'_1(t) \quad (6.22)$$

Elimination of $i'_1(t)$ from Eqs. (6.21) and (6.22) leads to

$$i_1(t) - ni_{D5}(t) + ni_{D6}(t) = i_M(t) \quad (6.23)$$

Equations (6.23) and (6.20) describe, in the general case, the transformer winding currents during the second subinterval. According to Eq. (6.23), the magnetizing current $i_M(t)$ may flow through the primary winding, through one of the secondary windings, or it may divide between all three of these windings. How the division occurs depends on the $i-v$ characteristics of the conducting transistors and diodes, and on the transformer leakage inductances. In the case where $i_1 = 0$, the solution to Eqs. (6.20) and (6.23) is

$$\begin{aligned} i_{D5}(t) &= \frac{1}{2}i(t) - \frac{1}{2n}i_M(t) \\ i_{D6}(t) &= \frac{1}{2}i(t) + \frac{1}{2n}i_M(t) \end{aligned} \quad (6.24)$$

Provided that $i_M \ll ni$, then i_{D5} and i_{D6} are each approximately $0.5i$.

The next switching period, $T_s < t < 2T_s$, proceeds in a similar manner, except that the transformer is excited with voltage of the opposite polarity. During $T_s < t < (T_s + DT_s)$, transistors Q_2 and Q_3 and diode D_6 conduct. The applied transformer primary voltage is $v_T = -V_g$, which causes the magnetizing current to decrease with slope $-V_g/L_M$. The voltage $v_s(t)$ is equal to nV_g , and the output inductor current $i(t)$ flows through diode D_6 . Diodes D_5 and D_6 again both conduct during $(T_s + DT_s) < t < 2T_s$, with operation similar to subinterval 2 described previously. It can be seen that the switching ripple in the output filter elements has frequency $f_s = 1/T_s$. However, the transformer waveforms have frequency $0.5f_s$.

By application of the principle of inductor volt-second balance to the magnetizing inductance, the average value of the transformer voltage $v_T(t)$ must be zero when the converter operates in steady state. During the first switching period, positive volt-seconds are applied to the transformer, approximately equal to

$$[V_g - (Q_1 \text{ and } Q_4 \text{ forward voltage drops})] (Q_1 \text{ and } Q_4 \text{ conduction time}) \quad (6.25)$$

During the next switching period, negative volt-seconds are applied to the transformer, given by

$$-[V_g - (Q_2 \text{ and } Q_3 \text{ forward voltage drops})] (Q_2 \text{ and } Q_3 \text{ conduction time}) \quad (6.26)$$

The net volt-seconds, that is, the sum of Eqs. (6.25) and (6.26), should equal zero. While the full-bridge scheme causes this to be approximately true, in practice there exist imbalances such as small differences in the transistor forward voltage drops or in the transistor switching times, so that $\langle v_T \rangle$ is small but nonzero. In consequence, during every two switching periods there is a net increase in the magnitude of the magnetizing current. This increase can cause the transistor forward voltage drops to change such that small imbalances are compensated. However, if the imbalances are too large, then the magnetizing current becomes large enough to saturate the transformer.

Transformer saturation under steady-state conditions can be avoided by placing a capacitor in series with the transformer primary. Imbalances then induce a dc voltage component across the capacitor, rather than across the transformer primary. Another solution is the use of current-programmed control, discussed in a later chapter. The series capacitor is omitted when current-programmed control is used.

By application of the principle of volt-second balance to the output filter inductor L , the dc load voltage must be equal to the dc component of $v_s(t)$:

$$V = \langle v_s \rangle \quad (6.27)$$

By inspection of the $v_s(t)$ waveform in Fig. 6.21, $\langle v_s \rangle = nDV_g$. Hence,

$$V = nDV_g \quad (6.28)$$

So as in the buck converter, the output voltage can be controlled by variation of the transistor duty cycle D . An additional increase or decrease of the voltage can be obtained via the physical transformer turns ratio n . Equation (6.28) is valid for operation in the continuous conduction mode; as in the nonisolated buck converter, the full-bridge and half-bridge converters can operate in discontinuous conduction mode at light load. The converter can operate over essentially the entire range of duty cycles $0 \leq D < 1$.

Transistors Q_1 and Q_2 must not conduct simultaneously; doing so would short out the dc source V_g , causing a *shoot-through* current spike. This transistor *cross-conduction* condition can lead to low efficiency and transistor failure. Cross conduction can be prevented by introduction of delay between the turn-off of one transistor and the turn-on of the next transistor. Diodes D_1 to D_4 ensure that the peak transistor voltage is limited to the dc input voltage V_g , and also provide a conduction path for the transformer magnetizing current at light load. Details of the switching transitions of the full-bridge circuit are discussed further in a later chapter, in conjunction with zero-voltage switching phenomena.

The full-bridge configuration is typically used in switching power supplies at power levels of approximately 750 W and greater. It is usually not used at lower power levels because of its high parts count—four transistors and their associated drive circuits are required. The utilization of the transformer is good, leading to small transformer size. In particular, the utilization of the transformer core is very good, since the transformer magnetizing current can be both positive and negative. Hence, the entire core $B-H$ loop can be used. However, in practice, the flux swing is usually limited by core loss. The transformer primary winding is effectively utilized. But the center-tapped secondary winding is not, since each half of the center-tapped winding transmits power only during alternate switching periods. Also, the secondary winding currents during subinterval 2 lead to winding power loss, but not to transmittal of energy to the load. Design of the transformer of the full-bridge configuration is discussed in detail in a later chapter.

The half-bridge transformer-isolated buck converter is illustrated in Fig. 6.22. Typical waveforms are illustrated in Fig. 6.23. This circuit is similar to the full-bridge of Fig. 6.20a, except transistors Q_3 and Q_4 , and their antiparallel diodes, have been replaced with large-value capacitors C_a and C_b . By volt-second balance of the transformer magnetizing inductance, the dc voltage across capacitor C_b is equal to the dc component of the voltage across transistor Q_2 , or

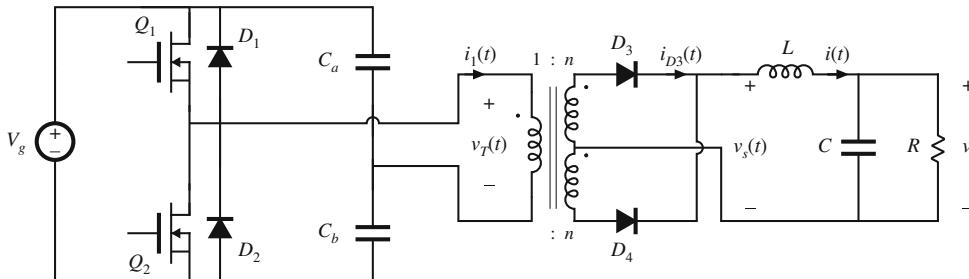


Fig. 6.22 Half-bridge transformer-isolated buck converter

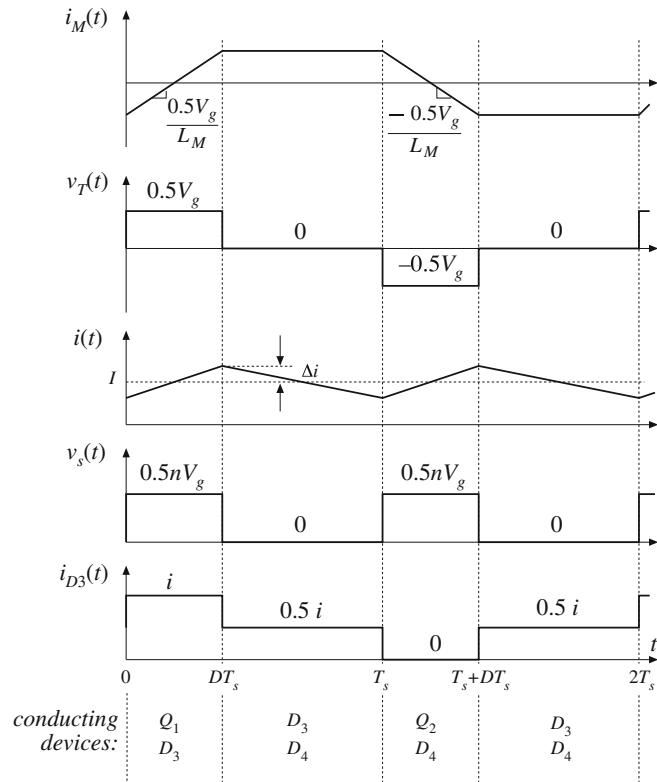


Fig. 6.23 Waveforms of the half-bridge transformer-isolated buck converter

$0.5V_g$. The transformer primary voltage $v_T(t)$ is then $0.5V_g$ when transistor Q_1 conducts, and $-0.5V_g$ when transistor Q_2 conducts. The magnitude of $v_T(t)$ is half as large as in the full-bridge configuration, with the result that the output voltage is reduced by a factor of 0.5:

$$V = 0.5nDV_g \quad (6.29)$$

The factor of 0.5 can be compensated for by doubling the transformer turns ratio n . However, this causes the transistor currents to double.

So the half-bridge configuration needs only two transistors rather than four, but these two transistors must handle currents that are twice as large as those of the full-bridge circuit. In consequence, the half-bridge configuration finds application at lower power levels, for which transistors with sufficient current rating are readily available, and where low parts count is important. Utilization of the transformer core and windings is essentially the same as in the full-bridge, and the peak transistor voltage is clamped to the dc input voltage V_g by diodes D_1 and D_2 . It is possible to omit capacitor C_a if desired. The current-programmed mode generally does not work with half-bridge converters.

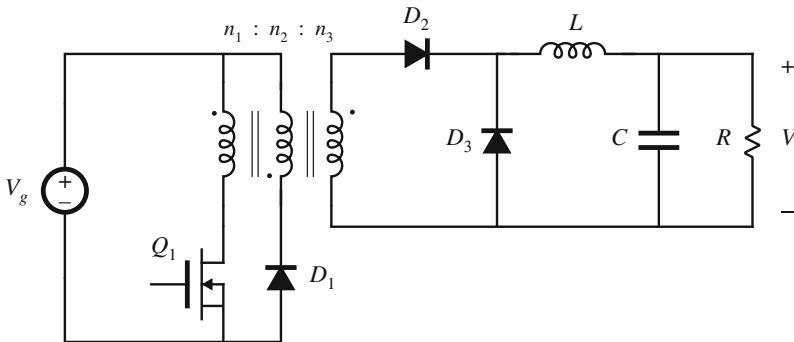


Fig. 6.24 Single-transistor forward converter

6.3.2 Forward Converter

The forward converter is illustrated in Fig. 6.24. This transformer-isolated converter is based on the buck converter. It requires a single transistor, and hence finds application at power levels lower than those commonly encountered in the full-bridge and half-bridge configurations. Its nonpulsating output current, shared with other buck-derived converters, makes the forward converter well suited for applications involving high output currents. The maximum transistor duty cycle is limited in value; for the common choice $n_1 = n_2$, the duty cycle is limited to the range $0 \leq D < 0.5$.

The transformer magnetizing current is reset to zero while the transistor is in the off state. How this occurs can be understood by replacing the three-winding transformer in Fig. 6.24 with the equivalent circuit of Fig. 6.18b. The resulting circuit is illustrated in Fig. 6.25, and typical waveforms are given in Fig. 6.26. The magnetizing inductance L_M , in conjunction with diode D_1 , must operate in the discontinuous conduction mode. The output inductor L , in conjunction with diode D_3 , may operate in either continuous or discontinuous conduction mode. The waveforms of Fig. 6.26 are sketched for continuous mode operation of inductor L . During each switching period, three subintervals then occur as illustrated in Fig. 6.27.

During subinterval 1, transistor Q_1 conducts and the circuit of Fig. 6.27a is obtained. Diode D_2 becomes forward-biased, while diodes D_1 and D_3 are reverse-biased. Voltage V_g is applied to the transformer primary winding, and hence the transformer magnetizing current $i_M(t)$ increases with a slope of V_g/L_M as illustrated in Fig. 6.26. The voltage across diode D_3 is equal to V_g , multiplied by the turns ratio n_3/n_1 .

The second subinterval begins when transistor Q_1 is switched off. The circuit of Fig. 6.27b is then obtained. The transformer magnetizing current $i_M(t)$ at this instant is positive, and must continue to flow. Since transistor Q_1 is off, the equivalent circuit model predicts that the magnetizing current must flow into the primary of the ideal transformer. It can be seen that $n_1 i_M$ ampere-turns flow out of the polarity mark of the primary winding. Hence, according to Eq. (6.16), an equal number of total ampere-turns must flow into the polarity marks of the other windings. Diode D_2 prevents current from flowing into the polarity mark of winding 3. Hence, the current $i_M n_1/n_2$ must flow into the polarity mark of winding 2. So diode D_1 becomes forward-biased, while

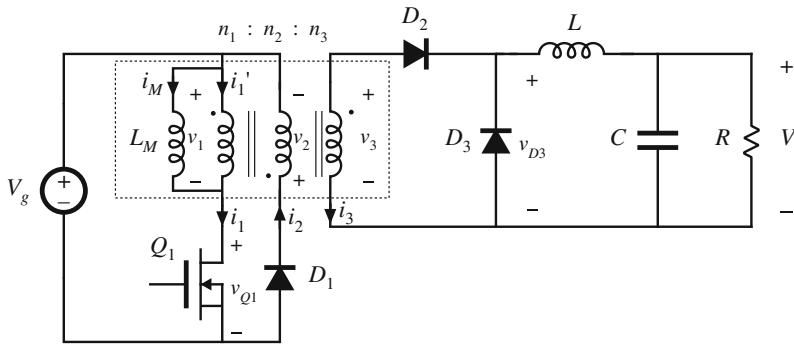
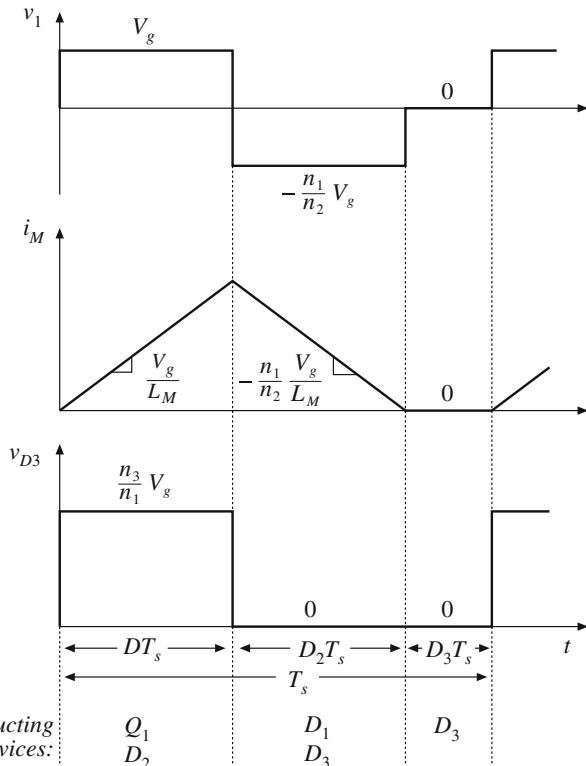


Fig. 6.25 Forward converter, with transformer equivalent circuit model

Fig. 6.26 Waveforms of the forward converter



diode D_2 is reverse-biased. Voltage V_g is applied to winding 2, and hence the voltage across the magnetizing inductance is $-V_g n_1 / n_2$, referred to winding 1. This negative voltage causes the magnetizing current to decrease, with a slope of $-V_g n_1 / n_2 L_M$. Since diode D_2 is reverse-biased, diode D_3 must turn on to conduct the output inductor current $i(t)$.

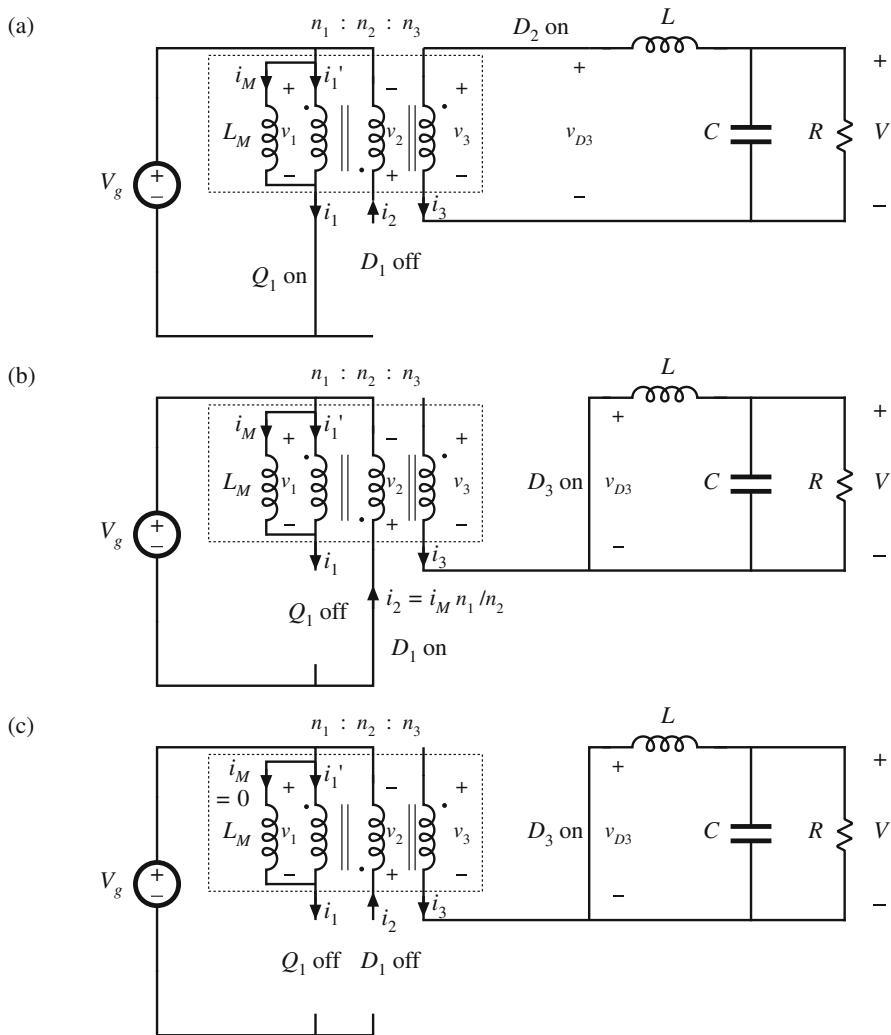


Fig. 6.27 Forward converter circuit: (a) during subinterval 1, (b) during subinterval 2, (c) during subinterval 3

When the magnetizing current reaches zero, diode D_1 becomes reverse-biased. Subinterval 3 then begins, and the circuit of Fig. 6.27c is obtained. Elements Q_1 , D_1 , and D_2 operate in the off state, and the magnetizing current remains at zero for the balance of the switching period.

By application of the principle of inductor volt-second balance to the transformer magnetizing inductance, the primary winding voltage $v_1(t)$ must have zero average. Referring to Fig. 6.26, the average of $v_1(t)$ is given by

$$\langle v_1 \rangle = D(V_g) + D_2(-V_g n_1/n_2) + D_3(0) = 0 \quad (6.30)$$

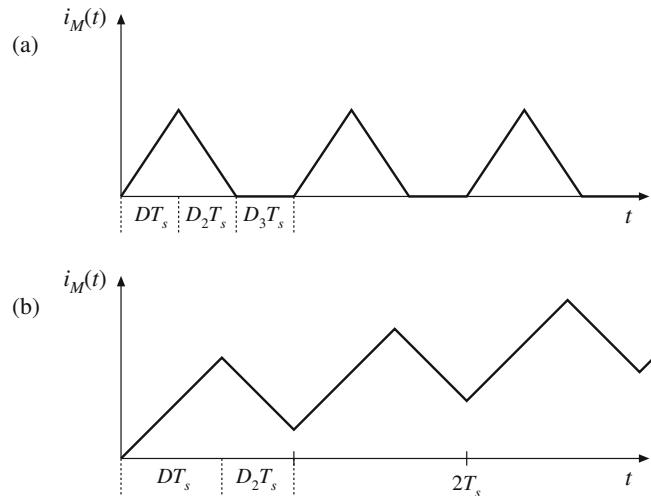


Fig. 6.28 Magnetizing current waveform, forward converter: (a) DCM, $D < 0.5$; (b) CCM, $D > 0.5$

Solution for the duty cycle D_2 yields

$$D_2 = \frac{n_2}{n_1} D \quad (6.31)$$

Note that the duty cycle D_3 cannot be negative. But since $D + D_2 + D_3 = 1$, we can write

$$D_3 = 1 - D - D_2 \geq 0 \quad (6.32)$$

Substitution of Eq. (6.31) into Eq. (6.32) leads to

$$D_3 = 1 - D \left(1 + \frac{n_2}{n_1} \right) \geq 0 \quad (6.33)$$

Solution for D then yields

$$D \leq \frac{1}{1 + \frac{n_2}{n_1}} \quad (6.34)$$

So the maximum duty cycle is limited. For the common choice $n_1 = n_2$, the limit becomes

$$D \leq \frac{1}{2} \quad (6.35)$$

If this limit is violated, then the transistor off-time is insufficient to reset the transformer magnetizing current to zero before the end of the switching period. Transformer saturation may then occur.

The transformer magnetizing current waveform $i_M(t)$ is illustrated in Fig. 6.28, for the typical case where $n_1 = n_2$. Figure 6.28a illustrates operation with $D < 0.5$. The magnetizing inductance, in conjunction with diode D_1 , operates in the discontinuous conduction mode, and $i_M(t)$ is reset to zero before the end of each switching period. Figure 6.28b illustrates what happens when the transistor duty cycle D is greater than 0.5. There is then no third subinterval, and the magnetizing inductance operates in continuous conduction mode. Furthermore, subinterval

2 is not long enough to reset the magnetizing current to zero. Hence, there is a net increase of $i_M(t)$ over each switching period. Eventually, the magnetizing current will become large enough to saturate the transformer.

The converter output voltage can be found by application of the principle of inductor volt-second balance to inductor L . The voltage across inductor L must have zero dc component, and therefore the dc output voltage V is equal to the dc component of diode D_3 voltage $v_{D3}(t)$. The waveform $v_{D3}(t)$ is illustrated in Fig. 6.26. It has an average value of

$$\langle v_{D3} \rangle = V = \frac{n_3}{n_1} DV_g \quad (6.36)$$

This is the solution of the forward converter in the continuous conduction mode. The solution is subject to the constraint given in Eq. (6.34).

It can be seen from Eq. (6.34) that the maximum duty cycle could be increased by decreasing the turns ratio n_2/n_1 . This would cause $i_M(t)$ to decrease more quickly during subinterval 2, resetting the transformer faster. Unfortunately, this also increases the voltage stress applied to transistor Q_1 . The maximum voltage applied to transistor Q_1 occurs during subinterval 2; solution of the circuit of Fig. 6.27b for this voltage yields

$$\max(v_{Q1}) = V_g \left(1 + \frac{n_1}{n_2} \right) \quad (6.37)$$

For the common choice $n_1 = n_2$, the voltage applied to the transistor during subinterval 2 is $2V_g$. In practice, a somewhat higher voltage is observed, due to ringing associated with the transformer leakage inductance. So decreasing the turns ratio n_2/n_1 allows increase of the maximum transistor duty cycle, at the expense of increased transistor blocking voltage.

A two-transistor version of the forward converter is illustrated in Fig. 6.29. Transistors Q_1 and Q_2 are controlled by the same gate drive signal, such that they both conduct during subinterval 1, and are off during subintervals 2 and 3. The secondary side of the converter is identical to the single-transistor forward converter; diode D_3 conducts during subinterval 1, while diode

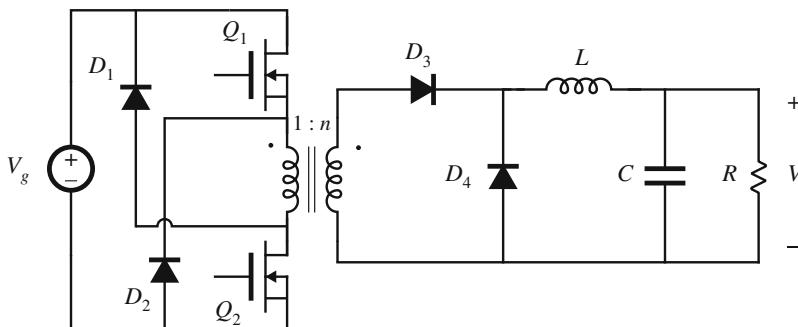


Fig. 6.29 Two-transistor forward converter

D_4 conducts during subintervals 2 and 3. During subinterval 2, the magnetizing current $i_M(t)$ forward-biases diodes D_1 and D_2 . The transformer primary winding is then connected to V_g , with polarity opposite to that of subinterval 1. The magnetizing current then decreases, with slope $-V_g/L_M$. When the magnetizing current reaches zero, diodes D_1 and D_2 become reverse-biased. The magnetizing current then remains at zero for the balance of the switching period. So operation of the two-transistor forward converter is similar to the single-transistor forward converter, in which $n_1 = n_2$. The duty cycle is limited to $D < 0.5$. This converter has the advantage that the transistor peak blocking voltage is limited to V_g , and is clamped by diodes D_1 and D_2 . Typical power levels of the two-transistor forward converter are similar to those of the half-bridge configuration.

The utilization of the transformer of the forward converter is quite good. Since the transformer magnetizing current cannot be negative, only half of the core B - H loop can be used. This would seemingly imply that the transformer cores of forward converters should be twice as large as those of full- or half-bridge converters. However, in modern high-frequency converters, the flux swing is constrained by core loss rather than by the core material saturation flux density. In consequence, the utilization of the transformer core of the forward converter can be as good as in the full- or half-bridge configurations. Utilization of the primary and secondary windings of the transformer is better than in the full-bridge, half-bridge, or push-pull configurations, since the forward converter requires no center-tapped windings. During subinterval 1, all of the available winding copper is used to transmit power to the load. Essentially no unnecessary current flows during subintervals 2 and 3. Typically, the magnetizing current is small compared to the reflected load current, and has negligible effect on the transformer utilization. So the transformer core and windings are effectively utilized in modern forward converters.

6.3.3 Push-Pull Isolated Buck Converter

The push-pull isolated buck converter is illustrated in Fig. 6.30. The secondary-side circuit is identical with the full- and half-bridge converters, with identical waveforms. The primary-side circuit contains a center-tapped winding. Transistor Q_1 conducts for time DT_s during the first switching period. Transistor Q_2 conducts for an identical length of time during the next switching period, such that volt-second balance is maintained across the transformer primary winding. Converter waveforms are illustrated in Fig. 6.31. This converter can operate over the entire range of duty cycles $0 \leq D < 1$. Its conversion ratio is given by

$$V = nDV_g \quad (6.38)$$

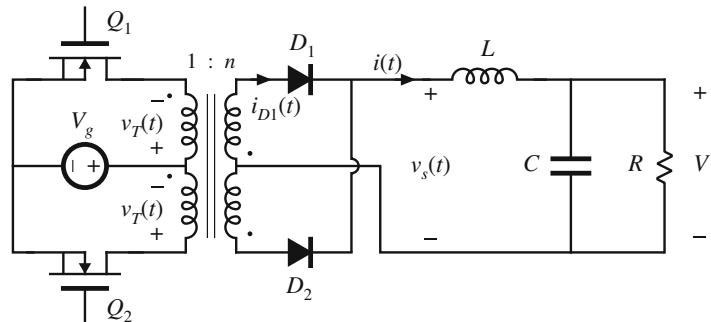


Fig. 6.30 Push-pull isolated buck converter

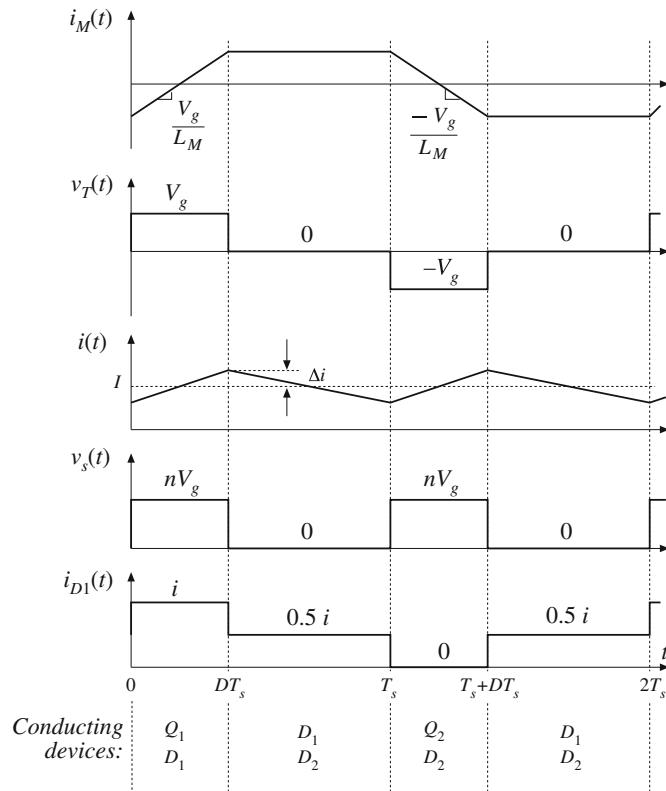


Fig. 6.31 Waveforms of the push-pull isolated buck converter

This converter is sometimes used in conjunction with low input voltages. It tends to exhibit low primary-side conduction losses, since at any given instant only one transistor is connected in series with the dc source V_g . The ability to operate with transistor duty cycles approaching unity also allows the turns ratio n to be minimized, reducing the transistor currents.

The push-pull configuration is prone to transformer saturation problems. Since it cannot be guaranteed that the forward voltage drops and conduction times of transistors Q_1 and Q_2 are exactly equal, small imbalances can cause the dc component of voltage applied to the transformer primary to be nonzero. In consequence, during every two switching periods there is a net increase in the magnitude of the magnetizing current. If this imbalance continues, then the magnetizing current can eventually become large enough to saturate the transformer.

Current-programmed control can be employed to mitigate the transformer saturation problems. Operation of the push-pull converter using only duty-cycle control is not recommended.

Utilization of the transformer core material and secondary winding is similar to that for the full-bridge converter. The flux and magnetizing current can be both positive and negative, and therefore the entire B - H loop can be used, if desired. Since the primary and secondary windings are both center-tapped, their utilization is suboptimal.

6.3.4 Flyback Converter

The flyback converter is based on the buck-boost converter. Its derivation is illustrated in Fig. 6.32. Figure 6.32a depicts the basic buck-boost converter, with the switch realized using a MOSFET and diode. In Fig. 6.32b, the inductor winding is constructed using two wires, with a 1:1 turns ratio. The basic function of the inductor is unchanged, and the parallel windings are equivalent to a single winding constructed of larger wire. In Fig. 6.32c, the connections between the two windings are broken. One winding is used while the transistor Q_1 conducts, while the other winding is used when diode D_1 conducts. The total current in the two windings is unchanged from the circuit of Fig. 6.32b; however, the current is now distributed between the windings differently. The magnetic fields inside the inductor in both cases are identical.

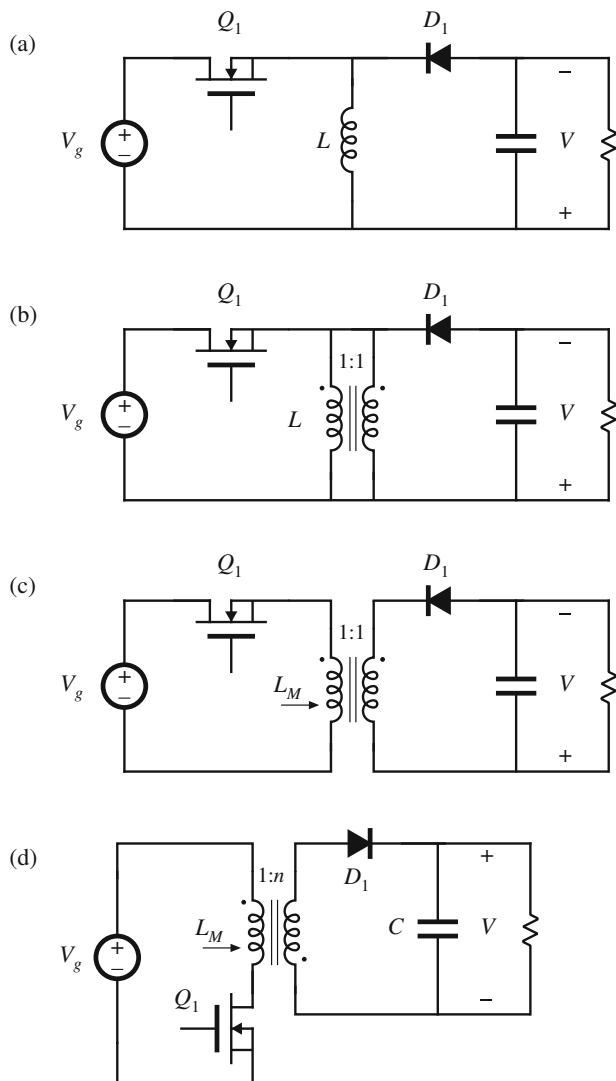


Fig. 6.32 Derivation of the flyback converter: (a) buck-boost converter; (b) inductor L is wound with two parallel wires; (c) inductor windings are isolated, leading to the flyback converter; (d) with a $1:n$ turns ratio and positive output

Although the two-winding magnetic device is represented using the same symbol as the transformer, a more descriptive name is “two-winding inductor.” This device is sometimes also called a *flyback transformer*. Unlike the ideal transformer, current does not flow simultaneously in both windings of the flyback transformer. Figure 6.32d illustrates the usual configuration of the flyback converter. The MOSFET source is connected to the primary-side ground, simplifying the gate drive circuit. The transformer polarity marks are reversed, to obtain a positive output voltage. A $1:n$ turns ratio is introduced; this allows better converter optimization.

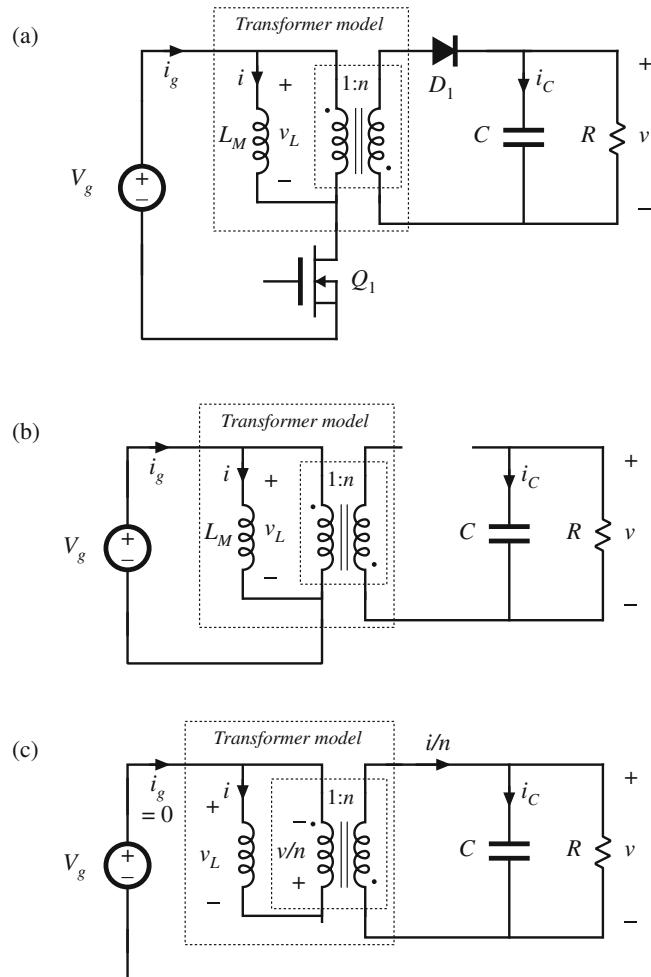


Fig. 6.33 Flyback converter circuit: (a) with transformer equivalent circuit model, (b) during subinterval 1, (c) during subinterval 2

The flyback converter may be analyzed by insertion of the model of Fig. 6.18b in place of the flyback transformer. The circuit of Fig. 6.33a is then obtained. The magnetizing inductance L_M functions in the same manner as inductor L of the original buck-boost converter of Fig. 6.32a. When transistor Q_1 conducts, energy from the dc source V_g is stored in L_M . When diode D_1 conducts, this stored energy is transferred to the load, with the inductor voltage and current scaled according to the $1:n$ turns ratio.

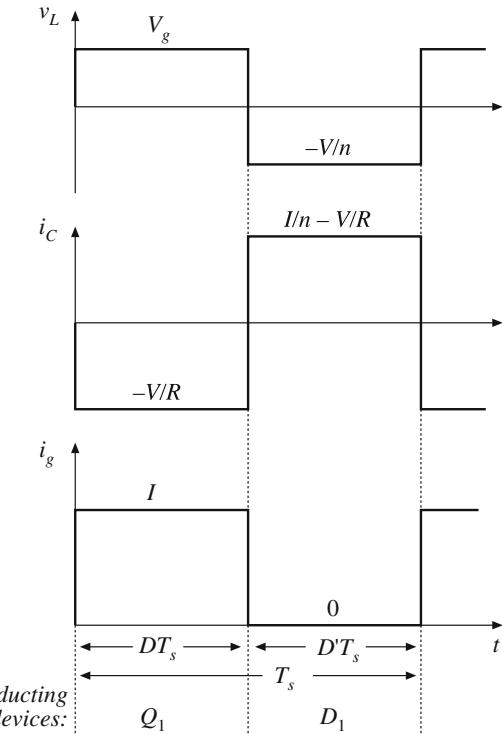


Fig. 6.34 Flyback converter waveforms, continuous conduction mode

During subinterval 1, while transistor Q_1 conducts, the converter circuit model reduces to Fig. 6.33b. The inductor voltage v_L , capacitor current i_C , and dc source current i_g are given by

$$\begin{aligned} v_L &= V_g \\ i_C &= -\frac{v}{R} \\ i_g &= I \end{aligned} \quad (6.39)$$

With the assumption that the converter operates in the continuous conduction mode, with small inductor current ripple and small capacitor voltage ripple, the magnetizing current i and output capacitor voltage v can be approximated by their dc components, I and V , respectively. Equation (6.39) then becomes

$$\begin{aligned} v_L &= V_g \\ i_C &= -\frac{V}{R} \\ i_g &= I \end{aligned} \quad (6.40)$$

During the second subinterval, the transistor is in the off state, and the diode conducts. The equivalent circuit of Fig. 6.33c is obtained. The primary-side magnetizing inductance voltage v_L , the capacitor current i_C , and the dc source current i_g for this subinterval are

$$\begin{aligned} v_L &= -\frac{v}{n} \\ i_C &= \frac{i}{n} - \frac{v}{R} \\ i_g &= 0 \end{aligned} \quad (6.41)$$

It is important to consistently define $v_L(t)$ on the same side of the transformer for all subintervals. Upon making the small-ripple approximation, one obtains

$$\begin{aligned} v_L &= -\frac{V}{n} \\ i_C &= \frac{I}{n} - \frac{V}{R} \\ i_g &= 0 \end{aligned} \quad (6.42)$$

The $v_L(t)$, $i_C(t)$, and $i_g(t)$ waveforms are sketched in Fig. 6.34 for continuous conduction mode operation.

Application of the principle of volt-second balance to the primary-side magnetizing inductance yields

$$\langle v_L \rangle = D(V_g) + D' \left(-\frac{V}{n} \right) = 0 \quad (6.43)$$

Solution for the conversion ratio then leads to

$$M(D) = \frac{V}{V_g} = n \frac{D}{D'} \quad (6.44)$$

So the conversion ratio of the flyback converter is similar to that of the buck-boost converter, but contains an added factor of n .

Application of the principle of charge balance to the output capacitor C leads to

$$\langle i_C \rangle = D \left(-\frac{V}{R} \right) + D' \left(\frac{I}{n} - \frac{V}{R} \right) = 0 \quad (6.45)$$

Solution for I yields

$$I = \frac{nV}{D'R} \quad (6.46)$$

This is the dc component of the magnetizing current, referred to the primary. The dc component of the source current i_g is

$$I_g = \langle i_g \rangle = D(I) + D'(0) \quad (6.47)$$

An equivalent circuit that models the dc components of the flyback converter waveforms can now be constructed. Circuits corresponding to the inductor loop equation (6.43) and to node equations (6.45) and (6.47) are illustrated in Fig. 6.35a. By replacing the dependent sources with ideal dc transformers, one obtains Fig. 6.35b. This is the dc equivalent circuit of the flyback converter. It contains a $1:D$ buck-type conversion ratio, followed by a $D' : 1$ boost-type conversion ratio, and an added factor of $1:n$ arising from the flyback transformer turns ratio. By use of the method developed in Chap. 3, the model can be refined to account for losses and to predict the converter efficiency. The flyback converter can also be operated in the discontinuous conduction mode; analysis is left as a homework problem. The results are similar to the DCM buck-boost converter results tabulated in Chap. 5, but are generalized to account for the turns ratio $1:n$.

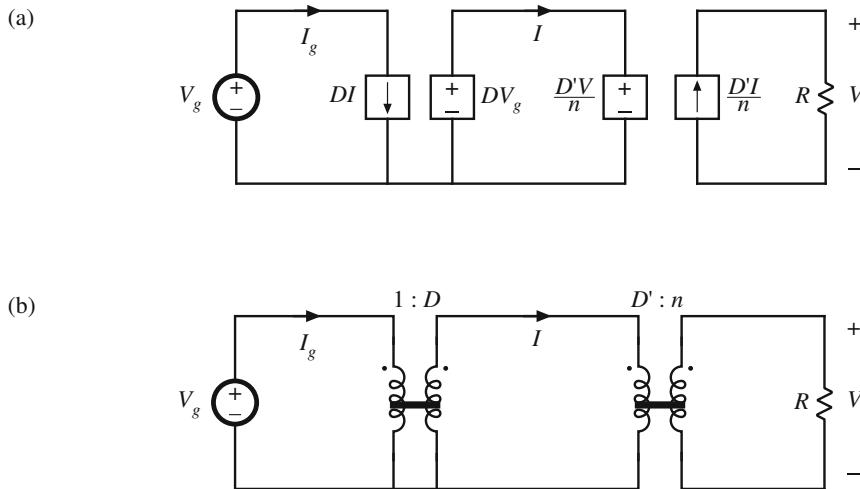


Fig. 6.35 Flyback converter equivalent circuit model, CCM: (a) circuits corresponding to Eqs. (6.43), (6.45), and (6.47); (b) equivalent circuit containing ideal dc transformers

The flyback converter is commonly used at the 50 to 100 W power range, as well as in high-voltage power supplies for televisions and computer monitors. It has the advantage of very low parts count. Multiple outputs can be obtained using a minimum number of parts: each additional output requires only an additional winding, diode, and capacitor. However, in comparison with the full-bridge, half-bridge, or two-transistor forward converters, the flyback converter has the disadvantages of high transistor voltage stress and poor cross-regulation. The peak transistor voltage is equal to the dc input voltage V_g plus the reflected load voltage V/n ; in practice, additional voltage is observed due to ringing associated with the transformer leakage inductance. Rigorous comparison of the utilization of the flyback transformer with the transformers of buck-derived circuits is difficult because of the different functions performed by these elements. The magnetizing current of the flyback transformer is unipolar, and hence no more than half of the core material $B-H$ loop can be utilized. The magnetizing current must contain a significant dc component. Yet, the size of the flyback transformer is quite small in designs intended to operate in the discontinuous conduction mode. However, DCM operation leads to increased peak currents in the transistor, diode, and filter capacitors. Continuous conduction mode designs require larger values of L_M , and hence larger flyback transformers, but the peak currents in the power-stage elements are lower.

6.3.5 Boost-Derived Isolated Converters

Transformer-isolated boost converters can be derived by inversion of the source and load of buck-derived isolated converters. A number of configurations are known, and two of these are briefly discussed here. These converters find some employment in high-voltage power supplies, as well as in low-harmonic rectifier applications.

A full-bridge configuration is diagrammed in Fig. 6.36, and waveforms for the continuous conduction mode are illustrated in Fig. 6.37. The circuit topologies during the first and second

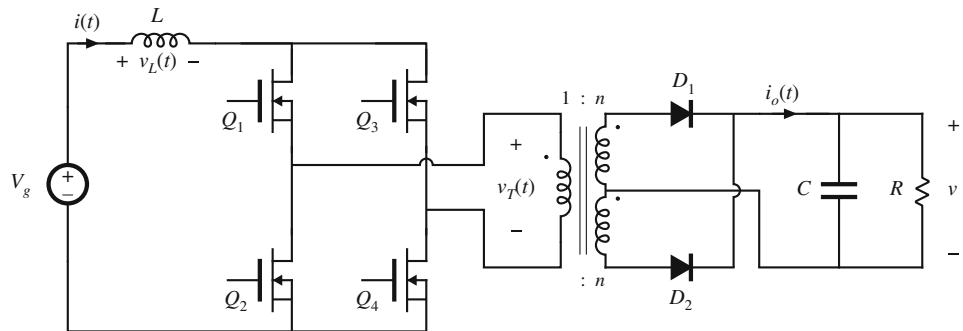


Fig. 6.36 Full-bridge transformer-isolated boost converter

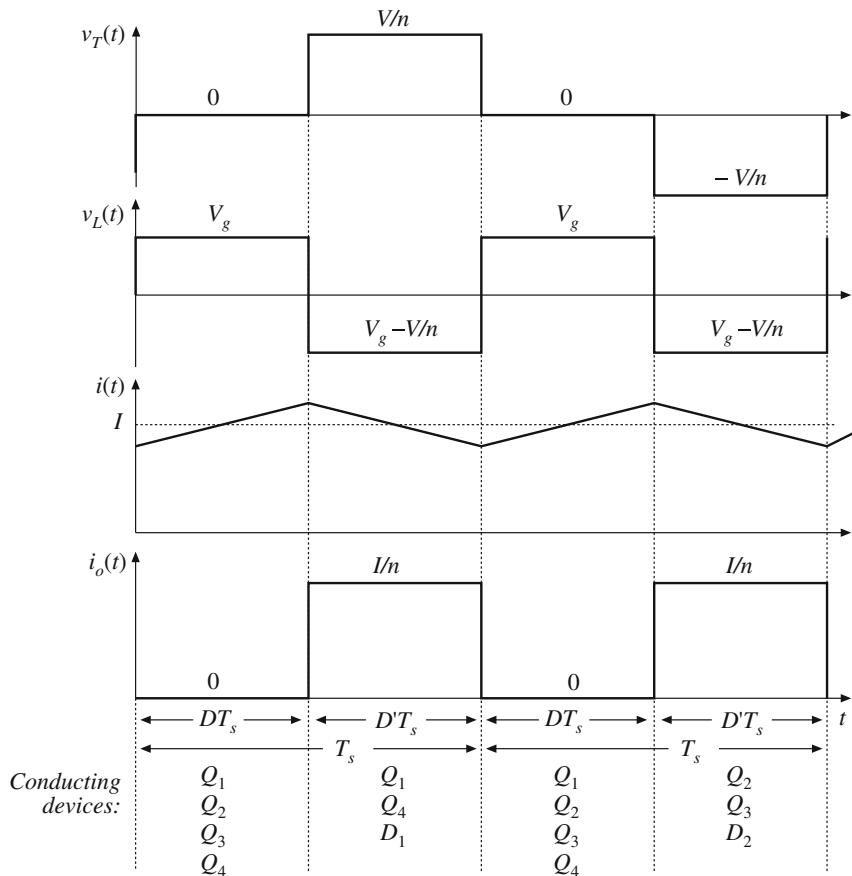


Fig. 6.37 Waveforms of the transformer-isolated full-bridge boost converter, CCM

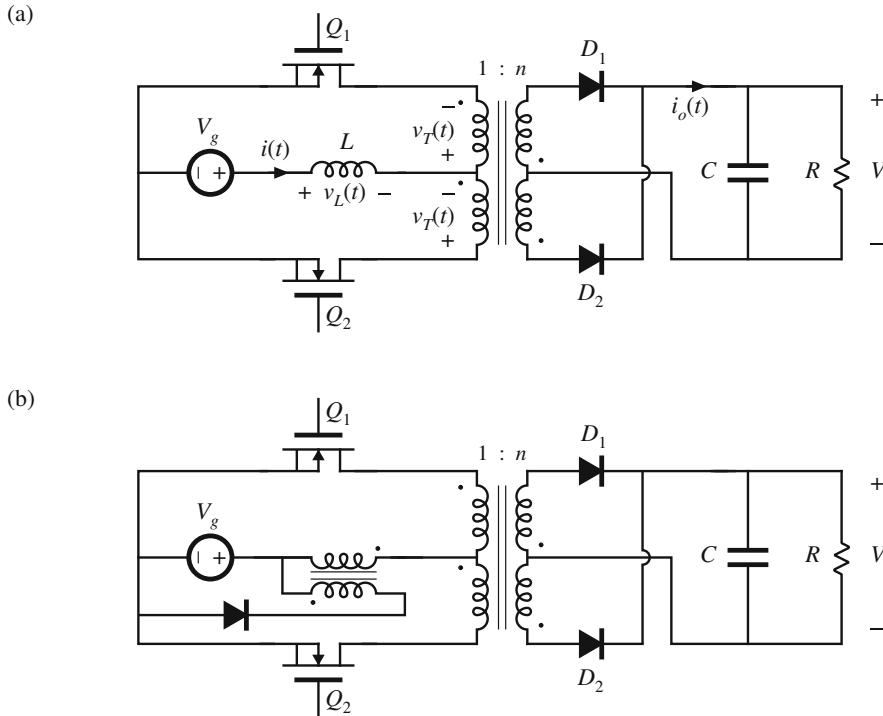


Fig. 6.38 Push-pull isolated converters: (a) based on the boost converter, (b) based on the Watkins–Johnson converter

subintervals are equivalent to those of the basic nonisolated boost converter, and when the turns ratio is 1:1, the inductor current $i(t)$ and output current $i_o(t)$ waveforms are identical to the inductor current and diode current waveforms of the nonisolated boost converter.

During subinterval 1, all four transistors operate in the on state. This connects the inductor L across the dc input source V_g , and causes diodes D_1 and D_2 to be reverse-biased. The inductor current $i(t)$ increases with slope V_g/L , and energy is transferred from the dc source V_g to inductor L . During the second subinterval, transistors Q_2 and Q_3 operate in the off state, so that inductor L is connected via transistors Q_1 and Q_4 through the transformer and diode D_1 to the dc output. The next switching period is similar, except that during subinterval 2, transistors Q_1 and Q_4 operate in the off state, and inductor L is connected via transistors Q_2 and Q_3 through the transformer and diode D_2 to the dc output. If the transistor off-times and the diode forward drops are identical, then the average transformer voltage is zero, and the net volt-seconds applied to the transformer magnetizing inductance over two switching periods is zero.

Application of the principle of inductor volt-second balance to the inductor voltage waveform $v_L(t)$ yields

$$\langle v_L \rangle = D(V_g) + D' \left(V_g - \frac{V}{n} \right) = 0 \quad (6.48)$$

Solution for the conversion ratio $M(D)$ then leads to

$$M(D) = \frac{V}{V_g} = \frac{n}{D'} \quad (6.49)$$

This result is similar to the boost converter $M(D)$, with an added factor of n due to the transformer turns ratio.

The transistors must block the reflected load voltage $V/n = V_g/D'$. In practice, additional voltage is observed due to ringing associated with the transformer leakage inductance. Because the instantaneous transistor current is limited by inductor L , saturation of the transformer due to small imbalances in the semiconductor forward voltage drops or conduction times is not catastrophic. Indeed, control schemes are known in which the transformer is purposely operated in saturation during subinterval 1 [53, 55].

A push-pull configuration is depicted in Fig. 6.38a. This configuration requires only two transistors, each of which must block voltage $2V/n$. Operation is otherwise similar to that of the full-bridge. During subinterval 1, both transistors conduct. During subinterval 2, one of the transistors operates in the off state, and energy is transferred from the inductor through the transformer and one of the diodes to the output. Transistors conduct during subinterval 2 during alternate switching periods, such that transformer volt-second balance is maintained. A similar push-pull version of the Watkins–Johnson converter, converter 6 of Fig. 6.15, is illustrated in Fig. 6.38b.

6.3.6 Isolated Versions of the SEPIC and the Ćuk Converter

The artifice used to obtain isolation in the flyback converter can also be applied to the SEPIC and inverse-SEPIC. Referring to Fig. 6.39a, inductor L_2 can be realized using two windings, leading to the isolated SEPIC of Fig. 6.39b. An equivalent circuit is given in Fig. 6.39c. It can be seen that the magnetizing inductance performs the energy storage function of the original inductor L_2 . In addition, the ideal transformer provides isolation and a turns ratio.

Typical primary and secondary winding current waveforms $i_p(t)$ and $i_s(t)$ are portrayed in Fig. 6.40, for the continuous conduction mode. The magnetic device must function as both a flyback transformer and also a conventional two-winding transformer. During subinterval 1, while transistor Q_1 conducts, the magnetizing current flows through the primary winding, and the secondary winding current is zero. During subinterval 2, while diode D_1 conducts, the magnetizing current flows through the secondary winding to the load. In addition, the input inductor current i_1 flows through the primary winding. This induces an additional component of secondary current i_1/n , which also flows to the load. So design of the SEPIC transformer is somewhat unusual, and the rms winding currents are larger than those of the flyback transformer.

By application of the principle of volt-second balance to inductors L_1 and L_M , the conversion ratio can be shown to be

$$M(D) = \frac{V}{V_g} = \frac{nD}{D'} \quad (6.50)$$

Ideally, the transistor must block voltage V_g/D' . In practice, additional voltage is observed due to ringing associated with the transformer leakage inductance.

An isolated version of the inverse-SEPIC is shown in Fig. 6.41. Operation and design of the transformer is similar to that of the SEPIC.

Isolation in the Ćuk converter is obtained in a different manner [58]. The basic nonisolated Ćuk converter is illustrated in Fig. 6.42a. In Fig. 6.42b, capacitor C_1 is split into two series capacitors C_{1a} and C_{1b} . A transformer can now be inserted between these capacitors, as indicated in Fig. 6.42c. The polarity marks have been reversed, so that a positive output voltage is obtained.

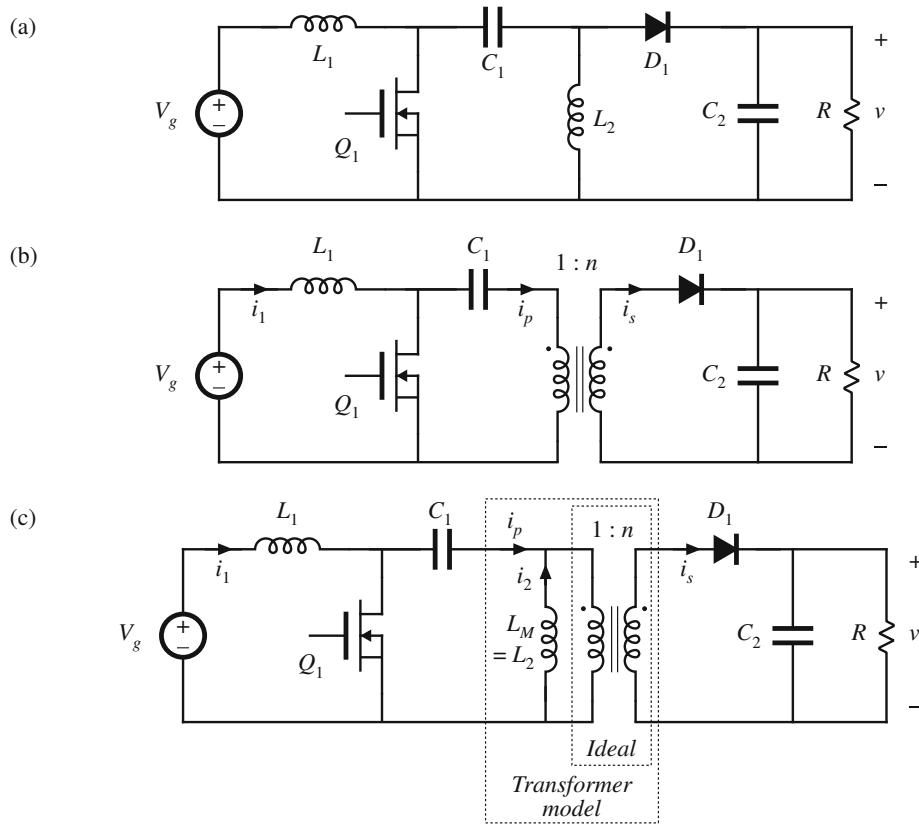


Fig. 6.39 Obtaining isolation in the SEPIC: (a) basic nonisolated converter, (b) isolated SEPIC, (c) with transformer equivalent circuit model

Having capacitors in series with the transformer primary and secondary windings ensures that no dc voltage is applied to the transformer. The transformer functions in a conventional manner, with small magnetizing current and negligible energy storage within the magnetizing inductance.

Utilization of the transformer of the Ćuk converter is quite good. The magnetizing current can be both positive and negative, and hence the entire core $B-H$ loop can be utilized if desired. There are no center-tapped windings, and all of the copper is effectively utilized. The transistor must block voltage V_g/D' , plus some additional voltage due to ringing associated with the transformer leakage inductance. The conversion ratio is identical to that of the isolated SEPIC, Eq. (6.50).

The isolated SEPIC and Ćuk converter find application as switching power supplies, typically at power levels of several hundred watts. They also find use as ac–dc low-harmonic rectifiers.

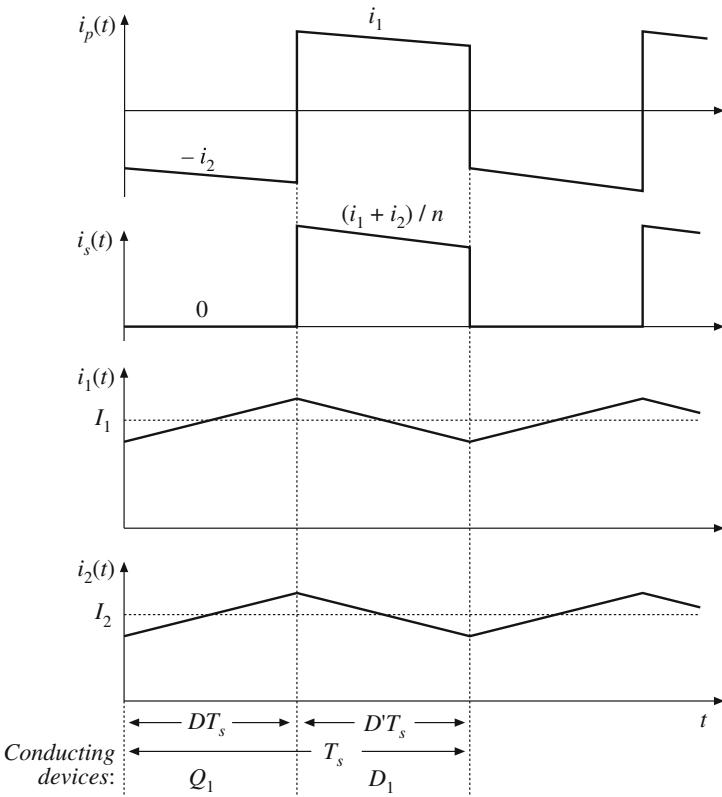


Fig. 6.40 Waveforms of the isolated SEPIC, continuous conduction mode

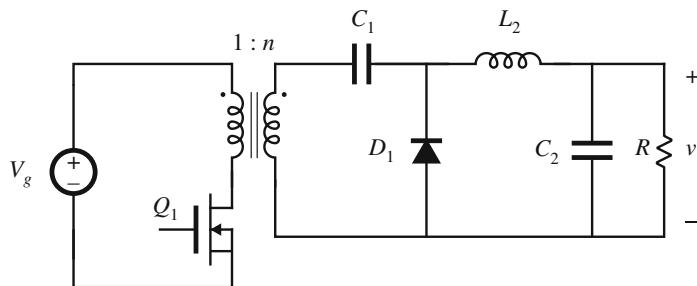


Fig. 6.41 Isolated inverse-SEPIC

1. The boost converter can be viewed as an inverse buck converter, while the buck-boost and Cuk converters arise from cascade connections of buck and boost converters. The properties of these converters are consistent with their origins. Ac outputs can be obtained by differential connection of the load. An infinite number of converters are possible, and several are listed in this chapter.
2. For understanding the operation of most converters containing transformers, the transformer can be modeled as a magnetizing inductance in parallel with an ideal transformer. The mag-

6.4 Summary of Key Points

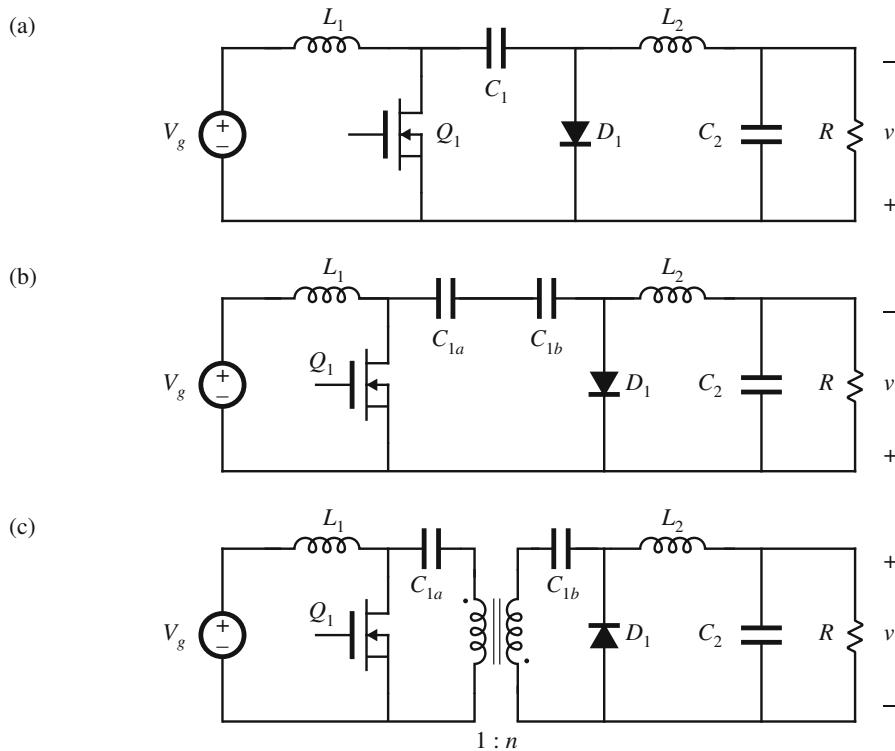


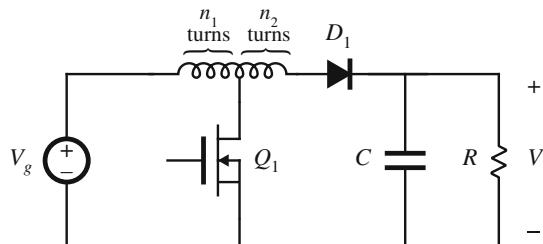
Fig. 6.42 Obtaining isolation in the Ćuk converter: (a) basic nonisolated Ćuk converter, (b) splitting capacitor C_1 into two series capacitors, (c) insertion of transformer between capacitors

netizing inductance must obey all of the usual rules for inductors, including the principle of volt-second balance.

3. The steady-state behavior of transformer-isolated converters may be understood by first replacing the transformer with the magnetizing-inductance-plus-ideal-transformer equivalent circuit. The techniques developed in the previous chapters can then be applied, including use of inductor volt-second balance and capacitor charge balance to find dc currents and voltages, use of equivalent circuits to model losses and efficiency, and analysis of the discontinuous conduction mode.
4. In the full-bridge, half-bridge, and push-pull isolated versions of the buck and/or boost converters, the transformer frequency is twice the output ripple frequency. The transformer is reset while it transfers energy: the applied voltage polarity alternates on successive switching periods.
5. In the conventional forward converter, the transformer is reset while the transistor is off. The transformer magnetizing inductance operates in the discontinuous conduction mode, and the maximum duty cycle is limited.
6. The flyback converter is based on the buck-boost converter. The flyback transformer is actually a two-winding inductor, which stores and transfers energy.

PROBLEMS

Fig. 6.43 Tapped-inductor boost converter, Problem 6.1



- 6.1** Tapped-inductor boost converter. The boost converter is sometimes modified as illustrated in Fig. 6.43, to obtain a larger conversion ratio than would otherwise occur. The inductor winding contains a total of $(n_1 + n_2)$ turns. The transistor is connected to a tap placed n_1 turns from the left side of the inductor, as shown. The tapped inductor can be viewed as a two-winding $(n_1 : n_2)$ transformer, in which the two windings are connected in series. The inductance of the entire $(n_1 + n_2)$ turn winding is L .
- Sketch an equivalent circuit model for the tapped inductor, which includes a magnetizing inductance and an ideal transformer. Label the values of the magnetizing inductance and turns ratio.
 - Determine an analytical expression for the conversion ratio $M = V/V_g$. You may assume that the transistor, diode, tapped inductor, and capacitor are lossless. You may also assume that the converter operates in continuous conduction mode.
 - Sketch $M(D)$ vs. D for $n_1 = n_2$, and compare to the nontapped ($n_2 = 0$) case.
- 6.2** Analysis of the DCM flyback converter. The flyback converter of Fig. 6.32d operates in the discontinuous conduction mode.
- Model the flyback transformer as a magnetizing inductance in parallel with an ideal transformer, and sketch the converter circuits during the three subintervals.
 - Derive the conditions for operation in discontinuous conduction mode.
 - Solve the converter: derive expressions for the steady-state output voltage V and subinterval 2 (diode conduction interval) duty cycle D_2 .
- 6.3** Analysis of the isolated inverse-SEPIC of Fig. 6.41. You may assume that the converter operates in the continuous conduction mode, and that all inductor current ripples and capacitor voltage ripples are small.
- Derive expressions for the dc components of the magnetizing current, inductor current, and capacitor voltages.
 - Derive analytical expressions for the rms values of the primary and secondary winding currents. Note that these quantities do not simply scale by the turns ratio.
- 6.4** The two-transistor flyback converter. The converter of Fig. 6.44 is sometimes used when the dc input voltage is high. Transistors Q_1 and Q_2 are driven with the same gating signal, such that they turn on and off simultaneously with the same duty cycle D . Diodes D_1 and D_2 ensure that the off-state voltages of the transistors do not exceed V_g . The converter operates in discontinuous conduction mode. The magnetizing inductance, referred to the primary side, is L_M .

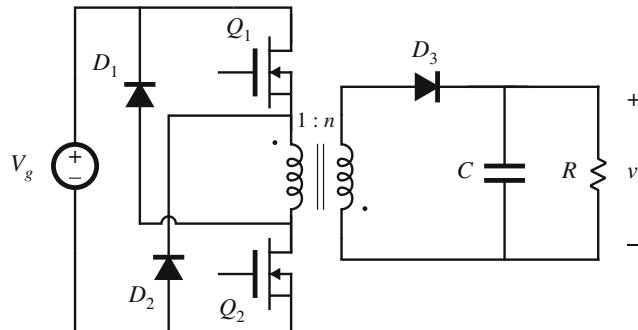


Fig. 6.44 Two-transistor flyback converter, Problem 6.4

- (a) Determine an analytical expression for the steady-state output voltage V .
 (b) Over what range of duty cycles does the transformer reset properly? Explain.
- 6.5** A nonideal flyback converter. The flyback converter shown in Fig. 6.32d operates in the continuous conduction mode. The MOSFET has on-resistance R_{on} , and the diode has a constant forward voltage drop V_D . The flyback transformer has primary winding resistance R_p and secondary winding resistance R_s .
- (a) Derive a complete steady-state equivalent circuit model, which is valid in the continuous conduction mode, and which correctly models the loss elements listed above as well as the converter input and output ports. Sketch your equivalent circuit.
 (b) Derive an analytical expression for the converter efficiency.
- 6.6** A low-voltage computer power supply with synchronous rectification. The trend in digital integrated circuits is towards lower power supply voltages. It is difficult to construct a high-efficiency low-voltage power supply, because the conduction loss arising in the secondary-side diodes becomes very large. The objective of this problem is to estimate how the efficiency of a forward converter varies as the output voltage is reduced, and to investigate the use of synchronous rectifiers.
- The forward converter of Fig. 6.24 operates from a dc input of $V_g = 325$ V, and supplies 20 A to its dc load. Consider three cases: (i) $V = 5$ V, (ii) $V = 3.3$ V, and (iii) $V = 1.5$ V. For each case, the turns ratio n_3/n_1 is chosen such that the converter produces the required output voltage at a transistor duty cycle of $D = 0.4$. The MOSFET has on-resistance $R_{on} = 5 \Omega$. The secondary-side Schottky diodes have forward voltage drops of $V_F = 0.5$ V. All other elements can be considered ideal.
- (a) Derive an equivalent circuit for the forward converter, which models the semiconductor conduction losses described above.
 (b) Solve your model for cases (i), (ii), and (iii) described above. For each case, determine numerical values of the turns ratio n_3/n_1 and for the efficiency η .
 (c) The secondary-side Schottky diodes are replaced by MOSFETs operating as synchronous rectifiers. The MOSFETs each have an on-resistance of $4 \text{ m}\Omega$. Determine the new numerical values of the turns ratio n_3/n_1 and the efficiency η , for cases (i), (ii), and (iii).
- 6.7** Rotation of switching cells. A network containing switches and reactive elements has terminals a , b , and c , as illustrated in Fig. 6.45a. You are given that the relationship between the terminal voltages is $V_{bc}/V_{ac} = \mu(D)$.

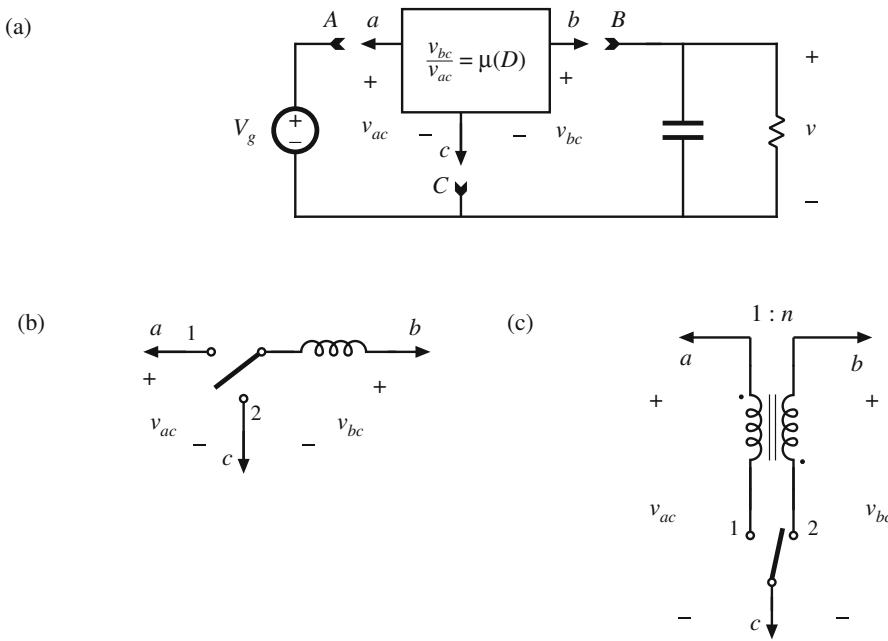
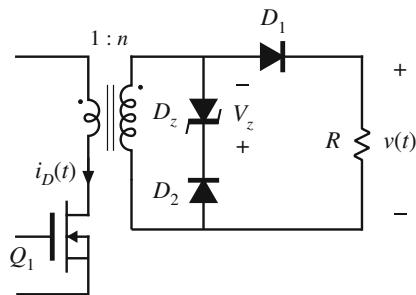


Fig. 6.45 Rotation of three-terminal switching cells, Problem 6.7

- (a) Derive expressions for the source-to-load conversion ratio $V/V_g = M(D)$, in terms of $\mu(D)$, for the following three connection schemes:
- a - A b - B c - C
 - a - B b - C c - A
 - a - C b - A c - B
- (b) Consider the three-terminal network of Fig. 6.45b. Determine $\mu(D)$ for this network. Plug your answer into your results from part (a), to verify that the buck, boost, and buck-boost converters are generated.
- (c) Consider the three-terminal network of Fig. 6.45c. Determine $\mu(D)$ for this network. Plug your answer into your results from part (a). What converters are generated?
- 6.8** Transformer-isolated current-sense circuit. It is often required that the current flowing in a power transistor be sensed. A noninductive resistor R placed in series with the transistor will produce a voltage $v(t)$ that is proportional to the transistor drain current $i_D(t)$. Use of a transformer allows isolation between the power transistor and the control circuit. The transformer turns ratio also allows reduction of the current and power loss and increase of the voltage of the resistor. This problem is concerned with design of the transformer-isolated current-sense circuit of Fig. 6.46.
- The transformer has a single-turn primary and an n -turn secondary winding. The transistor switches on and off with duty cycle D and switching frequency f_s . While the transistor conducts, its current is essentially constant and is equal to I . Diodes D_1 and D_2 are conventional silicon diodes having forward voltage drop V_D . Diode D_Z is a Zener diode, which can be modeled as a voltage source of value V_Z , with the polarity indicated in the fig-

Fig. 6.46 Transformer-isolated circuit for sensing the transistor switch current, Problem 6.8



ure. For a proper design, the circuit elements should be chosen such that the transformer magnetizing current, in conjunction with diode D_2 , operates in discontinuous conduction mode. In a good design, the magnetizing current is much smaller than the transistor current. Three subintervals occur during each switching period: subinterval 1, in which Q_1 and D_1 conduct; subinterval 2, in which D_2 and D_Z conduct; subinterval 3, in which Q_1 , D_1 and D_2 are off.

- (a) Sketch the current-sense circuit, replacing the transformer and zener diode by their equivalent circuits.
- (b) Sketch the waveforms of the transistor current $i_D(t)$, the transformer magnetizing current $i_M(t)$, the primary winding voltage, and the voltage $v(t)$. Label salient features.
- (c) Determine the conditions on the Zener voltage V_Z that ensure that the transformer magnetizing current is reset to zero before the end of the switching period.
- (d) You are given the following specifications:

Switching frequency	$f_s = 100 \text{ kHz}$
Transistor duty cycle	$D \leq 0.75$
Transistor peak current	$\max i_D(t) \leq 25 \text{ A}$

The output voltage $v(t)$ should equal 5 V when the transistor current is 25 A. To avoid saturating the transformer core, the volt-seconds applied to the single-turn primary winding while the transistor conducts should be no greater than 2 volt- μsec . The silicon diode forward voltage drops are $V_D = 0.7 \text{ V}$.

Design the circuit: select values of R , n , and V_Z .

- 6.9** Optimal reset of the forward converter transformer. As illustrated in Fig. 6.47, it is possible to reset the transformer of the forward converter using a voltage source other than the dc input V_g ; several such schemes appear in the literature. By optimally choosing the value of the reset voltage V_r , the peak voltage stresses imposed on transistor Q_1 and diode D_2 can be reduced. The maximum duty cycle can also be increased, leading to a lower transformer turns ratio and lower transistor current. The resulting improvement in converter cost and efficiency can be significant when the dc input voltage varies over a wide range.

- (a) As a function of V_g , the transistor duty cycle D , and the transformer turns ratios, what is the minimum value of V_r that causes the transformer magnetizing current to be reset to zero by the end of the switching period?
- (b) For your choice of V_r from part (a), what is the peak voltage imposed on transistor Q_1 ?

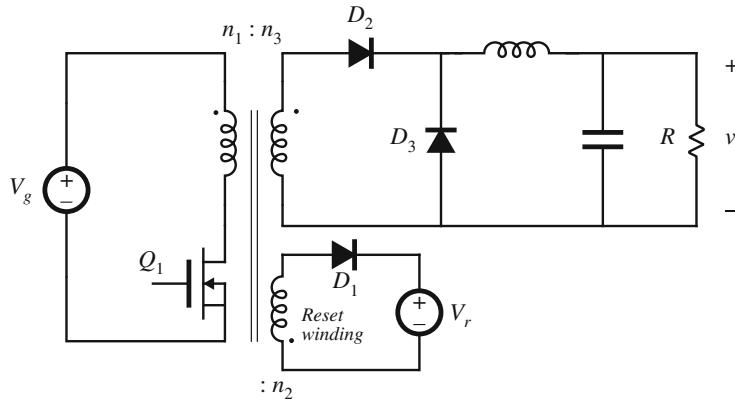


Fig. 6.47 Forward converter with auxiliary reset winding, Problem 6.9

This converter is to be used in a universal-input off-line application, with the following specifications. The input voltage V_g can vary between 127 and 380 V. The load voltage is regulated by variation of the duty cycle, and is equal to 12 V. The load power is 480 W.

- (c) Choose the turns ratio n_3/n_1 such that the total active switch stress is minimized. For your choice of n_3/n_1 , over what range will the duty cycle vary? What is the peak transistor current?
- (d) Compare your design of Part (c) with the conventional scheme in which $n_1 = n_2$ and $V_r = V_g$. Compare the worst-case peak transistor voltage and peak transistor current.
- (e) Suggest a way to implement the voltage source V_r . Give a schematic of the power stage components of your implementation. Use a few sentences to describe the control-circuit functions required by your implementation, if any.

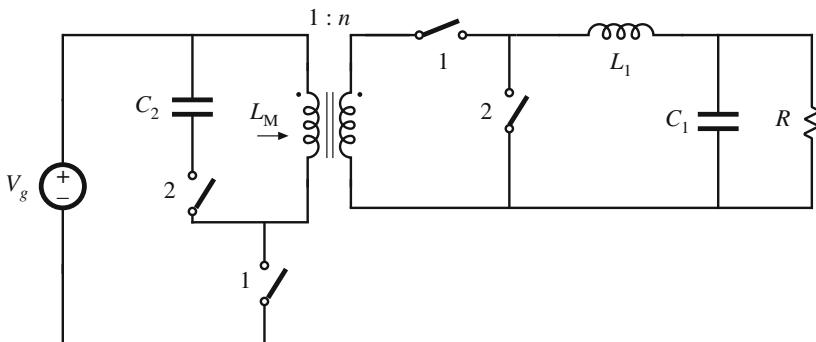


Fig. 6.48 Forward converter of Problem 6.10

- 6.10** In the converter illustrated in Fig. 6.48, the transformer has magnetizing inductance L_M referred to the primary side, and has turns ratio $1 : n$. It is desired that all elements operate

in the continuous conduction mode (CCM) over the range $0 \leq D < 1$. This mode is defined as follows: each switching period contains two subintervals numbered 1 and 2; in the schematic illustrated in Fig. 6.48, switches labeled “1” conduct during subinterval 1 for time DT_s , and switches labeled “2” conduct during subinterval 2 for time $(1 - D)T_s$.

- (a) Solve the converter in steady state, to find the dc components of both capacitor voltages and both inductor currents.
- (b) Sketch both capacitor voltage waveforms and both inductor current waveforms, including dc components and ripples.
- (c) Show how to realize the switches using BJTs and diodes, so that the converter operates in CCM over the range $0 \leq D < 1$.
- (d) Does the transformer reset properly (*i.e.*, do the volt-seconds balance on L_M) for $D > 0.5$? Explain.

6.11 A flyback converter with core loss and diode reverse recovery

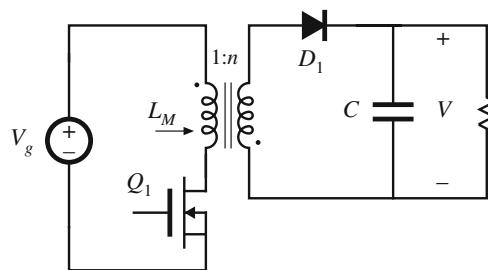


Fig. 6.49 Flyback converter

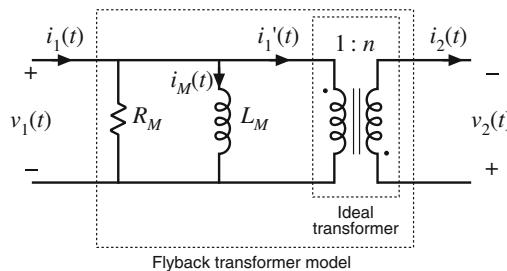


Fig. 6.50 Transformer equivalent circuit model, with core loss modeled by element R_M

A flyback converter is illustrated in Fig. 6.49. This converter operates in continuous conduction mode. The following two loss mechanisms are significant in this converter: diode reverse recovery, and transformer core loss. All other loss mechanisms can be ignored.

- The silicon diode D_1 has reverse recovery time t_r and recovered charge Q_r . You may model these parameters as being independent of current.

- The transformer core loss may be modeled using a resistor R_M in parallel with the magnetizing inductance L_M . This leads to the transformer equivalent circuit illustrated in Fig. 6.50.
- (a) Derive a dc equivalent circuit model for this converter. Your model should include the effects of the diode reverse-recovery process and the transformer core loss.
 (b) Derive an expression for the converter efficiency. It is not necessary to eliminate V_g , V , and I_M from your answer to this part.
 (c) The element values are $V_g = 24$ V, $f_s = 100$ kHz, $R = 15 \Omega$, $D = 0.4$, $n = 2$, $R_M = 240 \Omega$, $Q_r = 0.75 \mu\text{Coul}$, $t_r = 75$ nsec. Compute the efficiency and the output voltage.
- 6.12** Design of a multiple-output dc–dc flyback converter. For this problem, you may neglect all losses and transformer leakage inductances. It is desired that the three-output flyback converter shown in Fig. 6.51 operates in the discontinuous conduction mode, with a switching frequency of $f_s = 100$ kHz. The nominal operating conditions are given in the diagram, and you may assume that there are no variations in the input voltage or the load currents. Select $D_3 = 0.1$ (the duty cycle of subinterval 3, in which all semiconductors are off). The objective of this problem is to find a good steady-state design, in which the semiconductor peak blocking voltages and peak currents are reasonably low.

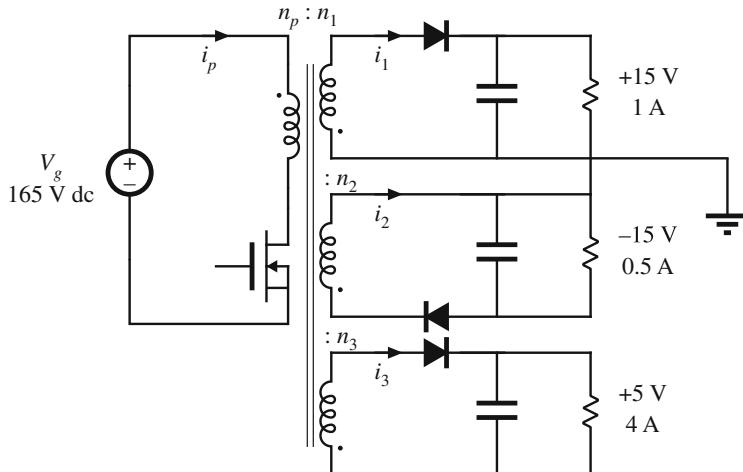


Fig. 6.51 Three-output flyback converter design, Problem 6.12

- (a) It is possible to find a design in which the transistor peak blocking voltage is less than 300 V, and the peak diode blocking voltages are all less than 35 V, under steady-state conditions. Design the converter such that this is true. Specify: (i) the transistor duty cycle D , (ii) the magnetizing inductance L_M , referred to the primary, (iii) the turns ratios n_1/n_p and n_3/n_p .
 (b) For your design of part (a), determine the rms currents of the four windings. Note that they do not simply scale by the turns ratios.

Part II

Converter Dynamics and Control



AC Equivalent Circuit Modeling

7.1 Introduction

Converter systems invariably require feedback. For example, in a typical dc–dc converter application, the output voltage $v(t)$ must be kept constant, regardless of changes in the input voltage $v_g(t)$ or in the effective load resistance R . This is accomplished by building a circuit that varies the converter control input [i.e., the duty cycle $d(t)$] in such a way that the output voltage $v(t)$ is regulated to be equal to a desired reference value v_{ref} . In inverter systems, a feedback loop causes the output voltage to follow a sinusoidal reference voltage. In modern low-harmonic rectifier systems, a control system causes the converter input current to be proportional to the input voltage, such that the input port presents a resistive load to the ac source. So feedback is commonly employed.

A typical dc–dc system incorporating a buck converter and feedback loop block diagram is illustrated in Fig. 7.1. It is desired to design this feedback system in such a way that the output voltage is accurately regulated, and is insensitive to disturbances in $v_g(t)$ or in the load current. In addition, the feedback system should be stable, and properties such as transient overshoot, settling time, and steady-state regulation should meet specifications. The ac modeling and design of converters and their control systems such as Fig. 7.1 is the subject of Part II of this book.

To design the system of Fig. 7.1, we need a dynamic model of the switching converter. How do variations in the power input voltage, the load current, or the duty cycle affect the output voltage? What are the small-signal transfer functions? To answer these questions, we will extend the steady-state models developed in Chaps. 2 and 3 to include the dynamics introduced by the inductors and capacitors of the converter. Dynamics of converters operating in the continuous conduction mode can be modeled using techniques quite similar to those of Chaps. 2 and 3; the resulting ac equivalent circuits bear a strong resemblance to the dc equivalent circuits derived in Chap. 3.

Modeling is the representation of physical phenomena by mathematical means. In engineering, it is desired to model the important dominant behavior of a system, while neglecting other insignificant phenomena. Simplified terminal equations of the component elements are used, and many aspects of the system response are neglected altogether, that is, they are “unmodeled.” The resulting simplified model yields physical insight into the system behavior, which aids the

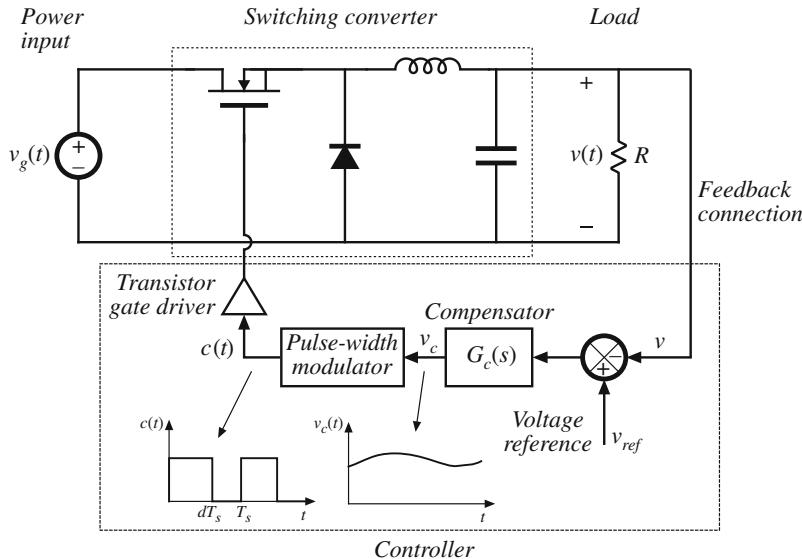


Fig. 7.1 A simple dc–dc regulator system, including a buck converter power stage and a feedback network

engineer in designing the system to operate in a given specified manner. Thus, the modeling process involves use of approximations to neglect small but complicating phenomena, in an attempt to understand what is most important. Once this basic insight is gained, it may be desirable to carefully refine the model, by accounting for some of the previously ignored phenomena. It is a fact of life that real, physical systems are complex, and their detailed analysis can easily lead to an intractable and useless mathematical mess. Approximate models are an important tool for gaining understanding and physical insight.

As discussed in Chap. 2, the switching ripple is small in a well-designed converter operating in continuous conduction mode (CCM). Hence, we should ignore the switching ripple, and model only the underlying ac variations in the converter waveforms. For example, suppose that some ac variation is introduced into the control signal $v_c(t)$, such that

$$v_c(t) = V_c + V_{cm} \cos \omega_m t \quad (7.1)$$

where V_c and V_{cm} are constants, $|V_{cm}| \ll V_c$, and the modulation frequency ω_m is much smaller than the converter switching frequency $\omega_s = 2\pi f_s$. This control signal is fed into a pulse-width modulator (PWM) that generates a gate drive signal having switching frequency $f_s = 1/T_s$ and whose duty cycle during each switching period depends on the control signal $v_c(t)$ applied during that period. The resulting transistor gate drive signal is illustrated in Fig. 7.2a, and typical buck–boost converter inductor current and output voltage waveforms $i_L(t)$ and $v(t)$ are illustrated in Fig. 7.2b. The spectrum of $v(t)$ is illustrated in Fig. 7.3. This spectrum contains components at the switching frequency as well as its harmonics and sidebands; these components are small in magnitude if the switching ripple is small. In addition, the spectrum contains a low-frequency

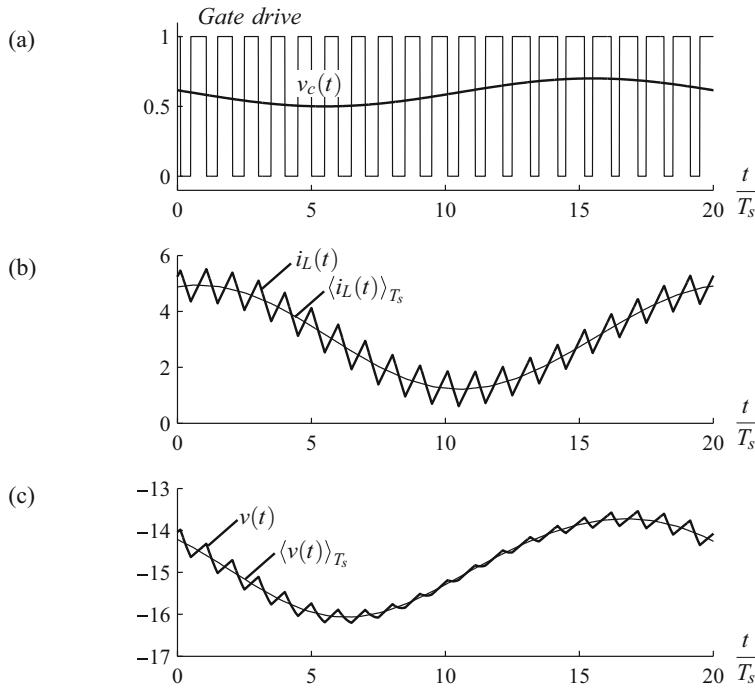


Fig. 7.2 Ac variation of the converter signals: (a) control signal $v_c(t)$ and transistor gate drive logic signal, in which the duty cycle varies slowly; (b) the resulting inductor current waveform; (c) the resulting output voltage waveform. Both the actual waveforms $i_L(t)$ and $v(t)$, as well as their averaged, low-frequency components $\langle i_L(t) \rangle_{T_s}$ and $\langle v(t) \rangle_{T_s}$ are illustrated

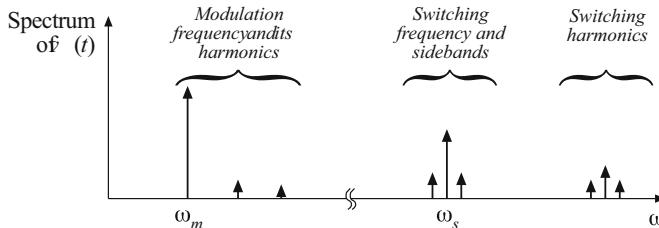


Fig. 7.3 Spectrum of the output voltage waveform $v(t)$ of Fig. 7.2

component at the modulation frequency ω_m . The magnitude and phase of this component depend not only on the control signal and duty-cycle variation, but also on the frequency response of the converter. If we neglect the switching ripple, then this low-frequency component remains [also illustrated in Fig. 7.2c]. The objective of our ac modeling efforts is to predict this low-frequency component.

A simple method for deriving the small-signal model of CCM converters is explained in Sect. 7.2. The switching ripples in the inductor current and capacitor voltage waveforms are removed by averaging over one switching period. Hence, the low-frequency components of the inductor and capacitor waveforms are modeled by equations of the form

$$\begin{aligned} L \frac{d\langle i_L(t) \rangle_{T_s}}{dt} &= \langle v_L(t) \rangle_{T_s} \\ C \frac{d\langle v_C(t) \rangle_{T_s}}{dt} &= \langle i_C(t) \rangle_{T_s} \end{aligned} \quad (7.2)$$

where $\langle x(t) \rangle_{T_s}$ denotes the average of $x(t)$ over an interval of length T_s :

$$\langle x(t) \rangle_{T_s} = \frac{1}{T_s} \int_{t-T_s/2}^{t+T_s/2} x(\tau) d\tau \quad (7.3)$$

So we will employ the basic approximation of removing the high-frequency switching ripple by averaging over one switching period. Yet the average value is allowed to vary from one switching period to the next, such that low-frequency variations are modeled. In effect, the “moving average” of Eq. (7.3) constitutes low-pass filtering of the waveform. A few of the numerous references on averaged modeling of switching converters are listed at the end of this chapter [15–17, 46, 61–76].

Note that the principles of inductor volt-second balance and capacitor charge balance predict that the right-hand sides of Eqs. (7.2) are zero when the converter operates in equilibrium. Equations (7.2) describe how the inductor currents and capacitor voltages change when nonzero average inductor voltage and capacitor current are applied over a switching period.

The averaged inductor voltage and capacitor currents of Eq. (7.2) are, in general, nonlinear functions of the signals in the converter, and hence Eqs. (7.2) constitute a set of nonlinear differential equations. Indeed, the spectrum in Fig. 7.3 also contains harmonics of the modulation frequency ω_m . In most converters, these harmonics become significant in magnitude as the modulation frequency ω_m approaches the switching frequency ω_s , or as the modulation amplitude D_m approaches the quiescent duty cycle D . Nonlinear elements are not uncommon in electrical engineering; indeed, all semiconductor devices exhibit nonlinear behavior. To obtain a linear model that is easier to analyze, we usually construct a small-signal model that has been linearized about a quiescent operating point, in which the harmonics of the modulation or excitation frequency are neglected. As an example, Fig. 7.4 illustrates linearization of the familiar diode i – v characteristic shown in Fig. 7.4b. Suppose that the diode current $i(t)$ has a quiescent (dc) value I and a signal component $\hat{i}(t)$. As a result, the voltage $v(t)$ across the diode has a quiescent value V and a signal component $\hat{v}(t)$. If the signal components are small compared to the quiescent values,

$$|\hat{v}| \ll |V|, |\hat{i}| \ll |I| \quad (7.4)$$

then the relationship between $\hat{v}(t)$ and $\hat{i}(t)$ is approximately linear, $\hat{v}(t) = r_D \hat{i}(t)$. The conductance $1/r_D$ represents the slope of the diode characteristic, evaluated at the quiescent operating point. The small-signal equivalent circuit model of Fig. 7.4c describes the diode behavior for small variations around the quiescent operating point.

An example of a nonlinear converter characteristic is the dependence of the steady-state output voltage V of the buck–boost converter on the duty cycle D , illustrated in Fig. 7.5. Suppose that the converter operates with some dc output voltage, say, $V = -V_g$, corresponding to a

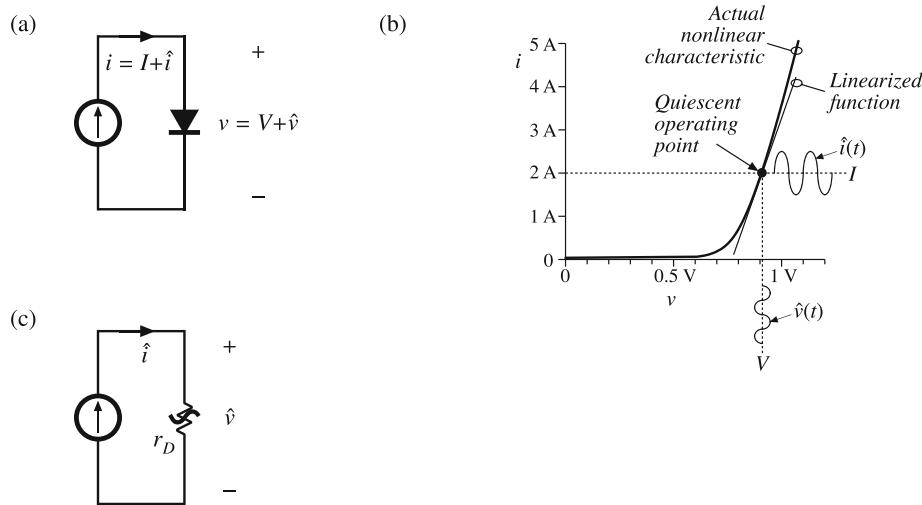
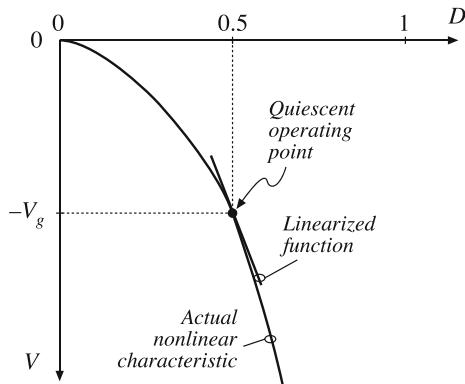


Fig. 7.4 Small-signal equivalent circuit modeling of the diode: (a) a nonlinear diode conducting current i ; (b) linearization of the diode characteristic around a quiescent operating point; (c) a linearized small-signal model



quiescent duty cycle of $D = 0.5$. Duty-cycle variations \hat{d} about this quiescent value will excite variations \hat{v} in the output voltage. If the magnitude of the duty-cycle variation is sufficiently small, then we can compute the resulting output voltage variations by linearizing the curve. The slope of the linearized characteristic in Fig. 7.5 is chosen to be equal to the slope of the actual nonlinear characteristic at the quiescent operating point; this slope is the dc control-to-output gain of the converter. The linearized and nonlinear characteristics are approximately equal in value provided that the duty-cycle variations \hat{d} are sufficiently small.

Although it illustrates the process of small-signal linearization, the buck-boost example of Fig. 7.5 is oversimplified. The inductors and capacitors of the converter cause the gain to exhibit a frequency response. To correctly predict the poles and zeroes of the small-signal transfer functions, we must linearize the converter averaged differential equations, Eqs. (7.2). This is done in Sect. 7.2. A small-signal ac equivalent circuit can then be constructed using the methods

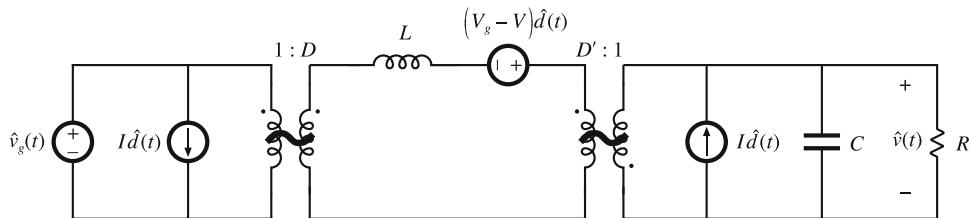


Fig. 7.6 Small-signal ac equivalent circuit model of the buck-boost converter

developed in Chap. 3. The resulting small-signal model of the buck-boost converter is illustrated in Fig. 7.6; this model can be solved using conventional circuit analysis techniques, to find the small-signal transfer functions, output impedance, and other frequency-dependent properties. In systems such as Fig. 6.51, the equivalent circuit model can be inserted in place of the converter. When small-signal models of the other system elements (such as the pulse-width modulator) are inserted, then a complete linearized system model is obtained. This model can be analyzed using standard linear techniques, such as the Laplace transform, to gain insight into the behavior and properties of the system.

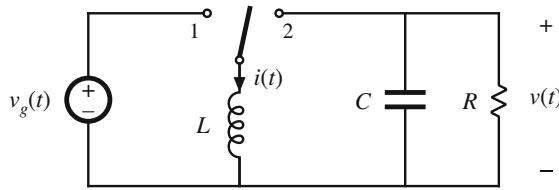
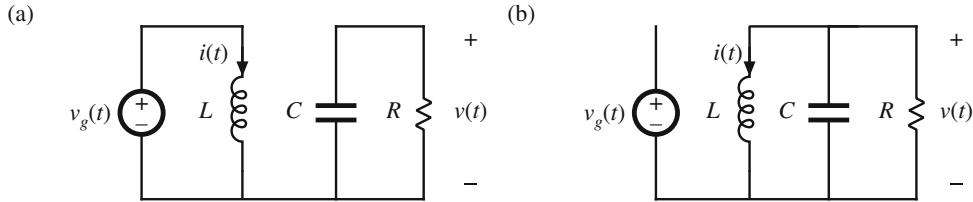
Two well-known variants of the ac modeling method, state-space averaging and circuit averaging, are explained in Sect. 7.5 and Chap. 14. An extension of circuit averaging, known as *averaged switch modeling*, is also discussed in Chap. 14. Since the switches are the only elements that introduce switching harmonics, equivalent circuit models can be derived by averaging only the switch waveforms. The converter models suitable for analysis or simulation are obtained simply by replacing the switches with the averaged switch model. The averaged switch modeling technique can be extended to other modes of operation such as the discontinuous conduction mode, as well as to current-programmed control and to resonant converters. In Sect. 7.4, it is shown that the small-signal model of any dc-dc pulse-width modulated CCM converter can be written in a standard form. Called the *canonical model*, this equivalent circuit describes the basic physical functions that any of these converters must perform. A simple model of the pulse-width modulator circuit is described in Sect. 7.3.

These models are useless if you do not know how to apply them. So in Chap. 8, the frequency response of converters is explored, in a design-oriented and detailed manner. Small-signal transfer functions of the basic converters are tabulated. Bode plots of converter transfer functions and impedances are derived in a simple, approximate manner, which allows insight to be gained into the origins of the frequency response of complex converter systems.

These results are used to design converter control systems in Chap. 9 and input filters in Chap. 17. The modeling techniques are extended in Chaps. 15 and 18 to cover the discontinuous conduction mode and the current-programmed mode.

7.2 The Basic AC Modeling Approach

In this section, the steps in derivation of the small-signal ac model of a PWM converter are derived and explained. The key steps are: (a) development of the equations relating the low-frequency averages of the inductor and capacitor waveforms, with use of a dynamic version of the small-ripple approximation, (b) perturbation and linearization of the averaged equations, and (c) construction of an ac equivalent circuit model.

**Fig. 7.7** Buck-boost converter example**Fig. 7.8** Buck-boost converter circuit: (a) when the switch is in position 1, (b) when the switch is in position 2

The buck-boost converter of Fig. 7.7 is employed as an example. The analysis begins as usual, by determination of the voltage and current waveforms of the inductor and capacitor. When the switch is in position 1, the circuit of Fig. 7.8a is obtained. The inductor voltage and capacitor current are

$$v_L(t) = L \frac{di(t)}{dt} = v_g(t) \quad (7.5)$$

$$i_C(t) = C \frac{dv(t)}{dt} = -\frac{v(t)}{R} \quad (7.6)$$

With the switch in position 2, the circuit of Fig. 7.8b is obtained. Its inductor voltage and capacitor current are

$$v_L(t) = L \frac{di(t)}{dt} = v(t) \quad (7.7)$$

$$i_C(t) = C \frac{dv(t)}{dt} = -i(t) - \frac{v(t)}{R} \quad (7.8)$$

7.2.1 Averaging the Inductor and Capacitor Waveforms

We first derive the equation that governs how the averaged components of the inductor waveforms evolve with time. We know that the instantaneous inductor current and voltage are related by the definition

$$L \frac{di(t)}{dt} = v_L(t) \quad (7.9)$$

Is there a similar relationship between the averages of the inductor voltage and current? Let us compute the derivative of the average inductor current:

$$\frac{d\langle i(t) \rangle_{T_s}}{dt} = \frac{d}{dt} \left[\frac{1}{T_s} \int_{t-T_s/2}^{t+T_s/2} i(\tau) d\tau \right] \quad (7.10)$$

On the right side of this equation, we can interchange the order of differentiation and integration because the inductor current is continuous, and because its derivative $v_L(t)/L$ has a finite number of discontinuities over the period of integration. Hence, the above equation becomes

$$\frac{d\langle i(t) \rangle_{T_s}}{dt} = \frac{1}{T_s} \int_{t-T_s/2}^{t+T_s/2} \frac{di(\tau)}{d\tau} d\tau \quad (7.11)$$

Finally, we can use Eq. (7.9) to replace $di(\tau)/d\tau$ with $v_L(\tau)$:

$$\frac{d\langle i(t) \rangle_{T_s}}{dt} = \frac{1}{T_s} \int_{t-T_s/2}^{t+T_s/2} \frac{v_L(\tau)}{L} d\tau \quad (7.12)$$

This can be rearranged to obtain

$$L \frac{d\langle i(t) \rangle_{T_s}}{dt} = \langle v_L(t) \rangle_{T_s} \quad (7.13)$$

This result shows that average components of the inductor voltage and current follow the same defining equation (7.9), with no change in L and no additional terms.

We can employ a similar analysis to find the relationship between the average components of a capacitor voltage and current, with the following result:

$$C \frac{d\langle v(t) \rangle_{T_s}}{dt} = \langle i_C(t) \rangle_{T_s} \quad (7.14)$$

We next need to evaluate the right sides of the above two equations, by averaging the inductor voltage and capacitor current waveforms.

7.2.2 The Average Inductor Voltage and the Small-Ripple Approximation

The inductor voltage and current waveforms for the buck-boost converter example are illustrated in Fig. 7.9. It is desired to compute the average inductor voltage $\langle v_L(t) \rangle_{T_s}$ at some arbitrary time t . As illustrated in Fig. 7.9, the averaging interval extends over the interval beginning at $t - T_s/2$ and ending at $t + T_s/2$. For the example time illustrated, there is an interval of length dT_s in which the inductor voltage is $v_L = v_g$, and there are two intervals of total length $d'T_s$ in which the inductor voltage is $v_L = v$.

We now make the small-ripple approximation. But rather than replacing $v_g(t)$, $v(t)$, and $i(t)$ with their dc components V_g , V and I as in Chap. 2, we now replace them with their low-frequency averaged values $\langle v_g(t) \rangle_{T_s}$, $\langle v(t) \rangle_{T_s}$, and $\langle i(t) \rangle_{T_s}$, defined by Eq. (7.3). It is important to note that it is valid to apply the small-ripple approximation only to quantities that actually have small ripple and are nonpulsating; hence, we apply this approximation to the inductor currents, capacitor voltages, and independent sources that indeed have small ripple and are continuous functions of time.

The usefulness of the small-ripple approximation here is that we ignore the changes in these quantities during one switching period or during the averaging interval $(t - T_s/2, t + T_s/2)$. As in the steady-state case, the small-ripple approximation considerably simplifies the mathematics.

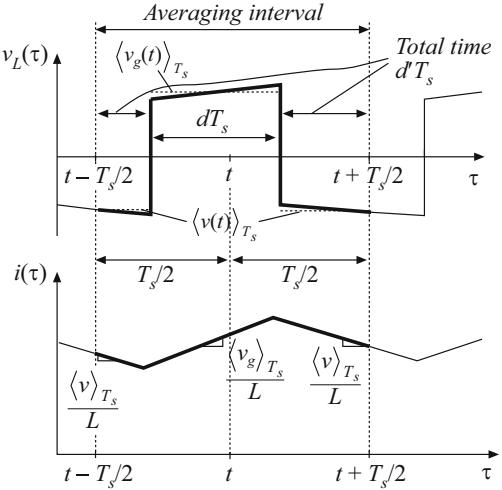


Fig. 7.9 Mechanics of evaluating the average inductor waveforms at some arbitrary time t : averaging the inductor voltage $v_L(t)$ and the inductor current $i(t)$

This approximation is valid provided that the natural frequencies of the circuit are sufficiently slower than the switching frequency, so that the ripples in the actual inductor current and capacitor voltage waveforms are indeed small.

With the small-ripple approximation, we can express the inductor voltage for the subinterval of length dT_s [Eq. (7.5)] as

$$v_L(t) = L \frac{di(t)}{dt} \approx \langle v_g(t) \rangle_{T_s} \quad (7.15)$$

In a similar manner, for the remaining subintervals of total length $d'T_s$ [Eq. (7.7)], we can express the inductor voltage as

$$v_L(t) = L \frac{di(t)}{dt} \approx \langle v(t) \rangle_{T_s} \quad (7.16)$$

The average inductor voltage is therefore

$$\langle v_L(t) \rangle_{T_s} = \frac{1}{T_s} \int_{t-T_s/2}^{t+T_s/2} v_L(\tau) d\tau \approx d(t) \langle v_g(t) \rangle_{T_s} + d'(t) \langle v(t) \rangle_{T_s} \quad (7.17)$$

Insertion of this expression into Eq. (7.13) leads to

$$L \frac{d\langle i(t) \rangle_{T_s}}{dt} = d(t) \langle v_g(t) \rangle_{T_s} + d'(t) \langle v(t) \rangle_{T_s} \quad (7.18)$$

This equation describes how the low-frequency components of the inductor current vary with time, and is the desired result.

7.2.3 Discussion of the Averaging Approximation

The averaging operator, Eq. (7.3), is repeated below:

$$\langle x(t) \rangle_{T_s} = \frac{1}{T_s} \int_{t-T_s/2}^{t+T_s/2} x(\tau) d\tau \quad (7.19)$$

Averaging is an artifice that facilitates the derivation of tractable equations describing the low-frequency dynamics of the switching converter. It removes the waveform components at the switching frequency and its harmonics, while preserving the magnitude and phase of the waveform low-frequency components. In this chapter, we replace the converter waveforms by their averages, to find models that describe the dynamic properties of switching converters operating in the continuous conduction mode. In later chapters of this text, this averaging operator is employed in other situations such as the discontinuous conduction mode or current-programmed control.

Figure 7.2 illustrates the inductor current and voltage waveforms of a buck–boost converter in which the duty cycle is varied sinusoidally. The waveform averages as computed by Eq. (7.19) are superimposed. It can be seen that the $\langle i(t) \rangle_{T_s}$ waveform indeed passes through the center of the actual $i(t)$ waveform. Additionally, an increase in $\langle v_L(t) \rangle_{T_s}$ causes an increase in the slope of $\langle i(t) \rangle_{T_s}$, as predicted by Eq. (7.13).

The averaging operator of Eq. (7.19) is a transformation that effectively performs a low-pass function to remove the switching ripple. Indeed, we can take the Laplace transformation of Eq. (7.19) to obtain:

$$\langle x(s) \rangle_{T_s} = G_{av}(s)x(s) \quad (7.20)$$

It can be shown that $G_{av}(s)$ is given by

$$G_{av}(s) = \frac{e^{sT_s/2} - e^{-sT_s/2}}{sT_s} \quad (7.21)$$

We can compute the effect of the averaging operator on a sinusoid of angular frequency ω by letting $s = j\omega$ in the above equation. The transfer function G_{av} then becomes

$$G_{av}(j\omega) = \frac{e^{j\omega T_s/2} - e^{-j\omega T_s/2}}{j\omega T_s} = \frac{\sin(\omega T_s/2)}{\omega T_s/2} \quad (7.22)$$

Figure 7.10 contains a plot of the magnitude (expressed in decibels) of Eq. 7.22 vs. frequency (for more information on frequency response plots, see Sect. 8.1). The averaging operator exhibits a low-frequency gain of 1 (or 0 dB), and a gain of zero (or $-\infty$ dB) at the switching frequency f_s and its harmonics. Equation (7.22) is purely real, and exhibits zero phase shift for frequencies less than the switching frequency. Thus, the averaging operator preserves the magnitude and phase of the low-frequency components of the waveform, while removing components at the switching frequency and its harmonics.

For frequencies f greater than approximately $f_s/3$, Fig. 7.10 exhibits substantial attenuation. This suggests that averaged models may not accurately predict transient responses at higher frequencies. The high-frequency dynamics of the discontinuous conduction mode is an example of this behavior, and is discussed further in Sect. 15.5.

Unlike the steady-state analyses of Chaps. 2 and 3, Fig. 7.9 is sketched at an arbitrary time t , with an averaging interval that does not necessarily begin when the transistor is switched on. This rigorous definition of averaging is important when modeling high-bandwidth control schemes such as the current-programmed mode of Chap. 18. The choice of averaging interval extending from $(t - T_s/2)$ to $(t + T_s/2)$ preserves the phase of the waveform, and therefore correctly predicts the behavior of current-programmed converters. It should also be noted that computing the average by integrating one half-cycle into the future [i.e., to $(t + T_s/2)$] does not violate any physical causality constraint, because this is merely a modeling artifice that is not implemented in a physical circuit.

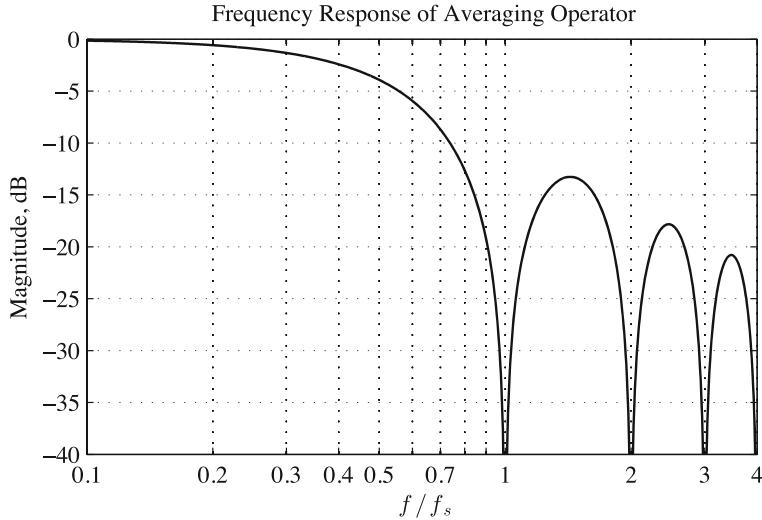


Fig. 7.10 Frequency response of the averaging operator: $\|G_{av}(j\omega)\|$ given by Eq. (7.22)

We may also note that the result of Eq. (7.18) can be derived without such rigor. For derivation of continuous-time models of the continuous conduction mode, the same result is obtained regardless of whether the averaging interval begins at $(t - T_s/2)$ or at the instant when the transistor is switched on. For the remainder of this textbook, we will continue to employ the simpler arguments begun in Chap. 2, in which the averaging interval begins when the transistor is switched on. In later chapters, the more rigorous treatment will be employed when necessary, such as when modeling the high-frequency dynamics of current-programmed control.

7.2.4 Averaging the Capacitor Waveforms

A similar procedure leads to the capacitor dynamic equation. The capacitor voltage and current waveforms are sketched in Fig. 7.11. When the switch is in position 1, the capacitor current is given by

$$i_C(t) = C \frac{dv(t)}{dt} = -\frac{v(t)}{R} \approx -\frac{\langle v(t) \rangle_{T_s}}{R} \quad (7.23)$$

With the switch in position 2, the capacitor current is

$$i_C(t) = C \frac{dv(t)}{dt} = -i(t) - \frac{v(t)}{R} \approx -\langle i(t) \rangle_{T_s} - \frac{\langle v(t) \rangle_{T_s}}{R} \quad (7.24)$$

The average capacitor current can be found by averaging Eqs. (7.23) and (7.24); the result is

$$\langle i_C(t) \rangle_{T_s} = d(t) \left(-\frac{\langle v(t) \rangle_{T_s}}{R} \right) + d'(t) \left(-\langle i(t) \rangle_{T_s} - \frac{\langle v(t) \rangle_{T_s}}{R} \right) \quad (7.25)$$

Upon inserting this equation into Eq. (7.2) and collecting terms, one obtains

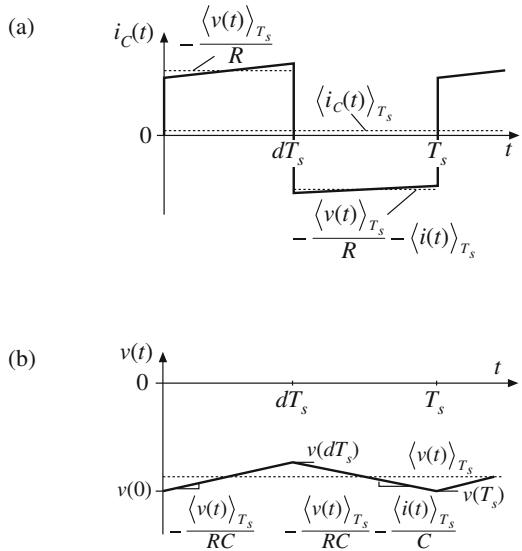


Fig. 7.11 Buck-boost converter waveforms: (a) capacitor current, (b) capacitor voltage

$$C \frac{d\langle v(t) \rangle_{T_s}}{dt} = -d'(t) \langle i(t) \rangle_{T_s} - \frac{\langle v(t) \rangle_{T_s}}{R} \quad (7.26)$$

This is the basic averaged equation which describes dc and low-frequency ac variations in the capacitor voltage.

7.2.5 The Average Input Current

In Chap. 3, it was found to be necessary to write an additional equation that models the dc component of the converter input current. This allowed the input port of the converter to be modeled by the dc equivalent circuit. A similar procedure must be followed here, so that low-frequency variations at the converter input port are modeled by the ac equivalent circuit.

For the buck-boost converter example, the current $i_g(t)$ drawn by the converter from the input source is equal to the inductor current $i(t)$ during the first subinterval, and zero during the second subinterval. By neglecting the inductor current ripple and replacing $i(t)$ with its averaged value $\langle i(t) \rangle_{T_s}$, we can express the input current as follows:

$$i_g(t) = \begin{cases} \langle i(t) \rangle_{T_s} & \text{during subinterval 1} \\ 0 & \text{during subinterval 2} \end{cases} \quad (7.27)$$

The input current waveform is illustrated in Fig. 7.12. Upon averaging over one switching period, one obtains

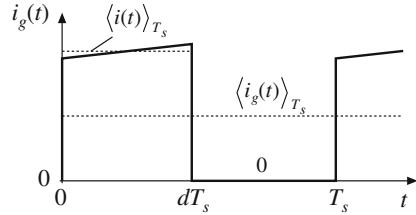


Fig. 7.12 Buck-boost converter waveforms: input source current $i_g(t)$

$$\langle i_g(t) \rangle_{T_s} = d(t) \langle i(t) \rangle_{T_s} \quad (7.28)$$

This is the basic averaged equation which describes dc and low-frequency ac variations in the converter input current.

7.2.6 Perturbation and Linearization

The buck-boost converter averaged equations, Eqs. (7.18), (7.26), and (7.28), are collected below:

$$\begin{aligned} L \frac{d\langle i(t) \rangle_{T_s}}{dt} &= d(t) \langle v_g(t) \rangle_{T_s} + d'(t) \langle v(t) \rangle_{T_s} \\ C \frac{d\langle v(t) \rangle_{T_s}}{dt} &= -d'(t) \langle i(t) \rangle_{T_s} - \frac{\langle v(t) \rangle_{T_s}}{R} \\ \langle i_g(t) \rangle_{T_s} &= d(t) \langle i(t) \rangle_{T_s} \end{aligned} \quad (7.29)$$

These equations are nonlinear because they involve the multiplication of time-varying quantities. For example, the capacitor current depends on the product of the control input $d'(t)$ and the low-frequency component of the inductor current, $\langle i(t) \rangle_{T_s}$. Multiplication of time-varying signals generates harmonics, and is a nonlinear process. Most of the techniques of ac circuit analysis, such as the Laplace transform and other frequency-domain methods, are not useful for nonlinear systems. So we need to linearize Eqs. (7.29) by constructing a small-signal model.

Suppose that we drive the converter at some steady-state, or quiescent, duty ratio $d(t) = D$, with quiescent input voltage $v_g(t) = V_g$. We know from our steady-state analysis of Chaps. 2 and 3 that, after any transients have subsided, the inductor current $\langle i(t) \rangle_{T_s}$, the capacitor voltage $\langle v(t) \rangle_{T_s}$, and the input current $\langle i_g(t) \rangle_{T_s}$ will reach the quiescent values I , V , and I_g , respectively, where

$$\begin{aligned} V &= -\frac{D}{D'} V_g \\ I &= -\frac{V}{D' R} \\ I_g &= DI \end{aligned} \quad (7.30)$$

Equations (7.30) are derived as usual via the principles of inductor volt-second and capacitor charge balance. They could also be derived from Eqs. (7.29) by noting that, in steady state, the derivatives must equal zero.

To construct a small-signal ac model at a quiescent operating point (I, V) , one assumes that the input voltage $v_g(t)$ and the duty cycle $d(t)$ are equal to some given quiescent values V_g and D , plus some superimposed small ac variations $\hat{v}_g(t)$ and $\hat{d}(t)$. Hence, we have

$$\begin{aligned} \langle v_g(t) \rangle_{T_s} &= V_g + \hat{v}_g(t) \\ d(t) &= D + \hat{d}(t) \end{aligned} \quad (7.31)$$

In response to these inputs, and after any transients have subsided, the averaged inductor current $\langle i(t) \rangle_{T_s}$, the averaged capacitor voltage $\langle v(t) \rangle_{T_s}$, and the averaged input current $\langle i_g(t) \rangle_{T_s}$ waveforms will be equal to the corresponding quiescent values I , V , and I_g , plus some superimposed small ac variations $\hat{i}(t)$, $\hat{v}(t)$, and $\hat{i}_g(t)$:

$$\begin{aligned}\langle i(t) \rangle_{T_s} &= I + \hat{i}(t) \\ \langle v(t) \rangle_{T_s} &= V + \hat{v}(t) \\ \langle i_g(t) \rangle_{T_s} &= I_g + \hat{i}_g(t)\end{aligned}\quad (7.32)$$

With the assumptions that the ac variations are small in magnitude compared to the dc quiescent values, or

$$\begin{aligned}|\hat{v}_g(t)| &\ll |V_g| \\ |\hat{d}(t)| &\ll |D| \\ |\hat{i}(t)| &\ll |I| \\ |\hat{v}(t)| &\ll |V| \\ |\hat{i}_g(t)| &\ll |I_g|\end{aligned}\quad (7.33)$$

then the nonlinear equations (7.29) can be linearized. This is done by inserting Eqs. (7.31) and (7.32) into Eq. (7.29). For the inductor equation, one obtains

$$L \frac{d(I + \hat{i}(t))}{dt} = (D + \hat{d}(t))(V_g + \hat{v}_g(t)) + (D' - \hat{d}(t))(V + \hat{v}(t)) \quad (7.34)$$

It should be noted that the complement of the duty cycle is given by

$$d'(t) = (1 - d(t)) = 1 - (D + \hat{d}(t)) = D' - \hat{d}(t) \quad (7.35)$$

where $D' = 1 - D$. The minus sign arises in the expression for $d'(t)$ because a $d(t)$ variation that causes $d(t)$ to increase will cause $d'(t)$ to decrease.

By multiplying out Eq. (7.34) and collecting terms, one obtains

$$L \left(\frac{dI}{dt} + \frac{d\hat{i}(t)}{dt} \right) = \underbrace{(DV_g + D'V)}_{\text{Dc terms}} + \underbrace{\left(D\hat{v}_g(t) + D'\hat{v}(t) + (V_g - V)\hat{d}(t) \right)}_{\substack{\text{1}^{\text{st}} \text{ order ac terms} \\ (\text{linear})}} + \underbrace{\hat{d}(t)(\hat{v}_g(t) - \hat{v}(t))}_{\substack{\text{2}^{\text{nd}} \text{ order ac terms} \\ (\text{nonlinear})}} \quad (7.36)$$

The derivative of I is zero, since I is by definition a dc (constant) term. For the purposes of deriving a small-signal ac model, the dc terms can be considered known constant quantities. On the right-hand side of Eq. (7.36), three types of terms arise:

Dc terms: These terms contain dc quantities only.

First-order ac terms: Each of these terms contains a single ac quantity, usually multiplied by a constant coefficient such as a dc term. These terms are linear functions of the ac variations.

Second-order ac terms: These terms contain the products of ac quantities. Hence they are nonlinear, because they involve the multiplication of time-varying signals.

It is desired to neglect the nonlinear ac terms. Provided that the small-signal assumption, Eq. (7.33), is satisfied, then each of the second-order nonlinear terms is much smaller in magnitude than one or more of the linear first-order ac terms. For example, the second-order ac term $\hat{d}(t)\hat{v}_g(t)$ is much smaller in magnitude than the first-order ac term $D\hat{v}_g(t)$ whenever $|\hat{d}(t)| \ll D$. So we can neglect the second-order terms. Also, by definition [or by use of Eq. (7.30)], the dc terms on the right-hand side of the equation are equal to the dc terms on the left-hand side, or zero.

We are left with the first-order ac terms on both sides of the equation. Hence,

$$L \frac{d\hat{i}(t)}{dt} = D\hat{v}_g(t) + D'\hat{v}(t) + (V_g - V)\hat{d}(t) \quad (7.37)$$

This is the desired result: the small-signal linearized equation that describes variations in the inductor current.

The capacitor equation can be linearized in a similar manner. Insertion of Eqs. (7.31) and (7.32) into the capacitor equation of Eq. (7.29) yields

$$C \frac{d(V + \hat{v}(t))}{dt} = - (D' - \hat{d}(t))(I + \hat{i}(t)) - \frac{(V + \hat{v}(t))}{R} \quad (7.38)$$

Upon multiplying out Eq. (7.38) and collecting terms, one obtains

$$C \left(\frac{dV}{dt} + \frac{d\hat{v}(t)}{dt} \right) = \underbrace{\left(-D'I - \frac{V}{R} \right)}_{\text{Dc terms}} + \underbrace{\left(-D'\hat{i}(t) - \frac{\hat{v}(t)}{R} + Id'(t) \right)}_{\substack{\text{1}^{\text{st}} \text{ order ac terms} \\ (\text{linear})}} + \underbrace{\hat{d}(t)\hat{i}(t)}_{\substack{\text{2}^{\text{nd}} \text{ order ac term} \\ (\text{nonlinear})}} \quad (7.39)$$

By neglecting the second-order terms, and noting that the dc terms on both sides of the equation are equal, we again obtain a linearized first-order equation, containing only the first-order ac terms of Eq. (7.39):

$$C \frac{d\hat{v}(t)}{dt} = -D'\hat{i}(t) - \frac{\hat{v}(t)}{R} + I\hat{d}(t) \quad (7.40)$$

This is the desired small-signal linearized equation that describes variations in the capacitor voltage.

Finally, the equation of the average input current is also linearized. Insertion of Eqs. (7.31) and (7.32) into the input current equation of Eq. (7.29) yields

$$I_g + \hat{i}_g(t) = (D + \hat{d}(t))(l + \hat{i}(t)) \quad (7.41)$$

By collecting terms, we obtain

$$\underbrace{I_g}_{\text{Dc term}} + \underbrace{\hat{i}_g(t)}_{\text{1}^{\text{st}} \text{ order ac term}} = \underbrace{(DI)}_{\text{Dc term}} + \underbrace{\left(D\hat{i}(t) + I\hat{d}(t) \right)}_{\substack{\text{1}^{\text{st}} \text{ order ac terms} \\ (\text{linear})}} + \underbrace{\hat{d}(t)\hat{i}(t)}_{\substack{\text{2}^{\text{nd}} \text{ order ac term} \\ (\text{nonlinear})}} \quad (7.42)$$

We again neglect the second-order nonlinear terms. The dc terms on both sides of the equation are equal. The remaining first-order linear ac terms are

$$\hat{i}_g(t) = D\hat{i}(t) + I\hat{d}(t) \quad (7.43)$$

This is the linearized small-signal equation that describes the low-frequency ac components of the converter input current.

In summary, the nonlinear averaged equations of a switching converter can be linearized about a quiescent operating point. The converter independent inputs are expressed as constant (dc) values, plus small ac variations. In response, the converter averaged waveforms assume similar forms. Insertion of Eqs. (7.31) and (7.32) into the converter averaged nonlinear equations yields dc terms, linear ac terms, and nonlinear terms. If the ac variations are sufficiently small in magnitude, then the nonlinear terms are much smaller than the linear ac terms, and so can be neglected. The remaining linear ac terms comprise the small-signal ac model of the converter.

7.2.7 Construction of the Small-Signal Equivalent Circuit Model

Equations (7.37), (7.40), and (7.43) are the small-signal ac description of the ideal buck-boost converter, and are collected below:

$$\begin{aligned} L \frac{d\hat{i}(t)}{dt} &= D\hat{v}_g(t) + D'\hat{v}(t) + (V_g - V)\hat{d}(t) \\ C \frac{d\hat{v}(t)}{dt} &= -D'\hat{i}(t) - \frac{\hat{v}(t)}{R} + I\hat{d}(t) \\ \hat{i}_g(t) &= D\hat{i}(t) + I\hat{d}(t) \end{aligned} \quad (7.44)$$

In Chap. 3, we collected the averaged dc equations of a converter, and reconstructed an equivalent circuit that modeled the dc properties of the converter. We can use the same procedure here, to construct averaged small-signal ac models of converters.

The inductor equation of (7.44), or Eq. (7.37), describes the voltages around a loop containing the inductor. Indeed, this equation was derived by finding the inductor voltage via loop analysis, then averaging, perturbing, and linearizing. So the equation represents the voltages around a loop of the small-signal model, which contains the inductor. The loop current is the small-signal ac inductor current $\hat{i}(t)$. As illustrated in Fig. 7.13, the term $L\hat{i}(t)/dt$ represents the voltage across the inductor L in the small-signal model. This voltage is equal to three other voltage terms. $D\hat{v}_g(t)$ and $D'\hat{v}(t)$ represent dependent sources as shown. These terms will be combined into ideal transformers. The term $(V_g - V)\hat{d}(t)$ is driven by the control input $\hat{d}(t)$, and is represented by an independent source as shown.

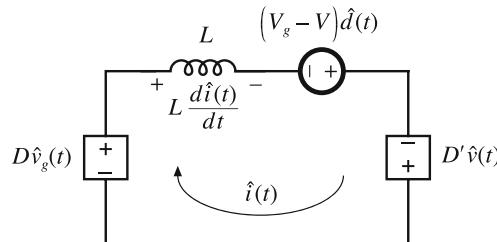


Fig. 7.13 Circuit equivalent to the small-signal ac inductor loop equation of Eq. (7.44) or (7.37)

The capacitor equation of (7.44), or Eq. (7.40), describes the currents flowing into a node attached to the capacitor. This equation was derived by finding the capacitor current via node analysis, then averaging, perturbing, and linearizing. Hence, this equation describes the currents flowing into a node of the small-signal model, attached to the capacitor. As illustrated in Fig. 7.14, the term $Cd\hat{v}(t)/dt$ represents the current flowing through capacitor C in the small-signal model. The capacitor voltage is $\hat{v}(t)$. According to the equation, this current is equal to three other terms. The term $-D'\hat{i}(t)$ represents a dependent source, which will eventually be combined into an ideal transformer. The term $-\hat{v}(t)/R$ is recognized as the current flowing through the load resistor in the small-signal model. The resistor is connected in parallel with the capacitor, such that the ac voltage across the resistor R is $\hat{v}(t)$ as expected. The term $I\hat{d}(t)$ is driven by the control input $\hat{d}(t)$, and is represented by an independent source as shown.

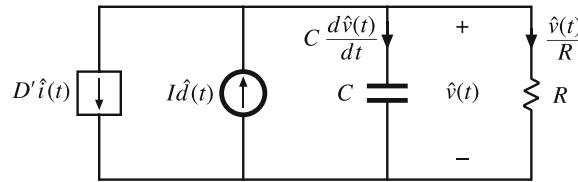


Fig. 7.14 Circuit equivalent to the small-signal ac capacitor node equation of Eq. (7.44) or (7.40)

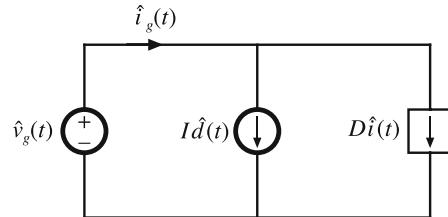


Fig. 7.15 Circuit equivalent to the small-signal ac input source current equation of Eq. (7.44) or (7.43)

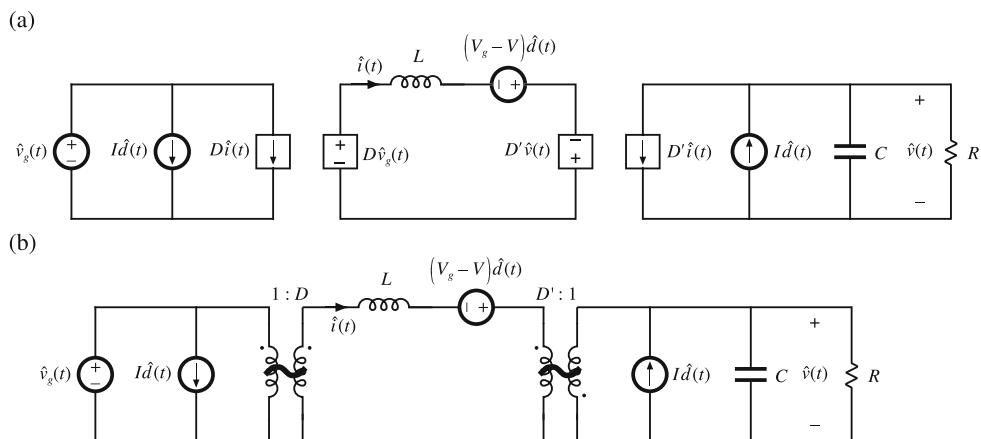


Fig. 7.16 Buck-boost converter small-signal ac equivalent circuit: (a) the circuits of Figs. 7.13, 7.14, 7.15, collected together; (b) combination of dependent sources into effective ideal transformers, leading to the final model

Finally, the input current equation of (7.44), or Eq. (7.43), describes the small-signal ac current $\hat{i}_g(t)$ drawn by the converter out of the input voltage source $\hat{v}_g(t)$. This is a node equation which states that $\hat{i}_g(t)$ is equal to the currents in two branches, as illustrated in Fig. 7.15. The first branch, corresponding to the $D\hat{i}(t)$ term, is dependent on the ac inductor current $\hat{i}(t)$. Hence, we represent this term using a dependent current source; this source will eventually be incorporated into an ideal transformer. The second branch, corresponding to the $I\hat{d}(t)$ term, is driven by the control input $d(t)$, and is represented by an independent source as shown.

The circuits of Figs. 7.13, 7.14, and 7.15 are collected in Fig. 7.16a. As discussed in Chap. 3, the dependent sources can be combined into effective ideal transformers, as illustrated in Fig. 7.16b. The sinusoid superimposed on the transformer symbol indicates that the transformer

is ideal, and is part of the averaged small-signal ac model. So the effective dc transformer property of CCM dc–dc converters also influences small-signal ac variations in the converter signals.

The equivalent circuit of Fig. 7.16b can now be solved using techniques of conventional linear circuit analysis, to find the converter transfer functions, input and output impedances, etc. This is done in detail in the next chapter. Also, the model can be refined by inclusion of losses and other nonidealities—an example is given in Sect. 7.2.10.

7.2.8 Discussion of the Perturbation and Linearization Step

In the perturbation and linearization step, it is assumed that an averaged voltage or current consists of a constant (dc) component and a small-signal ac variation around the dc component. In Sect. 7.2.6, the linearization step was completed by neglecting nonlinear terms that correspond to products of the small-signal ac variations. In general, the linearization step amounts to taking the Taylor expansion of a nonlinear relation and retaining only the constant and linear terms. For example, the large-signal averaged equation for the inductor current in Eq. (7.29) can be written as:

$$L \frac{d\langle i(t) \rangle_{T_s}}{dt} = d(t)\langle v_g(t) \rangle_{T_s} + d'(t)\langle v(t) \rangle_{T_s} = f_1(\langle v_g(t) \rangle_{T_s}, \langle v(t) \rangle_{T_s}, d(t)) \quad (7.45)$$

Let us expand this expression in a three-dimensional Taylor series, about the quiescent operating point (V_g , V , D):

$$\begin{aligned} L \left(\frac{dI}{dt} + \frac{\hat{d}i(t)}{dt} \right) &= f_1(V_g, V, D) + \hat{v}_g(t) \left. \frac{\partial f_1(v_g, V, D)}{\partial v_g} \right|_{v_g=V_g} \\ &\quad + \hat{v}(t) \left. \frac{\partial f_1(V_g, v, D)}{\partial v} \right|_{v=V} + \hat{d}(t) \left. \frac{\partial f_1(V_g, V, d)}{\partial d} \right|_{d=D} \\ &\quad + \text{higher-order nonlinear terms} \end{aligned} \quad (7.46)$$

For simplicity of notation, the angle brackets denoting average values are dropped in the above equation. The derivative of I is zero, since I is by definition a dc (constant) term. Equating the dc terms on both sides of Eq. (7.46) gives

$$0 = f_1(V_g, V, D) \quad (7.47)$$

which is the volt-second balance relationship for the inductor. The coefficients with the linear terms on the right-hand side of Eq. (7.46) are found as follows:

$$\left. \frac{\partial f_1(v_g, V, D)}{\partial v_g} \right|_{v_g=V_g} = D \quad (7.48)$$

$$\left. \frac{\partial f_1(V_g, v, D)}{\partial v} \right|_{v=V} = D' \quad (7.49)$$

$$\left. \frac{\partial f_1(V_g, V, d)}{\partial d} \right|_{d=D} = V_g - V \quad (7.50)$$

Using (7.48), (7.49), and (7.50), neglecting higher-order nonlinear terms, and equating the linear ac terms on both sides of Eq. (7.46) give

$$L \frac{d\hat{i}(t)}{dt} = D\hat{v}_g(t) + D'\hat{v}(t) + (V_g - V)\hat{d}(t) \quad (7.51)$$

which is identical to Eq. (7.37) derived in Sect. 7.2.6. In conclusion, the linearization step can always be accomplished using the Taylor expansion.

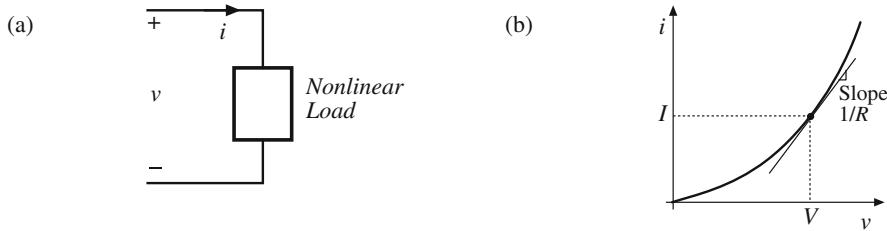


Fig. 7.17 Small-signal modeling of nonlinear load characteristic: (a) schematic, (b) linearization of i - v characteristic

A similar approach can be employed to nonlinear loads in the small-signal model. Figure 7.17 depicts linearization of a nonlinear load characteristic in which

$$i = f(v) \quad (7.52)$$

We can expand this i - v characteristic in a Taylor series about the quiescent operating point (V, I) :

$$I + \hat{i} = f(V) + \hat{v} \left. \frac{df(v)}{dv} \right|_{v=V} + \text{higher-order nonlinear terms} \quad (7.53)$$

The small-signal terms are

$$\hat{i} = \frac{\hat{v}}{R} \quad (7.54)$$

where R is determined by the slope at the quiescent operating point:

$$\frac{1}{R} = \left. \frac{df(v)}{dv} \right|_{v=V} \quad (7.55)$$

The DC solution of the converter proceeds from the nonlinear load characteristic of Eq. (7.52) with $v = V$ and $i = I$. The small-signal ac model of the converter employs the linearized equation (7.54).

7.2.9 Results for Several Basic Converters

The equivalent circuit models for the buck, boost, and buck-boost converters operating in the continuous conduction mode are summarized in Fig. 7.18. The buck and boost converter models contain ideal transformers having turns ratios equal to the converter conversion ratio. The buck-boost converter contains ideal transformers having buck and boost conversion ratios; this is consistent with the derivation of Sect. 6.1.2 of the buck-boost converter as a cascade connection of buck and boost converters. When the load is nonlinear, the incremental load resistance

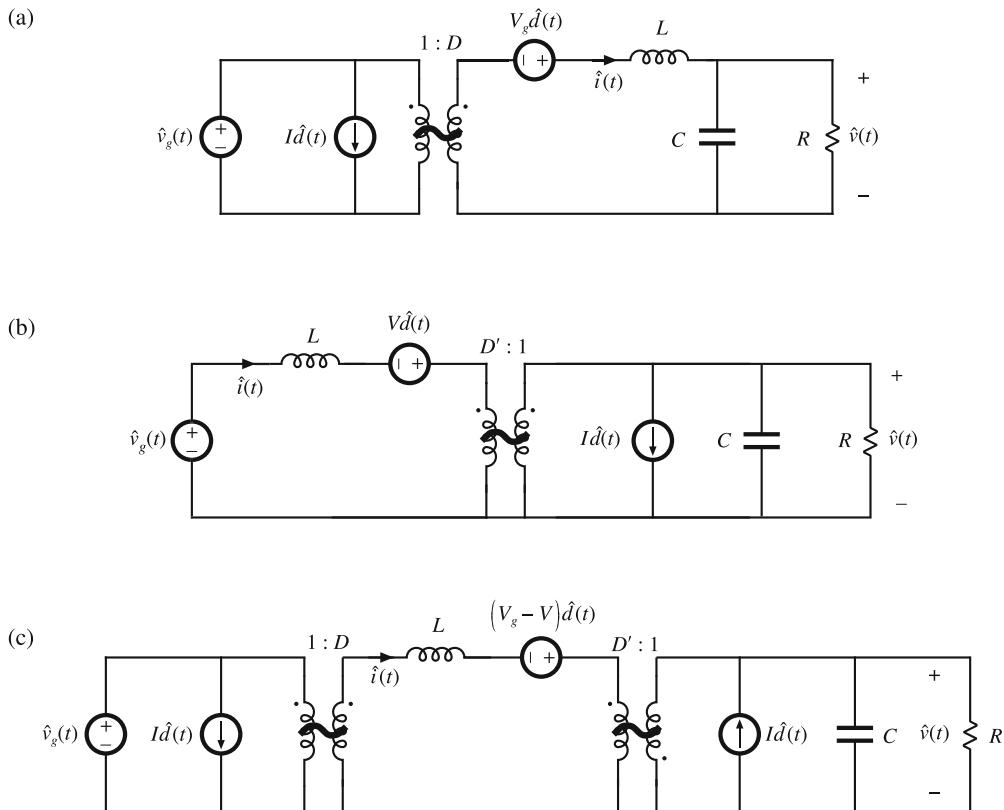


Fig. 7.18 Averaged small-signal ac models for several basic converters operating in continuous conduction mode: (a) buck, (b) boost, (c) buck-boost

of Eq. (7.55) is employed. These models can be solved to find the converter transfer functions, input and output impedances, inductor current variations, etc. By insertion of appropriate turns ratios, the equivalent circuits of Fig. 7.18 can be adapted to model the transformer-isolated versions of the buck, boost, and buck-boost converters, including the forward, flyback, and other converters.

7.2.10 Example: A Nonideal Flyback Converter

To illustrate that the techniques of the previous section are useful for modeling a variety of converter phenomena, let us next derive a small-signal ac equivalent circuit of a converter containing transformer isolation and resistive losses. An isolated flyback converter is illustrated in Fig. 7.19. The flyback transformer has magnetizing inductance L , referred to the primary winding, and turns ratio $1:n$. MOSFET Q_1 has on-resistance R_{on} . Other loss elements, as well as the transformer leakage inductances and the switching losses, are negligible. The ac modeling of this converter begins in a manner similar to the dc converter analysis of Sect. 6.3.4. The flyback transformer is replaced by an equivalent circuit consisting of the magnetizing inductance L in parallel with an ideal transformer, as illustrated in Fig. 7.20a.

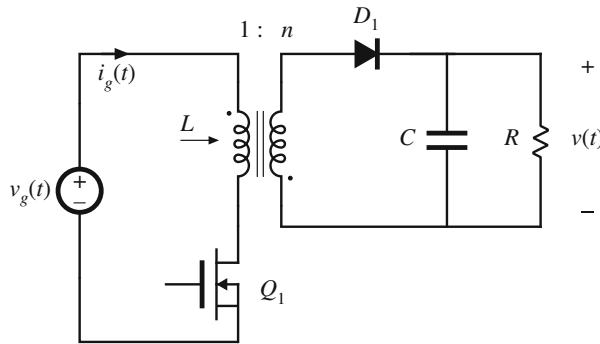


Fig. 7.19 Flyback converter example

During the first subinterval, when MOSFET Q_1 conducts, diode D_1 is off. The circuit then reduces to Fig. 7.20b. The inductor voltage $v_L(t)$, capacitor current $i_C(t)$, and converter input current $i_g(t)$ are

$$\begin{aligned} v_L(t) &= v_g(t) - i(t)R_{on} \\ i_C(t) &= -\frac{v(t)}{R} \\ i_g(t) &= i(t) \end{aligned} \quad (7.56)$$

We next make the small-ripple approximation, replacing the voltages and currents with their average values as defined by Eq. (7.3), to obtain

$$\begin{aligned} v_L(t) &= \langle v_g(t) \rangle_{T_s} - \langle i(t) \rangle_{T_s} R_{on} \\ i_C(t) &= -\frac{\langle v(t) \rangle_{T_s}}{R} \\ i_g(t) &= \langle i(t) \rangle_{T_s} \end{aligned} \quad (7.57)$$

During the second subinterval, MOSFET Q_1 is off, diode D_1 conducts, and the circuit of Fig. 7.20c is obtained. Analysis of this circuit shows that the inductor voltage, capacitor current, and input current are given by

$$\begin{aligned} v_L(t) &= -\frac{v(t)}{n} \\ i_C(t) &= \frac{i(t)}{n} - \frac{v(t)}{R} \\ i_g(t) &= 0 \end{aligned} \quad (7.58)$$

The small-ripple approximation leads to

$$\begin{aligned} v_L(t) &= \frac{\langle v(t) \rangle_{T_s}}{n} \\ i_C(t) &= \frac{-\langle i(t) \rangle_{T_s}}{n} - \frac{\langle v(t) \rangle_{T_s}}{R} \\ i_g(t) &= 0 \end{aligned} \quad (7.59)$$

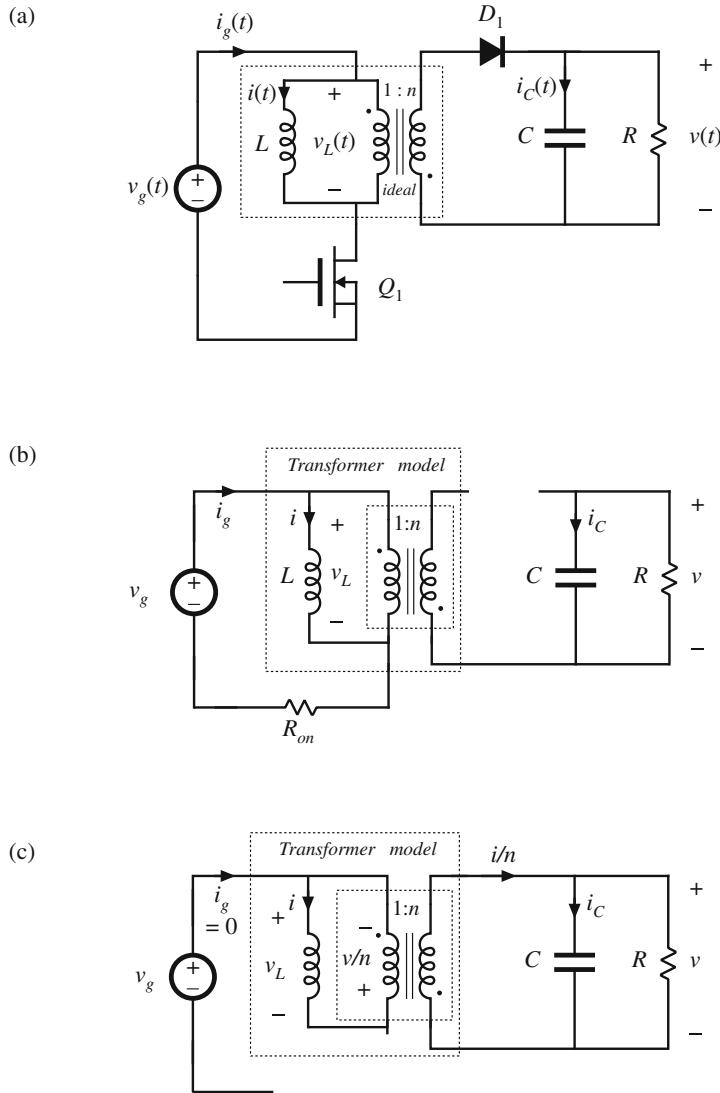


Fig. 7.20 Flyback converter example: (a) incorporation of transformer equivalent circuit, (b) circuit during subinterval 1, (c) circuit during subinterval 2

The inductor voltage and current waveforms are sketched in Fig. 7.21. The average inductor voltage can now be found by averaging the waveform of Fig. 7.21a over one switching period. The result is

$$\langle v_L(t) \rangle_{T_s} = d(t) \left(\langle v_g(t) \rangle_{T_s} - \langle i(t) \rangle_{T_s} R_{on} \right) + d'(t) \left(\frac{-\langle v(t) \rangle_{T_s}}{n} \right) \quad (7.60)$$

By inserting this result into Eq. (7.13), we obtain the averaged inductor equation,

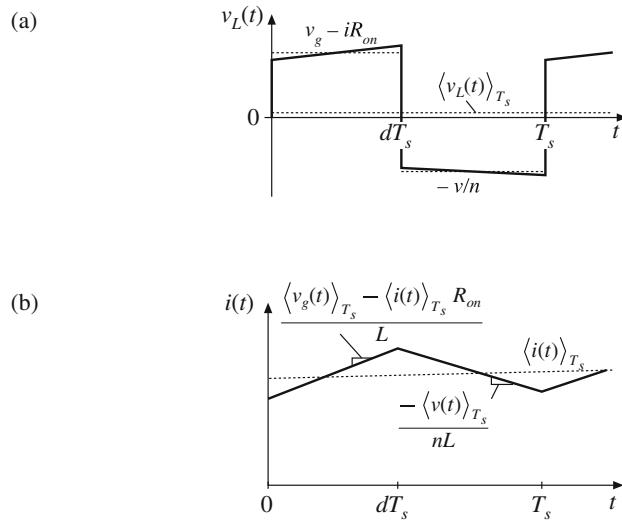


Fig. 7.21 Inductor waveforms for the flyback example: (a) inductor voltage, (b) inductor current

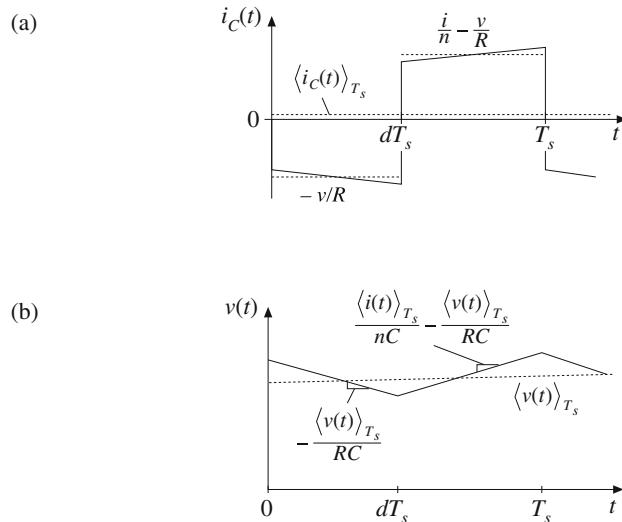


Fig. 7.22 Capacitor waveforms for the flyback example: (a) capacitor current, (b) capacitor voltage

$$L \frac{d\langle i(t) \rangle_{T_s}}{dt} = d(t) \langle v_g(t) \rangle_{T_s} - d(t) \langle i(t) \rangle_{T_s} R_{on} - d'(t) \frac{\langle v(t) \rangle_{T_s}}{n} \quad (7.61)$$

The capacitor waveforms are constructed in Fig. 7.22. The average capacitor current is

$$\langle i_C(t) \rangle_{T_s} = d(t) \left(\frac{-\langle v(t) \rangle_{T_s}}{R} \right) + d'(t) \left(\frac{\langle i(t) \rangle_{T_s}}{n} - \frac{\langle v(t) \rangle_{T_s}}{R} \right) \quad (7.62)$$

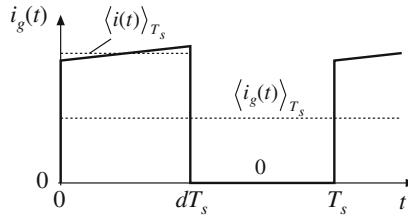


Fig. 7.23 Input source current waveform, flyback example

This leads to the averaged capacitor equation

$$C \frac{d\langle v(t) \rangle_{T_s}}{dt} = d'(t) \frac{\langle i(t) \rangle_{T_s}}{n} - \frac{\langle v(t) \rangle_{T_s}}{R} \quad (7.63)$$

The converter input current $i_g(t)$ is sketched in Fig. 7.23. Its average is

$$\langle i_g(t) \rangle_{T_s} = d(t) \langle i(t) \rangle_{T_s} \quad (7.64)$$

The averaged converter equations (7.61), (7.63), and (7.64) are collected below:

$$\begin{aligned} L \frac{d\langle i(t) \rangle_{T_s}}{dt} &= d(t) \langle v_g(t) \rangle_{T_s} - d(t) \langle i(t) \rangle_{T_s} R_{on} - d'(t) \frac{\langle v(t) \rangle_{T_s}}{n} \\ C \frac{d\langle v(t) \rangle_{T_s}}{dt} &= d'(t) \frac{\langle i(t) \rangle_{T_s}}{n} - \frac{\langle v(t) \rangle_{T_s}}{R} \\ \langle i_g(t) \rangle_{T_s} &= d(t) \langle i(t) \rangle_{T_s} \end{aligned} \quad (7.65)$$

This is a nonlinear set of differential equations, and hence the next step is to perturb and linearize, to construct the converter small-signal ac equations. We assume that the converter input voltage $v_g(t)$ and duty cycle $d(t)$ can be expressed as quiescent values plus small ac variations, as follows:

$$\begin{aligned} \langle v_g(t) \rangle_{T_s} &= V_g + \hat{v}_g(t) \\ d(t) &= D + \hat{d}(t) \end{aligned} \quad (7.66)$$

In response to these inputs, and after all transients have decayed, the average converter waveforms can also be expressed as quiescent values plus small ac variations:

$$\begin{aligned} \langle i(t) \rangle_{T_s} &= I + \hat{i}(t) \\ \langle v(t) \rangle_{T_s} &= V + \hat{v}(t) \\ \langle i_g(t) \rangle_{T_s} &= I_g + \hat{i}_g(t) \end{aligned} \quad (7.67)$$

With these substitutions, the large-signal averaged inductor equation becomes

$$L \frac{d(I + \hat{i}(t))}{dt} = (D + \hat{d}(t))(V_g + \hat{v}_g(t)) - (D' - \hat{d}(t)) \frac{(V + \hat{v}(t))}{n} - (D + \hat{d}(t))(I + \hat{i}(t))R_{on} \quad (7.68)$$

Upon multiplying this expression out and collecting terms, we obtain

$$\begin{aligned}
 L \left(\frac{dI}{dt} + \frac{\hat{d}i(t)}{dt} \right) = & \underbrace{\left(DV_g - D' \frac{V}{n} - DR_{on}I \right)}_{\text{Dc terms}} \\
 & + \underbrace{\left(D\hat{v}_g(t) - D' \frac{\hat{v}(t)}{n} + \left(V_g + \frac{V}{n} - IR_{on} \right) \hat{d}(t) - DR_{on}\hat{i}(t) \right)}_{1^{\text{st}} \text{ order ac terms (linear)}} \\
 & + \underbrace{\left(\hat{d}(t)\hat{v}_g(t) + \hat{d}(t)\frac{\hat{v}(t)}{n} - \hat{d}(t)\hat{i}(t)R_{on} \right)}_{2^{\text{nd}} \text{ order ac terms (nonlinear)}}
 \end{aligned} \tag{7.69}$$

As usual, this equation contains three types of terms. The dc terms contain no time-varying quantities. The first-order ac terms are linear functions of the ac variations in the circuit, while the second-order ac terms are functions of the products of the ac variations. If the small-signal assumptions of Eq. (7.33) are satisfied, then the second-order terms are much smaller in magnitude than the first-order terms, and hence can be neglected. The dc terms must satisfy

$$0 = DV_g - D' \frac{V}{n} - DR_{on}I \tag{7.70}$$

This result could also be derived by applying the principle of inductor volt-second balance to the steady-state inductor voltage waveform. The first-order ac terms must satisfy

$$L \frac{d\hat{i}(t)}{dt} = D\hat{v}_g(t) - D' \frac{\hat{v}(t)}{n} + \left(V_g + \frac{V}{n} - IR_{on} \right) \hat{d}(t) - DR_{on}\hat{i}(t) \tag{7.71}$$

This is the linearized equation that describes ac variations in the inductor current.

Upon substitution of Eqs. (7.66) and (7.67) into the averaged capacitor equation (7.65), one obtains

$$C \frac{d(V + \hat{v}(t))}{dt} = (D' - \hat{d}(t)) \frac{(I + \hat{i}(t))}{n} - \frac{(V + \hat{v}(t))}{R} \tag{7.72}$$

By collecting terms, we obtain

$$C \left(\frac{DV}{dt} + \frac{D\hat{v}(t)}{dt} \right) = \underbrace{\left(\frac{D'I}{n} - \frac{V}{R} \right)}_{\text{Dc terms}} + \underbrace{\left(\frac{D'\hat{i}(t)}{n} - \frac{\hat{v}(t)}{R} - \frac{I\hat{d}(t)}{n} \right)}_{1^{\text{st}} \text{ order ac terms (linear)}} - \underbrace{\frac{\hat{d}(t)\hat{i}(t)}{n}}_{2^{\text{nd}} \text{ order ac term (nonlinear)}} \tag{7.73}$$

We neglect the second-order terms. The dc terms of Eq. (7.73) must satisfy

$$0 = \left(\frac{D'I}{n} - \frac{V}{R} \right) \tag{7.74}$$

This result could also be obtained by use of the principle of capacitor charge balance on the steady-state capacitor current waveform. The first-order ac terms of Eq. (7.73) lead to the small-signal ac capacitor equation

$$C \frac{d\hat{v}(t)}{dt} = \frac{D'\hat{i}(t)}{n} - \frac{\hat{v}(t)}{R} - \frac{I\hat{d}(t)}{n} \quad (7.75)$$

Substitution of Eqs. (7.66) and (7.67) into the averaged input current equation (7.65) leads to

$$I_g + \hat{i}_g(t) = (D + \hat{d}(t))(I + \hat{i}(t)) \quad (7.76)$$

Upon collecting terms, we obtain

$$\underbrace{I_g}_{\text{Dc term}} + \underbrace{\hat{i}_g(t)}_{1^{\text{st}} \text{ order ac term}} = \underbrace{(DI)}_{\text{Dc term}} + \underbrace{(D\hat{i}(t) + I\hat{d}(t))}_{\substack{1^{\text{st}} \text{ order ac terms} \\ (\text{linear})}} + \underbrace{\hat{d}(t)\hat{i}(t)}_{2^{\text{nd}} \text{ order ac term} \\ (\text{nonlinear})} \quad (7.77)$$

The dc terms must satisfy

$$I_g = DI \quad (7.78)$$

We neglect the second-order nonlinear terms of Eq. (7.77), leaving the following linearized ac equation:

$$\hat{i}_g(t) = D\hat{i}(t) + I\hat{d}(t) \quad (7.79)$$

This result models the low-frequency ac variations in the converter input current.

The equations of the quiescent values, Eqs. (7.70), (7.74), and (7.78) are collected below:

$$\begin{aligned} 0 &= DV_g - D' \frac{V}{n} - DR_{on}I \\ 0 &= \left(\frac{D'I}{n} - \frac{V}{R} \right) \\ I_g &= DI \end{aligned} \quad (7.80)$$

For given quiescent values of the input voltage V_g and duty cycle D , this system of equations can be evaluated to find the quiescent output voltage V , inductor current I , and input current dc component I_g . The results are then inserted into the small-signal ac equations.

The small-signal ac equations, Eqs. (7.71), (7.75), and (7.79), are summarized below:

$$\begin{aligned} L \frac{d\hat{i}(t)}{dt} &= D\hat{v}_g(t) - D' \frac{\hat{v}(t)}{n} + \left(V_g + \frac{V}{n} - IR_{on} \right) \hat{d}(t) - DR_{on}\hat{i}(t) \\ C \frac{d\hat{v}(t)}{dt} &= \frac{D'\hat{i}(t)}{n} - \frac{\hat{v}(t)}{R} - \frac{I\hat{d}(t)}{n} \\ \hat{i}_g(t) &= D\hat{i}(t) + I\hat{d}(t) \end{aligned} \quad (7.81)$$

The final step is to construct an equivalent circuit that corresponds to these equations.

The inductor equation was derived by first writing loop equations, to find the applied inductor voltage during each subinterval. These equations were then averaged, perturbed, and

linearized, to obtain Eq. (7.71). So this equation describes the small-signal ac voltages around a loop containing the inductor. The loop current is the ac inductor current $\hat{i}(t)$. The quantity $L\hat{d}i(t)/dt$ is the low-frequency ac voltage across the inductor. The four terms on the right-hand side of the equation are the voltages across the four other elements in the loop. The terms $D\hat{V}_g(t)$ and $-D'\hat{v}(t)/n$ are dependent on voltages elsewhere in the converter, and hence are represented as dependent sources in Fig. 7.24. The third term is driven by the duty-cycle variations $\hat{d}(t)$ and hence is represented as an independent source. The fourth term, $-DR_{on}\hat{i}(t)$, is a voltage that is proportional to the loop current $\hat{i}(t)$. Hence this term obeys Ohm's law, with effective resistance DR_{on} as shown in the figure. So the influence of the MOSFET on-resistance on the converter small-signal transfer functions is modeled by an effective resistance of value DR_{on} .

Small-signal capacitor equation (7.75) leads to the equivalent circuit of Fig. 7.25. The equation constitutes a node equation of the equivalent circuit model. It states that the capacitor current $Cd\hat{v}(t)/dt$ is equal to three other currents. The current $D'\hat{i}(t)/n$ depends on a current elsewhere in the model, and hence is represented by a dependent current source. The term $-\hat{v}(t)/R$ is the ac component of the load current, which we model with a load resistance R connected in parallel with the capacitor. The last term is driven by the duty-cycle variations $\hat{d}(t)$, and is modeled by an independent source.

The input port equation, Eq. (7.79), also constitutes a node equation. It describes the small-signal ac current $\hat{i}_g(t)$, drawn by the converter out of the input voltage source $\hat{V}_g(t)$. There are two other terms in the equation. The term $D\hat{i}(t)$ is dependent on the inductor current ac variation $\hat{i}(t)$, and is represented with a dependent source. The term $I\hat{d}(t)$ is driven by the control variations, and is modeled by an independent source. The equivalent circuit for the input port is illustrated in Fig. 7.26.

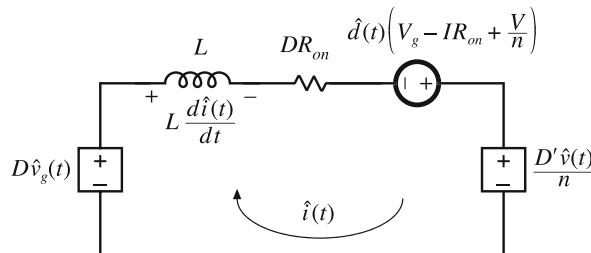


Fig. 7.24 Circuit equivalent to the small-signal ac inductor loop equation, Eq. (7.81) or (7.71)

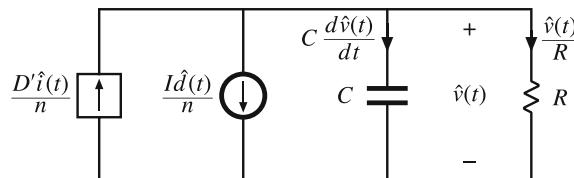


Fig. 7.25 Circuit equivalent to the small-signal ac capacitor node equation, Eq. (7.81) or (7.75)

Fig. 7.26 Circuit equivalent to the small-signal ac input source current equation, Eq. (7.81) or (7.79)

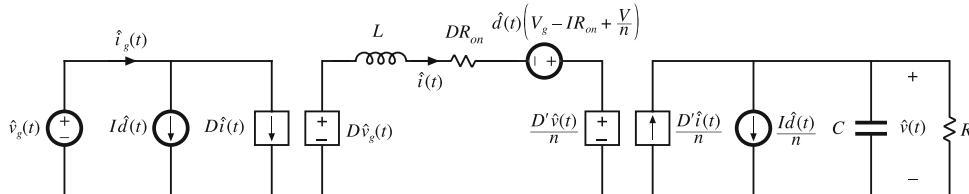
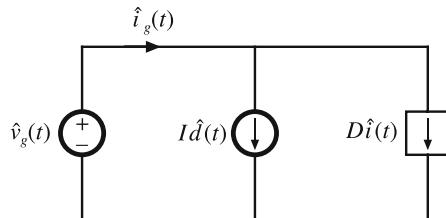


Fig. 7.27 The equivalent circuits of Figs. 7.24, 7.25, 7.26, collected together

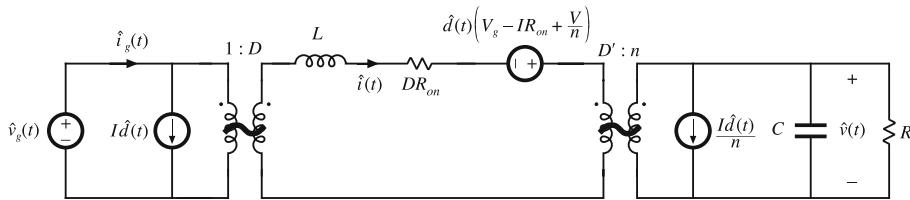


Fig. 7.28 Small-signal ac equivalent circuit model of the flyback converter

The circuits of Figs. 7.24, 7.25, and 7.26 are combined in Fig. 7.27. The dependent sources can be replaced by ideal transformers, leading to the equivalent circuit of Fig. 7.28. This is the desired result: an equivalent circuit that models the low-frequency small-signal variations in the converter waveforms. It can now be solved, using conventional linear circuit analysis techniques, to find the converter transfer functions, output impedance, and other ac quantities of interest.

7.3 Modeling the Pulse-Width Modulator

We have now achieved the goal, stated at the beginning of this chapter, of deriving a useful equivalent circuit model for the switching converter in Fig. 6.51. One detail remains: modeling the pulse-width modulator. The pulse-width modulator block shown in Fig. 6.51 produces a logic signal $\delta(t)$ that commands the converter power transistor to switch on and off. The logic signal $\delta(t)$ is periodic, with frequency f_s and duty cycle $d(t)$. The input to the pulse-width modulator is an analog control signal $v_c(t)$. The function of the pulse-width modulator is to produce a duty cycle $d(t)$ that is proportional to the analog control voltage $v_c(t)$.

A schematic diagram of a simple pulse-width modulator circuit is given in Fig. 7.29. A sawtooth-wave generator produces the voltage waveform $v_{saw}(t)$ illustrated in Fig. 7.30. The peak-to-peak amplitude of this waveform is V_M . The converter switching frequency f_s is de-

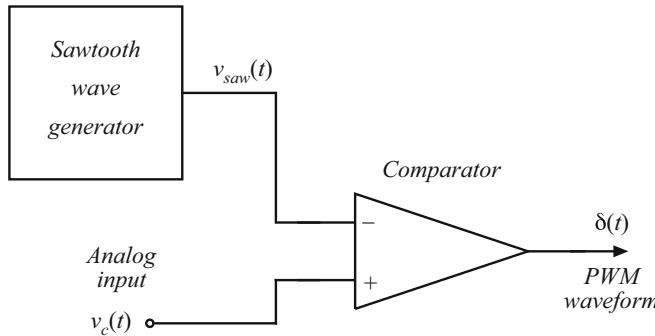


Fig. 7.29 A simple pulse-width modulator circuit

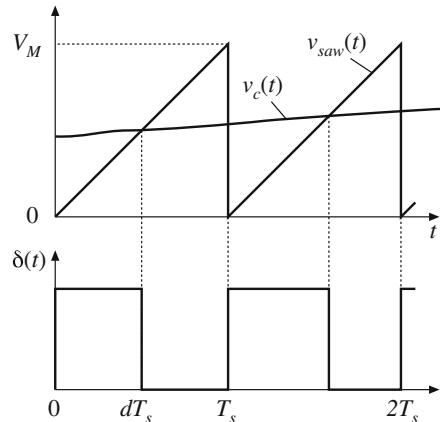


Fig. 7.30 Waveforms of the circuit of Fig. 7.29

terminated by and equal to the frequency of $v_{saw}(t)$. An analog comparator compares the analog control voltage $v_c(t)$ to $v_{saw}(t)$. This comparator produces a logic-level output which is high whenever $v_c(t)$ is greater than $v_{saw}(t)$, and is otherwise low. Typical waveforms are illustrated in Fig. 7.30.

If the sawtooth waveform $v_{saw}(t)$ has minimum value zero, then the duty cycle will be zero whenever $v_c(t)$ is less than or equal to zero. The duty cycle will be $D = 1$ whenever $v_c(t)$ is greater than or equal to V_M . If, over a given switching period, $v_{saw}(t)$ varies linearly with t , then for $0 \leq v_c(t) \leq V_M$ the duty cycle d will be a linear function of v_c . Hence, we can write

$$d(t) = \frac{v_c(t)}{V_M} \quad \text{for } 0 \leq v_c(t) \leq V_M \quad (7.82)$$

This equation is the input-output characteristic of the pulse-width modulator [15, 68].

To be consistent with the perturbed-and-linearized converter models of the previous sections, we can perturb Eq. (7.82). Let

$$\begin{aligned} v_c(t) &= V_c + \hat{v}_c(t) \\ d(t) &= D + \hat{d}(t) \end{aligned} \quad (7.83)$$

Fig. 7.31 Pulse-width modulator block diagram

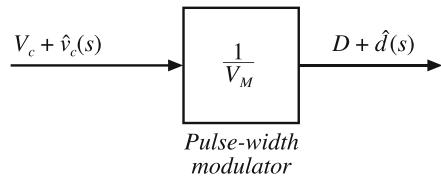
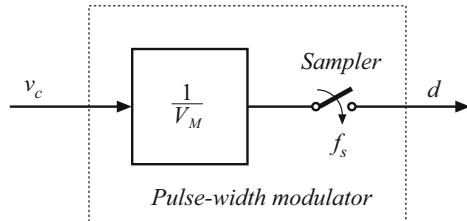


Fig. 7.32 A more accurate pulse-width modulator model, including sampling



Insertion of Eq. (7.83) into Eq. (7.82) leads to

$$D + \hat{d}(t) = \frac{V_c + \hat{v}_c(t)}{V_M} \quad (7.84)$$

A block diagram representing Eq. (7.84) is illustrated in Fig. 7.31. The pulse-width modulator has linear gain $1/V_M$. By equating like terms on both sides of Eq. (7.84), one obtains

$$\begin{aligned} D &= \frac{V_c}{V_M} \\ \hat{d}(t) &= \frac{\hat{v}_c(t)}{V_M} \end{aligned} \quad (7.85)$$

So the quiescent value of the duty cycle is determined in practice by V_c .

The pulse-width modulator model of Fig. 7.31 is sufficiently accurate for nearly all applications. However, it should be pointed out that pulse-width modulators also introduce sampling of the waveform. Although the analog input signal $v_c(t)$ is a continuous function of time, there can be only one discrete value of the duty cycle during every switching period. Therefore, the pulse-width modulator samples the waveform, with sampling rate equal to the switching frequency f_s . Hence, a more accurate modulator block diagram is as in Fig. 7.32 [10]. In the small-signal sense, sampling in the pulse-width modulator occurs at the modulated edge of the PWM signal. For example, in a trailing-edge PWM exemplified by the waveforms shown in Fig. 7.30, the sampling instants coincide with falling edges of the PWM output signal $\delta(t)$. This has important implications in developments of sampled-data dynamic models where the converter response to duty-cycle perturbations is modeled as an *equivalent hold* [77]. The sampled-data nature of pulse-width modulated converters is taken into account in the developments of high-frequency models of DCM converters in Sect. 15.5, and current-programmed converters in Sect. 18.7. Furthermore, PWM sampling effects are important in identification of delays in the control loop around a converter when the controller is implemented digitally, as discussed in Chap. 19.

In practice, PWM sampling restricts the useful frequencies of the ac variations to values much less than the switching frequency. The designer must ensure that the bandwidth of the control system be sufficiently less than the Nyquist rate $f_s/2$. Significant high-frequency variations in the control signal $v_c(t)$ can also alter the behavior of the pulse-width modulator. A

common example is when $v_c(t)$ contains switching ripple, introduced by the feedback loop. This phenomenon has been analyzed by several authors [67, 75], and effects of inductor current ripple on the transfer functions of current-programmed converters are investigated in Chap. 18. But it is generally best to avoid the case where $v_c(t)$ contains significant components at the switching frequency or higher, since the pulse-width modulators of such systems exhibit poor noise immunity.

7.4 The Canonical Circuit Model

Having discussed several methods for deriving the ac equivalent circuit models of switching converters, let us now pause to interpret the results. All PWM CCM dc–dc converters perform similar basic functions. First, they transform the voltage and current levels, ideally with 100% efficiency. Second, they contain low-pass filtering of the waveforms. While necessary to remove the high-frequency switching ripple, this filtering also influences low-frequency voltage and current variations. Third, the converter waveforms can be controlled by variation of the duty cycle.

We expect that converters having similar physical properties should have qualitatively similar equivalent circuit models. Hence, we can define a *canonical circuit model* that correctly accounts for all of these basic properties [15, 17, 61]. The ac equivalent circuit of any CCM PWM dc–dc converter can be manipulated into this canonical form. This allows us to extract physical insight, and to compare the ac properties of converters. The canonical model is used in several later chapters, where it is desired to analyze converter phenomena in a general manner, without reference to a specific converter. So the canonical model allows us to define and discuss the physical ac properties of converters.

In this section, the canonical circuit model is developed, based on physical arguments. An example is given which illustrates how to manipulate a converter equivalent circuit into canonical form. Finally, the parameters of the canonical model are tabulated for several basic ideal converters.

7.4.1 Development of the Canonical Circuit Model

The physical elements of the canonical circuit model are collected, one at a time, in Fig. 7.33. The converter contains a power input port $v_g(t)$ and a control input port $d(t)$, as well as a power output port and load having voltage $v(t)$. As discussed in Chap. 3, the basic function of any CCM PWM dc–dc converter is the conversion of dc voltage and current levels, ideally with 100% efficiency. As illustrated in Fig. 7.33a, we have modeled this property with an ideal dc transformer, having effective turns ratio $1:M(D)$ where M is the conversion ratio. This conversion ratio is a function of the quiescent duty cycle D . As discussed in Chap. 3, this model can be refined, if desired, by addition of resistors and other elements that model the converter losses.

Slow variations $v_g(t)$ in the power input induce ac variations $v(t)$ in the converter output voltage. As illustrated in Fig. 7.33b, we expect these variations also to be transformed by the conversion ratio $M(D)$.

The converter must also contain reactive elements that filter the switching harmonics and transfer energy between the power input and power output ports. Since it is desired that the output switching ripple be small, the reactive elements should comprise a low-pass filter having

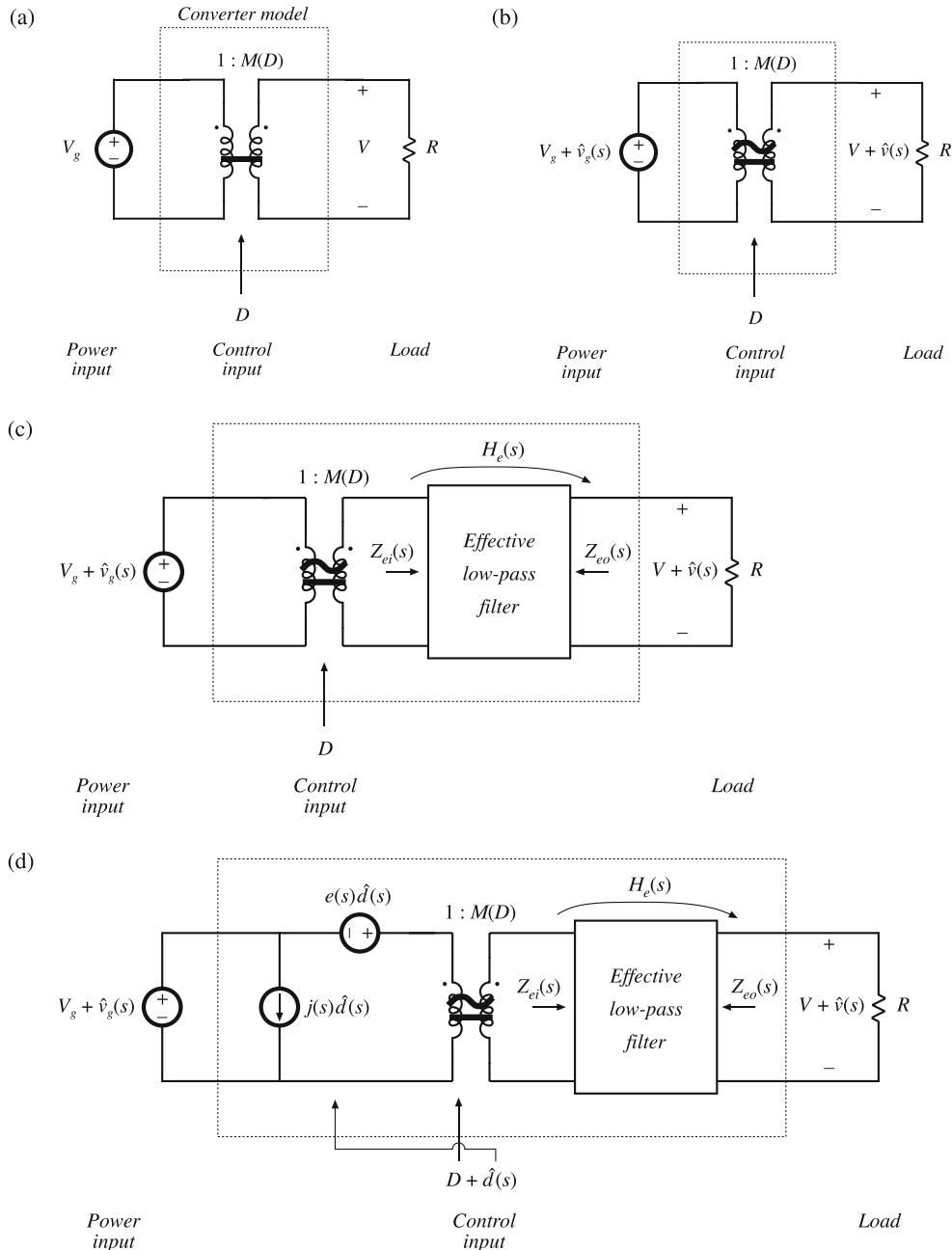


Fig. 7.33 Development of the canonical circuit model, based on physical arguments: (a) dc transformer model, (b) inclusion of ac variations, (c) reactive elements introduce effective low-pass filter, (d) inclusion of ac duty-cycle variations

a cutoff frequency well below the switching frequency. This low-pass characteristic also affects how ac line voltage variations influence the output voltage. So the model should contain an effective low-pass filter as illustrated in Fig. 7.33c. This figure predicts that the line-to-output transfer function is

$$G_{vg}(s) = \frac{\hat{v}(s)}{\hat{v}_g(s)} = M(D)H_e(s) \quad (7.86)$$

where $H_e(s)$ is the transfer function of the effective low-pass filter loaded by resistance R . When the load is nonlinear, R is the incremental load resistance, evaluated at the quiescent operating point. The effective filter also influences other properties of the converter, such as the small-signal input and output impedances. It should be noted that the elemental values in the effective low-pass filter do not necessarily coincide with the physical element values in the converter. In general, the element values, transfer function, and terminal impedances of the effective low-pass filter can vary with quiescent operating point. Examples are given in the following subsections.

Control input variations, specifically, duty-cycle variations $\hat{d}(t)$, also induce ac variations in the converter voltages and currents. Hence, the model should contain voltage and current sources driven by $\hat{d}(t)$. In the examples of the previous section, we have seen that both voltage sources and current sources appear, which are distributed around the circuit model. It is possible to manipulate the model such that all of the $\hat{d}(t)$ sources are pushed to the input side of the equivalent circuit. In the process, the sources may become frequency-dependent; an example is given in the next subsection. In general, the sources can be combined into a single voltage source $e(s)\hat{d}(s)$ and a single current source $j(s)\hat{d}(s)$ as shown in Fig. 7.33d. This model predicts that the small-signal control-to-output transfer function is

$$G_{vd}(s) = \frac{\hat{v}(s)}{\hat{d}(s)} = e(s)M(D)H_e(s) \quad (7.87)$$

This transfer function is found by setting the $\hat{v}_g(s)$ variations to zero, and solving for the dependence of $\hat{v}(s)$ on $\hat{d}(s)$. Figure 7.33d is the complete canonical circuit, which can model any PWM CCM dc–dc converter.

Often, we are also interested in the variations in output voltage \hat{v} induced by variations in load current \hat{i}_{load} . We can model this by addition of an independent current source at the converter output, as illustrated in Fig. 7.34. In this figure, the load is modeled as an effective resistor R , in parallel with an independent ac current source \hat{i}_{load} . In the ac model, the resistance R is the incremental resistance of the load, measured at the quiescent operating point, while \hat{i}_{load} is the ac variation in the load current. This model predicts that the transfer function from load current variations to output voltage variation is given by

$$Z_{out}(s) = -\frac{\hat{v}(s)}{\hat{i}_{load}(s)} = Z_{eo}(s)||R \quad (7.88)$$

To derive Eq. (7.88), we set the independent sources \hat{v}_g and \hat{d} to zero, and solve for the transfer function from \hat{i}_{load} to \hat{v} . This transfer function (with a minus sign) is the converter output impedance $Z_{out}(s)$. As defined above, the output impedance includes the incremental load resistance R . In some circumstances, it may be appropriate to exclude the load impedance from the definition of Z_{out} , or to further include additional load impedances.

Thus, the canonical model can be solved for the converter key ac transfer functions. Of common interest are the control-to-output transfer function $G_{vd}(s)$, the line-to-output transfer function $G_{vg}(s)$, and the output impedance $Z_{out}(s)$.

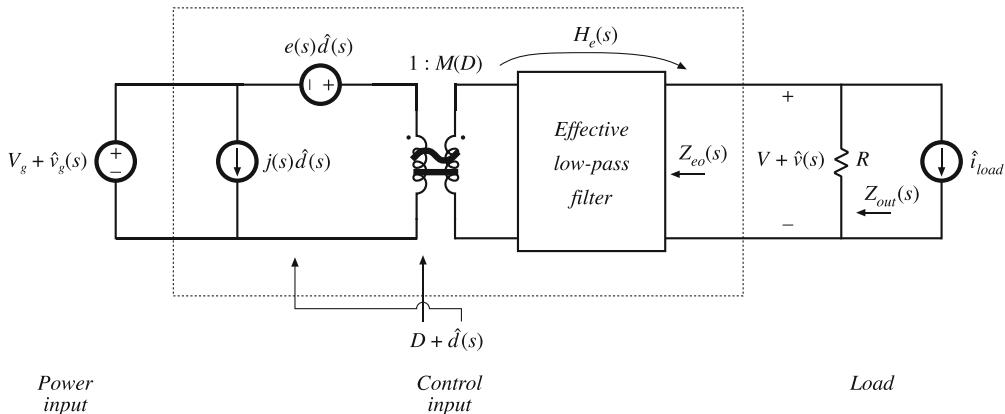


Fig. 7.34 Modeling the effect of load current variations by addition of independent current source \hat{i}_{load}

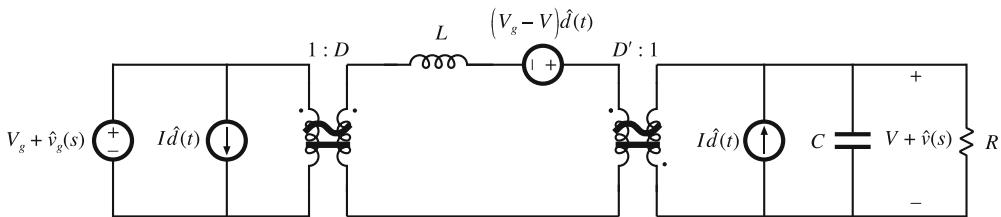


Fig. 7.35 Small-signal ac model of the buck-boost converter, before manipulation into canonical form

7.4.2 Example: Manipulation of the Buck-Boost Converter Model into Canonical Form

To illustrate the steps in the derivation of the canonical circuit model, let us manipulate the equivalent circuit of the buck-boost converter into canonical form. A small-signal ac equivalent circuit for the buck-boost converter is derived in Sect. 7.2. The result, Fig. 7.16b, is reproduced in Fig. 7.35. To manipulate this network into canonical form, it is necessary to push all of the independent $d(t)$ generators to the left, while pushing the inductor to the right and combining the transformers.

The $(V_g - V)\hat{d}(t)$ voltage source is in series with the inductor, and hence the positions of these two elements can be interchanged. In Fig. 7.36a, the voltage source is placed on the primary side of the $1:D$ ideal transformer; this requires dividing by the effective turns ratio D . The output-side $I\hat{d}(t)$ current source has also been moved to the primary side of the $D':1$ transformer. This requires multiplying by the turns ratio $1/D'$. The polarity is also reversed, in accordance with the polarities of the $D':1$ transformer windings.

Next, we need to move the $I\hat{d}(t)/D$ current source to the left of the inductor. This can be done using the artifice illustrated in Fig. 7.36b. The ground connection of the current source is broken, and the source is connected to node A instead. A second, identical, current source is connected from node A to ground. The second source causes the current flowing into node A to be unchanged, such that the node equations of Fig. 7.36a,b are identical.

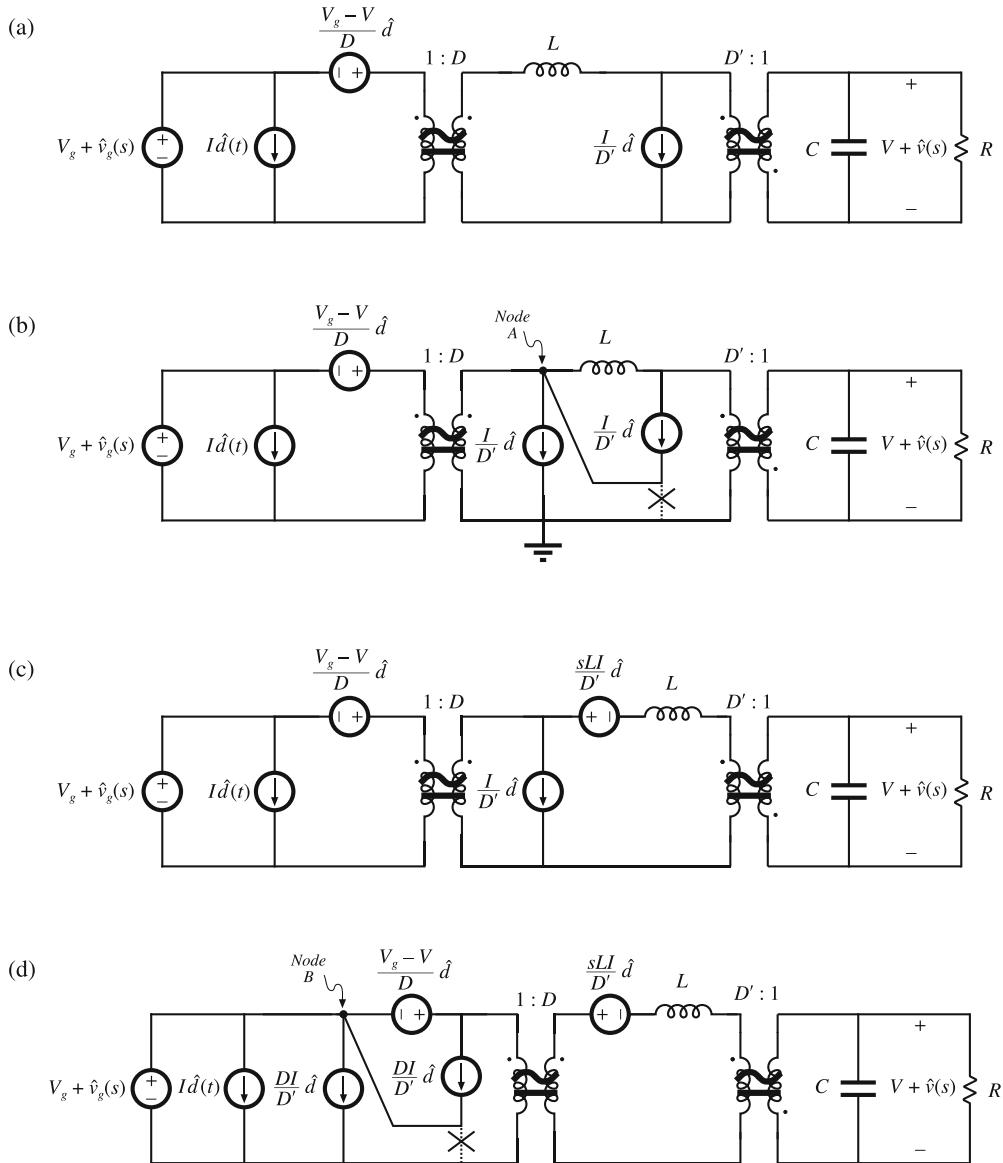


Fig. 7.36 Steps in the manipulation of the buck-boost ac model into canonical form

In Fig. 7.36c, the parallel combination of the inductor and current source is converted into Thevenin-equivalent form. The series combination of an inductor and voltage source is obtained.

In Fig. 7.36d, the $I\hat{d}(t)/D$ current source is pushed to the primary side of the $1:D$ transformer. The magnitude of the current source is multiplied by the turns ratio D . In addition, the current source is pushed through the $(V_g - V)\hat{d}(t)/D$ voltage source, using the previously described

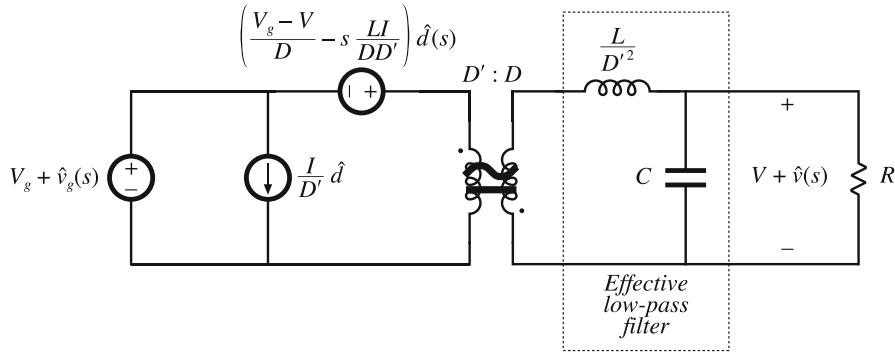


Fig. 7.37 The buck-boost converter model, in canonical form

artifice. The ground connection of the source is moved to node B , and an identical source is connected from node B to ground such that the circuit node equations are unchanged.

Figure 7.37 is the final form of the model. The inductor is moved to the secondary side of the $D':1$ transformer, by multiplying by the square of the turns ratio as shown. The $sLI\hat{d}(t)/D'$ voltage source is moved to the primary side of the $1:D$ transformer, by dividing by the turns ratio D . The voltage and current sources are combined as shown, and the two transformers are combined into a single $D':D$ transformer. The circuit is now in canonical form.

It can be seen that the inductance of the effective low-pass filter is not simply equal to the physical inductor value L , but rather is equal to L/D'^2 . At different quiescent operating points, with different values of D' , the value of the effective inductance will change. In consequence, the transfer function, input impedance, and output impedance of the effective low-pass filter will also vary with quiescent operating point. The reason for this variation is the transformation of the inductance value by the effective $D':1$ transformer.

It can also be seen from Fig. 7.37 that the coefficient of the $\hat{d}(t)$ voltage generator is

$$e(s) = \frac{V_g - V}{D} - s \frac{LI}{DD'} \quad (7.89)$$

This expression can be simplified by substitution of the dc relationships (7.30). The result is

$$e(s) = -\frac{V}{D^2} \left(1 - s \frac{DL}{D'^2 R} \right) \quad (7.90)$$

When we pushed the output-side $I\hat{d}(t)$ current source through the inductor, we obtained a voltage source having a frequency dependence. In consequence, the $e(s)\hat{d}$ voltage generator is frequency-dependent.

7.4.3 Canonical Circuit Parameter Values for Some Common Converters

For ideal CCM PWM dc–dc converters containing a single inductor and capacitor, the effective low-pass filter of the canonical model should contain a single inductor and a single capacitor. The canonical model then reduces to the circuit of Fig. 7.38. It is assumed that the capacitor is

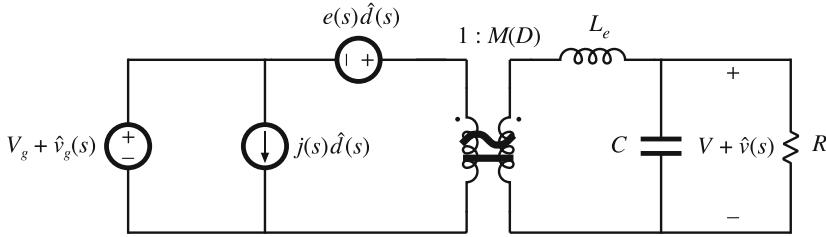


Fig. 7.38 The canonical model, for ideal CCM converters containing a single inductor and capacitor

connected directly across the load. The parameter values for the basic buck, boost, and buck-boost converters are collected in Table 7.1. Again, it should be pointed out that the effective inductance L_e depends not only on the physical inductor value L , but also on the quiescent duty cycle D . Furthermore, the current flowing in the effective inductance L_e does not in general coincide with the physical inductor current $I + \hat{i}(t)$.

Table 7.1 Canonical model parameters for the ideal buck, boost and buck-boost converters

Converter	$M(D)$	L_e	$e(s)$	$j(s)$
Buck	D	L	$\frac{V}{D^2}$	$\frac{V}{R}$
Boost	$\frac{1}{D'}$	$\frac{L}{D'^2}$	$V\left(1 - \frac{sL}{D'^2R}\right)$	$\frac{V}{D'^2R}$
Buck-boost	$-\frac{D}{D'}$	$\frac{L}{D'^2}$	$-\frac{V}{D'^2}\left(1 - \frac{sDL}{D'^2R}\right)$	$-\frac{V}{D'^2R}$

The model of Fig. 7.38 can be solved using conventional linear circuit analysis, to find quantities of interest such as the converter transfer functions, input impedance, and output impedance. Transformer-isolated versions of the buck, boost, and buck-boost converters, such as the full-bridge, forward, and flyback converters, can also be modeled using the equivalent circuit of Fig. 7.38 and the parameters of Table 7.1, provided that one correctly accounts for the transformer turns ratio.

7.5 State-Space Averaging

A number of ac converter modeling techniques have appeared in the literature, including the current-injected approach, circuit averaging, and the state-space averaging method. Although the proponents of a given method may prefer to express the end result in a specific form, the end results of nearly all methods are equivalent. And everybody will agree that averaging and small-signal linearization are the key steps in modeling PWM converters.

The state-space averaging approach [15, 61] is described in this section. The state-space description of dynamical systems is a mainstay of modern control theory; the state-space av-

eraging method makes use of this description to derive the small-signal averaged equations of PWM switching converters. The state-space averaging method is otherwise identical to the procedure derived in Sect. 7.2. Indeed, the procedure of Sect. 7.2 amounts to state-space averaging, but without the formality of writing the equations in matrix form. A benefit of the state-space averaging procedure is the generality of its result: a small-signal averaged model can always be obtained, provided that the state equations of the original converter can be written.

Section 7.5.1 summarizes how to write the state equations of a network. The basic results of state-space averaging are described in Sect. 7.5.2, and a short derivation is given in Sect. 7.5.3. Section 7.5.4 contains an example, in which the state-space averaging method is used to derive the quiescent dc and small-signal ac equations of a buck–boost converter.

7.5.1 The State Equations of a Network

The state-space description is a canonical form for writing the differential equations that describe a system. For a linear network, the derivatives of the *state variables* are expressed as linear combinations of the system independent inputs and the state variables themselves. The physical state variables of a system are usually associated with the storage of energy, and for a typical converter circuit, the physical state variables are the independent inductor currents and capacitor voltages. Other typical state variables include the position and velocity of a motor shaft. At a given point in time, the values of the state variables depend on the previous history of the system, rather than on the present values of the system inputs. To solve the differential equations of the system, the initial values of the state variables must be specified. So if we know the *state* of a system, that is, the values of all of the state variables, at a given time t_0 , and if we additionally know the system inputs, then we can in principle solve the system state equations to find the system waveforms at any future time.

The state equations of a system can be written in the compact matrix form of Eq. (7.91):

$$\begin{aligned} \mathbf{K} \frac{d\mathbf{x}(t)}{dt} &= \mathbf{Ax}(t) + \mathbf{Bu}(t) \\ \mathbf{y}(t) &= \mathbf{Cx}(t) + \mathbf{Eu}(t) \end{aligned} \quad (7.91)$$

Here, the state vector $\mathbf{x}(t)$ is a vector containing all of the state variables, that is, the inductor currents, capacitor voltages, etc. The input vector $\mathbf{u}(t)$ contains the independent inputs to the system, such as the input voltage source $v_g(t)$. The derivative of the state vector is a vector whose elements are equal to the derivatives of the corresponding elements of the state vector:

$$x(t) = \begin{bmatrix} x_1(t) \\ x_2(t) \\ \vdots \end{bmatrix}, \quad \frac{d\mathbf{x}(t)}{dt} = \begin{bmatrix} \frac{dx_1(t)}{dt} \\ \frac{dx_2(t)}{dt} \\ \vdots \end{bmatrix} \quad (7.92)$$

In the standard form of Eq. (7.91), \mathbf{K} is a matrix containing the values of capacitance, inductance, and mutual inductance (if any), such that $\mathbf{K}d\mathbf{x}(t)/dt$ is a vector containing the inductor winding voltages and capacitor currents. In other physical systems, \mathbf{K} may contain other quantities such as moment of inertia or mass. Equation (7.91) states that the inductor voltages and capacitor currents of the system can be expressed as linear combinations of the state variables and the independent inputs. The matrices \mathbf{A} and \mathbf{B} contain constants of proportionality.

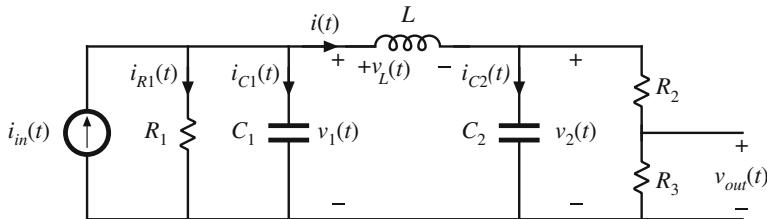


Fig. 7.39 Circuit example

It may also be desired to compute other circuit waveforms that do not coincide with the elements of the state vector $\mathbf{x}(t)$ or the input vector $\mathbf{u}(t)$. These other signals are, in general, dependent waveforms that can be expressed as linear combinations of the elements of the state vector and input vector. The vector $\mathbf{y}(t)$ is usually called the *output vector*. We are free to place any dependent signal in this vector, regardless of whether the signal is actually a physical output. The converter input current $i_g(t)$ is often chosen to be an element of $\mathbf{y}(t)$. In the state equations (7.91), the elements of $\mathbf{y}(t)$ are expressed as a linear combination of the elements of the $\mathbf{x}(t)$ and $\mathbf{u}(t)$ vectors. The matrices \mathbf{C} and \mathbf{E} contain constants of proportionality.

As an example, let us write the state equations of the circuit of Fig. 7.39. This circuit contains two capacitors and an inductor, and hence the physical state variables are the independent capacitor voltages $v_1(t)$ and $v_2(t)$, as well as the inductor current $i(t)$. So we can define the state vector as

$$\mathbf{x}(t) = \begin{bmatrix} v_1(t) \\ v_2(t) \\ i(t) \end{bmatrix} \quad (7.93)$$

Since there are no coupled inductors, the matrix \mathbf{K} is diagonal, and simply contains the values of capacitance and inductance:

$$\mathbf{K} = \begin{bmatrix} C_1 & 0 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & L \end{bmatrix} \quad (7.94)$$

The circuit has one independent input, the current source $i_{in}(t)$. Hence we should define the input vector as

$$\mathbf{u}(t) = [i_{in}(t)] \quad (7.95)$$

We are free to place any dependent signal in vector $\mathbf{y}(t)$. Suppose that we are interested in also computing the voltage $v_{out}(t)$ and the current $i_{R1}(t)$. We can therefore define $\mathbf{y}(t)$ as

$$\mathbf{y}(t) = \begin{bmatrix} v_{out}(t) \\ i_{R1}(t) \end{bmatrix} \quad (7.96)$$

To write the state equations in the canonical form of Eq. (7.91), we need to express the inductor voltages and capacitor currents as linear combinations of the elements of $\mathbf{x}(t)$ and $\mathbf{u}(t)$, that is, as linear combinations of $v_1(t)$, $v_2(t)$, $i(t)$, and $i_{in}(t)$.

The capacitor current $i_{C1}(t)$ is given by the node equation

$$i_{C1}(t) = C_1 \frac{dv_1(t)}{dt} = i_{in}(t) - \frac{v_1(t)}{R_1} - i(t) \quad (7.97)$$

This equation will become the top row of the matrix equation (7.91). The capacitor current $i_{C2}(t)$ is given by the node equation,

$$i_{C2}(t) = C_2 \frac{dv_2(t)}{dt} = i(t) - \frac{v_2(t)}{R_2 + R_3} \quad (7.98)$$

Note that we have been careful to express this current as a linear combination of the elements of $\mathbf{x}(t)$ and $\mathbf{u}(t)$ alone. The inductor voltage is given by the loop equation,

$$v_L(t) = L \frac{di(t)}{dt} = v_1(t) - v_2(t) \quad (7.99)$$

Equations (7.97) to (7.99) can be written in the following matrix form:

$$\underbrace{\begin{bmatrix} C_1 & 0 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & L \end{bmatrix}}_{\mathbf{K}} \begin{bmatrix} \frac{dv_1(t)}{dt} \\ \frac{dv_2(t)}{dt} \\ \frac{di(t)}{dt} \end{bmatrix} = \underbrace{\begin{bmatrix} -\frac{1}{R_1} & 0 & -1 \\ 0 & -\frac{1}{R_2 + R_3} & 1 \\ 1 & -1 & 0 \end{bmatrix}}_{\mathbf{A}} \begin{bmatrix} v_1(t) \\ v_2(t) \\ i(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{i}_{in}(t)} \quad (7.100)$$

$$\mathbf{K} \quad \frac{d\mathbf{x}(t)}{dt} = \mathbf{A} \quad \mathbf{x}(t) + \mathbf{B} \quad \mathbf{u}(t)$$

Matrices \mathbf{A} and \mathbf{B} are now known.

It is also necessary to express the elements of $\mathbf{y}(t)$ as linear combinations of the elements of $\mathbf{x}(t)$ and $\mathbf{u}(t)$. By solution of the circuit of Fig. 7.39, $v_{out}(t)$ can be written in terms of $v_2(t)$ as

$$v_{out}(t) = v_2(t) \frac{R_3}{R_2 + R_3} \quad (7.101)$$

Also, $i_{R1}(t)$ can be expressed in terms of $v_1(t)$ as

$$i_{R1}(t) = \frac{v_1(t)}{R_1} \quad (7.102)$$

By collecting Eqs. (7.101) and (7.102) into the standard matrix form of Eq. (7.91), we obtain

$$\underbrace{\begin{bmatrix} v_{out}(t) \\ i_{R1}(t) \end{bmatrix}}_{\mathbf{y}(t)} = \underbrace{\begin{bmatrix} 0 & \frac{R_3}{R_2 + R_3} & 0 \\ \frac{1}{R_1} & 0 & 0 \end{bmatrix}}_{\mathbf{C}} \begin{bmatrix} v_1(t) \\ v_2(t) \\ i(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 \\ 0 \end{bmatrix}}_{\mathbf{i}_{in}(t)} \quad (7.103)$$

$$\mathbf{y}(t) = \mathbf{C} \quad \mathbf{x}(t) + \mathbf{E} \quad \mathbf{u}(t)$$

We can now identify the matrices \mathbf{C} and \mathbf{E} as shown above.

It should be recognized that, starting in Chap. 2, we have always begun the analysis of converters by writing their state equations. We are now simply writing these equations in matrix form.

7.5.2 The Basic State-Space Averaged Model

Consider now that we are given a PWM converter, operating in the continuous conduction mode. The converter circuit contains independent states that form the state vector $\mathbf{x}(t)$, and the converter is driven by independent sources that form the input vector $\mathbf{u}(t)$. During the first subinterval, when the switches are in position 1, the converter reduces to a linear circuit that can be described by the following state equations:

$$\begin{aligned} \mathbf{K} \frac{d\mathbf{x}(t)}{dt} &= \mathbf{A}_1 \mathbf{x}(t) + \mathbf{B}_1 \mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}_1 \mathbf{x}(t) + \mathbf{E}_1 \mathbf{u}(t) \end{aligned} \quad (7.104)$$

During the second subinterval, with the switches in position 2, the converter reduces to another linear circuit whose state equations are

$$\begin{aligned} \mathbf{K} \frac{d\mathbf{x}(t)}{dt} &= \mathbf{A}_2 \mathbf{x}(t) + \mathbf{B}_2 \mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}_2 \mathbf{x}(t) + \mathbf{E}_2 \mathbf{u}(t) \end{aligned} \quad (7.105)$$

During the two subintervals, the circuit elements are connected differently; therefore, the respective state equation matrices \mathbf{A}_1 , \mathbf{B}_1 , \mathbf{C}_1 , \mathbf{E}_1 and \mathbf{A}_2 , \mathbf{B}_2 , \mathbf{C}_2 , \mathbf{E}_2 may also differ. Given these state equations, the result of state-space averaging is the state equations of the equilibrium and small-signal ac models.

Provided that the natural frequencies of the converter, as well as the frequencies of variations of the converter inputs, are much slower than the switching frequency, then the state-space averaged model that describes the converter in equilibrium is

$$\begin{aligned} \mathbf{0} &= \mathbf{AX} + \mathbf{BU} \\ \mathbf{Y} &= \mathbf{CX} + \mathbf{EU} \end{aligned} \quad (7.106)$$

where the averaged matrices are

$$\begin{aligned} \mathbf{A} &= D\mathbf{A}_1 + D'\mathbf{A}_2 \\ \mathbf{B} &= D\mathbf{B}_1 + D'\mathbf{B}_2 \\ \mathbf{C} &= D\mathbf{C}_1 + D'\mathbf{C}_2 \\ \mathbf{E} &= D\mathbf{E}_1 + D'\mathbf{E}_2 \end{aligned} \quad (7.107)$$

The equilibrium dc components are

$$\begin{aligned} \mathbf{X} &= \text{equilibrium (dc) state vector} \\ \mathbf{U} &= \text{equilibrium (dc) input vector} \\ \mathbf{Y} &= \text{equilibrium (dc) output vector} \\ D &= \text{equilibrium (dc) duty cycle} \end{aligned} \quad (7.108)$$

Quantities defined in Eq. (7.108) represent the equilibrium values of the averaged vectors. Equation (7.106) can be solved to find the equilibrium state and output vectors:

$$\begin{aligned} \mathbf{X} &= -\mathbf{A}^{-1}\mathbf{BU} \\ \mathbf{Y} &= (-\mathbf{CA}^{-1}\mathbf{B} + \mathbf{E})\mathbf{U} \end{aligned} \quad (7.109)$$

The state equations of the small-signal ac model are

$$\begin{aligned}\mathbf{K} \frac{d\hat{\mathbf{x}}(t)}{dt} &= \mathbf{A}\hat{\mathbf{x}}(t) + \mathbf{B}\hat{\mathbf{u}}(t) + \{(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}\} \hat{d}(t) \\ \hat{\mathbf{y}}(t) &= \mathbf{C}\hat{\mathbf{x}}(t) + \mathbf{E}\hat{\mathbf{u}}(t) + \{(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X} + (\mathbf{E}_1 - \mathbf{E}_2)\mathbf{U}\} \hat{d}(t)\end{aligned}\quad (7.110)$$

The quantities $\hat{\mathbf{x}}(t)$, $\hat{\mathbf{u}}(t)$, $\hat{\mathbf{y}}(t)$, and $\hat{d}(t)$ in Eq. (7.110) are small ac variations about the equilibrium solution, or quiescent operating point, defined by Eqs. (7.106) to (7.109).

So if we can write the converter state equations, Eqs. (7.104) and (7.105), then we can always find the averaged dc and small-signal ac models, by evaluation of Eqs. (7.106) to (7.110).

7.5.3 Discussion of the State-Space Averaging Result

As in Sects. 7.1 and 7.2, the low-frequency components of the inductor currents and capacitor voltages are modeled by averaging over an interval of length T_s . Hence, we can define the average of the state vector $\mathbf{x}(t)$ as

$$\langle \mathbf{x}(t) \rangle_{T_s} = \frac{1}{T_s} \int_{t-T_s/2}^{t+T_s/2} \mathbf{x}(\tau) d\tau \quad (7.111)$$

The low-frequency components of the input and output vectors are modeled in a similar manner. By averaging the inductor voltages and capacitor currents, one then obtains the following low-frequency state equation:

$$\mathbf{K} \frac{d\langle \mathbf{x}(t) \rangle_{T_s}}{dt} = (d(t)\mathbf{A}_1 + d'(t)\mathbf{A}_2) \langle \mathbf{x}(t) \rangle_{T_s} + (d(t)\mathbf{B}_1 + d'(t)\mathbf{B}_2) \langle \mathbf{u}(t) \rangle_{T_s} \quad (7.112)$$

This result is equivalent to Eq. (7.2).

For example, let us consider how the elements of the state vector $\mathbf{x}(t)$ change over one switching period. During the first subinterval, with the switches in position 1, the converter state equations are given by Eq. (7.104). Therefore, the elements of $\mathbf{x}(t)$ change with the slopes $\mathbf{K}^{-1}(\mathbf{A}_1\mathbf{x}(t) + \mathbf{B}_1\mathbf{u}(t))$. If we make the small ripple approximation, that $\mathbf{x}(t)$ and $\mathbf{u}(t)$ do not change much over one switching period, then the slopes are essentially constant and are approximately equal to

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{K}^{-1} (\mathbf{A}_1 \langle \mathbf{x}(t) \rangle_{T_s} + \mathbf{B}_1 \langle \mathbf{u}(t) \rangle_{T_s}) \quad (7.113)$$

This assumption coincides with the requirements for small switching ripple in all elements of $\mathbf{x}(t)$ and that variations in $\mathbf{u}(t)$ be slow compared to the switching frequency. If we assume that the state vector is initially equal to $\mathbf{x}(0)$, then we can write

$$\underbrace{\mathbf{x}(dT_s)}_{\text{final value}} = \underbrace{\mathbf{x}(0)}_{\text{initial value}} + \underbrace{(dT_s)}_{\text{interval length}} \underbrace{\mathbf{K}^{-1} (\mathbf{A}_1 \langle \mathbf{x}(t) \rangle_{T_s} + \mathbf{B}_1 \langle \mathbf{u}(t) \rangle_{T_s})}_{\text{slope}} \quad (7.114)$$

Similar arguments apply during the second subinterval. With the switch in position 2, the state equations are given by Eq. (7.105). With the assumption of small ripple during this subinterval, the state vector now changes with slope

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{K}^{-1} (\mathbf{A}_2 \langle \mathbf{x}(t) \rangle_{T_s} + \mathbf{B}_2 \langle \mathbf{u}(t) \rangle_{T_s}) \quad (7.115)$$

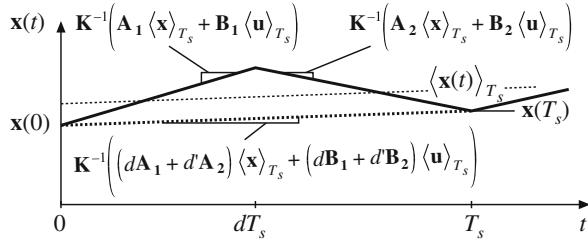


Fig. 7.40 How an element of the state vector, and its average, evolve over one switching period

The state vector at the end of the switching period is

$$\underbrace{\mathbf{x}(T_s)}_{\text{final value}} = \underbrace{\mathbf{x}(dT_s)}_{\text{initial value}} + \underbrace{(dT_s)}_{\text{interval length}} \underbrace{\mathbf{K}^{-1} (\mathbf{A}_2 \langle \mathbf{x}(t) \rangle_{T_s} + \mathbf{B}_2 \langle \mathbf{u}(t) \rangle_{T_s})}_{\text{slope}} \quad (7.116)$$

Substitution of Eq. (7.114) into Eq. (7.116) allows us to determine $\mathbf{x}(T_s)$ in terms of $\mathbf{x}(0)$:

$$\mathbf{x}(T_s) = \mathbf{x}(0) + dT_s \mathbf{K}^{-1} (\mathbf{A}_1 \langle \mathbf{x}(t) \rangle_{T_s} + \mathbf{B}_1 \langle \mathbf{u}(t) \rangle_{T_s}) + d'T_s \mathbf{K}^{-1} (\mathbf{A}_2 \langle \mathbf{x}(t) \rangle_{T_s} + \mathbf{B}_2 \langle \mathbf{u}(t) \rangle_{T_s}) \quad (7.117)$$

Upon collecting terms, one obtains

$$\mathbf{x}(T_s) = \mathbf{x}(0) + T_s \mathbf{K}^{-1} (d(t)\mathbf{A}_1 + d'(t)\mathbf{A}_2) \langle \mathbf{x}(t) \rangle_{T_s} + T_s \mathbf{K}^{-1} (d(t)\mathbf{B}_1 + d'(t)\mathbf{B}_2) \langle \mathbf{u}(t) \rangle_{T_s} \quad (7.118)$$

Next, we approximate the derivative of $\langle \mathbf{x}(t) \rangle_{T_s}$ using the net change over one switching period:

$$\frac{d\langle \mathbf{x}(t) \rangle_{T_s}}{dt} \approx \frac{\mathbf{x}(T_s) - \mathbf{x}(0)}{T_s} \quad (7.119)$$

Substitution of Eq. (7.118) into (7.119) leads to

$$\mathbf{K} \frac{d\langle \mathbf{x}(t) \rangle_{T_s}}{dt} = (d(t)\mathbf{A}_1 + d'(t)\mathbf{A}_2) \langle \mathbf{x}(t) \rangle_{T_s} + (d(t)\mathbf{B}_1 + d'(t)\mathbf{B}_2) \langle \mathbf{u}(t) \rangle_{T_s} \quad (7.120)$$

which is identical to Eq. (7.113). This is the basic averaged model which describes the converter dynamics. It is nonlinear because the control input $d(t)$ is multiplied by $\langle \mathbf{x}(t) \rangle_{T_s}$ and $\langle \mathbf{u}(t) \rangle_{T_s}$. Variation of a typical element of $\mathbf{x}(t)$ and its average are illustrated in Fig. 7.40.

It is also desired to find the low-frequency components of the output vector $\mathbf{y}(t)$ by averaging. The vector $\mathbf{y}(t)$ is described by Eq. (7.104) for the first subinterval, and by Eq. (7.105) for the second subinterval. Hence, the elements of $\mathbf{y}(t)$ may be discontinuous at the switching transitions, as illustrated in Fig. 7.41. We can again remove the switching harmonics by averaging over one switching period; the result is

$$\langle \mathbf{y}(t) \rangle_{T_s} = d(t) (\mathbf{C}_1 \langle \mathbf{x}(t) \rangle_{T_s} + \mathbf{E}_1 \langle \mathbf{u}(t) \rangle_{T_s}) + d'(t) (\mathbf{C}_2 \langle \mathbf{x}(t) \rangle_{T_s} + \mathbf{E}_2 \langle \mathbf{u}(t) \rangle_{T_s}) \quad (7.121)$$

Rearrangement of terms yields

$$\langle \mathbf{y}(t) \rangle_{T_s} = (d(t)\mathbf{C}_1 + d'(t)\mathbf{C}_2) \langle \mathbf{x}(t) \rangle_{T_s} + (d(t)\mathbf{E}_1 + d'(t)\mathbf{E}_2) \langle \mathbf{u}(t) \rangle_{T_s} \quad (7.122)$$

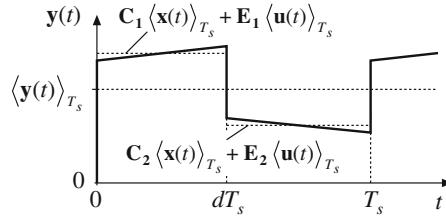


Fig. 7.41 Averaging an element of the output vector $\mathbf{y}(t)$

This is again a nonlinear equation.

The averaged state equations, (7.120) and (7.122), are collected below:

$$\begin{aligned}\mathbf{K} \frac{d\langle \mathbf{x}(t) \rangle_{T_s}}{dt} &= (d(t)\mathbf{A}_1 + d'(t)\mathbf{A}_2)\langle \mathbf{x}(t) \rangle_{T_s} + (d(t)\mathbf{B}_1 + d'(t)\mathbf{B}_2)\langle \mathbf{u}(t) \rangle_{T_s} \\ \langle \mathbf{y}(t) \rangle_{T_s} &= (d(t)\mathbf{C}_1 + d'(t)\mathbf{C}_2)\langle \mathbf{x}(t) \rangle_{T_s} + (d(t)\mathbf{E}_1 + d'(t)\mathbf{E}_2)\langle \mathbf{u}(t) \rangle_{T_s}\end{aligned}\quad (7.123)$$

The next step is the linearization of these equations about a quiescent operating point, to construct a small-signal ac model. When dc inputs $d(t) = D$ and $\mathbf{u}(t) = \mathbf{U}$ are applied, converter operates in equilibrium when the derivatives of all of the elements of $\langle \mathbf{x}(t) \rangle_{T_s}$ are zero. Hence, by setting the derivative of $\langle \mathbf{x}(t) \rangle_{T_s}$ to zero in Eq. (7.123), we can define the converter quiescent operating point as the solution of

$$\begin{aligned}\mathbf{0} &= \mathbf{AX} + \mathbf{BU} \\ \mathbf{Y} &= \mathbf{CX} + \mathbf{EU}\end{aligned}\quad (7.124)$$

where definitions (7.107) and (7.108) have been used. We now perturb and linearize the converter waveforms about this quiescent operating point:

$$\begin{aligned}\langle \mathbf{x}(t) \rangle_{T_s} &= \mathbf{X} + \hat{\mathbf{x}}(t) \\ \langle \mathbf{u}(t) \rangle_{T_s} &= \mathbf{U} + \hat{\mathbf{u}}(t) \\ \langle \mathbf{y}(t) \rangle_{T_s} &= \mathbf{Y} + \hat{\mathbf{y}}(t) \\ d(t) &= D + \hat{d}(t) \Rightarrow d'(t) = D' - \hat{d}'(t)\end{aligned}\quad (7.125)$$

Here, $\hat{\mathbf{u}}(t)$ and $\hat{d}(t)$ are small ac variations in the input vector and duty ratio. The vectors $\hat{\mathbf{x}}(t)$ and $\hat{\mathbf{y}}(t)$ are the resulting small ac variations in the state and output vectors. We must assume that these ac variations are much smaller than the quiescent values. In other words,

$$\begin{aligned}\|\mathbf{U}\| &\gg \|\hat{\mathbf{u}}(t)\| \\ D &\gg |\hat{d}(t)| \\ \|\mathbf{X}\| &\gg \|\hat{\mathbf{x}}(t)\| \\ \|\mathbf{Y}\| &\gg \|\hat{\mathbf{y}}(t)\|\end{aligned}\quad (7.126)$$

Here, $\|\mathbf{x}\|$ denotes a norm of the vector \mathbf{x} .

Substitution of Eq. (7.125) into Eq. (7.123) yields

$$\begin{aligned}\mathbf{K} \frac{d(\mathbf{X} + \hat{\mathbf{x}}(t))}{dt} &= \left((D + \hat{d}(t))\mathbf{A}_1 + (D' - \hat{d}(t))\mathbf{A}_2 \right) (\mathbf{X} + \hat{\mathbf{x}}(t)) \\ &\quad + \left((D + \hat{d}(t))\mathbf{B}_1 + (D' - \hat{d}(t))\mathbf{B}_2 \right) (\mathbf{U} + \hat{\mathbf{u}}(t)) \\ (\mathbf{Y} + \hat{\mathbf{y}}(t)) &= \left((D + \hat{d}(t))\mathbf{C}_1 + (D' - \hat{d}(t))\mathbf{C}_2 \right) (\mathbf{X} + \hat{\mathbf{x}}(t)) \\ &\quad + \left((D + \hat{d}(t))\mathbf{E}_1 + (D' - \hat{d}(t))\mathbf{E}_2 \right) (\mathbf{U} + \hat{\mathbf{u}}(t))\end{aligned}\tag{7.127}$$

The derivative $d\mathbf{X}/dt$ is zero. By collecting terms, one obtains

$$\begin{aligned}\underbrace{\mathbf{K} \frac{d\hat{\mathbf{x}}(t)}{dt}}_{\text{first order ac}} &= \underbrace{(\mathbf{AX} + \mathbf{BU})}_{\text{dc terms}} + \underbrace{\mathbf{A}\hat{\mathbf{x}}(t) + \mathbf{B}\hat{\mathbf{u}}(t) + \{(A_1 - A_2)\mathbf{X} + (B_1 - B_2)\mathbf{U}\}\hat{d}(t)}_{\text{first-order ac terms}} \\ &\quad + \underbrace{(\mathbf{A}_1 - \mathbf{A}_2)\hat{\mathbf{x}}(t)\hat{d}(t) + (\mathbf{B}_1 - \mathbf{B}_2)\hat{\mathbf{u}}(t)\hat{d}(t)}_{\text{second-order nonlinear terms}} \\ \underbrace{(\mathbf{Y} + \hat{\mathbf{y}}(t))}_{\text{dc+1st order ac}} &= \underbrace{(\mathbf{CX} + \mathbf{EU})}_{\text{dc terms}} + \underbrace{\mathbf{C}\hat{\mathbf{x}}(t) + \mathbf{E}\hat{\mathbf{u}}(t) + \{(C_1 - C_2)\mathbf{X} + (E_1 - E_2)\mathbf{U}\}\hat{d}(t)}_{\text{first-order ac terms}} \\ &\quad + \underbrace{(\mathbf{C}_1 - \mathbf{C}_2)\hat{\mathbf{x}}(t)\hat{d}(t) + (\mathbf{E}_1 - \mathbf{E}_2)\hat{\mathbf{u}}(t)\hat{d}(t)}_{\text{second-order nonlinear terms}}\end{aligned}\tag{7.128}$$

Since the dc terms satisfy Eq. (7.124), they drop out of Eq. (7.128). Also, if the small-signal assumption (7.126) is satisfied, then the second-order nonlinear terms of Eq. (7.128) are small in magnitude compared to the first-order ac terms. We can therefore neglect the nonlinear terms, to obtain the following linearized ac model:

$$\begin{aligned}\mathbf{K} \frac{d\hat{\mathbf{x}}(t)}{dt} &= \mathbf{A}\hat{\mathbf{x}}(t) + \mathbf{B}\hat{\mathbf{u}}(t) + \{(A_1 - A_2)\mathbf{X} + (B_1 - B_2)\mathbf{U}\}\hat{d}(t) \\ \hat{\mathbf{y}}(t) &= \mathbf{C}\hat{\mathbf{x}}(t) + \mathbf{E}\hat{\mathbf{u}}(t) + \{(C_1 - C_2)\mathbf{X} + (E_1 - E_2)\mathbf{U}\}\hat{d}(t)\end{aligned}\tag{7.129}$$

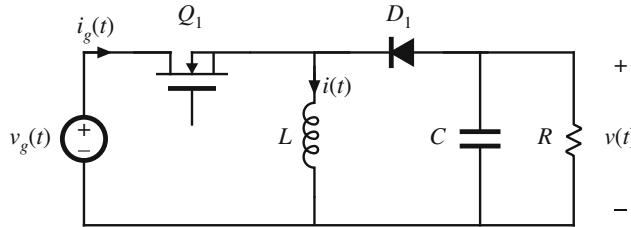
This is the desired result, which coincides with Eq. (7.109).

7.5.4 Example: State-Space Averaging of a Nonideal Buck-Boost Converter

Let us apply the state-space averaging method to model the buck-boost converter of Fig. 7.42. We will model the conduction loss of MOSFET Q_1 by on-resistance R_{on} , and the forward voltage drop of diode D_1 by an independent voltage source of value V_D . It is desired to obtain a complete equivalent circuit, which models both the input port and the output port of the converter.

The independent states of the converter are the inductor current $i(t)$ and the capacitor voltage $v(t)$. Therefore, we should define the state vector $\mathbf{x}(t)$ as

$$\mathbf{x}(t) = \begin{bmatrix} i(t) \\ v(t) \end{bmatrix}\tag{7.130}$$

**Fig. 7.42** Buck-boost converter example

The input voltage $v_g(t)$ is an independent source which should be placed in the input vector $\mathbf{u}(t)$. In addition, we have chosen to model the diode forward voltage drop with an independent voltage source of value V_D . So this voltage source should also be included in the input vector $\mathbf{u}(t)$. Therefore, let us define the input vector as

$$\mathbf{u}(t) = \begin{bmatrix} v_g(t) \\ V_D \end{bmatrix} \quad (7.131)$$

To model the converter input port, we need to find the converter input current $i_g(t)$. To calculate this dependent current, it should be included in the output vector $\mathbf{y}(t)$. Therefore, let us choose to define $\mathbf{y}(t)$ as

$$\mathbf{y}(t) = [i_g(t)] \quad (7.132)$$

Note that it is not necessary to include the output voltage $v(t)$ in the output vector $\mathbf{y}(t)$, since $v(t)$ is already included in the state vector $\mathbf{x}(t)$.

Next, let us write the state equations for each subinterval. When the switch is in position 1, the converter circuit of Fig. 7.43a is obtained. The inductor voltage, capacitor current, and converter input current are

$$\begin{aligned} L \frac{di(t)}{dt} &= v_g(t) - i(t)R_{on} \\ C \frac{dv(t)}{dt} &= -\frac{v(t)}{R} \\ i_g(t) &= i(t) \end{aligned} \quad (7.133)$$

These equations can be written in the following state-space form:

$$\underbrace{\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}}_{\mathbf{K}} \underbrace{\frac{d}{dt} \begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\mathbf{dx}(t)} = \underbrace{\begin{bmatrix} -R_{on} & 0 \\ 0 & -\frac{1}{R} \end{bmatrix}}_{\mathbf{A}_1} \underbrace{\begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}}_{\mathbf{B}_1} \underbrace{\begin{bmatrix} v_g(t) \\ V_D \end{bmatrix}}_{\mathbf{u}(t)} \quad (7.134)$$

$$\underbrace{\begin{bmatrix} i_g(t) \\ y(t) \end{bmatrix}}_{\mathbf{y}(t)} = \underbrace{\begin{bmatrix} 1 & 0 \end{bmatrix}}_{\mathbf{C}_1} \underbrace{\begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 0 & 0 \end{bmatrix}}_{\mathbf{E}_1} \underbrace{\begin{bmatrix} v_g(t) \\ V_D \end{bmatrix}}_{\mathbf{u}(t)}$$

So we have identified the state equation matrices \mathbf{A}_1 , \mathbf{B}_1 , \mathbf{C}_1 , and \mathbf{E}_1 .

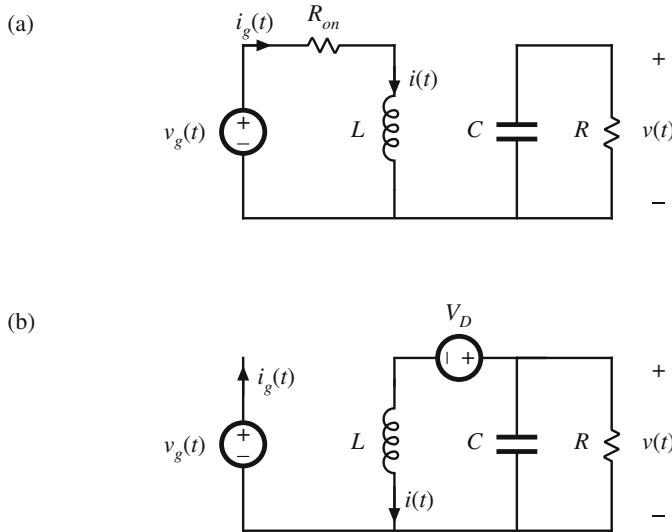


Fig. 7.43 Buck-boost converter circuit: (a) during subinterval 1, (b) during subinterval 2

With the switch in position 2, the converter circuit of Fig. 7.43b is obtained. For this subinterval, the inductor voltage, capacitor current, and converter input current are given by

$$\begin{aligned} L \frac{di(t)}{dt} &= v(t) - V_D \\ C \frac{dv(t)}{dt} &= -\frac{v(t)}{R} - i(t) \\ i_g(t) &= 0 \end{aligned} \quad (7.135)$$

When written in state-space form, these equations become

$$\underbrace{\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}}_{\mathbf{K}} \underbrace{\frac{d}{dt} \begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\frac{d\mathbf{x}(t)}{dt}} = \underbrace{\begin{bmatrix} 0 & 1 \\ -1 & -\frac{1}{R} \end{bmatrix}}_{\mathbf{A}_2} \underbrace{\begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 0 & -1 \\ 0 & 0 \end{bmatrix}}_{\mathbf{B}_2} \underbrace{\begin{bmatrix} v_g(t) \\ V_D \end{bmatrix}}_{\mathbf{u}(t)}$$

$$\underbrace{\begin{bmatrix} i_g(t) \\ v(t) \end{bmatrix}}_{\mathbf{y}(t)} = \underbrace{\begin{bmatrix} 0 & 0 \end{bmatrix}}_{\mathbf{C}_2} \underbrace{\begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 0 & 0 \end{bmatrix}}_{\mathbf{E}_2} \underbrace{\begin{bmatrix} v_g(t) \\ V_D \end{bmatrix}}_{\mathbf{u}(t)} \quad (7.136)$$

So we have also identified the subinterval 2 matrices \mathbf{A}_2 , \mathbf{B}_2 , \mathbf{C}_2 , and \mathbf{E}_2 .

The next step is to evaluate the state-space averaged equilibrium equations (7.106) to (7.108). The averaged matrix \mathbf{A} is

$$\mathbf{A} = D\mathbf{A}_1 + D'\mathbf{A}_2 = D \begin{bmatrix} -R_{on} & 0 \\ 0 & -\frac{1}{R} \end{bmatrix} + D' \begin{bmatrix} 0 & 1 \\ -1 & -\frac{1}{R} \end{bmatrix} = \begin{bmatrix} -DR_{on} & D' \\ -D' & -\frac{1}{R} \end{bmatrix} \quad (7.137)$$

In a similar manner, the averaged matrices \mathbf{B} , \mathbf{C} , and \mathbf{E} are evaluated, with the following results:

$$\begin{aligned} \mathbf{B} &= D\mathbf{B}_1 + D'\mathbf{B}_2 = \begin{bmatrix} D & -D' \\ 0 & 0 \end{bmatrix} \\ \mathbf{C} &= D\mathbf{C}_1 + D'\mathbf{C}_2 = \begin{bmatrix} D & 0 \end{bmatrix} \\ \mathbf{E} &= D\mathbf{E}_1 + D'\mathbf{E}_2 = \begin{bmatrix} 0 & 0 \end{bmatrix} \end{aligned} \quad (7.138)$$

The dc state equations (7.106) therefore become

$$\begin{aligned} \begin{bmatrix} 0 \\ 0 \end{bmatrix} &= \begin{bmatrix} -DR_{on} & D' \\ -D' & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} I \\ V \end{bmatrix} + \begin{bmatrix} D & -D' \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_g \\ V_D \end{bmatrix} \\ \begin{bmatrix} I_g \end{bmatrix} &= \begin{bmatrix} D & 0 \end{bmatrix} \begin{bmatrix} I \\ V \end{bmatrix} + \begin{bmatrix} 0 & 0 \end{bmatrix} \begin{bmatrix} V_g \\ V_D \end{bmatrix} \end{aligned} \quad (7.139)$$

Evaluation of Eq. (7.109) leads to the following solution for the equilibrium state and output vectors:

$$\begin{aligned} \begin{bmatrix} I \\ V \end{bmatrix} &= \left(\frac{1}{1 + \frac{D}{D'^2} \frac{R_{on}}{R}} \right) \begin{bmatrix} D & \frac{1}{D'R} \\ \frac{D}{D'^2 R} & 1 \end{bmatrix} \begin{bmatrix} V_g \\ V_D \end{bmatrix} \\ \begin{bmatrix} I_g \end{bmatrix} &= \left(\frac{1}{1 + \frac{D}{D'^2} \frac{R_{on}}{R}} \right) \begin{bmatrix} D^2 & \frac{1}{D'R} \end{bmatrix} \begin{bmatrix} V_g \\ V_D \end{bmatrix} \end{aligned} \quad (7.140)$$

Alternatively, the steady-state equivalent circuit of Fig. 7.44 can be constructed as usual from Eq. (7.139). The top row of Eq. (7.139) could have been obtained by application of the principle of inductor volt-second balance to the inductor voltage waveform. The second row of Eq. (7.139) could have been obtained by application of the principle of capacitor charge balance to the capacitor current waveform. The $i_g(t)$ equation expresses the dc component of the converter input current. By reconstructing circuits that are equivalent to these three equations, the dc model of Fig. 7.44 is obtained.

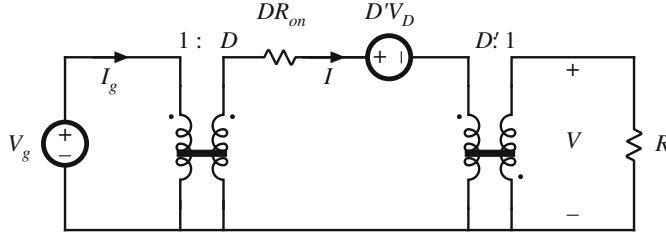


Fig. 7.44 Dc circuit model for the buck–boost converter model, equivalent to Eq. (7.139)

The small-signal model is found by evaluation of Eq. (7.109). The vector coefficients of $\hat{d}(t)$ in Eq. (7.109) are

$$\begin{aligned} (\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U} &= \begin{bmatrix} -V - IR_{on} \\ I \end{bmatrix} + \begin{bmatrix} V_g + V_D \\ 0 \end{bmatrix} = \begin{bmatrix} V_g - V - IR_{on} + V_D \\ I \end{bmatrix} \\ (\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X} + (\mathbf{E}_1 - \mathbf{E}_2)\mathbf{U} &= [I] \end{aligned} \quad (7.141)$$

The small-signal ac state equations (7.109) therefore become

$$\begin{aligned} \begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \hat{i}(t) \\ \hat{v}(t) \end{bmatrix} &= \begin{bmatrix} -DR_{on} & D' \\ -D' & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} \hat{i}(t) \\ \hat{v}(t) \end{bmatrix} + \begin{bmatrix} D & -D' \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_g(t) \\ 0 \end{bmatrix} + \begin{bmatrix} V_g - V - IR_{on} + V_D \\ I \end{bmatrix} \hat{d}(t) \\ \begin{bmatrix} \hat{i}_g(t) \\ \hat{v}_g(t) \end{bmatrix} &= \begin{bmatrix} D & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}(t) \\ \hat{v}(t) \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_g(t) \\ 0 \end{bmatrix} + [I]\hat{d}(t) \end{aligned} \quad (7.142)$$

Note that, since the diode forward voltage drop is modeled as the constant value V_D , there are no ac variations in this source, and $\hat{v}_D(t)$ equals zero. Again, a circuit model equivalent to Eq. (7.142) can be constructed, in the usual manner. When written in scalar form, Eq. (7.142) becomes

$$\begin{aligned} L \frac{d\hat{i}(t)}{dt} &= D'\hat{v}(t) - DR_{on}\hat{i}(t) + D\hat{v}_g(t) + (V_g - V - IR_{on} + V_D)\hat{d}(t) \\ C \frac{d\hat{v}(t)}{dt} &= -D'\hat{i}(t) - \frac{\hat{v}(t)}{R} + I\hat{d}(t) \\ \hat{i}_g(t) &= D\hat{i}(t) + I\hat{d}(t) \end{aligned} \quad (7.143)$$

Circuits corresponding to these equations are listed in Fig. 7.45. These circuits can be combined into the complete small-signal ac equivalent circuit model of Fig. 7.46.

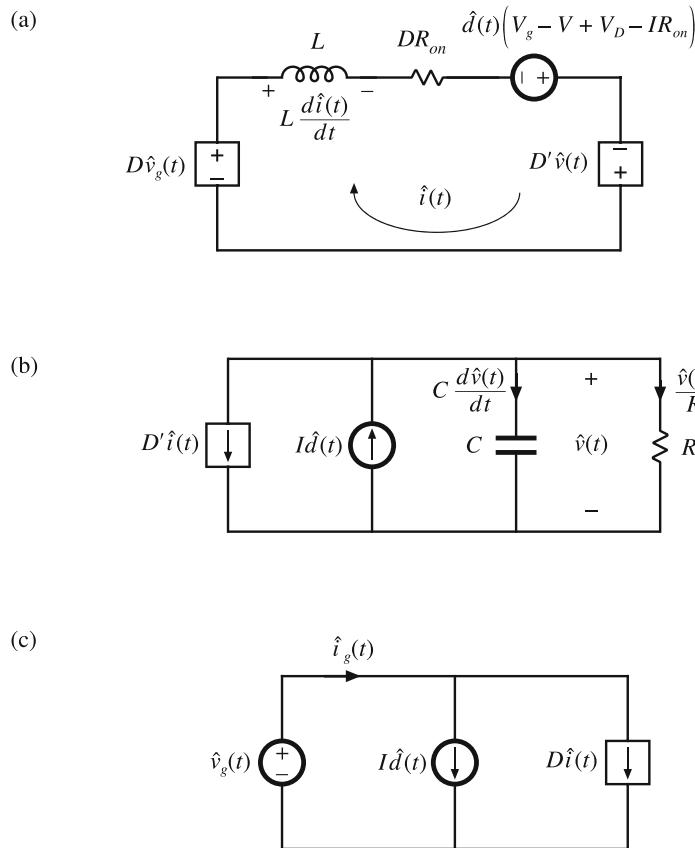


Fig. 7.45 Circuits equivalent to the small-signal converter equations: (a) inductor loop, (b) capacitor node, (c) input port

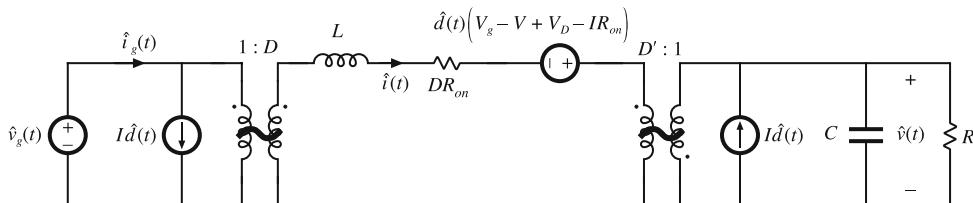


Fig. 7.46 Complete small-signal ac equivalent circuit model, nonideal buck-boost converter example

7.5.5 Example: State-Space Averaging of a Boost Converter with ESR

As a final example, let us employ the state-space averaging method to derive the model of the nonideal boost converter of Fig. 7.47. This circuit includes a resistor R_C that models the capacitor equivalent series resistance; the dashed line encloses the capacitor model including an ideal capacitor C and ESR R_C . Students often experience difficulty in deriving the averaged equations

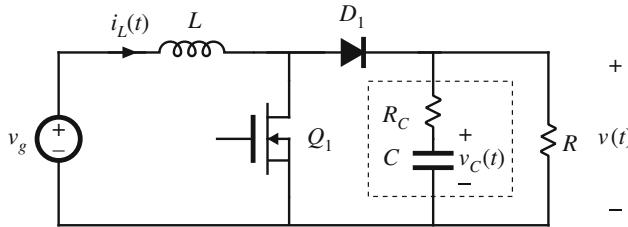


Fig. 7.47 Boost converter circuit, including capacitor equivalent series resistance R_C

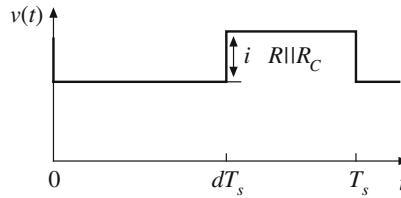


Fig. 7.48 The capacitor ESR causes the output voltage waveform $v(t)$ to become discontinuous

of this circuit, and the state-space averaging method provides a framework for correctly deriving the averaged model. With the exception of the capacitor ESR, we will model all elements as ideal.

As illustrated in Fig. 7.48, the capacitor ESR causes the output voltage $v(t)$ to be discontinuous. When the diode conducts, the inductor current causes the output voltage to be greater by an amount $i_L(t)R||R_C$ and so the voltage exhibits a discontinuity during the switching times. Hence, we must be careful not to attempt to apply the small-ripple approximation to the output voltage $v(t)$. On the other hand, the voltage $v_C(t)$ of the ideal capacitor portion of the capacitor model is continuous and exhibits small ripple.

The independent states of this circuit are the inductor current $i_L(t)$ and the capacitor voltage $v_C(t)$. Note that $v_C(t)$ is defined as the voltage across the ideal capacitor portion of the capacitor model. The state vector $\mathbf{x}(t)$ is therefore defined as

$$\mathbf{x}(t) = \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} \quad (7.144)$$

The input voltage $v_g(t)$ is an independent source which should be placed in the input vector $\mathbf{u}(t)$. We have chosen to model no other independent sources. Therefore, let us define the input vector as

$$\mathbf{u}(t) = [v_g(t)] \quad (7.145)$$

To model the converter input port, we need to find the converter input current $i_g(t)$. For the boost converter, the input current $i_g(t)$ coincides with the inductor current $i_L(t)$. Since $i_L(t)$ is already in the state vector $\mathbf{x}(t)$, no additional information is gained by inclusion of $i_g(t)$ in the output vector. On the other hand, to model the output port, we must write an equation for the output voltage $v(t)$. Since the actual output voltage $v(t)$ no longer coincides with the capacitor state

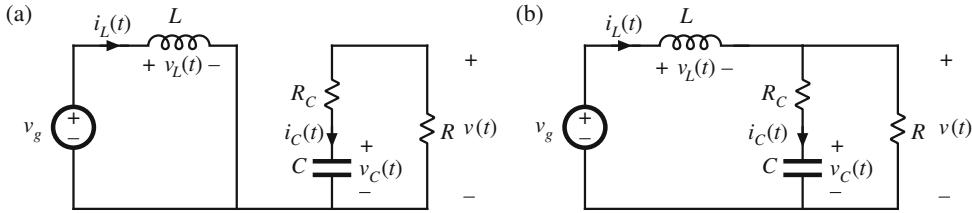


Fig. 7.49 Boost with ESR converter circuit: (a) during subinterval 1, (b) during subinterval 2

$v_C(t)$, we must write additional equations that can be solved for the averaged output voltage. Therefore $v(t)$ must be included in the output vector. Hence, let us choose to define $\mathbf{y}(t)$ as

$$\mathbf{y}(t) = \begin{bmatrix} v(t) \end{bmatrix} \quad (7.146)$$

Thus for this example, the output vector contains only the dependent quantity $v(t)$.

Next, we will develop the state equations for each subinterval. For the first subinterval, the MOSFET conducts and the converter circuit reduces to that of Fig. 7.49a. We can express the inductor voltage and capacitor current as:

$$\begin{aligned} L \frac{di_L(t)}{dt} &= v_g(t) \\ C \frac{dv_C(t)}{dt} &= -\frac{v_C(t)}{R + R_C} \end{aligned} \quad (7.147)$$

Note that we have been careful to express the capacitor current in terms of the capacitor voltage $v_C(t)$, rather than the output voltage $v(t)$. This is necessary because the state equations must be written as functions of the elements of the independent vectors $\mathbf{x}(t)$ and $\mathbf{u}(t)$, but not the dependent vector $\mathbf{y}(t)$.

For the first subinterval, we can express the output quantity also as a function of the elements of $\mathbf{x}(t)$ and $\mathbf{u}(t)$, as follows:

$$v(t) = v_C(t) \frac{R}{R + R_C} \quad (7.148)$$

Again, we have been careful to express $v(t)$ as a function of the capacitor state $v_C(t)$.

We can next write Eqs. (7.147) and (7.148) in matrix form. The result is

$$\begin{aligned} \underbrace{\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}}_{\mathbf{K}} \underbrace{\frac{d}{dt} \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix}}_{\frac{d\mathbf{x}(t)}{dt}} &= \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R + R_C} \end{bmatrix}}_{\mathbf{A}_1} \underbrace{\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 1 \\ 0 \end{bmatrix}}_{\mathbf{B}_1} \underbrace{\begin{bmatrix} v_g(t) \end{bmatrix}}_{\mathbf{u}(t)} \\ \mathbf{y}(t) &= \underbrace{\begin{bmatrix} v(t) \end{bmatrix}}_{\mathbf{y}(t)} = \underbrace{\begin{bmatrix} 0 & \frac{R}{R + R_C} \end{bmatrix}}_{\mathbf{C}_1} \underbrace{\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 0 \end{bmatrix}}_{\mathbf{E}_1} \underbrace{\begin{bmatrix} v_g(t) \end{bmatrix}}_{\mathbf{u}(t)} \end{aligned} \quad (7.149)$$

For the second subinterval, the MOSFET is off and the diode conducts. The circuit of Fig. 7.49b is obtained. We can express the inductor voltage and capacitor current as:

$$\begin{aligned} L \frac{di_L(t)}{dt} &= v_g(t) - v(t) = v_g(t) - v_C(t) \frac{R}{R + R_C} - i_L(t) R \| R_C \\ C \frac{dv_C(t)}{dt} &= \frac{v(t) - v_C(t)}{R_C} = -\frac{v_C(t)}{R + R_C} + i_L(t) \frac{R}{R + R_C} \end{aligned} \quad (7.150)$$

In the above equations, it was necessary to eliminate the output voltage $v(t)$, again because the state equations must be written as functions of the elements of the independent vectors $\mathbf{x}(t)$ and $\mathbf{u}(t)$, but not the dependent vector $\mathbf{y}(t)$. The notation $R \| R_C$ denotes the parallel combination of R and R_C .

For this subinterval, we can express the output also as a function of the elements of $\mathbf{x}(t)$ and $\mathbf{u}(t)$, as follows:

$$v(t) = v_C(t) \frac{R}{R + R_C} + i_L(t) R \| R_C \quad (7.151)$$

Again, we have been careful to express $v(t)$ as a function of the capacitor state $v_C(t)$. We can now assemble the above equations to obtain the state-space description of the circuit during the second subinterval:

$$\underbrace{\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}}_{\mathbf{K}} \underbrace{\frac{d}{dt} \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix}}_{\frac{d\mathbf{x}(t)}{dt}} = \underbrace{\begin{bmatrix} -R \| R_C & \frac{R}{R + R_C} \\ \frac{R}{R + R_C} & -\frac{1}{R + R_C} \end{bmatrix}}_{\mathbf{A}_2} \underbrace{\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 1 \\ 0 \end{bmatrix}}_{\mathbf{B}_2} \underbrace{\begin{bmatrix} v_g(t) \end{bmatrix}}_{\mathbf{u}(t)} \quad (7.152)$$

$$\underbrace{\begin{bmatrix} v(t) \end{bmatrix}}_{\mathbf{y}(t)} = \underbrace{\begin{bmatrix} R \| R_C & \frac{R}{R + R_C} \end{bmatrix}}_{\mathbf{C}_2} \underbrace{\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 0 \\ 1 \end{bmatrix}}_{\mathbf{E}_2} \underbrace{\begin{bmatrix} v_g(t) \end{bmatrix}}_{\mathbf{u}(t)}$$

The state-space averaging method predicts that the converter steady-state model is

$$\underbrace{\begin{bmatrix} 0 \\ 0 \end{bmatrix}}_{\mathbf{0}} = \underbrace{\begin{bmatrix} -D'(R \| R_C) & -D' \frac{R}{R + R_C} \\ D' \frac{R}{R + R_C} & -\frac{1}{R + R_C} \end{bmatrix}}_{D\mathbf{A}_1 + D'\mathbf{A}_2} \underbrace{\begin{bmatrix} I_L \\ V_C \end{bmatrix}}_{\mathbf{X}} + \underbrace{\begin{bmatrix} 1 \\ 0 \end{bmatrix}}_{D\mathbf{B}_1 + D'\mathbf{B}_2} \underbrace{\begin{bmatrix} V_g \end{bmatrix}}_{\mathbf{U}} \quad (7.153)$$

$$\underbrace{\begin{bmatrix} V \end{bmatrix}}_{\mathbf{Y}} = \underbrace{\begin{bmatrix} D'(R \| R_C) & \frac{R}{R + R_C} \\ DC_1 + D'C_2 & \frac{R}{R + R_C} \end{bmatrix}}_{DC_1 + D'C_2} \underbrace{\begin{bmatrix} I_L \\ V_C \end{bmatrix}}_{\mathbf{X}} + \underbrace{\begin{bmatrix} 0 \\ 1 \end{bmatrix}}_{DE_1 + D'E_2} \underbrace{\begin{bmatrix} V_g \end{bmatrix}}_{\mathbf{U}}$$

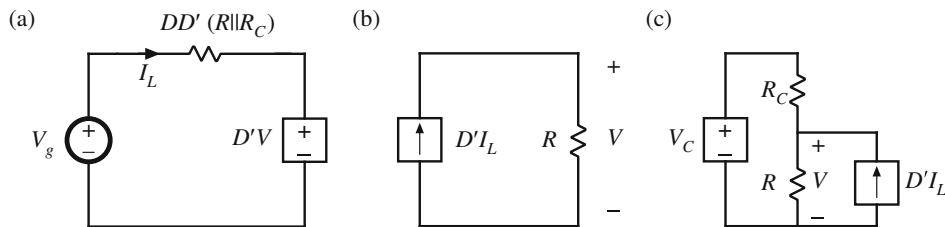


Fig. 7.50 Steps in the construction of the steady-state equivalent circuit for the boost converter with capacitor equivalent series resistance: (a) inductor loop, (b) output node, (c) connection of capacitor to output node

Let us construct a steady-state equivalent circuit corresponding to the above equations. The output terminal of our converter is the output voltage V , rather than the capacitor voltage V_C . Therefore, it is helpful to first express the above equations in terms of the output voltage V , by using the output equation to eliminate V_C . This leads to the following equations:

$$0 = V_g - D'V - DD'I_L(R\parallel R_C) \quad (7.154a)$$

$$0 = D'I_L - \frac{V}{R} \quad (7.154b)$$

$$V = V_C \frac{R}{R + R_C} + D'I_L(R\parallel R_C) \quad (7.154c)$$

Equation (7.154a) can be recognized as a voltage loop equation, resulting from volt-second balance on the inductor. The current of this loop is the dc inductor current I_L . Construction of an equivalent circuit corresponding to this equation leads to the network of Fig. 7.50a. Likewise, Eq. (7.154b) is the equation of the output node, having voltage V . A corresponding equivalent circuit for this equation is shown in Fig. 7.50b. Equation (7.154c) describes how the capacitor C and its voltage V_C is connected to the output node. We might expect that the ideal capacitor element C is connected through the ESR R_C to the output node, as it is in the original converter circuit of Fig. 7.47. Indeed this is the case: Fig. 7.50c is a circuit corresponding to Eq. (7.154c), with the capacitor voltage V_C connected to the output node voltage V through resistor R_C . Resistors R and R_C constitute a voltage divider having the divider ratio $R/(R + R_C)$ shown in Eq. (7.154c). The second term in the equation accounts for how the current $D'I_L$ increases the output voltage, through the Thevenin-equivalent output resistance of the voltage divider, $R\parallel R_C$.

The circuits of Fig. 7.50 can be combined into the complete steady-state equivalent circuit illustrated in Fig. 7.51. It can be observed that the steady-state voltages V and V_C are equal. Additionally, the capacitor ESR leads to an additional effective series resistor $DD'(R\parallel R_C)$. This resistor models the loss induced in the ESR by the ac capacitor current, and its effect on the converter efficiency.

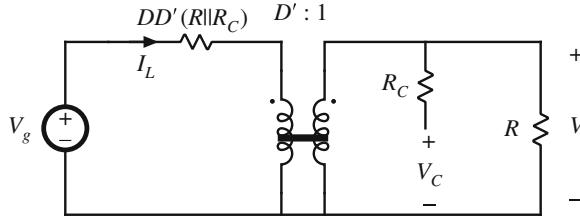


Fig. 7.51 Steady-state model of the boost converter, including effects of capacitor equivalent series resistance R_C

The small-signal ac state-space averaged model is found by evaluation of Eq. (7.110). The result is

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_C(t) \end{bmatrix} = \begin{bmatrix} -D'(R||R_C) & -D' \frac{R}{R+R_C} \\ D' \frac{R}{R+R_C} & -\frac{1}{R+R_C} \end{bmatrix} \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_C(t) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} \begin{bmatrix} \hat{v}_g(t) \end{bmatrix} \quad (7.155)$$

$$+ \begin{bmatrix} I_L R || R_C + V_C \frac{R}{R+R_C} \\ -I_L \frac{R}{R+R_C} \end{bmatrix} \hat{d}(t) \quad (7.156)$$

$$\begin{bmatrix} \hat{v}(t) \end{bmatrix} = \begin{bmatrix} D'(R||R_C) & \frac{R}{R+R_C} \end{bmatrix} \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_C(t) \end{bmatrix} + \begin{bmatrix} -I_L R || R_C \end{bmatrix} \hat{d}(t) \quad (7.157)$$

To construct a small-signal ac circuit model, it is helpful to again express the equations in terms of the converter output voltage \hat{v} rather than the capacitor voltage \hat{v}_C . This is accomplished by using the output equation to eliminate \hat{v}_C from the right side of the state equations. After some algebra, we obtain

$$L \frac{d\hat{i}_L}{dt} = \hat{v}_g - D'\hat{v} - DD'(R||R_C)\hat{i}_L + ((D - D')(R||R_C)I_L + V)\hat{d} \quad (7.158a)$$

$$C \frac{d\hat{v}_C}{dt} = D'\hat{i}_L - \frac{\hat{v}}{R} - I_L\hat{d} \quad (7.158b)$$

$$\hat{v} = \hat{v}_C \frac{R}{R+R_C} + (D'\hat{i}_L - I_L\hat{d})(R||R_C) \quad (7.158c)$$

Equation (7.158a) can be recognized as a voltage loop equation, describing the small-signal ac components of the voltage around a loop containing the inductor. The current of this loop is the ac inductor current \hat{i}_L . Construction of an equivalent circuit corresponding to this equation

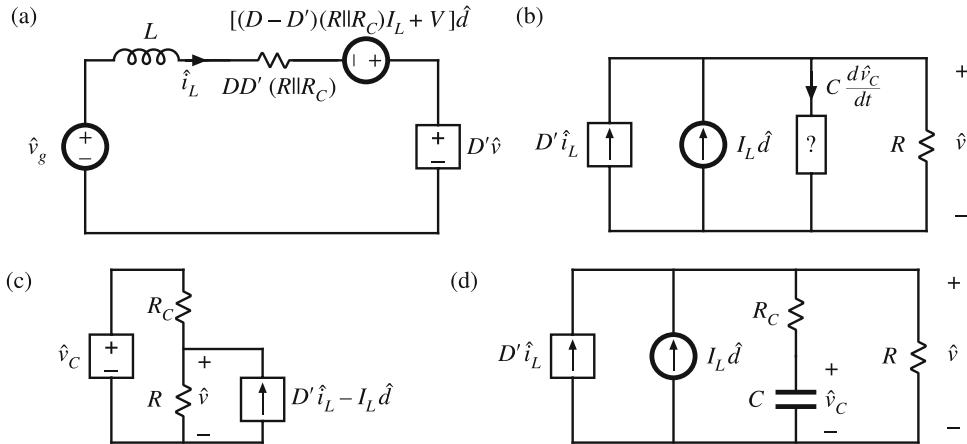


Fig. 7.52 Steps in the construction of the small-signal ac equivalent circuit for the boost converter with capacitor equivalent series resistance: (a) inductor loop, (b) output node, (c) connection of capacitor to output node, (d) composite circuit, output node and capacitor

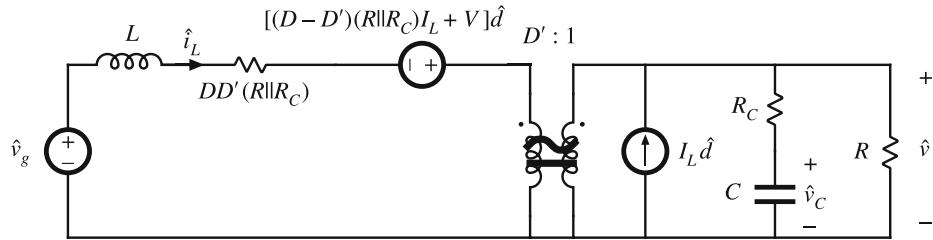


Fig. 7.53 Complete small-signal ac model of the boost converter, including effects of capacitor equivalent series resistance R_C

leads to the network of Fig. 7.52a. Likewise, Eq. (7.158b) is the equation of the output node, having voltage \hat{v} . A corresponding equivalent circuit for this equation is shown in Fig. 7.52b. Although the capacitor current $C d\hat{v}_C/dt$ flows out of this node, Eq. (7.158b) does not describe whether the capacitor is connected through the capacitor ESR, and so at this point we will leave the capacitor branch as an unknown element.

Equation (7.158c) describes how the capacitor C and its voltage \hat{v}_C are connected to the output node. As in the steady-state model, we expect that the ideal capacitor element C is connected through the ESR R_C to the output node. Again, this is the case: Fig. 7.52c is a circuit corresponding to Eq. (7.158c), with the capacitor voltage \hat{v}_C connected to the output node voltage \hat{v} through resistor R_C . Resistors R and R_C again constitute a voltage divider having the

divider ratio $R/(R + R_C)$ shown in Eq. (7.158c). The second term in the equation accounts for how the total current ($D'\hat{i}_L + I_L\hat{d}$) (from the transformer secondary plus the \hat{d} current source) increases the output voltage, through the Thevenin-equivalent output resistance of the voltage divider, $R||R_C$. The circuits of Fig. 7.52b and c can be combined into the single circuit illustrated in Fig. 7.52d.

The circuits of Fig. 7.52a,d now can be combined, and the dependent sources replaced by an effective transformer as illustrated in Fig. 7.53. In this small-signal ac model, the voltages \hat{v} and \hat{v}_C can differ, and the capacitor ESR leads to new transfer function dynamics not present in the converter without ESR.

7.6 Summary of Key Points

1. The CCM converter analytical techniques of Chaps. 2 and 3 can be extended to predict converter ac behavior. The key step is to average the converter waveforms over one switching period. This removes the switching harmonics, thereby exposing directly the desired dc and low-frequency ac components of the waveforms. In particular, expressions for the averaged inductor voltages, capacitor currents, and converter input current are usually found.
2. Since switching converters are nonlinear systems, it is desirable to construct small-signal linearized models. This is accomplished by perturbing and linearizing the averaged model about a quiescent operating point.
3. Ac equivalent circuits can be constructed, in the same manner used in Chap. 3 to construct dc equivalent circuits. If desired, the ac equivalent circuits may be refined to account for the effects of converter losses and other nonidealities.
4. The conventional pulse-width modulator circuit has linear gain, dependent on the slope of the sawtooth waveform, or equivalently on its peak-to-peak magnitude. The pulse-width modulator also introduces sampling to the system.
5. The canonical circuit describes the basic properties shared by all dc–dc PWM converters operating in the continuous conduction mode. At the heart of the model is the ideal $1:M(D)$ transformer, introduced in Chap. 3 to represent the basic dc–dc conversion function, and generalized here to include ac variations. The converter reactive elements introduce an effective low-pass filter into the network. The model also includes independent sources that represent the effect of duty-cycle variations. The parameter values in the canonical models of several basic converters are tabulated for easy reference.
6. The state-space averaging method of Sect. 7.5 is essentially the same as the basic approach of Sect. 7.2, except that the formality of the state-space network description is used. The general results are listed in Sect. 7.5.2. State-space averaging is a formal approach that shows how a small-signal averaged model can always be derived, provided that the state equations can be written for each subinterval.

PROBLEMS

7.1 An ideal boost converter operates in the continuous conduction mode.

- (a) Determine the nonlinear averaged equations of this converter.
- (b) Now construct a small-signal ac model. Let

$$\begin{aligned}\langle v_g(t) \rangle_{T_s} &= V_g + \hat{v}_g(t) \\ d(t) &= D + \hat{d}(t) \\ \langle i(t) \rangle_{T_s} &= I + \hat{i}(t) \\ \langle v(t) \rangle_{T_s} &= V + \hat{v}(t)\end{aligned}$$

where V_g , D , I , and V are steady-state dc values; $\hat{v}_g(t)$ and $\hat{d}(t)$ are small ac variations in the power and control inputs; and $\hat{i}(t)$ and $\hat{v}(t)$ are the resulting small ac variations in the inductor current and output voltage, respectively. Show that the following model results:

Large-signal dc components

$$\begin{aligned}0 &= -D'V + V_g \\ 0 &= D'I - \frac{V}{R}\end{aligned}$$

Small-signal ac components

$$\begin{aligned}L \frac{d\hat{i}(t)}{dt} &= -D'\hat{v}(t) + V\hat{d}(t) + \hat{v}_g(t) \\ C \frac{d\hat{v}(t)}{dt} &= D'\hat{i}(t) - I\hat{d}(t) - \frac{\hat{v}(t)}{R}\end{aligned}$$

7.2 Construct an equivalent circuit that corresponds to the boost converter small-signal ac equations derived in Problem 7.1(b).

7.3 Manipulate your boost converter equivalent circuit of Problem 7.2 into canonical form. Explain each step in your derivation. Verify that the elements in your canonical model agree with Table 7.1.

7.4 The ideal current-fed bridge converter of Fig. 2.32 operates in the continuous conduction mode.

- (a) Determine the nonlinear averaged equations of this converter.
- (b) Perturb and linearize, to determine the small-signal ac equations.
- (c) Construct a small-signal ac equivalent circuit model for this converter.

7.5 Construct a complete small-signal ac equivalent circuit model for the flyback converter shown in Fig. 7.19, operating in continuous conduction mode. The transformer contains magnetizing inductance L , referred to the primary. In addition, the transformer exhibits significant core loss, which can be modeled by a resistor R_C in parallel with the primary winding. All other elements are ideal. You may use any valid method to solve this problem. Your model should correctly predict variations in $i_g(t)$.

7.6 Modeling the Ćuk converter. You may use any valid method to solve this problem.

- (a) Derive the small-signal dynamic equations that model the ideal Ćuk converter.
- (b) Construct a complete small-signal equivalent circuit model for the Ćuk converter.

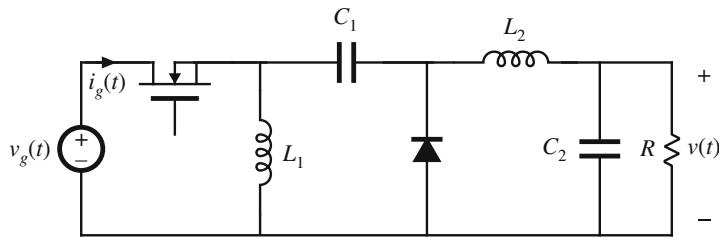


Fig. 7.54 Inverse-SEPIC, Problem 7.7

- 7.7** Modeling the inverse-SEPIC. You may use any valid method to solve this problem.
- Derive the small-signal dynamic equations that model the converter shown in Fig. 7.54.
 - Construct a complete small-signal equivalent circuit model for the inverse-SEPIC.
- 7.8** Consider the nonideal buck converter of Fig. 7.55. The input voltage source $v_g(t)$ has internal resistance R_g . Other component nonidealities may be neglected.

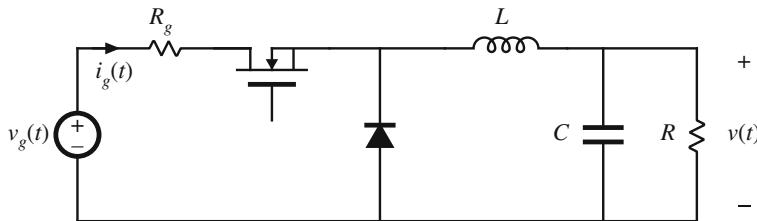


Fig. 7.55 Nonideal buck converter, Problem 7.8

- Using the state-space averaging method, determine the small-signal ac equations that describe variations in i , v , and i_g , which occur owing to variations in the transistor duty cycle d and input voltage v_g .
 - Construct an ac equivalent circuit model corresponding to your equations of part (a).
 - Solve your model to determine an expression for the small-signal control-to-output transfer function.
- 7.9** Starting with Eq. (7.19), derive Eqs. (7.20) and (7.22). Show all steps in your derivation.
- 7.10** A flyback converter operates in the continuous conduction mode. The MOSFET switch has on-resistance R_{on} , and the secondary-side diode has a constant forward voltage drop V_D . The flyback transformer has primary winding resistance R_p and secondary winding resistance R_s .
- Derive the small-signal ac equations for this converter.
 - Derive a complete small-signal ac equivalent circuit model, which is valid in the continuous conduction mode and which correctly models the above losses, as well as the converter input and output ports.
- 7.11** The two-output flyback converter of Fig. 7.56a operates in the continuous conduction mode. It may be assumed that the converter is lossless.

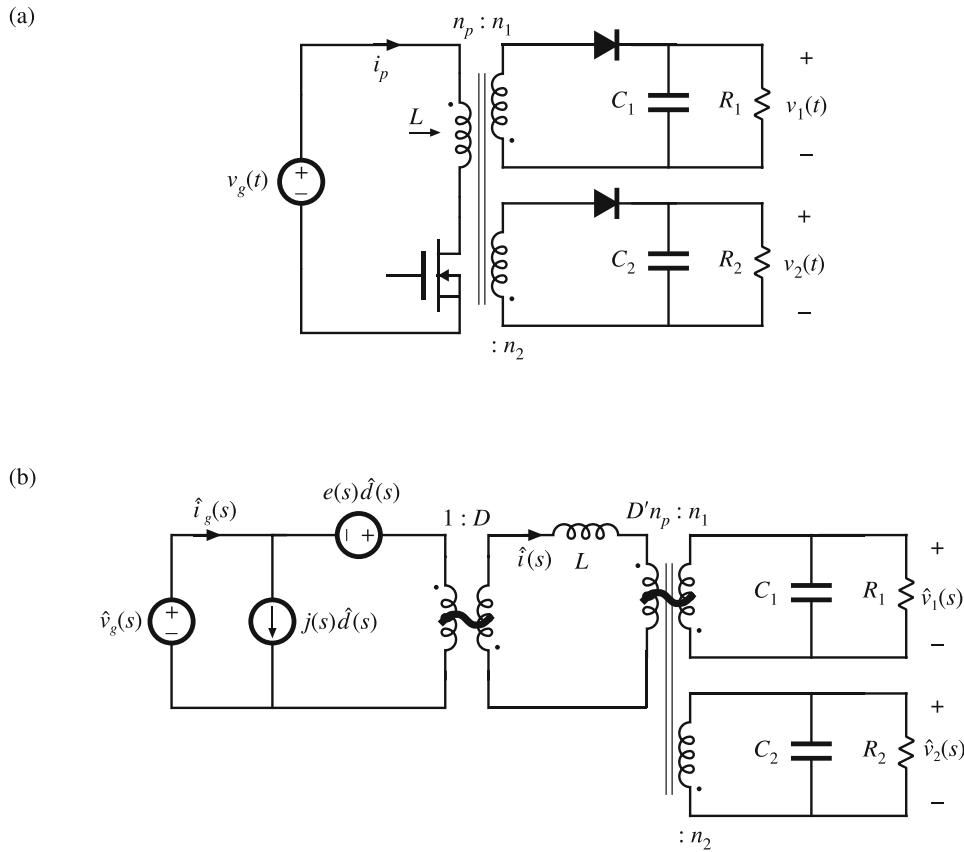


Fig. 7.56 Two-output flyback converter, Problem 7.11: (a) converter circuit, (b) small-signal ac equivalent circuit

- (a) Derive a small-signal ac equivalent circuit for this converter.
- (b) Show that the small-signal ac equivalent circuit for this two-output converter can be written in the generalized canonical form of Fig. 7.56b. Give analytical expressions for the generators $e(s)$ and $j(s)$.

7.12 A pulse-width modulator circuit is constructed in which the sawtooth-wave generator is replaced by a triangle-wave generator, as illustrated in Fig. 7.57a. The triangle waveform is illustrated in Fig. 7.57b.

- (a) Determine the converter switching frequency, in Hz.
- (b) Determine the gain $d(t)/v_c(t)$ for this circuit.
- (c) Over what range of v_c is your answer to (b) valid?

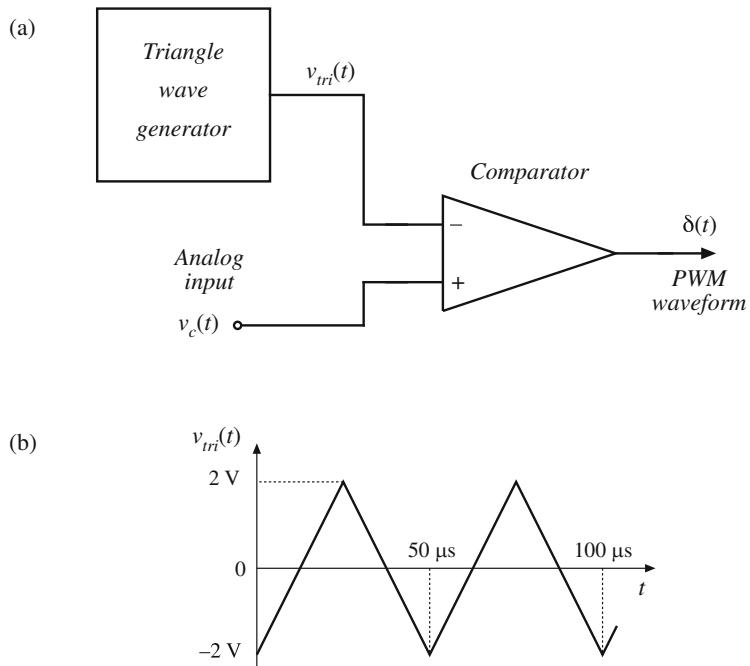


Fig. 7.57 Pulse-width modulator, Problem 7.12 (a) looks very large. Adjust magnification to be the same as (b)



Converter Transfer Functions

The engineering design process is comprised of several major steps:

1. *Specifications and other design goals* are defined.
2. *A circuit is proposed.* This is a creative process that draws on the physical insight and experience of the engineer.
3. *The circuit is modeled.* The converter power stage is modeled as described in Chap. 7. Components and other portions of the system are modeled as appropriate, often with vendor-supplied data.
4. *Design-oriented analysis* of the circuit is performed. This involves development of equations that allow element values to be chosen such that specifications and design goals are met. In addition, it may be necessary for the engineer to gain additional understanding and physical insight into the circuit behavior, so that the design can be improved by adding elements to the circuit or by changing circuit connections.
5. *Model verification.* Predictions of the model are compared to a laboratory prototype, under nominal operating conditions. The model is refined as necessary, so that the model predictions agree with laboratory measurements.
6. *Worst-case analysis* (or other reliability and production yield analysis) of the circuit is performed. This involves quantitative evaluation of the model performance, to judge whether specifications are met under all conditions. Computer simulation is well suited to this task.
7. *Iteration.* The above steps are repeated to improve the design until the worst-case behavior meets specifications, or until the reliability and production yield are acceptably high.

This chapter covers techniques of design-oriented analysis, measurement of experimental transfer functions, and computer simulation, as needed in steps 4, 5, and 6.

Sections 8.1 to 8.3 discuss techniques for analysis and construction of the Bode plots of the converter transfer functions, input impedance, and output impedance predicted by the equivalent circuit models of Chap. 7. For example, the small-signal equivalent circuit model of the buck-boost converter is illustrated in Fig. 7.18c. This model is reproduced in Fig. 8.1, with the important inputs and terminal impedances identified. The line-to-output transfer function $G_{vg}(s)$ is found by setting duty cycle variations $\hat{d}(s)$ to zero, and then solving for the transfer function from $\hat{v}_g(s)$ to $\hat{v}(s)$:

$$G_{vg}(s) = \left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\hat{d}(s)=0} \quad (8.1)$$

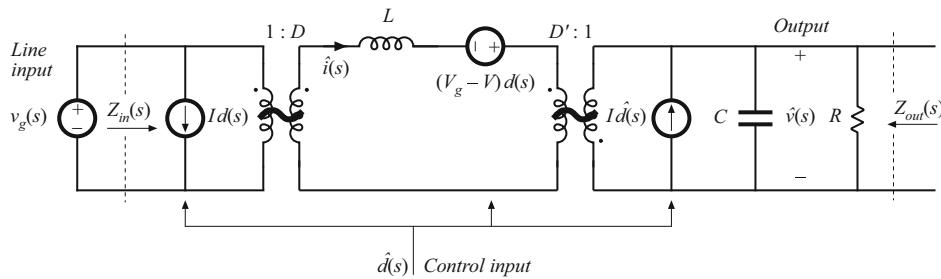


Fig. 8.1 Small-signal equivalent circuit model of the buck–boost converter, as derived in Chap. 7

This transfer function describes how variations or disturbances in the applied input voltage $v_g(t)$ lead to disturbances in the output voltage $v(t)$. It is important in design of an output voltage regulator. For example, in an off-line power supply, the converter input voltage $v_g(t)$ contains undesired even harmonics of the ac power line voltage. The transfer function $G_{vg}(s)$ is used to determine the effect of these harmonics on the converter output voltage $v(t)$.

The control-to-output transfer function $G_{vd}(s)$ is found by setting the input voltage variations $\hat{v}_g(s)$ to zero, and then solving the equivalent circuit model for $\hat{v}(s)$ as a function of $\hat{d}(s)$:

$$G_{vd}(s) = \left. \frac{\hat{v}(s)}{\hat{d}(s)} \right|_{\hat{v}_g(s)=0} \quad (8.2)$$

This transfer function describes how control input variations $\hat{d}(s)$ influence the output voltage $\hat{v}(s)$. In an output voltage regulator system, $G_{vd}(s)$ is a key component of the loop gain and has a significant effect on regulator performance.

The output impedance $Z_{out}(s)$ is found under the conditions that $\hat{v}_g(s)$ and $\hat{d}(s)$ variations are set to zero. $Z_{out}(s)$ describes how variations in the load current affect the output voltage. This quantity is also important in voltage regulator design. It may be appropriate to define $Z_{out}(s)$ either including or not including the load resistance R .

The converter input impedance $Z_{in}(s)$ plays a significant role when an electromagnetic interference (EMI) filter is added at the converter power input. The relative magnitudes of Z_{in} and the EMI filter output impedance influence whether the EMI filter disrupts the transfer function $G_{vd}(s)$. Design of input EMI filters is the subject of Chap. 17.

An objective of this chapter is the construction of Bode plots of the important transfer functions and terminal impedances of switching converters. For example, Fig. 8.2 illustrates the magnitude and phase plots of $G_{vd}(s)$ for the buck–boost converter model of Fig. 8.1. Rules for construction of magnitude and phase asymptotes are reviewed in Sect. 8.1, including two types of features that often appear in converter transfer functions: resonances and right half-plane zeroes. Bode diagrams of the small-signal transfer functions of the buck–boost converter are derived in detail in Sect. 8.2, and the transfer functions of the basic buck, boost, and buck–boost converters are tabulated. The physical origins of the right half-plane zero are also described.

A difficulty usually encountered in circuit analysis (step 4 of the above list) is the complexity of the circuit model: practical circuits may contain hundreds of elements, and hence their

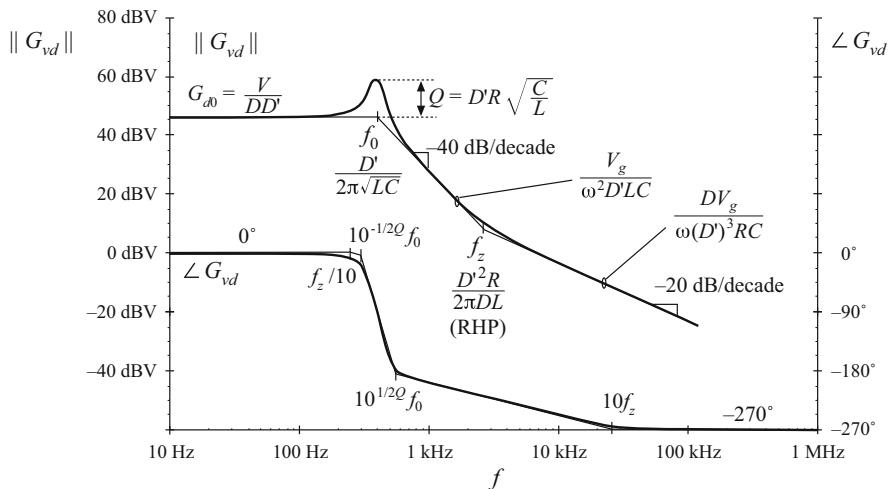


Fig. 8.2 Bode plot of control-to-output transfer function predicted by the model of Fig. 8.1, with analytical expressions for the important features

analysis may lead to complicated derivations, intractable equations, and lots of algebra mistakes. *Design-oriented analysis* [78] is a collection of tools and techniques that can alleviate these problems. Some tools for approaching the design of a complicated converter system are described in this chapter. Writing the transfer functions in normalized form directly exposes the important features of the response. Analytical expressions for these features, as well as for the asymptotes, lead to simple equations that are useful in design. Well-separated roots of transfer function polynomials can be approximated in a simple way. Sect. 8.3 describes a graphical method for constructing Bode plots of transfer functions and impedances, essentially by inspection. This method can: (1) reduce the amount of algebra and associated algebra mistakes; (2) lead to greater insight into circuit behavior, which can be applied to design the circuit; and (3) lead to the insight necessary to make suitable approximations that render the equations tractable. Some more advanced techniques of design-oriented analysis are covered in Part IV.

Experimental measurement of transfer functions and impedances (needed in step 4, model verification) is discussed in Sect. 8.5. Use of computer simulation to plot converter transfer functions (as needed in step 6, worst-case analysis) is covered in Chap. 14.

8.1 Review of Bode Plots

A Bode plot is a plot of the magnitude and phase of a transfer function or other complex-valued quantity, vs. frequency. Magnitude in decibels and phase in degrees are plotted vs. frequency, using semi-logarithmic axes. The magnitude plot is effectively a log–log plot, since the magnitude is expressed in decibels and the frequency axis is logarithmic.

The magnitude of a dimensionless quantity G can be expressed in decibels as follows:

$$\|G\|_{\text{dB}} = 20 \log_{10} (\|G\|) \quad (8.3)$$

Decibel values of some simple magnitudes are listed in Table 8.1. Care must be used when the magnitude is dimensionless. Since it is not proper to take the logarithm of a quantity having dimensions, the magnitude must first be normalized. For example, to express the magnitude of an impedance Z in decibels, we should normalize by dividing by a base impedance R_{base} :

$$\|Z\|_{\text{dB}} = 20 \log_{10} \left(\frac{\|Z\|}{R_{\text{base}}} \right) \quad (8.4)$$

The value of R_{base} is arbitrary, but we need to tell others what value we have used. So if $\|Z\|$ is 5Ω , and we choose $R_{\text{base}} = 10 \Omega$, then we can say that $\|Z\|_{\text{dB}} = 20 \log_{10}(5 \Omega / 10 \Omega) = -6 \text{ dB}$ with respect to 10Ω . A common choice is $R_{\text{base}} = 1 \Omega$; decibel impedances expressed with $R_{\text{base}} = 1 \Omega$ are said to be expressed in $\text{dB}\Omega$. So 5Ω is equivalent to $14 \text{ dB}\Omega$. Current switching harmonics at the input port of a converter are often expressed in $\text{dB}\mu\text{A}$, or dB using a base current of $1 \mu\text{A}$: $60 \text{ dB}\mu\text{A}$ is equivalent to $1000 \mu\text{A}$, or 1 mA .

The magnitude Bode plots of functions equal to powers of f are linear. For example, suppose that the magnitude of a dimensionless quantity $G(f)$ is

$$\|G\| = \left(\frac{f}{f_0} \right)^n \quad (8.5)$$

where f_0 and n are constants. The magnitude in decibels is

$$\|G\|_{\text{dB}} = 20 \log_{10} \left(\frac{f}{f_0} \right)^n = 20n \log_{10} \left(\frac{f}{f_0} \right) \quad (8.6)$$

This equation is plotted in Fig. 8.3, for several values of n . The magnitudes have value $1 \Rightarrow 0 \text{ dB}$ at frequency $f = f_0$. They are linear functions of $\log_{10}(f)$. The slope is the change in $\|G\|_{\text{dB}}$ arising from a unit change in $\log_{10}(f)$; a unit increase in $\log_{10}(f)$ corresponds to a factor of 10, or a decade, increase in f . From Eq. (8.6), a decade increase in f leads to an increase in $\|G\|_{\text{dB}}$ of $20n \text{ dB}$. Hence, the slope is $20n \text{ dB}$ per decade. Equivalently, we can say that the slope is $20n \log_{10}(2) \approx 6n \text{ dB}$ per octave, where an octave is a factor of 2 change in frequency. In practice, the magnitudes of most frequency-dependent functions can usually be approximated over a limited range of frequencies by functions of the form (8.5); over this range of frequencies, the magnitude Bode plot is approximately linear with slope $20n \text{ dB}/\text{decade}$.

A simple transfer function whose magnitude is of the form (8.5) is the *pole at the origin*:

$$G(s) = \frac{1}{\left(\frac{s}{\omega_0} \right)} \quad (8.7)$$

Table 8.1 Expressing magnitudes in decibels

Actual magnitude	Magnitude in dB
$1/2$	-6 dB
1	0 dB
2	6 dB
$5 = 10/2$	$20 \text{ dB} - 6 \text{ dB} = 14 \text{ dB}$
10	20 dB
$1000 = 10^3$	$3 \cdot 20 \text{ dB} = 60 \text{ dB}$

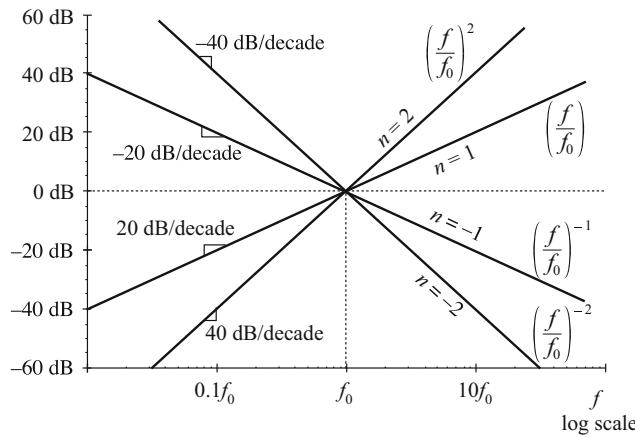


Fig. 8.3 Magnitude Bode plots of functions which vary as f^n are linear, with slope n dB per decade

The magnitude is

$$\|G(j\omega)\| = \frac{1}{\left\| \frac{j\omega}{\omega_0} \right\|} = \frac{1}{\left(\frac{\omega}{\omega_0} \right)} \quad (8.8)$$

If we define $f = \omega/2\pi$ and $f_0 = \omega_0/2\pi$, then Eq. (8.8) becomes

$$\|G\| = \left(\frac{f}{f_0} \right)^{-1} \quad (8.9)$$

which is of the form of Eq. (8.5) with $n = -1$. As illustrated in Fig. 8.3, the magnitude Bode plot of the pole at the origin (8.7) has a -20 dB per decade slope, and passes through 0 dB at frequency $f = f_0$.

8.1.1 Single-Pole Response

Consider the simple R - C low-pass filter illustrated in Fig. 8.4. The transfer function is given by the voltage divider ratio

$$G(s) = \frac{v_2(s)}{v_1(s)} = \frac{\frac{1}{sC}}{\frac{1}{sC} + R} \quad (8.10)$$

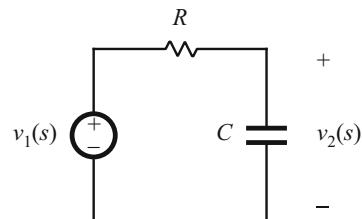


Fig. 8.4 Simple R - C low-pass filter example

This transfer function is a ratio of voltages, and hence is dimensionless. By multiplying the numerator and denominator by sC , we can express the transfer function as a rational fraction:

$$G(s) = \frac{1}{1 + sRC} \quad (8.11)$$

The transfer function now coincides with the following standard normalized form for a single pole:

$$G(s) = \frac{1}{\left(1 + \frac{s}{\omega_0}\right)} \quad (8.12)$$

The parameter $\omega_0 = 2\pi f_0$ is found by equating the coefficients of s in the denominators of Eqs. (8.11) and (8.12). The result is

$$\omega_0 = \frac{1}{RC} \quad (8.13)$$

Since R and C are real positive quantities, ω_0 is also real and positive. The denominator of Eq. (8.12) contains a root at $s = -\omega_0$, and hence $G(s)$ contains a real pole in the left half of the complex plane.

To find the magnitude and phase of the transfer function, we let $s = j\omega$, where j is the square root of -1 . We then find the magnitude and phase of the resulting complex-valued function. With $s = j\omega$, Eq. (8.12) becomes

$$G(j\omega) = \frac{1}{\left(1 + j\frac{\omega}{\omega_0}\right)} = \frac{1 - j\frac{\omega}{\omega_0}}{1 + \left(\frac{\omega}{\omega_0}\right)^2} \quad (8.14)$$

The complex-valued $G(j\omega)$ is illustrated in Fig. 8.5, for one value of ω . The magnitude is

$$\begin{aligned} \|G(j\omega)\| &= \sqrt{[\text{Re}(G(j\omega))]^2 + [\text{Im}(G(j\omega))]^2} \\ &= \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2}} \end{aligned} \quad (8.15)$$

Here, we have assumed that ω_0 is real. In decibels, the magnitude is

$$\|G(j\omega)\|_{\text{dB}} = -20 \log_{10} \left(\sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2} \right) \text{dB} \quad (8.16)$$

The easy way to sketch the magnitude Bode plot of G is to investigate the asymptotic behavior for large and small frequency.

For small frequency, $\omega \ll \omega_0$ and $f \ll f_0$, it is true that

$$\left(\frac{\omega}{\omega_0}\right) \ll 1 \quad (8.17)$$

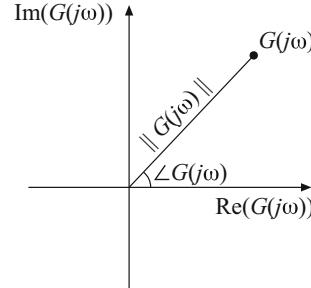


Fig. 8.5 Magnitude and phase of the complex-valued function $G(j\omega)$

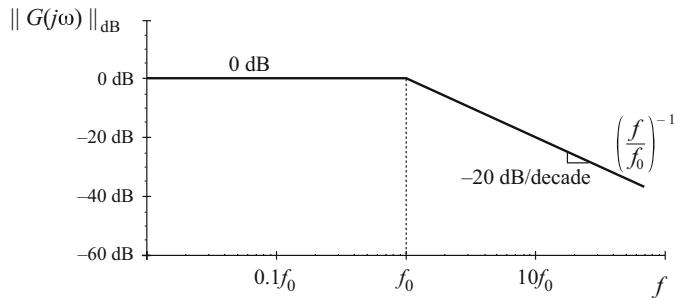


Fig. 8.6 Magnitude asymptotes for the single real pole transfer function

The $(\omega/\omega_0)^2$ term of Eq. (8.15) is therefore much smaller than 1, and hence Eq. (8.15) becomes

$$\|G(j\omega)\| \approx \frac{1}{\sqrt{1}} = 1 \quad (8.18)$$

In decibels, the magnitude is approximately

$$\|G(j\omega)\|_{\text{dB}} \approx 0 \text{ dB} \quad (8.19)$$

Thus, as illustrated in Fig. 8.6, at low frequency $\|G(j\omega)\|_{\text{dB}}$ is asymptotic to 0 dB.

At high frequency, $\omega \gg \omega_0$ and $f \gg f_0$. In this case, it is true that

$$\left(\frac{\omega}{\omega_0}\right) \gg 1 \quad (8.20)$$

We can then say that

$$1 + \left(\frac{\omega}{\omega_0}\right)^2 \approx \left(\frac{\omega}{\omega_0}\right)^2 \quad (8.21)$$

Hence, Eq. (8.15) now becomes

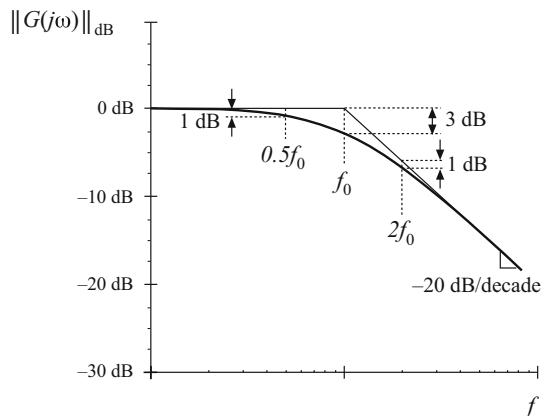
$$\|G(j\omega)\| \approx \frac{1}{\sqrt{\left(\frac{\omega}{\omega_0}\right)^2}} = \left(\frac{f}{f_0}\right)^{-1} \quad (8.22)$$

This expression coincides with Eq. (8.5), with $n = -1$. So at high frequency, $\|G(j\omega)\|_{\text{dB}}$ has slope $-20 \text{ dB per decade}$, as illustrated in Fig. 8.6. Thus, the asymptotes of $\|G(j\omega)\|$ are equal to 1 at low frequency, and $(f/f_0)^{-1}$ at high frequency. The asymptotes intersect at f_0 . The actual magnitude tends toward these asymptotes at very low frequency and very high frequency. In the vicinity of the corner frequency f_0 , the actual curve deviates somewhat from the asymptotes.

The deviation of the exact curve from the asymptotes can be found by simply evaluating Eq. (8.15). At the corner frequency $f = f_0$, Eq. (8.15) becomes

$$\|G(j\omega_0)\| = \frac{1}{1 + \left(\frac{\omega_0}{\omega_0}\right)^2} = \frac{1}{\sqrt{2}} \quad (8.23)$$

Fig. 8.7 Deviation of the actual curve from the asymptotes, real pole



In decibels, the magnitude is

$$\|G(j\omega_0)\|_{\text{dB}} = -20 \log_{10} \left(\sqrt{1 + \left(\frac{\omega_0}{\omega_0} \right)^2} \right) \approx -3 \text{ dB} \quad (8.24)$$

So the actual curve deviates from the asymptotes by -3 dB at the corner frequency, as illustrated in Fig. 8.7. Similar arguments show that the actual curve deviates from the asymptotes by -1 dB at $f = f_0/2$ and at $f = 2f_0$.

The phase of $G(j\omega)$ is

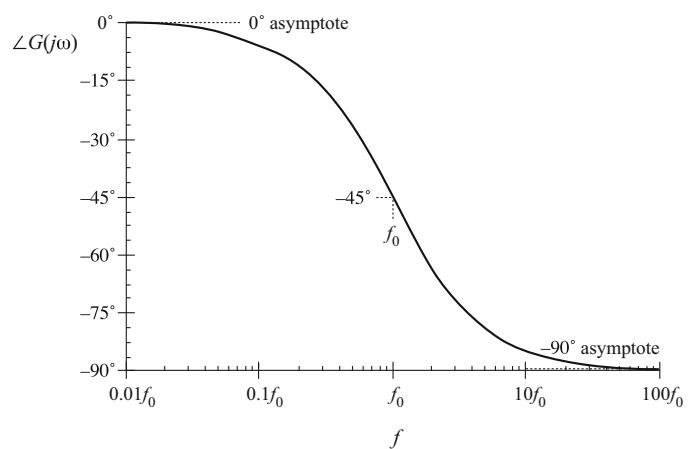
$$\angle G(j\omega) = \tan^{-1} \left(\frac{\text{Im}(G(j\omega))}{\text{Re}(G(j\omega))} \right) \quad (8.25)$$

Insertion of the real and imaginary parts of Eq. (8.14) into Eq. (8.25) leads to

$$\angle G(j\omega) = -\tan^{-1} \left(\frac{\omega}{\omega_0} \right) \quad (8.26)$$

This function is plotted in Fig. 8.8. It tends to 0° at low frequency and to -90° at high frequency. At the corner frequency $f = f_0$, the phase is -45° .

Fig. 8.8 Exact phase plot, real pole



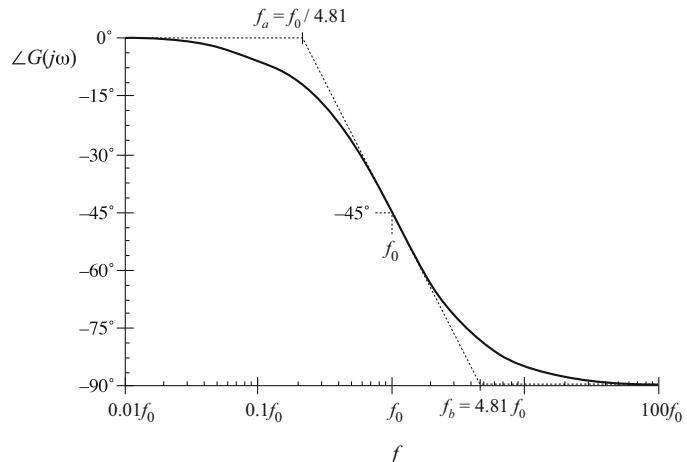


Fig. 8.9 One choice for the mid-frequency phase asymptote, which correctly predicts the actual slope at $f = f_0$

Since the high-frequency and low-frequency phase asymptotes do not intersect, we need a third asymptote to approximate the phase in the vicinity of the corner frequency f_0 . One way to do this is illustrated in Fig. 8.9, where the slope of the asymptote is chosen to be identical to the slope of the actual curve at $f = f_0$. It can be shown that, with this choice, the asymptote intersection frequencies f_a and f_b are given by

$$\begin{aligned} f_a &= f_0 e^{-\pi/2} \approx \frac{f_0}{4.81} \\ f_b &= f_0 e^{\pi/2} \approx 4.81 f_0 \end{aligned} \quad (8.27)$$

A simpler choice, which better approximates the actual curve, is

$$\begin{aligned} f_a &= \frac{f_0}{10} \\ f_b &= 10 f_0 \end{aligned} \quad (8.28)$$

This asymptote is compared to the actual curve in Fig. 8.10. The pole causes the phase to change over a frequency span of approximately two decades, centered at the corner frequency. The slope of the asymptote in this frequency span is -45° per decade. At the break frequencies f_a and f_b , the actual phase deviates from the asymptotes by $\tan^{-1}(0.1) = 5.7^\circ$.

The magnitude and phase asymptotes for the single-pole response are summarized in Fig. 8.11. It is good practice to consistently express single-pole transfer functions in the normalized form of Eq. (8.12). Both terms in the denominator of Eq. (8.12) are dimensionless, and the coefficient of s^0 is unity. Equation (8.12) is easy to interpret, because of its normalized form. At low frequencies, where the (s/ω_0) term is small in magnitude, the transfer function is approximately equal to 1. At high frequencies, where the (s/ω_0) term has magnitude much greater than 1, the transfer function is approximately $(s/\omega_0)^{-1}$. This leads to a magnitude of $(f/f_0)^{-1}$. The corner frequency is $f_0 = \omega_0/2\pi$. So the transfer function is written directly in terms of its salient features, that is, its asymptotes and its corner frequency.

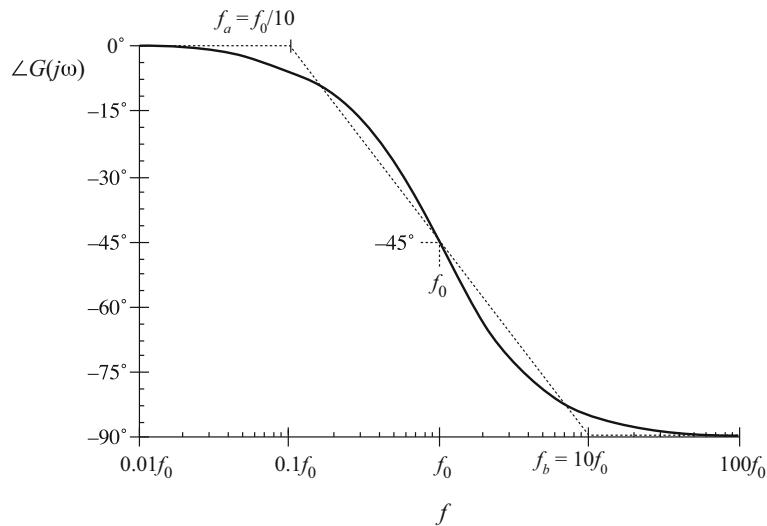


Fig. 8.10 A simpler choice for the mid-frequency phase asymptote, which better approximates the curve over the entire frequency range

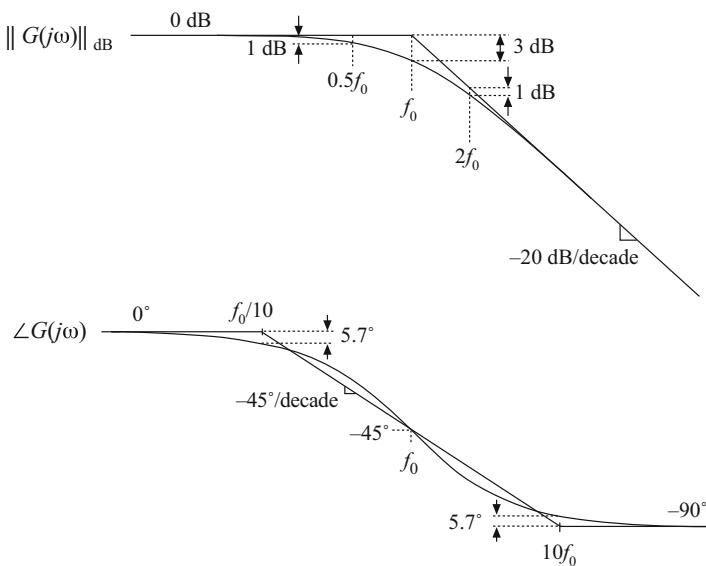


Fig. 8.11 Summary of the magnitude and phase Bode plot for the single real pole

8.1.2 Single Zero Response

A single zero response contains a root in the numerator of the transfer function, and can be written in the following normalized form:

$$G(s) = \left(1 + \frac{s}{\omega_0}\right) \quad (8.29)$$

This transfer function has magnitude

$$\|G(j\omega)\| = \sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2} \quad (8.30)$$

At low frequency, $f \ll f_0 = \omega_0/2\pi$, the transfer function magnitude tends to 1 $\Rightarrow 0$ dB. At high frequency, $f \gg f_0$, the transfer function magnitude tends to (f/f_0) . As illustrated in Fig. 8.12, the high-frequency asymptote has slope +20 dB/decade. The phase is given by

$$\angle G(j\omega) = \tan^{-1}\left(\frac{\omega}{\omega_0}\right) \quad (8.31)$$

With the exception of a minus sign, the phase is identical to Eq. (8.26). Hence, suitable asymptotes are as illustrated in Fig. 8.12. The phase tends to 0° at low frequency and to $+90^\circ$ at high frequency. Over the interval $f_0/10 < f < 10f_0$, the phase asymptote has a slope of $+45^\circ/\text{decade}$.

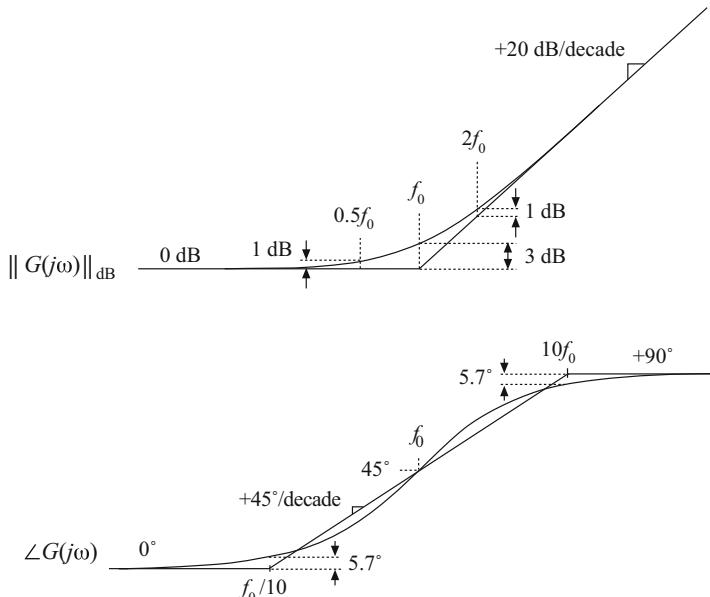


Fig. 8.12 Summary of the magnitude and phase Bode plot for the single real zero

8.1.3 Right Half-Plane Zero

Right half-plane zeroes are often encountered in the small-signal transfer functions of switching converters. These terms have the following normalized form:

$$G(s) = \left(1 - \frac{s}{\omega_0}\right) \quad (8.32)$$

The root of Eq. (8.32) is positive, and hence lies in the right half of the complex s -plane. The right half-plane zero is also sometimes called a nonminimum phase zero. Its normalized form, Eq. (8.32), resembles the normalized form of the (left half-plane) zero of Eq. (8.29), with the exception of a minus sign in the coefficient of s . The minus sign causes a phase reversal at high frequency.

The transfer function has magnitude

$$\|G(j\omega)\| = \sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2} \quad (8.33)$$

This expression is identical to Eq. (8.30). Hence, it is impossible to distinguish a right half-plane zero from a left half-plane zero by the magnitude alone. The phase is given by

$$\angle G(j\omega) = -\tan^{-1}\left(\frac{\omega}{\omega_0}\right) \quad (8.34)$$

This coincides with the expression for the phase of the single pole, Eq. (8.26). So the right half-plane zero exhibits the magnitude response of the left half-plane zero, but the phase response of the pole. Magnitude and phase asymptotes are summarized in Fig. 8.13.

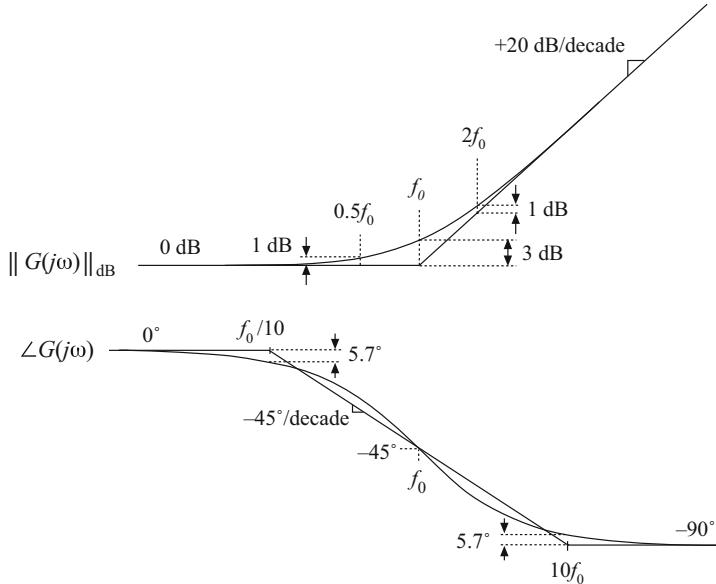


Fig. 8.13 Summary of the magnitude and phase Bode plot for the single real RHP zero

8.1.4 Frequency Inversion

Two other forms arise, from inversion of the frequency axis. The inverted pole has the transfer function

$$G(s) = \frac{1}{\left(1 + \frac{\omega_0}{s}\right)} \quad (8.35)$$

As illustrated in Fig. 8.14, the inverted pole has a high-frequency gain of 1, and a low-frequency asymptote having a +20 dB/decade slope. This form is useful for describing the gain of high-pass filters, and of other transfer functions where it is desired to emphasize the high-frequency gain, with attenuation of low frequencies. Equation (8.35) is equivalent to

$$G(s) = \frac{\left(\frac{s}{\omega_0}\right)}{\left(1 + \frac{s}{\omega_0}\right)} \quad (8.36)$$

However, Eq. (8.35) more directly emphasizes that the high-frequency gain is 1.

The inverted zero has the form

$$G(s) = \left(1 + \frac{\omega_0}{s}\right) \quad (8.37)$$

As illustrated in Fig. 8.15, the inverted zero has a high-frequency gain asymptote equal to 1, and a low-frequency asymptote having a slope equal to -20 dB/decade. An example of the use of

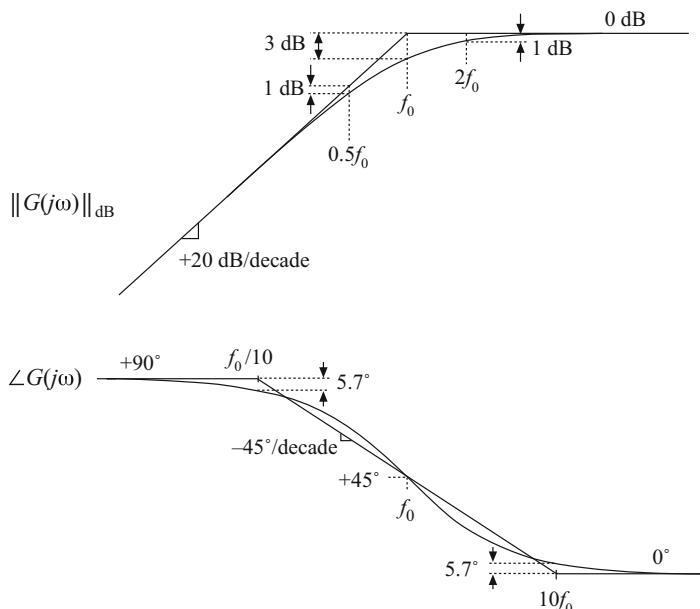


Fig. 8.14 Inversion of the frequency axis: summary of the magnitude and phase Bode plots for the inverted real pole

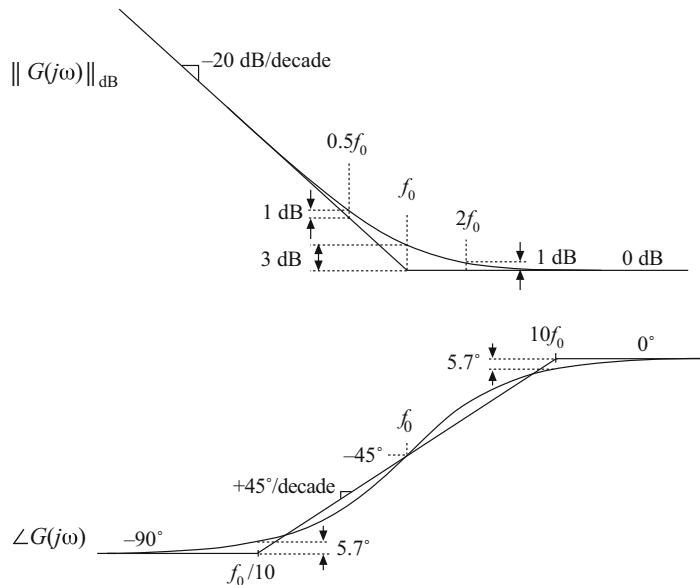


Fig. 8.15 Inversion of the frequency axis: summary of the magnitude and phase Bode plot for the inverted real zero

this type of transfer function is the proportional-plus-integral controller, discussed in connection with feedback loop design in the next chapter. Equation (8.37) is equivalent to

$$G(s) = \frac{\left(1 + \frac{s}{\omega_0}\right)}{\left(\frac{s}{\omega_0}\right)} \quad (8.38)$$

However, Eq. (8.37) is the preferred form when it is desired to emphasize the value of the high-frequency gain asymptote.

The use of frequency inversion is illustrated by example in the next section.

8.1.5 Combinations

The Bode diagram of a transfer function containing several pole, zero, and gain terms can be constructed by simple addition. At any given frequency, the magnitude (in decibels) of the composite transfer function is equal to the sum of the decibel magnitudes of the individual terms. Likewise, at a given frequency the phase of the composite transfer function is equal to the sum of the phases of the individual terms.

For example, suppose that we have already constructed the Bode diagrams of two complex-valued functions of ω , $G_1(\omega)$ and $G_2(\omega)$. These functions have magnitudes $R_1(\omega)$ and $R_2(\omega)$, and phases $\theta_1(\omega)$ and $\theta_2(\omega)$, respectively. It is desired to construct the Bode diagram of the product $G_3(\omega) = G_1(\omega) G_2(\omega)$. Let $G_3(\omega)$ have magnitude $R_3(\omega)$, and phase $\theta_3(\omega)$. To find this magnitude and phase, we can express $G_1(\omega)$, $G_2(\omega)$, and $G_3(\omega)$ in polar form:

$$\begin{aligned} G_1(\omega) &= R_1(\omega)e^{j\theta_1(\omega)} \\ G_2(\omega) &= R_2(\omega)e^{j\theta_2(\omega)} \\ G_3(\omega) &= R_3(\omega)e^{j\theta_3(\omega)} \end{aligned} \quad (8.39)$$

The product $G_3(\omega)$ can then be expressed as

$$G_3(\omega) = G_1(\omega)G_2(\omega) = R_1(\omega)e^{j\theta_1(\omega)}R_2(\omega)e^{j\theta_2(\omega)} \quad (8.40)$$

Simplification leads to

$$G_3(\omega) = (R_1(\omega)R_2(\omega))e^{j(\theta_1(\omega)+\theta_2(\omega))} \quad (8.41)$$

Hence, the composite phase is

$$\theta_3(\omega) = \theta_1(\omega) + \theta_2(\omega) \quad (8.42)$$

The total magnitude is

$$R_3(\omega) = R_1(\omega)R_2(\omega) \quad (8.43)$$

When expressed in decibels, Eq. (8.43) becomes

$$|R_3(\omega)|_{\text{dB}} = |R_1(\omega)|_{\text{dB}} + |R_2(\omega)|_{\text{dB}} \quad (8.44)$$

So the composite phase is the sum of the individual phases, and when expressed in decibels, the composite magnitude is the sum of the individual magnitudes. The composite magnitude slope, in dB per decade, is therefore also the sum of the individual slopes in dB per decade.

For example, consider construction of the Bode plot of the following transfer function:

$$G(s) = \frac{G_0}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)} \quad (8.45)$$

where $G_0 = 40 \Rightarrow 32 \text{ dB}$, $f_1 = \omega_1/2\pi = 100 \text{ Hz}$, $f_2 = \omega_2/2\pi = 2 \text{ kHz}$. This transfer function contains three terms: the gain G_0 , and the poles at frequencies f_1 and f_2 . The asymptotes for each of these terms are illustrated in Fig. 8.16. The gain G_0 is a positive real number, and therefore contributes zero phase shift with the gain 32 dB. The poles at 100 Hz and 2 kHz each contribute asymptotes as in Fig. 8.11.

At frequencies less than 100 Hz, the G_0 term contributes a gain magnitude of 32 dB, while the two poles each contribute magnitude asymptotes of 0 dB. So the low-frequency composite magnitude asymptote is $32 \text{ dB} + 0 \text{ dB} + 0 \text{ dB} = 32 \text{ dB}$. For frequencies between 100 Hz and 2 kHz, the G_0 gain again contributes 32 dB, and the pole at 2 kHz continues to contribute a 0 dB magnitude asymptote. However, the pole at 100 Hz now contributes a magnitude asymptote that decreases with a -20 dB/decade slope. The composite magnitude asymptote therefore also decreases with a -20 dB/decade slope, as illustrated in Fig. 8.16. For frequencies greater than 2 kHz, the poles at 100 Hz and 2 kHz each contribute decreasing asymptotes having slopes of -20 dB/decade . The composite asymptote therefore decreases with a slope of $-20 \text{ dB/decade} - 20 \text{ dB/decade} = -40 \text{ dB/decade}$, as illustrated.

The composite phase asymptote is also constructed in Fig. 8.16. Below 10 Hz, all terms contribute 0° asymptotes. For frequencies between $f_1/10 = 10 \text{ Hz}$ and $f_2/10 = 200 \text{ Hz}$, the pole at f_1 contributes a decreasing phase asymptote having a slope of $-45^\circ/\text{decade}$. Between 200 Hz and $10f_1 = 1 \text{ kHz}$, both poles contribute decreasing asymptotes with $-45^\circ/\text{decade}$ slopes; the

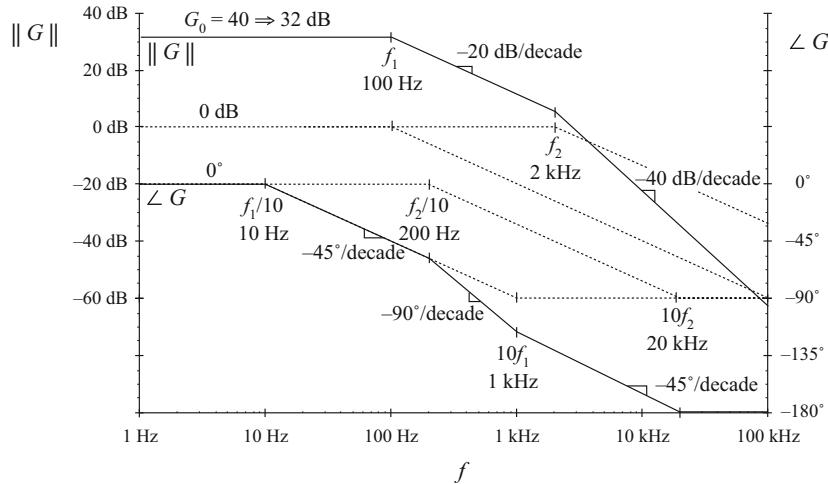


Fig. 8.16 Construction of magnitude and phase asymptotes for the transfer function of Eq. (8.45). Dashed lines: asymptotes for individual terms. Solid lines: composite asymptotes

composite slope is therefore $-90^\circ/\text{decade}$. Between 1kHz and $10f_2 = 20\text{kHz}$, the pole at f_1 contributes a constant -90° phase asymptote, while the pole at f_2 contributes a decreasing asymptote with $-45^\circ/\text{decade}$ slope. The composite slope is then $-45^\circ/\text{decade}$. For frequencies greater than 20kHz , both poles contribute constant -90° asymptotes, leading to a composite phase asymptote of -180° .

As a second example, consider the transfer function $A(s)$ represented by the magnitude and phase asymptotes of Fig. 8.17. Let us write the transfer function that corresponds to these asymptotes. The dc asymptote is A_0 . At corner frequency f_1 , the asymptote slope increases from 0 dB/decade to $+20\text{ dB/decade}$. Hence, there must be a zero at frequency f_1 . At frequency f_2 , the asymptote slope decreases from $+20\text{ dB/decade}$ to 0 dB/decade . Therefore the transfer function contains a pole at frequency f_2 . So we can express the transfer function as

$$A(s) = A_0 \frac{\left(1 + \frac{s}{\omega_1}\right)}{\left(1 + \frac{s}{\omega_2}\right)} \quad (8.46)$$

where ω_1 and ω_2 are equal to $2\pi f_1$ and $2\pi f_2$, respectively.

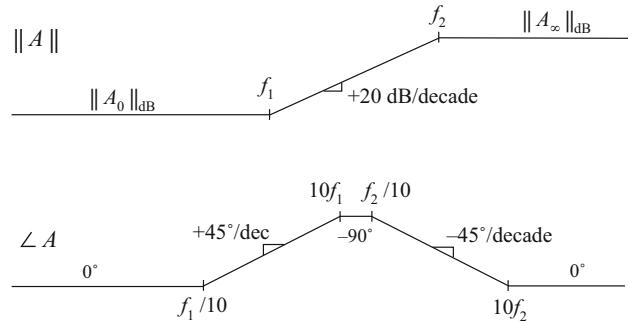


Fig. 8.17 Magnitude and phase asymptotes of example transfer function $A(s)$

We can use Eq. (8.46) to derive analytical expressions for the asymptotes. For $f < f_1$, and letting $s = j\omega$, we can see that the (s/ω_1) and (s/ω_2) terms each have magnitude less than 1. The asymptote is derived by neglecting these terms. Hence, the low-frequency magnitude asymptote is

$$\left\| A_0 \frac{\left(1 + \frac{s}{\omega_1}\right)}{\left(1 + \frac{s}{\omega_2}\right)} \right\|_{s=j\omega} = A_0 \frac{1}{1} = A_0 \quad (8.47)$$

For $f_1 < f < f_2$, the numerator term (s/ω_1) has magnitude greater than 1, while the denominator term (s/ω_2) has magnitude less than 1. The asymptote is derived by neglecting the smaller terms:

$$\left\| A_0 \frac{\left(1 + \frac{s}{\omega_1}\right)}{\left(1 + \frac{s}{\omega_2}\right)} \right\|_{s=j\omega} = A_0 \frac{\left\| \frac{s}{\omega_1} \right\|_{s=j\omega}}{1} = A_0 \frac{\omega}{\omega_1} = A_0 \frac{f}{f_1} \quad (8.48)$$

This is the expression for the mid-frequency magnitude asymptote of $A(s)$. For $f > f_2$, the (s/ω_1) and (s/ω_2) terms each have magnitude greater than 1. The expression for the high-frequency asymptote is therefore:

$$\left\| A_0 \frac{\left(1 + \frac{s}{\omega_1}\right)}{\left(1 + \frac{s}{\omega_2}\right)} \right\|_{s=j\omega} = A_0 \frac{\left\| \frac{s}{\omega_1} \right\|_{s=j\omega}}{\left\| \frac{s}{\omega_2} \right\|_{s=j\omega}} = A_0 \frac{\omega_2}{\omega_1} = A_0 \frac{f_2}{f_1} \quad (8.49)$$

We can conclude that the high-frequency gain is

$$A_\infty = A_0 \frac{f_2}{f_1} \quad (8.50)$$

Thus, we can derive analytical expressions for the asymptotes.

The transfer function $A(s)$ can also be written in a second form, using inverted poles and zeroes. Suppose that $A(s)$ represents the transfer function of a high-frequency amplifier, whose dc gain is not important. We are then interested in expressing $A(s)$ directly in terms of the high-frequency gain A_∞ . We can view the transfer function as having an inverted pole at frequency f_2 , which introduces attenuation at frequencies less than f_2 . In addition, there is an inverted zero at $f = f_1$. So $A(s)$ could also be written as

$$A(s) = A_\infty \frac{\left(1 + \frac{\omega_1}{s}\right)}{\left(1 + \frac{\omega_2}{s}\right)} \quad (8.51)$$

It can be verified that Eqs. (8.51) and (8.46) are equivalent.

8.1.6 Quadratic Pole Response: Resonance

Consider next the transfer function $G(s)$ of the two-pole low-pass filter of Fig. 8.18. The buck converter contains a filter of this type. When manipulated into canonical form, the models of the boost and buck-boost also contain similar filters. One can show that the transfer function of this network is

$$G(s) = \frac{v_2(s)}{v_1(s)} = \frac{1}{1 + s\frac{L}{R} + s^2LC} \quad (8.52)$$

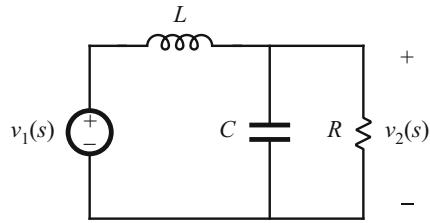


Fig. 8.18 Two-pole low-pass filter example

This transfer function contains a second-order denominator polynomial, and is of the form

$$G(s) = \frac{1}{1 + a_1s + a_2s^2} \quad (8.53)$$

with $a_1 = L/R$ and $a_2 = LC$.

To construct the Bode plot of this transfer function, we might try to factor the denominator into its two roots:

$$G(s) = \frac{1}{\left(1 - \frac{s}{s_1}\right)\left(1 - \frac{s}{s_2}\right)} \quad (8.54)$$

Use of the quadratic formula leads to the following expressions for the roots:

$$s_1 = -\frac{a_1}{2a_2} \left[1 - \sqrt{1 - \frac{4a_2}{a_1^2}} \right] \quad (8.55)$$

$$s_2 = -\frac{a_1}{2a_2} \left[1 + \sqrt{1 - \frac{4a_2}{a_1^2}} \right] \quad (8.56)$$

If $4a_2 \leq a_1^2$, then the roots are real. Each real pole then exhibits a Bode diagram as derived in Sect. 8.1.1, and the composite Bode diagram can be constructed as described in Sect. 8.1.5 (but a better approach is described in Sect. 8.1.7).

If $4a_2 > a_1^2$, then the roots (8.55) and (8.56) are complex. In Sect. 8.1.1, the assumption was made that ω_0 is real; hence, the results of that section cannot be applied to this case. We need to do some additional work, to determine the magnitude and phase for the case when the roots are complex.

The transfer functions of Eqs. (8.52) and (8.53) can be written in the following standard normalized form:

$$G(s) = \frac{1}{1 + 2\zeta\frac{s}{\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \quad (8.57)$$

If the coefficients a_1 and a_2 are real and positive, then the parameters ζ and ω_0 are also real and positive. The parameter ω_0 is again the angular corner frequency, and we can define $f_0 = \omega_0/2\pi$. The parameter ζ is called the *damping factor*: ζ controls the shape of the transfer function in the vicinity of $f = f_0$. An alternative standard normalized form is

$$G(s) = \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \quad (8.58)$$

where

$$Q = \frac{1}{2\zeta} \quad (8.59)$$

The parameter Q is called the *quality factor* of the circuit, and is a measure of the dissipation in the system. A more general definition of Q , for sinusoidal excitation of a passive element or network, is

$$Q = 2\pi \frac{(\text{peak stored energy})}{(\text{energy dissipated per cycle})} \quad (8.60)$$

For a second-order passive system, Eqs. (8.59) and (8.60) are equivalent. We will see that the Q -factor has a very simple interpretation in the magnitude Bode diagrams of second-order transfer functions.

Analytical expressions for the parameters Q and ω_0 can be found by equating like powers of s in the original transfer function, Eq. (8.52), and in the normalized form, Eq. (8.58). The result is

$$\begin{aligned} f_0 &= \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{LC}} \\ Q &= R\sqrt{\frac{C}{L}} \end{aligned} \quad (8.61)$$

The roots s_1 and s_2 of Eqs. (8.55) and (8.56) are real when $Q \leq 0.5$, and are complex when $Q > 0.5$.

The magnitude of G is

$$\|G(j\omega)\| = \frac{1}{\sqrt{\left(1 - \left(\frac{\omega}{\omega_0}\right)^2\right)^2 + \frac{1}{Q^2}\left(\frac{\omega}{\omega_0}\right)^2}} \quad (8.62)$$

Asymptotes of $\|G\|$ are illustrated in Fig. 8.19. At low frequencies, $(\omega/\omega_0) \ll 1$, and hence

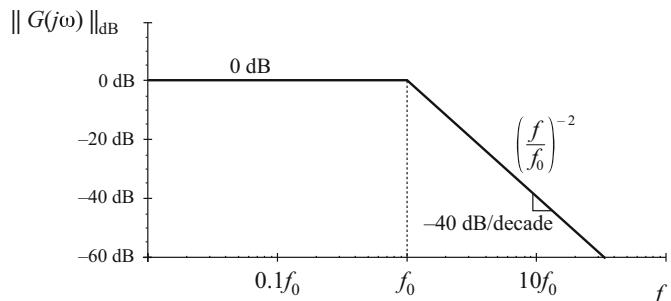


Fig. 8.19 Magnitude asymptotes for the two-pole transfer function

$$\|G\| \rightarrow 1 \quad \text{for } \omega \ll \omega_0 \quad (8.63)$$

At high frequencies where $(\omega/\omega_0) \gg 1$, the $(\omega/\omega_0)^4$ term dominates the expression inside the radical of Eq. (8.62). Hence, the high-frequency asymptote is

$$\|G\| \rightarrow \left(\frac{f}{f_0}\right)^{-2} \quad \text{for } \omega \gg \omega_0 \quad (8.64)$$

This expression coincides with Eq. (8.5), with $n = -2$. Therefore, the high-frequency asymptote has slope -40 dB/decade . The asymptotes intersect at $f = f_0$, and are independent of Q .

The parameter Q affects the deviation of the actual curve from the asymptotes, in the neighborhood of the corner frequency f_0 . The exact magnitude at $f = f_0$ is found by substitution of $\omega = \omega_0$ into Eq. (8.62):

$$\|G(j\omega_0)\| = Q \quad (8.65)$$

So the exact transfer function has magnitude Q at the corner frequency f_0 . In decibels, Eq. (8.65) is

$$\|G(j\omega_0)\|_{\text{dB}} = |Q|_{\text{dB}} \quad (8.66)$$

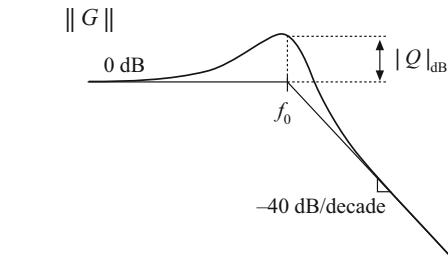


Fig. 8.20 Important features of the magnitude Bode plot, for the two-pole transfer function

So if, for example, $Q = 2 \Rightarrow 6 \text{ dB}$, then the actual curve deviates from the asymptotes by 6 dB at the corner frequency $f = f_0$. Salient features of the magnitude Bode plot of the second-order transfer function are summarized in Fig. 8.20.

The phase of G is

$$\angle G(j\omega) = -\tan^{-1} \left[\frac{\frac{1}{Q} \left(\frac{\omega}{\omega_0} \right)}{1 - \left(\frac{\omega}{\omega_0} \right)^2} \right] \quad (8.67)$$

The phase tends to 0° at low frequency and to -180° at high frequency. At $f = f_0$, the phase is -90° . As illustrated in Fig. 8.21, increasing the value of Q causes a sharper phase change between the 0° and -180° asymptotes. We again need a mid-frequency asymptote, to approximate the phase transition in the vicinity of the corner frequency f_0 , as illustrated in Fig. 8.22. As in the case of the real single pole, we could choose the slope of this asymptote to be identical to the slope of the actual curve at $f = f_0$. It can be shown that this choice leads to the following asymptote break frequencies:

$$\begin{aligned} f_a &= \left(e^{\pi/2}\right)^{-\frac{1}{2Q}} f_0 \\ f_b &= \left(e^{\pi/2}\right)^{\frac{1}{2Q}} f_0 \end{aligned} \quad (8.68)$$

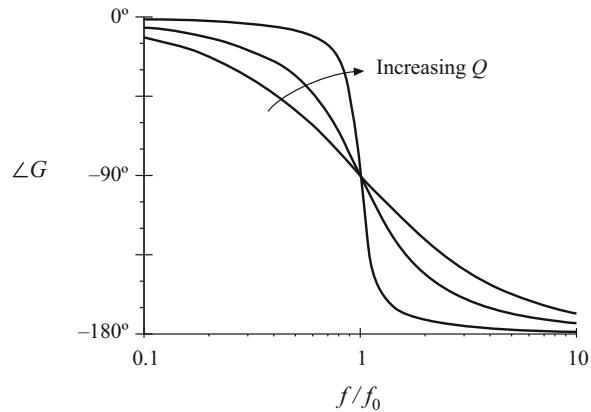


Fig. 8.21 Phase plot, second-order poles. Increasing Q causes a sharper phase change

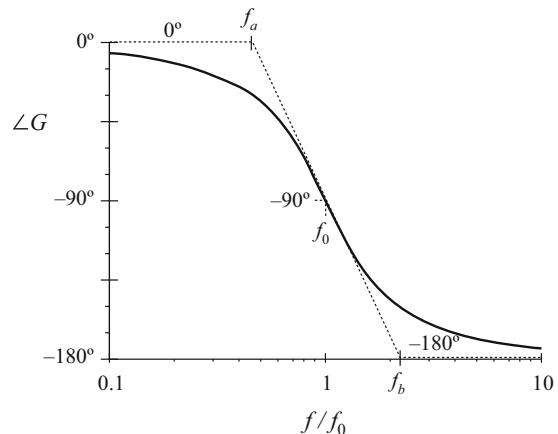


Fig. 8.22 One choice for the mid-frequency phase asymptote of the two-pole response, which correctly predicts the actual slope at $f = f_0$

A better choice, which is consistent with the approximation (8.28) used for the real single pole, is

$$\begin{aligned}f_a &= 10^{-1/2Q} f_0 \\f_b &= 10^{1/2Q} f_0\end{aligned}\quad (8.69)$$

With this choice, the mid-frequency asymptote has slope $-180 Q$ degrees per decade. The phase asymptotes are summarized in Fig. 8.23. With $Q = 0.5$, the phase changes from 0° to -180° over a frequency span of approximately two decades, centered at the corner frequency f_0 . Increasing the Q causes this frequency span to decrease rapidly.

Second-order response magnitude and phase curves are plotted in Figs. 8.24 and 8.25.

Fig. 8.23 A simpler choice for the mid-frequency phase asymptote, which better approximates the curve over the entire frequency range and is consistent with the asymptote used for real poles

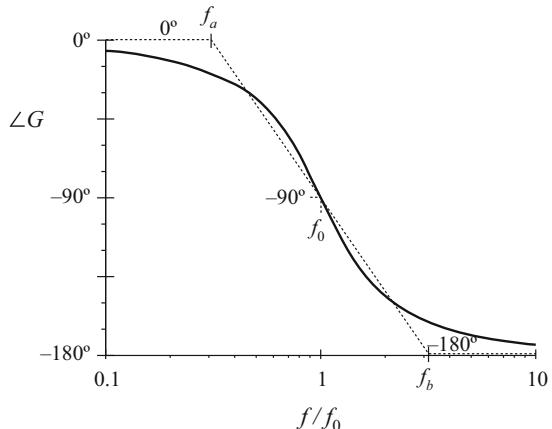
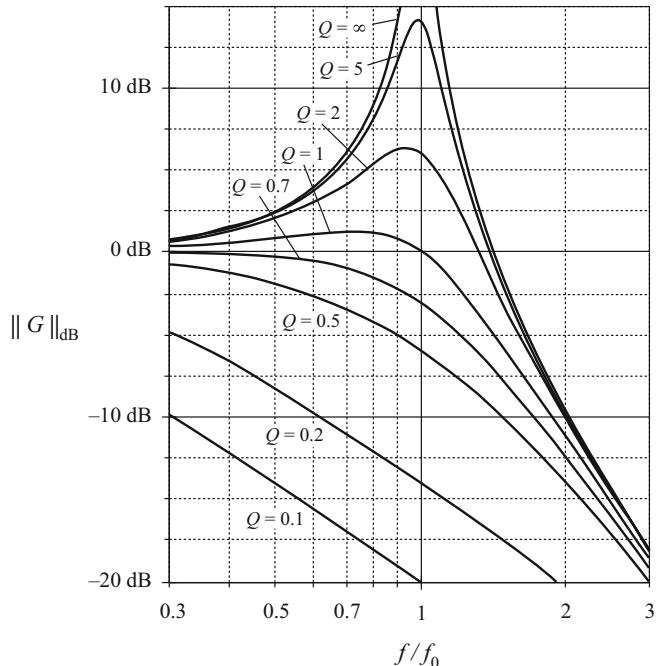


Fig. 8.24 Exact magnitude curves, two-pole response, for several values of Q



8.1.7 The Low- Q Approximation

As mentioned in Sect. 8.1.6, when the roots of second-order denominator polynomial of Eq. (8.53) are real, then we can factor the denominator, and construct the Bode diagram using the asymptotes for real poles. We would then use the following normalized form:

$$G(s) = \frac{1}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)} \quad (8.70)$$

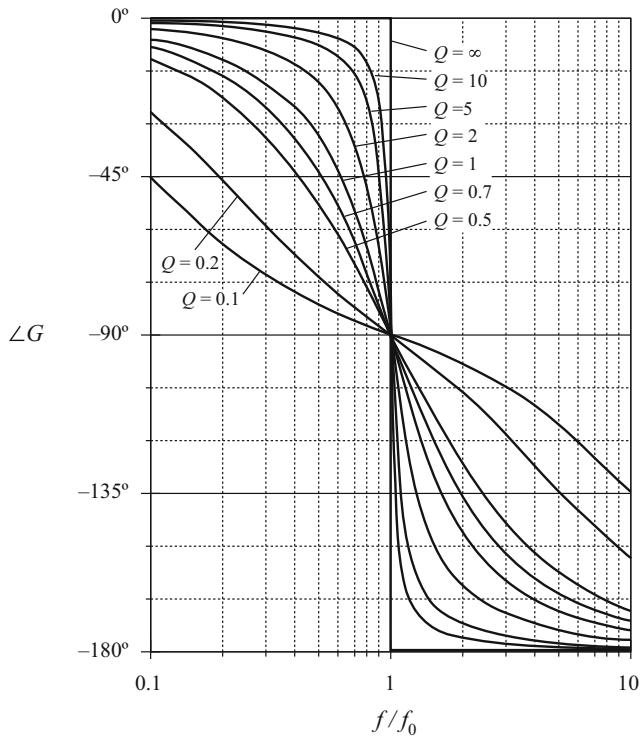


Fig. 8.25 Exact phase curves, two-pole response, for several values of Q

This is a particularly desirable approach when the corner frequencies ω_1 and ω_2 are well separated in value.

The difficulty in this procedure lies in the complexity of the quadratic formula used to find the corner frequencies. Expressing the corner frequencies ω_1 and ω_2 in terms of the circuit elements R , L , C , etc., invariably leads to complicated and unilluminating expressions, especially when the circuit contains many elements. Even in the case of the simple circuit of Fig. 8.18, whose transfer function is given by Eq. (8.52), the conventional quadratic formula leads to the following complicated formula for the corner frequencies:

$$\omega_1, \omega_2 = \frac{\frac{L}{R} \pm \sqrt{\left(\frac{L}{R}\right)^2 - 4LC}}{2LC} \quad (8.71)$$

This equation yields essentially no insight regarding how the corner frequencies depend on the element values. For example, it can be shown that when the corner frequencies are well separated in value, they can be expressed with high accuracy by the much simpler relations

$$\omega_1 \approx \frac{R}{L}, \quad \omega_2 \approx \frac{1}{RC} \quad (8.72)$$

In this case, ω_1 is essentially independent of the value of C , and ω_2 is essentially independent of L , yet Eq. (8.71) apparently predicts that both corner frequencies are dependent on all element values. The simple expressions of Eq. (8.72) are far preferable to Eq. (8.71), and can be easily derived using the low- Q approximation [79].

Let us assume that the transfer function has been expressed in the standard normalized form of Eq. (8.58), reproduced below:

$$G(s) = \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \quad (8.73)$$

For $Q \leq 0.5$, let us use the quadratic formula to write the real roots of the denominator polynomial of Eq. (8.73) as

$$\omega_1 = \frac{\omega_0}{Q} \frac{1 - \sqrt{1 - 4Q^2}}{2} \quad (8.74)$$

$$\omega_2 = \frac{\omega_0}{Q} \frac{1 + \sqrt{1 - 4Q^2}}{2} \quad (8.75)$$

The corner frequency ω_2 can be expressed as

$$\omega_2 = \frac{\omega_0}{Q} F(Q) \quad (8.76)$$

where $F(Q)$ is defined as [79]:

$$F(Q) = \frac{1}{2} \left(1 + \sqrt{1 - 4Q^2} \right) \quad (8.77)$$

Note that, when $Q \ll 0.5$, then $4Q^2 \ll 1$ and $F(Q)$ is approximately equal to 1. We then obtain

$$\omega_2 \approx \frac{\omega_0}{Q} \quad \text{for } Q \ll \frac{1}{2} \quad (8.78)$$

The function $F(Q)$ is plotted in Fig. 8.26. It can be seen that $F(Q)$ approaches 1 very rapidly as Q decreases below 0.5.

To derive a similar approximation for ω_1 , we can multiply and divide Eq. (8.74) by $F(Q)$, Eq. (8.77). Upon simplification of the numerator, we obtain

$$\omega_1 = \frac{Q\omega_0}{F(Q)} \quad (8.79)$$

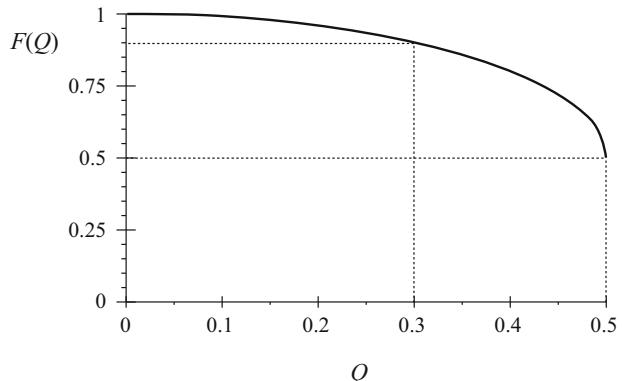


Fig. 8.26 $F(Q)$ vs. Q , as given by Eq. (8.77). The approximation $F(Q) = 1$ is within 10% of the exact value for $Q < 3$

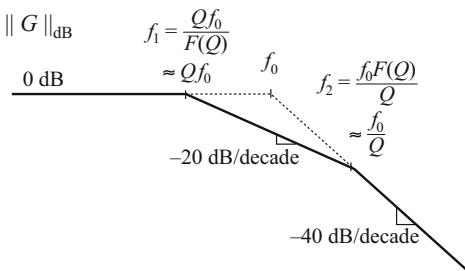


Fig. 8.27 Magnitude asymptotes predicted by the low- Q approximation. Real poles occur at frequencies Qf_0 and f_0/Q

Again, $F(Q)$ tends to 1 for small Q . Hence, ω_1 can be approximated as

$$\omega_1 \approx Q\omega_0 \quad \text{for } Q \ll \frac{1}{2} \quad (8.80)$$

Magnitude asymptotes for the low- Q case are summarized in Fig. 8.27. For $Q < 0.5$, the two poles at ω_0 split into real poles. One real pole occurs at corner frequency $\omega_1 < \omega_0$, while the other occurs at corner frequency $\omega_2 > \omega_0$. The corner frequencies are easily approximated, using Eqs. (8.78) and (8.80).

For the filter circuit of Fig. 8.18, the parameters Q and ω_0 are given by Eq. (8.61). For the case when $Q \ll 0.5$, we can derive the following analytical expressions for the corner frequencies, using Eqs. (8.78) and (8.80):

$$\begin{aligned} \omega_1 &\approx Q\omega_0 = R \sqrt{\frac{C}{L}} \frac{1}{\sqrt{LC}} = \frac{R}{L} \\ \omega_2 &\approx \frac{\omega_0}{Q} = \frac{1}{\sqrt{LC}} \frac{1}{R \sqrt{\frac{C}{L}}} = \frac{1}{RC} \end{aligned} \quad (8.81)$$

So the low- Q approximation allows us to derive simple design-oriented analytical expressions for the corner frequencies.

8.1.8 The High- Q Approximation

Another case of interest is the determination of the Q -factor of a high- Q resonant circuit containing multiple resistive elements. Consider, for example, the resonant $L-C$ circuit illustrated in Fig. 8.28, which contains load resistor R and an additional resistor R_C in series with the capacitor. In the case of large R and small R_C , the circuit approaches an undamped $L-C$ network having resonant frequency

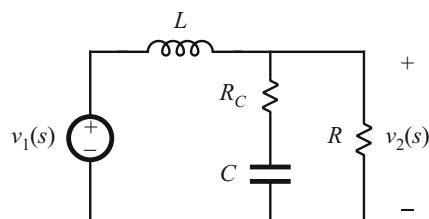


Fig. 8.28 Two-pole low-pass filter with two resistive elements

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (8.82)$$

When R_C is negligibly small but R is significant, then the circuit previously considered in Sect. 8.1.6 (Fig. 8.18) is obtained. We previously found that this circuit exhibits a Q -factor given by

$$Q_{load} = \frac{R}{R_0} \quad (8.83)$$

with

$$R_0 = \sqrt{\frac{L}{C}}$$

leading to the transfer function

$$G(s) = \frac{1}{1 + \frac{s}{Q_{load} \omega_0} + \left(\frac{s}{\omega_0}\right)^2} \quad (8.84)$$

Conversely, in the case where the load resistor R is very large but R_C is significant, we can analyze the circuit to find the following transfer function:

$$G(s) = \frac{\left(1 + \frac{s}{\omega_z}\right)}{1 + \frac{s}{Q_C \omega_0} + \left(\frac{s}{\omega_0}\right)^2} \quad (8.85)$$

The corner frequency ω_0 is again given by Eq. (8.82), but the Q -factor is

$$Q_C = \frac{R_0}{R_C} \quad (8.86)$$

So individually, the two damping cases lead to similar second-order denominators, whose Q factors depend on the individual resistor values.

For the case when R and R_C simultaneously cause significant damping, we can analyze the circuit of Fig. 8.28 to show that the transfer function is

$$G(s) = \frac{1 + sR_C C}{1 + s\left(\frac{L}{R} + R_C C\right) + s^2 LC \left(1 + \frac{R_C}{R}\right)} \quad (8.87)$$

This equation can be expressed in the following normalized form:

$$G(s) = \frac{\left(1 + \frac{s}{\omega_z}\right)}{1 + \left(\frac{s}{\omega_0}\right)\left(\frac{1}{Q_{load}} + \frac{1}{Q_C}\right) + \left(\frac{s}{\omega_0}\right)^2 \left(1 + \frac{1}{Q_{load} Q_C}\right)} \quad (8.88)$$

where

$$\begin{aligned}\omega_0 &= \frac{1}{\sqrt{LC}} \\ Q_{load} &= \frac{R}{R_0} \\ Q_C &= \frac{R_0}{R_C} \\ R_0 &= \sqrt{\frac{L}{C}}\end{aligned}\tag{8.89}$$

If $Q_{load} \gg 1$ and $Q_C \gg 1$, then

$$1 + \frac{1}{Q_{load} Q_C} \approx 1\tag{8.90}$$

Equation (8.88) can then be simplified as follows:

$$G(s) \approx \frac{\left(1 + \frac{s}{\omega_z}\right)}{1 + \left(\frac{s}{\omega_0}\right)\left(\frac{1}{Q_{load} \| Q_C}\right) + \left(\frac{s}{\omega_0}\right)^2}\tag{8.91}$$

Thus, for the case when R and R_C simultaneously cause significant damping, the composite Q -factor can be estimated from Q_{load} and Q_C by use of the *High-Q Approximation*:

$$Q \approx Q_{load} \| Q_C = \frac{1}{\frac{1}{Q_{load}} + \frac{1}{Q_C}}\tag{8.92}$$

The notation $x \| y$ denotes inverse addition as shown above. This approximation for the Q -factor of the denominator poles is accurate provided that

$$Q_{load} \gg 1 \quad \text{and} \quad Q_C \gg 1\tag{8.93}$$

The two damping terms Q_{load} and Q_C affect both the exact frequency and the exact Q -factor. We can express Eq. (8.88) in the following standard normalized form:

$$G(s) = \frac{\left(1 + \frac{s}{\omega_z}\right)}{1 + \left(\frac{s}{\omega_e}\right)\left(\frac{1}{Q_e}\right) + \left(\frac{s}{\omega_e}\right)^2}\tag{8.94}$$

where the exact corner frequency ω_e and exact Q -factor Q_e are given by

$$\omega_e = \frac{\omega_0}{F_H(Q_{load} Q_C)}, \quad Q_e = (Q_{load} \| Q_C) F_H(Q_{load} Q_C)\tag{8.95}$$

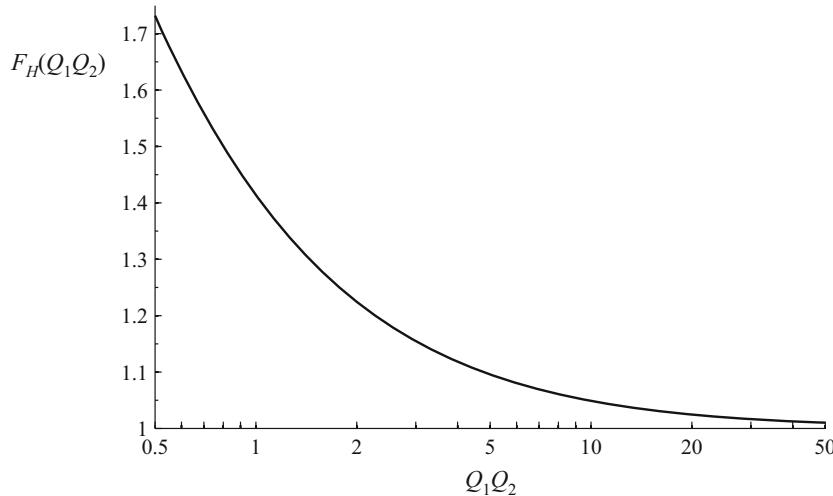


Fig. 8.29 $F_H(Q_1 Q_2)$ vs. $Q_1 Q_2$, as given by Eq. (8.96). The approximation $F_H(Q_1 Q_2) \approx 1$ is within 10% of the correct value for $Q_1 Q_2 > 5$

and with

$$F_H(Q_1 Q_2) = \sqrt{1 + \frac{1}{Q_1 Q_2}} \quad (8.96)$$

The factor $F_H(Q_1 Q_2)$ is plotted in Fig. 8.29. It can be seen that this factor converges to 1 as the product of the two Q factors is increased above 1.

In summary, the high- Q approximation states that in a resonant circuit damped by two elements that individually induce Q -factors of Q_1 and Q_2 , the composite Q -factor is approximately $Q_1 \parallel Q_2$. This approximation facilitates derivation of simple design-oriented expressions for resonant circuits having multiple damping elements. An example of its use is given in Sect. 9.5.4, where the high- Q approximation substantially simplifies the equations of a buck converter in which inductor and capacitor resistances are modeled.

8.1.9 Approximate Roots of an Arbitrary-Degree Polynomial

The low- Q approximation can be generalized, to find approximate analytical expressions for the roots of the n th-order polynomial

$$P(s) = 1 + a_1 s + a_2 s^2 + \cdots + a_n s^n \quad (8.97)$$

It is desired to factor the polynomial $P(s)$ into the form

$$P(s) = (1 + \tau_1 s)(1 + \tau_2 s) \cdots (1 + \tau_n s) \quad (8.98)$$

In a real circuit, the coefficients a_1, \dots, a_n are real, while the time constants τ_1, \dots, τ_n may be either real or complex. Very often, some or all of the time constants are well separated in value, and depend in a very simple way on the circuit element values. In such cases, simple approximate analytical expressions for the time constants can be derived.

The time constants τ_1, \dots, τ_n can be related to the original coefficients a_1, \dots, a_n by multiplying out Eq. (8.98). The result is

$$\begin{aligned} a_1 &= \tau_1 + \tau_2 + \dots + \tau_n \\ a_2 &= \tau_1(\tau_2 + \dots + \tau_n) + \tau_2(\tau_3 + \dots + \tau_n) + \dots \\ a_3 &= \tau_1\tau_2(\tau_3 + \dots + \tau_n) + \tau_2\tau_3(\tau_4 + \dots + \tau_n) + \dots \\ &\vdots \\ a_n &= \tau_1\tau_2\tau_3 \cdots \tau_n \end{aligned} \quad (8.99)$$

General solution of this system of equations amounts to exact factoring of the arbitrary-degree polynomial, a hopeless task. Nonetheless, Eq. (8.99) does suggest a way to approximate the roots.

Suppose that all of the time constants τ_1, \dots, τ_n are real and well separated in value. We can further assume, without loss of generality, that the time constants are arranged in decreasing order of magnitude:

$$|\tau_1| \gg |\tau_2| \gg \dots \gg |\tau_n| \quad (8.100)$$

When the inequalities of Eq. (8.100) are satisfied, then the expressions for a_1, \dots, a_n of Eq. (8.99) are each dominated by their first terms:

$$\begin{aligned} a_1 &\approx \tau_1 \\ a_2 &\approx \tau_1\tau_2 \\ a_3 &\approx \tau_1\tau_2\tau_3 \\ &\vdots \\ a_n &= \tau_1\tau_2\tau_3 \cdots \tau_n \end{aligned} \quad (8.101)$$

These expressions can now be solved for the time constants, with the result

$$\begin{aligned} \tau_1 &\approx a_1 \\ \tau_2 &\approx \frac{a_2}{a_1} \\ \tau_3 &\approx \frac{a_3}{a_2} \\ &\vdots \\ \tau_n &\approx \frac{a_1}{a_{n-1}} \end{aligned} \quad (8.102)$$

Hence, if

$$|a_1| \gg \left| \frac{a_2}{a_1} \right| \gg \left| \frac{a_3}{a_2} \right| \gg \dots \gg \left| \frac{a_n}{a_{n-1}} \right| \quad (8.103)$$

then the polynomial $P(s)$ given by Eq. (8.97) has the approximate factorization

$$P(s) \approx (1 + a_1 s) \left(1 + \frac{a_2}{a_1} s\right) \left(1 + \frac{a_3}{a_2} s\right) \cdots \left(1 + \frac{a_n}{a_{n-1}} s\right) \quad (8.104)$$

Note that if the original coefficients in Eq. (8.97) are simple functions of the circuit elements, then the approximate roots given by Eq. (8.104) are similar simple functions of the circuit elements. So approximate analytical expressions for the roots can be obtained. Numerical values are substituted into Eq. (8.103) to justify the approximation.

In the case where two of the roots are not well separated, then one of the inequalities of Eq. (8.103) is violated. We can then leave the corresponding terms in quadratic form. For example, suppose that inequality k is not satisfied:

$$|a_1| \gg \left|\frac{a_2}{a_1}\right| \gg \cdots \gg \left|\frac{a_k}{a_{k-1}}\right| \not\gg \left|\frac{a_{k+1}}{a_k}\right| \gg \cdots \gg \left|\frac{a_n}{a_{n-1}}\right| \quad (8.105)$$

Then an approximate factorization is

$$P(s) \approx (1 + a_1 s) \left(1 + \frac{a_2}{a_1} s\right) \cdots \left(1 + \frac{a_k}{a_{k-1}} s + \frac{a_{k+1}}{a_{k-1}} s^2\right) \cdots \left(1 + \frac{a_n}{a_{n-1}} s\right) \quad (8.106)$$

The conditions for accuracy of this approximation are

$$|a_1| \gg \left|\frac{a_2}{a_1}\right| \gg \cdots \gg \left|\frac{a_k}{a_{k-1}}\right| \gg \left|\frac{a_{k-2} a_{k+1}}{a_{k-1}^2}\right| \gg \left|\frac{a_{k+2}}{a_{k+1}}\right| \gg \cdots \gg \left|\frac{a_n}{a_{n-1}}\right| \quad (8.107)$$

Complex conjugate roots can be approximated in this manner.

When the first inequality of Eq. (8.103) is violated, that is,

$$|a_1| \not\gg \left|\frac{a_2}{a_1}\right| \gg \left|\frac{a_3}{a_2}\right| \gg \cdots \gg \left|\frac{a_n}{a_{n-1}}\right| \quad (8.108)$$

then the first two roots should be left in quadratic form:

$$P(s) \approx \left(1 + a_1 s + a_2 s^2\right) \left(1 + \frac{a_3}{a_2} s\right) \cdots \left(1 + \frac{a_n}{a_{n-1}} s\right) \quad (8.109)$$

This approximation is justified provided that

$$\left|\frac{a_2^2}{a_3}\right| \gg |a_1| \gg \left|\frac{a_3}{a_2}\right| \gg \left|\frac{a_4}{a_3}\right| \gg \cdots \gg \left|\frac{a_n}{a_{n-1}}\right| \quad (8.110)$$

If none of the above approximations is justified, then there are three or more roots that are close in magnitude. One must then resort to cubic or higher-order forms.

As an example, consider the damped EMI filter illustrated in Fig. 8.30. Filters such as this are typically placed at the power input of a converter, to attenuate the switching harmonics present in the converter input current. By circuit analysis, one can show that this filter exhibits the following transfer function:

$$G(s) = \frac{i_g(s)}{i_c(s)} = \frac{1 + s \frac{L_1 + L_2}{R}}{1 + s \frac{L_1 + L_2}{R} + s^2 L_1 C + s^3 \frac{L_1 L_2 C}{R}} \quad (8.111)$$

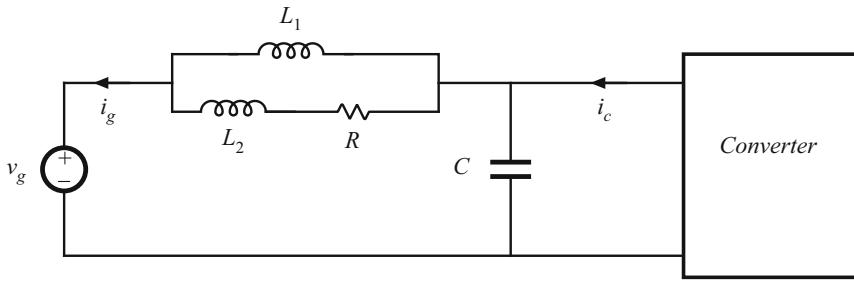


Fig. 8.30 Input EMI filter example

This transfer function contains a third-order denominator, with the following coefficients:

$$\begin{aligned} a_1 &= \frac{L_1 + L_2}{R} \\ a_2 &= L_1 C \\ a_3 &= \frac{L_1 L_2 C}{R} \end{aligned} \quad (8.112)$$

It is desired to factor the denominator, to obtain analytical expressions for the poles. The correct way to do this depends on the numerical values of R , L_1 , L_2 , and C . When the roots are real and well separated, then Eq. (8.104) predicts that the denominator can be factored as follows:

$$\left(1 + s \frac{L_1 + L_2}{R}\right) \left(1 + sRC \frac{L_1}{L_1 + L_2}\right) \left(1 + s \frac{L_2}{R}\right) \quad (8.113)$$

According to Eq. (8.103), this approximation is justified provided that

$$\frac{L_1 + L_2}{R} \gg RC \frac{L_1}{L_1 + L_2} \gg \frac{L_2}{R} \quad (8.114)$$

These inequalities cannot be satisfied unless $L_1 \gg L_2$. When $L_1 \gg L_2$, then Eq. (8.114) can be further simplified to

$$\frac{L_1}{R} \gg RC \gg \frac{L_2}{R} \quad (8.115)$$

The approximate factorization, Eq. (8.113), can then be further simplified to

$$\left(1 + s \frac{L_1}{R}\right) \left(1 + sRC\right) \left(1 + s \frac{L_2}{R}\right) \quad (8.116)$$

Thus, in this case the transfer function contains three well-separated real poles. Equations (8.113) and (8.116) represent approximate analytical factorizations of the denominator of Eq. (8.111). Although numerical values must be substituted into Eqs. (8.114) or (8.115) to justify the approximation, we can nonetheless express Eqs. (8.113) and (8.116) as analytical functions of L_1 , L_2 , R , and C . Equations (8.113) and (8.116) are design-oriented, because they yield insight into how the element values can be chosen such that given specified pole frequencies are obtained.

When the second inequality of Eq. (8.114) is violated,

$$\frac{L_1 + L_2}{R} \gg RC \frac{L_1}{L_1 + L_2} \not\gg \frac{L_2}{R} \quad (8.117)$$

then the second and third roots should be left in quadratic form:

$$\left(1 + s \frac{L_1 + L_2}{R}\right) \left(1 + sRC \frac{L_1}{L_1 + L_2} + s^2 L_1 \| L_2 C\right) \quad (8.118)$$

This expression follows from Eq. (8.106), with $k = 2$. Equation (8.107) predicts that this approximation is justified provided that

$$\frac{L_1 + L_2}{R} \gg RC \frac{L_1}{L_1 + L_2} \gg \frac{L_1 \| L_2}{L_1 + L_2} RC \quad (8.119)$$

In application of Eq. (8.107), we take a_0 to be equal to 1. The inequalities of Eq. (8.119) can be simplified to obtain

$$L_1 \gg L_2, \quad \text{and} \quad \frac{L_1}{R} \gg RC \quad (8.120)$$

Note that it is no longer required that $RC \gg L_2/R$. Equation (8.120) implies that factorization (8.118) can be further simplified to

$$\left(1 + s \frac{L_1}{R}\right) \left(1 + sRC + s^2 L_2 C\right) \quad (8.121)$$

Thus, for this case, the transfer function contains a low-frequency pole that is well separated from a high-frequency quadratic pole pair. Again, the factored result (8.121) is expressed as an analytical function of the element values, and consequently is design-oriented.

In the case where the first inequality of Eq. (8.114) is violated:

$$\frac{L_1 + L_2}{R} \not\gg RC \frac{L_1}{L_1 + L_2} \gg \frac{L_2}{R} \quad (8.122)$$

then the first and second roots should be left in quadratic form:

$$\left(1 + s \frac{L_1 + L_2}{R} + s^2 L_1 C\right) \left(1 + s \frac{L_2}{R}\right) \quad (8.123)$$

This expression follows directly from Eq. (8.109). Equation (8.110) predicts that this approximation is justified provided that

$$\frac{L_1 RC}{L_2} \gg \frac{L_1 + L_2}{R} \gg \frac{L_2}{R} \quad (8.124)$$

that is,

$$L_1 \gg L_2, \quad \text{and} \quad RC \gg \frac{L_2}{R} \quad (8.125)$$

For this case, the transfer function contains a low-frequency quadratic pole pair that is well separated from a high-frequency real pole. If none of the above approximations are justified, then all three of the roots are similar in magnitude. We must then find other means of dealing with the original cubic polynomial. Design of input filters, including the filter of Fig. 8.30, is covered in Chap. 17.

8.2 Analysis of Converter Transfer Functions

Let us next derive analytical expressions for the poles, zeroes, and asymptote gains in the transfer functions of the basic converters.

8.2.1 Example: Transfer Functions of the Buck–Boost Converter

The small-signal equivalent circuit model of the buck–boost converter is derived in Sect. 7.2, with the result (Fig. 7.16b) repeated in Fig. 8.31. Let us derive and plot the control-to-output and line-to-output transfer functions for this circuit.

The converter contains two independent ac inputs: the control input $\hat{d}(s)$ and the line input $\hat{v}_g(s)$. The ac output voltage variations $\hat{v}(s)$ can be expressed as the superposition of terms arising from these two inputs:

$$\hat{v}(s) = G_{vd}(s)\hat{d}(s) + G_{vg}(s)\hat{v}_g(s) \quad (8.126)$$

Hence, the transfer functions $G_{vd}(s)$ and $G_{vg}(s)$ can be defined as

$$G_{vd}(s) = \left. \frac{\hat{v}(s)}{\hat{d}(s)} \right|_{\hat{v}_g(s)=0} \quad \text{and} \quad G_{vg}(s) = \left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\hat{d}(s)=0} \quad (8.127)$$

To find the line-to-output transfer function $G_{vg}(s)$, we set the \hat{d} sources to zero as in Fig. 8.32a. We can then push the $v_g(s)$ source and the inductor through the transformers, to obtain the circuit of Fig. 8.32b. The transfer function $G_{vg}(s)$ is found using the voltage divider formula:

$$G_{vg}(s) = \left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\hat{d}(s)=0} = -\frac{D}{D'} \frac{\left(R \parallel \frac{1}{sC} \right)}{\frac{sL}{D'^2} + \left(R \parallel \frac{1}{sC} \right)} \quad (8.128)$$

We next expand the parallel combination, and express as a rational fraction:

$$\begin{aligned} G_{vg}(s) &= \left(-\frac{D}{D'} \right) \frac{\left(\frac{R}{1+sRC} \right)}{\frac{sL}{D'^2} + \left(\frac{R}{1+sRC} \right)} \\ &= \left(-\frac{D}{D'} \right) \frac{R}{R + \frac{sL}{D'^2} + \frac{s^2RLC}{D'^2}} \end{aligned} \quad (8.129)$$

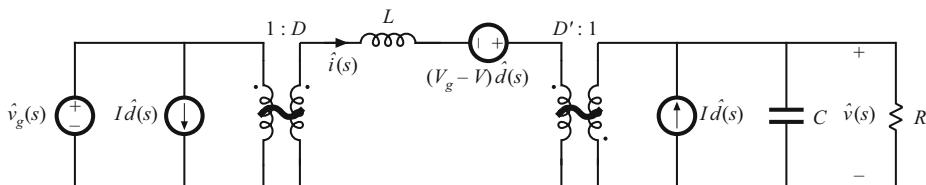


Fig. 8.31 Buck–boost converter equivalent circuit derived in Sect. 7.2

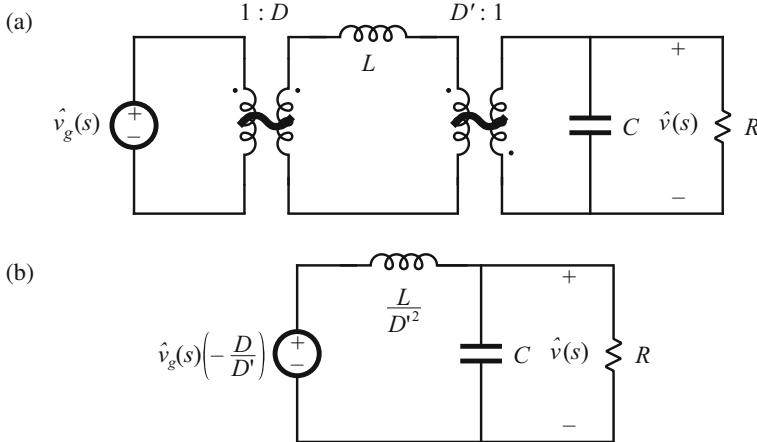


Fig. 8.32 Manipulation of buck-boost equivalent circuit to find the line-to-output transfer function $G_{vg}(s)$: (a) set \hat{d} sources to zero; (b) push inductor and \hat{v}_g source through transformers

We are not done yet—the next step is to manipulate the expression into normalized form, such that the coefficients of s^0 in the numerator and denominator polynomials are equal to one. This can be accomplished by dividing the numerator and denominator by R :

$$G_{vg}(s) = \left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\hat{d}(s)=0} = \left(-\frac{D}{D'} \right) \frac{1}{1 + s \frac{L}{D'^2 R} + s^2 \frac{LC}{D'^2}} \quad (8.130)$$

Thus, the line-to-output transfer function contains a dc gain G_{g0} and a quadratic pole pair:

$$G_{vg}(s) = G_{g0} \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0} \right)^2} \quad (8.131)$$

Analytical expressions for the salient features of the line-to-output transfer function are found by equating like terms in Eqs. (8.130) and (8.131). The dc gain is

$$G_{g0} = -\frac{D}{D'} \quad (8.132)$$

By equating the coefficients of s^2 in the denominators of Eqs. (8.130) and (8.131), we obtain

$$\frac{1}{\omega_0^2} = \frac{LC}{D'^2} \quad (8.133)$$

Hence, the angular corner frequency is

$$\omega_0 = \frac{D'}{\sqrt{LC}} \quad (8.134)$$

By equating coefficients of s in the denominators of Eqs. (8.130) and (8.131), we obtain

$$\frac{1}{Q\omega_0} = \frac{L}{D'^2 R} \quad (8.135)$$

Elimination of ω_0 using Eq. (8.134) and solution for Q leads to

$$Q = D'R \sqrt{\frac{C}{L}} \quad (8.136)$$

Equations (8.132), (8.134), and (8.136) are the desired results in the analysis of the line-to-output transfer function. These expressions are useful not only in analysis situations, where it is desired to find numerical values of the salient features G_{go} , ω_0 , and Q , but also in design situations, where it is desired to select numerical values for R , L , and C such that given values of the salient features are obtained.

Derivation of the control-to-output transfer function $G_{vd}(s)$ is complicated by the presence in Fig. 8.31 of three generators that depend on $\hat{d}(s)$. One good way to find $G_{vd}(s)$ is to manipulate the circuit model as in the derivation of the canonical model, Fig. 7.36. Another approach, used here, employs the principle of superposition. First, we set the \hat{v}_g source to zero. This shorts the input to the $1:D$ transformer, and we are left with the circuit illustrated in Fig. 8.33a. Next, we push the inductor and \hat{d} voltage source through the $D':1$ transformer, as in Fig. 8.33b.

Figure 8.33b contains a \hat{d} -dependent voltage source and a \hat{d} -dependent current source. The transfer function $G_{vd}(s)$ can therefore be expressed as a superposition of terms arising from these two sources. When the current source is set to zero (i.e., open-circuited), the circuit of Fig. 8.34a is obtained. The output $\hat{v}(s)$ can then be expressed as

$$\frac{\hat{v}(s)}{\hat{d}(s)} = \left(-\frac{V_g - V}{D'} \right) \frac{\left(R \parallel \frac{1}{sC} \right)}{\frac{sL}{D'^2} + \left(R \parallel \frac{1}{sC} \right)} \quad (8.137)$$

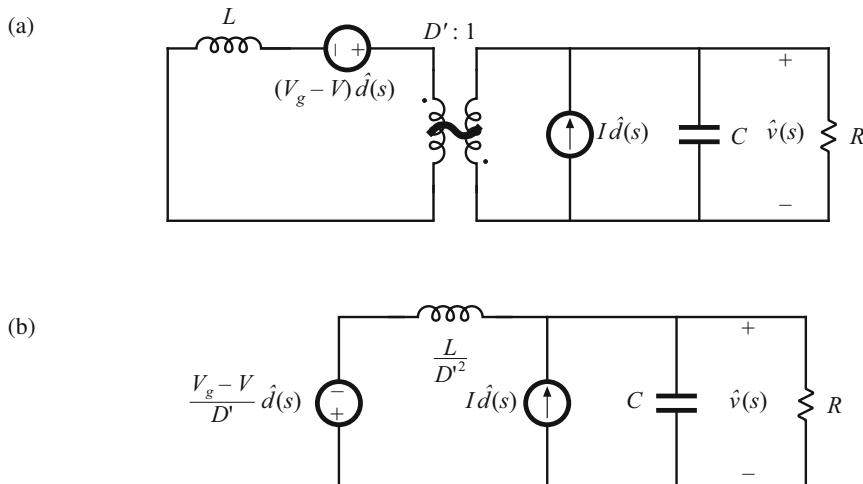


Fig. 8.33 Manipulation of buck-boost equivalent circuit to find the control-to-output transfer function $G_{vd}(s)$: (a) set \hat{v}_g source to zero; (b) push inductor and voltage source through transformer

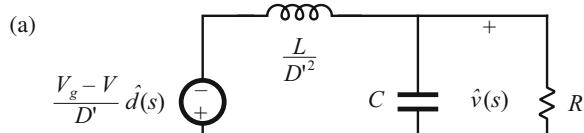
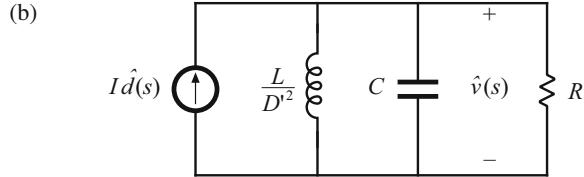


Fig. 8.34 Solution of the model of Fig. 8.33b by superposition: (a) current source set to zero; (b) voltage source set to zero



When the voltage source is set to zero (i.e., short-circuited), Fig. 8.33b reduces to the circuit illustrated in Fig. 8.34b. The output $\hat{v}(s)$ can then be expressed as

$$\frac{\hat{v}(s)}{\hat{d}(s)} = I \left(\frac{sL}{D'^2} \| R \| \frac{1}{sC} \right) \quad (8.138)$$

The transfer function $G_{vd}(s)$ is the sum of Eqs. (8.137) and (8.138):

$$G_{vd}(s) = \left(-\frac{V_g - V}{D'} \right) \frac{\left(R \| \frac{1}{sC} \right)}{\frac{sL}{D'^2} + \left(R \| \frac{1}{sC} \right)} + I \left(\frac{sL}{D'^2} \| R \| \frac{1}{sC} \right) \quad (8.139)$$

By algebraic manipulation, one can reduce this expression to

$$G_{vd}(s) = \frac{\hat{v}(s)}{\hat{d}(s)} \Big|_{\hat{v}_g(s)=0} = \left(-\frac{V_g - V}{D'} \right) \frac{\left(1 - s \frac{LI}{D'(V_g - V)} \right)}{\left(1 + s \frac{L}{D'^2 R} + s^2 \frac{LC}{D'^2} \right)} \quad (8.140)$$

This equation is of the form

$$G_{vd}(s) = G_{d0} \frac{\left(1 - \frac{s}{\omega_z} \right)}{\left(1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0} \right)^2 \right)} \quad (8.141)$$

The denominators of Eq. (8.140) and (8.130) are identical, and hence $G_{vd}(s)$ and $G_{vg}(s)$ share the same ω_0 and Q , given by Eqs. (8.134) and (8.136). The dc gain is

$$G_{d0} = -\frac{V_g - V}{D'} = -\frac{V_g}{D'^2} = \frac{V}{DD'} \quad (8.142)$$

The angular frequency of the zero is found by equating coefficients of s in the numerators of Eqs. (8.140) and (8.141). One obtains

$$\omega_z = \frac{D'(V_g - V)}{LI} = \frac{D'^2 R}{DL} \quad (\text{RHP}) \quad (8.143)$$

This zero lies in the right half-plane. Equations (8.142) and (8.143) have been simplified by use of the dc relationships

$$\begin{aligned} V &= -\frac{D}{D'} V_g \\ I &= -\frac{V}{D' R} \end{aligned} \quad (8.144)$$

Equations (8.134), (8.136), (8.142), and (8.143) constitute the results of the analysis of the control-to-output transfer function: analytical expressions for the salient features ω_0 , Q , G_{d0} , and ω_z . These expressions can be used to choose the element values such that given desired values of the salient features are obtained.

Having found analytical expressions for the salient features of the transfer functions, we can now plug in numerical values and construct the Bode plot. Suppose that we are given the following values:

$$\begin{aligned} D &= 0.6 \\ R &= 10 \Omega \\ V_g &= 30 \text{ V} \\ L &= 160 \mu\text{H} \\ C &= 160 \mu\text{F} \end{aligned} \quad (8.145)$$

We can evaluate Eqs. (8.132), (8.134), (8.136), (8.142), and (8.143), to determine numerical values of the salient features of the transfer functions. The results are:

$$\begin{aligned} |G_{g0}| &= \frac{D}{D'} = 1.5 \Rightarrow 3.5 \text{ dB} \\ |G_{d0}| &= \frac{|V|}{DD'} = 187.5 \text{ V} \Rightarrow 45.5 \text{ dB V} \\ f_0 &= \frac{\omega_0}{2\pi} = \frac{D'}{2\pi\sqrt{LC}} = 400 \text{ Hz} \\ Q &= D'R \sqrt{\frac{C}{L}} = 4 \Rightarrow 12 \text{ dB} \\ f_z &= \frac{\omega_z}{2\pi} = \frac{D'^2 R}{2\pi DL} = 2.65 \text{ kHz} \end{aligned} \quad (8.146)$$

The Bode plot of the magnitude and phase of G_{vd} is constructed in Fig. 8.35. The transfer function contains a dc gain of 45.5 dBV, resonant poles at 400 Hz having a Q of 4 \Rightarrow 12dB, and a right half-plane zero at 2.65 kHz. the resonant poles contribute -180° to the high-frequency phase asymptote, while the right half-plane zero contributes -90° . In addition, the inverting characteristic of the buck-boost converter leads to a 18° phase reversal, not included in Fig. 8.35.

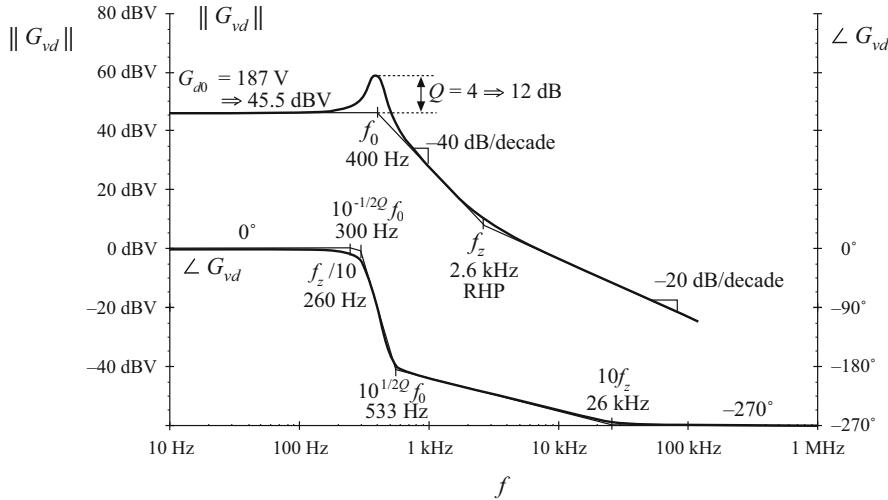


Fig. 8.35 Bode plot of the control-to-output transfer function G_{vd} , buck-boost converter example. Phase reversal owing to output voltage inversion is not included

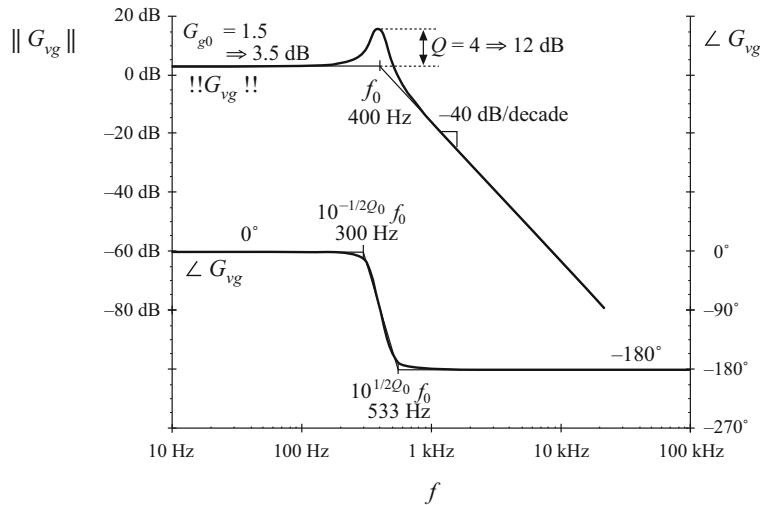


Fig. 8.36 Bode plot of the line-to-output transfer function G_{vg} , buck-boost converter example. Phase reversal owing to output voltage inversion is not included

The Bode plot of the magnitude and phase of the line-to-output transfer function G_{vg} is constructed in Fig. 8.36. This transfer function contains the same resonant poles at 400 Hz, but is missing the right half-plane zero. The dc gain G_{g0} is equal to the conversion ratio $M(D)$ of the converter. Again, the 180° phase reversal, caused by the inverting characteristic of the buck-boost converter, is not included in Fig. 8.36.

Table 8.2 Salient features of the small-signal CCM transfer functions of some basic dc–dc converters

Converter	G_{g0}	G_{d0}	ω_0	Q	ω_z
Buck	D	$\frac{V}{D}$	$\frac{1}{\sqrt{LC}}$	$R\sqrt{\frac{C}{L}}$	∞
Boost	$\frac{1}{D'}$	$\frac{V}{D'}$	$\frac{D'}{\sqrt{LC}}$	$D'R\sqrt{\frac{C}{L}}$	$\frac{D'^2R}{L}$
Buck-boost	$-\frac{D}{D'}$	$\frac{V}{DD'}$	$\frac{D'}{\sqrt{LC}}$	$D'R\sqrt{\frac{C}{L}}$	$\frac{D'^2R}{DL}$

8.2.2 Transfer Functions of Some Basic CCM Converters

The salient features of the line-to-output and control-to-output transfer functions of the basic buck, boost, and buck-boost converters are summarized in Table 8.2. In each case, the control-to-output transfer function is of the form

$$G_{vd}(s) = G_{d0} \frac{\left(1 - \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)} \quad (8.147)$$

and the line-to-output transfer function is of the form

$$G_{vg}(s) = G_{g0} \frac{1}{\left(1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)} \quad (8.148)$$

The boost and buck-boost converters exhibit control-to-output transfer functions containing two poles and a right half-plane zero. The buck converter $G_{vd}(s)$ exhibits two poles but no zero. The line-to-output transfer functions of all three ideal converters contain two poles and no zeroes.

These results can be easily adapted to transformer-isolated versions of the buck, boost, and buck-boost converters. The transformer has negligible effect on the transfer functions $G_{vg}(s)$ and $G_{vd}(s)$, other than introduction of a turns ratio. For example, when the transformer of the bridge topology is driven symmetrically, its magnetizing inductance does not contribute dynamics to the converter small-signal transfer functions. Likewise, when the transformer magnetizing inductance of the forward converter is reset by the input voltage v_g , as in Figs. 6.24 or 6.29, then it also contributes negligible dynamics. In all transformer-isolated converters based on the buck, boost, and buck-boost converters, the line-to-output transfer function $G_{vg}(s)$ should be multiplied by the transformer turns ratio; the transfer functions (8.147) and (8.148) and the parameters listed in Table 8.2 can otherwise be directly applied.

8.2.3 Physical Origins of the Right Half-Plane Zero in Converters

Figure 8.37 contains a block diagram that illustrates the behavior of the right half-plane zero. At low frequencies, the gain (s/ω_z) has negligible magnitude, and hence $u_{out} \approx u_{in}$. At high frequencies, where the magnitude of the gain (s/ω_z) is much greater than 1, $u_{out} \approx -(s/\omega_z)u_{in}$. The negative sign causes a phase reversal at high frequency. The implication for the transient response is that the output initially tends in the opposite direction of the final value.

We have seen that the control-to-output transfer functions of the boost and buck-boost converters, Fig. 8.38, exhibit RHP zeroes. Typical transient response waveforms for a step change in duty cycle are illustrated in Fig. 8.39. For this example, the converter initially operates in equilibrium, at $d = 0.4$ and $d' = 0.6$. Equilibrium inductor current $i_L(t)$, diode current $i_D(t)$, and output voltage $v(t)$ waveforms are illustrated. The average diode current is

$$\langle i_D \rangle_{T_s} = d' \langle i_L \rangle_{T_s} \quad (8.149)$$

By capacitor charge balance, this average diode current is equal to the dc load current when the converter operates in equilibrium. At time $t = t_1$, the duty cycle is increased to 0.6. In consequence, d' decreases to 0.4. The average diode current, given by Eq. (8.149), therefore decreases, and the output capacitor begins to discharge. The output voltage magnitude initially decreases as illustrated.

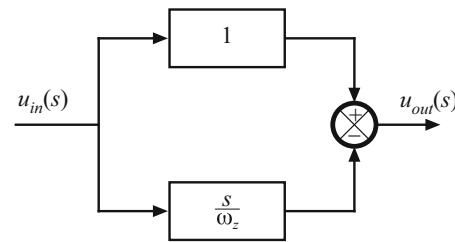


Fig. 8.37 Block diagram having a right half-plane zero transfer function, as in Eq. (8.32), with $\omega_0 = \omega_z$

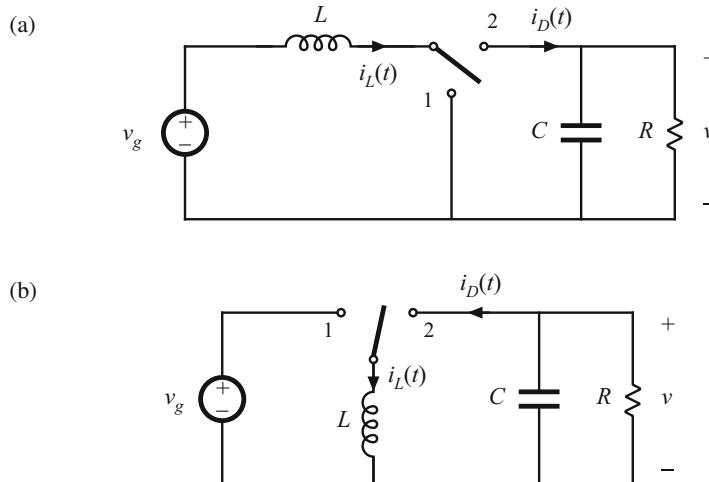


Fig. 8.38 Two basic converters whose CCM control-to-output transfer functions exhibit RHP zeroes: (a) boost, (b) buck-boost

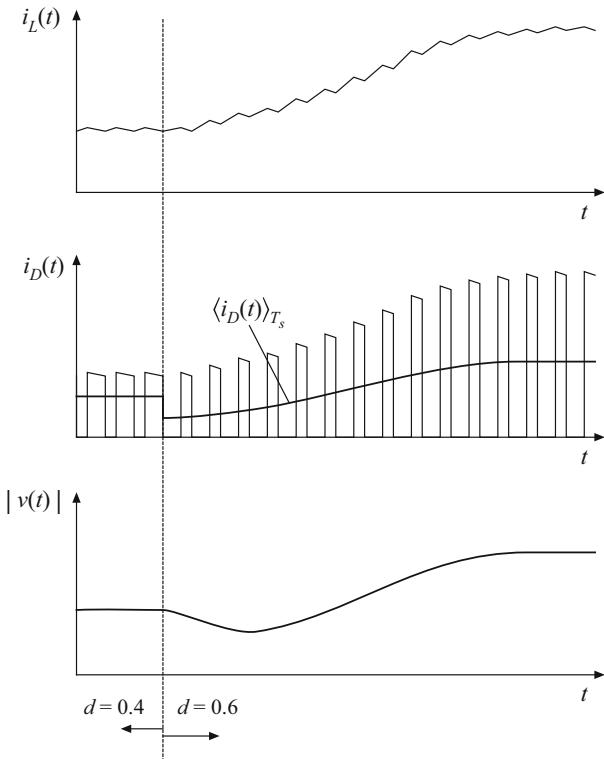


Fig. 8.39 Waveforms of the converters of Fig. 8.38, for a step response in duty cycle. The average diode current and output voltage initially decrease, as predicted by the RHP zero. Eventually, the inductor current increases, causing the average diode current and the output voltage to increase

The increased duty cycle causes the inductor current to slowly increase, and hence the average diode current eventually exceeds its original $d = 0.4$ equilibrium value. The output voltage eventually increases in magnitude, to the new equilibrium value corresponding to $d = 0.6$.

The presence of a right half-plane zero tends to destabilize wide-bandwidth feedback loops, because during a transient the output initially changes in the wrong direction. The phase margin test for feedback loop stability is discussed in the next chapter; when a RHP zero is present, it is difficult to obtain an adequate phase margin in conventional single-loop feedback systems having wide bandwidth. Prediction of the right half-plane zero, and the consequent explanation of why the feedback loops controlling CCM boost and buck-boost converters tend to oscillate, was one of the early successes of averaged converter modeling.

8.3 Graphical Construction of Impedances and Transfer Functions

Often, we can draw approximate Bode diagrams by inspection, without large amounts of messy algebra and the inevitable associated algebra mistakes. A great deal of insight can be gained into the operation of the circuit using this method. It becomes clear which components dominate the circuit response at various frequencies, and so suitable approximations become obvious. Analytical expressions for the approximate corner frequencies and asymptotes can be obtained directly. Impedances and transfer functions of quite complicated networks can be constructed. Thus insight can be gained, so that the design engineer can modify the circuit to obtain a desired frequency response.

The graphical construction method, also known as “doing algebra on the graph,” involves use of a few simple rules for combining the magnitude Bode plots of impedances and transfer functions.

8.3.1 Series Impedances: Addition of Asymptotes

A series connection represents the addition of impedances. If the Bode diagrams of the individual impedance magnitudes are known, then the asymptotes of the series combination are found by simply taking the largest of the individual impedance asymptotes. In many cases, the result is exact. In other cases, such as when the individual asymptotes have the same slope, then the result is an approximation; nonetheless, the accuracy of the approximation can be quite good.

Consider the series-connected R - C network of Fig. 8.40. It is desired to construct the magnitude asymptotes of the total series impedance $Z(s)$, where

$$Z(s) = R + \frac{1}{sC} \quad (8.150)$$

Let us first sketch the magnitudes of the individual impedances. The $10\ \Omega$ resistor has an impedance magnitude of $10\ \Omega \Rightarrow 20\ \text{dB}\Omega$. This value is independent of frequency, and is given in Fig. 8.41. The capacitor has an impedance magnitude of $1/\omega C$. This quantity varies inversely with ω , and hence its magnitude Bode plot is a line with slope $-20\ \text{dB}/\text{decade}$. The line passes through $1\ \Omega \Rightarrow 0\ \text{dB}\Omega$ at the angular frequency ω where

$$\frac{1}{\omega C} = 1\ \Omega \quad (8.151)$$

that is, at

$$\omega = \frac{1}{(1\ \Omega)C} = \frac{1}{(1\ \Omega)(10^{-6}\text{F})} = 10^6\ \text{rad/sec} \quad (8.152)$$

Fig. 8.41
Impedance magnitudes of the individual elements in the network of Fig. 8.40

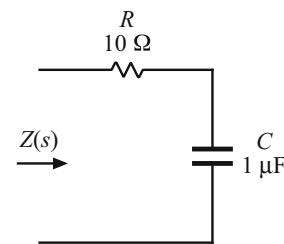
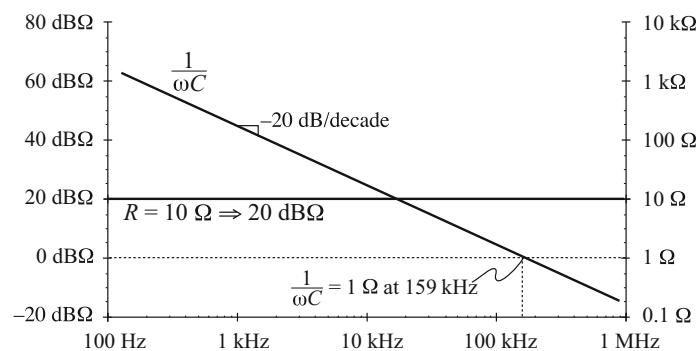


Fig. 8.40 Series R - C network example

In terms of frequency f , this occurs at

$$f = \frac{\omega}{2\pi} = \frac{10^6}{2\pi} = 159 \text{ kHz} \quad (8.153)$$

So the capacitor impedance magnitude is a line with slope -20 dB/dec , and which passes through $0 \text{ dB}\Omega$ at 159 kHz , as shown in Fig. 8.41. It should be noted that, for simplicity, the asymptotes in Fig. 8.41 have been labeled R and $1/\omega C$. But to draw the Bode plot, we must actually plot $\text{dB}\Omega$; for example, $20 \log_{10}(R/1 \Omega)$ and $20 \log_{10}((1/\omega C)/1 \Omega)$.

Let us now construct the magnitude of $Z(s)$, given by Eq. (8.150). The magnitude of Z can be approximated as follows:

$$\|Z(j\omega)\| = \left\| R + \frac{1}{j\omega C} \right\| \approx \begin{cases} R & \text{for } R \gg 1/\omega C \\ \frac{1}{\omega C} & \text{for } R \ll 1/\omega C \end{cases} \quad (8.154)$$

The asymptotes of the series combination are simply the larger of the individual resistor and capacitor asymptotes, as illustrated by the heavy lines in Fig. 8.42. For this example, these are in fact the exact asymptotes of $\|Z\|$. In the limiting case as frequency tends to zero (dc), then the capacitor tends to an open circuit. The series combination is then dominated by the capacitor, and the exact function tends asymptotically to the capacitor impedance magnitude. In the limiting case as frequency tends to infinity, then the capacitor tends to a short circuit, and the total impedance becomes simply R . So the R and $1/\omega C$ lines are the exact asymptotes for this example.

The corner frequency f_0 , where the asymptotes intersect, can now be easily deduced. At angular frequency $\omega_0 = 2\pi f_0$, the two asymptotes are equal in value:

$$\frac{1}{\omega_0 C} = R \quad (8.155)$$

Solution for ω_0 and f_0 leads to:

$$\begin{aligned} \omega_0 &= \frac{1}{RC} = \frac{1}{(10 \Omega)(10^{-6} \text{ F})} = 10^5 \text{ rad/sec} \\ f_0 &= \frac{\omega_0}{2\pi} = \frac{1}{2\pi RC} = 16 \text{ kHz} \end{aligned} \quad (8.156)$$

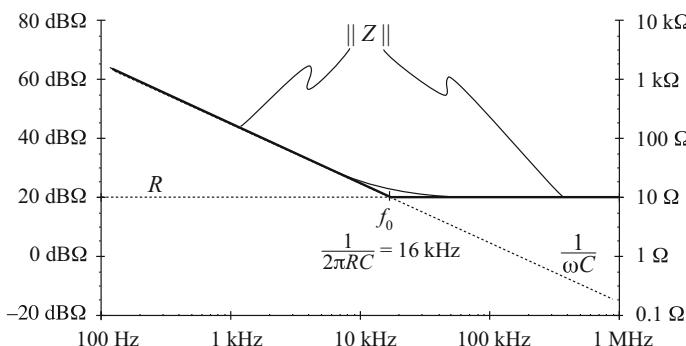


Fig. 8.42 Construction of the composite asymptotes of $\|Z\|$. The asymptotes of the series combination can be approximated by simply selecting the larger of the individual resistor and capacitor asymptotes

So if we can write analytical expressions for the asymptotes, then we can equate the expressions to find analytical expressions for the corner frequencies where the asymptotes intersect.

The deviation of the exact curve from the asymptotes follows all of the usual rules. The slope of the asymptotes changes by +20 dB/decade at the corner frequency f_0 (i.e., from $-20 \text{ dB}\Omega/\text{decade}$ to $0 \text{ dB}\Omega/\text{decade}$), and hence there is a zero at $f = f_0$. So the exact curve deviates from the asymptotes by $+3 \text{ dB}\Omega$ at $f = f_0$, and by $+1 \text{ dB}\Omega$ at $f = 2f_0$ and at $f = f_0/2$.

8.3.2 Series Resonant Circuit Example

As a second example, let us construct the magnitude asymptotes for the series $R-L-C$ circuit of Fig. 8.43. The series impedance $Z(s)$ is

$$Z(s) = R + sL + \frac{1}{sC} \quad (8.157)$$

The magnitudes of the individual resistor, inductor, and capacitor asymptotes are plotted in Fig. 8.44, for the values

$$\begin{aligned} R &= 1 \text{ k}\Omega \\ L &= 1 \text{ mH} \\ C &= 0.1 \mu\text{F} \end{aligned} \quad (8.158)$$

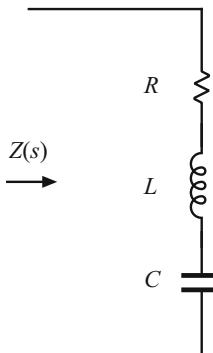


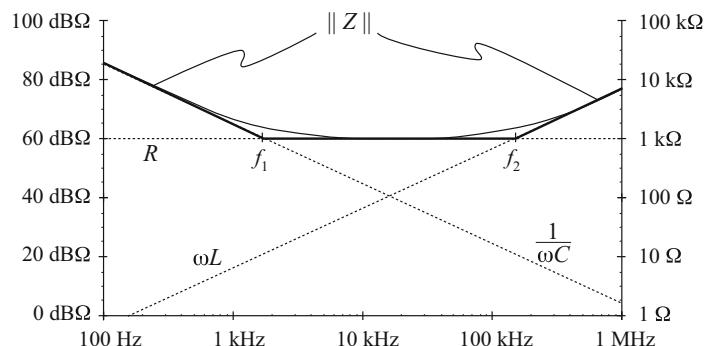
Fig. 8.43 Series $R-L-C$ network example

The series impedance $Z(s)$ is dominated by the capacitor at low frequency, by the resistor at mid frequencies, and by the inductor at high frequencies, as illustrated by the bold line in Fig. 8.44. The impedance $Z(s)$ contains a zero at angular frequency ω_1 , where the capacitor and resistor asymptotes intersect. By equating the expressions for the resistor and capacitor asymptotes, we can find ω_1 :

$$R = \frac{1}{\omega_1 C} \Rightarrow \omega_1 = \frac{1}{RC} \quad (8.159)$$

A second zero occurs at angular frequency ω_2 , where the inductor and resistor asymptotes intersect. Upon equating the expressions for the resistor and inductor asymptotes at ω_2 , we obtain the following:

Fig. 8.44 Graphical construction of $\|Z\|$ of the series $R-L-C$ network of Fig. 8.43, for the element values specified by Eq. (8.158)



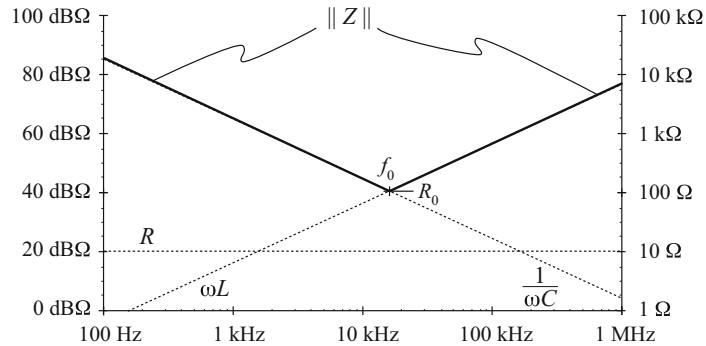


Fig. 8.45 Graphical construction of impedance asymptotes for the series $R-L-C$ network example, with R decreased to 10Ω

$$R = \omega_2 L \Rightarrow \omega_2 = \frac{R}{L} \quad (8.160)$$

So simple expressions for all important features of the magnitude Bode plot of $Z(s)$ can be obtained directly. It should be noted that Eqs. (8.159) and (8.160) are approximate, rather than exact, expressions for the corner frequencies ω_1 and ω_2 . Equations (8.159) and (8.160) coincide with the results obtained via the low- Q approximation of Sect. 8.1.7.

Next, suppose that the value of R is decreased to 10Ω . As R is reduced in value, the approximate corner frequencies ω_1 and ω_2 move closer together until, at $R = 100 \Omega$, they are both 100 krad/sec . Reducing R further in value causes the asymptotes to become independent of the value of R , as illustrated in Fig. 8.45 for $R = 10 \omega$. The $\|Z\|$ asymptotes now switch directly from ωL to $1/\omega C$.

So now there are two zeroes at $\omega = \omega_0$. At corner frequency ω_0 , the inductor and capacitor asymptotes are equal in value. Hence,

$$\omega_0 L = \frac{1}{\omega_0 C} = R_0 \quad (8.161)$$

Solution for the angular corner frequency ω_0 leads to

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (8.162)$$

At $\omega = \omega_0$, the inductor and capacitor impedances both have magnitude R_0 , called the characteristic impedance.

Since there are two zeroes at $\omega = \omega_0$, there is a possibility that the two poles could be complex conjugates, and that peaking could occur in the vicinity of $\omega = \omega_0$. So let us investigate what the actual value of the series impedance $Z(j\omega_0)$ is

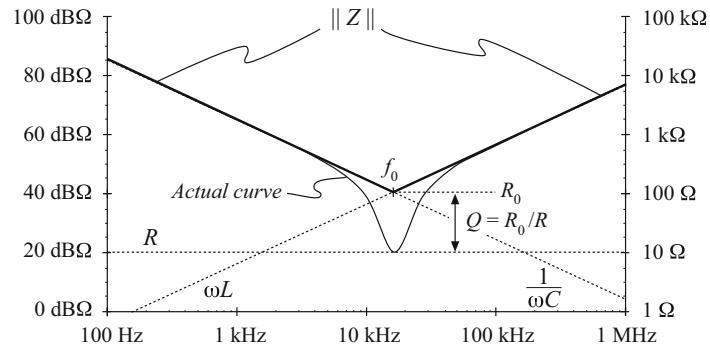
$$Z(j\omega_0) = R + j\omega_0 L + \frac{1}{j\omega_0 C} \quad (8.163)$$

Substitution of Eq. (8.161) into Eq. (8.163) leads to

$$Z(j\omega_0) = R + jR_0 + \frac{R_0}{j} = R + jR_0 - jR_0 = R \quad (8.164)$$

At $\omega = \omega_0$, the inductor and capacitor impedances are equal in magnitude but opposite in phase. Hence, they exactly cancel out in the series impedance, and we are left with $Z(j\omega_0) = R$, as

Fig. 8.46 Actual impedance magnitude (solid line) for the series resonant $R-L-C$ example. The inductor and capacitor impedances cancel out at $f = f_0$, and hence $Z(j\omega_0) = R$



illustrated in Fig. 8.46. The actual curve in the vicinity of the resonance at $\omega = \omega_0$ can deviate significantly from the asymptotes, because its value is determined by R rather than ωL or $1/\omega C$.

We know from Sect. 8.1.6 that the deviation of the actual curve from the asymptotes at $\omega = \omega_0$ is equal to Q . From Fig. 8.46, one can see that

$$|Q|_{\text{dB}} = |R_0|_{\text{dB}\Omega} - |R|_{\text{dB}\Omega} \quad (8.165)$$

or,

$$Q = \frac{R_0}{R} \quad (8.166)$$

Equations (8.161) to (8.166) are exact results for the series resonant circuit.

The practice of adding asymptotes by simply selecting the larger asymptote can be applied to transfer functions as well as impedances. For example, suppose that we have already constructed the magnitude asymptotes of two transfer functions, G_1 and G_2 , and we wish to find the asymptotes of $G = G_1 + G_2$. At each frequency, the asymptote for G can be approximated by simply selecting the larger of the asymptotes for G_1 and G_2 :

$$G = G_1 + G_2 \approx \begin{cases} G_1, & \|G_1\| \gg \|G_2\| \\ G_2, & \|G_2\| \gg \|G_1\| \end{cases} \quad (8.167)$$

Corner frequencies can be found by equating expressions for asymptotes as illustrated in the preceding examples. In the next chapter, we will see that this approach yields a simple and powerful method for determining the closed-loop transfer functions of feedback systems.

8.3.3 Parallel Impedances: Inverse Addition of Asymptotes

A parallel combination represents inverse addition of impedances:

$$Z_{\text{par}} = \frac{1}{\left(\frac{1}{Z_1} + \frac{1}{Z_2} + \dots \right)} = Z_1 \parallel Z_2 \parallel \dots \quad (8.168)$$

If the asymptotes of the individual impedances Z_1 , Z_2 , ..., are known, then the asymptotes of the parallel combination Z_{par} can be found by simply selecting the smallest individual impedance asymptote. This is true because the smallest impedance will have the largest inverse, and will dominate the inverse sum. As in the case of the series impedances, this procedure will often yield the exact asymptotes of Z_{par} .

Let us construct the magnitude asymptotes for the parallel $R-L-C$ network of Fig. 8.47, using the following element values:

$$\begin{aligned} R &= 10 \Omega \\ L &= 1 \text{ mH} \\ C &= 0.1 \mu\text{F} \end{aligned} \quad (8.169)$$

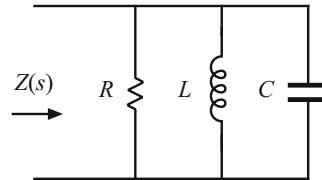


Fig. 8.47 Parallel $R-L-C$ network example

Impedance magnitudes of the individual elements are illustrated in Fig. 8.48. The asymptotes for the total parallel impedance Z are approximated by simply selecting the smallest individual element impedance, as shown by the heavy line in Fig. 8.48. So the parallel impedance is dominated by the inductor at low frequency, by the resistor at mid frequencies, and by the capacitor at high frequency. Approximate expressions for the angular corner frequencies are again found by equating asymptotes:

$$\begin{aligned} \text{at } \omega = \omega_1, R = \omega_1 L \Rightarrow \omega_1 = \frac{R}{L} \\ \text{at } \omega = \omega_2, R = \frac{1}{\omega_2 C} \Rightarrow \omega_2 = \frac{1}{RC} \end{aligned} \quad (8.170)$$

These expressions could have been obtained by conventional analysis, combined with the low- Q approximation of Sect. 8.1.7.

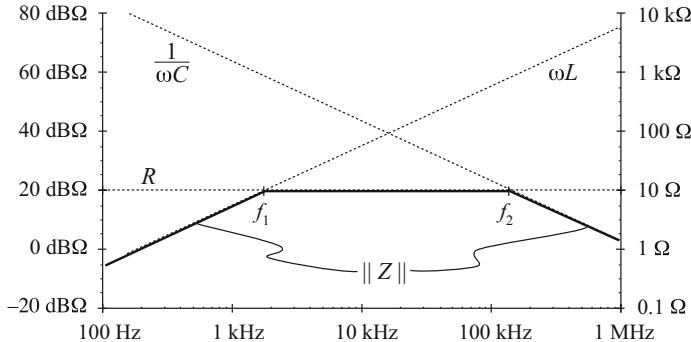


Fig. 8.48 Construction of the composite asymptotes of $\|Z\|$, for the parallel $R-L-C$ example. The asymptotes of the parallel combination can be approximated by simply selecting the smallest of the individual resistor, inductor, and capacitor asymptotes

8.3.4 Parallel Resonant Circuit Example

Figure 8.49 illustrates what happens when the value of R in the parallel $R-L-C$ network is increased to $1 \text{ k}\Omega$. The asymptotes for $\|Z\|$ then become independent of R , and change directly from ωL to $1/\omega C$ at angular frequency ω_0 . The corner frequency ω_0 is now the frequency where the inductor and capacitor asymptotes have equal value:

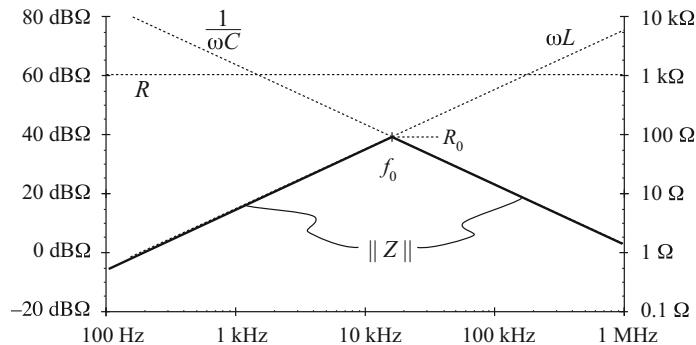


Fig. 8.49 Graphical construction of impedance asymptotes for the parallel $R-L-C$ example, with R increased to $1\text{ k}\Omega$

$$\omega_0 L = \frac{1}{\omega_0 C} = R_0 \quad (8.171)$$

which implies that

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (8.172)$$

At $\omega = \omega_0$, the slope of the asymptotes of $\|Z\|$ changes from $+20\text{ dB/decade}$ to -20 dB/decade , and hence there are two poles. We should investigate whether peaking occurs, by determining the exact value of $\|Z\|$ at $\omega = \omega_0$, as follows:

$$Z(j\omega_0) = (R) \parallel (j\omega_0 L) \parallel \left(\frac{1}{j\omega_0 C} \right) = \frac{1}{\left(\frac{1}{R} + \frac{1}{j\omega_0 L} + j\omega_0 C \right)} \quad (8.173)$$

Substitution of Eq. (8.171) into (8.173) yields

$$Z(j\omega_0) = \frac{1}{\frac{1}{R} + \frac{1}{jR_0} + \frac{j}{R_0}} = \frac{1}{\frac{1}{R} - \frac{j}{R_0} + \frac{j}{R_0}} = R \quad (8.174)$$

So at $\omega = \omega_0$, the impedances of the inductor and capacitor again cancel out, and we are left with $Z(j\omega_0) = R$. The values of L and C determine the values of the asymptotes, but R determines the value of the actual curve at $\omega = \omega_0$.

The actual curve is illustrated in Fig. 8.50. The deviation of the actual curve from the asymptotes at $\omega = \omega_0$ is

$$|Q|_{\text{dB}} = |R|_{\text{dB}\Omega} - |R_0|_{\text{dB}\Omega} \quad (8.175)$$

or,

$$Q = \frac{R}{R_0} \quad (8.176)$$

Equations (8.171) to (8.176) are exact results for the parallel resonant circuit.

The graphical construction method for impedance magnitudes is well known, and *reactance paper* can be purchased commercially. As illustrated in Fig. 8.51, the magnitudes of the impedances of various inductances, capacitances, and resistances are plotted on semi-logarithmic axes. Asymptotes for the impedances of $R-L-C$ networks can be sketched directly on these axes, and numerical values of corner frequencies can then be graphically determined.

Fig. 8.50 Actual impedance magnitude (solid line) for the parallel resonant $R-L-C$ example. The inductor and capacitor impedances cancel out at $f = f_0$, and hence $Z(j\omega_0) = R$

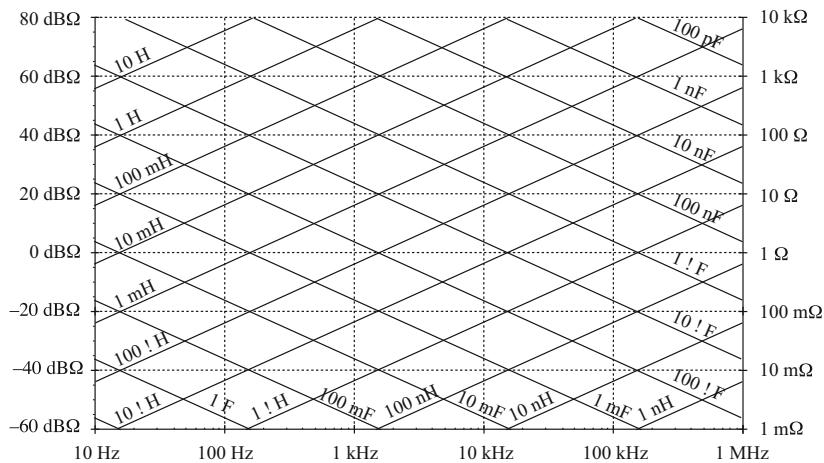
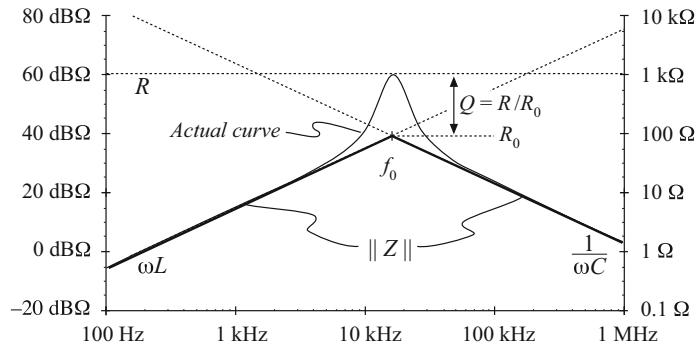


Fig. 8.51 “Reactance paper”: an aid for graphical construction of impedances, with the magnitudes of various inductive, capacitive, and resistive impedances preplotted

8.3.5 Voltage Divider Transfer Functions: Division of Asymptotes

Usually, we can express transfer functions in terms of impedances—for example, as the ratio of two impedances. If we can construct these impedances as described in the previous sections, then we can divide to construct the transfer function. In this section, construction of the transfer function $H(s)$ of the two-pole $R-L-C$ low-pass filter (Fig. 8.52) is discussed in detail. A filter of this form appears in the canonical model for two-pole converters, and the results of this section are applied in the converter examples of the next section.

The familiar voltage divider formula shows that the transfer function of this circuit can be expressed as the ratio of impedances Z_2/Z_{in} , where $Z_{in} = Z_1 + Z_2$ is the network input impedance:

$$\frac{\hat{v}_2(s)}{\hat{v}_1(s)} = \frac{Z_2}{Z_1 + Z_2} = \frac{Z_2}{Z_{in}} \quad (8.177)$$

For this example, $Z_1(s) = sL$, and $Z_2(s)$ is the parallel combination of R and $1/sC$. Hence, we can find the transfer function asymptotes by constructing the asymptotes of Z_2 and of the series

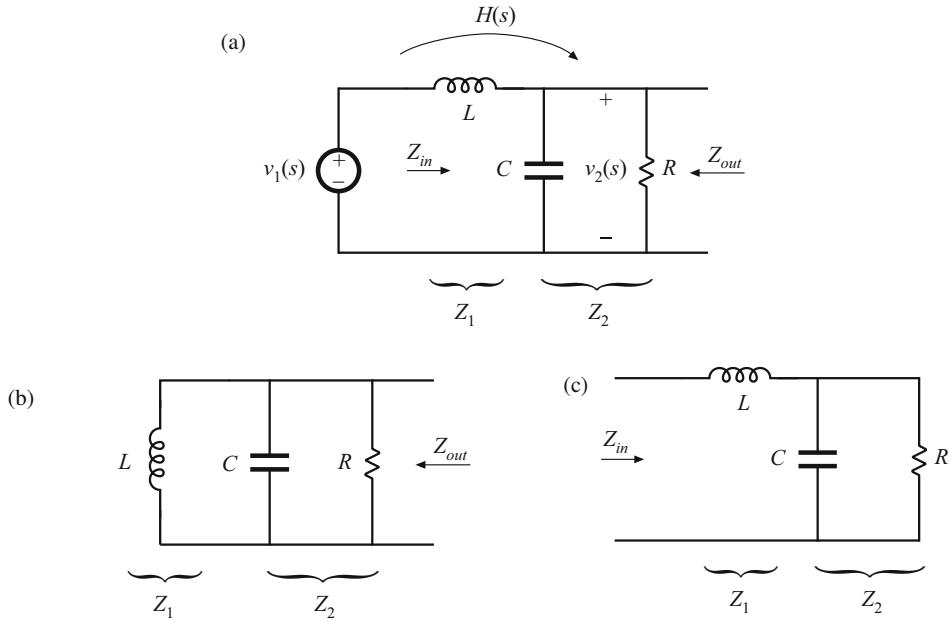


Fig. 8.52 Two-pole low-pass filter based on voltage divider circuit: (a) transfer function $H(s)$, (b) determination of $Z_{out}(s)$ by setting independent sources to zero, (c) determination of $Z_{in}(s)$

combination represented by Z_{in} , and then dividing. Another approach, which is easier to apply in this example, is to multiply the numerator and denominator of Eq. (8.177) by Z_1 :

$$\frac{\hat{v}_2(s)}{\hat{v}_1(s)} = \frac{Z_2 Z_1}{Z_1 + Z_2} \frac{1}{Z_1} = \frac{Z_{out}}{Z_1} \quad (8.178)$$

where $Z_{out} = Z_1 \parallel Z_2$ is the output impedance of the voltage divider. So another way to construct the voltage divider transfer function is to first construct the asymptotes for Z_1 and for the parallel combination represented by Z_{out} , and then divide. This method is useful when the parallel combination $Z_1 \parallel Z_2$ is easier to construct than the series combination $Z_1 + Z_2$. It often gives a different approximate result, which may be more (or sometimes less) accurate than the result obtained using Z_{in} .

The output impedance Z_{out} in Fig. 8.52b is

$$Z_{out}(s) = R \parallel \frac{1}{sC} \parallel sL \quad (8.179)$$

The impedance of the parallel $R-L-C$ network is constructed in Sect. 8.3.3, and is illustrated in Fig. 8.51a for the high- Q case.

According to Eq. (8.178), the voltage divider transfer function magnitude is $\|H\| = \|Z_{out}\|/\|Z_1\|$. This quantity is constructed in Fig. 8.53b. For $\omega < \omega_0$, the asymptote of $\|Z_{out}\|$ coincides with $\|Z_1\|$: both are equal to ωL . Hence, the ratio is $\|Z_{out}\|/\|Z_1\| = 1$. For $\omega > \omega_0$, the asymptote of $\|Z_{out}\|$ is $1/\omega C$, while $\|Z_1\|$ is equal to ωL . The ratio then becomes $\|Z_{out}\|/\|Z_1\| = 1/\omega^2 LC$, and hence the high-frequency asymptote has a -40 dB/decade slope.

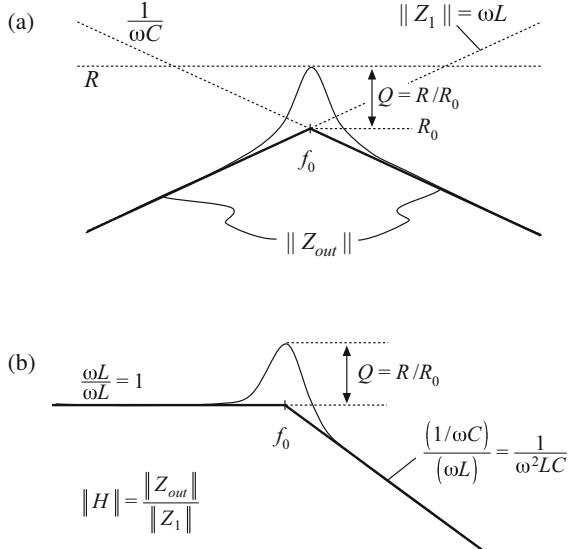
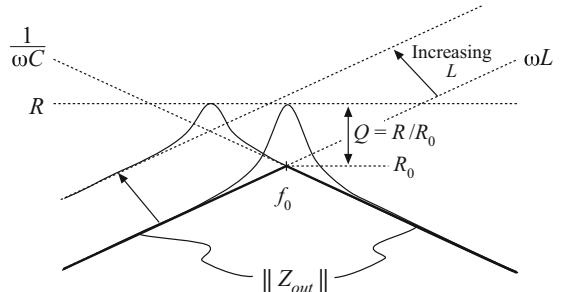


Fig. 8.53 Graphical construction of H and Z_{out} of the voltage divider circuit: (a) output impedance Z_{out} ; (b) transfer function H



At $\omega = \omega_0$, $\|Z_{out}\|$ has exact value R , while $\|Z_1\|$ has exact value R_0 . The ratio is then $\|H(j\omega_0)\| = \|Z_{out}(j\omega_0)\|/\|Z_1(j\omega_0)\| = R/R_0 = Q$. So the filter transfer function H has the same ω_0 and Q as the impedance Z_{out} .

It now becomes obvious how variations in element values affect the salient features of the transfer function and output impedance. For example, the effect of increasing L is illustrated in Fig. 8.54. This causes the angular resonant frequency ω_0 to be reduced, and also reduces the Q -factor.

8.4 Graphical Construction of Converter Transfer Functions

The small-signal equivalent circuit model of the buck converter, derived in Chap. 7, is reproduced in Fig. 8.55. Let us construct the transfer functions and terminal impedances of this converter, using the graphical approach of the previous section.

The output impedance $Z_{out}(s)$ is found with the $\hat{d}(s)$ and $\hat{v}_g(s)$ sources set to zero; the circuit of Fig. 8.56a is then obtained. This model coincides with the parallel $R-L-C$ circuit analyzed in Sects. 8.3.3 and 8.3.4. As illustrated in Fig. 8.56b, the output impedance is dominated by the

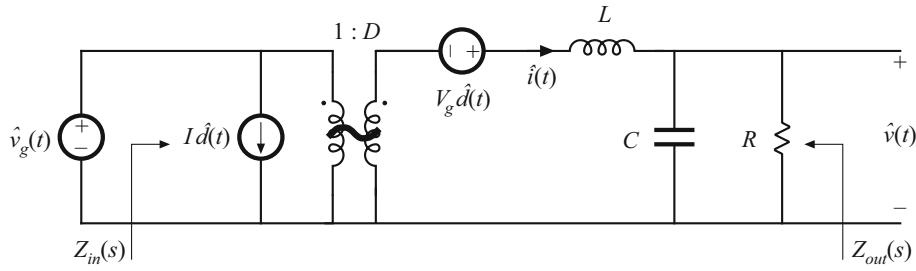


Fig. 8.55 Small-signal model of the buck converter, with input impedance $Z_{in}(s)$ and output impedance $Z_{out}(s)$ explicitly defined

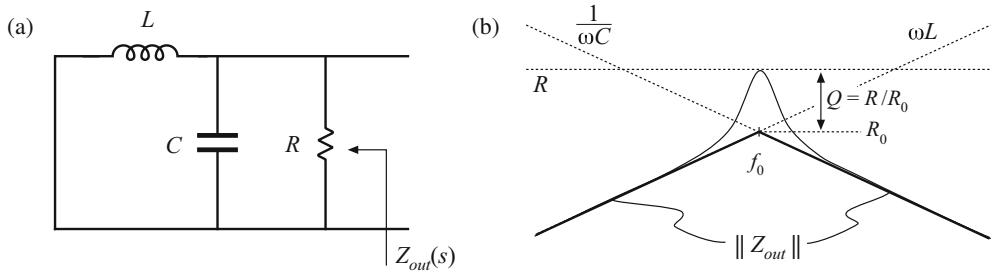


Fig. 8.56 Construction of buck converter output impedance $Z_{out}(s)$: (a) circuit model; (b) impedance asymptotes

inductor at low frequency, and by the capacitor at high frequency. At the resonant frequency f_0 , given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (8.180)$$

the output impedance is equal to the load resistance R . The Q -factor of the circuit is equal to

$$Q = \frac{R}{R_0} \quad (8.181)$$

where

$$R_0 = \omega_0 L = \frac{1}{\omega_0 C} = \sqrt{\frac{L}{C}} \quad (8.182)$$

Thus, the circuit is lightly damped (high Q) at light load, where the value of R is large.

The converter input impedance $Z_{in}(s)$ is also found with the $\hat{d}(s)$ and $\hat{v}_g(s)$ sources set to zero, as illustrated in Fig. 8.57a. The input impedance is referred to the primary side of the 1:D transformer, and is equal to

$$Z_{in}(s) = \frac{1}{D^2} [Z_1(s) + Z_2(s)] \quad (8.183)$$

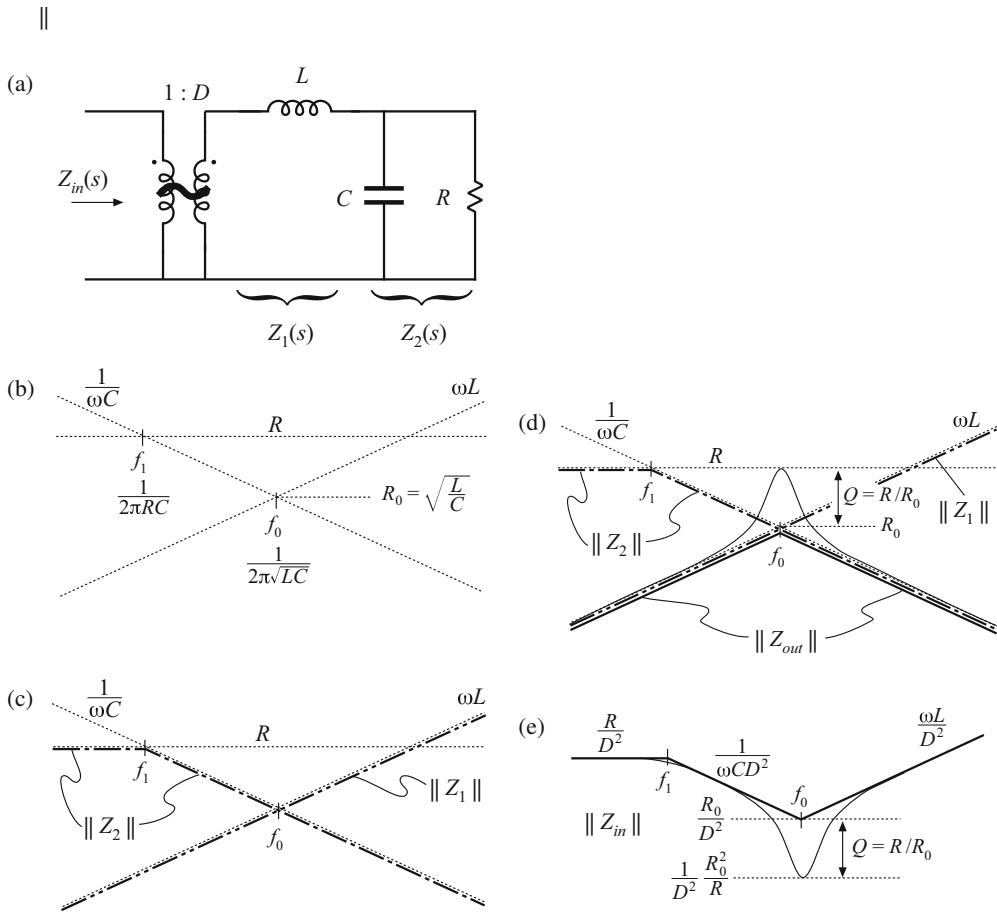


Fig. 8.57 Construction of the input impedance $Z_{in}(s)$ for the buck converter: (a) circuit model; (b) the individual resistor, inductor, and capacitor impedance magnitudes; (c) construction of the impedance magnitudes $\|Z_1\|$ and $\|Z_2\|$; (d) construction of $\|Z_{out}\|$; (e) final result $\|Z_{in}\|$

where

$$Z_1(s) = sL \quad (8.184)$$

and

$$Z_2(s) = R \left\| \frac{1}{sC} \right\| \quad (8.185)$$

We begin construction of the impedance asymptotes corresponding to Eqs. (8.183) to (8.185) by constructing the individual resistor, capacitor, and inductor impedances as in Fig. 8.57b. The impedances in Fig. 8.57 are constructed for the case $R > R_0$. As illustrated in Fig. 8.57c, $\|Z_1\|$ coincides with the inductor reactance ωL . The impedance $\|Z_2\|$ is asymptotic to resistance R

at low frequencies and to the capacitor reactance $1/\omega C$ at high frequency. The resistor and capacitor asymptotes intersect at corner frequency f_1 , given by

$$f_1 = \frac{1}{2\pi RC} \quad (8.186)$$

According to Eq. (8.183), the input impedance $Z_{in}(s)$ is equal to the series combination of $Z_1(s)$ and $Z_2(s)$, divided by the square of the turns ratio D . The asymptotes for the series combination $[Z_1(s) + Z_2(s)]$ are found by selecting the larger of the $\|Z_1\|$ and $\|Z_2\|$ asymptotes. The $\|Z_1\|$ and $\|Z_2\|$ asymptotes intersect at frequency f_0 , given by Eq. (8.180). It can be seen from Fig. 8.57c that the series combination is dominated by Z_2 for $f < f_0$ and by Z_1 for $f > f_0$. Upon scaling the $[Z_1(s) + Z_2(s)]$ asymptotes by the factor $1/D^2$, the input impedance asymptotes of Fig. 8.57e are obtained.

The zeroes of $Z_{in}(s)$, at frequency f_0 , have the same Q -factor as the poles of $Z_{out}(s)$ [Eq. (8.181)]. One way to see that this is true is to note that the output impedance can be expressed as

$$Z_{out}(s) = \frac{Z_1(s)Z_2(s)}{Z_1(s) + Z_2(s)} = \frac{Z_1(s)Z_2(s)}{D^2Z_{in}(s)} \quad (8.187)$$

Hence, we can relate $Z_{out}(s)$ to $Z_{in}(s)$ as follows:

$$Z_{in}(s) = \frac{1}{D^2} \frac{Z_1(s)Z_2(s)}{Z_{out}(s)} \quad (8.188)$$

The impedances $\|Z_1\|$, $\|Z_2\|$, and $\|Z_{out}\|$ are illustrated in Fig. 8.57d. At the resonant frequency $f = f_0$, impedance Z_1 has magnitude R_0 and impedance Z_2 has magnitude approximately equal to R_0 . The output impedance Z_{out} has magnitude R . Hence, Eq. (8.188) predicts that the input impedance has the magnitude

$$\|Z_{in}\| \approx \frac{1}{D^2} \frac{R_0 R_0}{R} \text{ at } f = f_0 \quad (8.189)$$

At $f = f_0$, the asymptotes of the input impedance have magnitude R_0/D^2 . The deviation from the asymptotes is therefore equal to $Q = R/R_0$, as illustrated in Fig. 8.57e.

The control-to-output transfer function $G_{vd}(s)$ is found with the $\hat{V}_g(s)$ source set to zero, as in Fig. 8.58a. This circuit coincides with the voltage divider analyzed in Sect. 8.3.5. Hence, $G_{vd}(s)$ can be expressed as

$$G_{vd}(s) = V_g \frac{Z_{out}(s)}{Z_1(s)} \quad (8.190)$$

The quantities $\|Z_{out}\|$ and $\|Z_1\|$ are constructed in Fig. 8.58b. According to Eq. (8.190), we can construct $\|G_{vd}(s)\|$ by finding the ratio of $\|Z_{out}\|$ and $\|Z_1\|$, and then scaling the result by V_g . For $f < f_0$, $\|Z_{out}\|$ and $\|Z_1\|$ are both equal to ωL and hence $\|Z_{out}\|/\|Z_1\|$ is equal to 1. As illustrated in Fig. 8.58c, the low-frequency asymptote of $\|G_{vd}(s)\|$ has value V_g . For $f > f_0$, $\|Z_{out}\|$ has asymptote $1/\omega C$, and $\|Z_1\|$ is equal to ωL . Hence, $\|Z_{out}\|/\|Z_1\|$ has asymptote $1/\omega^2 LC$, and the high-frequency asymptote of $\|G_{vd}(s)\|$ is equal to $V_g/\omega^2 LC$. The Q -factor of the two poles at $f = f_0$ is again equal to R/R_0 .

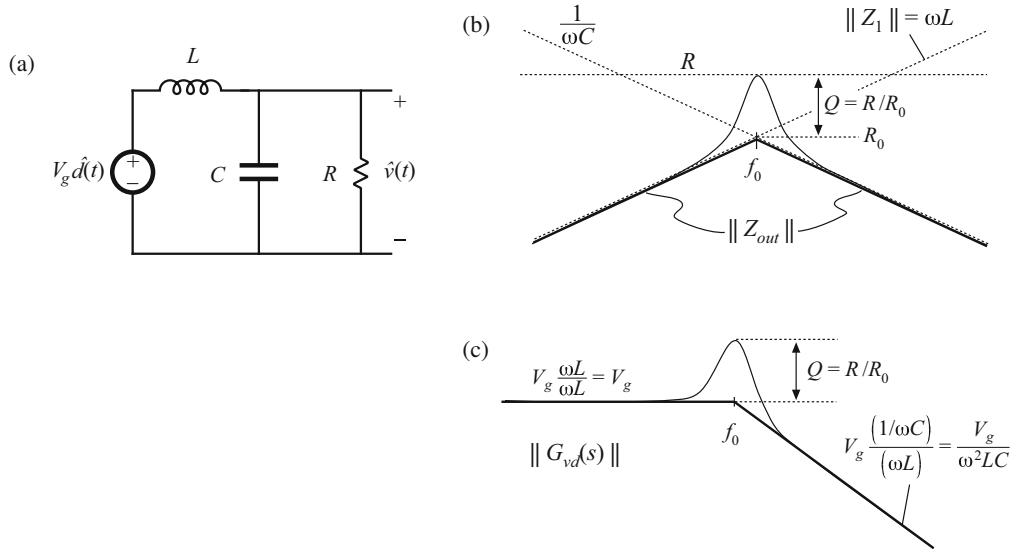


Fig. 8.58 Construction of the control-to-output transfer function $G_{vd}(s)$ for the buck converter: (a) circuit model; (b) relevant impedance asymptotes; (c) transfer function $\|G_{vd}(s)\|$

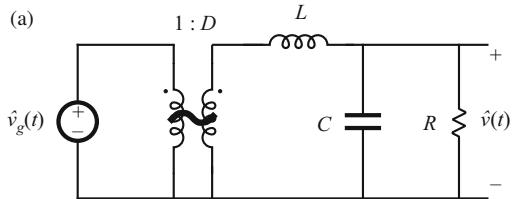
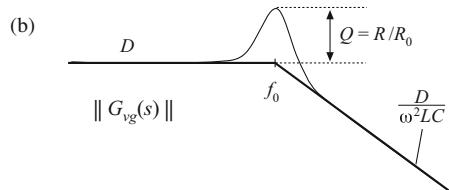


Fig. 8.59 The line-to-output transfer function $G_{vg}(s)$ for the buck converter: (a) circuit model; (b) magnitude asymptotes



The line-to-output transfer function $G_{vg}(s)$ is found with the $\hat{d}(s)$ sources set to zero, as in Fig. 8.59a. This circuit contains the same voltage divider as in Fig. 8.58, and additionally contains the $1:D$ transformer. The transfer function $G_{vg}(s)$ can be expressed as

$$G_{vg}(s) = D \frac{Z_{out}(s)}{Z_1(s)} \quad (8.191)$$

This expression is similar to Eq. (8.190), except for the scaling factor of D . Therefore, the line-to-output transfer function of Fig. 8.59b has the same shape as the control-to-output transfer function $G_{vd}(s)$.

8.5 Measurement of AC Transfer Functions and Impedances

It is good engineering practice to measure the transfer functions of prototype converters and converter systems. Such an exercise can verify that the system has been correctly modeled and designed. Also, it is often useful to characterize individual circuit elements through measurement of their terminal impedances.

Small-signal ac magnitude and phase measurements can be made using an instrument known as a network analyzer, or frequency response analyzer. The key inputs and outputs of a basic network analyzer are illustrated in Fig. 8.60. The network analyzer provides a sinusoidal output voltage \hat{v}_z of controllable amplitude and frequency. This signal can be injected into the system to be measured, at any desired location. The network analyzer also has two (or more) inputs, \hat{v}_x and \hat{v}_y . The return electrodes of \hat{v}_z , \hat{v}_y , and \hat{v}_x are internally connected to earth ground. The network analyzer performs the function of a narrowband tracking voltmeter: it measures the components of \hat{v}_x and \hat{v}_y at the injection frequency, and displays the magnitude and phase of the quantity \hat{v}_y/\hat{v}_x . The narrowband tracking voltmeter feature is essential for switching converter measurements; otherwise, switching ripple and noise corrupt the desired sinusoidal signals and make accurate measurements impossible [80]. Modern network analyzers can automatically sweep the frequency of the injection source \hat{v}_z to generate magnitude and phase Bode plots of the transfer function \hat{v}_y/\hat{v}_x .

A typical test setup for measuring the transfer function of an amplifier is illustrated in Fig. 8.61. A potentiometer, connected between a dc supply voltage V_{CC} and ground, is used to bias the amplifier input to attain the correct quiescent operating point. The injection source voltage \hat{v}_z is coupled to the amplifier input terminals via a dc blocking capacitor. This blocking capacitor prevents the injection voltage source from upsetting the dc bias. The network analyzer inputs \hat{v}_x and \hat{v}_y are connected to the input and output terminals of the amplifier. Hence, the measured transfer function is

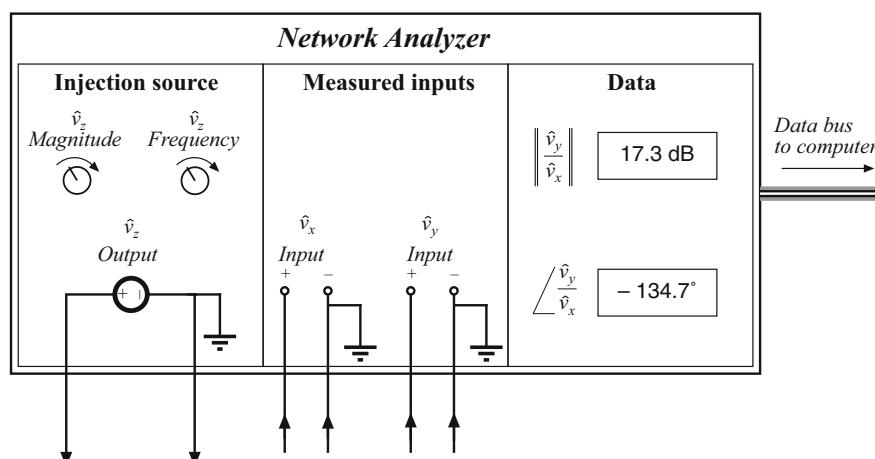


Fig. 8.60 Key features and functions of a network analyzer: sinusoidal source of controllable amplitude and frequency, two inputs, and determination of relative magnitude and phase of the input components at the injection frequency

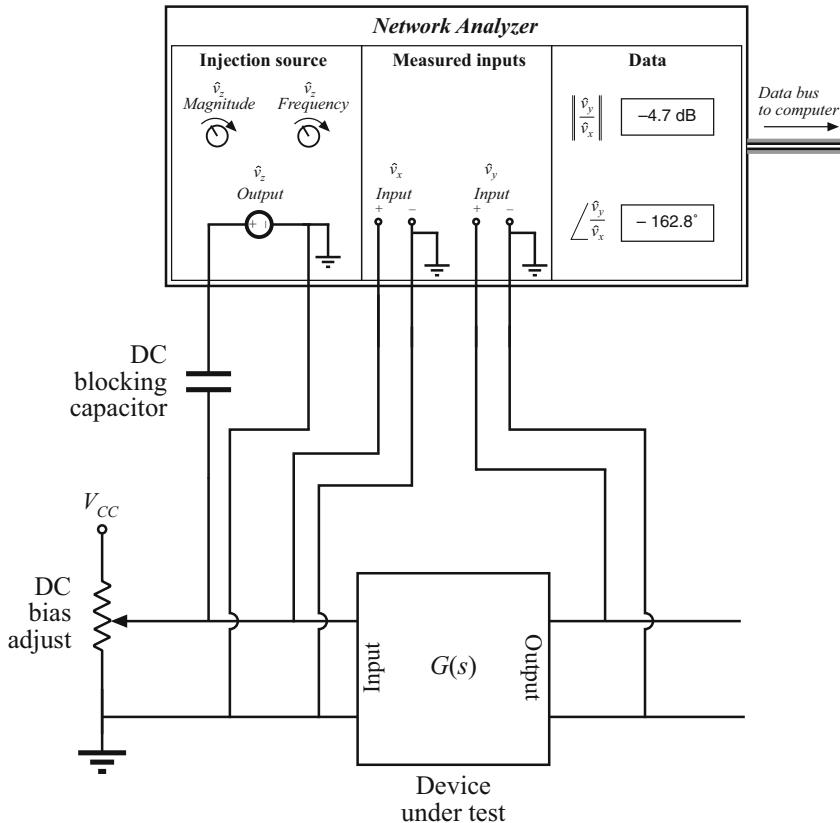


Fig. 8.61 Measurement of a transfer function

$$\frac{\hat{v}_y(s)}{\hat{v}_x(s)} = G(s) \quad (8.192)$$

Note that the blocking capacitance, bias potentiometer, and \hat{v}_z amplitude have no effect on the measured transfer function

An impedance

$$Z(s) = \frac{\hat{v}(s)}{\hat{i}(s)} \quad (8.193)$$

can be measured by treating the impedance as a transfer function from current to voltage. For example, measurement of the output impedance of an amplifier is illustrated in Fig. 8.62. The quiescent operating condition is again established by a potentiometer which biases the amplifier input. The injection source \hat{v}_z is coupled to the amplifier output through a dc blocking capacitor. The injection source voltage \hat{v}_z excites a current \hat{i}_{out} in impedance Z_s . This current flows into the output of the amplifier, and excites a voltage across the amplifier output impedance:

$$Z_{out}(s) = \left. \frac{\hat{v}_y(s)}{\hat{i}_{out}(s)} \right|_{\substack{\text{amplifier} \\ \text{ac input}}} = 0 \quad (8.194)$$

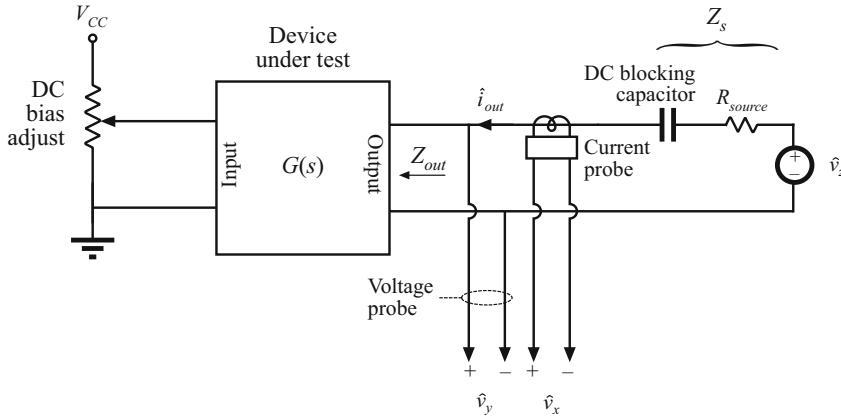


Fig. 8.62 Measurement of the output impedance of a circuit

A current probe is used to measure \hat{i}_{out} . The current probe produces a voltage proportional to \hat{i}_{out} ; this voltage is connected to the network analyzer input \hat{v}_x . A voltage probe is used to measure the amplifier output voltage \hat{v}_y . The network analyzer displays the transfer function \hat{v}_y/\hat{v}_x , which is proportional to Z_{out} . Note that the value of Z_s and the amplitude of \hat{v}_z do not affect the measurement of Z_{out} .

In power applications, it is sometimes necessary to measure impedances that are very small in magnitude. Grounding problems [4] cause the test setup of Fig. 8.62 to fail in such cases. The reason is illustrated in Fig. 8.63a. Since there turn connections of the injection source \hat{v}_z and the analyzer input \hat{v}_y are both connected to earth ground, the injected current \hat{i}_{out} can return to the source through the return connections of either the injection source or the voltage probe. In practice, \hat{i}_{out} divides between the two paths according to their relative impedances. Hence, a significant current $(1 - k)\hat{i}_{out}$ flows through the return connection of the voltage probe. If the voltage probe return connection has some total contact and wiring impedance Z_{probe} , then the current induces a voltage drop $(1 - k)\hat{i}_{out}Z_{probe}$ in the voltage probe wiring, as illustrated in Fig. 8.63a. Hence, the network analyzer does not correctly measure the voltage drop across the impedance Z . If the internal ground connections of the network analyzer have negligible impedance, then the network analyzer will display the following impedance:

$$Z + (1 - k)Z_{probe} = Z + Z_{probe}\|Z_{rz} \quad (8.195)$$

Here, Z_{rz} is the impedance of the injection source return connection. So to obtain an accurate measurement, the following condition must be satisfied:

$$\|Z\| \gg \|(Z_{probe}\|Z_{rz})\| \quad (8.196)$$

A typical lower limit on $\|Z\|$ is a few tens or hundreds of milliohms.

An improved test setup for measurement of small impedances is illustrated in Fig. 8.63b. An isolation transformer is inserted between the injection source and the dc blocking capacitor. The return connections of the voltage probe and injection source are no longer in parallel, and the injected current \hat{i}_{out} must now return entirely through the injection source return connection. An

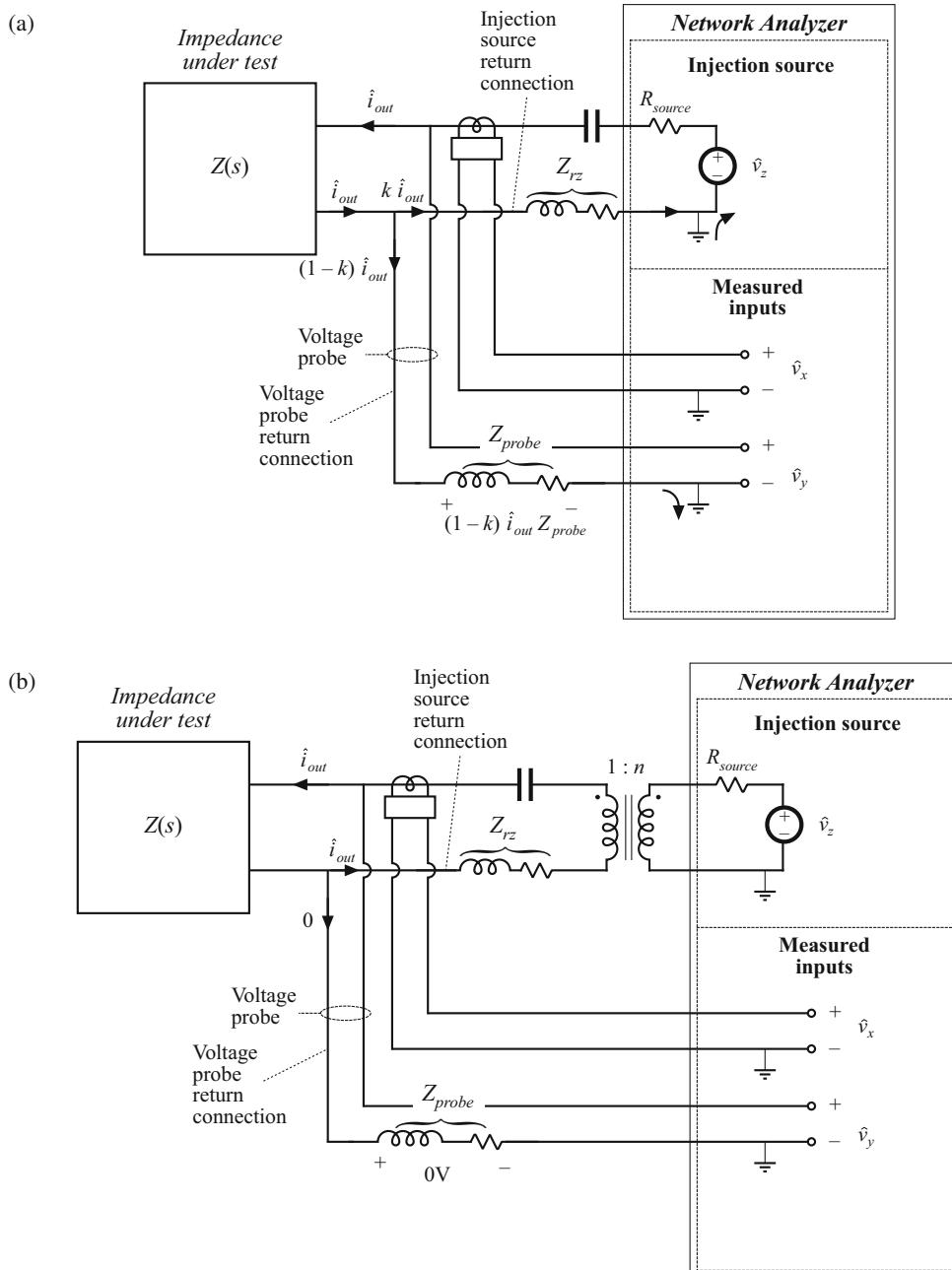


Fig. 8.63 Measurement of a small impedance $Z(s)$: (a) current flowing in the return connection of the voltage probe induces a voltage drop that corrupts the measurement; (b) an improved experiment, incorporating isolation of the injection source

added benefit is that the transformer turns ratio n can be increased, to better match the injection source impedance to the impedance under test. Note that the impedances of the transformer, of the blocking capacitor, and of the probe and injection source return connections, do not affect the measurement. Much smaller impedances can therefore be measured using this improved approach.

8.6 Summary of Key Points

1. The magnitude Bode diagrams of functions which vary as $(f/f_0)^n$ have slopes equal to $20n$ dB per decade, and pass through 0 dB at $f = f_0$.
2. It is good practice to express transfer functions in normalized pole-zero form; this form directly exposes expressions for the salient features of the response, that is, the corner frequencies, reference gain, etc.
3. The right half-plane zero exhibits the magnitude response of the left half-plane zero, but the phase response of the pole.
4. Poles and zeroes can be expressed in frequency-inverted form when it is desirable to refer the gain to a high-frequency asymptote.
5. A two-pole response can be written in the standard normalized form of Eq. (8.58). When $Q > 0.5$, the poles are complex conjugates. The magnitude response then exhibits peaking in the vicinity of the corner frequency, with an exact value of Q at $f = f_0$. High Q also causes the phase to change sharply near the corner frequency.
6. When Q is less than 0.5, the two-pole response can be plotted as two real poles. The low- Q approximation predicts that the two poles occur at frequencies f_0/Q and Qf_0 . These frequencies are within 10% of the exact values for $Q \leq 0.3$.
7. When a circuit includes two damping elements, the composite Q -factor can be estimated as the “parallel combination” (inverse addition) of the Q -factors determined by the two elements individually. This estimation is within 10% of the exact value when the product of the individual Q -factors is greater than 5.
8. The low- Q approximation can be extended to find approximate roots of an arbitrary-degree polynomial. Approximate analytical expressions for the salient features can be derived. Numerical values are used to justify the approximations.
9. Salient features of the transfer functions of the buck, boost, and buck-boost converters are tabulated in Sect. 8.2.2. The line-to-output transfer functions of these converters contain two poles. Their control-to-output transfer functions contain two poles, and may additionally contain a right half-plane zero.
10. Approximate magnitude asymptotes of impedances and transfer functions can be easily derived by graphical construction. This approach is a useful supplement to conventional analysis, because it yields physical insight into the circuit behavior, and because it exposes suitable approximations. Several examples, including the impedances of basic series and parallel resonant circuits and the transfer function $H(s)$ of the voltage divider circuit, are worked in Sect. 8.3. The input impedance, output impedance, and transfer functions of the buck converter are constructed in Sect. 8.4, and physical origins of the asymptotes, corner frequencies, and Q -factor are found.
11. Measurement of transfer functions and impedances using a network analyzer is discussed in Sect. 8.5. Careful attention to ground connections is important when measuring small impedances.

PROBLEMS

- 8.1** Express the gains represented by the asymptotes of Fig. 8.64a–c in factored pole-zero form. You may assume that all poles and zeroes have negative real parts.

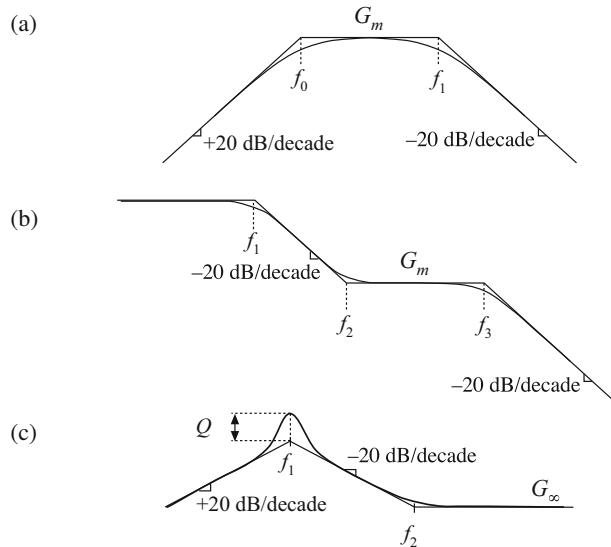
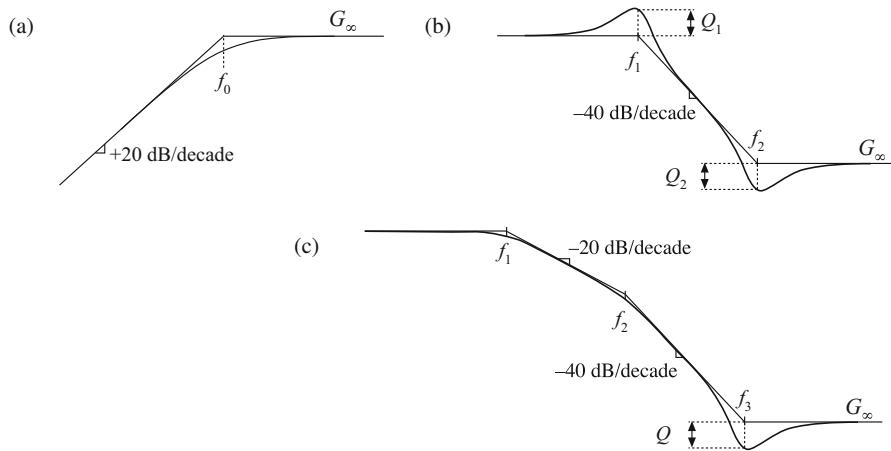
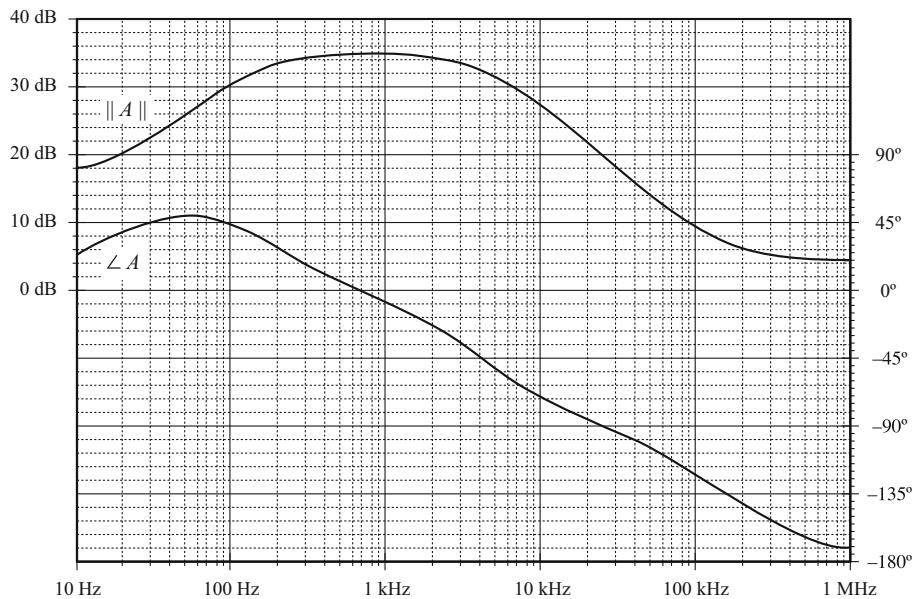


Fig. 8.64 Gain asymptotes for Problem 8.1

- 8.2** Express the gains represented by the asymptotes of Fig. 8.65a–c in factored pole-zero form. You may assume that all poles and zeroes have negative real parts.
- 8.3** Derive analytical expressions for the low-frequency asymptotes of the magnitude Bode plots shown in Fig. 8.65a–c.
- 8.4** Derive analytical expressions for the three magnitude asymptotes of Fig. 8.16.
- 8.5** An experimentally measured transfer function. Figure 8.66 contains experimentally measured magnitude and phase data for the gain function $A(s)$ of a certain amplifier. The object of this problem is to find an expression for $A(s)$. Overlay asymptotes as appropriate on the magnitude and phase data, and hence deduce numerical values for the gain asymptotes and corner frequencies of $A(s)$. Your magnitude and phase asymptotes must, of course, follow all of the rules: magnitude slopes must be multiples of ± 20 dB per decade, phase slopes for real poles must be multiples of $\pm 45^\circ$ per decade, etc. The phase and magnitude asymptotes must be consistent with each other.
It is suggested that you start by guessing $A(s)$ based on the magnitude data. Then construct the phase asymptotes for your guess, and compare them with the given data. If there are discrepancies, then modify your guess accordingly and redo your magnitude and phase asymptotes. You should turn in: (1) your analytical expression for $A(s)$, with numerical values given, and (2) a copy of Fig. 8.66, with your magnitude and phase asymptotes superimposed and with all break frequencies and slopes clearly labeled.

**Fig. 8.65** Gain asymptotes for Problems 8.2 and 8.3**Fig. 8.66** Experimentally measured magnitude and phase data, Problem 8.5

8.6 An experimentally measured impedance. Figure 8.67 contains experimentally measured magnitude and phase data for the driving-point impedance $Z(s)$ of a passive network. The object of this problem is to find an expression for $Z(s)$. Overlay asymptotes as appropriate on the magnitude and phase data, and hence deduce numerical values for the salient features of the impedance function. You should turn in: (1) your analytical expression for

$Z(s)$, with numerical values given, and (2) a copy of Fig. 8.67, with your magnitude and phase asymptotes superimposed and with all salient features and asymptote slopes clearly labeled.

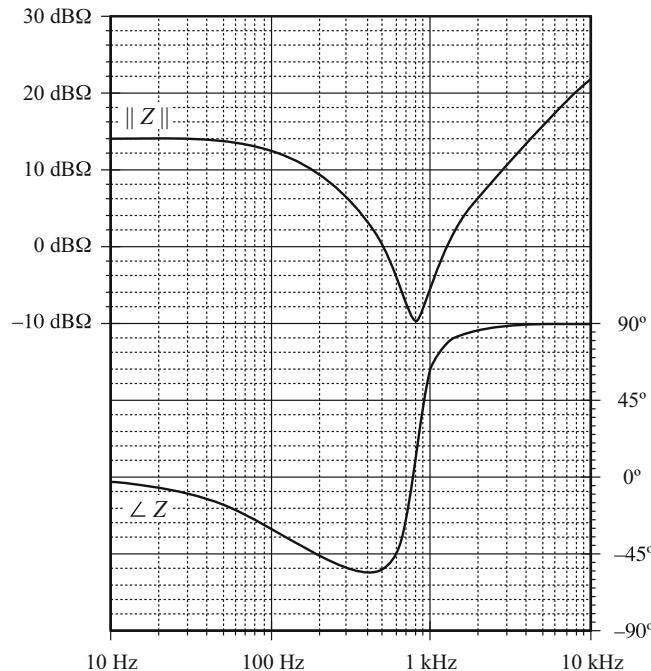
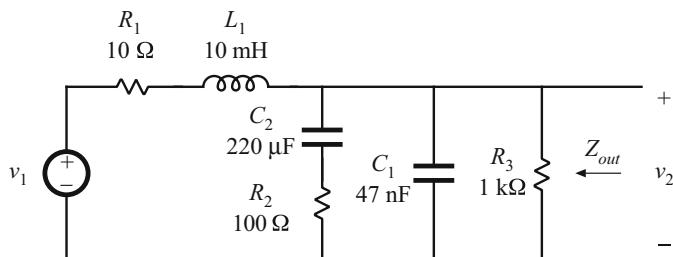


Fig. 8.67 Impedance magnitude and phase data, Problem 8.6

8.7 For the nonideal flyback converter modeled in Sect. 7.2.10:

- Derive analytical expressions for the control-to-output and line-to-output transfer functions $G_{vd}(s)$ and $G_{vg}(s)$. Express your results in standard normalized form.
 - Derive analytical expressions for the salient features of these transfer functions.
 - Construct the magnitude and phase Bode plots of the control-to-output transfer function, using the following values: $n = 2$, $V_g = 48 \text{ V}$, $D = 0.3$, $R = 5 \Omega$, $L = 250 \mu\text{H}$, $C = 100 \mu\text{F}$, $R_{on} = 1.2 \Omega$. Label the numerical values of the constant asymptotes, all corner frequencies, the Q -factor, and asymptote slopes.
- 8.8** Magnitude Bode diagram of an $R-L-C$ filter circuit. For the filter circuit of Fig. 8.68, construct the Bode plots for the magnitudes of the Thevenin-equivalent output impedance Z_{out} and the transfer function $H(s) = v_2/v_1$. Plot your results on semi-log graph paper. Give approximate analytical expressions and numerical values for the important corner frequencies and asymptotes. Do all of the elements significantly affect Z_{out} and H ?

Fig. 8.68 Filter circuit of Problem 8.8



- 8.9** Operational amplifier filter circuit. The op-amp circuit shown in Fig. 8.69 is a practical realization of what is known as a *PID controller*, and is sometimes used to modify the loop gain of feedback circuits to improve their performance. Using semi-log graph paper, sketch the Bode diagram of the magnitude of the transfer function $v_2(s)/v_1(s)$ of the circuit shown. Label all corner frequencies, flat asymptote gains, and asymptote slopes, as appropriate, giving both analytical expressions and numerical values. You may assume that the op-amp is ideal.

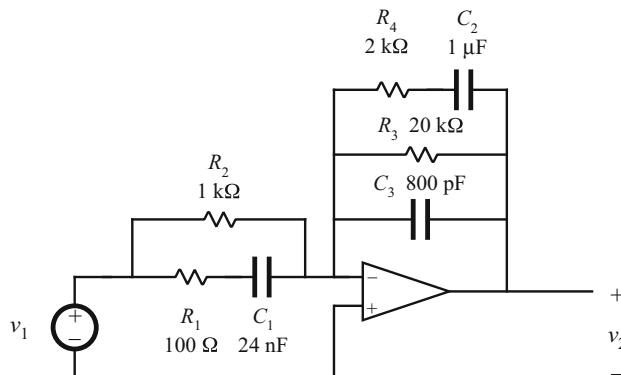
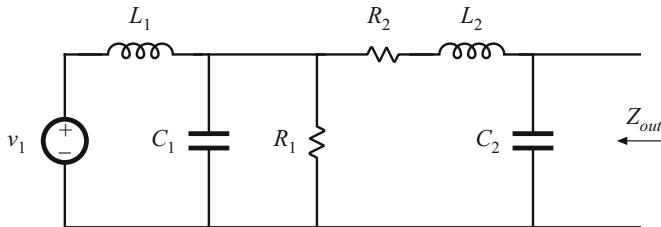
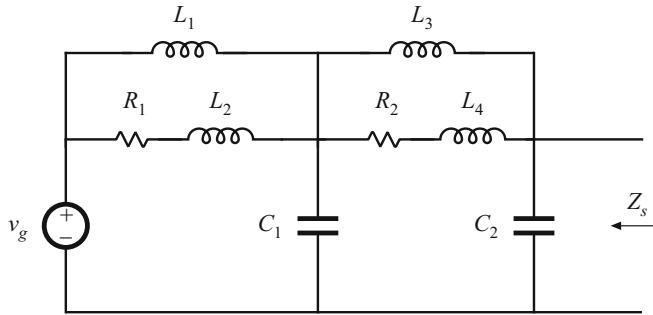


Fig. 8.69 Op-amp PID controller circuit, Problem 8.9

- 8.10** Phase asymptotes. Construct the phase asymptotes for the transfer function $v_2(s)/v_1(s)$ of Problem 8.9. Label all break frequencies, flat asymptotes, and asymptote slopes.
- 8.11** Construct the Bode diagram for the magnitude of the output impedance Z_{out} of the network shown in Fig. 8.70. Give suitable analytical expressions for each asymptote, corner frequency, and Q -factor, as appropriate. Justify any approximations that you use. The component values are: $L_1 = 100 \mu\text{H}$, $L_2 = 16 \text{ mH}$, $C_1 = 1000 \mu\text{F}$, $C_2 = 10 \mu\text{F}$, $R_1 = 5 \Omega$, $R_2 = 50 \Omega$

**Fig. 8.70** Filter network of Problem 8.11**Fig. 8.71** Input filter circuit of Problem 8.12

- 8.12** The two section input filter in the circuit of Fig. 8.71 should be designed such that its output impedance $Z_{out}|_{v_g = 0}$ meets certain input filter design criteria, and hence it is desirable to construct the Bode plot for the magnitude of Z_s . Although this filter contains six reactive elements, $\|Z_s\|$ can nonetheless be constructed in a relatively straightforward manner using graphical construction techniques. The element values are:

$$\begin{array}{ll} L_1 = 32\text{mH} & C_1 = 32\text{\mu F} \\ L_2 = 400\text{\mu H} & C_2 = 6.8\text{\mu F} \\ L_3 = 800\text{\mu H} & R_1 = 10\Omega \\ L_4 = 1\text{\mu H} & R_2 = 1\Omega \end{array}$$

- (a) Construct $\|Z_s\|$ using the “algebra on the graph” method. Give simple approximate analytical expressions for all asymptotes and corner frequencies.
 - (b) It is desired that $\|Z_s\|$ be approximately equal to 5Ω at 500 Hz and 2.5Ω at 1 kHz . Suggest a simple way to accomplish this by changing the value of one component.
- 8.13** Construct the Bode plot of the magnitude of the output impedance of the filter illustrated in Fig. 8.72. Give approximate analytical expressions for each corner frequency. No credit will be given for computer-generated plots.

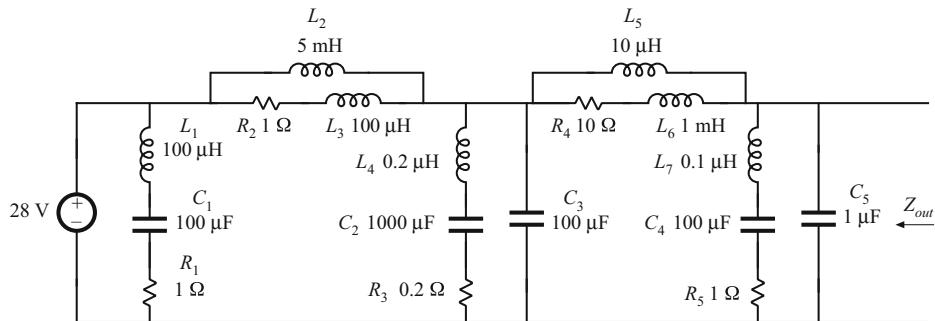


Fig. 8.72 Input filter circuit of Problem 8.13

- 8.14** A certain open-loop buck-boost converter contains an input filter. Its small-signal ac model is shown in Fig. 8.73, and the element values are specified below. Construct the Bode plot for the magnitude of the converter output impedance $\|Z_{out}(s)\|$. Label the values of all important corner frequencies and asymptotes.

$$\begin{array}{ll} D = 0.6 & L_f = 150 \mu\text{H} \\ R = 6 \Omega & C_f = 16 \mu\text{F} \\ C = 0.33 \mu\text{F} & C_b = 2200 \mu\text{F} \\ L = 25 \mu\text{H} & R_f = 1 \Omega \end{array}$$

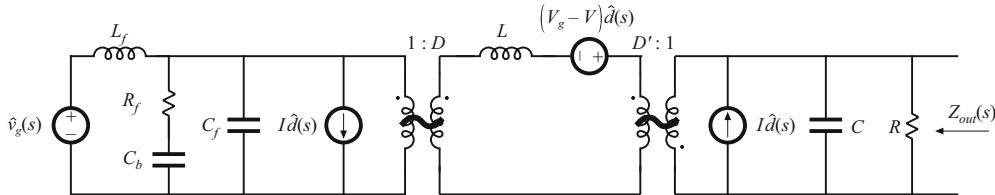


Fig. 8.73 Small-signal model of a buck converter with input filter, Problem 8.14

- 8.15** In Sect. 7.2.10, the small-signal ac model of a nonideal flyback converter is derived, with the result illustrated in Fig. 7.28. Construct a Bode plot of the magnitude and phase of the converter output impedance $Z_{out}(s)$. Give both analytical expressions and numerical values for all important features in your plot. Note: $Z_{out}(s)$ includes the load resistance R . The element values are: $D = 0.4$, $n = 0.2$, $R = 6 \Omega$, $L = 600 \mu\text{H}$, $C = 100 \mu\text{F}$, $R_{on} = 5 \Omega$.
- 8.16** The small-signal equations of the Watkins-Johnson converter operating in continuous conduction mode are:

$$\begin{aligned} L \frac{d\hat{i}(t)}{dt} &= -D\hat{v}(t) + (2V_g - V)\hat{d}(t) + (D - D')\hat{v}_g(t) \\ C \frac{d\hat{v}(t)}{dt} &= D\hat{i}(t) - \frac{\hat{v}(t)}{R} \\ \hat{i}_g(t) &= (D - D')\hat{i}(t) + 2I\hat{d}(t) \end{aligned}$$

- (a) Derive analytical expressions for the line-to-output transfer function $G_{vg}(s)$ and the control-to-output transfer function $G_{vd}(s)$.
- (b) Derive analytical expressions for the salient features (dc gains, corner frequencies, and Q -factors) of the transfer functions $G_{vg}(s)$ and $G_{vd}(s)$. Express your results as functions of V_g , D , R , L , and C .
- (c) The converter operates at $V_g = 28 \text{ V}$, $D = 0.25$, $R = 28 \Omega$, $C = 100 \mu\text{F}$, $L = 400 \mu\text{H}$. Sketch the Bode diagram of the magnitude and phase of $G_{vd}(s)$. Label salient features.

8.17 The element values in the buck converter of Fig. 7.55 are:

$$\begin{array}{ll} V_g = 120 \text{ V} & D = 0.6 \\ R = 10 \Omega & R_g = 2 \Omega \\ L = 550 \mu\text{H} & C = 100 \mu\text{F} \end{array}$$

- (a) Determine an analytical expression for the control-to-output transfer function $G_{vg}(s)$ of this converter.
- (b) Find analytical expressions for the salient features of $G_{vg}(s)$.
- (c) Construct magnitude and phase asymptotes for G_{vg} . Label the numerical values of all slopes and other important features.

8.18 The LCC resonant inverter circuit contains the following transfer function:

$$H(s) = \frac{sC_1R}{1 + sR(C_1 + C_2) + s^2LC_1 + s^3LC_1C_2R}$$

- (a) When C_1 is sufficiently large, this transfer function can be expressed as an inverted pole and a quadratic pole pair. Derive analytical expressions for the corner frequencies and Q -factor in this case, and sketch typical magnitude asymptotes. Determine analytical conditions for validity of your approximation.
- (b) When C_2 is sufficiently large, the transfer function can be also expressed as an inverted pole and a quadratic pole pair. Derive analytical expressions for the corner frequencies and Q -factor in this case, and sketch typical magnitude asymptotes. Determine analytical conditions for validity of your approximation in this case.
- (c) When $C_1 = C_2$ and when the quadratic poles have sufficiently high Q , then the transfer function can again be expressed as an inverted pole and a quadratic pole pair. Derive analytical expressions for the corner frequencies and Q -factor in this case, and sketch typical magnitude asymptotes. Determine analytical conditions for validity of your approximation in this case.

8.19 A two-section $L - C$ filter has the following transfer function:

$$G(s) = \frac{1}{1 + s\left(\frac{L_1 + L_2}{R}\right) + s^2(L_1(C_1 + C_2) + L_2C_2) + s^3\left(\frac{L_1L_2C_1}{R}\right) + s^4(L_1L_2C_1C_2)}$$

The element values are:

$$\begin{array}{ll} R = 50 \text{ m}\Omega & \\ C_1 = 680 \mu\text{F} & C_2 = 4.7 \mu\text{F} \\ L_1 = 500 \mu\text{H} & L_2 = 50 \mu\text{H} \end{array}$$

- (a) Use the above numerical values to determine how to factor $G(s)$ into approximate real and quadratic poles, as appropriate. Give approximate analytical expressions for the salient features that are valid for the above numerical values.
- (b) Construct the magnitude and phase asymptotes of $G(s)$.
- (c) It is desired to reduce the Q to 2, without significantly changing the corner frequencies or other features of the response. It is possible to do this by changing only two element values. Specify how to accomplish this.

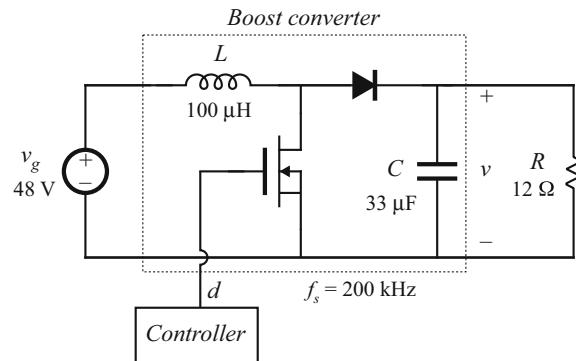


Fig. 8.74 Boost converter of Problem 8.20

- 8.20** The boost converter of Fig. 8.74 operates in the continuous conduction mode, with quiescent duty cycle $D = 0.6$. On semi-log axes, construct the magnitude and phase Bode plots of
- (a) the control-to-output transfer function $G_{vd}(s)$,
 - (b) the line-to-output transfer function $G_{vg}(s)$,
 - (c) the output impedance $Z_{out}(s)$, and
 - (d) the input impedance $Z_{in}(s)$.
- On each plot, label the corner frequencies and asymptotes.

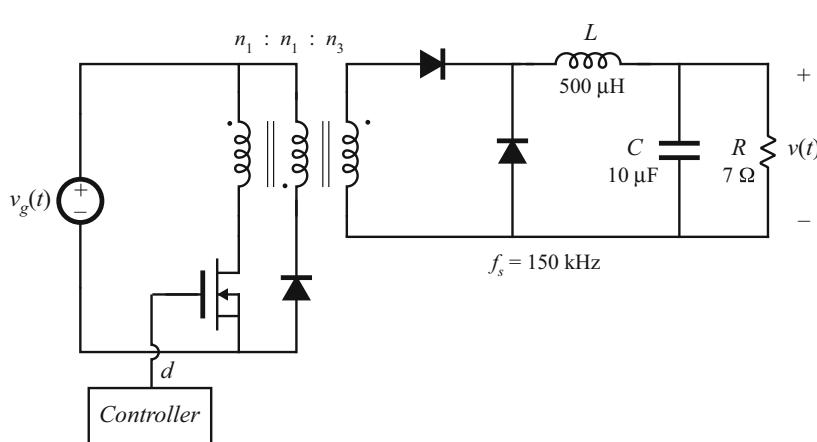


Fig. 8.75 Forward converter of Problem 8.21

- 8.21** The forward converter of Fig. 8.75 operates in the continuous conduction mode, with the quiescent values $V_g = 380$ V and $V = 28$ V. The transformer turns ratio is $n_1/n_3 = 4.5$. On semi-log axes, construct the magnitude and phase Bode plots of
 (a) the control-to-output transfer function $G_{vd}(s)$, and
 (b) the line-to-output transfer function $G_{vg}(s)$.

On each plot, label the corner frequencies and asymptotes. Hint: other than introduction of the turns ratio n_1/n_3 , the transformer does not significantly affect the small-signal behavior of the forward converter.

- 8.22** Loss mechanisms in capacitors, such as dielectric loss and contact and foil resistance, can be modeled electrically using an *equivalent series resistance* (ESR). Capacitors whose dielectric materials exhibit a high dielectric constant, such as electrolytic capacitors, tantalum capacitors, and some types of multi-layer ceramic capacitors, typically exhibit relatively high ESR.

A buck converter contains a 1.6 mH inductor, and operates with a quiescent duty cycle of 0.5. Its output capacitor can be modeled as a 16 μF capacitor in series with a 0.2 Ω ESR. The load resistance is 10 Ω . The converter operates in continuous conduction mode. The quiescent input voltage is $V_g = 120$ V.

- Determine an analytical expression for the control-to-output transfer function $G_{vg}(s)$ of this converter.
- Find analytical expressions for the salient features of $G_{vg}(s)$.
- Construct magnitude and phase asymptotes for G_{vg} . Label the numerical values of all slopes and other important features.

- 8.23** The boost converter of Fig. 8.76 operates in the continuous conduction mode, with the following quiescent values: $V_g = 120$ V, $V = 300$ V. It is desired to control the converter input current waveform, and hence it is necessary to determine the small-signal transfer function

$$G_{id}(s) = \left. \frac{\hat{i}_g(s)}{\hat{d}(s)} \right|_{\hat{v}_g(s)=0}$$

- Derive an analytical expression for $G_{id}(s)$. Express all poles and zeroes in normalized standard form, and give analytical expressions for the corner frequencies, Q -factor, and dc gain.
- On semi-log axes, construct the Bode plot for the magnitude and phase of $G_{id}(s)$.

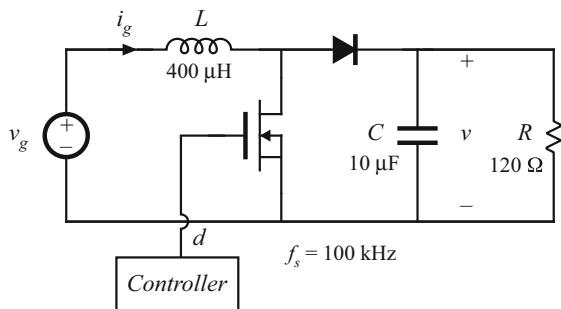


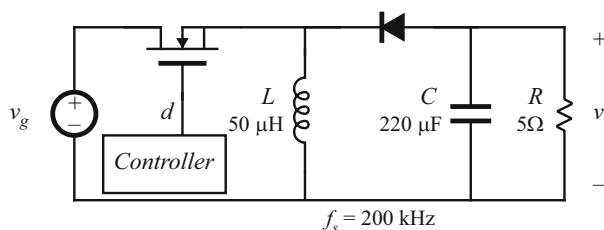
Fig. 8.76 Boost converter of Problem 8.23

8.24 The buck-boost converter of Fig. 8.77 operates in the continuous conduction mode, with the following quiescent values: $V_g = 48 \text{ V}$, $V = -24 \text{ V}$. On semi-log axes, construct the magnitude and phase Bode plots of:

- the control-to-output transfer function $G_{vd}(s)$, and
- the output impedance $Z_{out}(s)$.

On each plot, label the corner frequencies and asymptotes as appropriate.

Fig. 8.77 Buck-boost converter of Problem 8.24





Controller Design

9.1 Introduction

In all switching converters, the output voltage $v(t)$ is a function of the input line voltage $v_g(t)$, the duty cycle $d(t)$, and the load current $i_{load}(t)$, as well as the converter circuit element values. In a dc–dc converter application, it is desired to obtain a constant output voltage $v(t) = V$, in spite of disturbances in $v_g(t)$ and $i_{load}(t)$, and in spite of variations in the converter circuit element values. The sources of these disturbances and variations are many, and a typical situation is illustrated in Fig. 9.1. The input voltage $v_g(t)$ of an off-line power supply may typically contain periodic variations at the second harmonic of the ac power system frequency (100 Hz or 120 Hz), produced by a rectifier circuit. The magnitude of $v_g(t)$ may also vary when neighboring power system loads are switched on or off. The load current $i_{load}(t)$ may contain variations of significant amplitude, and a typical power supply specification is that the output voltage must remain within a specified range (for example, $3.3 \text{ V} \pm 0.05 \text{ V}$) when the load current takes a step change from, for example, full rated load current to 50% of the rated current, and vice versa. The values of the circuit elements are constructed to a certain tolerance, and so in high-volume manufacturing of a converter, converters are constructed whose output voltages lie in some distribution. It is desired that essentially all of this distribution fall within the specified range; however, this is not practical to achieve without the use of negative feedback. Similar considerations apply to inverter applications, except that the output voltage is ac.

So we cannot expect to simply set the dc–dc converter duty cycle to a single value, and obtain a given constant output voltage under all conditions. The idea behind the use of negative feedback is to build a circuit that automatically adjusts the duty cycle as necessary, to obtain the desired output voltage with high accuracy, regardless of disturbances in $v_g(t)$ or $i_{load}(t)$ or variations in component values. This is a useful thing to do whenever there are variations and unknowns that otherwise prevent the system from attaining the desired performance.

A block diagram of a feedback system is shown in Fig. 9.2. The output voltage $v(t)$ is measured, using a “sensor” with gain $H(s)$. In a dc voltage regulator or dc–ac inverter, the sensor circuit is usually a voltage divider, comprised of precision resistors. The sensor output signal $H(s)v(s)$ is compared with a reference input voltage $v_{ref}(s)$. The objective is to make $H(s)v(s)$ equal to $v_{ref}(s)$, so that $v(s)$ accurately follows $v_{ref}(s)$ regardless of disturbances or component variations in the compensator, pulse-width modulator, gate driver, or converter power stage.

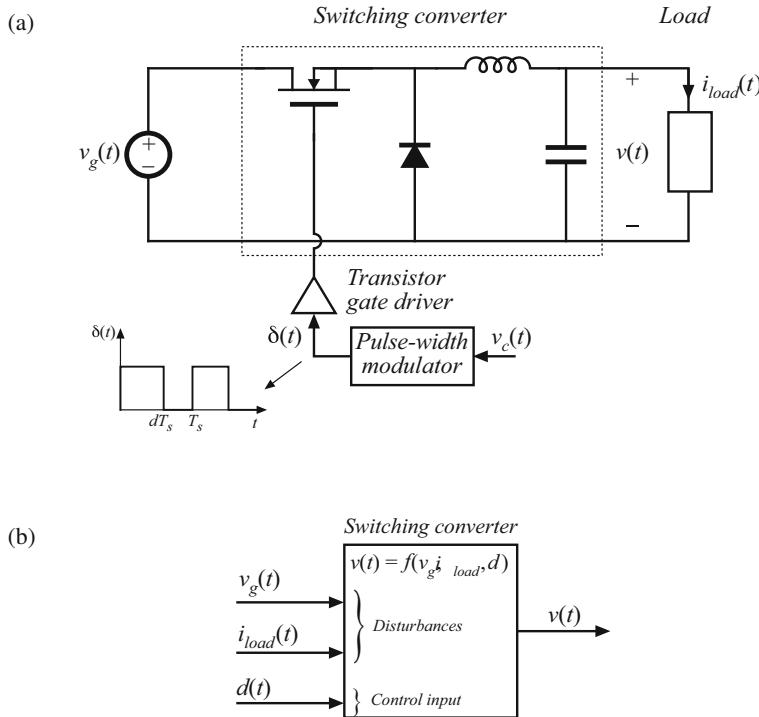


Fig. 9.1 The output voltage of a typical switching converter is a function of the line input voltage v_g , the duty cycle d , and the load current i_{load} : (a) open-loop buck converter; (b) functional diagram illustrating dependence of v on the independent quantities v_g , d , and i_{load}

The difference between the reference input $v_{ref}(s)$ and the sensor output $H(s)v(s)$ is called the error signal $v_e(s)$. If the feedback system works perfectly, then $v_{ref}(s) = H(s)v(s)$, and hence the error signal is zero. In practice, the error signal is usually nonzero but nonetheless small. Obtaining a small error is one of the objectives in adding a compensator network $G_c(s)$ as shown in Fig. 9.2. Note that the transfer function from the error signal $v_e(s)$ to the output voltage $v(s)$ is equal to the gains of the compensator, pulse-width modulator, and converter power stage. If the compensator gain $G_c(s)$ is large enough in magnitude, then a small error signal can produce the required output voltage $v(t) = V$ for a dc regulator (Q : how should H and v_{ref} then be chosen?). So a large compensator gain leads to a small error, and therefore the output follows the reference input with good accuracy. This is the key idea behind feedback systems.

The averaged small-signal converter models derived in Chap. 7 are used in the following sections to find the effects of feedback on the small-signal transfer functions of the regulator. The loop gain $T(s)$ is defined as the product of the small-signal gains in the forward and feedback paths of the feedback loop. It is found that the transfer function from a disturbance to the output is multiplied by the factor $1/(1 + T(s))$. Hence, when the loop gain T is large in magnitude, then the influence of disturbances on the output voltage is small. A large loop gain also causes the output voltage $v(s)$ to be nearly equal to $v_{ref}(s)/H(s)$, with very little dependence on the

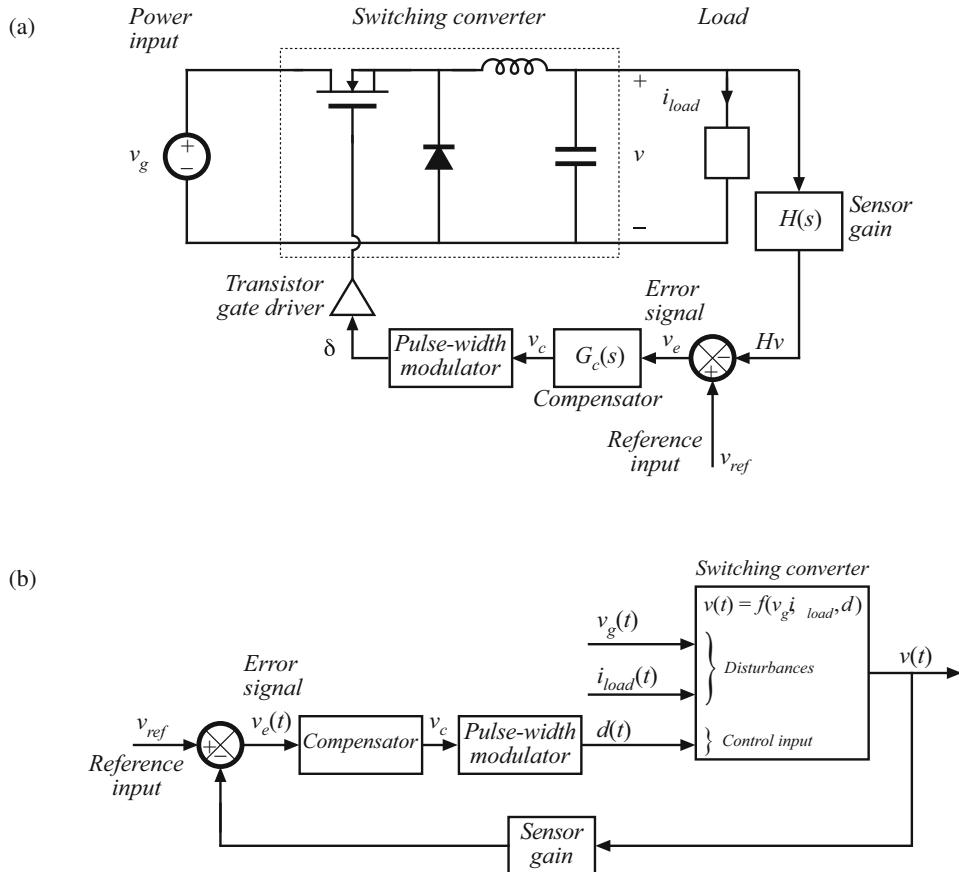


Fig. 9.2 Feedback loop for regulation of the output voltage: (a) buck converter, with feedback loop block diagram; (b) functional block diagram of the feedback system

gains in the forward path of the feedback loop. So the loop gain magnitude $\| T \|$ is a measure of how well the feedback system works. All of these gains can be easily constructed using the algebra-on-the-graph method; this allows easy evaluation of important closed-loop performance measures, such as the output voltage ripple resulting from 120 Hz rectification ripple in $v_g(t)$ or the closed-loop output impedance.

Stability is another important issue in feedback systems. Adding a feedback loop can cause an otherwise well-behaved circuit to exhibit oscillations, ringing and overshoot, and other undesirable behavior. An in-depth treatment of stability is beyond the scope of this book; however, the simple phase margin criterion for assessing stability is used here. When the phase margin of the loop gain T is positive, then the feedback system is stable. Moreover, increasing the phase margin causes the system transient response to be better behaved, with less overshoot and ringing. The relation between phase margin and closed-loop response is quantified in Sect. 9.4.

An example is given in Sect. 9.5, in which a compensator network is designed for a dc regulator system. The compensator network is designed to attain adequate phase margin and good

rejection of expected disturbances. Lead compensators and $P-D$ controllers are used to improve the phase margin and extend the bandwidth of the feedback loop. This leads to better rejection of high-frequency disturbances. Lag compensators and $P-I$ controllers are used to increase the low-frequency loop gain. This leads to better rejection of low-frequency disturbances and very small steady-state error. More complicated compensators can achieve the advantages of both approaches.

Injection methods for experimental measurement of loop gain are introduced in Sect. 9.6. The use of voltage or current injection solves the problem of establishing the correct quiescent operating point in high-gain systems. Conditions for obtaining an accurate measurement are exposed. The injection method also allows measurement of the loop gains of unstable systems.

9.2 Effect of Negative Feedback on the Network Transfer Functions

We have seen how to derive the small-signal ac transfer functions of a switching converter. For example, the equivalent circuit model of the buck converter can be written as in Fig. 9.3. This equivalent circuit contains three independent inputs: the control input variations \hat{d} , the power input voltage variations \hat{v}_g , and the load current variations \hat{i}_{load} . The output voltage variation \hat{v} can therefore be expressed as a linear combination of the three independent inputs, as follows:

$$\hat{v}(s) = G_{vd}(s)\hat{d}(s) + G_{vg}(s)\hat{v}_g(s) - Z_{out}(s)\hat{i}_{load}(s) \quad (9.1)$$

where

$$G_{vd}(s) = \left. \frac{\hat{v}(s)}{\hat{d}(s)} \right|_{\begin{subarray}{l} \hat{v}_g=0 \\ \hat{i}_{load}=0 \end{subarray}} \quad \text{converter control-to-output transfer function} \quad (9.1a)$$

$$G_{vg}(s) = \left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\begin{subarray}{l} \hat{d}=0 \\ \hat{i}_{load}=0 \end{subarray}} \quad \text{converter line-to-output transfer function} \quad (9.1b)$$

$$Z_{out}(s) = -\left. \frac{\hat{v}(s)}{\hat{i}_{load}(s)} \right|_{\begin{subarray}{l} \hat{v}_g=0 \\ \hat{d}=0 \end{subarray}} \quad \text{converter output impedance} \quad (9.1c)$$

The Bode diagrams of these quantities are constructed in Chap. 8. Equation (9.1) describes how disturbances v_g and i_{load} propagate to the output v , through the transfer function $G_{vg}(s)$ and the output impedance $Z_{out}(s)$. If the disturbances v_g and i_{load} are known to have some maximum worst-case amplitude, then Eq. (9.1) can be used to compute the resulting worst-case open-loop variation in v .

As described previously, the feedback loop of Fig. 9.2 can be used to reduce the influences of v_g and i_{load} on the output v . To analyze this system, let us perturb and linearize its averaged signals about their quiescent operating points. Both the power stage and the control block diagram are perturbed and linearized:

$$v_{ref}(t) = V_{ref} + \hat{v}_{ref}(t) \quad (9.2)$$

$$v_e(t) = V_e + \hat{v}_e(t)$$

etc.

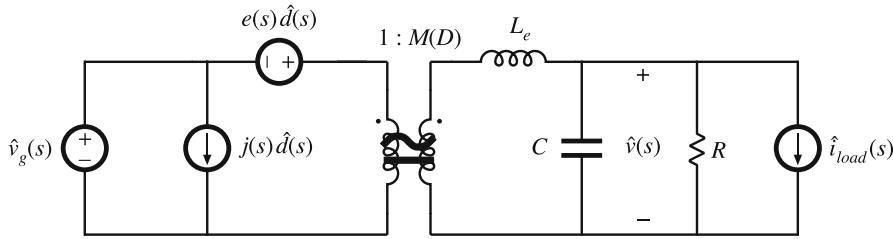


Fig. 9.3 Small-signal converter model, which represents variations in v_g , d , and i_{load}

In a dc regulator system, the reference input is constant, so $\hat{v}_{ref}(t) = 0$. In a switching amplifier or dc-ac inverter, the reference input may contain an ac variation. In Fig. 9.4a, the converter model of Fig. 9.3 is combined with the perturbed and linearized control circuit block diagram. This is equivalent to the reduced block diagram of Fig. 9.4b, in which the converter model has been replaced by blocks representing Eq. (9.1).

Solution of Fig. 9.4b for the output voltage variation v yields

$$\hat{v} = \hat{v}_{ref} \frac{G_c G_{vd}/V_M}{1 + HG_c G_{vd}/V_M} + \hat{v}_g \frac{G_{vg}}{1 + HG_c G_{vd}/V_M} - \hat{i}_{load} \frac{Z_{out}}{1 + HG_c G_{vd}/V_M} \quad (9.3)$$

which can be written in the form

$$\hat{v} = \hat{v}_{ref} \frac{1}{H} \frac{T}{1+T} + \hat{v}_g \frac{G_{vg}}{1+T} - \hat{i}_{load} \frac{Z_{out}}{1+T} \quad (9.4)$$

with

$$T(s) = H(s)G_c(s)G_{vd}(s)/V_M = \text{"loop gain"}$$

Equation (9.4) is a general result. The loop gain $T(s)$ is defined in general as the product of the gains around the forward and feedback paths of the loop. This equation shows how the addition of a feedback loop modifies the transfer functions and performance of the system, as described in detail below.

9.2.1 Feedback Reduces the Transfer Functions from Disturbances to the Output

The transfer function from v_g to v in the open-loop buck converter of Fig. 9.3 is $G_{vg}(s)$, as given in Eq. (9.1). When feedback is added, this transfer function becomes

$$\left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\substack{\hat{v}_{ref}=0 \\ \hat{i}_{load}=0}} = \frac{G_{vg}(s)}{1 + T(s)} \quad (9.5)$$

from Eq. (9.4). So this transfer function is reduced via feedback by the factor $1/(1 + T(s))$. If the loop gain $T(s)$ is large in magnitude, then the reduction can be substantial. Hence, the output voltage variation v resulting from a given v_g variation is attenuated by the feedback loop.

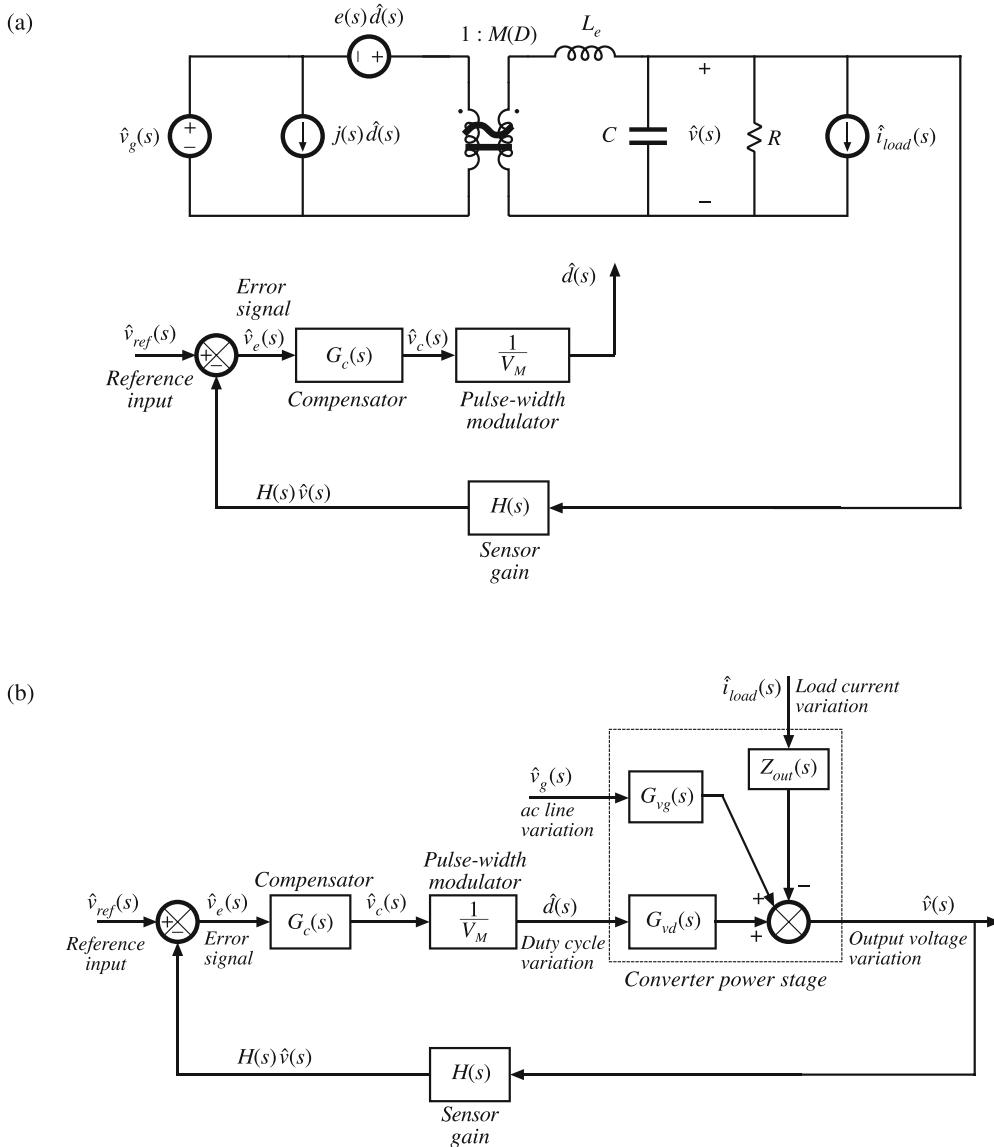


Fig. 9.4 Voltage regulator system small-signal model: (a) with converter equivalent circuit; (b) complete block diagram

Equation (9.4) also predicts that the converter output impedance is reduced, from $Z_{out}(s)$ to

$$\left. \frac{\hat{v}(s)}{-\hat{i}_{load}(s)} \right|_{\begin{subarray}{l} \hat{v}_g=0 \\ \hat{v}_{ref}=0 \end{subarray}} = \frac{Z_{out}(s)}{1 + T(s)} \quad (9.6)$$

So the feedback loop also reduces the converter output impedance by a factor of $1/(1 + T(s))$, and the influence of load current variations on the output voltage is reduced.

9.2.2 Feedback Causes the Transfer Function from the Reference Input to the Output to Be Insensitive to Variations in the Gains in the Forward Path of the Loop

According to Eq. (9.4), the closed-loop transfer function from v_{ref} to v is

$$\frac{\hat{v}(s)}{\hat{v}_{ref}(s)} \Bigg|_{\begin{subarray}{l} \hat{v}_g=0 \\ \hat{i}_{load}=0 \end{subarray}} = \frac{1}{H(s)} \frac{T(s)}{1 + T(s)} \quad (9.7)$$

If the loop gain is large in magnitude, that is, $\|T\| \gg 1$, then $(1 + T) \approx T$ and $T/(1 + T) \approx T/T = 1$. The transfer function then becomes

$$\frac{\hat{v}(s)}{\hat{v}_{ref}(s)} \approx \frac{1}{H(s)} \quad (9.8)$$

which is independent of $G_c(s)$, V_M , and $G_{vd}(s)$. So provided that the loop gain is large in magnitude, then variations in $G_c(s)$, V_M , and $G_{vd}(s)$ have negligible effect on the output voltage. Of course, in the dc regulator application, $v_{ref}(t)$ is constant and $\hat{v}_{ref} = 0$. But Eq. (9.8) applies equally well to the dc values. For example, if the system is linear, then we can write

$$\frac{V}{V_{ref}} = \frac{1}{H(0)} \frac{T(0)}{1 + T(0)} \approx \frac{1}{H(0)} \quad (9.9)$$

So to make the dc output voltage V accurately follow the dc reference V_{ref} , we need only ensure that the dc sensor gain $H(0)$ and dc reference V_{ref} are well known and accurate, and that $T(0)$ is large. Precision resistors are normally used to realize H , but components with tightly controlled values need not be used in G_c , the pulse-width modulator, or the power stage. The sensitivity of the output voltage to the gains in the forward path is reduced, while the sensitivity of v to the feedback gain H and the reference input v_{ref} is increased.

9.3 Construction of the Important Quantities $1/(1 + T)$ and $T/(1 + T)$ and the Closed-Loop Transfer Functions

The transfer functions in Eqs. (9.4) to (9.9) can be easily constructed using the algebra-on-the-graph method [81]. Let us assume that we have analyzed the blocks in our feedback system, and have plotted the Bode diagram of $\|T(s)\|$. To use a concrete example, suppose that the result is given in Fig. 9.5, for which $T(s)$ is

$$T(s) = T_0 \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{Q\omega_{p1}} + \left(\frac{s}{\omega_{p1}}\right)^2\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \quad (9.10)$$

This example appears somewhat complicated. But the loop gains of practical voltage regulators are often even more complex, and may contain four, five, or more poles. Evaluation of Eqs. (9.5)

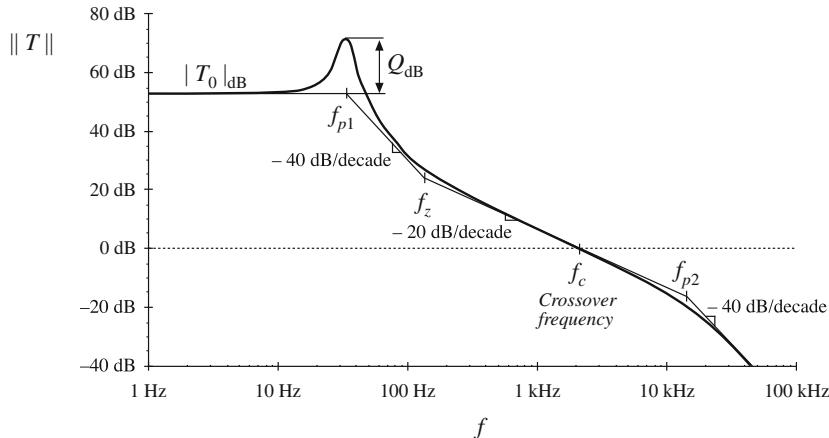


Fig. 9.5 Magnitude of the loop gain example, Eq. (9.10)

to (9.7), to determine the closed-loop transfer functions, requires quite a bit of work. The loop gain T must be added to 1, and the resulting numerator and denominator must be refactored. Using this approach, it is difficult to obtain physical insight into the relationship between the closed-loop transfer functions and the loop gain. In consequence, design of the feedback loop to meet specifications is difficult.

Using the algebra-on-the-graph method, the closed-loop transfer functions can be constructed by inspection, and hence the relation between these transfer functions and the loop gain becomes obvious. Let us first investigate how to plot $\|T/(1+T)\|$. It can be seen from Fig. 9.5 that there is a frequency f_c , called the “crossover frequency,” where $\|T\| = 1$. At frequencies less than f_c , $\|T\| > 1$; indeed, $\|T\| \gg 1$ for $f \ll f_c$. Hence, at low frequency, $(1+T) \approx T$, and $T/(1+T) \approx T/T = 1$. At frequencies greater than f_c , $\|T\| < 1$, and $\|T\| \ll 1$ for $f \gg f_c$. So at high frequency, $(1+T) \approx 1$ and $T/(1+T) \approx T/1 = T$. So we have

$$\frac{T}{1+T} \approx \begin{cases} 1 & \text{for } \|T\| \gg 1 \\ T & \text{for } \|T\| \ll 1 \end{cases} \quad (9.11)$$

The asymptotes corresponding to Eq. (9.11) are relatively easy to construct. The low-frequency asymptote, for $f < f_c$, is 1 or 0 dB. The high-frequency asymptotes, for $f > f_c$, follow T . The result is shown in Fig. 9.6.

So at low frequency, where $\|T\|$ is large, the reference-to-output transfer function is

$$\frac{\hat{v}(s)}{\hat{v}_{ref}(s)} = \frac{1}{H(s)} \frac{T(s)}{1+T(s)} \approx \frac{1}{H(s)} \quad (9.12)$$

This is the desired behavior, and the feedback loop works well at frequencies where $\|T\|$ is large. At high frequency ($f \gg f_c$) where $\|T\|$ is small, the reference-to-output transfer function is

$$\frac{\hat{v}(s)}{\hat{v}_{ref}(s)} = \frac{1}{H(s)} \frac{T(s)}{1+T(s)} \approx \frac{T(s)}{H(s)} = \frac{G_c(s)G_{vd}(s)}{V_M} \quad (9.13)$$

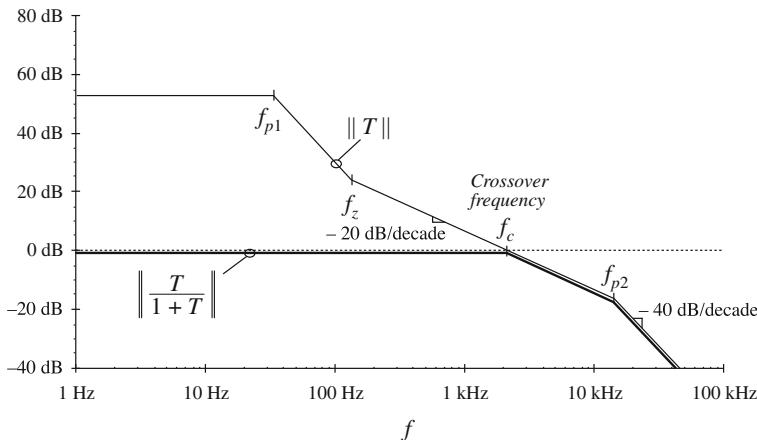


Fig. 9.6 Graphical construction of the asymptotes of $\|T/(1+T)\|$. Exact curves are omitted

This is not the desired behavior; in fact, this is the gain with the feedback connection removed ($H \rightarrow 0$). At high frequencies, the feedback loop is unable to reject the disturbance because the bandwidth of T is limited. The reference-to-output transfer function can be constructed on the graph by multiplying the $T/(1+T)$ asymptotes of Fig. 9.6 by $1/H$.

Thus, the crossover frequency f_c represents the bandwidth of the feedback system, and within this bandwidth the closed-loop behavior is improved. Further, it can be observed from Fig. 9.6 that feedback moves the poles of the system: T contains two poles at frequency f_{p1} that are not present in $T/(1+T)$, and instead $T/(1+T)$ contains a pole at frequency f_c . It can be shown that one of the poles of T is moved from frequency f_{p1} to approximately f_z , where it cancels the zero. The second pole at f_{p1} is moved to approximately f_c . Figure 9.6 illustrates how, within the bandwidth of the feedback loop, the frequencies of the poles are increased and their Q -factors are changed.

We can plot the asymptotes of $\|1/(1+T)\|$ using similar arguments. At low frequencies where $\|T\| \gg 1$, then $(1+T) \approx T$, and hence $1/(1+T) \approx 1/T$. At high frequencies where $\|T\| \ll 1$, then $(1+T) \approx 1$ and $1/(1+T) \approx 1$. So we have

$$\frac{1}{1+T(s)} \approx \begin{cases} \frac{1}{T(s)} & \text{for } \|T\| \gg 1 \\ 1 & \text{for } \|T\| \ll 1 \end{cases} \quad (9.14)$$

The asymptotes for the $T(s)$ example of Fig. 9.5 are plotted in Fig. 9.7.

At low frequencies where $\|T\|$ is large, the disturbance transfer function from v_g to v is

$$\frac{\hat{v}(s)}{\hat{v}_g(s)} = \frac{G_{vg}(s)}{1+T(s)} \approx \frac{G_{vg}(s)}{T(s)} \quad (9.15)$$

Again, $G_{vg}(s)$ is the original transfer function, with no feedback. The closed-loop transfer function has magnitude reduced by the factor $1/\|T\|$. So if, for example, we want to reduce this transfer function by a factor of 20 at 120 Hz, then we need a loop gain $\|T\|$ of at least $20 \Rightarrow 26 \text{ dB}$ at 120 Hz. The disturbance transfer function from v_g to v can be constructed on the graph, by multiplying the asymptotes of Fig. 9.7 by the asymptotes for $G_{vg}(s)$.

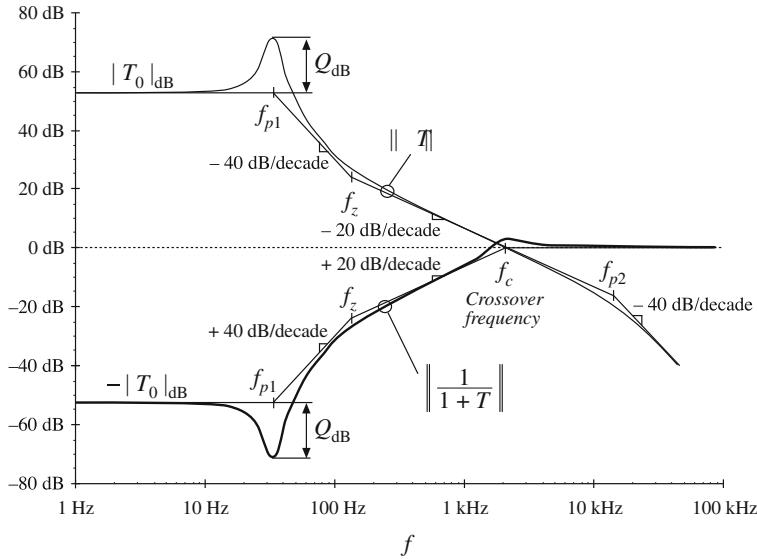


Fig. 9.7 Graphical construction of $\|1/(1+T)\|$

Similar arguments apply to the output impedance. The closed-loop output impedance at low frequencies is

$$\frac{\hat{v}(s)}{-\hat{i}_{load}(s)} = \frac{Z_{out}(s)}{1+T(s)} \approx \frac{Z_{out}(s)}{T(s)} \quad (9.16)$$

The output impedance is also reduced in magnitude by a factor of $1/\|T\|$ at frequencies below the crossover frequency.

At high frequencies ($f > f_c$) where $\|T\|$ is small, then $1/(1+T) \approx 1$, and

$$\begin{aligned} \frac{\hat{v}(s)}{\hat{v}_g(s)} &= \frac{G_{vg}(s)}{1+T(s)} \approx G_{vg}(s) \\ \frac{\hat{v}(s)}{-\hat{i}_{load}(s)} &= \frac{Z_{out}(s)}{1+T(s)} \approx Z_{out}(s) \end{aligned} \quad (9.17)$$

This is the same as the original disturbance transfer function and output impedance. So the feedback loop has essentially no effect on the disturbance transfer functions at frequencies above the crossover frequency.

Figure 9.8a illustrates an example of a buck converter having a loop gain $T(s)$ given by

$$T(s) = H(s)G_{vd}(s)/V_M \quad (9.18)$$

This simple example contains no compensator. The $L-C$ filter of the buck converter introduces resonant poles at frequency $f = f_{p1}$, and the capacitor equivalent series resistance R_C leads to a zero at frequency f_z . The feedback sensor block $H(s)$ contains a high-frequency pole at $f = f_{p2}$. Hence, this example exhibits a loop gain $T(s)$ identical to Eq. (9.10); let us assume that the element values lead to the magnitude plotted in Fig. 9.5. Hence, the quantity $\|1/(1+T)\|$ is given by the plot of Fig. 9.7.

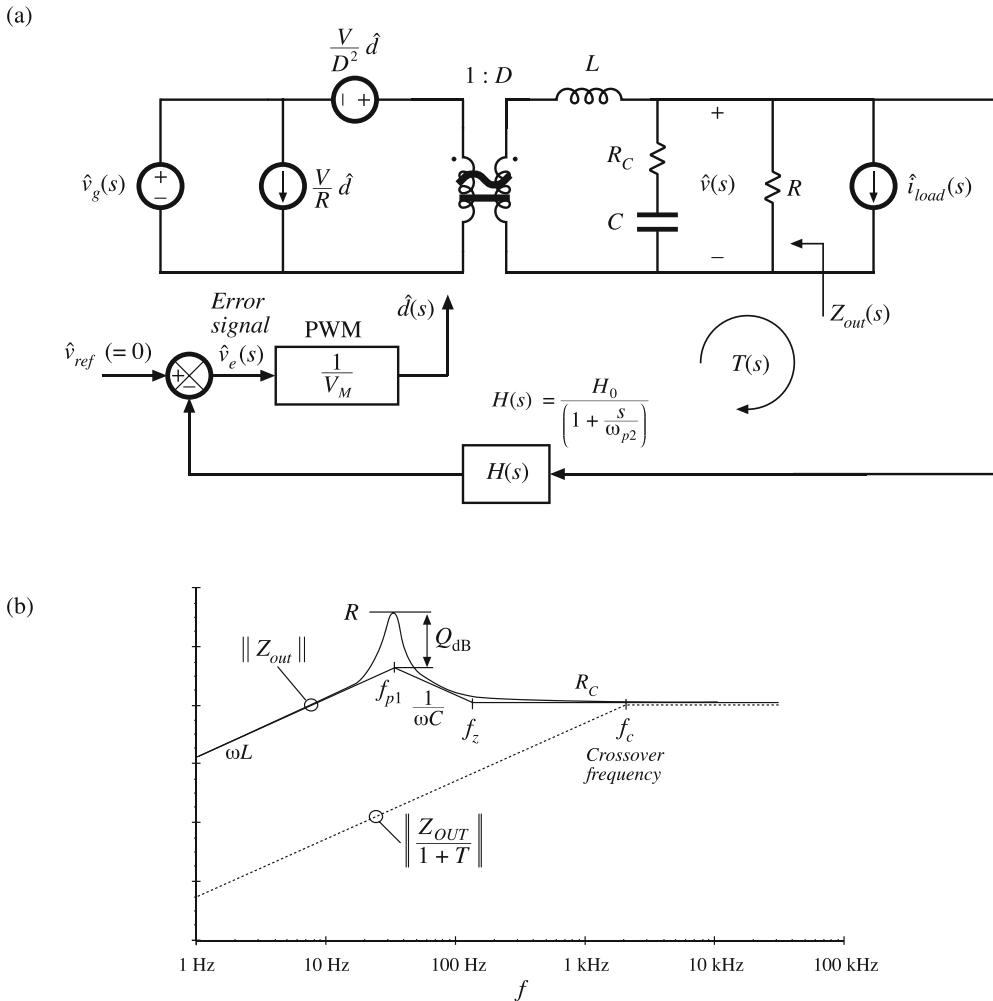


Fig. 9.8 Construction of the closed-loop output impedance of a simple buck regulator: (a) feedback system, (b) open-loop (solid line) and closed-loop (dashed line) output impedance asymptotes

We can construct the Bode plot of the open-loop output impedance Z_{out} by setting \hat{v}_g and \hat{d} to zero in Fig. 9.8a and then finding the impedance between the output terminals; the result is:

$$Z_{out}(s) = sL \left\| R \right\| \left(R_C + \frac{1}{sC} \right) \quad (9.19)$$

The approximate Bode diagram of the open-loop output impedance is constructed in Fig. 9.8b, for the typical case with $R_C \ll R$. The closed-loop output impedance is next constructed by multiplying the open-loop output impedance of Fig. 9.8b by the $\|1/(1+T)\|$ asymptotes of Fig. 9.7, with the result illustrated in Fig. 9.8b. At frequencies greater than the crossover frequency f_c ,

the output impedance is unaffected by the feedback loop. At frequencies immediately below f_c , the feedback loop reduces the output impedance and the $\|1/(1 + T)\|$ term introduces a +20 dB/decade slope to $\|Z_{out}/(1 + T)\|$. At $f = f_z$, the zero of Z_{out} is cancelled by the pole of $1/(1 + T)$, and hence no change in slope is observed in the closed-loop output impedance plot. Likewise, at $f = f_{p1}$, the resonant poles of Z_{out} are cancelled by the resonant zeroes of $1/(1 + T)$, and again there is no change in the slope of $\|Z_{out}/(1 + T)\|$. These cancellations occur because the power stage circuit introduces the same poles into $G_{vd}(s)$ and $Z_{out}(s)$.

Another example is given later in this chapter, in which a feedback compensator circuit introduces poles and zeroes into $T(s)$ that are not present in $Z_{out}(s)$. As a result, the closed-loop output impedance exhibits poles and zeroes induced by the compensator dynamics within $\|1/(1 + T)\|$.

9.4 Stability

It is well known that adding a feedback loop can cause an otherwise stable system to become unstable. Even though the transfer functions of the original converter, Eq. (9.1), as well as of the loop gain $T(s)$, contain no right half-plane poles, it is possible for the closed-loop transfer functions of Eq. (9.4) to contain right half-plane poles. The feedback loop then fails to regulate the system at the desired quiescent operating point, and oscillations are usually observed. It is important to avoid this situation. And even when the feedback system is stable, it is possible for the transient response to exhibit undesirable ringing and overshoot. The stability problem is discussed in this section, and a method for ensuring that the feedback system is stable and well-behaved is explained.

When feedback destabilizes the system, the denominator $(1+T(s))$ terms in Eq. (9.4) contain roots in the right half-plane (i.e., with positive real parts). If $T(s)$ is a rational fraction, that is, the ratio $N(s)/D(s)$ of two polynomial functions $N(s)$ and $D(s)$, then we can write

$$\begin{aligned} \frac{T(s)}{1 + T(s)} &= \frac{\frac{N(s)}{D(s)}}{1 + \frac{N(s)}{D(s)}} = \frac{N(s)}{N(s) + D(s)} \\ \frac{1}{1 + T(s)} &= \frac{1}{1 + \frac{N(s)}{D(s)}} = \frac{D(s)}{N(s) + D(s)} \end{aligned} \quad (9.20)$$

So $T(s)/(1+T(s))$ and $1/(1+T(s))$ contain the same poles, given by the roots of the polynomial $(N(s) + D(s))$. A brute-force test for stability is to evaluate $(N(s) + D(s))$, and factor the result to see whether any of the roots have positive real parts. However, for all but very simple loop gains, this involves a great deal of work. A more illuminating method is given by the Nyquist stability theorem, in which the number of right half-plane roots of $(N(s) + D(s))$ can be determined by testing $T(s)$ [82, 83]. This theorem is discussed in Sect. 9.4.2. Often, a special case of the theorem known as the phase margin test is sufficient for designing most voltage regulators; the simpler phase margin test is discussed first.

9.4.1 The Phase Margin Test

The crossover frequency f_c is defined as the frequency where the magnitude of the loop gain is unity:

$$\|T(j2\pi f_c)\| = 1 \Rightarrow 0 \text{ dB} \quad (9.21)$$

To compute the phase margin φ_m , the phase of the loop gain T is evaluated at the crossover frequency, and 180° is added. Hence,

$$\varphi_m = 180^\circ + \angle T(j2\pi f_c) \quad (9.22)$$

If there is exactly one crossover frequency, and if the loop gain $T(s)$ contains no right half-plane poles, then the quantities $1/(1 + T)$ and $T/(1 + T)$ contain no right half-plane poles when the defined in Eq. (9.22) is positive. Thus, using a simple test on $T(s)$, we can determine the stability of $T/(1 + T)$ and $1/(1 + T)$. This is an easy-to-use design tool—we simply ensure that the phase of T is greater than -180° at the crossover frequency.

When there are multiple crossover frequencies, the phase margin test may be ambiguous. Also, when T contains right half-plane poles (i.e., the original open-loop system is unstable), then the phase margin test cannot be used. In either case, the more general Nyquist stability theorem (Sect. 9.4.2) must be employed.

The loop gain of a typical stable system is shown in Fig. 9.9. It can be seen that $\angle T(j2\pi f_c) = -112^\circ$. Hence, $\varphi_m = 180^\circ - 112^\circ = +68^\circ$. Since the phase margin is positive, $T/(1 + T)$ and $1/(1 + T)$ contain no right half-plane poles, and the feedback system is stable.

The loop gain of an unstable system is sketched in Fig. 9.10. For this example, $\angle T(j2\pi f_c) = -230^\circ$. The phase margin is $\varphi_m = 180^\circ - 230^\circ = -50^\circ$. The negative phase margin implies that $T/(1 + T)$ and $1/(1 + T)$ each contain at least one right half-plane pole.

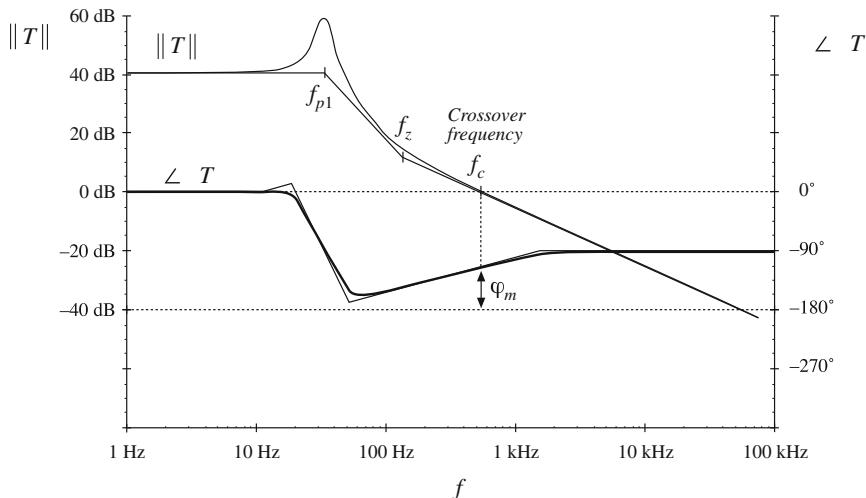


Fig. 9.9 Magnitude and phase of the loop gain of a stable system. The phase margin φ_m is positive

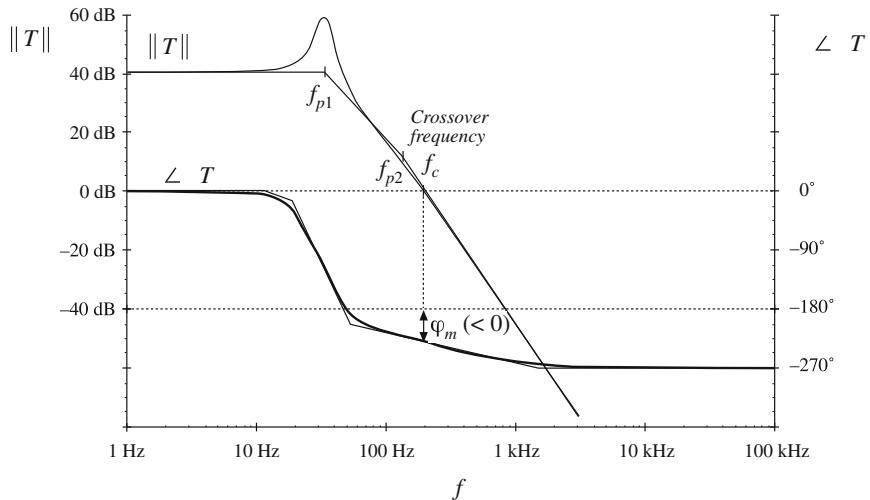


Fig. 9.10 Magnitude and phase of the loop gain of an unstable system. The phase margin φ_m is negative

9.4.2 The Nyquist Stability Criterion

The *Nyquist Stability Criterion* is a rigorous and general technique to evaluate stability of a closed-loop system, based on its loop gain. This technique determines the number of poles of the closed-loop transfer functions $T/(1+T)$ and $1/(1+T)$ that lie in the right half of the complex s -plane, based on a plot of the loop gain $T(s)$ that can be derived from its Bode plot. The phase margin test of Sect. 9.4.1 is based on the Nyquist plot, and is a useful but not entirely general test for stability. In some cases, including several encountered later in this textbook, the more general Nyquist stability test must be employed.

The Nyquist Stability Criterion is based on the conformal mapping of a contour Γ that encloses the right half (positive real portion) of the complex s -plane. The contour is mapped through the loop gain transfer function $T(s)$. Encirclements of the -1 point by the mapped contour are employed to count the number of right half-plane poles that are present in the closed-loop transfer functions. The subsections below present a derivation, the precise rules for application, and some important examples.

The Principle of the Argument

Let us consider a transfer function $T(s)$ having a zero at $s = s_1$:

$$T(s) = (s - s_1) \quad (9.23)$$

Let us also consider a closed contour Γ in the complex s -plane that encircles the point s_1 as illustrated in Fig. 9.11a. The complex variable s is varied to follow the path Γ , beginning at some point a and proceeding around the contour in the clockwise direction through points b , c , and back to a . For the example $T(s)$ of Eq. (9.23), the value of $T(s)$ at some point s is seen to be the vector extending from s_1 to s , having magnitude and phase as illustrated in Fig. 9.11a.

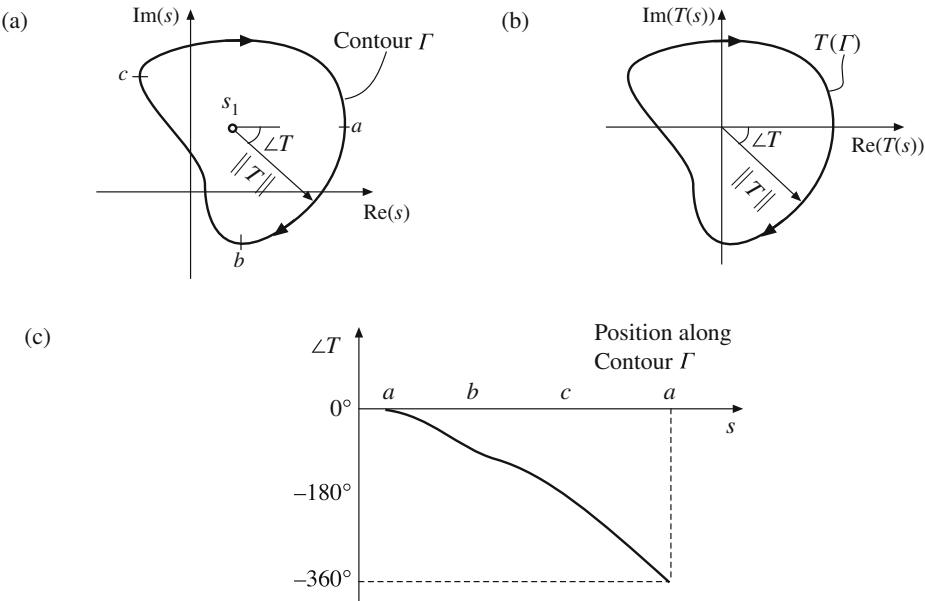


Fig. 9.11 Principle of the argument, example 1: (a) a closed contour Γ in the complex s plane, (b) mapping of the contour Γ through the transfer function $T(s)$ of Eq. (9.23), (c) variation of the phase of $T(s)$, as s varies around the contour Γ

As sketched in Fig. 9.11c, at $s = a$ the phase $\angle T$ is 0° . As s varies along the contour, through b , c , and then back to a , the phase $\angle T$ decreases, and becomes -360° after one complete traverse of contour Γ . This net phase change of -360° indicates that the zero at s_1 lies inside contour Γ .

Figure 9.11b contains a plot of $T(s)$ as s varies around the contour Γ ; the magnitude $\|T\|$ and phase $\angle T$ are identified and are identical to the quantities identified in Fig. 9.11a. This plot is a *conformal mapping* of the contour Γ through the transfer function $T(s)$; conformal mappings preserve local angles. The mapped contour $T(\Gamma)$ encircles the origin of the $T(s)$ plane, as indicated by the net change of -360° in $\angle T(s)$.

Figure 9.12a illustrates a second contour Γ' that does not enclose the zero of $T(s)$ at s_1 . As illustrated in Fig. 9.12c, after one complete traverse of contour Γ' , the net change in $\angle T$ is zero. The mapped contour $T(\Gamma')$ is illustrated in Fig. 9.12b; this contour does not encircle the origin of the $T(s)$ plane.

The phase of a complex function is sometimes referred to as its *argument*. Cauchy's principle of the argument tells us that when the closed contour Γ encloses the zero s_1 , then the phase $\angle T(s)$ exhibits a net change of -360° as s traverses Γ once in the clockwise direction. This is equivalent to saying that the mapped contour $T(\Gamma)$ encircles the origin of the T plane.

Next let us consider a transfer function $T(s)$ that contains multiple poles and zeroes:

$$T(s) = T_{ref} \frac{(s - z_1)(s - z_2)\dots}{(s - p_1)(s - p_2)\dots} \quad (9.24)$$

As usual, we can express the phase of $T(s)$ as a sum of terms that arise from each zero or pole, as follows:

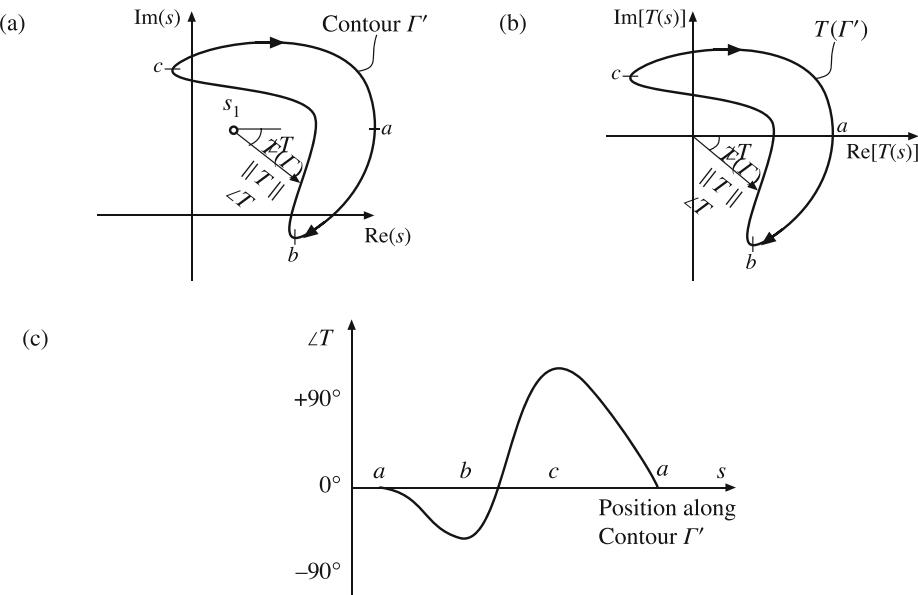


Fig. 9.12 Principle of the argument, example 2: (a) a closed contour Γ' in the complex s plane, (b) mapping of the contour Γ' through the transfer function $T(s)$ of Eq. (9.23), (c) variation of the phase of $T(s)$, as s varies around the contour Γ' . Since the zero at $s = s_1$ does not lie inside contour Γ' , there is no net change in the phase of T , and the mapped contour $T(\Gamma')$ does not encircle the origin of the T plane

$$\angle T(s) = \angle(s - z_1) + \angle(s - z_2) + \cdots - \angle(s - p_1) - \angle(s - p_2) - \cdots \quad (9.25)$$

We can again define a closed contour Γ in the complex s plane, and examine how the phase $T(s)$ changes as s traverses the contour once in the clockwise direction. Each zero of $T(s)$ that lies inside the contour will cause a net change of -360° in $\angle T$, and each pole of $T(s)$ lying inside the contour will cause a net change of $+360^\circ$ in $\angle T$. If a total of Z zeroes and P poles lie inside the contour Γ , then $\angle T$ will exhibit a net phase shift of $-N360^\circ$, where

$$N = Z - P \quad (9.26)$$

The mapped contour $T(\Gamma)$ will encircle the origin of the $T(s)$ plane N times in the clockwise direction.

Thus, the principle of the argument provides us with a tool to determine the number of poles and zeroes that lie inside a contour Γ .

The Nyquist Contour

It is desired to determine whether the closed-loop transfer functions of Eq. (9.20) contain unstable poles that lie in the right half of the complex plane. To accomplish this, we can define a contour Γ that encloses the complete right half-plane, then employ the principle of the argument to test the number of closed-loop poles that are enclosed by this contour.

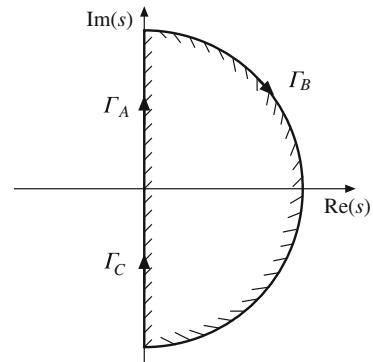


Fig. 9.13 The Nyquist contour, which encloses the right half of the complex s plane

Figure 9.13 illustrates a contour Γ called the *Nyquist contour*. This contour is traversed in the clockwise direction, and the region enclosed to the right of the contour is the right half of the complex s plane. The Nyquist contour is comprised of three parts. Segment Γ_A is the positive part of the imaginary axis, in which

$$s = j\omega \quad \text{with} \quad \omega \in (0, \infty) \quad (9.27)$$

Segment Γ_B can be chosen to be a semicircular arc that lies to the right of all closed-loop poles, defined as follows:

$$s = Re^{j\theta} \quad \text{with} \quad R \rightarrow \infty \quad \text{and} \quad \theta \in (+90^\circ, -90^\circ) \quad (9.28)$$

Segment Γ_C is the negative part of the imaginary axis, in which

$$s = -j\omega \quad \text{with} \quad \omega \in (\infty, 0) \quad (9.29)$$

Segment Γ_C is the complex conjugate of segment Γ_A .

If a transfer function $F(s)$ contains Z zeroes and P poles in the right half of the complex plane, then the mapping $F(\Gamma)$ of the Nyquist contour will encircle the origin of the $F(s)$ plane $N = (Z - P)$ times.

Stability Test

The closed-loop transfer functions of Eq. (9.20) contain the denominator polynomial $N(s) + D(s)$, whose roots are the closed-loop poles. It is desired to test whether this polynomial contains roots in the right half of the complex s -plane. Note from Eq. (9.20) that these roots are the zeroes of the quantity $(1 + T(s))$, and additionally that the poles of $(1 + T(s))$ coincide with the poles of $T(s)$. Hence we could map the Nyquist contour of Fig. 9.13 through the transfer function $(1 + T(s))$, and evaluate the number of encirclements of the origin.

In the complex plane, the quantity $(1 + T(s))$ is simply equal to the quantity $T(s)$ shifted to the right by one unit. If the mapped Nyquist contour $(1 + T(\Gamma))$ encircles the origin, then the contour $T(\Gamma)$ encircles the -1 point. So one could map the Nyquist contour Γ of Fig. 9.13 through the loop gain $T(s)$ and count the number of encirclements N of the -1 point by $T(\Gamma)$. The number of encirclements N is related to the number of poles in the right half-plane according to $N = Z - P$,

where Z is the number of right half-plane poles of the closed-loop gains $T/(1+T)$ or $1/(1+T)$, and P is the number of right half-plane poles present in the original loop gain $T(s)$.

If the original open-loop system is stable, so that $T(s)$ contains no right half-plane poles, then $P = 0$. In this common case $N = Z$: the number of encirclements of the -1 point by $T(\Gamma)$ is equal to the number of right half-plane closed-loop poles in $T/(1+T)$ or $1/(1+T)$.

A Basic Example

As a first example, let us consider a loop gain $T(s)$ having three poles:

$$T(s) = \frac{T_0}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)\left(1 + \frac{s}{\omega_3}\right)} \quad (9.30)$$

The magnitude and phase Bode plot of $T(s)$ is sketched in Fig. 9.14 for some specific values of T_0 , ω_1 , ω_2 , and ω_3 . For this example, $T(s)$ exhibits a crossover frequency ω_c with phase margin φ_m as illustrated.

Figure 9.15a illustrates the first part of the Nyquist plot, in which segment Γ_A defined by Eq. (9.27) is mapped through the loop gain. Since $s = j\omega$ along Γ_A , this amounts to a polar plot of $T(j\omega)$ that corresponds to the magnitude and phase data of the Bode plot in Fig. 9.14. At $\omega = 0$, the loop gain has magnitude T_0 and phase 0° , so that the Nyquist plot begins on the positive real axis at $T = T_0$. As ω increases, the magnitude decreases and the phase becomes negative as illustrated.

At the crossover frequency f_c , the loop gain has magnitude 1 and phase $(-180^\circ + \varphi_m)$. The contour $T(j\omega)$ crosses the unit circle at this point, as illustrated in Fig. 9.15a. At frequencies above f_c the magnitude continues to decrease, and the contour $T(j\omega)$ tends towards the origin.

The second portion of the Nyquist contour Γ_B is defined by Eq. (9.28). To evaluate how the loop gain $T(s)$ maps the contour Γ_B , we first substitute $s = Re^{j\theta}$ into Eq. (9.30):

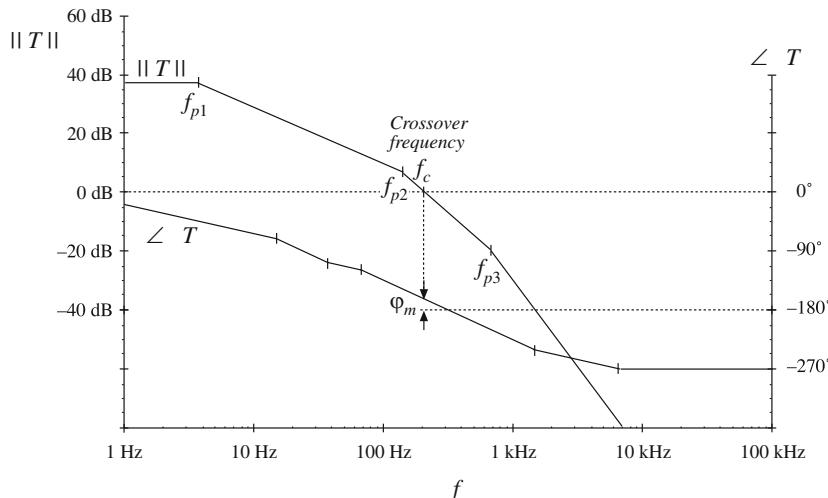


Fig. 9.14 Bode plot of loop gain $T(s)$ for the example of Eq. (9.30)

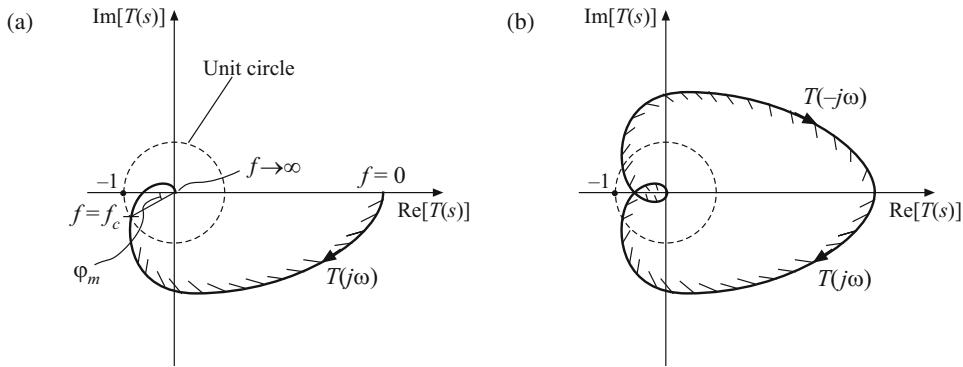


Fig. 9.15 Nyquist plot for the loop gain of Fig. 9.14: (a) mapping of the contour Γ_A through the loop gain $T(s)$, (b) mapping of the complete Nyquist contour through the loop gain $T(s)$

$$T(Re^{j\theta}) = \frac{T_0}{\left(1 + \frac{Re^{j\theta}}{\omega_1}\right)\left(1 + \frac{Re^{j\theta}}{\omega_2}\right)\left(1 + \frac{Re^{j\theta}}{\omega_3}\right)} \quad (9.31)$$

Next, we let $R \rightarrow \infty$. This causes the denominator of Eq. (9.31) to tend to infinity in magnitude, which causes the magnitude of T to tend to zero. This portion of the Nyquist plot collapses to the origin.

The third portion of the Nyquist plot involves mapping the segment Γ_C defined by Eq. (9.29) through the loop gain $T(s)$. This portion of the Nyquist contour is a polar plot of $T(-j\omega)$, which is the complex conjugate of $T(j\omega)$. Hence this plot is easily sketched by reflecting the $T(j\omega)$ plot about the real axis, as illustrated in Fig. 9.15b.

We can now determine the number of encirclements of the -1 point by $T(\Gamma)$. Examination of Fig. 9.15b shows that the -1 point lies outside the contour $T(\Gamma)$ and hence there are no encirclements: $N = 0$. Since the original loop gain $T(s)$ contains no right half-plane poles, $P = 0$. According to Eq. (9.26), $Z = 0$ so the closed-loop transfer functions contain no right half-plane poles, and the feedback loop is stable.

If the phase margin φ_m identified in Fig. 9.14 had been negative, then the contour $T(\Gamma)$ would appear as illustrated in Fig. 9.16. The plot of $T(j\omega)$ crosses the unit circle in the third quadrant. In this case, the Nyquist plot of Fig. 9.16b encircles the -1 point twice: $N = 2$. Hence $Z = 2$ and the closed-loop transfer functions contain two RHP poles. The feedback loop is unstable. For this example, the original $T(s)$ contained three poles in the left half of the complex s -plane; in the closed-loop transfer function $T/(1 + T)$, two of these poles have moved into the right half-plane, while one pole remains in the left half of the complex s -plane.

Example 2: Three Crossover Frequencies

As a second example, let us consider a loop gain having a low-frequency real pole at $f = f_1$, and higher-frequency resonant poles at frequency $f = f_2$ that is just beyond the (first) crossover frequency:

$$T(s) = \frac{T_0}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{Q\omega_2} + \left(\frac{s}{\omega_2}\right)^2\right)} \quad (9.32)$$

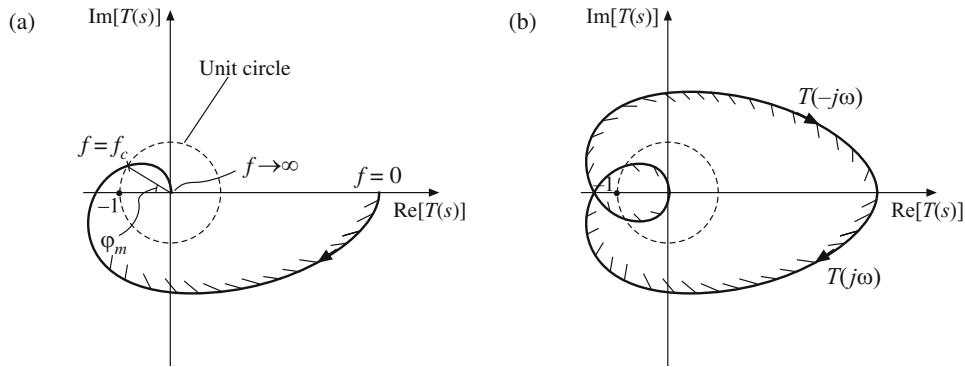


Fig. 9.16 Nyquist plot for an unstable system: (a) mapping of the contour Γ_A through the loop gain $T(s)$, with negative phase margin φ_m , (b) mapping of the complete Nyquist contour through the loop gain $T(s)$

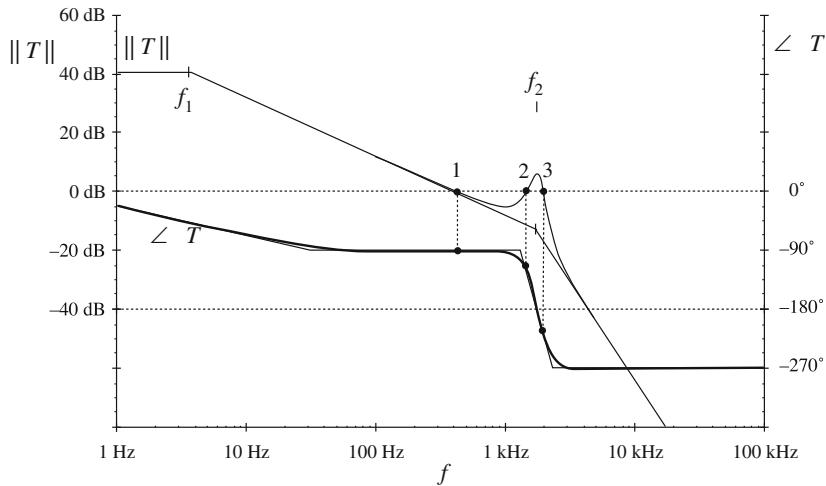


Fig. 9.17 Bode plot of loop gain $T(s)$ for the example of Eq. (9.32). The loop gain exhibits three crossover frequencies

A Bode plot of the loop gain for this case is illustrated in Fig. 9.17. The resonant poles at f_2 cause the magnitude of T increase above 0 dB in the vicinity of f_2 . Consequently, there are three crossover frequencies (designated 1, 2, and 3). We could associate a phase margin with each crossover frequency; for the plot of Fig. 9.17, the phase margins associated with crossover frequencies 1 and 2 are positive, while the phase margin associated with crossover frequency 3 is negative. Hence the simple phase margin test is ambiguous, and it is necessary to sketch the Nyquist plot to correctly determine whether this loop gain leads to a stable system.

Figure 9.18 contains the Nyquist plot corresponding to the Bode plot of Fig. 9.17. Figure 9.18a contains the mapped contour $T(\Gamma_A) = T(j\omega)$, with crossover points 1, 2, and 3 identified. Figure 9.18b contains the mapping of the complete Nyquist contour. It can be seen that

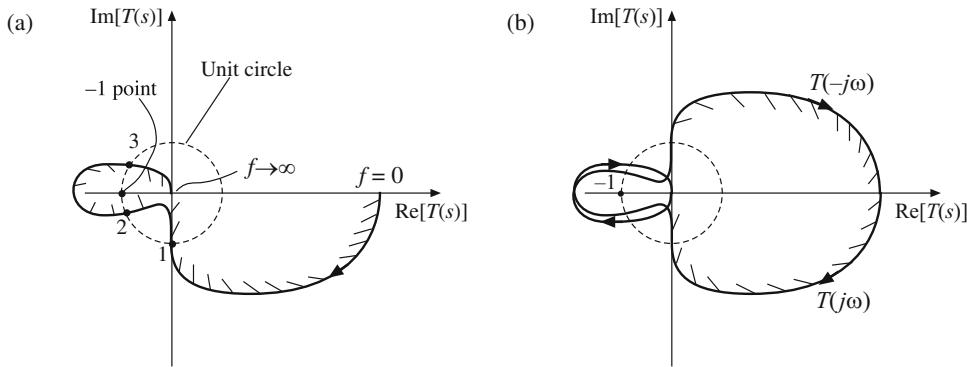


Fig. 9.18 Nyquist plot for the example having three crossover frequencies (Fig. 9.17): (a) mapping of the contour Γ_A through the loop gain $T(s)$, (b) mapping of the complete Nyquist contour through the loop gain $T(s)$

the -1 point is encircled twice. Hence, the closed-loop transfer functions contain two poles in the right half of the complex plane, and this feedback system is unstable.

Example 3: Integrator in Feedback Loop

If the Nyquist contour Γ passes through one or more singularities of the loop gain $T(s)$, then the conformal mapping property is lost, and the arguments of the above sections no longer apply. This case can occur when the loop gain $T(s)$ contains one or more poles lying on the imaginary axis. A common example is the use of an integrator in the compensator (see Sect. 9.5.2), leading to a pole at the origin. An example of a loop gain containing a pole at the origin is:

$$T(s) = \frac{1}{\left(\frac{s}{\omega_0}\right)\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)} \quad (9.33)$$

The corner frequencies ω_0 , ω_1 , and ω_2 are positive and real in this example. This special case can be handled by redefining the Nyquist contour of Fig. 9.13 as illustrated in Fig. 9.19. A fourth segment Γ_D is added, to jog the contour around the singularity. Segment Γ_D is defined to be a semicircular arc as follows:

$$s = \epsilon e^{j\theta} \quad \text{with} \quad \epsilon \rightarrow 0 \quad \text{and} \quad \theta \in (-90^\circ, +90^\circ) \quad (9.34)$$

The loop gain $T(s)$ of Eq. (9.33) contains no poles inside the modified Nyquist contour of Fig. 9.19. Hence the number of right half-plane poles of the closed-loop transfer function $T/(1 + T)$ is equal to the number of encirclements of the -1 point by the mapped modified Nyquist contour $T(\Gamma)$.

The magnitude and phase Bode plot of $T(s)$ is sketched in Fig. 9.20 for some specific values of ω_0 , ω_1 , and ω_2 . For this example, $T(s)$ exhibits a crossover frequency f_c with phase margin φ_m as illustrated.

Figure 9.21a illustrates the first part of the Nyquist plot, in which segment Γ_A is mapped through the loop gain $T(s)$. Along this segment, $s = j\omega$ with ω varying from $\epsilon (\rightarrow 0)$ to ∞ .

Fig. 9.19 Modification of the Nyquist contour to handle the special case in which the loop gain includes a pole at the origin. Segment Γ_D defined by Eq. (9.34) routes the Nyquist contour around the pole at $s = 0$. The locations of poles of Eq. (9.33) are marked \times

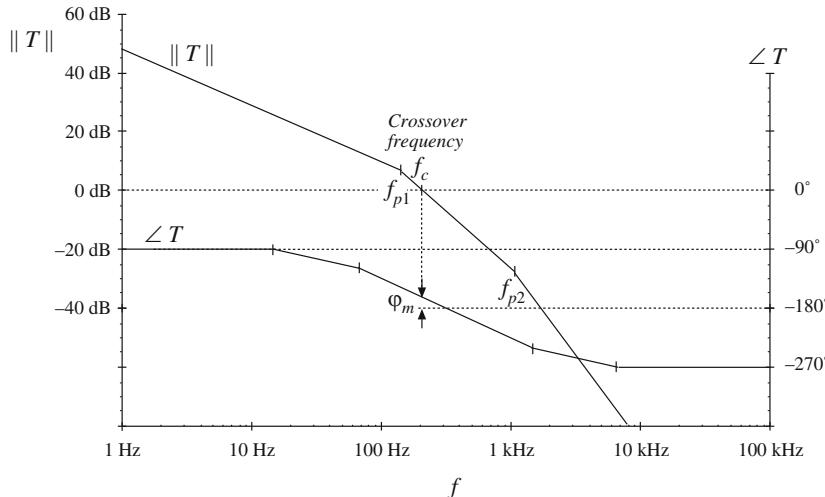
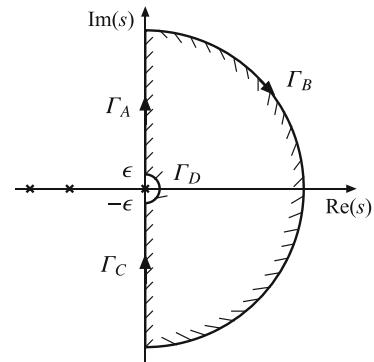


Fig. 9.20 Bode plot of loop gain $T(s)$ for the example of Eq. (9.33)

Segment Γ_B is again defined by Eq. (9.28), and this segment again maps to the origin. Segment Γ_C is the complex conjugate of Γ_B . The mapping of contours Γ_A , Γ_B , and Γ_C through the loop gain $T(s)$ is illustrated in Fig. 9.21b. It can be seen that this contour is not closed; to complete the mapped contour, Γ_D must be incorporated.

Substitution of the mapping defined by Eq. (9.34) into the loop gain of Eq. (9.33) leads to:

$$T(\epsilon e^{j\theta}) = \frac{1}{\left(\frac{\epsilon e^{j\theta}}{\omega_0}\right)\left(1 + \frac{\epsilon e^{j\theta}}{\omega_1}\right)\left(1 + \frac{\epsilon e^{j\theta}}{\omega_2}\right)} \quad (9.35)$$

As ϵ tends to zero, the pole terms associated with the corner frequencies ω_1 and ω_2 tend to 1. Equation (9.35) then reduces to

$$T(\epsilon e^{j\theta}) = \frac{\omega_0 e^{-j\theta}}{\epsilon} \quad (9.36)$$

As ϵ tends to zero, the magnitude of Eq. (9.36) tends to infinity. As θ varies from -90° to $+90^\circ$, the phase of the mapped contour varies from $+90^\circ$ to -90° . The complete contour is

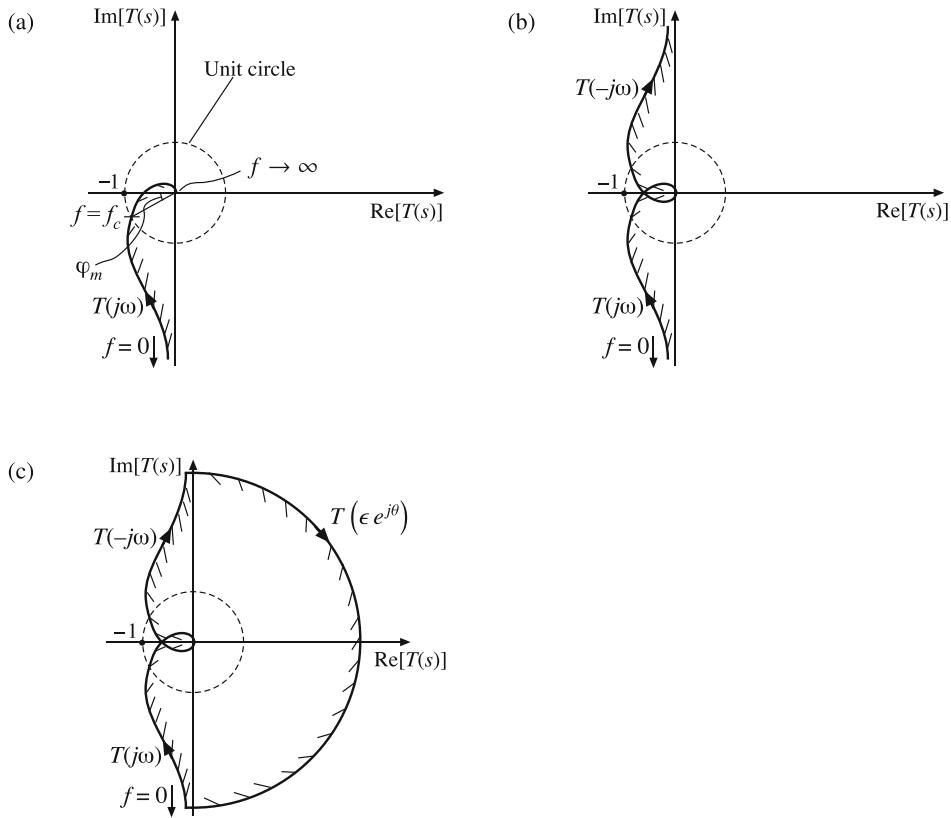


Fig. 9.21 Nyquist plot for the example of an integrator in the feedback loop (Fig. 9.20): (a) mapping of the contour Γ_A through the loop gain $T(s)$, (b) mapping of the contours Γ_A , Γ_B , and Γ_C through the loop gain $T(s)$, (c) mapping of complete modified Nyquist contour

illustrated in Fig. 9.21c. It can be seen that the mapped contour is now closed, and that there are no encirclements of the -1 point provided that the phase margin is positive. The contour of Fig. 9.21c represents a stable system.

Summary: Nyquist Stability Criterion

Thus, the Nyquist stability criterion is closely related to the Bode plot of the loop gain. The segment Γ_A corresponds to letting $s = j\omega$, and the mapping of Γ_A through the loop gain $T(s)$ constitutes a polar plot of $T(j\omega)$. The number of right half-plane poles of the closed-loop transfer functions $T/(1+T)$ and $1/(1+T)$ is rigorously discerned via determination of the number of encirclements of the -1 point by the Nyquist contour mapped through the loop gain $T(s)$. This explains the origins of the phase margin test, and also provides a stability test for more complex cases such as loop gains having multiple crossover frequencies.

9.4.3 The Relationship Between Phase Margin and Closed-Loop Damping Factor

How much phase margin is necessary? Is a worst-case phase margin of 1° satisfactory? Of course, good designs should have adequate design margins, but there is another important reason why additional phase margin is needed. A small phase margin (in T) causes the closed-loop transfer functions $T/(1 + T)$ and $1/(1 + T)$ to exhibit resonant poles with high Q in the vicinity of the crossover frequency. The system transient response exhibits overshoot and ringing. As the phase margin is reduced these characteristics become worse (higher Q , longer ringing) until, for $\varphi_m \leq 0^\circ$, the system becomes unstable.

Let us consider a loop gain $T(s)$ which is well-approximated, in the vicinity of the crossover frequency, by the following function:

$$T(s) = \frac{1}{\left(\frac{s}{\omega_0}\right)\left(1 + \frac{s}{\omega_2}\right)} \quad (9.37)$$

Magnitude and phase asymptotes are plotted in Fig. 9.22. This function is a good approximation near the crossover frequency for many common loop gains, in which $\|T\|$ approaches unity gain with a -20 dB/decade slope, with an additional pole at frequency $f_2 = \omega_2/2\pi$. Any additional poles and zeroes are assumed to be sufficiently far above or below the crossover frequency, such that they have negligible effect on the system transfer functions near the crossover frequency.

Note that, as $f_2 \rightarrow \infty$, the phase margin φ_m approaches 90° . As $f_2 \rightarrow 0$, $\varphi_m \rightarrow 0^\circ$. So as f_2 is reduced, the phase margin is also reduced. Let's investigate how this affects the closed-loop response via $T/(1 + T)$. We can write

$$\frac{T(s)}{1 + T(s)} = \frac{1}{1 + \frac{1}{T(s)}} = \frac{1}{1 + \frac{s}{\omega_0} + \frac{s^2}{\omega_0 \omega_2}} \quad (9.38)$$

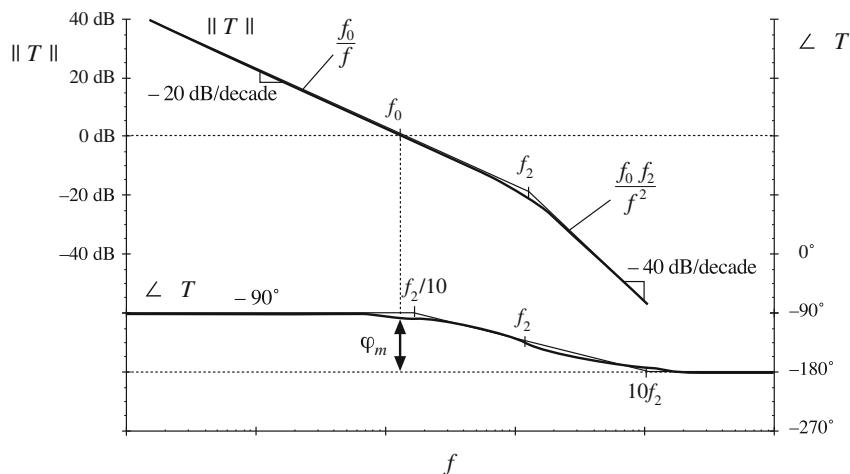


Fig. 9.22 Magnitude and phase asymptotes for the loop gain T of Eq. (9.37)

using Eq. (9.37). By putting this into the standard normalized quadratic form, one obtains

$$\frac{T(s)}{1+T(s)} = \frac{1}{1 + \frac{s}{Q\omega_c} + \left(\frac{s}{\omega_c}\right)^2} \quad (9.39)$$

where

$$\begin{aligned}\omega_c &= \sqrt{\omega_0\omega_2} = 2\pi f_c \\ Q &= \frac{\omega_0}{\omega_c} = \sqrt{\frac{\omega_0}{\omega_2}}\end{aligned}$$

So the closed-loop response contains quadratic poles at f_c , the geometric mean of f_0 and f_2 . These poles have a low Q -factor when $f_0 \ll f_2$. In this case, we can use the low- Q approximation to estimate their frequencies:

$$\begin{aligned}Q\omega_c &= \omega_0 \\ \frac{\omega_c}{Q} &= \omega_2\end{aligned} \quad (9.40)$$

Magnitude asymptotes are plotted in Fig. 9.23 for this case. It can be seen that these asymptotes conform to the rules of Sect. 9.3 for constructing $T/(1+T)$ by the algebra-on-the-graph method.

Next consider the high- Q case. When the pole frequency f_2 is reduced, reducing the phase margin, then the Q -factor given by Eq. (9.39) is increased. For $Q > 0.5$, resonant poles occur at frequency f_c . The magnitude Bode plot for the case $f_2 < f_0$ is given in Fig. 9.24. The frequency f_c continues to be the geometric mean of f_2 and f_0 , and f_c now coincides with the crossover (unity-gain) frequency of the $\| T \|$ asymptotes. The exact value of the closed-loop gain $T/(1+T)$ at frequency f_c is equal to $Q = f_0/f_c$. As shown in Fig. 9.24, this is identical to the value of the low-frequency -20 dB/decade asymptote (f_0/f), evaluated at frequency f_c . It can be seen that the Q -factor becomes very large as the pole frequency f_2 is reduced.

The asymptotes of Fig. 9.24 also follow the algebra-on-the-graph rules of Sect. 9.3, but the deviation of the exact curve from the asymptotes is not predicted by the algebra-on-the-graph method.

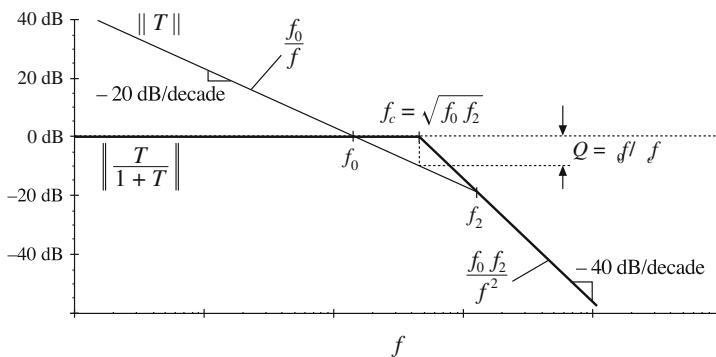


Fig. 9.23 Construction of magnitude asymptotes of the closed-loop transfer function $T/(1+T)$, for the low- Q case

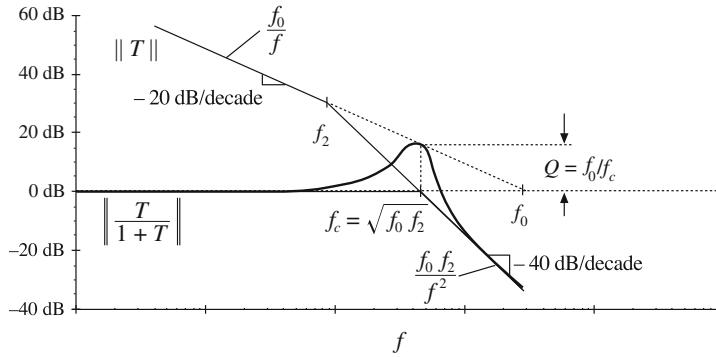


Fig. 9.24 Construction of magnitude asymptotes of the closed-loop transfer function $T/(1 + T)$, for the high- Q case

These two poles with Q -factor appear in both $T/(1 + T)$ and $1/(1 + T)$. We need an easy way to predict the Q -factor. We can obtain such a relationship by finding the frequency at which the magnitude of T is exactly equal to unity. We then evaluate the exact phase of T at this frequency, and compute the phase margin. This phase margin is a function of the ratio f_0/f_2 , or Q^2 . We can then solve to find Q as a function of the phase margin. The result is

$$Q = \frac{\sqrt{\cos \varphi_m}}{\sin \varphi_m} \quad (9.41)$$

$$\varphi_m = \tan^{-1} \sqrt{\frac{1 + \sqrt{1 + 4Q^4}}{2Q^4}}$$

This function is plotted in Fig. 9.25, with Q expressed in dB. It can be seen that obtaining real poles ($Q < 0.5$) requires a phase margin of at least 76° . To obtain $Q = 1$, a phase margin of 52° is needed. The system with a phase margin of 1° exhibits a closed-loop response with very high Q ! With a small phase margin, $T(j\omega)$ is very nearly equal to -1 in the vicinity of the crossover frequency. The denominator $(1 + T)$ then becomes very small, causing the closed-loop transfer functions to exhibit a peaked response at frequencies near the crossover frequency f_c .

Figure 9.25 is the result for the simple loop gain defined by Eq. (9.37). However, this loop gain is a good approximation for many other loop gains that are encountered in practice, in which $\|T\|$ approaches unity gain with a -20 dB/decade slope, with an additional pole at frequency f_2 . If all other poles and zeroes of $T(s)$ are sufficiently far above or below the crossover frequency, then they have negligible effect on the system transfer functions near the crossover frequency, and Fig. 9.25 gives a good approximation for the relationship between φ_m and Q .

Another common case is the one in which $\|T\|$ approaches unity gain with a -40 dB/decade slope, with an additional zero at frequency f_2 . As f_2 is increased, the phase margin is decreased and Q is increased. It can be shown that the relation between φ_m and Q is exactly the same, Eq. (9.41).

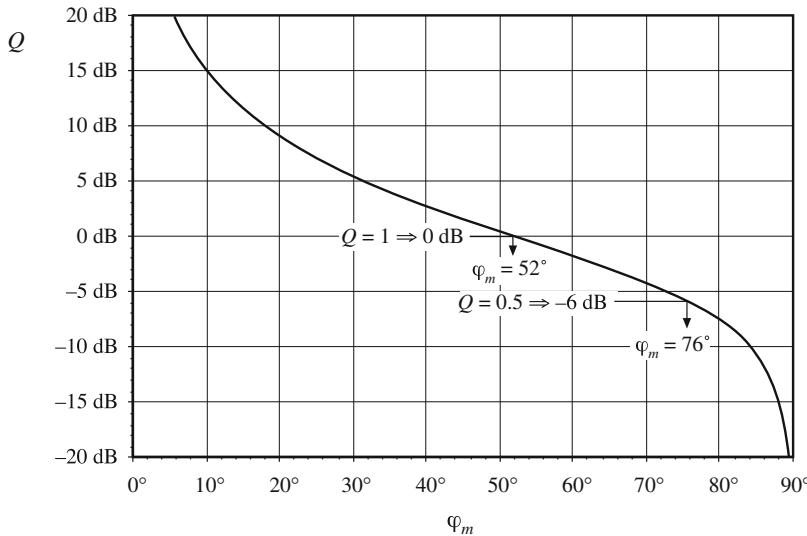


Fig. 9.25 Relationship between loop-gain phase margin φ_m and closed-loop peaking factor Q

A case where Fig. 9.25 fails is when the loop gain $T(s)$ contains three or more poles at or near the crossover frequency. The closed-loop response then also contains three or more poles near the crossover frequency, and these poles cannot be completely characterized by a single Q -factor. Additional work is required to find the behavior of the exact $T/(1+T)$ and $1/(1+T)$ near the crossover frequency, but nonetheless it can be said that a small phase margin leads to a peaked closed-loop response.

9.4.4 Transient Response vs. Damping Factor

One can solve for the unit-step response of the $T/(1+T)$ transfer function, by multiplying Eq. (9.39) by $1/s$ and then taking the inverse Laplace transform. The result for $Q > 0.5$ is

$$\hat{v}(t) = 1 + \frac{2Qe^{-\omega_c t/2Q}}{\sqrt{4Q^2 - 1}} \sin \left[\frac{\sqrt{4Q^2 - 1}}{2Q} \omega_c t + \tan^{-1}(\sqrt{4Q^2 - 1}) \right] \quad (9.42)$$

For $Q < 0.5$, the result is

$$\hat{v}(t) = 1 - \frac{\omega_2}{\omega_2 - \omega_1} e^{-\omega_1 t} - \frac{\omega_1}{\omega_1 - \omega_2} e^{-\omega_2 t} \quad (9.43)$$

with

$$\omega_1, \omega_2 = \frac{\omega_c}{2Q} (1 \pm \sqrt{1 - 4Q^2}) \quad (9.44)$$

These equations are plotted in Fig. 9.26 for various values of Q .

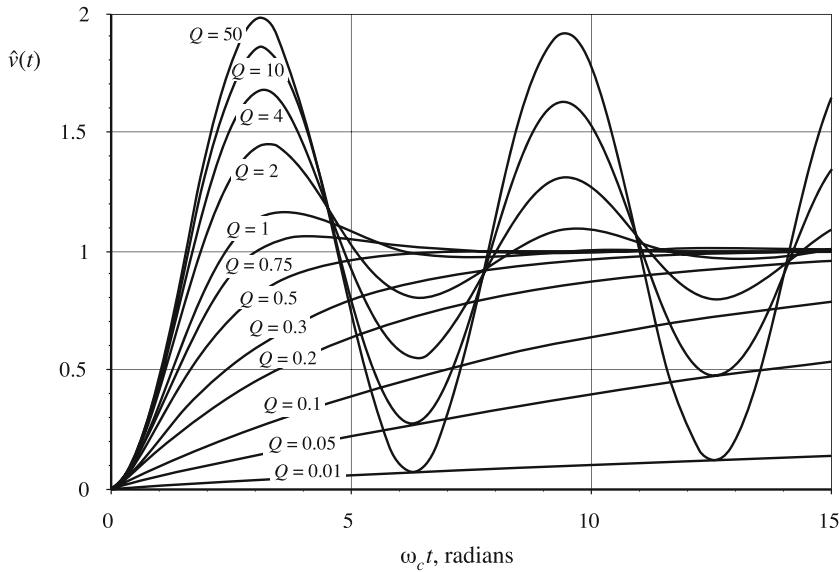


Fig. 9.26 Unit-step response of the second-order system, Eqs. (9.42) and (9.43), for various values of Q

According to Eq. (9.39), when $f_2 > 4f_0$, the Q -factor is less than 0.5, and the closed-loop response contains a low-frequency and a high-frequency real pole. The transient response in this case, Eq. (9.43), contains decaying-exponential functions of time, of the form

$$Ae^{(pole)t} \quad (9.45)$$

This is called the “overdamped” case. With very low Q , the low-frequency pole leads to a slow step response.

For $f_2 = 4f_0$, the Q -factor is equal to 0.5. The closed-loop response contains two real poles at frequency $2f_0$. This is called the “critically damped” case. The transient response is faster than in the overdamped case, because the lowest-frequency pole is at a higher frequency. This is the fastest response that does not exhibit overshoot. At $\omega_c t = \pi$ radians ($t = 1/2f_c$), the voltage has reached 82% of its final value. At $\omega_c t = 2\pi$ radians ($t = 1/f_c$), the voltage has reached 98.6% of its final value.

For $f_2 < 4f_0$, the Q -factor is greater than 0.5. The closed-loop response contains complex poles, and the transient response exhibits sinusoidal-type waveforms with decaying amplitude, Eq. (9.42). The rise time of the step response is faster than in the critically damped case, but the waveforms exhibit overshoot. The peak value of $v(t)$ is

$$\text{peak } \hat{v}(t) = 1 + e^{-\pi/\sqrt{4Q^2-1}} \quad (9.46)$$

This is called the “underdamped” case. A Q -factor of 1 leads to an overshoot of 16.3%, while a Q -factor of 2 leads to a 44.4% overshoot. Large Q -factors lead to overshoots approaching 100%.

The exact transient response of the feedback loop may differ from the plots of Fig. 9.26, because of additional poles and zeroes in T , and because of differences in initial conditions. Nonetheless, Fig. 9.26 illustrates how high- Q poles lead to overshoot and ringing. In most power applications, overshoot is unacceptable. For example, in a 3.3 V computer power supply, the voltage must not be allowed to overshoot to 5 or 6 volts when the supply is turned on—this would likely destroy all of the integrated circuits in the computer! So the Q -factor must be sufficiently low, often 0.5 or less, corresponding to a phase margin of at least 76°.

9.4.5 Load Step Response vs. Damping Factor

Usually we also are interested in the response of the output voltage to a step change in load current. Let us consider the case where the closed-loop output impedance can be well approximated by a second-order function of the form

$$Z_{out}(s) = \frac{\left(\frac{sR_0}{\omega_c}\right)}{1 + \frac{s}{Q\omega_c} + \left(\frac{s}{\omega_c}\right)^2} \quad (9.47)$$

This constitutes an effective parallel $R - L - C$ impedance having characteristic impedance R_0 , resonant frequency f_c , and Q -factor Q . Also consider that the load current takes a step change of magnitude I_0 , with the following Laplace transform:

$$\hat{i}_{load} = \frac{I_0}{s} \quad (9.48)$$

One can multiply Eqs. (9.47) and (9.48), and then invert the Laplace transform to derive an expression for the output voltage response $\hat{v}(t)$. For $Q < 0.5$, the result is:

$$\hat{v}(t) = -\frac{I_0 R_0 Q}{\sqrt{1 - 4Q^2}} \left(e^{-\omega_1 t} - e^{-\omega_2 t} \right) \quad (9.49)$$

with ω_1 and ω_2 defined as in Eq. (9.44). For the high- Q case $Q > 0.5$, the result is:

$$\hat{v}(t) = -\frac{I_0 R_0 2Q}{\sqrt{4Q^2 - 1}} e^{-\omega_c t/2Q} \sin\left(\frac{\sqrt{4Q^2 - 1}}{2Q} \omega_c t\right) \quad (9.50)$$

These equations are plotted in Fig. 9.27 for various values of Q and for $I_0 R_0 = 1$. For non-unity $I_0 R_0$, the curves can be multiplied by $I_0 R_0$: the peak deviation in $\hat{v}(t)$ is proportional to the magnitude of the current step I_0 multiplied by the characteristic impedance R_0 . For $Q < 0.5$, the peak voltage deviation has magnitude slightly less than $I_0 R_0 Q$. At $Q = 0.5$, the peak voltage deviation is approximately $-0.368 I_0 R_0$. As $Q \rightarrow \infty$, the peak voltage deviation tends to $-I_0 R_0$.

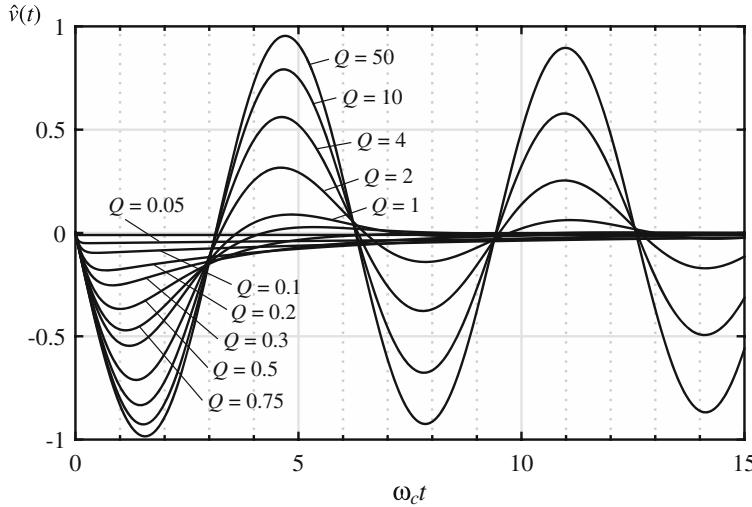


Fig. 9.27 Response of the second-order system to a unit step change in load current, Eqs. (9.49) and (9.50), for various values of Q . These curves are plotted for $I_0R_0 = 1$

9.5 Regulator Design

Let's now consider how to design a regulator system, to meet specifications or design goals regarding rejection of disturbances, transient response, and stability. Typical dc regulator designs are defined using specifications such as the following:

1. *Effect of load current variations on the output voltage regulation.* The output voltage must remain within a specified range when the load current varies in a prescribed way. This amounts to a limit on the maximum magnitude of the closed-loop output impedance of Eq. (9.6), repeated below

$$\left. \frac{\hat{v}(s)}{-\hat{i}_{load}(s)} \right|_{\begin{subarray}{l} \hat{v}_g=0 \\ \hat{v}_{ref}=0 \end{subarray}} = \frac{Z_{out}(s)}{1 + T(s)} \quad (9.51)$$

If, over some frequency range, the open-loop output impedance Z_{out} has magnitude that exceeds the limit, then the loop gain T must be sufficiently large in magnitude over the same frequency range, such that the magnitude of the closed-loop output impedance given in Eq. (9.51) is less than the given limit.

2. *Effect of input voltage variations (for example, at the second harmonic of the ac line frequency) on the output voltage regulation.* Specific maximum limits are usually placed on the amplitude of variations in the output voltage at the second harmonic of the ac line frequency (120 Hz or 100 Hz). If we know the magnitude of the rectification voltage ripple which appears at the converter input (as \hat{v}_g), then we can calculate the resulting output voltage ripple (in \hat{v}) using the closed loop line-to-output transfer function of Eq. (9.5), repeated below

$$\left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\begin{subarray}{l} \hat{v}_{ref}=0 \\ \hat{i}_{load}=0 \end{subarray}} = \frac{G_{vg}(s)}{1 + T(s)} \quad (9.52)$$

The output voltage ripple can be reduced by increasing the magnitude of the loop gain at the ripple frequency. In a typical good design, $\| T \|$ is 20 dB or more at 120 Hz, so that the transfer function of Eq. (9.52) is at least an order of magnitude smaller than the open-loop line-to-output transfer function $\| G_{vg} \|$.

3. *Transient response time.* When a specified large disturbance occurs, such as a large step change in load current or input voltage, the output voltage may undergo a transient. During this transient, the output voltage typically deviates from its specified allowable range. Eventually, the feedback loop operates to return the output voltage within tolerance. The time required to do so is the transient response time; typically, the response time can be shortened by increasing the feedback loop crossover frequency.
4. *Overshoot and ringing.* As discussed in Sect. 9.4.4, the amount of overshoot and ringing allowed in the transient response may be limited. Such a specification implies that the phase margin must be sufficiently large.

Each of these requirements imposes constraints on the loop gain $T(s)$. Therefore, the design of the control system involves modifying the loop gain. As illustrated in Fig. 9.2, a compensator network is added for this purpose. Several well-known strategies for design of the compensator transfer function $G_c(s)$ are discussed below.

9.5.1 Lead (PD) compensator

This type of compensator transfer function is used to improve the phase margin. A zero is added to the loop gain, at a frequency f_z sufficiently far below the crossover frequency f_c , such that the phase margin of $T(s)$ is increased by the desired amount. The lead compensator is also called a *proportional-plus-derivative*, or *PD*, controller—at high frequencies, the zero causes the compensator to differentiate the error signal. It often finds application in systems originally containing a two-pole response. By use of this type of compensator, the bandwidth of the feedback loop (i.e., the crossover frequency f_c) can be extended while maintaining an acceptable phase margin.

A side effect of the zero is that it causes the compensator gain to increase with frequency, with a +20 dB/decade slope. So steps must be taken to ensure that $\| T \|$ remains equal to unity at the desired crossover frequency. Also, since the gain of any practical amplifier must tend to zero at high frequency, the compensator transfer function $G_c(s)$ must contain high-frequency poles. These poles also have the beneficial effect of attenuating high-frequency noise. Of particular concern are the switching frequency harmonics present in the output voltage and feedback signals. If the compensator gain at the switching frequency is too great, then these switching harmonics are amplified by the compensator, and can disrupt the operation of the pulse-width modulator (see Sect. 7.3). So the compensator network should contain poles at a frequency less than the switching frequency. These considerations typically restrict the crossover frequency f_c to be less than approximately 10% of the converter switching frequency f_s . In addition, the circuit designer must take care not to exceed the gain-bandwidth limits of available operational amplifiers.

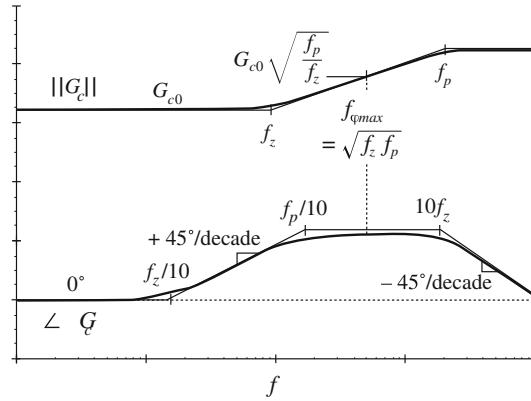


Fig. 9.28 Magnitude and phase asymptotes of the *PD* compensator transfer function G_c of Eq. (9.53)

The transfer function of the lead compensator therefore contains a low-frequency zero and several high-frequency poles. A simplified example containing a single high-frequency pole is given in Eq. (9.53) and illustrated in Fig. 9.28.

$$G_c(s) = G_{c0} \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \quad (9.53)$$

The maximum phase occurs at a frequency $f_{\varphi\max}$ given by the geometrical mean of the pole and zero frequencies:

$$f_{\varphi\max} = \sqrt{f_z f_p} \quad (9.54)$$

To obtain the maximum improvement in phase margin, we should design our compensator so that the frequency $f_{\varphi\max}$ coincides with the loop gain crossover frequency f_c . The value of the phase at this frequency can be shown to be

$$\angle G_c(f_{\varphi\max}) = \tan^{-1} \left(\frac{1}{2} \sqrt{\frac{f_p}{f_z}} - \frac{1}{2} \sqrt{\frac{f_z}{f_p}} \right) \quad (9.55)$$

This equation is plotted in Fig. 9.29. Equation (9.55) can be inverted to obtain

$$\frac{f_p}{f_z} = \frac{1 + \sin(\theta)}{1 - \sin(\theta)} \quad (9.56)$$

where $\theta = \angle G_c(f_{\varphi\max})$. Equations (9.55) and (9.53) imply that, to optimally obtain a compensator phase lead of θ at frequency f_c , the pole and zero frequencies should be chosen as follows:

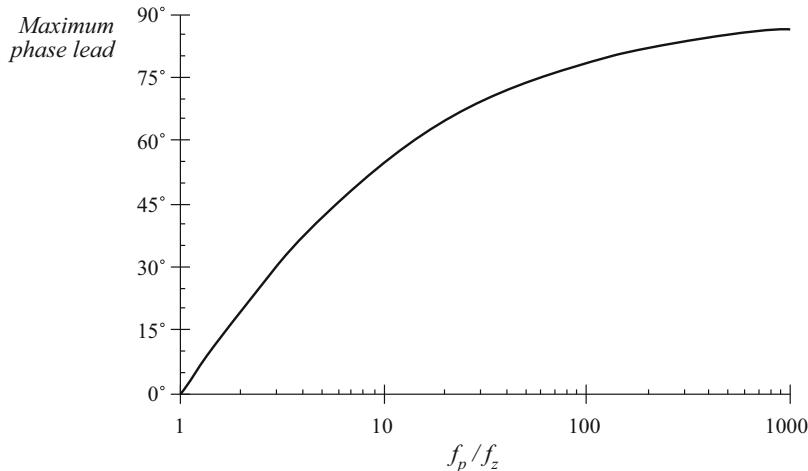


Fig. 9.29 Maximum phase lead θ vs. frequency ratio f_p/f_z for the lead compensator

$$\begin{aligned} f_z &= f_c \sqrt{\frac{1 - \sin(\theta)}{1 + \sin(\theta)}} \\ f_p &= f_c \sqrt{\frac{1 + \sin(\theta)}{1 - \sin(\theta)}} \end{aligned} \quad (9.57)$$

When it is desired to avoid changing the crossover frequency, the magnitude of the compensator gain is chosen to be unity at the loop gain crossover frequency f_c . This requires that G_{c0} be chosen according to the following formula:

$$G_{c0} = \sqrt{\frac{f_z}{f_p}} \quad (9.58)$$

It can be seen that G_{c0} is less than unity, and therefore the lead compensator reduces the dc gain of the feedback loop. Other choices of G_{c0} can be selected when it is desired to shift the crossover frequency f_c ; for example, increasing the value of G_{c0} causes the crossover frequency to increase. If the frequencies f_p and f_z are chosen as in Eq. (9.57), then $f_{\varphi_{max}}$ of Eq. (9.53) will coincide with the new crossover frequency f_c .

The Bode diagram of a typical loop gain $T(s)$ containing two poles is illustrated in Fig. 9.30. The phase margin of the original $T(s)$ is small, since the crossover frequency f_c is substantially greater than the pole frequency f_0 . The result of adding a lead compensator is also illustrated. The lead compensator of this example is designed to maintain the same crossover frequency but improve the phase margin.

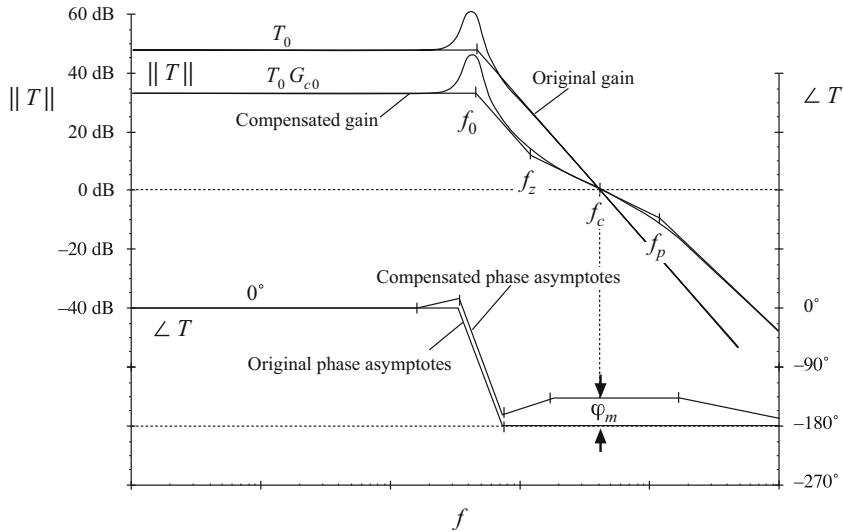


Fig. 9.30 Compensation of a loop gain containing two poles, using a lead (PD) compensator. The phase margin φ_m is improved

9.5.2 Lag (PI) Compensator

This type of compensator is used to increase the low-frequency loop gain, such that the output is better regulated at dc and at frequencies well below the loop crossover frequency. As given in Eq. (9.59) and illustrated in Fig. 9.31, an inverted zero is added to the loop gain, at frequency f_L .

$$G_c(s) = G_{c\infty} \left(1 + \frac{\omega_L}{s} \right) \quad (9.59)$$

If f_L is sufficiently lower than the loop crossover frequency f_c , then the phase margin is unchanged. This type of compensator is also called a *proportional-plus-integral*, or *PI*, controller. At low frequencies, the inverted zero causes the compensator to integrate the error signal.

To the extent that the compensator gain can be made arbitrarily large at dc, the dc loop gain $T(0)$ becomes arbitrarily large. This causes the dc component of the error signal to approach zero. In consequence, the steady-state output voltage is perfectly regulated, and the disturbance-to-output transfer functions approach zero at dc. Such behavior is easily obtained in practice, with the compensator of Eq. (9.59) realized using a conventional operational amplifier.

Although the *PI* compensator is useful in nearly all types of feedback systems, it is an especially simple and effective approach for systems originally containing a single pole. For the example of Fig. 9.32, the original uncompensated loop gain is of the form

$$T_u(s) = \frac{T_{u0}}{\left(1 + \frac{s}{\omega_0} \right)} \quad (9.60)$$

The compensator transfer function of Eq. (9.59) is used, so that the compensated loop gain is $T(s) = T_u(s)G_c(s)$. Magnitude and phase asymptotes of $T(s)$ are also illustrated in Fig. 9.32. The compensator high-frequency gain $G_{c\infty}$ is chosen to obtain the desired crossover frequency

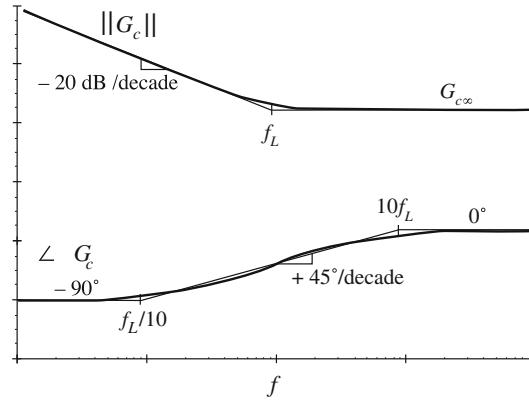


Fig. 9.31 Magnitude and phase asymptotes of the *PI* compensator transfer function G_c of Eq. (9.59)

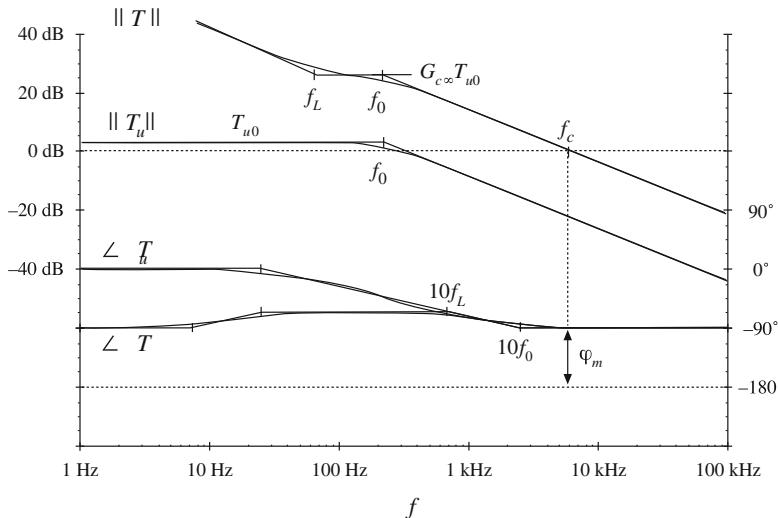


Fig. 9.32 Compensation of a loop gain containing a single pole, using a lag (*PI*) compensator. The loop gain magnitude is increased

f_c . If we approximate the compensated loop gain by its high-frequency asymptote, then at high frequencies we can write

$$\|T\| \approx \frac{T_{u0}G_{c\infty}}{\left(\frac{f}{f_0}\right)} \quad (9.61)$$

At the crossover frequency $f = f_c$, the loop gain has unity magnitude. Equation (9.61) predicts that the crossover frequency is

$$f_c \approx T_{u0}G_{c\infty}f_0 \quad (9.62)$$

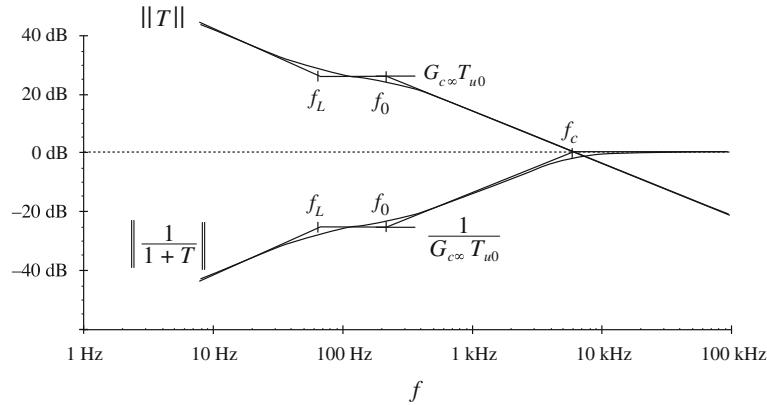


Fig. 9.33 Construction of $\|1/(1+T)\|$, for the *PI*-compensated example of Fig. 9.32

Hence, to obtain a desired crossover frequency f_c , we should choose the compensator gain $G_{c\infty}$ as follows:

$$G_{c\infty} = \frac{f_c}{T_{u0}f_0} \quad (9.63)$$

The corner frequency f_L is then chosen to be sufficiently less than f_c , such that an adequate phase margin is maintained.

Magnitude asymptotes of the quantity $1/(1+T(s))$ are constructed in Fig. 9.33. At frequencies less than f_L , the *PI* compensator improves the rejection of disturbances. At dc, where the magnitude of G_c approaches infinity, the magnitude of $1/(1+T)$ tends to zero. Hence, the closed-loop disturbance-to-output transfer functions, such as Eqs. (9.51) and (9.52), tend to zero at dc.

9.5.3 Combined (*PID*) Compensator

The advantages of the lead and lag compensators can be combined, to obtain both wide bandwidth and zero steady-state error. At low frequencies, the compensator integrates the error signal, leading to large low-frequency loop gain and accurate regulation of the low-frequency components of the output voltage. At high frequency (in the vicinity of the crossover frequency), the compensator introduces phase lead into the loop gain, improving the phase margin. Such a compensator is sometimes called a *PID* controller.

A typical Bode diagram of a practical version of this compensator is illustrated in Fig. 9.34. The compensator has transfer function

$$G_c(s) = G_{cm} \frac{\left(1 + \frac{\omega_L}{s}\right) \left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right)} \quad (9.64)$$

The inverted zero at frequency f_L functions in the same manner as the *PI* compensator. The zero at frequency f_z adds phase lead in the vicinity of the crossover frequency, as in the *PD*

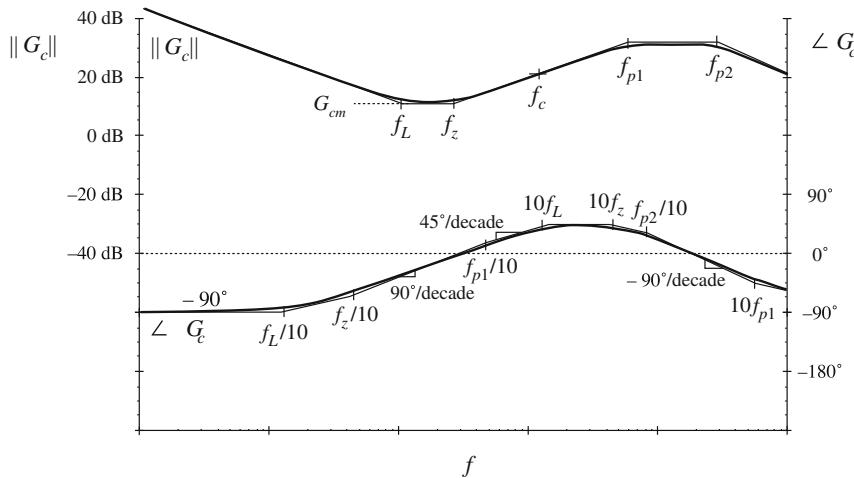


Fig. 9.34 Magnitude and phase asymptotes of the combined (PID) compensator transfer function G_c of Eq. (9.64)

compensator. The high-frequency poles at frequencies f_{p1} and f_{p2} must be present in practical compensators, to cause the gain to roll off at high frequencies and to prevent the switching ripple from disrupting the operation of the pulse-width modulator. The loop gain crossover frequency f_c is chosen to be greater than f_L and f_z , but less than f_{p1} and f_{p2} .

9.5.4 Design Example

To illustrate the design of *PI* and *PD* compensators, let us consider the design of a combined *PID* compensator for the dc–dc buck converter system of Fig. 9.35. The input voltage $v_g(t)$ for this system has nominal value 28 V. It is desired to supply a regulated 15 V to a 5 A load. The load is modeled here with a $3\ \Omega$ resistor. An accurate 5 V reference is available.

The first step is to select the feedback gain $H(s)$. The gain H is chosen such that the regulator produces a regulated 15 V dc output. Let us assume that we will succeed in designing a good feedback system, which causes the output voltage to accurately follow the reference voltage. This is accomplished via a large loop gain T , which leads to a small error voltage: $v_e \approx 0$. Hence, $Hv \approx v_{ref}$. So we should choose

$$H = \frac{V_{ref}}{V} = \frac{15}{28} = \frac{1}{3} \quad (9.65)$$

The quiescent duty cycle is given by the steady-state solution of the converter:

$$D = \frac{V}{V_g} = \frac{15}{28} = 0.536 \quad (9.66)$$

The quiescent value of the control voltage, V_c , must satisfy Eq. (7.85). Hence,

$$V_c = DV_M = 2.14 \text{ V} \quad (9.67)$$

Thus, the quiescent conditions of the system are known. It remains to design the compensator gain $G_c(s)$.

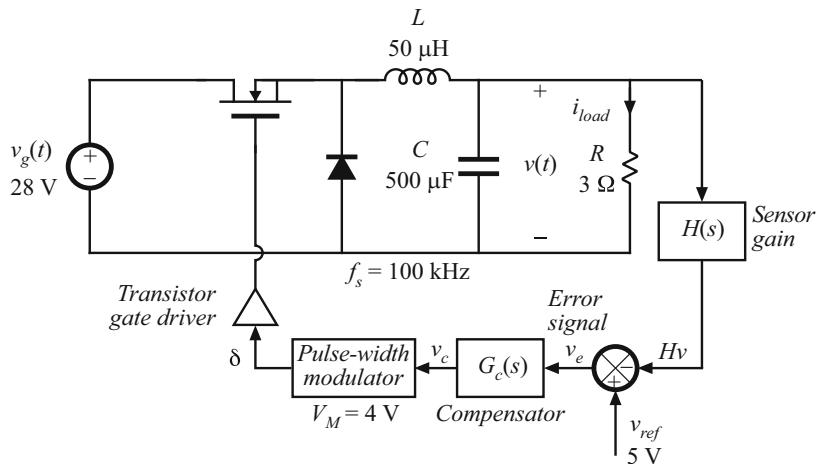


Fig. 9.35 Design example

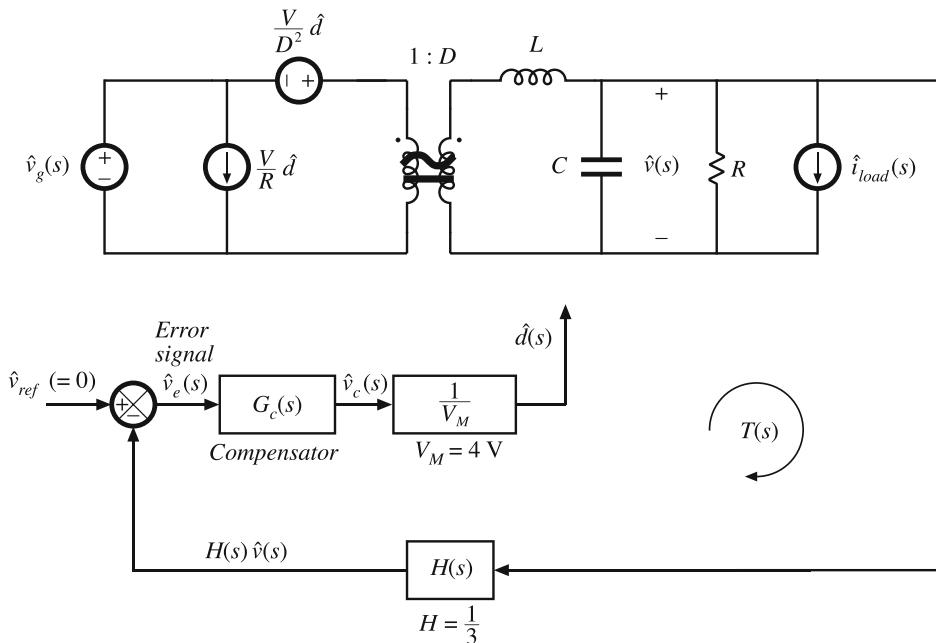


Fig. 9.36 System small-signal ac model, design example

A small-signal ac model of the regulator system is illustrated in Fig. 9.36. The buck converter ac model is represented in canonical form. Disturbances in the input voltage and in the load current are modeled. For generality, reference voltage variations \hat{v}_{ref} are included in the diagram; in a dc voltage regulator, these variations are normally zero.

The open-loop converter transfer functions are discussed in the previous chapters. The open-loop control-to-output transfer function is

$$G_{vd}(s) = \frac{V}{D} \frac{1}{1 + s\frac{L}{R} + s^2LC} \quad (9.68)$$

The open-loop control-to-output transfer function contains two poles, and can be written in the following normalized form:

$$G_{vd}(s) = G_{d0} \frac{1}{1 + \frac{s}{Q_0\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \quad (9.69)$$

By equating like coefficients in Eqs. (9.68) and (9.69), one finds that the dc gain, corner frequency, and Q -factor are given by

$$\begin{aligned} G_{d0} &= \frac{V}{D} = 28 \text{ V} \\ f_0 &= \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{LC}} = 1 \text{ kHz} \\ Q_0 &= R\sqrt{\frac{C}{L}} = 9.5 \Rightarrow 19.5 \text{ dB} \end{aligned} \quad (9.70)$$

In practice, parasitic loss elements, such as the capacitor equivalent series resistance (*esr*), would cause a lower Q -factor to be observed. Figure 9.37 contains a Bode diagram of $G_{vd}(s)$.

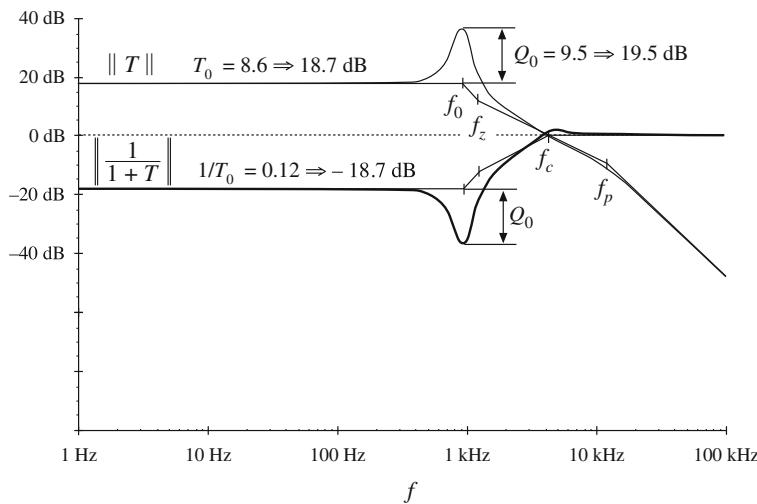


Fig. 9.37 Converter small-signal control-to-output transfer function G_{vd} , design example

The open-loop line-to-output transfer function is

$$G_{vg}(s) = D \frac{1}{1 + s \frac{L}{R} + s^2 LC} \quad (9.71)$$

This transfer function contains the same poles as in $G_{vd}(s)$, and can be written in the normalized form

$$G_{vg}(s) = G_{g0} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0}\right)^2} \quad (9.72)$$

with $G_{g0} = D$. The open-loop output impedance of the buck converter is

$$Z_{out}(s) = R \left| \frac{1}{sC} \right| sL = \frac{sL}{1 + s \frac{L}{R} + s^2 LC} \quad (9.73)$$

Use of these equations to represent the converter in block-diagram form leads to the complete system block diagram of Fig. 9.38. The loop gain of the system is

$$T(s) = G_c(s) \left(\frac{1}{V_M} \right) G_{vd}(s) H(s) \quad (9.74)$$

Substitution of Eq. (9.69) into (9.74) leads to

$$T(s) = \left(\frac{G_c(s) H(s)}{V_M} \right) \left(\frac{V}{D} \right) \frac{1}{\left(1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0} \right)^2 \right)} \quad (9.75)$$

The closed-loop disturbance-to-output transfer functions are given by Eqs. (9.5) and (9.6).

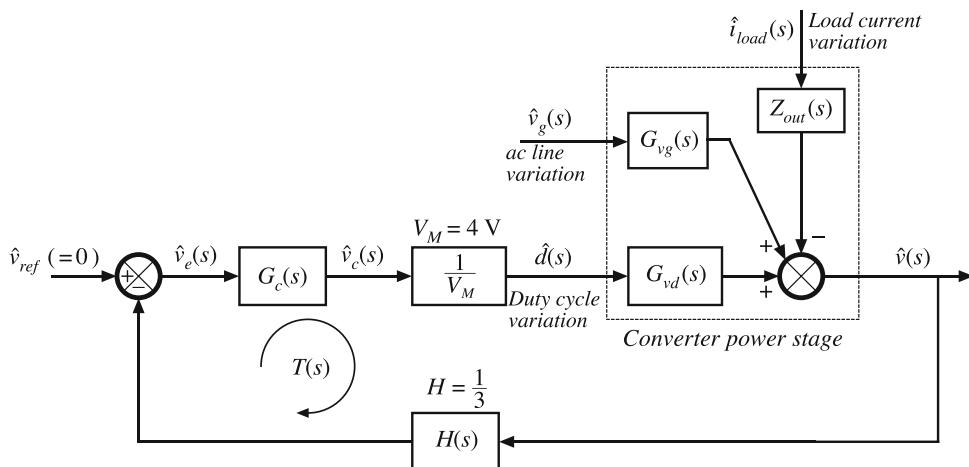


Fig. 9.38 System block diagram, design example

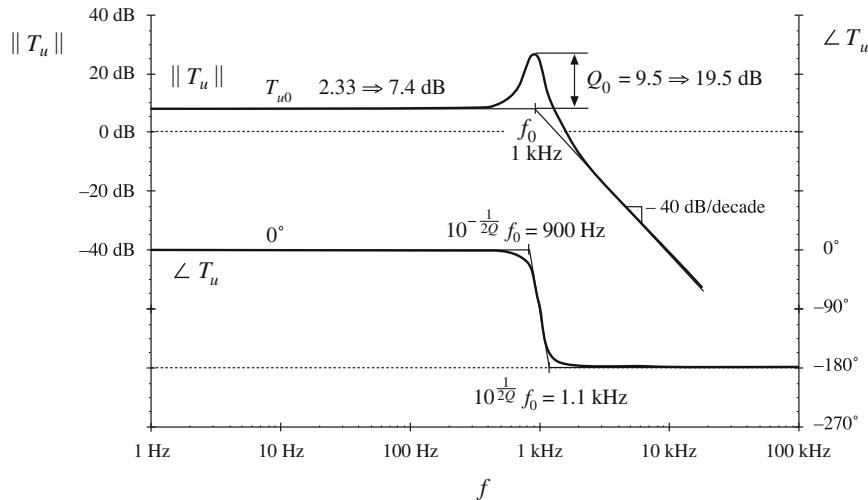


Fig. 9.39 Uncompensated loop gain T_u , design example

The uncompensated loop gain $T_u(s)$, with unity compensator gain, is sketched in Fig. 9.39. With $G_c(s) = 1$, Eq. (9.75) can be written

$$T_u(s) = T_{u0} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0} \right)^2} \quad (9.76)$$

where the dc gain is

$$T_{u0} = \frac{HV}{DV_M} = 2.33 \Rightarrow 7.4 \text{ dB} \quad (9.77)$$

The uncompensated loop gain has a crossover frequency of approximately 1.8 kHz, with a phase margin of less than five degrees.

Let us design a compensator, to attain a crossover frequency of $f_c = 5 \text{ kHz}$, or one twentieth of the switching frequency. From Fig. 9.39, the uncompensated loop gain has a magnitude at 5 kHz of approximately $T_{u0}(f_0/f_c)^2 = 0.093 \Rightarrow -20.6 \text{ dB}$. So to obtain unity loop gain at 5 kHz, our compensator should have a 5 kHz gain of +20.6 dB. In addition, the compensator should improve the phase margin, since the phase of the uncompensated loop gain is nearly -180° at 5 kHz. So a lead (PD) compensator is needed. Let us (somewhat arbitrarily) choose to design for a phase margin of 52° . According to Fig. 9.25, this choice leads to closed-loop poles having a Q -factor of 1. The unit step response, Fig. 9.26, then exhibits a peak overshoot of 16%. Evaluation of Eq. (9.57), with $f_c = 5 \text{ kHz}$ and $\theta = 52^\circ$, leads to the following compensator pole and zero frequencies:

$$f_z = (5 \text{ kHz}) \sqrt{\frac{1 - \sin(52^\circ)}{1 + \sin(52^\circ)}} = 1.7 \text{ kHz} \quad (9.78)$$

$$f_p = (5 \text{ kHz}) \sqrt{\frac{1 + \sin(52^\circ)}{1 - \sin(52^\circ)}} = 14.5 \text{ kHz}$$

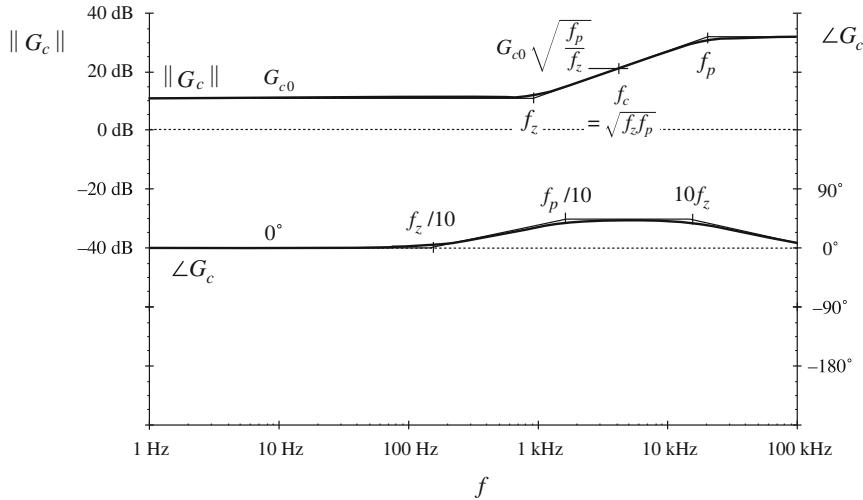


Fig. 9.40 PD compensator transfer function G_c , design example

To obtain a compensator gain of 20.6 dB \Rightarrow 10.7 at 5 kHz, the low-frequency compensator gain must be

$$G_{c0} = \left(\frac{f_c}{f_0}\right)^2 \frac{1}{T_{u0}} \sqrt{\frac{f_z}{f_p}} = 3.7 \Rightarrow 11.3 \text{ dB} \quad (9.79)$$

A Bode diagram of the PD compensator magnitude and phase is sketched in Fig. 9.40.

With this PD controller, the loop gain becomes

$$T(s) = T_{u0}G_{c0} \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)\left(1 + \frac{s}{Q_0\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)} \quad (9.80)$$

The compensated loop gain is sketched in Fig. 9.41. It can be seen that the phase of $T(s)$ is approximately equal to 52° over the frequency range of 1.4 kHz to 17 kHz. Hence variations in component values, which cause the crossover frequency to deviate somewhat from 5 kHz, should have little impact on the phase margin. In addition, it can be seen from Fig. 9.41 that the loop gain has a dc magnitude of $T_{u0}G_{c0} \Rightarrow 18.7$ dB.

Asymptotes of the quantity $1/(1 + T)$ are constructed in Fig. 9.42. This quantity has a dc asymptote of -18.7 dB. Therefore, at frequencies less than 1 kHz, the feedback loop attenuates output voltage disturbances by 18.7 dB. For example, suppose that the input voltage $v_g(t)$ contains a 100 Hz variation of amplitude 1 V. With no feedback loop, this disturbance would propagate to the output according to the open-loop transfer function $G_{vg}(s)$, given in Eq. (9.72).

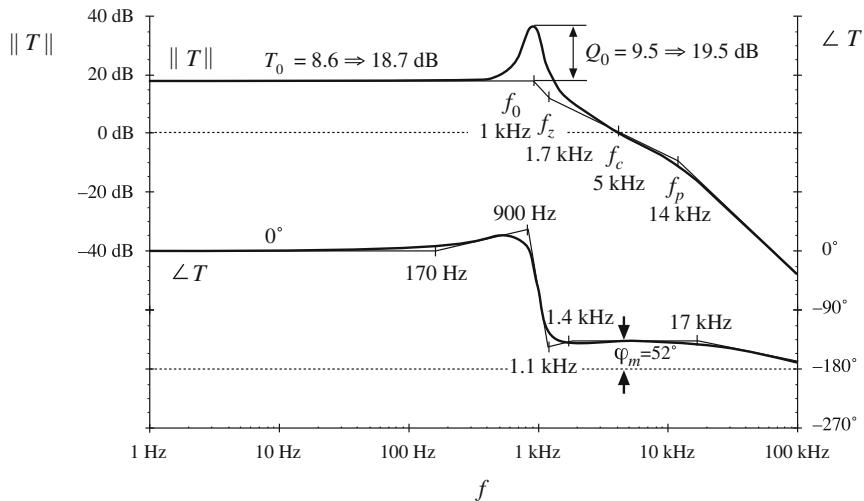


Fig. 9.41 The compensated loop gain of Eq. (9.80)

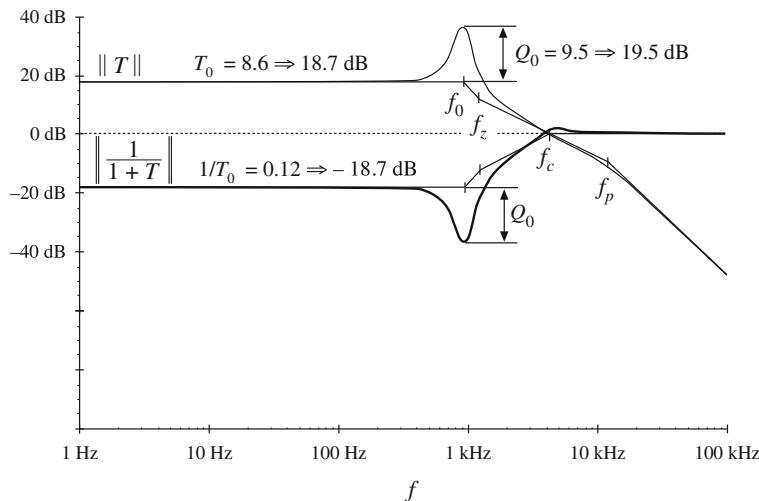


Fig. 9.42 Construction of $\|1/(1+T)\|$ for the PD-compensated design example of Fig. 9.41

At 100 Hz, this transfer function has a gain essentially equal to the dc asymptote $D = 0.536$. Therefore, with no feedback loop, a 100 Hz variation of amplitude 0.536 V would be observed at the output. In the presence of feedback, the closed-loop line-to-output transfer function of Eq. (9.5) is obtained; for our example, this attenuates the 100 Hz variation by an additional factor of $18.7 \text{ dB} \Rightarrow 8.6$. The 100 Hz output voltage variation now has magnitude $0.536/8.6 = 0.062 \text{ V}$.

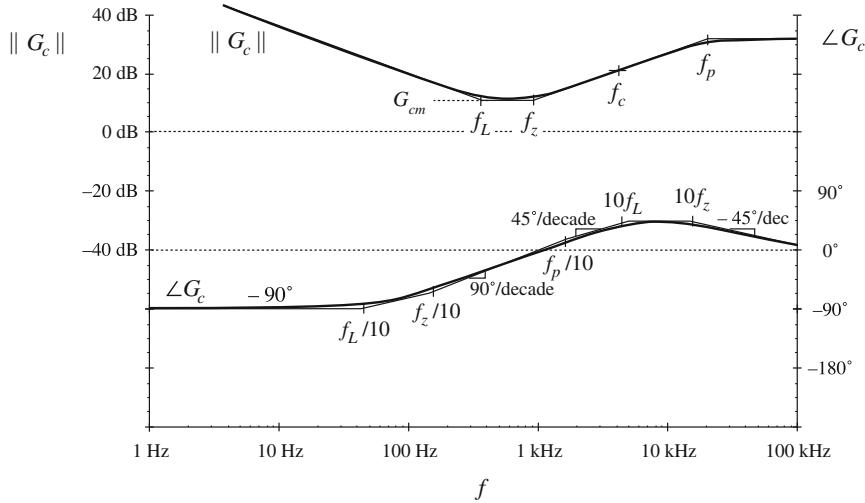


Fig. 9.43 PID compensator transfer function, Eq. (9.81)

The low-frequency regulation can be further improved by addition of an inverted zero, as discussed in Sect. 9.5.2. A *PID* controller, as in Sect. 9.5.3, is then obtained. The compensator transfer function becomes

$$G_c(s) = G_{cm} \frac{\left(1 + \frac{s}{\omega_z}\right)\left(1 + \frac{\omega_L}{s}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \quad (9.81)$$

The Bode diagram of this compensator gain is illustrated in Fig. 9.43. The pole and zero frequencies f_z and f_p are unchanged, and are given by Eq. (9.78). The midband gain G_{cm} is chosen to be the same as the previous G_{c0} , Eq. (9.79). Hence, for frequencies greater than f_L , the magnitude of the loop gain is unchanged by the inverted zero. The loop continues to exhibit a crossover frequency of 5 kHz.

So that the inverted zero does not significantly degrade the phase margin, let us (somewhat arbitrarily) choose f_L to be one-tenth of the crossover frequency, or 500 Hz. The inverted zero will then increase the loop gain at frequencies below 500 Hz, improving the low-frequency regulation of the output voltage. The loop gain of Fig. 9.44 is obtained. The magnitude of the quantity $1/(1+T)$ is also constructed. It can be seen that the inverted zero at 500 Hz causes the magnitude of $1/(1+T)$ at 100 Hz to be reduced by a factor of approximately $(100 \text{ Hz})/(500 \text{ Hz}) = 1/5$. The total attenuation of $1/(1+T)$ at 100 Hz is -32.7 dB . A 1 V, 100 Hz variation in $v_g(t)$ would now induce a 12 mV variation in $v(t)$. Further improvements could be obtained by increasing f_L ; however, this would require redesign of the *PD* portion of the compensator to maintain an adequate phase margin.

The line-to-output transfer function is constructed in Fig. 9.45. Both the open-loop transfer function $G_{vg}(s)$, Eq. (9.72), and the closed-loop transfer function $G_{vg}(s)/(1+T(s))$, are constructed using the algebra-on-the-graph method. The two transfer functions coincide at frequencies greater than the crossover frequency. At frequencies less than the crossover frequency f_c ,

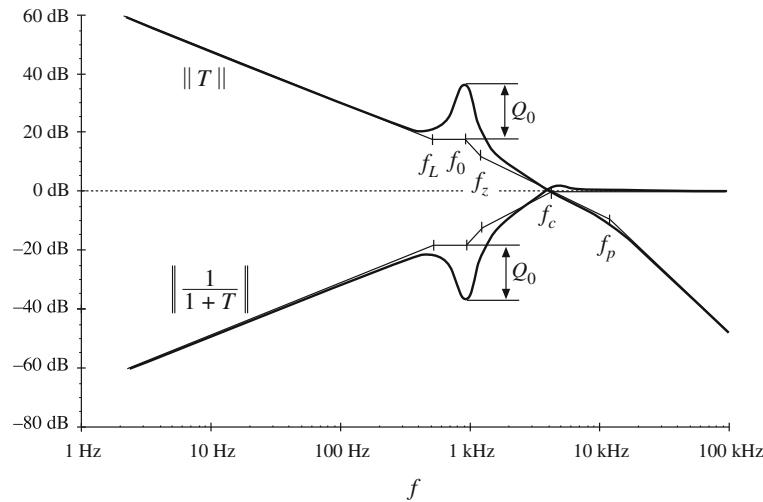


Fig. 9.44 Construction of $\|T\|$ and $\|1/(1+T)\|$ with the PID compensator of Fig. 9.43

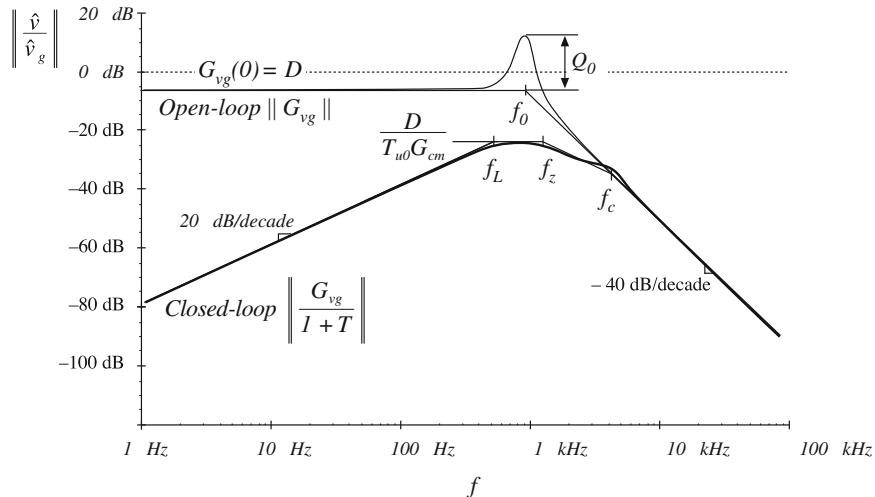


Fig. 9.45 Comparison of open-loop line-to-output transfer function G_{vg} and the closed-loop line-to-output transfer function of Eq. (9.82)

the closed-loop transfer function is reduced by a factor of $T(s)$. It can be seen that the poles of $G_{vg}(s)$ are cancelled by zeroes of $1/(1+T)$. Hence the closed-loop line-to-output transfer function is approximately

$$\frac{G_{vg}(s)}{(1+T(s))} \approx \frac{D}{T_{u0}G_{cm}} \frac{1}{\left(1 + \frac{\omega_L}{s}\right)\left(1 + \frac{s}{\omega_z}\right)\left(1 + \frac{s}{\omega_c}\right)} \quad (9.82)$$

So the algebra-on-the-graph method allows simple approximate disturbance-to-output closed-loop transfer functions to be written. Armed with such an analytical expression, the system designer can easily compute the output disturbances, and can gain the insight required to shape the loop gain $T(s)$ such that system specifications are met. Computer simulations can then be used to judge whether the specifications are met under all operating conditions, and over expected ranges of component parameter values. Results of computer simulations of the design example described in this section can be found in Sect. 15.4.2.

9.6 Measurement of Loop Gains

It is a good engineering practice to measure the loop gains of prototype feedback systems. The objective of such an exercise is to verify that the system has been correctly modeled. If so, then provided that a good controller design has been implemented, then the system behavior will meet expectations regarding transient overshoot (and phase margin), rejection of disturbances, dc output voltage regulation, etc. Unfortunately, there are reasons why practical system prototypes are likely to differ from theoretical models. Phenomena may occur that were not accounted for in the original model, and that significantly influence the system behavior. Noise and electromagnetic interference (EMI) can be present, which cause the system transfer functions to deviate in unexpected ways.

So let us consider the measurement of the loop gain $T(s)$ of the feedback system of Fig. 9.46. We will make measurements at some point A , where two blocks of the network are connected electrically. In Fig. 9.46, the output port of block 1 is represented by a Thevenin-equivalent network, composed of the dependent voltage source $G_1 \hat{v}_e$ and output impedance Z_1 . Block 1 is loaded by the input impedance Z_2 of block 2. The remainder of the feedback system is represented by a block diagram as shown. The loop gain of the system is

$$T(s) = G_1(s) \left(\frac{Z_2(s)}{Z_1(s) + Z_2(s)} \right) G_2(s) H(s) \quad (9.83)$$

Measurement of this loop gain presents several challenges not present in other frequency response measurements.

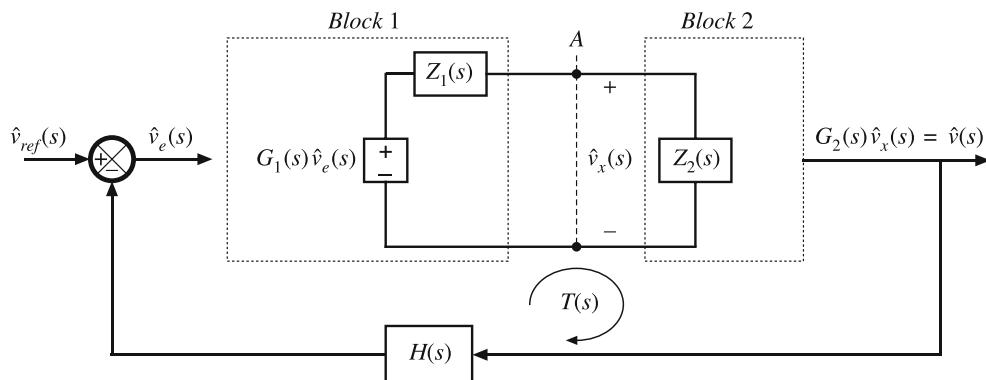


Fig. 9.46 It is desired to determine the loop gain $T(s)$ experimentally, by making measurements at point A

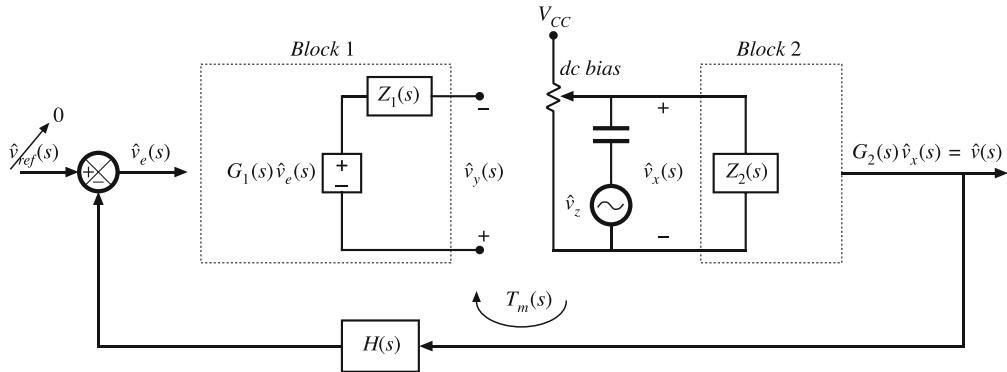


Fig. 9.47 Measurement of loop gain by breaking the loop

In principle, one could break the loop at point A , and attempt to measure $T(s)$ using the transfer function measurement method of the previous chapter. As illustrated in Fig. 9.47, a dc supply voltage V_{CC} and potentiometer would be used, to establish a dc bias in the voltage v_x , such that all of the elements of the network operate at the correct quiescent point. Ac voltage variations in $v_z(t)$ are coupled into the injection point via a dc blocking capacitor. Any other independent ac inputs to the system are disabled. A network analyzer is used to measure the relative magnitudes and phases of the ac components of the voltages $v_y(t)$ and $v_x(t)$:

$$T_m(s) = \left. \frac{\hat{v}_y(s)}{\hat{v}_x(s)} \right|_{\substack{\hat{v}_{ref}=0 \\ \hat{v}_g=0}} \quad (9.84)$$

The measured gain $T_m(s)$ differs from the actual gain $T(s)$ because, by breaking the connection between blocks 1 and 2 at the measurement point, we have removed the loading of block 2 on block 1. Solution of Fig. 9.47 for the measured gain $T_m(s)$ leads to

$$T_m(s) = G_1(s)G_2(s)H(s) \quad (9.85)$$

Equations (9.83) and (9.85) can be combined to express $T_m(s)$ in terms of $T(s)$:

$$T_m(s) = T(s) \left(1 + \frac{Z_1(s)}{Z_2(s)} \right) \quad (9.86)$$

Hence,

$$T_m(s) \approx T(s) \text{ provided that } \|Z_2\| \gg \|Z_1\| \quad (9.87)$$

So to obtain an accurate measurement, we need to find an injection point where loading is negligible over the range of frequencies to be measured.

Other difficulties are encountered when using the method of Fig. 9.47. The most serious problem is adjustment of the dc bias using a potentiometer. The dc loop gain is typically very large, especially when a PI controller is used. A small change in the dc component of $v_x(t)$ can therefore lead to very large changes in the dc biases of some elements in the system. So it is difficult to establish the correct dc conditions in the circuit. The dc gains may drift during the experiment, making the problem even worse, and saturation of the error amplifier is a common complaint. Also, we have seen that the gains of the converter can be a function of the quiescent operating point; significant deviation from the correct operating point can cause the measured gain to differ from the loop gain of actual operating conditions.

9.6.1 Voltage Injection

An approach that avoids the dc biasing problem [84] is illustrated in Fig. 9.48. The voltage source $v_z(t)$ is injected between blocks 1 and 2, without breaking the feedback loop. Ac variations in $v_z(t)$ again excite variations in the feedback system, but dc bias conditions are determined by the circuit. Indeed, if $v_z(t)$ contains no dc component, then the biasing circuits of the system itself establish the quiescent operating point. Hence, the loop gain measurement is made at the actual system operating point.

The injection source is modeled in Fig. 9.48 by a Thevenin equivalent network, containing an independent voltage source with source impedance $Z_s(s)$. The magnitudes of v_z and Z_s are irrelevant in the determination of the loop gain. However, the injection of v_z does disrupt the loading of block 2 on block 1. Hence, a suitable injection point must be found, where the loading effect is negligible.

To measure the loop gain by voltage injection, we connect a network analyzer to measure the transfer function from \hat{v}_x to \hat{v}_y . The system independent ac inputs are set to zero, and the network analyzer sweeps the injection voltage $\hat{v}_z(t)$ over the intended frequency range. The measured gain is

$$T_v(s) = \left. \frac{\hat{v}_y(s)}{\hat{v}_x(s)} \right|_{\begin{subarray}{l} \hat{v}_{ref}=0 \\ \hat{v}_g=0 \end{subarray}} \quad (9.88)$$

Let us solve Fig. 9.48, to compare the measured gain $T_v(s)$ with the actual loop gain $T(s)$ given by (9.83). The error signal is

$$\hat{v}_e(s) = -H(s)G_2(s)\hat{v}_x(s) \quad (9.89)$$

The voltage \hat{v}_y can be written

$$-\hat{v}_y(s) = G_1(s)\hat{v}_e(s) - \hat{i}(s)Z_1(s) \quad (9.90)$$

where $\hat{i}(s)Z_1(s)$ is the voltage drop across the source impedance Z_1 . Substitution of Eq. (9.89) into (9.90) leads to

$$-\hat{v}_y(s) = -\hat{v}_x(s)G_2(s)H(s)G_1(s) - \hat{i}(s)Z_1(s) \quad (9.91)$$

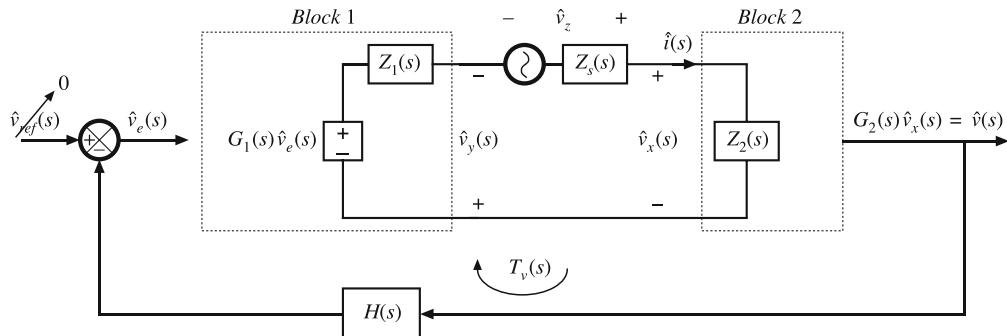


Fig. 9.48 Measurement of loop gain by voltage injection

But $\hat{i}(s)$ is

$$\hat{i}(s) = \frac{\hat{v}_x(s)}{Z_2(s)} \quad (9.92)$$

Therefore, Eq. (9.91) becomes

$$\hat{v}_y(s) = \hat{v}_x(s) \left(G_1(s)G_2(s)H(s) + \frac{Z_1(s)}{Z_2(s)} \right) \quad (9.93)$$

Substitution of Eq. (9.93) into (9.88) leads to the following expression for the measured gain $T_v(s)$:

$$T_v(s) = G_1(s)G_2(s)H(s) + \frac{Z_1(s)}{Z_2(s)} \quad (9.94)$$

Equations (9.83) and (9.94) can be combined to determine the measured gain $T_v(s)$ in terms of the actual loop gain $T(s)$:

$$T_v(s) = T(s) \left(1 + \frac{Z_1(s)}{Z_2(s)} \right) + \frac{Z_1(s)}{Z_2(s)} \quad (9.95)$$

Thus, $T_v(s)$ can be expressed as the sum of two terms. The first term is proportional to the actual loop gain $T(s)$, and is approximately equal to $T(s)$ whenever $\| Z_1 \| \ll \| Z_2 \|$. The second term is not proportional to $T(s)$, and limits the minimum $T(s)$ that can be measured with the voltage injection technique. If Z_1/Z_2 is much smaller in magnitude than $T(s)$, then the second term can be ignored, and $T_v(s) \approx T(s)$. At frequencies where $T(s)$ is smaller in magnitude than Z_1/Z_2 , the measured data must be discarded. Thus,

$$T_v(s) \approx T(s) \quad (9.96)$$

provided

$$(i) \| Z_1(s) \| \ll \| Z_2(s) \|$$

and

$$(ii) \| T(s) \| \gg \left\| \frac{Z_1(s)}{Z_2(s)} \right\|$$

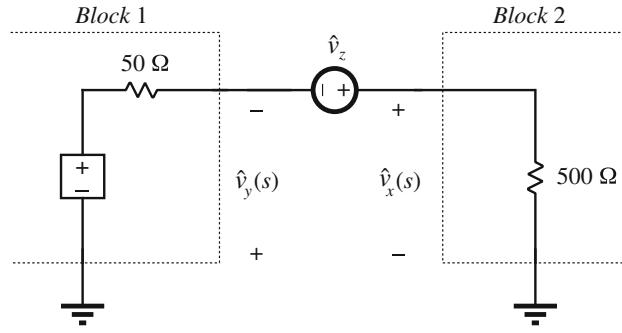
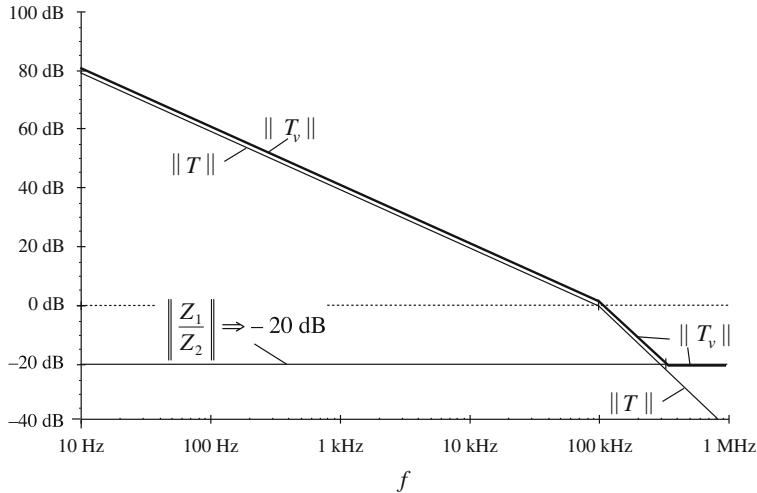
Again, note that the value of the injection source impedance Z_s is irrelevant.

As an example, consider voltage injection at the output of an operational amplifier, having a 50Ω output impedance, which drives a 500Ω effective load. The system in the vicinity of the injection point is illustrated in Fig. 9.49. So $Z_1(s) = 50 \Omega$ and $Z_2(s) = 500 \Omega$. The ratio Z_1/Z_2 is 0.1, or -20 dB. Let us further suppose that the actual loop gain $T(s)$ contains poles at 10 Hz and 100 kHz, with a dc gain of 80 dB. The actual loop gain magnitude is illustrated in Fig. 9.50.

Voltage injection would result in measurement of $T_v(s)$ given in Eq. (9.95). Note that

$$\left(1 + \frac{Z_1(s)}{Z_2(s)} \right) = 1.1 \Rightarrow 0.83 \text{ dB} \quad (9.97)$$

Hence, for large $\| T \|$, the measured $\| T_v \|$ deviates from the actual loop gain by less than 1 dB. However, at high frequency where $\| T \|$ is less than -20 dB, the measured gain differs significantly. Apparently, $T_v(s)$ contains two high-frequency zeroes that are not present in $T(s)$. Depending on the Q -factor of these zeroes, the phase of T_v at the crossover frequency could be influenced. To ensure that the phase margin is correctly measured, it is important that Z_1/Z_2 be sufficiently small in magnitude.

**Fig. 9.49** Voltage injection example**Fig. 9.50** Comparison of measured loop gain T_v and actual loop gain T , voltage injection example. The measured gain deviates at high frequency

9.6.2 Current Injection

The results of the preceding paragraphs can also be obtained in dual form, where the loop gain is measured by current injection [84]. As illustrated in Fig. 9.51, we can model block 1 and the analyzer injection source by their Norton equivalents, and use current probes to measure \hat{i}_x and \hat{i}_y . The gain measured by current injection is

$$T_i(s) = \left. \frac{\hat{i}_y(s)}{\hat{i}_x(s)} \right|_{\begin{subarray}{l} \hat{v}_{ref}=0 \\ \hat{v}_g=0 \end{subarray}} \quad (9.98)$$

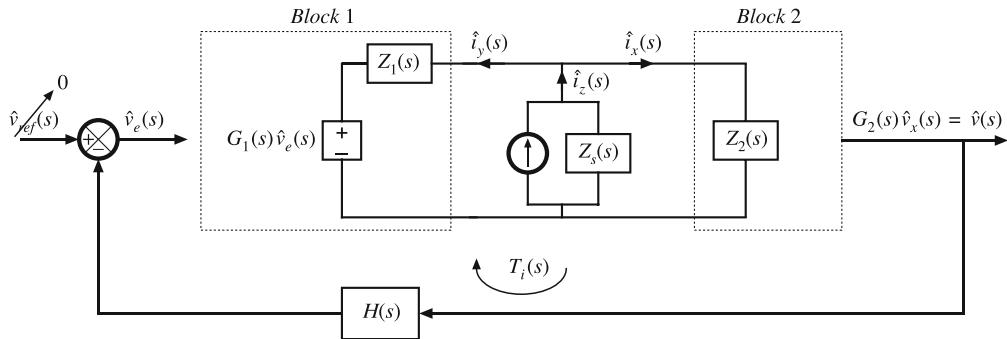


Fig. 9.51 Measurement of loop gain by current injection

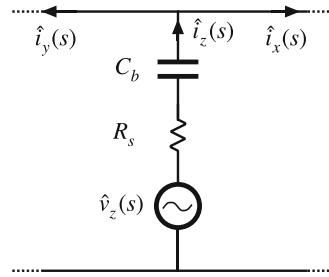


Fig. 9.52 Current injection using Thevenin-equivalent source

It can be shown that

$$T_i(s) = T(s) \left(1 + \frac{Z_2(s)}{Z_1(s)} \right) + \frac{Z_2(s)}{Z_1(s)} \quad (9.99)$$

Hence,

$$T_i(s) \approx T(s) \text{ provided}$$

$$(i) \|Z_2(s)\| \ll \|Z_1(s)\|, \text{ and} \quad (9.100)$$

$$(ii) \|T(s)\| \gg \left\| \frac{Z_2(s)}{Z_1(s)} \right\|$$

So to obtain an accurate measurement of the loop gain by current injection, we must find a point in the network where block 2 has sufficiently small input impedance. Again, note that the injection source impedance Z_s does not affect the measurement. In fact, we can realize i_z by use of a Thevenin-equivalent source, as illustrated in Fig. 9.52. The network analyzer injection source is represented by voltage source $\hat{v}_z(s)$ and output resistance R_s . A series capacitor, C_b , is inserted to avoid disrupting the dc bias at the injection point.

9.6.3 Measurement of Unstable Systems

When the prototype feedback system is unstable, we are even more eager to measure the loop gain—to find out what went wrong. But measurements cannot be made while the system oscillates.

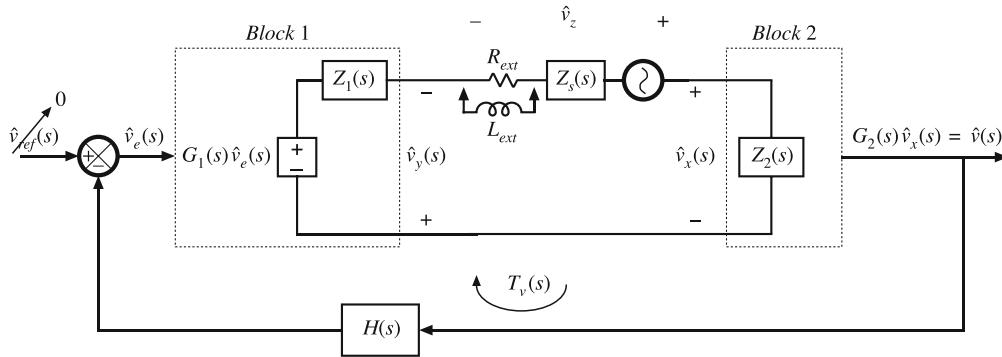


Fig. 9.53 Measurement of an unstable loop gain by voltage injection

lates. We need to stabilize the system, yet measure the original unstable loop gain. It is possible to do this by recognizing that the injection source impedance Z_s does not influence the measured loop gain [84]. As illustrated in Fig. 9.53, we can even add additional resistance R_{ext} , effectively increasing the source impedance Z_s . The measured loop gain $T_v(s)$ is unaffected.

Adding series impedance generally lowers the loop gain of a system, leading to a lower crossover frequency and a more positive phase margin. Hence, it is usually possible to add a resistor R_{ext} that is sufficiently large to stabilize the system. The gain $T_v(s)$, Eq. (9.88), continues to be approximately equal to the original unstable loop gain, according to Eq. (9.96). To avoid disturbing the dc bias conditions, it may be necessary to bypass R_{ext} with inductor L_{ext} . If the inductance value is sufficiently large, then it will not influence the stability of the modified system.

9.7 Summary of Key Points

1. Negative feedback causes the system output to closely follow the reference input, according to the gain $1/H(s)$. The influence on the output of disturbances and variation of gains in the forward path is reduced.
2. The loop gain $T(s)$ is equal to the products of the gains in the forward and feedback paths. The loop gain is a measure of how well the feedback system works: a large loop gain leads to better regulation of the output. The crossover frequency f_c is the frequency at which the loop gain T has unity magnitude, and is a measure of the bandwidth of the control system.
3. The introduction of feedback causes the transfer functions from disturbances to the output to be multiplied by the factor $1/(1 + T(s))$. At frequencies where T is large in magnitude (i.e., below the crossover frequency), this factor is approximately equal to $1/T(s)$. Hence, the influence of low-frequency disturbances on the output is reduced by a factor of $1/T(s)$. At frequencies where T is small in magnitude (i.e., above the crossover frequency), the factor is approximately equal to 1. The feedback loop then has no effect. Closed-loop disturbance-to-output transfer functions, such as the line-to-output transfer function or the output impedance, can easily be constructed using the algebra-on-the-graph method.
4. Stability can be assessed using the phase margin test. The phase of T is evaluated at the crossover frequency, and the stability of the important closed-loop quantities $T/(1 + T)$ and $1/(1 + T)$ is then deduced. Inadequate phase margin leads to ringing and overshoot in the system transient response, and peaking in the closed-loop transfer functions.

5. Compensators are added in the forward paths of feedback loops to shape the loop gain, such that desired performance is obtained. Lead compensators, or *PD* controllers, are added to improve the phase margin and extend the control system bandwidth. *PI* controllers are used to increase the low-frequency loop gain, to improve the rejection of low-frequency disturbances and reduce the steady-state error.
6. Loop gains can be experimentally measured by use of voltage or current injection. This approach avoids the problem of establishing the correct quiescent operating conditions in the system, a common difficulty in systems having a large dc loop gain. An injection point must be found where interstage loading is not significant. Unstable loop gains can also be measured.

PROBLEMS

9.1 Derive both forms of Eq. (9.41).

9.2 The flyback converter system of Fig. 9.54 contains a feedback loop for regulation of the main output voltage v_1 . An auxiliary output produces voltage v_2 . The dc input voltage v_g lies in the range $280 \text{ V} \leq v_g \leq 380 \text{ V}$. The compensator network has transfer function

$$G_c(s) = G_{c\infty} \left(1 + \frac{\omega_1}{s} \right)$$

where $G_{c\infty} = 0.05$, and $f_1 = \omega_1/2\pi = 400 \text{ Hz}$.

- (a) What is the steady-state value of the error voltage $v_e(t)$? Explain your reasoning.
- (b) Determine the steady-state value of the main output voltage v_1 .
- (c) Estimate the steady-state value of the auxiliary output voltage v_2 .

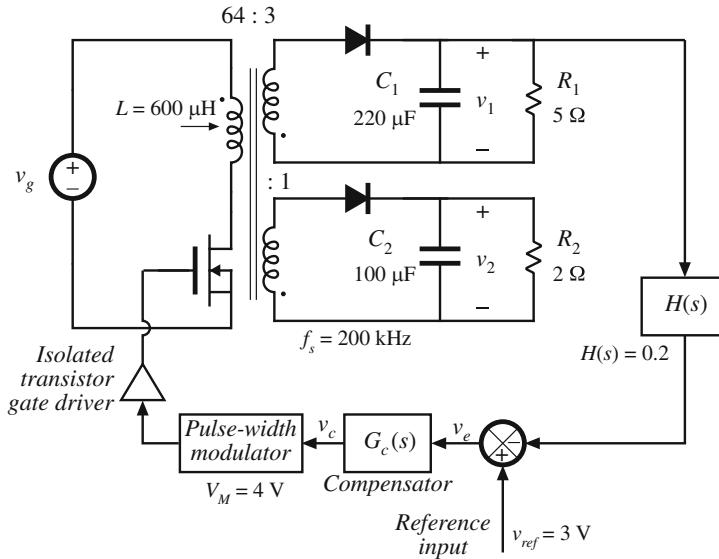


Fig. 9.54 Flyback converter system of Problem 9.2

- 9.3** In the boost converter system of Fig. 9.55, all elements are ideal. The compensator has gain $G_c(s) = 250/s$.

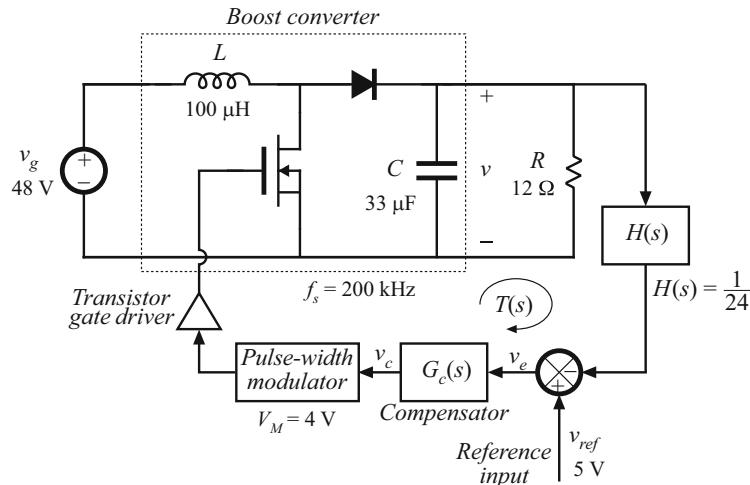


Fig. 9.55 Boost converter system of Problem 9.3

- Construct the Bode plot of the loop gain $T(s)$ magnitude and phase. Label values of all corner frequencies and Q -factors, as appropriate.
- Determine the crossover frequency and phase margin.
- Construct the Bode diagram of the magnitude of $1/(1 + T)$, using the algebra-on-the-graph method. Label values of all corner frequencies and Q -factors, as appropriate.
- Construct the Bode diagram of the magnitude of the closed-loop line-to-output transfer function. Label values of all corner frequencies and Q -factors, as appropriate.

- 9.4** A certain inverter system has the following loop gain

$$T(s) = T_0 \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)\left(1 + \frac{s}{\omega_3}\right)}$$

and the following open-loop line-to-output transfer function

$$G_{vg}(s) = G_{g0} \frac{1}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)\left(1 + \frac{s}{\omega_3}\right)}$$

where

$T_0 = 100$	$\omega_1 = 500 \text{ rad/sec}$
$\omega_2 = 1000 \text{ rad/sec}$	$\omega_3 = 24000 \text{ rad/sec}$
$\omega_z = 4000 \text{ rad/sec}$	$G_{g0} = 0.5$

The gain of the feedback connection is $H(s) = 0.1$.

- (a) Sketch the magnitude and phase asymptotes of the loop gain $T(s)$. Determine numerical values of the crossover frequency in Hz and phase margin in degrees.
- (b) Construct the magnitude asymptotes of the closed-loop line-to-output transfer function. Label important features.
- (c) Construct the magnitude asymptotes of the closed-loop transfer function from the reference voltage to the output voltage. Label important features.

9.5 The forward converter system of Fig. 9.56a is constructed with the element values shown. The quiescent value of the input voltage is $V_g = 380$ V. The transformer has turns ratio $n_1/n_3 = 4.5$. The duty cycle produced by the pulse-width modulator is restricted to the range $0 \leq d(t) \leq 0.5$. Within this range, $d(t)$ follows the control voltage $v_c(t)$ according to

$$d(t) = \frac{1}{2} \frac{v_c(t)}{V_M}$$

with $V_M = 3$ V.

- (a) Determine the quiescent values of: the duty cycle D , the output voltage V , and the control voltage V_c .

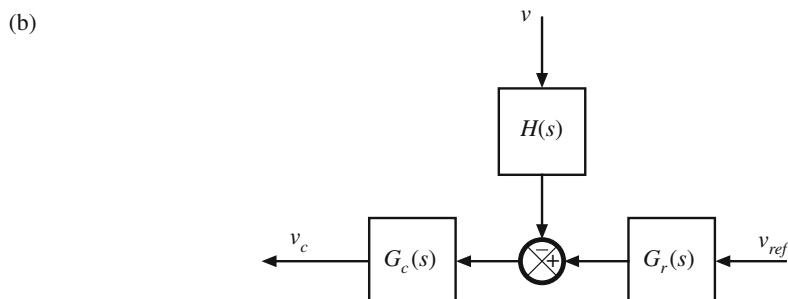
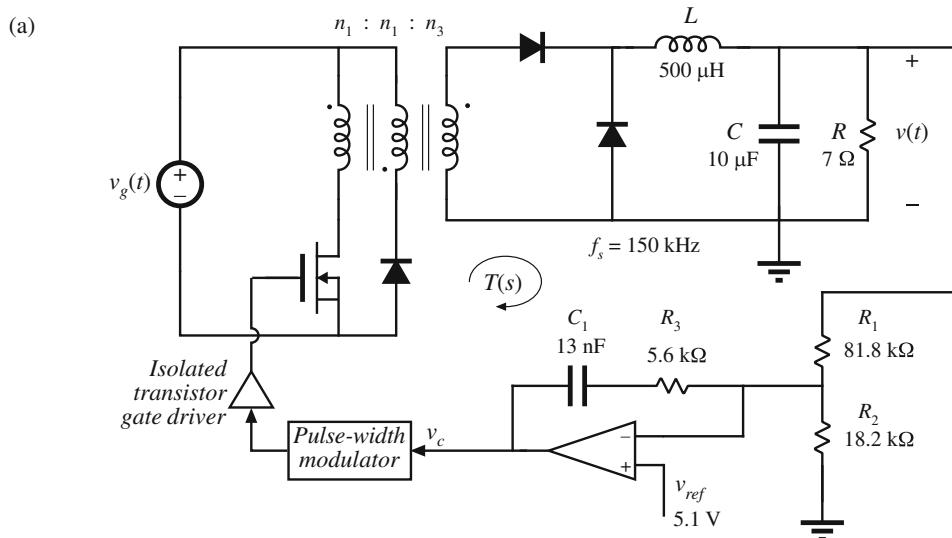


Fig. 9.56 Forward converter system of Problem 9.5: (a) system diagram, (b) modeling the op amp circuit using a block diagram

- (b) The op-amp circuit and feedback connection can be modeled using the block diagram illustrated in Fig. 9.56b, with $H(s) = R_2/(R_1 + R_2)$. Determine the transfer functions $G_c(s)$ and $G_r(s)$.
- (c) Sketch a block diagram which models the small-signal ac variations of the complete system, and determine the transfer function of each block. Hint: the transformer magnetizing inductance has negligible influence on the converter dynamics, and can be ignored. The small-signal models of the forward and buck converters are similar.
- (d) Construct a Bode plot of the loop gain magnitude and phase. What is the crossover frequency? What is the phase margin?
- (e) Construct the Bode plot of the closed-loop line-to-output transfer function magnitude

$$\left\| \frac{\hat{v}}{\hat{v}_g} \right\|$$

Label important features. What is the gain at 120 Hz? At what frequency do disturbances in v_g have the greatest influence on the output voltage?

- 9.6** In the voltage regulator system of Fig. 9.56, described in Problem 9.5, the input voltage $v_g(t)$ contains a 120 Hz variation of peak amplitude 10 V.

- (a) What is the amplitude of the resulting 120 Hz variation in $v(t)$?
 (b) Modify the compensator network such that the 120 Hz output voltage variation has peak amplitude less than 25 mV. Your modification should leave the dc output voltage unchanged, and should result in a crossover frequency no greater than 10 kHz.

- 9.7** Design of a boost converter with current feedback and a *PI* compensator. In some applications, it is desired to control the converter input terminal current waveform. The boost converter system of Fig. 9.57 contains a feedback loop which causes the converter input current $i_g(t)$ to be proportional to a reference voltage $v_{ref}(t)$. The feedback connection is a current sense circuit having gain $H(s) = 0.2$ volts per ampere. A conventional pulse width modulator circuit (Fig. 7.29) is employed, having a sawtooth waveform with peak-peak amplitude of $V_M = 3$ V. The quiescent values of the inputs are: $V_g = 120$ V, $V_{ref} = 2$ V. All elements are ideal.

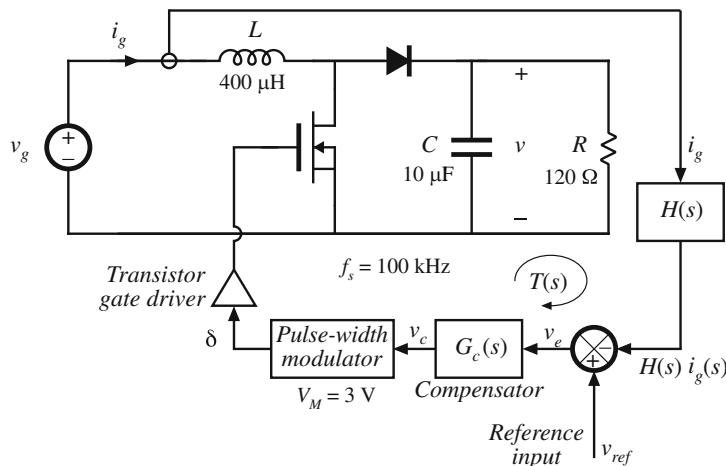


Fig. 9.57 Boost converter system with current feedback, Problem 9.7

- (a) Determine the quiescent values D , V , and I_g .
 (b) Determine the small-signal transfer function

$$G_{id}(s) = \frac{\hat{i}_g(s)}{\hat{d}(s)}$$

- (c) Sketch the magnitude and phase asymptotes of the uncompensated ($G_c(s) = 1$) loop gain.
 (d) It is desired to obtain a loop gain magnitude of at least 35 dB at 120 Hz, while maintaining a phase margin of at least 72° . The crossover frequency should be no greater than $f_s/10 = 10$ kHz. Design a PI compensator that accomplishes this. Sketch the magnitude and phase asymptotes of the resulting loop gain, and label important features.
 (e) For your design of part (d), sketch the magnitude of the closed-loop transfer function

$$\frac{\hat{i}_g(s)}{\hat{v}_{ref}(s)}$$

Label important features.

- 9.8** Design of a buck regulator to meet closed-loop output impedance specifications. The buck converter with control system illustrated in Fig. 9.58 is to be designed to meet the following specifications. The closed-loop output impedance should be less than 0.2Ω over the entire frequency range 0 to 20 kHz. To ensure that the transient response is well-behaved, the poles of the closed-loop transfer functions, in the vicinity of the crossover frequency, should have Q -factors no greater than unity. The quiescent load current I_{LOAD} can vary from 5 A to 50 A, and the above specifications must be met for every value of I_{LOAD} in this range. For simplicity, you may assume that the input voltage v_g does not vary. The loop gain crossover frequency f_c may be chosen to be no greater than $f_s/10$, or 10 kHz. You may also assume that all elements are ideal. The pulse-width modulator circuit obeys Eq. (7.85).

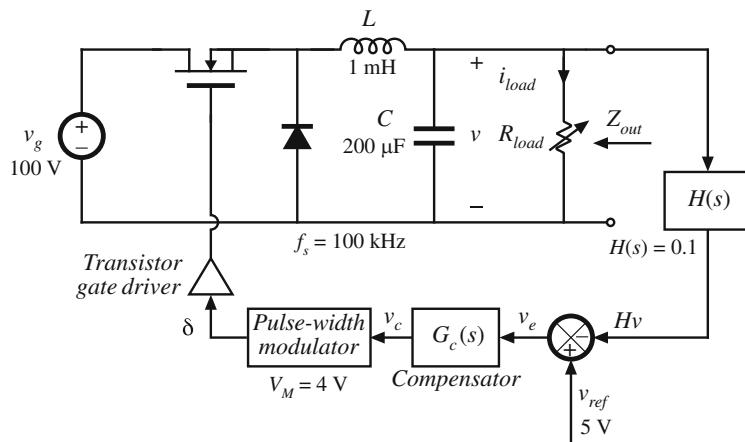


Fig. 9.58 Buck regulator system, Problem 9.8

- (a) What is the intended dc output voltage V ? Over what range does the effective load resistance R_{LOAD} vary?
- (b) Construct the magnitude asymptotes of the open-loop output impedance $Z_{out}(s)$. Over what range of frequencies is the output impedance specification not met? Hence, deduce how large the minimum loop gain $T(s)$ must be in magnitude, such that the closed-loop output impedance meets the specification. Choose a suitable crossover frequency f_c .
- (c) Design a compensator network $G_c(s)$ such that all specifications are met. Additionally, the dc loop gain $T(s)$ should be at least 20 dB. Specify the following:
- Your choice for the transfer function $G_c(s)$
 - The worst-case closed-loop Q
 - Bode plots of the loop gain $T(s)$ and the closed-loop output impedance, for load currents of 5 A and 50 A. What effect does variation of R_{LOAD} have on the closed-loop behavior of your design?
- (d) Design a circuit using resistors, capacitors, and an op amp to realize your compensator transfer function $G_c(s)$.
- 9.9** Design of a buck–boost voltage regulator. The buck–boost converter of Fig. 9.59 operates in the continuous conduction mode, with the element values shown. The nominal input voltage is $V_g = 48$ V, and it is desired to regulate the output voltage at -15 V. Design the best compensator that you can, which has high crossover frequency (but no greater than 10% of the switching frequency), large loop gain over the bandwidth of the feedback loop, and phase margin of at least 52° .
- (a) Specify the required value of H . Sketch Bode plots of the uncompensated loop gain magnitude and phase, as well as the magnitude and phase of your proposed compensator transfer function $G_c(s)$. Label the important features of your plots.
- (b) Construct Bode diagrams of the magnitude and phase of your compensated loop gain $T(s)$, and also of the magnitude of the quantities $T/(1 + T)$ and $1/(1 + T)$.
- (c) Discuss your design. What prevents you from further increasing the crossover frequency? How large is the loop gain at 120 Hz? Can you obtain more loop gain at 120 Hz?

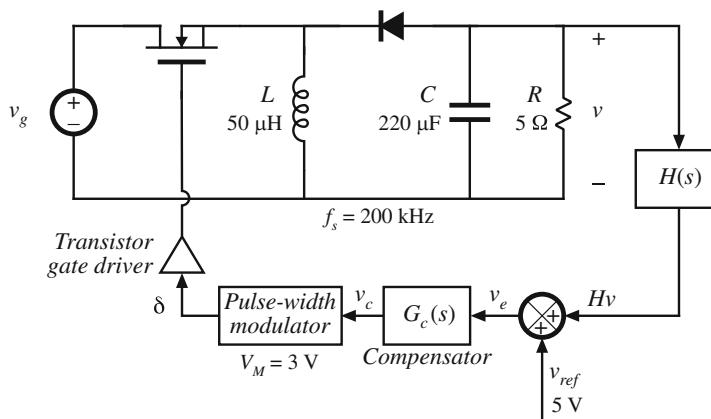


Fig. 9.59 Buck–boost voltage regulator system, Problem 9.9

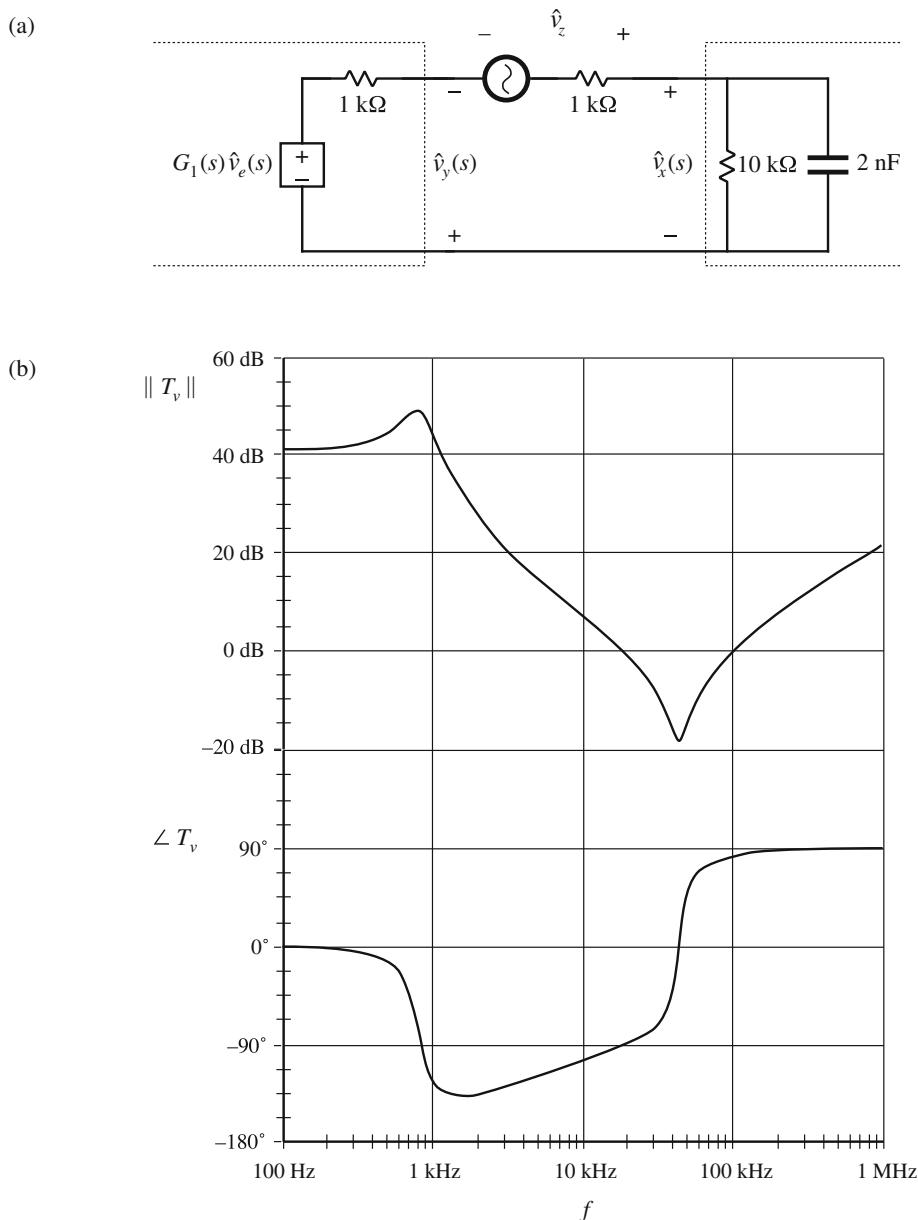


Fig. 9.60 Experimental measurement of loop gain, Problem 9.10: (a) measurement via voltage injection, (b) measured data

9.10 The loop gain of a certain feedback system is measured, using voltage injection at a point in the forward path of the loop as illustrated in Fig. 9.60a. The data in Fig. 9.60b is obtained. What is $T(s)$? Specify $T(s)$ in factored pole-zero form, and give numerical values for all important features. Over what range of frequencies does the measurement give valid results?

Part III

Magnetics



Basic Magnetics Theory

Magnetics are an integral part of every switching converter. Often, the design of the magnetic devices cannot be isolated from the converter design. The power electronics engineer must not only model and design the converter, but must model and design the magnetics as well. Modeling and designing of magnetics for switching converters is the topic of Part III of this book.

In this chapter, basic magnetics theory is reviewed, including magnetic circuits, inductor modeling, and transformer modeling [85–89]. Loss mechanisms in magnetic devices are described. Winding eddy currents and the proximity effect, a significant loss mechanism in high-current high-frequency windings, are explained in detail [90–95]. Inductor design is introduced in Chap. 11, and transformer design is covered in Chap. 12.

10.1 Review of Basic Magnetics

10.1.1 Basic Relationships

The basic magnetic quantities are illustrated in Fig. 10.1. Also illustrated are the analogous, and perhaps more familiar, electrical quantities. The *magnetomotive force* \mathcal{F} , or scalar potential, between two points x_1 and x_2 is given by the integral of the magnetic field \mathbf{H} along a path connecting the points:

$$\mathcal{F} = \int_{x_1}^{x_2} \mathbf{H} \cdot d\ell \quad (10.1)$$

where $d\ell$ is a vector length element pointing in the direction of the path. The dot product yields the component of \mathbf{H} in the direction of the path. If the magnetic field is of uniform strength H passing through an element of length ℓ as illustrated, then Eq. (10.1) reduces to

$$\mathcal{F} = H\ell \quad (10.2)$$

This is analogous to the electric field of uniform strength E , which induces a voltage $V = E\ell$ between two points separated by distance ℓ .

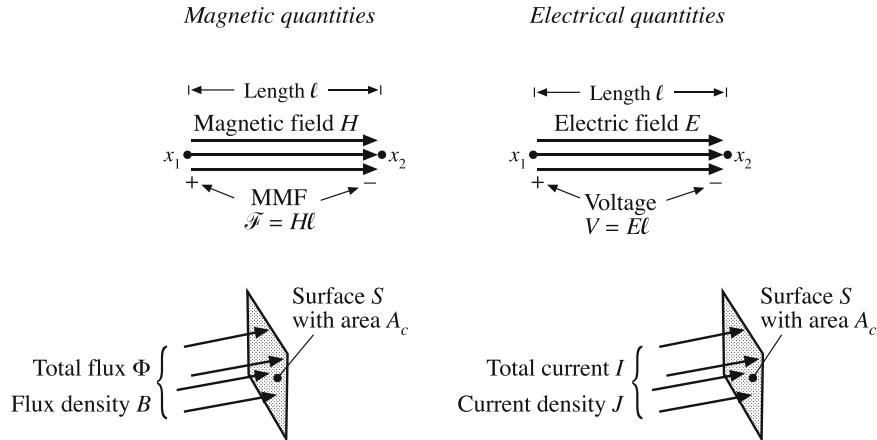


Fig. 10.1 Comparison of magnetic field H , MMF \mathcal{F} , flux Φ , and flux density B , with the analogous electrical quantities E , V , I , and J

Figure 10.1 also illustrates a total magnetic flux Φ passing through a surface S having area A_c . The total flux Φ is equal to the integral of the normal component of the flux density B over the surface

$$\Phi = \int_{\text{surface } S} \mathbf{B} \cdot d\mathbf{A} \quad (10.3)$$

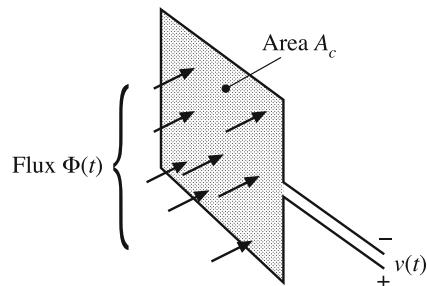
where $d\mathbf{A}$ is a vector area element having direction normal to the surface. For a uniform flux density of magnitude B as illustrated, the integral reduces to

$$\Phi = BA_c \quad (10.4)$$

Flux density \mathbf{B} is analogous to the electrical current density \mathbf{J} , and flux Φ is analogous to the electric current I . If a uniform current density of magnitude J passes through a surface of area A_c , then the total current is $I = JA_c$.

Faraday's law relates the voltage induced in a winding to the total flux passing through the interior of the winding. Figure 10.2 illustrates flux $\Phi(t)$ passing through the interior of a loop of

Fig. 10.2 The voltage $v(t)$ induced in a loop of wire is related by Faraday's law to the derivative of the total flux $\Phi(t)$ passing through the interior of the loop



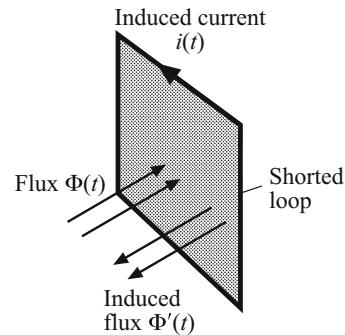


Fig. 10.3 Illustration of Lenz's law in a shorted loop of wire. The flux $\Phi(t)$ induces current $i(t)$, which in turn generates flux $\Phi'(t)$ that tends to oppose changes in $\Phi(t)$

wire. The loop encloses cross-sectional area A_c . According to Faraday's law, the flux induces a voltage $v(t)$ in the wire, given by

$$v(t) = \frac{d\Phi(t)}{dt} \quad (10.5)$$

where the polarities of $v(t)$ and $\Phi(t)$ are defined according to the right-hand rule, as in Fig. 10.2. For a uniform flux distribution, we can express $v(t)$ in terms of the flux density $B(t)$ by substitution of Eq. (10.4):

$$v(t) = A_c \frac{dB(t)}{dt} \quad (10.6)$$

Thus, the voltage induced in a winding is related to the flux Φ and flux density B passing through the interior of the winding.

Lenz's law states that the voltage $v(t)$ induced by the changing flux $\Phi(t)$ in Fig. 10.2 is of the polarity that tends to drive a current through the loop to counteract the flux change. For example, consider the shorted loop of Fig. 10.3. The changing flux $\Phi(t)$ passing through the interior of the loop induces a voltage $v(t)$ around the loop. This voltage, divided by the impedance of the loop conductor, leads to a current $i(t)$ as illustrated. The current $i(t)$ induces a flux $\Phi'(t)$, which tends to oppose the changes in $\Phi(t)$. Lenz's law is invoked later in this chapter, to provide a qualitative understanding of eddy current phenomena.

Ampere's law relates the current in a winding to the magnetomotive force \mathcal{F} and magnetic field \mathbf{H} . The net MMF around a closed path of length ℓ_m is equal to the total current passing through the interior of the path. For example, Fig. 10.4 illustrates a magnetic core, in which a wire carrying current $i(t)$ passes through the window in the center of the core. Let us consider the closed path illustrated, which follows the magnetic field lines around the interior of the core. Ampere's law states that

$$\oint_{closed\ path} \mathbf{H} \cdot d\ell = \text{total current passing through interior of path} \quad (10.7)$$

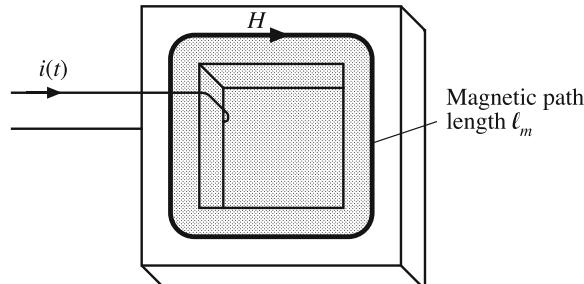


Fig. 10.4 The net MMF around a closed path is related by Ampere's law to the total current passing through the interior of the path

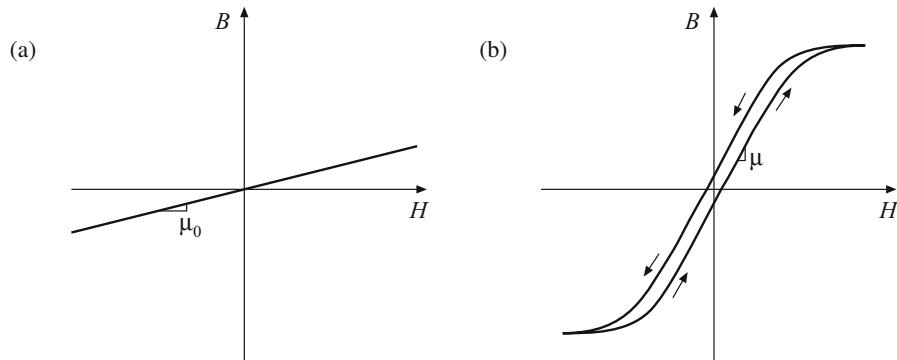


Fig. 10.5 B - H characteristics: (a) of free space or air, (b) of a typical magnetic core material

The total current passing through the interior of the path is equal to the total current passing through the window in the center of the core, or $i(t)$. If the magnetic field is uniform and of magnitude $H(t)$, then the integral is $H(t)\ell_m$. So for the example of Fig. 10.4, Eq. (10.7) reduces to

$$\mathcal{F}(t) = H(t)\ell_m = i(t) \quad (10.8)$$

Thus, the magnetic field strength $H(t)$ is related to the winding current $i(t)$. We can view winding currents as sources of MMF. Equation (10.8) states that the MMF around the core, $\mathcal{F}(t) = H(t)\ell_m$, is equal to the winding current MMF $i(t)$. The total MMF around the closed loop, accounting for both MMFs, is zero.

The relationship between \mathbf{B} and \mathbf{H} , or equivalently between Φ and \mathcal{F} , is determined by the core material characteristics. Figure 10.5a illustrates the characteristics of free space, or air:

$$\mathbf{B} = \mu_0 \mathbf{H} \quad (10.9)$$

The quantity μ_0 is the permeability of free space, and is equal to $4\pi \cdot 10^{-7}$ Henries per meter in MKS units. Figure 10.5b illustrates the B - H characteristic of a typical iron alloy under high-level sinusoidal steady-state excitation. The characteristic is highly nonlinear, and exhibits both *hysteresis* and *saturation*. The exact shape of the characteristic is dependent on the excitation, and is difficult to predict for arbitrary waveforms.

For purposes of analysis, the core material characteristic of Fig. 10.5b is usually modeled by the linear or piecewise-linear characteristics of Fig. 10.6. In Fig. 10.6a, hysteresis and saturation are ignored. The B - H characteristic is then given by

$$\begin{aligned} \mathbf{B} &= \mu \mathbf{H} \\ \mu &= \mu_r \mu_0 \end{aligned} \quad (10.10)$$

The core material permeability μ can be expressed as the product of the relative permeability μ_r and of μ_0 . Typical values of μ_r lie in the range 10^3 to 10^5 .

The piecewise-linear model of Fig. 10.6b accounts for saturation but not hysteresis. The core material saturates when the magnitude of the flux density B exceeds the saturation flux density B_{sat} . For $|B| < B_{sat}$, the characteristic follows Eq. (10.10). When $|B| > B_{sat}$, the model predicts that the core reverts to free space, with a characteristic having a much smaller

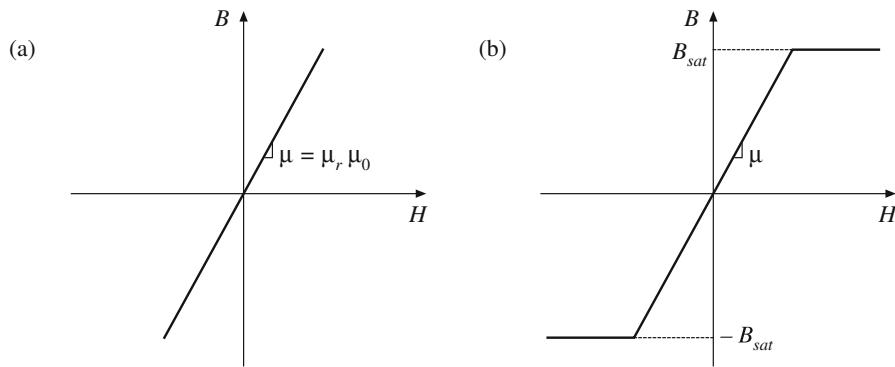


Fig. 10.6 Approximation of the B - H characteristics of a magnetic core material: (a) by neglecting both hysteresis and saturation, (b) by neglecting hysteresis

slope approximately equal to μ_0 . Square-loop materials exhibit this type of abrupt-saturation characteristic, and additionally have a very large relative permeability μ_r . Soft materials exhibit a less abrupt saturation characteristic, in which μ gradually decreases as H is increased. Typical values of B_{sat} are 1 to 2 Tesla for iron laminations and silicon steel, 0.5 to 1 Tesla for powdered iron and molypermalloy materials, and 0.25 to 0.5 Tesla for ferrite materials.

Unit systems for magnetic quantities are summarized in Table 10.1. The MKS system is used throughout this book. The unratinalized CGS system also continues to find some use. Conversions between these systems are listed.

Table 10.1 Units for magnetic quantities

Quantity	MKS	Unratinalized CGS	Conversions
Core material equation	$B = \mu_0 \mu_r H$	$B = \mu_r H$	
B	Tesla	Gauss	$1 \text{ T} = 10^4 \text{ G}$
H	Ampere/meter	Oersted	$1 \text{ A/m} = 4\pi \cdot 10^{-3} \text{ Oe}$
Φ	Weber	Maxwell	$1 \text{ Wb} = 10^8 \text{ Mx}$ $1 \text{ T} = 1 \text{ Wb/m}^2$

Figure 10.7 summarizes the relationships between the basic electrical and magnetic quantities of a magnetic device. The winding voltage $v(t)$ is related to the core flux and flux density via Faraday's law. The winding current $i(t)$ is related to the magnetic field strength via Ampere's law. The core material characteristics relate B and H .

We can now determine the electrical terminal characteristics of the simple inductor of Fig. 10.8a. A winding of n turns is placed on a core having permeability μ . Faraday's law states that the flux $\Phi(t)$ inside the core induces a voltage $v_{turn}(t)$ in each turn of the winding, given by

$$v_{turn}(t) = \frac{d\Phi(t)}{dt} \quad (10.11)$$

Since the same flux $\Phi(t)$ passes through each turn of the winding, the total winding voltage is

Fig. 10.7 Summary of the steps in determination of the terminal electrical $i-v$ characteristics of a magnetic element

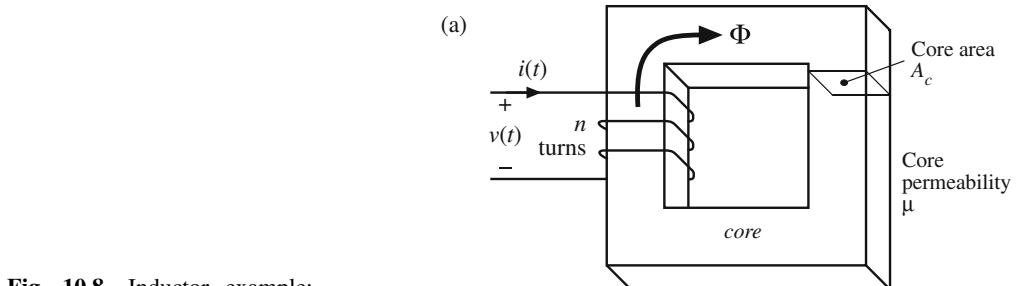
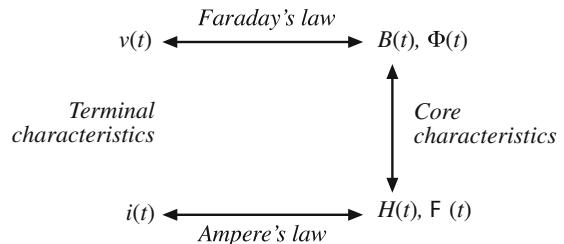
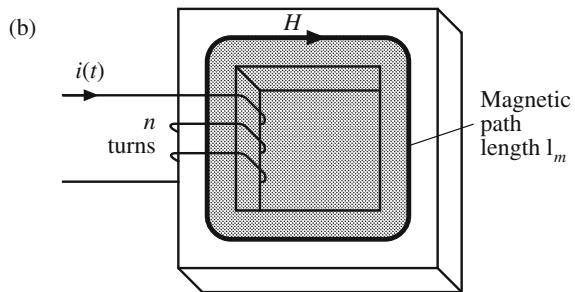


Fig. 10.8 Inductor example:
(a) inductor geometry, (b) application of Ampere's law



$$v(t) = nv_{turn}(t) = n \frac{d\Phi(t)}{dt} \quad (10.12)$$

Equation (10.12) can be expressed in terms of the average flux density $B(t)$ by substitution of Eq. (10.4):

$$v(t) = nA_c \frac{dB(t)}{dt} \quad (10.13)$$

where the average flux density $B(t)$ is $\Phi(t)/A_c$.

The use of Ampere's law is illustrated in Fig. 10.8b. A closed path is chosen which follows an average magnetic field line around the interior of the core. The length of this path is called the *mean magnetic path length* ℓ_m . If the magnetic field strength $H(t)$ is uniform, then Ampere's law states that $H\ell_m$ is equal to the total current passing through the interior of the path, that is, the net current passing through the window in the center of the core. Since there are n turns of wire passing through the window, each carrying current $i(t)$, the net current passing through the window is $ni(t)$. Hence, Ampere's law states that

$$H(t)\ell_m = ni(t) \quad (10.14)$$

Let us model the core material characteristics by neglecting hysteresis but accounting for saturation, as follows:

$$B = \begin{cases} B_{sat} & \text{for } H \geq B_{sat}/\mu \\ \mu H & \text{for } |H| < B_{sat}/\mu \\ -B_{sat} & \text{for } H \leq -B_{sat}/\mu \end{cases} \quad (10.15)$$

The B - H characteristic saturated slope μ_0 is much smaller than μ , and is ignored here. A characteristic similar to Fig. 10.6b is obtained. The current magnitude I_{sat} at the onset of saturation can be found by substitution of $H = B_{sat}/\mu$ into Eq. (10.14). The result is

$$I_{sat} = \frac{B_{sat}\ell_m}{\mu n} \quad (10.16)$$

We can now eliminate B and H from Eqs. (10.13) to (10.15), and solve for the electrical terminal characteristics. For $|I| < I_{sat}$, $B = \mu H$. Equation (10.13) then becomes

$$v(t) = \mu n A_c \frac{dH(t)}{dt} \quad (10.17)$$

Substitution of Eq. (10.14) into Eq. (10.17) to eliminate $H(t)$ then leads to

$$v(t) = \frac{\mu n^2 A_c}{\ell_m} \frac{di(t)}{dt} \quad (10.18)$$

which is of the form

$$v(t) = L \frac{di(t)}{dt} \quad (10.19)$$

with

$$L = \frac{\mu n^2 A_c}{\ell_m} \quad (10.20)$$

So the device behaves as an inductor for $|I| < I_{sat}$. When $|I| > I_{sat}$, then the flux density $B(t) = B_{sat}$ is constant. Faraday's law states that the terminal voltage is then

$$v(t) = n A_c \frac{dB_{sat}}{dt} = 0 \quad (10.21)$$

When the core saturates, the magnetic device behavior approaches a short circuit. The device behaves as an inductor only when the winding current magnitude is less than I_{sat} . Practical inductors exhibit some small residual inductance due to their nonzero saturated permeabilities; nonetheless, in saturation the inductor impedance is greatly reduced, and large inductor currents may result.

10.1.2 Magnetic Circuits

Figure 10.9a illustrates uniform flux and magnetic field inside an element having permeability μ , length ℓ , and cross-sectional area A_c . The MMF between the two ends of the element is

$$\mathcal{F} = H\ell \quad (10.22)$$

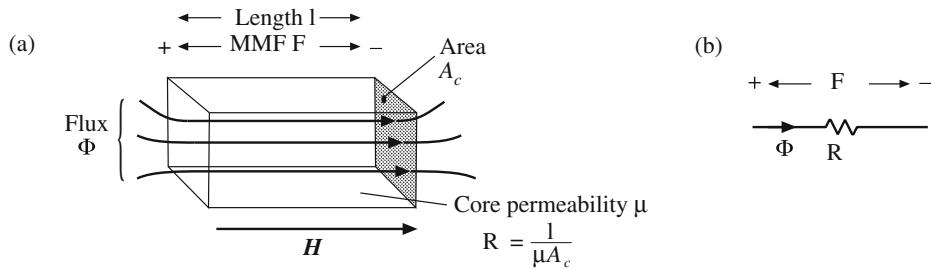


Fig. 10.9 An element containing magnetic flux (a), and its equivalent magnetic circuit (b)

Since \$H = B/\mu\$ and \$B = \Phi/A_c\$, we can express \$\mathcal{F}\$ as

$$\mathcal{F} = \frac{\ell}{\mu A_c} \Phi \quad (10.23)$$

This equation is of the form

$$\mathcal{F} = \Phi \mathcal{R} \quad (10.24)$$

with

$$\mathcal{R} = \frac{\ell}{\mu A_c} \quad (10.25)$$

Equation (10.24) resembles Ohm's law. This equation states that the magnetic flux through an element is proportional to the MMF across the element. The constant of proportionality, or the reluctance \$\mathcal{R}\$, is analogous to the resistance \$R\$ of an electrical conductor. Indeed, we can construct a lumped-element magnetic circuit model that corresponds to Eq. (10.24), as in Fig. 10.9b. In this magnetic circuit model, voltage and current are replaced by MMF and flux, while the element characteristic, Eq. (10.24), is represented by the analog of a resistor, having reluctance \$\mathcal{R}\$.

Complicated magnetic structures, composed of multiple windings and multiple heterogeneous elements such as cores and air gaps, can be represented using equivalent magnetic circuits. These magnetic circuits can then be solved using conventional circuit analysis, to determine the various fluxes, MMFs, and terminal voltages and currents. Kirchhoff's laws apply to magnetic circuits, and follow directly from Maxwell's equations. The analog of Kirchhoff's current law holds because the divergence of \$\mathbf{B}\$ is zero, and hence magnetic flux lines are continuous and cannot end. Therefore, any flux line that enters a node must leave the node. As illustrated in Fig. 10.10, the total flux entering a node must be zero. The analog of Kirchhoff's voltage law follows from Ampere's law, Eq. (10.7). The left-hand-side integral in Eq. (10.7) is the sum of the MMFs across the reluctances around the closed path. The right-hand-side of Eq. (10.7) states that currents in windings are sources of MMF. An \$n\$-turn winding carrying current \$i(t)\$ can be modeled as an MMF source, analogous to a voltage source, of value \$ni(t)\$. When these MMF sources are included, the total MMF around a closed path is zero.

Consider the inductor with air gap of Fig. 10.11a. A closed path following the magnetic field lines is illustrated. This path passes through the core, of permeability \$\mu\$ and length \$\ell_c\$, and across the air gap, of permeability \$\mu_0\$ and length \$\ell_g\$. The cross-sectional areas of the core and air gap are approximately equal. Application of Ampere's law for this path leads to

$$\mathcal{F}_c + \mathcal{F}_g = ni \quad (10.26)$$

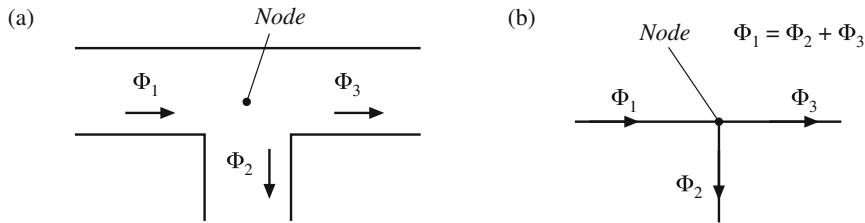


Fig. 10.10 Kirchhoff's current law, applied to magnetic circuits: the net flux entering a node must be zero. (a) physical element, in which three legs of a core meet at a node; (b) magnetic circuit model

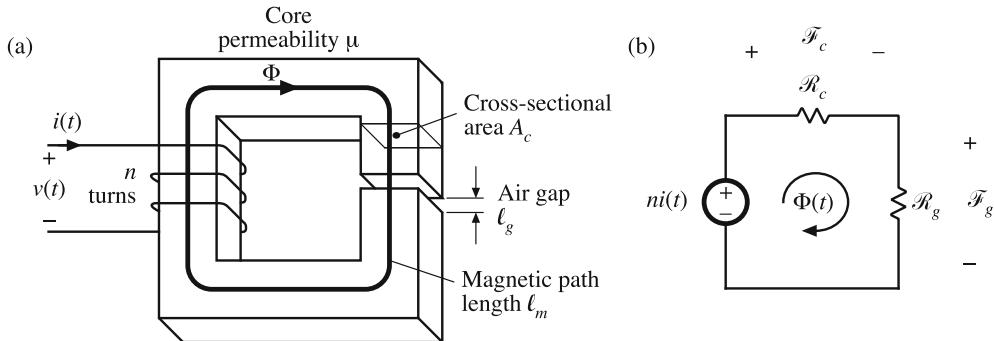


Fig. 10.11 Inductor with air gap example: (a) physical geometry; (b) magnetic circuit model

where \mathcal{F}_c and \mathcal{F}_g are the MMFs across the core and air gap, respectively. The core and air gap characteristics can be modeled by reluctances as in Fig. 10.9 and Eq. (10.25); the core reluctance \mathcal{R}_c and air gap reluctance \mathcal{R}_g are given by

$$\begin{aligned}\mathcal{R}_c &= \frac{\ell_c}{\mu A_c} \\ \mathcal{R}_g &= \frac{\ell_g}{\mu_0 A_c}\end{aligned}\quad (10.27)$$

A magnetic circuit corresponding to Eqs. (10.26) and (10.27) is given in Fig. 10.11b. The winding is a source of MMF, of value ni . The core and air gap reluctances are effectively in series. The solution of the magnetic circuit is

$$ni = \Phi(\mathcal{R}_c + \mathcal{R}_g) \quad (10.28)$$

The flux $\Phi(t)$ passes through the winding, and so we can use Faraday's law to write

$$v(t) = n \frac{d\Phi(t)}{dt} \quad (10.29)$$

Use of Eq. (10.28) to eliminate $\Phi(t)$ yields

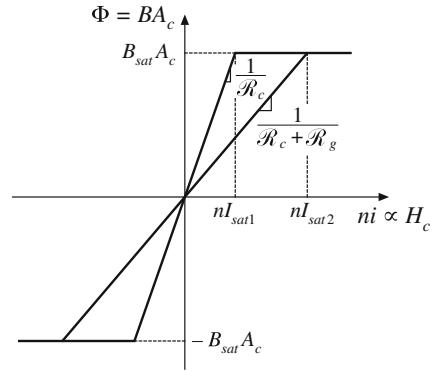


Fig. 10.12 Effect of air gap on the magnetic circuit Φ vs. ni characteristics. The air gap increases the current I_{sat} at the onset of core saturation

$$v(t) = \frac{n^2}{\mathcal{R}_c + \mathcal{R}_g} \frac{di(t)}{dt} \quad (10.30)$$

Therefore, the inductance L is

$$L = \frac{n^2}{\mathcal{R}_c + \mathcal{R}_g} \quad (10.31)$$

The air gap increases the total reluctance of the magnetic circuit, and decreases the inductance.

Air gaps are employed in practical inductors for two reasons. With no air gap ($\mathcal{R}_g = 0$), the inductance is directly proportional to the core permeability μ . This quantity is dependent on temperature and operating point, and is difficult to control. Hence, it may be difficult to construct an inductor having a well-controlled value of L . Addition of an air gap having a reluctance \mathcal{R}_g greater than \mathcal{R}_c causes the value of L in Eq. (10.31) to be insensitive to variations in μ .

Addition of an air gap also allows the inductor to operate at higher values of winding current $i(t)$ without saturation. The total flux Φ is plotted vs. the winding MMF ni in Fig. 10.12. Since Φ is proportional to B , and when the core is not saturated ni is proportional to the magnetic field strength H in the core, Fig. 10.12 has the same shape as the core B - H characteristic. When the core is not saturated, Φ is related to ni according to the linear relationship of Eq. (10.28). When the core saturates, Φ is equal to

$$\Phi_{sat} = B_{sat}A_c \quad (10.32)$$

The winding current I_{sat} at the onset of saturation is found by substitution of Eq. (10.32) into (10.28):

$$I_{sat} = \frac{B_{sat}A_c}{n}(\mathcal{R}_c + \mathcal{R}_g) \quad (10.33)$$

The Φ - ni characteristics are plotted in Fig. 10.12 for two cases: (a) air gap present, and (b) no air gap ($\mathcal{R}_g = 0$). It can be seen that I_{sat} is increased by addition of an air gap. Thus, the air gap allows increase of the saturation current, at the expense of decreased inductance.

10.2 Transformer Modeling

Consider next the two-winding transformer of Fig. 10.13. The core has cross-sectional area A_c , mean magnetic path length ℓ_m , and permeability μ . An equivalent magnetic circuit is given in Fig. 10.14. The core reluctance is

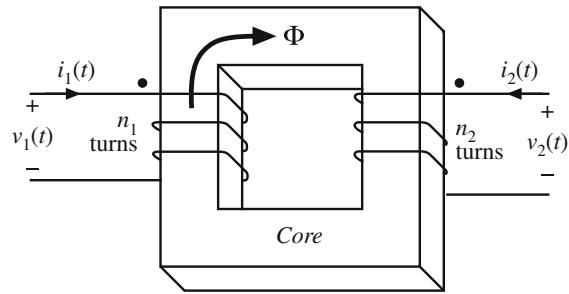


Fig. 10.13 A two-winding transformer

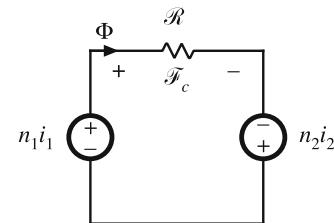


Fig. 10.14 Magnetic circuit that models the two-winding transformer of Fig. 10.13

$$\mathcal{R} = \frac{\ell_m}{\mu A_c} \quad (10.34)$$

Since there are two windings in this example, it is necessary to determine the relative polarities of the MMF generators. Ampere's law states that

$$\mathcal{F}_c = n_1 i_1 + n_2 i_2 \quad (10.35)$$

The MMF generators are additive, because the currents i_1 and i_2 pass in the same direction through the core window. Solution of Fig. 10.14 yields

$$\Phi \mathcal{R} = n_1 i_1 + n_2 i_2 \quad (10.36)$$

This expression could also be obtained by substitution of $\mathcal{F}_c = \Phi \mathcal{R}$ into Eq. (10.35).

10.2.1 The Ideal Transformer

In the ideal transformer, the core reluctance \mathcal{R} approaches zero. This causes the core MMF $\mathcal{F}_c = \Phi \mathcal{R}$ also to approach zero. Equation (10.35) then becomes

$$0 = n_1 i_1 + n_2 i_2 \quad (10.37)$$

Also, by Faraday's law, we have

$$v_1 = n_1 \frac{d\Phi}{dt} \quad (10.38)$$

$$v_2 = n_2 \frac{d\Phi}{dt}$$

Note that Φ is the same in both equations above: the same total flux links both windings. Elimination of Φ leads to

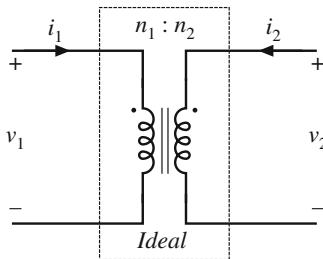


Fig. 10.15 Ideal transformer symbol

$$\frac{d\Phi}{dt} = \frac{v_1}{n_1} = \frac{v_2}{n_2} \quad (10.39)$$

Equations (10.37) and (10.39) are the equations of the ideal transformer:

$$\frac{v_1}{n_1} = \frac{v_2}{n_2} \quad \text{and} \quad n_1 i_1 + n_2 i_2 = 0 \quad (10.40)$$

The ideal transformer symbol of Fig. 10.15 is defined by Eq. (10.40).

10.2.2 The Magnetizing Inductance

For the actual case in which the core reluctance \mathcal{R} is nonzero, we have

$$\Phi \mathcal{R} = n_1 i_1 + n_2 i_2 \quad \text{with} \quad v_1 = n_1 \frac{d\Phi}{dt} \quad (10.41)$$

Elimination of Φ yields

$$v_1 = \frac{n_1^2}{\mathcal{R}} \frac{d}{dt} \left[i_1 + \frac{n_2}{n_1} i_2 \right] \quad (10.42)$$

This equation is of the form

$$v_1 = L_M \frac{di_M}{dt} \quad (10.43)$$

where

$$\begin{aligned} L_M &= \frac{n_1^2}{\mathcal{R}} \\ i_M &= i_1 + \frac{n_2}{n_1} i_2 \end{aligned} \quad (10.44)$$

are the *magnetizing inductance* and *magnetizing current*, referred to the primary winding. An equivalent circuit is illustrated in Fig. 10.16.

Figure 10.16 coincides with the transformer model introduced in Chap. 6. The magnetizing inductance models the magnetization of the core material. It is a real, physical inductor, which exhibits saturation and hysteresis. All physical transformers must contain a magnetizing inductance. For example, suppose that we disconnect the secondary winding. We are then left with a single winding on a magnetic core—an inductor. Indeed, the equivalent circuit of Fig. 10.16

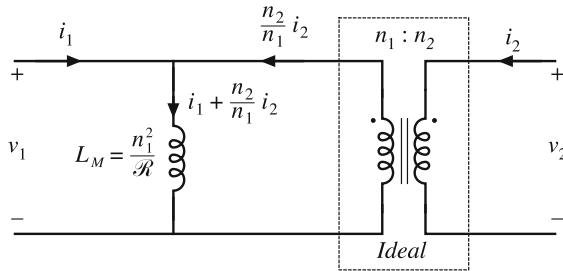


Fig. 10.16 Transformer model including magnetizing inductance

predicts this behavior, via the magnetizing inductance. The magnetizing current causes the ratio of the winding currents to differ from the turns ratio.

The transformer saturates when the core flux density $B(t)$ exceeds the saturation flux density B_{sat} . When the transformer saturates, the magnetizing current $i_M(t)$ becomes large, the impedance of the magnetizing inductance becomes small, and the transformer windings become short circuits. It should be noted that large winding currents $i_1(t)$ and $i_2(t)$ do not necessarily cause saturation: if these currents obey Eq. (10.37), then the magnetizing current is zero and there is no net magnetization of the core. Rather, saturation of a transformer is a function of the applied volt-seconds. The magnetizing current is given by

$$i_M(t) = \frac{1}{L_M} \int v_1(t) dt \quad (10.45)$$

Alternatively, Eq. (10.45) can be expressed in terms of the core flux density $B(t)$ as

$$B(t) = \frac{1}{n_1 A_c} \int v_1(t) dt \quad (10.46)$$

The flux density and magnetizing current will become large enough to saturate the core when the applied volt-seconds λ_1 is too large, where λ_1 is defined for a periodic ac voltage waveform as

$$\lambda_1 = \int_1^{t_2} v_1(t) dt \quad (10.47)$$

The limits are chosen such that the integral is taken over the positive portion of the applied periodic voltage waveform.

To fix a saturating transformer, the flux density should be decreased by increasing the number of turns, or by increasing the core cross-sectional area A_c . Adding an air gap has no effect on saturation of conventional transformers, since it does not modify Eq. (10.46). An air gap simply makes the transformer less ideal, by decreasing L_M and increasing $i_M(t)$ without changing $B(t)$. Saturation mechanisms in transformers differ from those of inductors, because transformer saturation is determined by the applied winding voltage waveforms, rather than the applied winding currents.

10.2.3 Leakage Inductances

In practice, there is some flux which links one winding but not the other, by “leaking” into the air or by some other mechanism. As illustrated in Fig. 10.17, this flux leads to *leakage inductance*.

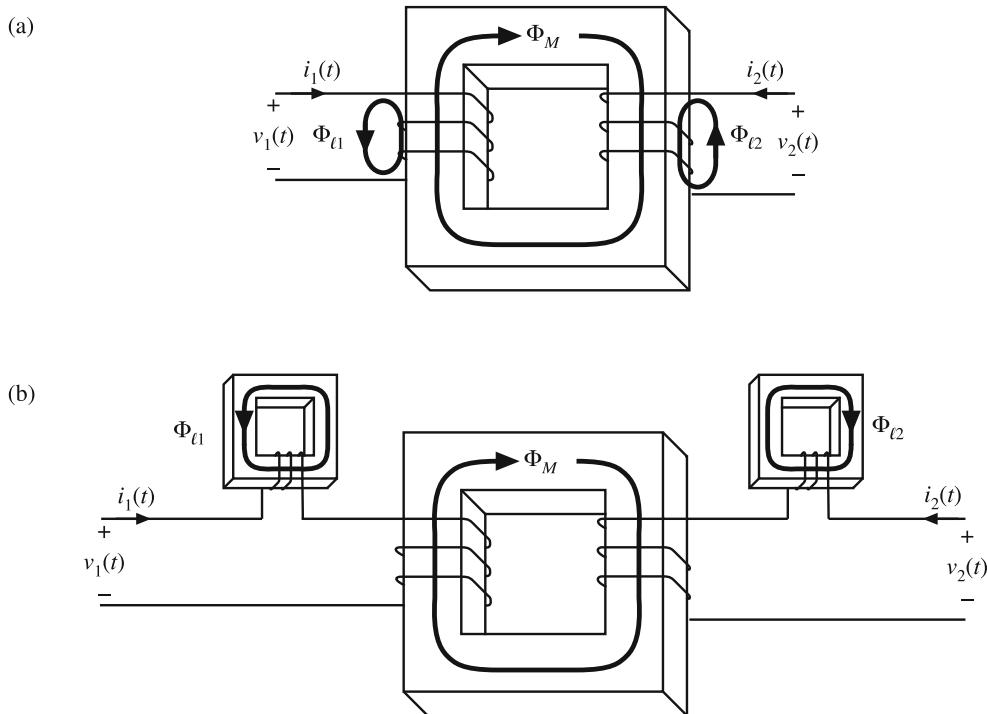


Fig. 10.17 Leakage flux in a two-winding transformer: (a) transformer geometry, (b) an equivalent system

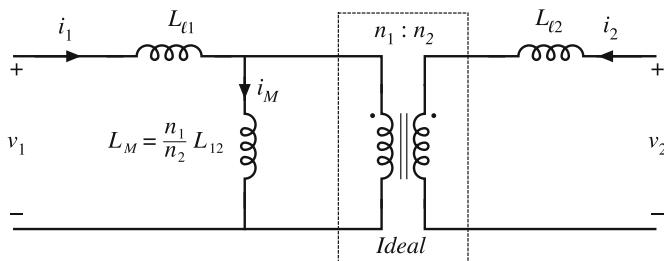


Fig. 10.18 Two-winding transformer equivalent circuit, including magnetizing inductance referred to primary, and primary and secondary leakage inductances

tance, i.e., additional effective inductances that are in series with the windings. A topologically equivalent structure is illustrated in Fig. 10.17b, in which the leakage fluxes $\Phi_{\ell 1}$ and $\Phi_{\ell 2}$ are shown explicitly as separate inductors.

Figure 10.18 illustrates a transformer electrical equivalent circuit model, including series inductors $L_{\ell 1}$ and $L_{\ell 2}$ which model the leakage inductances. These leakage inductances cause the terminal voltage ratio $v_2(t)/v_1(t)$ to differ from the ideal turns ratio n_2/n_1 . In general, the terminal equations of a two-winding transformer can be written

$$\begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{22} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1(t) \\ i_2(t) \end{bmatrix} \quad (10.48)$$

The quantity L_{12} is called the *mutual inductance*, and is given by

$$L_{12} = \frac{n_1 n_2}{\mathcal{R}} = \frac{n_2}{n_1} L_M \quad (10.49)$$

The quantities L_{11} and L_{22} are called the primary and secondary *self-inductances*, given by

$$\begin{aligned} L_{11} &= L_{\ell 1} + \frac{n_1}{n_2} L_{12} \\ L_{22} &= L_{\ell 2} + \frac{n_2}{n_1} L_{12} \end{aligned} \quad (10.50)$$

Note that Eq. (10.48) does not explicitly identify the physical turns ratio n_2/n_1 . Rather, Eq. (10.48) expresses the transformer behavior as a function of electrical quantities alone. Equation (10.48) can be used, however, to define the *effective turns ratio*

$$n_e = \sqrt{\frac{L_{22}}{L_{11}}} \quad (10.51)$$

and the *coupling coefficient*

$$k = \frac{L_{12}}{\sqrt{L_{11} L_{22}}} \quad (10.52)$$

The coupling coefficient k lies in the range $0 \leq k \leq 1$, and is a measure of the degree of magnetic coupling between the primary and secondary windings. In a transformer with perfect coupling, the leakage inductances $L_{\ell 1}$ and $L_{\ell 2}$ are zero. The coupling coefficient k is then equal to 1. Construction of low-voltage transformers having coupling coefficients in excess of 0.99 is quite feasible. When the coupling coefficient is close to 1, then the effective turns ratio n_e is approximately equal to the physical turns ratio n_2/n_1 .

10.3 Loss Mechanisms in Magnetic Devices

10.3.1 Core Loss

Energy is required to effect a change in the magnetization of a core material. Not all of this energy is recoverable in electrical form; a fraction is lost as heat. This power loss can be observed electrically as hysteresis of the B - H loop.

Consider an n -turn inductor excited by periodic waveforms $v(t)$ and $i(t)$ having frequency f . The net energy that flows into the inductor over one cycle is

$$W = \int_{\text{one cycle}} v(t)i(t)dt \quad (10.53)$$

We can relate this expression to the core B - H characteristic: substitute $B(t)$ for $v(t)$ using Faraday's law, Eq. (10.13), and substitute $H(t)$ for $i(t)$ using Ampere's law, i.e., Eq. (10.14):

$$\begin{aligned} W &= \int_{\text{one cycle}} \left(nA_c \frac{dB(t)}{dt} \right) \left(\frac{H(t)\ell_m}{n} \right) dt \\ &= (A_c \ell_m) \int_{\text{one cycle}} H dB \end{aligned} \quad (10.54)$$

The term $A_c \ell_m$ is the volume of the core, while the integral is the area of the B - H loop:

$$(\text{energy lost per cycle}) = (\text{core volume})(\text{area of } B - H \text{ loop}) \quad (10.55)$$

The *hysteresis power loss* P_H is equal to the energy lost per cycle, multiplied by the excitation frequency f :

$$P_H = (f)(A_c \ell_m) \int_{\text{one cycle}} H dB \quad (10.56)$$

To the extent that the size of the hysteresis loop is independent of frequency, hysteresis loss increases directly with operating frequency.

Magnetic core materials are iron alloys that, unfortunately, are also good electrical conductors. As a result, ac magnetic fields can cause electrical *eddy currents* to flow within the core material itself. An example is illustrated in Fig. 10.19. The ac flux $\Phi(t)$ passes through the core. This induces eddy currents $i(t)$ which, according to Lenz's law, flow in paths that oppose the time-varying flux $\Phi(t)$. These eddy currents cause $i^2 R$ losses in the resistance of the core material. The eddy current losses are especially significant in high-frequency applications.

According to Faraday's law, the ac flux $\Phi(t)$ induces voltage in the core, which drives the current around the paths illustrated in Fig. 10.19. Since the induced voltage is proportional to the derivative of the flux, the voltage magnitude increases directly with the excitation frequency f . If the impedance of the core material is purely resistive and independent of frequency, then the magnitude of the induced eddy currents also increases directly with f . This implies that the $i^2 R$ eddy current losses should increase as f^2 . In power ferrite materials, the core material impedance magnitude actually decreases with increasing f . Over the useful frequency range, the eddy current losses typically increase faster than f^2 .

There is a basic tradeoff between saturation flux density and core loss. Use of a high operating flux density leads to reduced size, weight, and cost. Silicon steel and similar materials exhibit saturation flux densities of 1.5 to 2 T. Unfortunately, these core materials exhibit high core loss. In particular, the low resistivity of these materials leads to high eddy current loss. Hence, these materials are suitable for filter inductor and low-frequency transformer applications. The core material is produced in laminations or thin ribbons, to reduce the eddy current magnitude. Other ferrous alloys may contain molybdenum, cobalt, or other elements, and exhibit somewhat lower core loss as well as somewhat lower saturation flux densities.

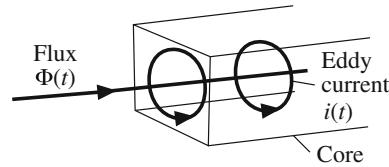


Fig. 10.19 Eddy currents in an iron core

Iron alloys are also employed in powdered cores, containing ferromagnetic particles of sufficiently small diameter such that eddy currents are small. These particles are bound together using an insulating medium. Powdered iron and molybdenum permalloy powder cores exhibit typical saturation flux densities of 0.6 to 0.8 T, with core losses significantly lower than laminated ferrous alloy materials. The insulating medium behaves effectively as a distributed air gap, and hence these cores have relatively low permeability. Powder cores find application as transformers at frequencies of several kHz, and as filter inductors in high frequency (100 kHz) switching converters.

Amorphous alloys exhibit low hysteresis loss. Core conductivity and eddy current losses are somewhat lower than ferrous alloys, but higher than ferrites. Saturation flux densities in the range 0.6 to 1.5 T are obtained.

Ferrite cores are ceramic materials having low saturation flux density, 0.25 to 0.5 T. Their resistivities are much higher than other materials, and hence eddy current losses are much smaller. Manganese-zinc ferrite cores find widespread use as inductors and transformers in converters having switching frequencies of 10 kHz to 1 MHz. Nickel-zinc ferrite materials can be employed at yet higher frequencies.

Figure 10.20 contains typical total core loss data, for a certain ferrite material. Power loss density, in Watts per cubic centimeter of core material, is plotted as a function of sinusoidal excitation frequency f and peak ac flux density ΔB . At a given frequency, the core loss P_{fe} can be approximated by an empirical function of the form

$$P_{fe} = K_{fe}(\Delta B)^\beta A_c \ell_m \quad (10.57)$$

The parameters K_{fe} and β are determined by fitting Eq. (10.57) to the manufacturer's published data. Typical values of β for ferrite materials operating in their intended range of ΔB and f lie in the range 2.6 to 2.8. The constant of proportionality K_{fe} increases rapidly with excitation frequency f . The dependence of K_{fe} on f can also be approximated by empirical formulae that are fitted to the manufacturer's published data; a fourth-order polynomial or a function of the form $K_{fe0}f^\xi$ are sometimes employed for this purpose. Parameters in empirical formulae fitted to data measured under sinusoidal excitation can be used to improve prediction of ferrite core loss with nonsinusoidal waveforms, as described in [96].

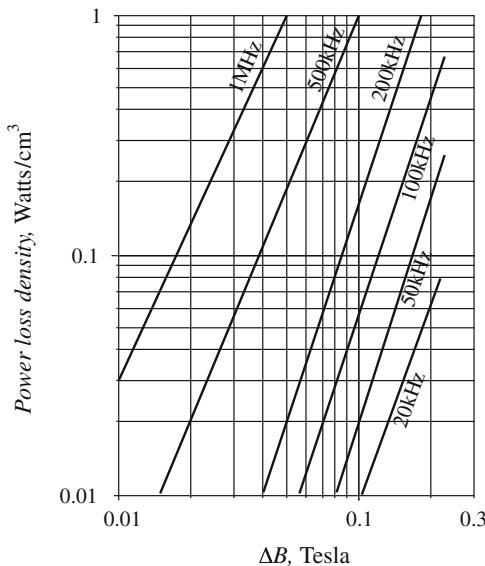


Fig. 10.20 Typical core loss data for a high-frequency power ferrite material. Power loss density is plotted vs. peak ac flux density ΔB , for sinusoidal excitation

10.3.2 Low-Frequency Copper Loss

Significant loss also occurs in the resistance of the copper windings. This is also a major determinant of the size of a magnetic device: if copper loss and winding resistance were irrelevant, then inductor and transformer elements could be made arbitrarily small by use of many small turns of small wire.

Figure 10.21 contains an equivalent circuit of a winding, in which element R models the winding resistance. The copper loss of the winding is

$$P_{cu} = I_{rms}^2 R \quad (10.58)$$

where I_{rms} is the rms value of $i(t)$. The dc resistance of the winding conductor can be expressed as

$$R = \rho \frac{\ell_b}{A_w} \quad (10.59)$$

where A_w is the wire bare cross-sectional area, and ℓ_b is the length of the wire. The resistivity ρ is equal to $1.724 \cdot 10^{-6} \Omega\text{-cm}$ for soft-annealed copper at room temperature. This resistivity increases to $2.3 \cdot 10^{-6} \Omega\text{-cm}$ at 100°C .

If a core has a *mean length per turn* given by MLT , then an n turn winding on this core will have length $\ell_b = nMLT$. The resistance of this winding will be:

$$R = \rho \frac{n(MLT)}{A_w} \quad (10.60)$$

Appendix B contains tables of the mean lengths per turn of standard ferrite core shapes, as well as the areas of standard American wire gauges.

10.4 Eddy Currents in Winding Conductors

Eddy currents also cause power losses in winding conductors. This can lead to copper losses significantly in excess of the value predicted by Eqs. (10.58) and (10.59). The specific conductor eddy current mechanisms are called the *skin effect* and the *proximity effect*. These mechanisms are most pronounced in high-current conductors of multi-layer windings, particularly in high-frequency converters.

10.4.1 Introduction to the Skin and Proximity Effects

Figure 10.22a illustrates a current $i(t)$ flowing through a solitary conductor. This current induces magnetic flux $\Phi(t)$, whose flux lines follow circular paths around the current as shown. According to Lenz's law, the ac flux in the conductor induces eddy currents, which flow in a manner that tends to oppose the ac flux $\Phi(t)$. Figure 10.22b illustrates the paths of the eddy currents. It can be seen that the eddy currents tend to reduce the net current density in the center of the conductor, and increase the net current density near the surface of the conductor.

The current distribution within the conductor can be found by solution of Maxwell's equations. For a sinusoidal current $i(t)$ of frequency f , the result is that the current density is greatest

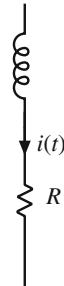


Fig. 10.21 Winding equivalent circuit that models copper loss

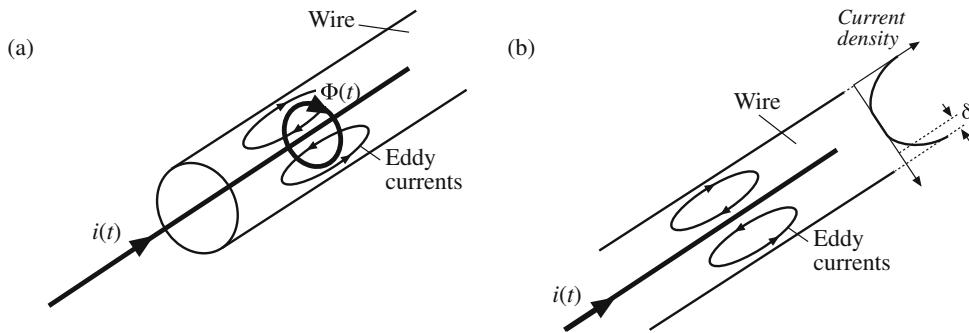


Fig. 10.22 The skin effect: (a) current $i(t)$ induces flux $\Phi(t)$, which in turn induces eddy currents in conductor; (b) the eddy currents tend to oppose the current $i(t)$ in the center of the wire, and increase the current on the surface of the wire

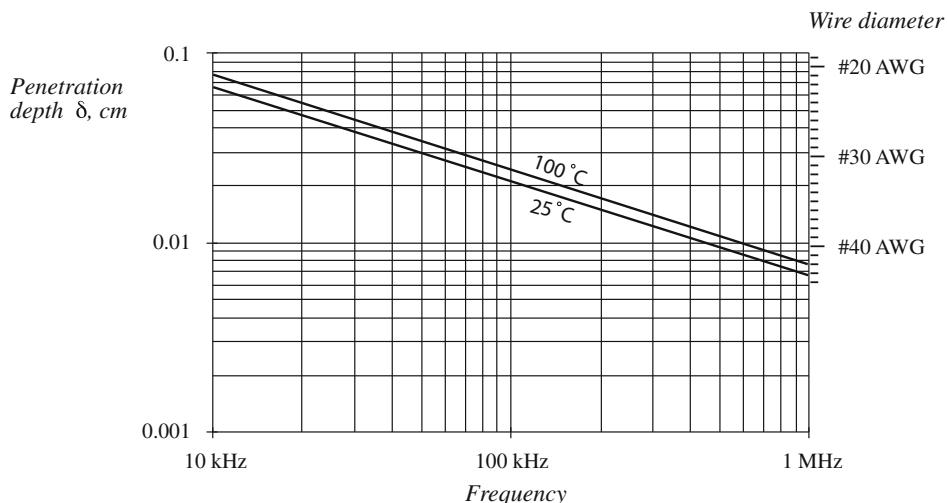


Fig. 10.23 Penetration depth δ , as a function of frequency f , for copper wire

at the surface of the conductor. The current density is an exponentially decaying function of distance into the conductor, with characteristic length δ known as the *penetration depth* or *skin depth*. The penetration depth is given by

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \quad (10.61)$$

For a copper conductor, the permeability μ is equal to μ_0 , and the resistivity ρ is given in Sect. 10.3.2. At 100°C, the penetration depth of a copper conductor is

$$\delta = \frac{7.5}{\sqrt{f}} \text{ cm} \quad (10.62)$$

with f expressed in Hz. The penetration depth of copper conductors is plotted in Fig. 10.23, as a function of frequency f . For comparison, the wire diameters d of standard American Wire

Gauge (AWG) conductors are also listed. It can be seen that $d/\delta = 1$ for AWG #40 at approximately 500 kHz, while $d/\delta = 1$ for AWG #22 at approximately 10 kHz.

The skin effect causes the resistance and copper loss of solitary large-diameter wires to increase at high frequency. High-frequency currents do not penetrate to the center of the conductor. The current crowds at the surface of the wire, the inside of the wire is not utilized, and the effective wire cross-sectional area is reduced. However, the skin effect alone is not sufficient to explain the increased high-frequency copper losses observed in multiple-layer transformer windings.

A conductor that carries a high-frequency current $i(t)$ induces copper loss in an adjacent conductor by a phenomenon known as the *proximity effect*. Figure 10.24 illustrates two copper foil conductors that are placed in close proximity to each other. Conductor 1 carries a high-frequency sinusoidal current $i(t)$, whose penetration depth δ is much smaller than the thickness h of conductors 1 or 2. Conductor 2 is open-circuited, so that it carries a net current of zero. However, it is possible for eddy currents to be induced in conductor 2 by the current $i(t)$ flowing in conductor 1.

The current $i(t)$ flowing in conductor 1 generates a flux $\Phi(t)$ in the space between conductors 1 and 2; this flux attempts to penetrate conductor 2. By Lenz's law, a current is induced on the adjacent (left) side of conductor 2, which tends to oppose the flux $\Phi(t)$. If the conductors are closely spaced, and if $h \gg \delta$, then the induced current will be equal and opposite to the current $i(t)$, as illustrated in Fig. 10.24.

Since conductor 2 is open-circuited, the net current in conductor 2 must be zero. Therefore, a current $+i(t)$ flows on the right-side surface of conductor 2. So the current flowing in conductor 1 induces a current that circulates on the surfaces of conductor 2.

Figure 10.25 illustrates the proximity effect in a simple transformer winding. The primary winding consists of three series-connected turns of copper foil, having thickness $h \gg \delta$, and carrying net current $i(t)$. The copper foil is a strip of copper whose width is the same as the height of the core window; this strip is wound around a leg of the core. Consequently, each turn of this foil comprises one layer of the winding, as illustrated in Fig. 10.25b. The secondary winding is identical; to the extent that the magnetizing current is small, the secondary turns carry net current $-i(t)$. The windings pass through the window of a magnetic core; the magnetic core material encloses the mutual flux of the transformer.

The high-frequency sinusoidal current $i(t)$ flows on the right surface of primary layer 1, adjacent to layer 2. This induces a copper loss in layer 1, which can be calculated as follows. Let R_{dc} be the dc resistance of layer 1, given by Eq. (10.59), and let I be the rms value of $i(t)$. The skin effect causes the copper loss in layer 1 to be equal to the loss in a conductor of thickness δ with uniform current density. This reduction of the conductor thickness from h to δ effectively increases the resistance by the same factor. Hence, layer 1 can be viewed as having an "ac resistance" given by

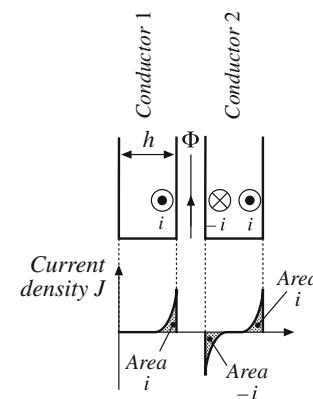


Fig. 10.24 The proximity effect in adjacent copper foil conductors. Conductor 1 carries current $i(t)$. Conductor 2 is open-circuited

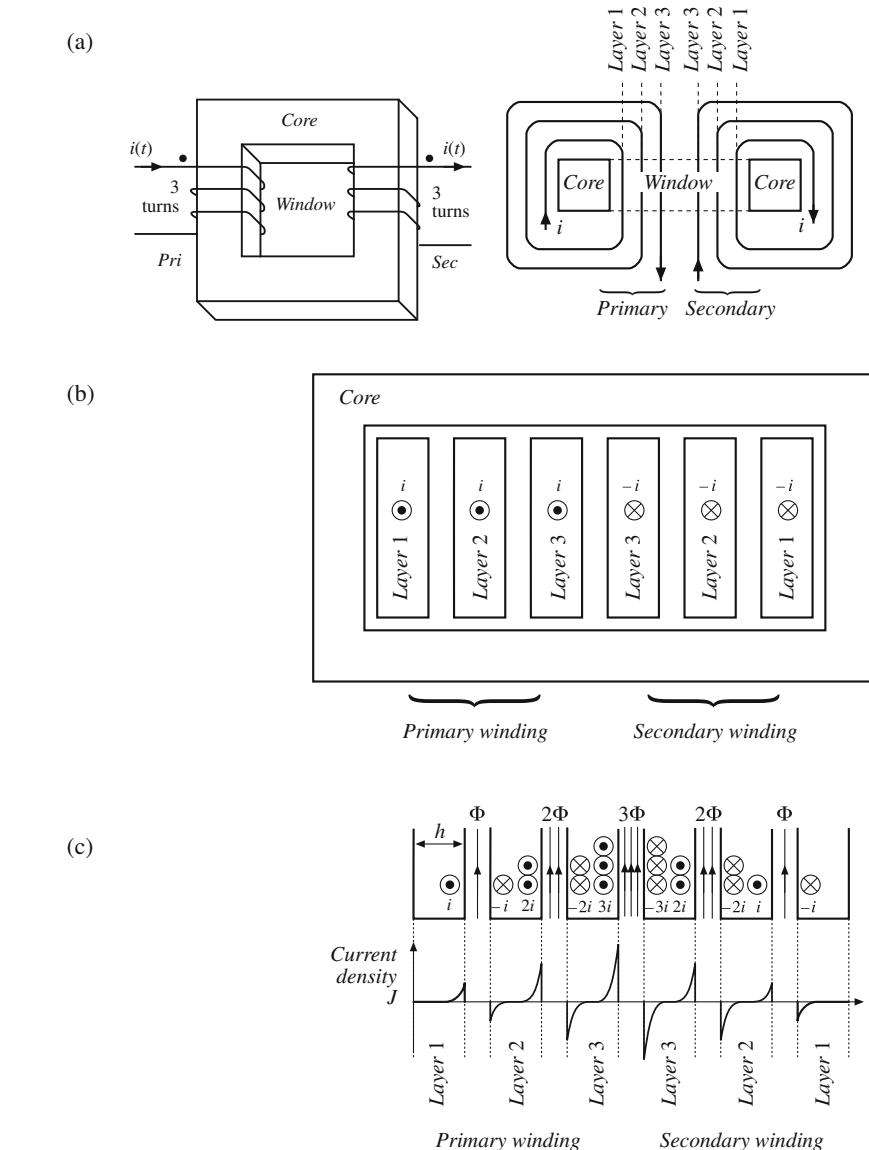


Fig. 10.25 A simple transformer example illustrating the proximity effect: (a) effective core geometry (left) and winding geometry (top view) (right), (b) winding geometry (side view of core window) with one turn per layer, (c) distribution of currents on surfaces of conductors

$$R_{ac} = \frac{h}{\delta} R_{dc} \quad (10.63)$$

The copper loss in layer 1 is

$$P_1 = I^2 R_{ac} \quad (10.64)$$

The proximity effect causes a current to be induced in the adjacent (left-side) surface of primary layer 2, which tends to oppose the flux generated by the current of layer 1. If the

conductors are closely spaced, and if $h \gg \delta$, then the induced current will be equal and opposite to the current $i(t)$, as illustrated in Fig. 10.25c. Hence, current $-i(t)$ flows on the left surface of the second layer. Since layers 1 and 2 are connected in series, they must both conduct the same net current $i(t)$. As a result, a current $+2i(t)$ must flow on the right-side surface of layer 2.

The current flowing on the left surface of layer 2 has the same magnitude as the current of layer 1, and hence the copper loss is the same: P_1 . The current flowing on the right surface of layer 2 has rms magnitude $2I$; hence, it induces copper loss $(2I)^2 R_{ac} = 4P_1$. The total copper loss in primary layer 2 is therefore

$$P_2 = P_1 + 4P_1 = 5P_1 \quad (10.65)$$

The copper loss in the second layer is five times as large as the copper loss in the first layer!

The current $2i(t)$ flowing on the right surface of layer 2 induces a flux $2\Phi(t)$ as illustrated in Fig. 10.25c. This causes an opposing current $-2i(t)$ to flow on the adjacent (left) surface of primary layer 3. Since layer 3 must also conduct net current $i(t)$, a current $+3i(t)$ flows on the right surface of layer 3. The total copper loss in layer 3 is

$$p_3 = (2^2 + 3^2)P_1 = 13P_1 \quad (10.66)$$

Likewise, the copper loss in layer m of a multiple-layer winding can be written

$$P_m = I^2 \left[(m-1)^2 + m^2 \right] \left(\frac{h}{\delta} R_{dc} \right) \quad (10.67)$$

It can be seen that the copper loss compounds very quickly in a multiple-layer winding.

The total copper loss in the three-layer primary winding is $P_1 + 5P_1 + 13P_1$, or $19P_1$. More generally, if the winding contains a total of M layers, then the total copper loss is

$$\begin{aligned} P &= I^2 \left(\frac{h}{\delta} R_{dc} \right) \sum_{m=1}^M [(m-1)^2 + m^2] \\ &= I^2 \left(\frac{h}{\delta} R_{dc} \right) \frac{M}{3} (2M^2 + 1) \end{aligned} \quad (10.68)$$

If a dc or low-frequency ac current of rms amplitude I were applied to the M -layer winding, its copper loss would be $P_{dc} = I^2 M R_{dc}$. Hence, the proximity effect increases the copper loss by the factor

$$F_R = \frac{P}{P_{dc}} = \frac{1}{3} \left(\frac{h}{\delta} \right) (2M^2 + 1) \quad (10.69)$$

This expression is valid for a foil winding having $h \gg \delta$.

As illustrated in Fig. 10.25c, the surface currents in the secondary winding are symmetrical, and hence the secondary winding has the same conduction loss.

The example above and the associated equations are limited to $h \gg \delta$ and to the winding geometry shown. The equations do not quantify the behavior for $h \sim \delta$, nor for round conductors, nor are the equations sufficiently general to cover the more complicated winding geometries often encountered in the magnetic devices of switching converters. Optimum designs may, in fact, occur with conductor thicknesses in the vicinity of one penetration depth. The discussions of the following sections allow computation of proximity losses in more general circumstances.

10.4.2 Leakage Flux in Windings

As described above, an externally applied magnetic field will induce eddy currents to flow in a conductor, and thereby induce copper loss. To understand how magnetic fields are oriented in windings, let us consider the simple two-winding transformer illustrated in Fig. 10.26. In this example, the core has large permeability $\mu \gg \mu_0$. The primary winding consists of eight turns of wire arranged in two layers, and each turn carries current $i(t)$ in the direction indicated. The secondary winding is identical to the primary winding, except that the current polarity is reversed.

Flux lines for typical operation of this transformer are sketched in Fig. 10.26b. As described in Sect. 10.2, a relatively large mutual flux is present, which magnetizes the core. In addition, leakage flux is present, which does not completely link both windings. Because of the symmetry of the winding geometry in Fig. 10.26, the leakage flux runs approximately vertically through the windings.

To determine the magnitude of the leakage flux, we can apply Ampere's law. Consider the closed path taken by one of the leakage flux lines, as illustrated in Fig. 10.27. Since the core has

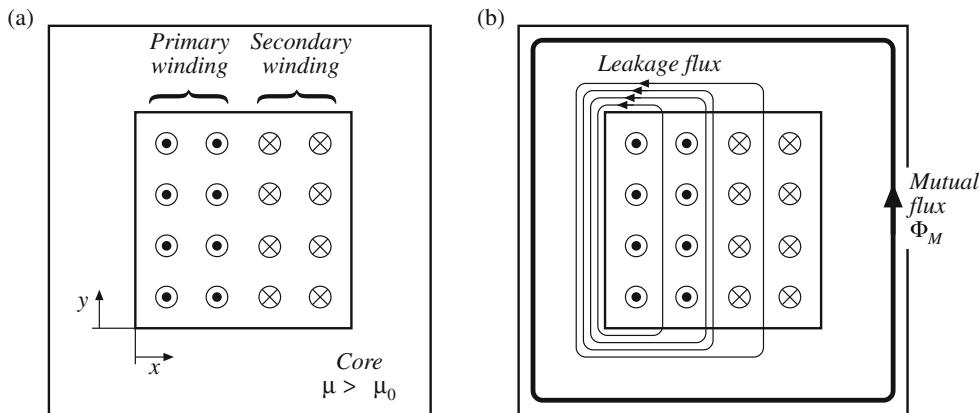
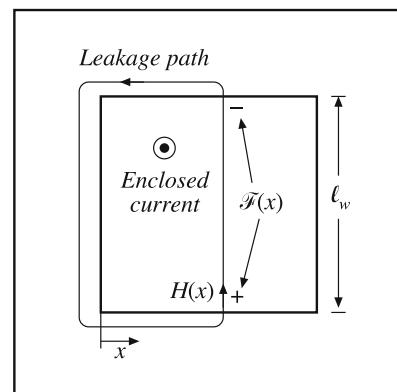


Fig. 10.26 Two-winding transformer example: (a) core and winding geometry, (b) typical flux distribution

Fig. 10.27 Analysis of leakage flux using Ampere's law, for the transformer of Fig. 10.26



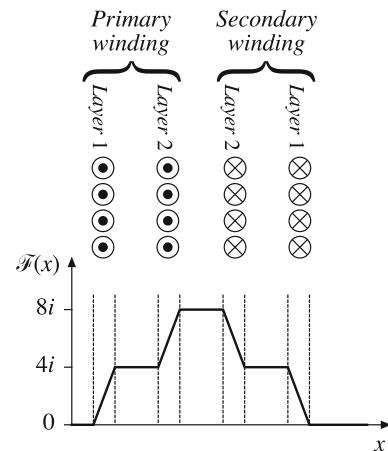


Fig. 10.28 MMF diagram for the transformer winding example of Figs. 10.26 and 10.27

large permeability, we can assume that the MMF induced in the core by this flux is negligible, and that the total MMF around the path is dominated by the MMF $\mathcal{F}(x)$ across the core window. Hence, Ampere's law states that the net current enclosed by the path is equal to the MMF across the air gap:

$$\text{Enclosed current} = \mathcal{F}(x) = H(x)\ell_w \quad (10.70)$$

where ℓ_w is the height of the window as shown in Fig. 10.27. The net current enclosed by the path depends on the number of primary and secondary conductors enclosed by the path, and is therefore a function of the horizontal position x . The first layer of the primary winding consists of 4 turns, each carrying current $i(t)$. So when the path encloses only the first layer of the primary winding, then the enclosed current is $4i(t)$ as shown in Fig. 10.28. Likewise, when the path encloses both layers of the primary winding, then the enclosed current is $8i(t)$. When the path encloses the entire primary, plus layer 2 of the secondary winding, then the net enclosed current is $8i(t) - 4i(t) = 4i(t)$. The MMF $\mathcal{F}(x)$ across the core window is zero outside the winding, and rises to a maximum of $8i(t)$ at the interface between the primary and secondary windings. Since $H(x) = \mathcal{F}(x)/\ell_w$, the magnetic field intensity $H(x)$ is proportional to the sketch of Fig. 10.28.

It should be noted that the shape of the $\mathcal{F}(x)$ curve in the vicinity of the winding conductors depends on the distribution of the current within the conductors. Since this distribution is not yet known, the $\mathcal{F}(x)$ curve of Fig. 10.28 is arbitrarily drawn as straight line segments.

In general, the magnetic fields that surround conductors and lead to eddy currents must be determined using finite element analysis or other similar methods. However, in a large class of coaxial solenoidal winding geometries, the magnetic field lines are nearly parallel to the winding layers. As shown below, we can then obtain an analytical solution for the proximity losses.

10.4.3 Foil Windings and Layers

The winding symmetry described in the previous section allows simplification of the analysis. For the purposes of determining leakage inductance and winding eddy currents, a layer consisting of n_ℓ turns of round wire carrying current $i(t)$ can be approximately modeled as an effective

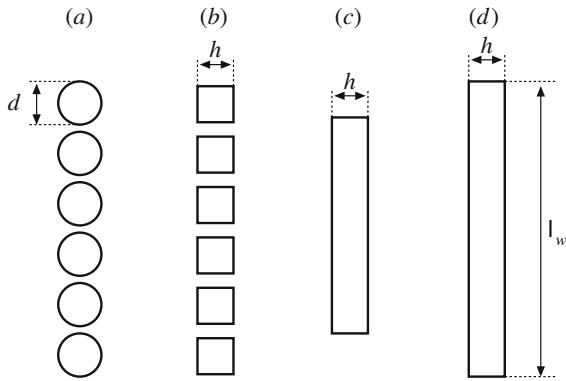


Fig. 10.29 Approximating a layer of round conductors as an effective foil conductor

single turn of foil, which carries current $n_\ell i(t)$. The steps in the transformation of a layer of round conductors into a foil conductor are formalized in Fig. 10.29 [90, 92–95]. The round conductors are replaced by square conductors having the same copper cross-sectional area, Fig. 10.29b. The thickness h of the square conductors is therefore equal to the bare copper wire diameter, multiplied by the factor $\sqrt{\pi/4}$:

$$h = \sqrt{\frac{\pi}{4}} d \quad (10.71)$$

These square conductors are then joined together, into a foil layer (Fig. 10.29c). Finally, the width of the foil is increased, such that it spans the width of the core window (Fig. 10.29d). Since this stretching process increases the conductor cross-sectional area, a compensating factor η must be introduced such that the correct dc conductor resistance is predicted. This factor, sometimes called the *conductor spacing factor* or the winding *porosity*, is defined as the ratio of the actual layer copper area (Fig. 10.29a) to the area of the effective foil conductor of Fig. 10.29d. Porosity is less than unity: $0 \leq \eta \leq 1$. The porosity effectively increases the resistivity ρ of the conductor, and thereby increases its skin depth:

$$\delta' = \frac{\delta}{\sqrt{\eta}} \quad (10.72)$$

If a layer of width ℓ_w contains n_ℓ turns of round wire having diameter d , then the winding porosity η is given by

$$\eta = \sqrt{\frac{\pi}{4}} d \frac{n_\ell}{\ell_w} \quad (10.73)$$

A typical value of η for round conductors that span the width of the winding bobbin is 0.8. In the following analysis, the factor φ is given by h/δ for foil conductors, and by the ratio of the effective foil conductor thickness h to the effective skin depth δ' for round conductors as follows:

$$\varphi = \frac{h}{\delta'} = \sqrt{\eta} \sqrt{\frac{\pi}{4}} \frac{d}{\delta} \quad (10.74)$$

10.4.4 Power Loss in a Layer

In this section, the average power loss P in a uniform layer of thickness h is determined. As illustrated in Fig. 10.30, the magnetic field strengths on the left and right sides of the conductor are denoted $H(0)$ and $H(h)$, respectively. It is assumed that the component of magnetic field normal to the conductor surface is zero. These magnetic fields are driven by the magnetomotive forces $\mathcal{F}(0)$ and $\mathcal{F}(h)$, respectively. Sinusoidal waveforms are assumed, and rms magnitudes are employed. It is further assumed here that $H(0)$ and $H(h)$ are in phase; the effect of a phase shift is treated in [94].

With these assumptions, Maxwell's equations are solved to find the current density distribution in the layer. The power loss density is then computed, and is integrated over the volume of the layer to find the total copper loss in the layer [94]. The result is

$$P = R_{dc} \frac{\Phi}{n_\ell^2} \left[(\mathcal{F}^2(h) + \mathcal{F}^2(0)) G_1(\varphi) - 4\mathcal{F}(h)\mathcal{F}(0)G_2(\varphi) \right] \quad (10.75)$$

where n_ℓ is the number of turns in the layer, and R_{dc} is the dc resistance of the layer. The functions $G_1(\varphi)$ and $G_2(\varphi)$ are

$$\begin{aligned} G_1(\varphi) &= \frac{\sinh(2\varphi) + \sin(2\varphi)}{\cosh(2\varphi) - \cos(2\varphi)} \\ G_2(\varphi) &= \frac{\sinh(\varphi)\cos(\varphi) + \cosh(\varphi)\sin(\varphi)}{\cosh(2\varphi) - \cos(2\varphi)} \end{aligned} \quad (10.76)$$

If the winding carries current of rms magnitude I , then we can write

$$\mathcal{F}(h) - \mathcal{F}(0) = n_\ell I \quad (10.77)$$

Let us further express $\mathcal{F}(h)$ in terms of the winding current I , as

$$\mathcal{F}(h) = mn_\ell I \quad (10.78)$$

The quantity m is therefore the ratio of the MMF $\mathcal{F}(h)$ to the layer ampere-turns $n_\ell I$. Then,

$$\frac{\mathcal{F}(0)}{\mathcal{F}(h)} = \frac{m-1}{m} \quad (10.79)$$

The power dissipated in the layer, Eq. (10.75), can then be written

$$P = I^2 R_{dc} \varphi Q'(\varphi, m) \quad (10.80)$$

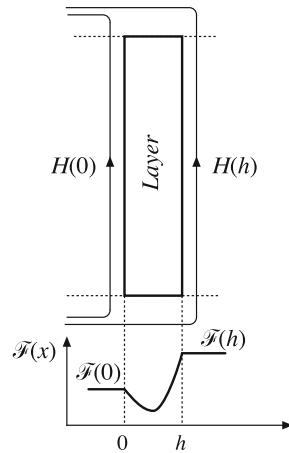


Fig. 10.30 The power loss is determined for a uniform layer. Uniform tangential magnetic fields $H(0)$ and $H(h)$ are applied to the layer surfaces

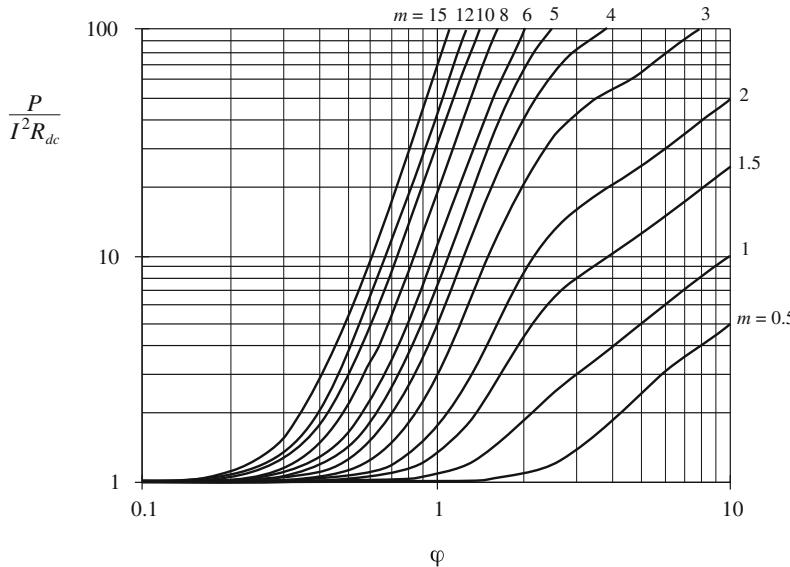


Fig. 10.31 Increase of layer copper loss due to the proximity effect, as a function of φ and MMF ratio m , for sinusoidal excitation

where

$$Q'(\varphi, m) = (2m^2 - 2m + 1)G_1(\varphi) - 4m(m - 1)G_2(\varphi) \quad (10.81)$$

We can conclude that the proximity effect increases the copper loss in the layer by the factor

$$\frac{P}{I^2R_{dc}} = \varphi Q'(\varphi, m) \quad (10.82)$$

Equation (10.82), in conjunction with the definitions (10.81), (10.78), (10.76), and (10.74), can be plotted using a computer spreadsheet or small computer program. The result is illustrated in Fig. 10.31, for several values of m .

It is illuminating to express the layer copper loss P in terms of the dc power loss $P_{dc}|_{\varphi=1}$ that would be obtained in a foil conductor having a thickness $\varphi = 1$. This loss is found by dividing Eq. (10.82) by the effective thickness ratio φ :

$$\frac{P}{P_{dc}|_{\varphi=1}} = Q'(\varphi, m) \quad (10.83)$$

Equation (10.83) is plotted in Fig. 10.32. Large copper loss is obtained for small φ simply because the layer is thin and hence the dc resistance of the layer is large. For large m and large φ , the proximity effect leads to large power loss; Eq. (10.67) predicts that $Q'(\varphi, m)$ is asymptotic to $m^2 + (m - 1)^2$ for large φ . Between these extremes, there is a value of φ which minimizes the layer copper loss.

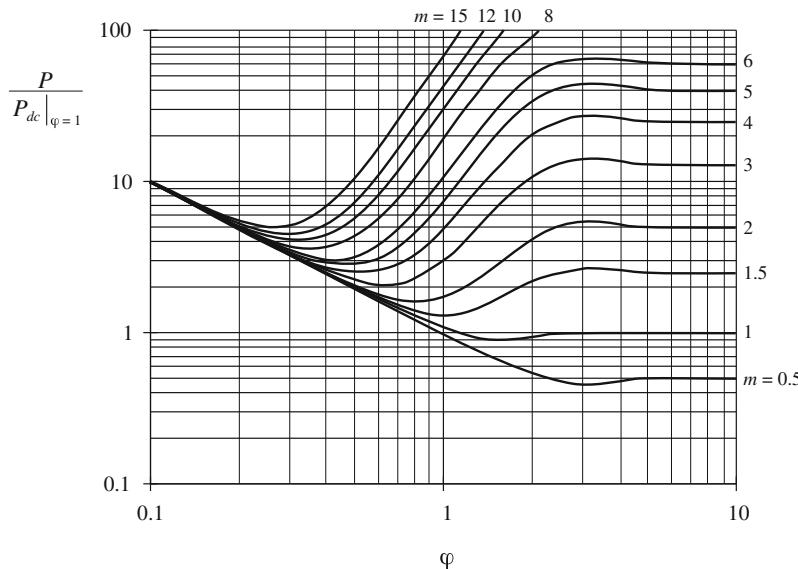


Fig. 10.32 Layer copper loss, relative to the dc loss in a layer having effective thickness of one penetration depth

10.4.5 Example: Power Loss in a Transformer Winding

Let us again consider the proximity loss in a conventional transformer, in which the primary and secondary windings each consist of M layers. The normalized MMF diagram is illustrated in Fig. 10.33. As given by Eq. (10.82), the proximity effect increases the copper loss in each layer by the factor $\varphi Q'(\varphi, m)$. The total increase in primary winding copper loss P_{pri} is found by summation over all of the primary layers:

$$F_R = \frac{P_{pri}}{P_{pri,dc}} = \frac{1}{M} \sum_{m=1}^M \varphi Q'(\varphi, m) \quad (10.84)$$

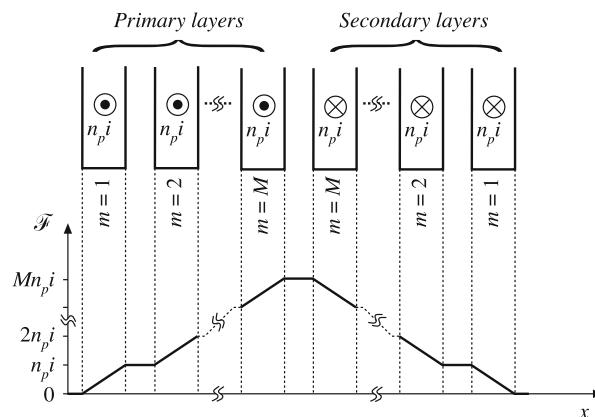


Fig. 10.33 Conventional two-winding transformer example. Each winding consists of M layers

Owing to the symmetry of the windings in this example, the secondary winding copper loss is increased by the same factor. Upon substituting Eq. (10.81) and collecting terms, we obtain

$$F_R = \frac{\varphi}{M} \sum_{m=1}^M [m^2 (2G_1(\varphi) - 4G_2(\varphi)) - m (2G_1(\varphi) - 4G_2(\varphi)) + G_1(\varphi)] \quad (10.85)$$

The summation can be expressed in closed form with the help of the identities

$$\sum_{m=1}^M m = \frac{M(M+1)}{2} \quad (10.86)$$

$$\sum_{m=1}^M m^2 = \frac{M(M+1)(2M+1)}{6}$$

Use of these identities to simplify Eq. (10.85) leads to

$$F_R = \varphi \left[G_1(\varphi) + \frac{2}{3} (M^2 - 1) (G_1(\varphi) - 2G_2(\varphi)) \right] \quad (10.87)$$

This expression is plotted in Fig. 10.34, for several values of M . For large φ , $G_1(\varphi)$ tends to 1, while $G_2(\varphi)$ tends to 0. It can be verified that F_R then tends to the value predicted by Eq. (10.69).

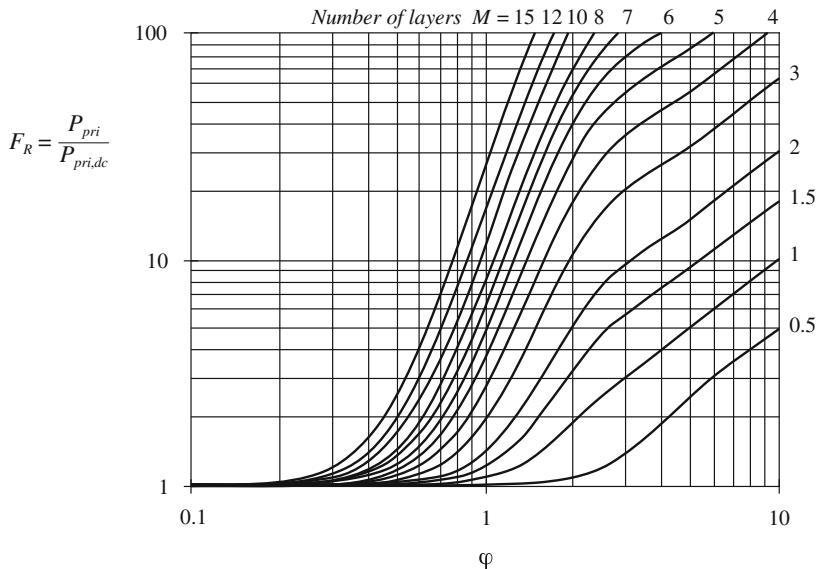


Fig. 10.34 Increased total winding copper loss in the two-winding transformer example, as a function of φ and number of layers M , for sinusoidal excitation

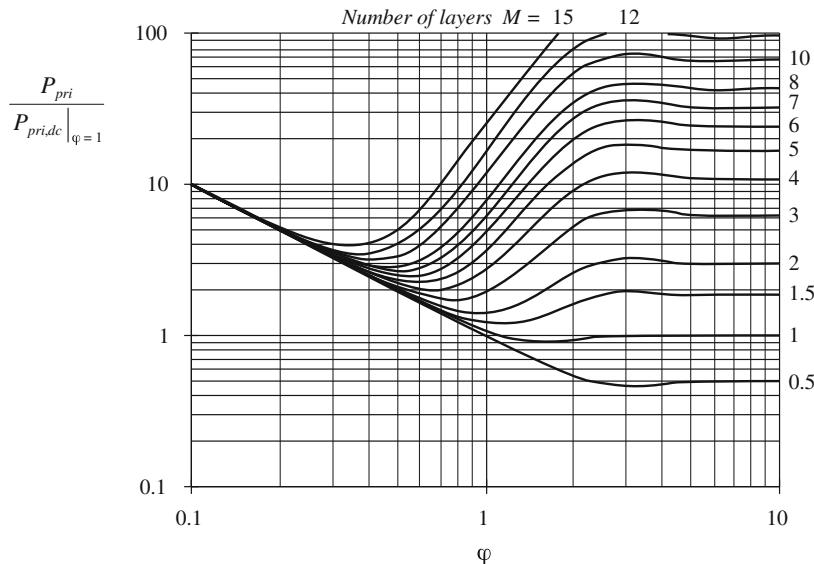


Fig. 10.35 Transformer example winding total copper loss, relative to the winding dc loss for layers having effective thicknesses of one penetration depth

We can again express the total primary power loss in terms of the dc power loss that would be obtained using a conductor in which $\varphi = 1$. This loss is found by dividing Eq. (10.87) by φ :

$$\frac{P_{pri}}{P_{pri,dc}|_{\varphi=1}} = G_1(\varphi) + \frac{2}{3} (M^2 - 1) (G_1(\varphi) - 2G_2(\varphi)) \quad (10.88)$$

This expression is plotted in Fig. 10.35, for several values of M . Depending on the number of layers, the minimum copper loss for sinusoidal excitation is obtained for φ near to, or somewhat less than, unity.

10.4.6 Interleaving the Windings

One way to reduce the copper losses due to the proximity effect is to interleave the windings. Figure 10.36 illustrates the MMF diagram for a simple transformer in which the primary and secondary layers are alternated, with net layer current of magnitude i . It can be seen that each layer operates with $\mathcal{F} = 0$ on one side, and $\mathcal{F} = i$ on the other. Hence, each layer operates effectively with $m = 1$. Note that Eq. (10.75) is symmetric with respect to $\mathcal{F}(0)$ and $\mathcal{F}(h)$; hence, the copper losses of the interleaved secondary and primary layers are identical. The proximity losses of the entire winding can therefore be determined directly from Figs. 10.34 and 10.35, with $M = 1$. It can be shown that the minimum copper loss for this case (with sinusoidal currents) occurs with $\varphi = \pi/2$, although the copper loss is nearly constant for any $\varphi \geq 1$, and is approximately equal to the dc copper loss obtained when $\varphi = 1$. It should be apparent that interleaving can lead to significant improvements in copper loss when the winding contains several layers.

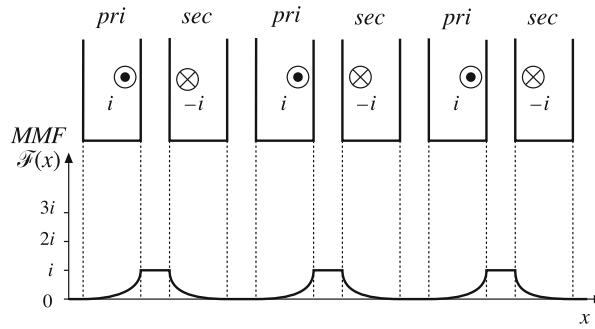


Fig. 10.36 MMF diagram for a simple transformer with interleaved windings. Each layer operates with $m = 1$

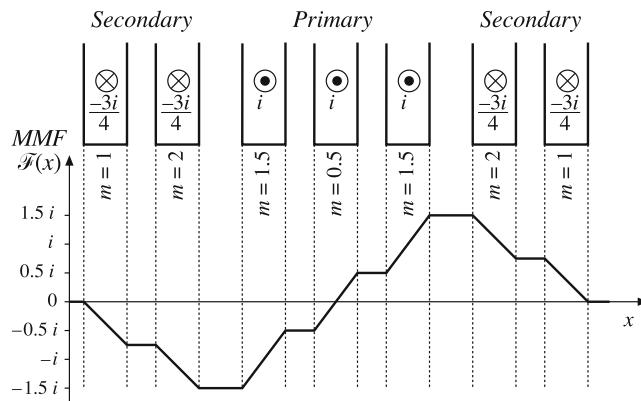


Fig. 10.37 A partially interleaved two-winding transformer, illustrating fractional values of m . The MMF diagram is constructed for the low-frequency limit

Partial interleaving can lead to a partial improvement in proximity loss. Figure 10.37 illustrates a transformer having three primary layers and four secondary layers. If the total current carried by each primary layer is $i(t)$, then each secondary layer should carry current $0.75i(t)$. The maximum MMF again occurs in the spaces between the primary and secondary windings, but has value $1.5i(t)$.

To determine the value for m in a given layer, we can solve Eq. (10.79) for m :

$$m = \frac{\mathcal{F}(h)}{\mathcal{F}(h) - \mathcal{F}(0)} \quad (10.89)$$

The above expression is valid in general, and Eq. (10.75) is symmetrical in $\mathcal{F}(0)$ and $\mathcal{F}(h)$. Interchanging $\mathcal{F}(0)$ and $\mathcal{F}(h)$ leads to a different value for m but does not change the result of Eq. (10.81). When $F(0)$ is greater in magnitude than $\mathcal{F}(h)$, it is convenient to interchange the roles of $\mathcal{F}(0)$ and $\mathcal{F}(h)$, so that the plots of Figs. 10.31 and 10.32 can be employed.

In the leftmost secondary layer of Fig. 10.37, the layer carries current $-0.75i$. The MMF changes from 0 to $-0.75i$. The value of m for this layer is found by evaluation of Eq. (10.89):

$$m = \frac{\mathcal{F}(h)}{\mathcal{F}(h) - \mathcal{F}(0)} = \frac{-0.75i}{-0.75i - 0} = 1 \quad (10.90)$$

The loss in this layer, relative to the dc loss of this secondary layer, can be determined using the plots of Figs. 10.31 and 10.32 with $m = 1$. For the next secondary layer, we obtain

$$m = \frac{\mathcal{F}(h)}{\mathcal{F}(h) - \mathcal{F}(0)} = \frac{-1.5i}{-1.5i - (-0.75i)} = 2 \quad (10.91)$$

Hence the loss in this layer can be determined using the plots of Figs. 10.31 and 10.32 with $m = 2$. The next layer is a primary winding layer. Its value of m can be expressed as

$$m = \frac{\mathcal{F}(0)}{\mathcal{F}(0) - \mathcal{F}(h)} = \frac{-1.5i}{-1.5i - (-0.5i)} = 1.5 \quad (10.92)$$

The loss in this layer, relative to the dc loss of this primary layer, can be determined using the plots of Figs. 10.31 and 10.32 with $m = 1.5$. The center layer has an m of

$$m = \frac{\mathcal{F}(h)}{\mathcal{F}(h) - \mathcal{F}(0)} = \frac{0.5i}{0.5i - (-0.5i)} = 0.5 \quad (10.93)$$

The loss in this layer, relative to the dc loss of this primary layer, can be determined using the plots of Figs. 10.31 and 10.32 with $m = 0.5$. The remaining layers are symmetrical to the corresponding layers described above, and have identical copper losses. The total loss in the winding is found by summing the losses described above for each layer.

Interleaving windings can significantly reduce the proximity loss when the primary and secondary currents are in phase. However, in some cases such as the transformers of the flyback and SEPIC converters, the winding currents are out of phase. Interleaving then does little to reduce the MMFs and magnetic fields in the vicinity of the windings, and hence the proximity loss is essentially unchanged. It should also be noted that Eqs. (10.75) to (10.83) assume that the winding currents are in phase. General expressions for out of phase currents, as well as analysis of a flyback example, are given in [94].

The above procedure can be used to determine the high-frequency copper losses of more complicated multiple-winding magnetic devices. The MMF diagrams are constructed, and then the power loss in each layer is evaluated using Eq. (10.82). These losses are summed, to find the total copper loss. The losses induced in electrostatic shields can also be determined. Several additional examples are given in [94].

It can be concluded that, for sinusoidal currents, there is an optimal conductor thickness in the vicinity of $\varphi = 1$ that leads to minimum copper loss. It is highly advantageous to minimize the number of layers, and to interleave the windings. The amount of copper in the vicinity of the high-MMF portions of windings should be kept to a minimum. Core geometries that maximize the width ℓ_w of the layers, while minimizing the overall number of layers, lead to reduced proximity loss.

Use of *Litz* wire is another means of increasing the conductor area while maintaining low proximity losses. Tens, hundreds, or more strands of small-gauge insulated copper wire are bundled together, and are externally connected in parallel. These strands are twisted, or transposed, such that each strand passes equally through each position inside and on the surface of the bundle. This prevents the circulation of high-frequency currents between strands. To be effective, the diameter of the strands should be sufficiently less than one skin depth. Also, it should be

pointed out that the Litz wire bundle itself is composed of multiple layers. The disadvantages of Litz wire are its increased cost, and its reduced fill factor. The name “Litz” is derived from the German word *Litzendraht*, or braided.

10.4.7 PWM Waveform Harmonics

The pulse-width modulated waveforms encountered in switching converters contain significant harmonics, which can lead to increased proximity losses. The effect of harmonics on the losses in a layer can be determined via field harmonic analysis [94], in which the MMF waveforms $\mathcal{F}(0, t)$ and $\mathcal{F}(d, t)$ of Eq. (10.75) are expressed in Fourier series. The power loss of each individual harmonic is computed as in Sect. 10.4.4, and the losses are summed to find the total loss in a layer. For example, the PWM waveform of Fig. 10.38 can be represented by the following Fourier series:

$$i(t) = I_0 + \sum_{j=1}^{\infty} \sqrt{2} I_j \cos(j\omega t) \quad (10.94)$$

where

$$I_j = \frac{\sqrt{2} I_{pk}}{j\pi} \sin(j\pi D)$$

with $\omega = 2\pi/T_s$. This waveform contains a dc component $I_0 = DI_{pk}$, plus harmonics of rms magnitude I_j proportional to $1/j$. The transformer winding current waveforms of most switching converters follow this Fourier series, or a similar series.

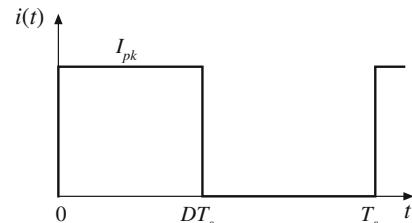


Fig. 10.38 Pulse-width modulated winding current waveform

Effects of waveforms harmonics on proximity losses are discussed in [92–94]. The dc component of the winding currents does not lead to proximity loss, and should not be included in proximity loss calculations. Failure to remove the dc component can lead to significantly pessimistic estimates of copper loss. The skin depth δ is smaller for high-frequency harmonics than for the fundamental, and hence the waveform harmonics exhibit an increased effective φ . Let φ_1 be given by Eq. (10.74), in which δ is found by evaluation of Eq. (10.61) at the fundamental frequency. Since the penetration depth δ varies as the inverse square-root of frequency, the effective value of φ for harmonic j is

$$\varphi_j = \sqrt{j} \varphi_1 \quad (10.95)$$

In a multiple-layer winding excited by a current waveform whose fundamental component has $\varphi = \varphi_1$ close to 1, harmonics can significantly increase the total copper loss. This occurs because, for $m > 1$, $Q'(\varphi, m)$ is a rapidly increasing function of φ in the vicinity of 1. When

φ_1 is sufficiently greater than 1, then $Q'(\varphi, m)$ is nearly constant, and harmonics have less influence on the total copper loss.

For example, suppose that the two-winding transformer of Fig. 10.33 is employed in a converter such as the forward converter, in which a winding current waveform $i(t)$ can be well approximated by the Fourier series of Eq. (10.94). The winding contains M layers, and has dc resistance R_{dc} . The copper loss induced by the dc component is

$$P_{dc} = I_0^2 R_{dc} \quad (10.96)$$

The copper loss P_j ascribable to harmonic j is found by evaluation of Eq. (10.87) with $\varphi = \varphi_j$:

$$P_j = I_j^2 R_{dc} \sqrt{j} \varphi_1 \left[G_1(\sqrt{j} \varphi_1) + \frac{2}{3}(M^2 - 1)(G_1(\sqrt{j} \varphi_1) - 2G_2(\sqrt{j} \varphi_1)) \right] \quad (10.97)$$

The total copper loss in the winding is the sum of losses arising from all components of the harmonic series:

$$\frac{P_{cu}}{DI_{pk}^2 R_{dc}} = D + \frac{2\varphi_1}{D\pi^2} \sum_{j=1}^{\infty} \frac{\sin^2(j\pi D)}{j\sqrt{j}} \left[G_1(\sqrt{j} \varphi_1) + \frac{2}{3}(M^2 - 1)(G_1(\sqrt{j} \varphi_1) - 2G_2(\sqrt{j} \varphi_1)) \right] \quad (10.98)$$

In Eq. (10.98), the copper loss is expressed relative to the loss $DI_{pk}^2 R_{dc}$ predicted by a low-frequency analysis. This expression can be evaluated by use of a computer program or computer spreadsheet.

To explicitly quantify the effects of harmonics, we can define the harmonic loss factor F_H as

$$F_H = \frac{\sum_{j=1}^{\infty} P_j}{P_1} \quad (10.99)$$

with P_j given by Eq. (10.97). The total winding copper loss is then given by

$$P_{cu} = I_0^2 R_{dc} + F_H F_R I_1^2 R_{dc} \quad (10.100)$$

with F_R given by Eq. (10.87). The harmonic factor F_H is a function not only of the winding geometry, but also of the harmonic spectrum of the winding current waveform. The harmonic factor F_H is plotted in Fig. 10.39 for several values of D , for the simple transformer example. The total harmonic distortion (THD) of the example current waveforms are: 48% for $D = 0.5$, 76% for $D = 0.3$, and 191% for $D = 0.1$. The waveform THD is defined as

$$\text{THD} = \frac{\sqrt{\sum_{j=2}^{\infty} I_j^2}}{I_1} \quad (10.101)$$

It can be seen that harmonics significantly increase the proximity loss of a multi-layer winding when φ_1 is close to 1. For sufficiently small φ_1 , the proximity effect can be neglected, and F_H tends to the value $1 + (\text{THD})^2$. For large φ_1 , the harmonics also increase the proximity loss; however, the increase is less dramatic than for φ_1 near 1 because the fundamental component proximity loss is large. It can be concluded that, when the current waveform contains high THD and when the winding contains several layers or more, then proximity losses can be kept low only by choosing φ_1 much less than 1. Interleaving the windings allows a larger value of φ_1 to be employed.

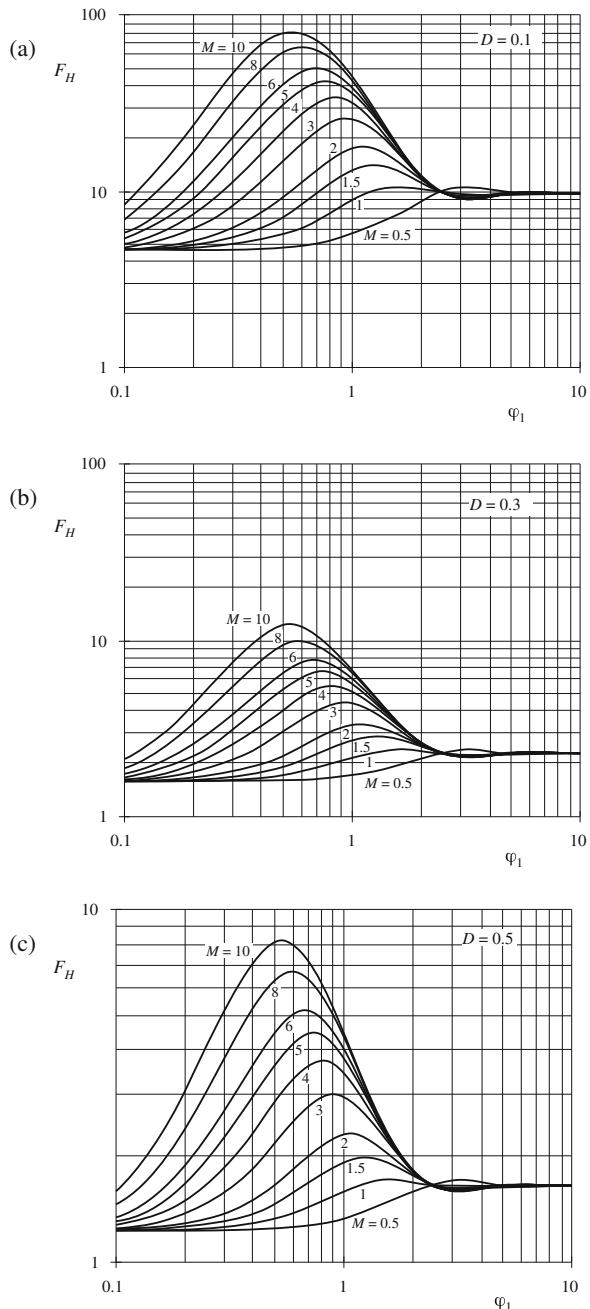


Fig. 10.39 Increased proximity losses induced by PWM waveform harmonics, forward converter example: (a) at $D = 0.1$, (b) at $D = 0.3$, (c) at $D = 0.5$

10.5 Several Types of Magnetic Devices, Their B - H Loops, and Core vs. Copper Loss

A variety of magnetic elements are commonly used in power applications, which employ the properties of magnetic core materials and windings in different ways. As a result, quite a few factors constrain the design of a magnetic device. The maximum flux density must not saturate the core. The peak ac flux density should also be sufficiently small, such that core losses are acceptably low. The wire size should be sufficiently small, to fit the required number of turns in the core window. Subject to this constraint, the wire cross-sectional area should be as large as possible, to minimize the winding dc resistance and copper loss. But if the wire is too thick, then unacceptable copper losses occur owing to the proximity effect. An air gap is needed when the device stores significant energy. But an air gap is undesirable in transformer applications. It should be apparent that, for a given magnetic device, some of these constraints are active while others are not significant.

Thus, design of a magnetic element involves not only obtaining the desired inductance or turns ratio, but also ensuring that the core material does not saturate and that the total power loss is not too large. Several common power applications of magnetics are discussed in this section, which illustrate the factors governing the choice of core material, maximum flux density, and design approach.

10.5.1 Filter Inductor

A filter inductor employed in a CCM buck converter is illustrated in Fig. 10.40a. In this application, the value of inductance L often is chosen such that the inductor current ripple peak magnitude Δi is a small fraction of the full-load inductor current dc component I , as illustrated

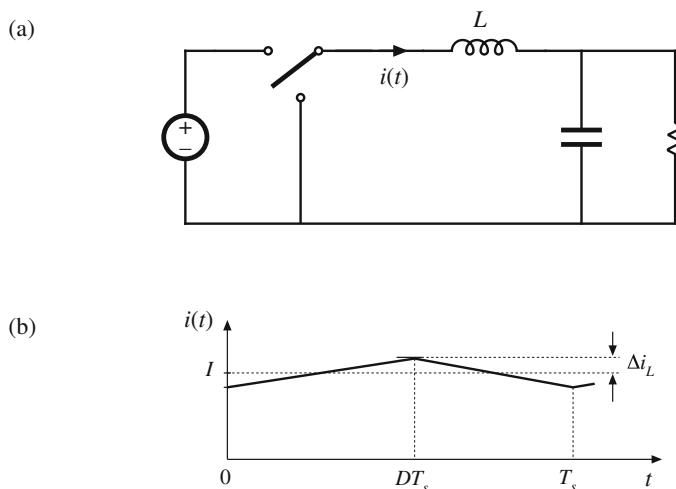


Fig. 10.40 Filter inductor employed in a CCM buck converter: (a) circuit schematic, (b) inductor current waveform

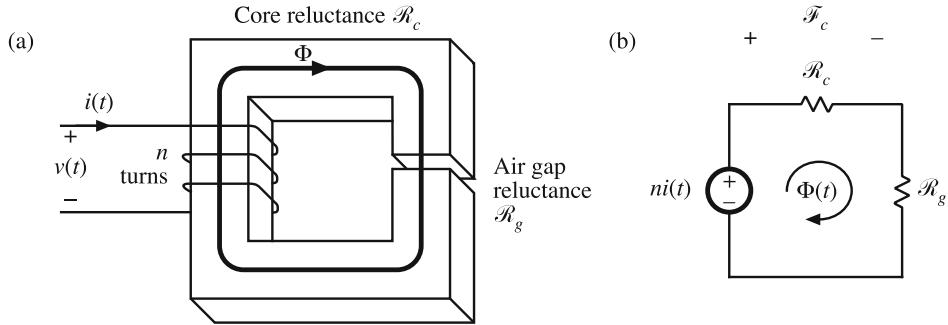
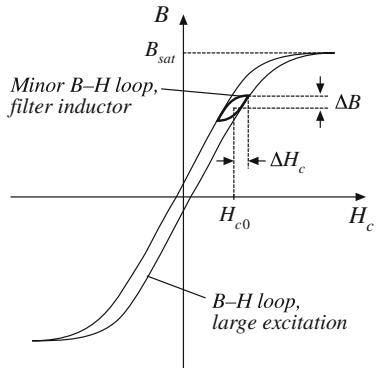


Fig. 10.41 Filter inductor: (a) structure, (b) magnetic circuit model

Fig. 10.42 Filter inductor minor B - H loop



in Fig. 10.40b. As illustrated in Fig. 10.41, an air gap is employed that is sufficiently large to prevent saturation of the core by the peak current $I + \Delta i$.

The core magnetic field strength $H_c(t)$ is related to the winding current $i(t)$ according to

$$H_c(t) = \frac{ni(t)}{\ell_c} \frac{\mathcal{R}_c}{\mathcal{R}_c + \mathcal{R}_g} \quad (10.102)$$

where ℓ_c is the magnetic path length of the core. Since $H_c(t)$ is proportional to $i(t)$, $H_c(t)$ can be expressed as a large dc component H_{c0} and a small superimposed ac ripple ΔH_c , where

$$\begin{aligned} H_{c0} &= \frac{nI}{\ell_c} \frac{\mathcal{R}_c}{\mathcal{R}_c + \mathcal{R}_g} \\ \Delta H_c &= \frac{n\Delta i}{\ell_c} \frac{\mathcal{R}_c}{\mathcal{R}_c + \mathcal{R}_g} \end{aligned} \quad (10.103)$$

A sketch of $B(t)$ vs. $H_c(t)$ for this application is given in Fig. 10.42. This device operates with the minor B - H loop illustrated. The size of the minor loop, and hence the core loss, depends on the magnitude of the inductor current ripple Δi . The copper loss depends on the rms inductor

current ripple, essentially equal to the dc component I . Typically, the core loss can be ignored, and the design is driven by the copper loss. The maximum flux density is limited by saturation of the core. Proximity losses are negligible. Although a high-frequency ferrite material can be employed in this application, other materials having higher core losses and greater saturation flux density lead to a physically smaller device. Design of a filter inductor in which the maximum flux density is a specified value is considered in the next chapter.

10.5.2 AC Inductor

An ac inductor employed in a resonant converter is illustrated in Fig. 10.43. In this application, the high-frequency current variations are large. In consequence, the $B(t) - H(t)$ loop illustrated in Fig. 10.44 is large. Core loss and proximity loss are usually significant in this application. The maximum flux density is limited by core loss rather than saturation. Both core loss and copper loss must be accounted for in the design of this element, and the peak ac flux density ΔB is a design variable that is typically chosen to minimize the total loss. A high-frequency material having low core loss, such as ferrite, is normally employed. Design of magnetics such as this, in which the ac flux density is a design variable that is chosen in a optimal manner, is considered in Chap. 12.

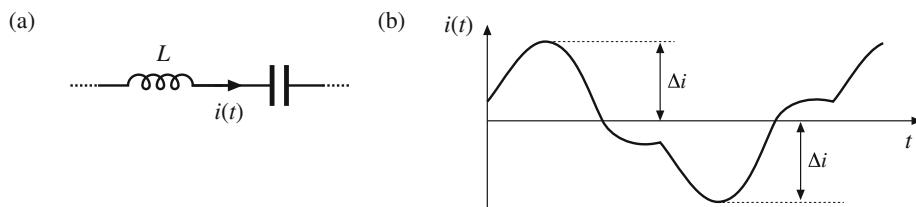
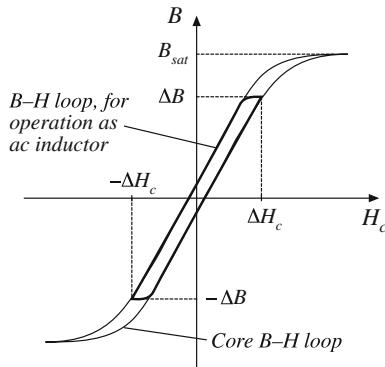


Fig. 10.43 Ac inductor, resonant converter example: (a) resonant tank circuit, (b) inductor current waveform

Fig. 10.44 Operational B - H loop of an ac inductor



10.5.3 Transformer

Figure 10.45 illustrates a conventional transformer employed in a switching converter. Magnetization of the core is modeled by the magnetizing inductance L_M . The magnetizing current $i_M(t)$ is related to the core magnetic field $H(t)$ according to Ampere's law

$$H(t) = \frac{n i_M(t)}{\ell_m} \quad (10.104)$$

However, $i_M(t)$ is not a direct function of the winding currents $i_1(t)$ or $i_2(t)$. Rather, the magnetizing current is dependent on the applied winding voltage waveform $v_1(t)$. Specifically, the maximum ac flux density is directly proportional to the applied volt-seconds λ_1 . A typical B - H loop for this application is illustrated in Fig. 10.46.

In the transformer application, core loss and proximity losses are usually significant. Typically the maximum flux density is limited by core loss rather than by saturation. A high-frequency material having low core loss is employed; in a transformer-isolated switching converter, ferrite typically is used. Both core and copper losses must be accounted for in the design of the transformer. The design must also incorporate multiple windings. Transformer design with flux density optimized for minimum total loss is described in Chap. 12.

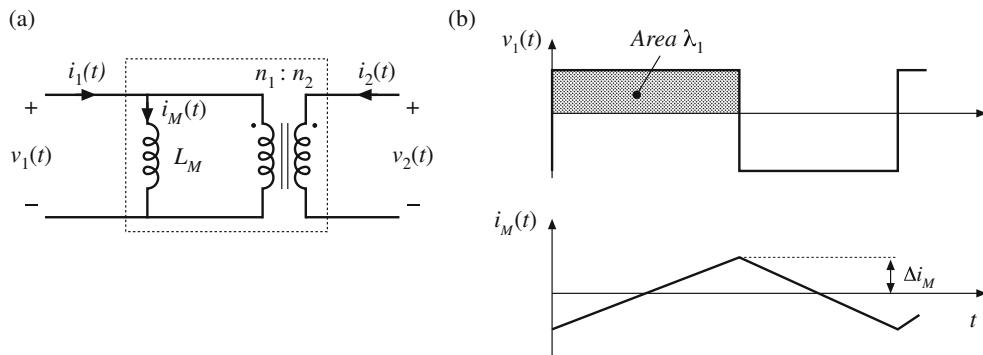
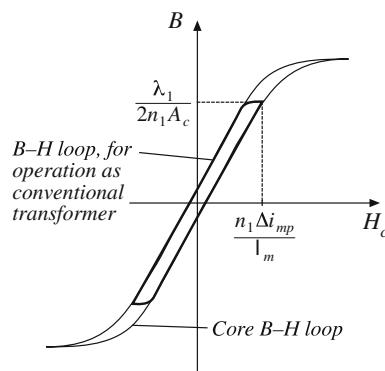


Fig. 10.45 Conventional transformer: (a) equivalent circuit, (b) typical primary voltage and magnetizing current waveforms

Fig. 10.46 Operational B - H loop of a conventional transformer



10.5.4 Coupled Inductor

A coupled inductor is a filter inductor having multiple windings. Figure 10.47a illustrates coupled inductors in a two-output forward converter. The inductors can be wound on the same core, because the winding voltage waveforms are proportional. The inductors of the SEPIC and Ćuk converters, as well as of multiple-output buck-derived converters and some other converters, can be coupled. The inductor current ripples can be controlled by control of the winding leakage inductances [97, 98]. Dc currents flow in each winding as illustrated in Fig. 10.47b, and the net magnetization of the core is proportional to the sum of the winding ampere-turns:

$$H_c(t) = \frac{n_1 i_1(t) + n_2 i_2(t)}{\ell_c} \frac{\mathcal{R}_c}{\mathcal{R}_c + \mathcal{R}_g} \quad (10.105)$$

As in the case of the single winding filter inductor, the size of the minor B - H loop is proportional to the total current ripple (Fig. 10.48). Small ripple implies small core loss, as well as small proximity loss. An air gap is employed, and the maximum flux density is typically limited by saturation.

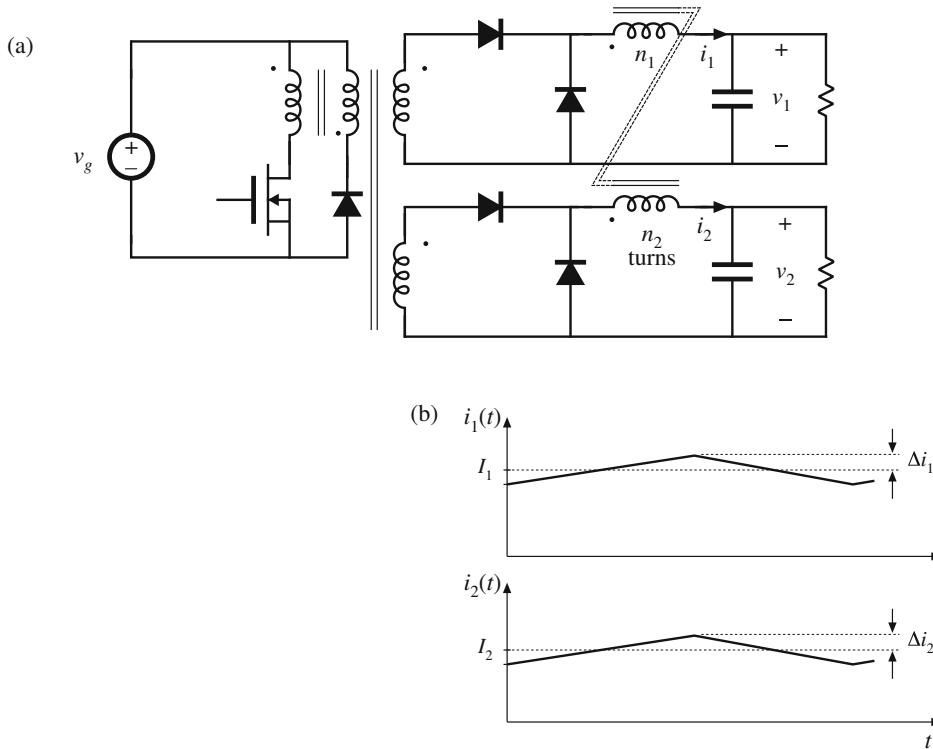
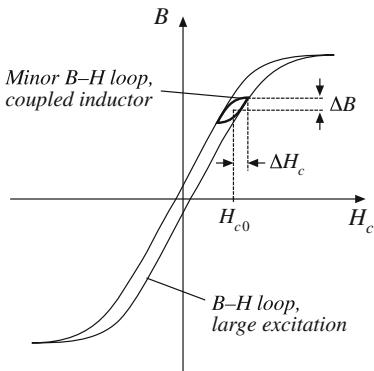


Fig. 10.47 Coupling the output filter inductors of a two-output forward converter: (a) schematic, (b) typical inductor current waveforms

Fig. 10.48 Coupled inductor minor B - H loop



10.5.5 Flyback Transformer

As discussed in Chap. 6, the flyback transformer functions as an inductor with two windings. The primary winding is used during the transistor conduction interval, and the secondary is used during the diode conduction interval. A flyback converter is illustrated in Fig. 10.49a, with the flyback transformer modeled as a magnetizing inductance in parallel with an ideal transformer. The magnetizing current $i_M(t)$ is proportional to the core magnetic field strength $H_c(t)$. Typical DCM waveforms are given in Fig. 10.49b.

Since the flyback transformer stores energy, an air gap is needed. Core loss depends on the magnitude of the ac component of the magnetizing current. The B - H loop for discontinuous conduction mode operation is illustrated in Fig. 10.50. When the converter is designed to operate in DCM, the core loss is significant. The peak ac flux density ΔB is then chosen to maintain an acceptably low core loss. For CCM operation, core loss is less significant, and the maximum flux density may be limited only by saturation of the core. In either case, winding proximity losses are typically quite significant. Unfortunately, interleaving the windings has little impact on the proximity loss because the primary and secondary winding currents are out of phase.

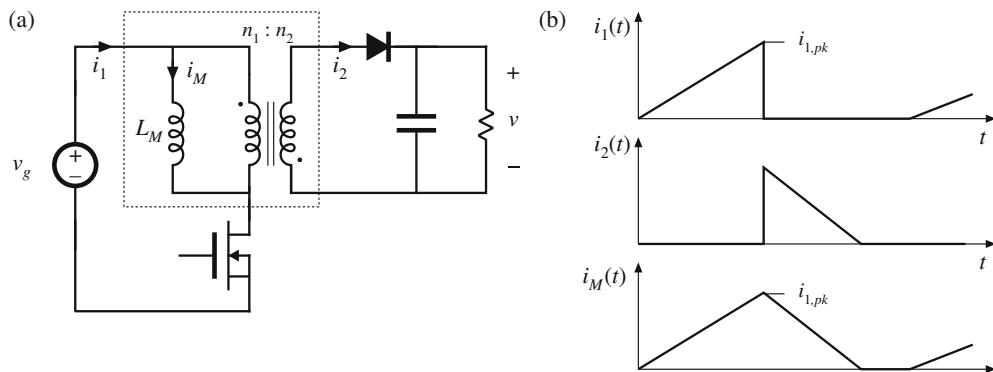
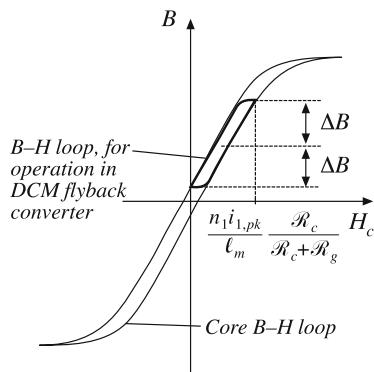


Fig. 10.49 Flyback transformer: (a) converter schematic, with transformer equivalent circuit; (b) DCM current waveforms

Fig. 10.50 Operational B - H loop of a DCM flyback transformer



10.6 Summary of Key Points

1. Magnetic devices can be modeled using lumped-element magnetic circuits, in a manner similar to that commonly used to model electrical circuits. The magnetic analogs of electrical voltage V , current I , and resistance R are magnetomotive force (MMF) \mathcal{F} , flux Φ , and reluctance \mathcal{R} , respectively.
2. Faraday's law relates the voltage induced in a loop of wire to the derivative of flux passing through the interior of the loop.
3. Ampere's law relates the total MMF around a loop to the total current passing through the center of the loop. Ampere's law implies that winding currents are sources of MMF, and that when these sources are included, then the net MMF around a closed path is equal to zero.
4. Magnetic core materials exhibit hysteresis and saturation. A core material saturates when the flux density B reaches the saturation flux density B_{sat} .
5. Air gaps are employed in inductors to prevent saturation when a given maximum current flows in the winding, and to stabilize the value of inductance. The inductor with air gap can be analyzed using a simple magnetic equivalent circuit, containing core and air gap reluctances and a source representing the winding MMF.
6. Conventional transformers can be modeled using sources representing the MMFs of each winding, and the core MMF. The core reluctance approaches zero in an ideal transformer. Nonzero core reluctance leads to an electrical transformer model containing a magnetizing inductance, effectively in parallel with the ideal transformer. Flux that does not link both windings, or "leakage flux," can be modeled using series inductors.
7. The conventional transformer saturates when the applied winding volt-seconds are too large. Addition of an air gap has no effect on saturation. Saturation can be prevented by increasing the core cross-sectional area, or by increasing the number of primary turns.
8. Magnetic materials exhibit core loss, due to hysteresis of the B - H loop and to induced eddy currents flowing in the core material. In available core materials, there is a tradeoff between high saturation flux density B_{sat} and high core loss P_{fe} . Laminated iron alloy cores exhibit the highest B_{sat} but also the highest P_{fe} , while ferrite cores exhibit the lowest P_{fe} but also the lowest B_{sat} . Between these two extremes are powdered iron alloy and amorphous alloy materials.
9. The skin and proximity effects lead to eddy currents in winding conductors, which increase the copper loss P_{cu} in high-current high-frequency magnetic devices. When a conductor has

thickness approaching or larger than the penetration depth δ , magnetic fields in the vicinity of the conductor induce eddy currents in the conductor. According to Lenz's law, these eddy currents flow in paths that tend to oppose the applied magnetic fields.

10. The magnetic field strengths in the vicinity of the winding conductors can be determined by use of MMF diagrams. These diagrams are constructed by application of Ampere's law, following the closed paths of the magnetic field lines which pass near the winding conductors. Multiple-layer noninterleaved windings can exhibit high maximum MMFs, with resulting high eddy currents and high copper loss.
11. An expression for the copper loss in a layer, as a function of the magnetic field strengths or MMFs surrounding the layer, is given in Sect. 10.4.4. This expression can be used in conjunction with the MMF diagram, to compute the copper loss in each layer of a winding. The results can then be summed, yielding the total winding copper loss. When the effective layer thickness is near to or greater than one skin depth, the copper losses of multiple-layer noninterleaved windings are greatly increased.
12. Pulse-width modulated winding currents contain significant total harmonic distortion; this can lead to a further increase of copper loss. The increase in proximity loss caused by current harmonics is most pronounced in multiple-layer noninterleaved windings, with an effective layer thickness near one skin depth.

PROBLEMS

- 10.1** The core illustrated in Fig. 10.51a is 1 cm thick. All legs are 1 cm wide, except for the right-hand side vertical leg, which is 0.5 cm wide. You may neglect nonuniformities in the flux distribution caused by turning comers.

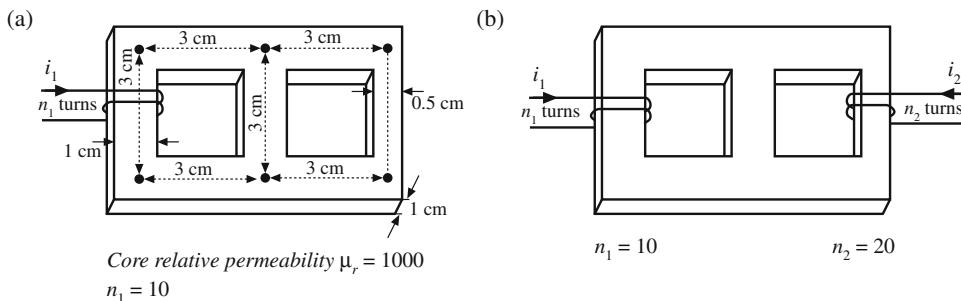


Fig. 10.51 Problem 10.1

- (a) Determine the magnetic circuit model of this device, and label the values of all reluctances in your model.
 - (b) Determine the inductance of the winding.
- A second winding is added to the same core, as shown in Fig. 10.51b.
- (c) Modify your model of part (a) to include this winding.

(d) The electrical equations for this circuit may be written in the form

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{22} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$

Use superposition to determine analytical expressions and numerical values for L_{11} , L_{12} , and L_{22} .

- 10.2** Two windings are placed as illustrated in Fig. 10.52a on a core of uniform cross-sectional area $A_c = 1 \text{ cm}^2$. Each winding has 50 turns. The relative permeability of the core is $\mu_r = 10^4$.

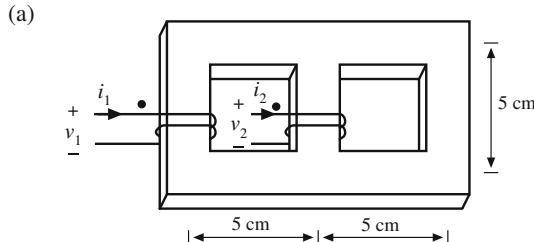
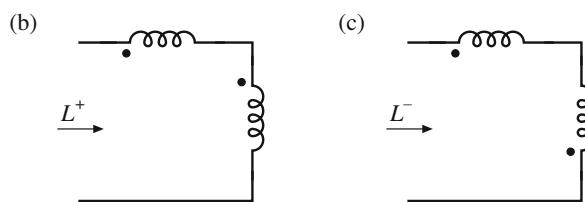


Fig. 10.52 Problem 10.2



- (a) Sketch an equivalent magnetic circuit, and determine numerical values for each reluctance.
- (b) Determine the self-inductance of each winding.
- (c) Determine the inductance L^+ obtained when the windings are connected in series as in Fig. 10.52b.
- (d) Determine the inductance L^- obtained when the windings are connected in anti-series as in Fig. 10.52c.

- 10.3** All three legs of the magnetic device illustrated in Fig. 10.53 are of uniform cross-sectional area A_C . Legs 1 and 2 each have magnetic path length 3ℓ , while leg 3 has magnetic path length ℓ . Both windings have n turns. The core has permeability $\mu \gg \mu_0$.

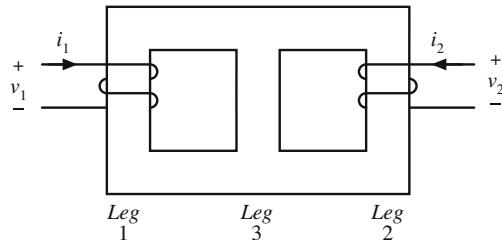


Fig. 10.53 Magnetic core for Problem 10.3

- (a) Sketch a magnetic equivalent circuit, and give analytical expressions for all element values. A voltage source is connected to winding 1, such that $v_1(t)$ is a square wave of peak value V_{max} and period T_s . Winding 2 is open-circuited.
- (b) Sketch $i_1(t)$ and label its peak value.
- (c) Find the flux $\varphi_2(t)$ in leg 2. Sketch $\varphi_2(t)$ and label its peak value.
- (d) Sketch $v_2(t)$ and label its peak value.
- 10.4** The magnetic device illustrated in Fig. 10.54a consists of two windings, which can replace the two inductors in a Ćuk, SEPIC, or other similar converter. For this problem, all three legs have the same uniform cross-sectional area A_c . The legs have gaps of lengths g_1 , g_2 , and g_3 , respectively. The core permeability μ is very large. You may neglect fringing flux. Legs 1 and 2 have windings containing n_1 and n_2 turns, respectively.

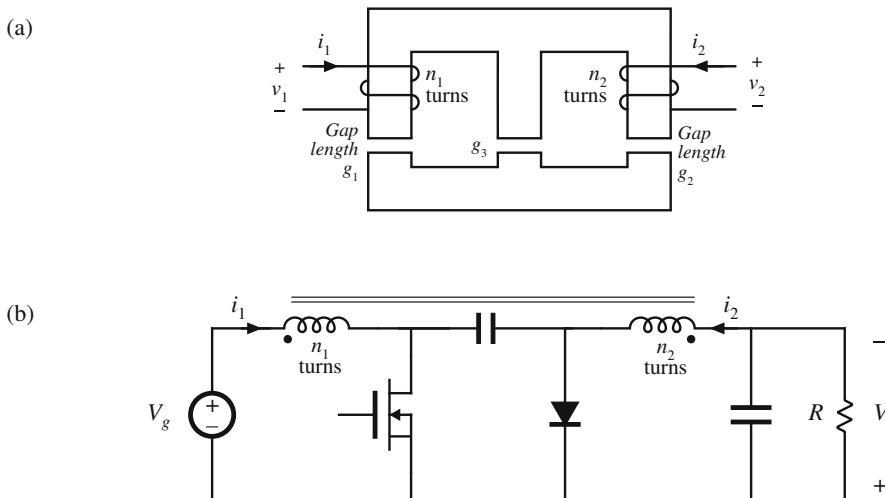


Fig. 10.54 Magnetic core and converter for Problem 10.4

- (a) Derive a magnetic circuit model for this device, and give analytical expressions for each reluctance in your model. Label the polarities of the MMF generators.
- (b) Write the electrical terminal equations of this device in the matrix form

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{22} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$

and derive analytical expressions for L_{11} , L_{12} , and L_{22} .

- (c) Derive an electrical circuit model for this device, and give analytical expressions for the turns ratio and each inductance in your model, in terms of the turns and reluctances of part (a).

This single magnetic device is to be used to realize the two inductors of the Ćuk converter, as in Fig. 10.54b.

- (d) Sketch the voltage waveforms $v_1(t)$ and $v_2(t)$, making the linear-ripple approximation as appropriate. You may assume that the converter operates in the continuous conduction mode.
- (e) The voltage waveforms of part (d) are applied to your model of parts (b) and (c). Solve your model to determine the slopes of the inductor current ripples during intervals DT_s and $D'T_s$. Sketch the steady-state inductor current waveforms $i_1(t)$ and $i_2(t)$, and label all slopes.
- (f) By skillful choice of n_1/n_2 and the air gap lengths, it is possible to make the inductor current ripple Δi in either $i_1(t)$ or $i_2(t)$ go to zero. Determine the conditions on n_1/n_2 , g_1 , g_2 , and g_3 that cause the current ripple in $i_2(t)$ to become zero. Sketch the resulting $i_1(t)$ and $i_2(t)$, and label all slopes.

It is possible to couple the inductors in this manner, and cause one of the inductor current ripples to go to zero, in any converter in which the inductor voltage waveforms are proportional.

- 10.5** Over its usable operating range, a certain permanent magnet material has the B - H characteristics illustrated by the solid line in Fig. 10.55. The magnet has length $\ell_m = 0.5$ cm, and cross-sectional area 4 cm^2 . $B_m = 1 \text{ T}$. Derive an equivalent magnetic circuit model for the magnet, and label the numerical values of the elements.

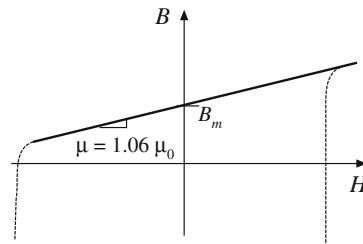


Fig. 10.55 B - H characteristic of the permanent magnet material for Problem 10.5

- 10.6** The two-transistor forward converter of Fig. 6.29 operates with $V_g = 300 \text{ V}$, $V = 28 \text{ V}$, switching frequency $f_s = 100 \text{ kHz}$, and turns ratio $n = 0.25$. The dc load power is 250 W. The transformer uses an EC41 ferrite core; relevant data for this core is listed in Appendix B. The core loss is given by Fig. 10.20. The primary winding consists of 44 turns of #21 AWG wire, and the secondary winding is composed of 11 turns of #15 AWG wire. Data regarding the American wire gauge is also listed in Appendix B. For this problem, you may assume that $\Delta B = B_{max}/2$, and you may neglect skin and proximity losses. You may assume that the magnetizing current and the output filter inductor current are very small.

- (a) Estimate the core loss of this transformer
 (b) Determine the copper loss of this transformer. You may neglect proximity losses.

- 10.7** The two-transistor forward converter of Fig. 6.29 operates in CCM with $V_g = 300 \text{ V}$, $V = 28 \text{ V}$, switching frequency $f_s = 100 \text{ kHz}$, and turns ratio $n = 0.25$. The dc load power is 250 W. The transformer uses an EC41 ferrite core; relevant data for this core is listed in Appendix B. This core has window height $\ell_w = 2.78 \text{ cm}$. The primary winding consists of 44 turns of #24 AWG wire, and the secondary winding is composed of 11 turns of #14 AWG wire. Each winding comprises one layer. Data regarding the American wire gauge is also listed in Appendix B. The winding operates at room temperature.

- (a) Determine the primary and secondary copper losses induced by the dc components of the winding currents.
 - (b) Determine the primary and secondary copper losses induced by the fundamental components of the winding currents.
 - (c) Determine the primary and secondary copper losses induced by the second harmonic components of the winding currents.
- 10.8** The winding currents of the transformer in a high-voltage inverter are essentially sinusoidal, with negligible harmonics and no dc components. The primary winding consists of one layer containing 10 turns of round copper wire. The secondary winding consists of 250 turns of round copper wire, arranged in ten layers. The operating frequency is $f = 50 \text{ kHz}$, and the winding porosity is 0.8. Determine the primary and secondary wire diameters and wire gauges that minimize the total copper loss.
- 10.9** A certain three-winding transformer contains one primary and two secondaries. The operating frequency is 40 kHz. The primary winding contains a total of 60 turns of #26 AWG, arranged in three layers. The secondary windings each consist of five turns of copper foil, one turn per layer. The foil thickness is 0.25 mm. The primary layers have porosity 0.8, while the secondary layer porosity is 1. The primary winding carries a sinusoidal current having rms value I , while each secondary carries rms current $6I$. The windings are not interleaved: the primary winding is closest to the center leg of the core, followed by secondary winding #1, followed by secondary winding #2.
- (a) Sketch an MMF diagram illustrating the magnetic fields in the vicinity of each winding layer.
 - (b) Determine the increased copper loss, due to the proximity effect, in each layer.
 - (c) Determine the ratio of copper loss to dc copper loss, F_R , for the entire transformer windings.
 - (d) In this application, it is not feasible to interleave the primary winding with the other windings. However, changing the conductor size is permissible. Discuss how the windings could be better optimized.
- 10.10** A transformer winding contains a four-layer primary winding, and two two-layer secondary windings. Each layer of the primary winding carries total current I . Each layer of secondary winding #1 carries total current $1.5I$. Each layer of secondary winding #2 carries total current $0.5I$. All currents are sinusoidal. The effective relative conductor thickness is $\varphi = 2$. The windings are partially interleaved, in the following order: two primary layers, followed by both layers of secondary #1, followed by both layers of secondary #2, and finally the two remaining primary layers. You may assume that the core has negligible reluctance.
- (a) Sketch an MMF diagram for this winding arrangement.
 - (b) Each primary layer has dc resistance R_{dc-p} , and each secondary layer has dc resistance R_{dc-s} . Determine the increased copper loss, due to the proximity effect, for each layer.
 - (c) Determine the increase in total transformer copper loss, due to the proximity effect.
- 10.11** A transformer is connected to a voltage source and a load as illustrated in Fig. 10.56. The primary winding is excited by the voltage $v_1(t)$ whose waveform is illustrated in Fig. 10.57. The switching frequency is $f_s = 1/T_s = 200 \text{ kHz}$, and the duty cycle is $D = 1/3$. The load current is a 200 kHz sinusoid having amplitude 5 A rms.

Fig. 10.56 Transformer circuit of Problem 10.11

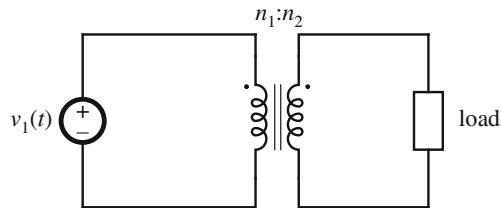
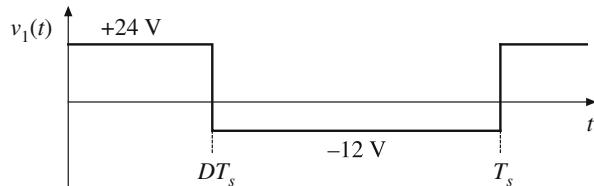
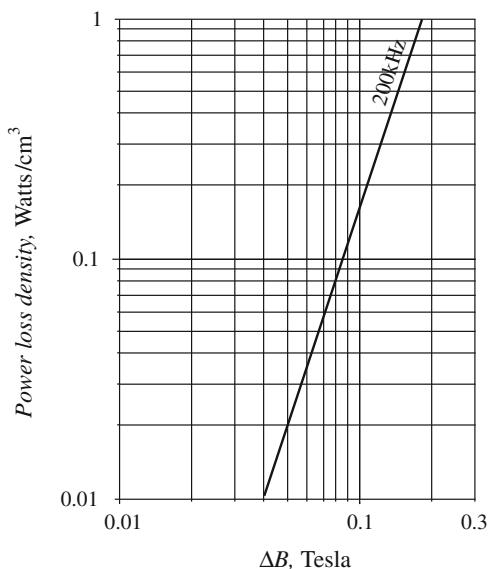


Fig. 10.57 Primary voltage waveform $v_1(t)$ for Problem 10.11



The transformer consists of a ferrite PQ 26/25 core, with flat copper (ribbon) windings. The primary winding consists of two turns of flat copper of rectangular cross-section, with a copper width of 1.25 cm and a copper thickness of 0.07 cm. The secondary winding consists of eight turns of flat copper also of rectangular cross-section, with a copper width of 1.25 cm and a copper thickness of 0.017 cm. Each turn comprises one layer in the winding. You may assume that the transformer operates at a temperature of 100°C. The core loss data for this core operating at 200 kHz is plotted in Fig. 10.58.

Fig. 10.58 Core loss vs. peak ac flux density for Problem 10.11



The primary and secondary windings are interleaved as follows:

- Three layers of secondary
- One layer of primary
- Two layers of secondary

- One layer of primary
- Three layers of secondary
- (a) Find the peak ac flux density ΔB and the core loss P_{fe} for this transformer.
- (b) Find the dc resistance R_{dc} and φ for each layer.
- (c) Sketch the MMF diagram for this transformer, and find the effective m for each layer.
- (d) Compute the total power loss in each layer, and the total transformer loss, in Watts.

10.12 The windings in the transformer shown in Fig. 10.59 are realized using copper foil layers arranged as shown in Fig. 10.60. The primary has two turns, each consisting of a layer of copper foil carrying high-frequency sinusoidal current $2i$. The secondary has four turns,

Fig. 10.59 Transformer of Problem 10.12

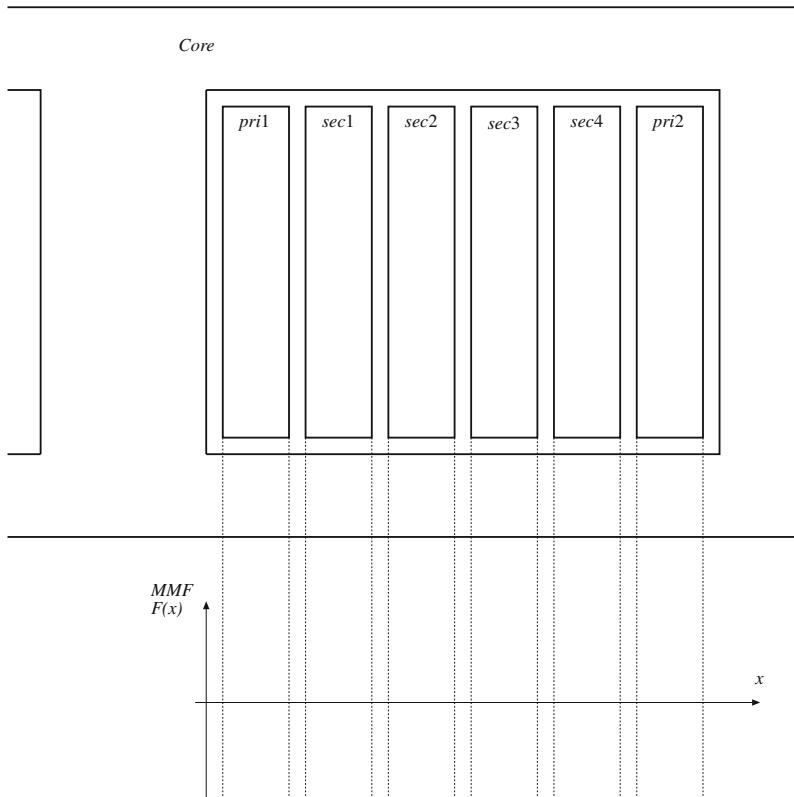
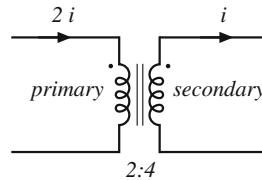


Fig. 10.60 MMF diagram for a simple transformer with interleaved windings. Each layer operates with $m = 1$

each consisting of a layer of copper foil carrying current i . The foil thickness is much greater than the penetration depth δ , i.e., $\varphi \gg 1$. The windings are partially interleaved as illustrated in Fig. 10.60. The copper loss due to a current i through a copper layer of thickness δ is equal to P .

- (a) Sketch the current distribution in the layers, and the MMF diagram for this winding arrangement.
- (b) Find the total copper loss in the transformer, in terms of P .
- (c) It is desired to rearrange the winding layers to minimize the total copper loss. Sketch how the layers should be arranged, sketch the corresponding MMF diagram, and compute the total loss in terms of P .

- 10.13** A single-output forward converter contains a transformer having a noninterleaved secondary winding with four layers. The converter operates at $D = 0.3$ in CCM, with a secondary winding current waveform similar to Fig. 10.38.
- (a) Estimate the value of φ_1 that minimizes the secondary winding copper losses.
 - (b) Determine the resulting secondary copper loss, relative to $I_{rms}^2 R_{dc}$.

- 10.14** A schematic diagram and waveforms of the isolated SEPIC, operating in CCM, are given in Figs. 6.39 and 6.40.
- (a) Do you expect the SEPIC transformer to contain an air gap? Why or why not?
 - (b) Sketch the SEPIC transformer B - H loop, for CCM operation.
 - (c) For CCM operation, do you expect core loss to be significant? Explain your reasoning.
 - (d) For CCM operation, do you expect winding proximity losses to be significant? Explain your reasoning.



Inductor Design

This chapter treats the design of magnetic elements such as filter inductors, using the geometrical constant (K_g) method. With this method, the maximum flux density B_{max} is specified in advance, and the element is designed to attain a given copper loss.

The design of a basic filter inductor is discussed in Sects. 11.1 and 11.1.5. In the filter inductor application, it is necessary to obtain the required inductance, avoid saturation, and obtain an acceptable low dc winding resistance and copper loss. The geometrical constant K_g is a measure of the effective magnetic size of a core, when dc copper loss and winding resistance are the dominant constraints [4, 99]. Design of a filter inductor involves selection of a core having a K_g sufficiently large for the application, then computing the required air gap, turns, and wire size. A first-pass filter inductor design procedure is given. Values of K_g for common ferrite core shapes are tabulated in Appendix B. In practice, the K_g method might be employed to find a starting estimate of an inductor design. Details of the winding geometry would be examined, and all losses computed. Design iterations can then further optimize the design.

Extension of the K_g method to multiple-winding elements is covered in Sect. 11.3. In applications requiring multiple windings, it is necessary to optimize the wire sizes of the windings so that the overall copper loss is minimized. It is also necessary to write an equation that relates the peak flux density to the applied waveforms or to the desired winding inductance. Again, a simple step-by-step transformer design approach is given.

The goal of the K_g approach of this chapter is the design of a magnetic device having a given copper loss. Core loss is not specifically addressed in the K_g approach, and B_{max} is a given fixed value. In the next chapter, the flux density is treated as a design variable to be optimized. This allows the overall loss (i.e., core loss plus copper loss) to be minimized.

11.1 Filter Inductor Design Constraints

A filter inductor employed in a CCM buck converter is illustrated in Fig. 11.1a. In this application, the value of inductance L is usually chosen such that the inductor current ripple peak magnitude Δi is a small fraction of the full-load inductor current dc component I , as illustrated in Fig. 11.1b. As illustrated in Fig. 11.2, an air gap is employed that is sufficiently large to prevent saturation of the core by the peak current $I + \Delta i$.

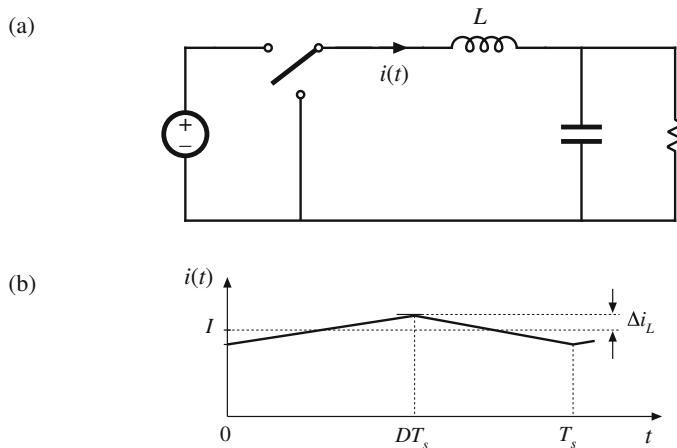


Fig. 11.1 Filter inductor employed in a CCM buck converter: (a) circuit schematic, (b) inductor current waveform

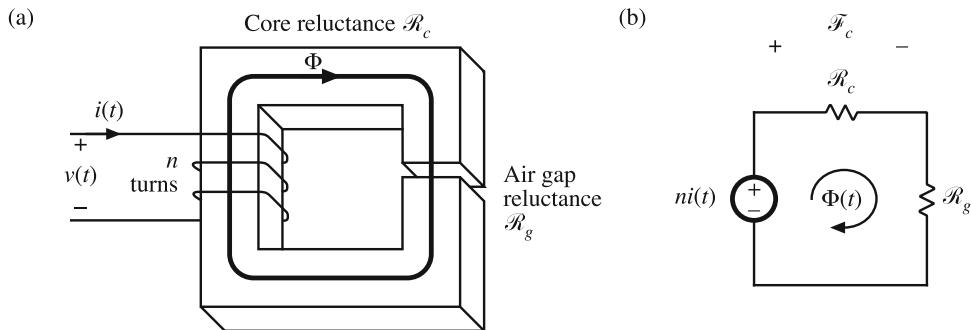


Fig. 11.2 Filter inductor: (a) structure, (b) magnetic circuit model

Let us consider the design of the filter inductor illustrated in Figs. 11.1 and 11.2. It is assumed that the core and proximity losses are negligible, so that the inductor losses are dominated by the low-frequency copper losses. The inductor can therefore be modeled by the equivalent circuit of Fig. 11.3, in which R represents the dc resistance of the winding. It is desired to obtain a given inductance L and given winding resistance R . The inductor should not saturate when a given worst-case peak current I_{max} is applied. Note that specification of R is equivalent to specification of the copper loss P_{cu} , since

$$P_{cu} = I_{rms}^2 R \quad (11.1)$$

The influence of inductor winding resistance on converter efficiency and output voltage is modeled in Chap. 3.

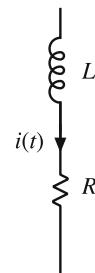


Fig. 11.3 Filter inductor equivalent circuit

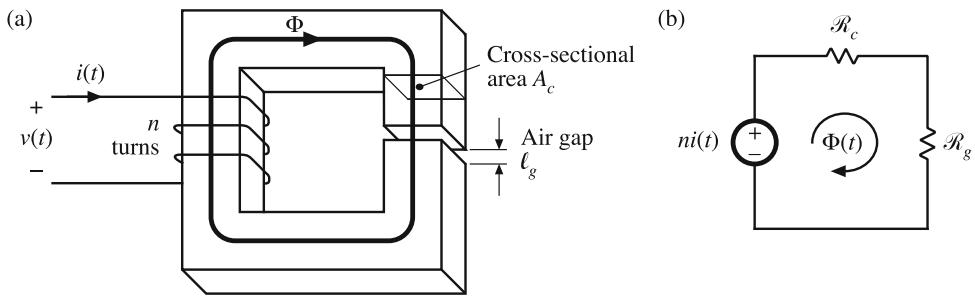


Fig. 11.4 Filter inductor: (a) assumed geometry, (b) magnetic circuit

It is assumed that the inductor geometry is topologically equivalent to Fig. 11.4a. An equivalent magnetic circuit is illustrated in Fig. 11.4b. The core reluctance \mathcal{R}_c and air gap reluctance \mathcal{R}_g are

$$\begin{aligned}\mathcal{R}_c &= \frac{\ell_c}{\mu_c A_c} \\ \mathcal{R}_g &= \frac{\ell_g}{\mu_0 A_c}\end{aligned}\quad (11.2)$$

where ℓ_c is the core magnetic path length, A_c is the core cross-sectional area, μ_c is the core permeability, and ℓ_g is the air gap length. It is assumed that the core and air gap have the same cross-sectional areas. Solution of Fig. 11.4b yields

$$ni = \Phi(\mathcal{R}_c + \mathcal{R}_g) \quad (11.3)$$

Usually, $\mathcal{R}_c \ll \mathcal{R}_g$, and hence Eq. (11.3) can be approximated as

$$ni \approx \Phi \mathcal{R}_g \quad (11.4)$$

The air gap dominates the inductor properties. Four design constraints now can be identified.

11.1.1 Maximum Flux Density

Given a peak winding current I_{max} , it is desired to operate the core flux density at a maximum value B_{max} . The value of B_{max} is chosen to be less than the worst-case saturation flux density B_{sat} of the core material.

Substitution of $\Phi = BA_c$ into Eq. (11.4) leads to

$$ni = BA_c \mathcal{R}_g \quad (11.5)$$

Upon letting $I = I_{max}$ and $B = B_{max}$, we obtain

$$nI_{max} = B_{max}A_c \mathcal{R}_g = B_{max} \frac{\ell_g}{\mu_0} \quad (11.6)$$

This is the first design constraint. The turns ratio n and the air gap length ℓ_g are unknowns.

11.1.2 Inductance

The given inductance value L must be obtained. The inductance is equal to

$$L = \frac{n^2}{\mathcal{R}_g} = \frac{\mu_0 A_c n^2}{\ell_g} \quad (11.7)$$

This is the second design constraint. The turns ratio n , core area A_c , and gap length ℓ_g are unknown.

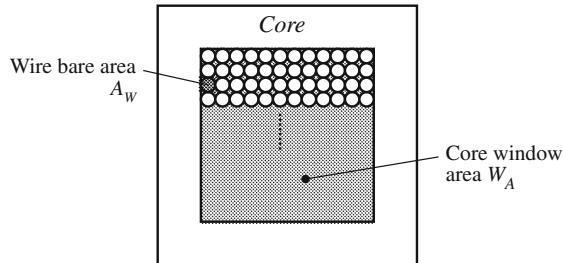


Fig. 11.5 The winding must fit in the core window area

11.1.3 Winding Area

As illustrated in Fig. 11.5, the winding must fit through the window, i.e., the hole in the center of the core. The cross-sectional area of the conductor, or bare area, is A_W . If the winding has n turns, then the area of copper conductor in the window is

$$nA_W \quad (11.8)$$

If the core has window area W_A , then we can express the area available for the winding conductors as

$$K_u W_A \quad (11.9)$$

where K_u is the *window utilization factor*, or *fill factor*. Hence, the third design constraint can be expressed as

$$K_u W_A \geq nA_W \quad (11.10)$$

The fill factor K_u is the fraction of the core window area that is filled with copper. K_u must lie between zero and one. As discussed in [99], there are several mechanism that cause K_u to be less than unity. Round wire does not pack perfectly; this reduces K_u by a factor of 0.7 to 0.55, depending on the winding technique. The wire has insulation; the ratio of wire conductor area to total wire area varies from approximately 0.95 to 0.65, depending on the wire size and type of insulation. The bobbin uses some of the window area. Insulation may be required between windings and/or winding layers. Typical values of K_u for cores with winding bobbins are 0.5 for a simple low-voltage inductor, 0.25 to 0.3 for an off-line transformer, 0.05 to 0.2 for a high-voltage transformer supplying several kV, and 0.65 for a low-voltage foil transformer or inductor.

11.1.4 Winding Resistance

The resistance of the winding is

$$R = \rho \frac{\ell_b}{A_W} \quad (11.11)$$

where ρ is the resistivity of the conductor material, ℓ_b is the length of the wire, and A_W is the wire bare area. The resistivity of copper at room temperature is $1.724 \cdot 10^{-6} \Omega\text{-cm}$. The length of the wire comprising an n -turn winding can be expressed as

$$\ell_b = n(MLT) \quad (11.12)$$

where (MLT) is the mean-length-per-turn of the winding. The mean-length-per-turn is a function of the core geometry. Substitution of Eq. (11.12) into (11.11) leads to

$$R = \rho \frac{n(MLT)}{A_W} \quad (11.13)$$

This is the fourth constraint.

11.1.5 The Core Geometrical Constant K_g

The four constraints, Eqs. (11.6), (11.7), (11.10), and (11.13), involve the quantities A_c , W_A , and MLT , which are functions of the core geometry, the quantities I_{max} , B_{max} , μ_0 , L , K_u , R , and ρ , which are given specifications or other known quantities, and n , ℓ_g , and A_W , which are unknowns. Elimination of the unknowns n , ℓ_g , and A_W leads to the following equation:

$$\frac{A_c^2 W_A}{(MLT)} \geq \frac{\rho L^2 I_{max}^2}{B_{max}^2 R K_u} \quad (11.14)$$

The quantities on the right side of this equation are specifications or other known quantities. The left side of the equation is a function of the core geometry alone. It is necessary to choose a core whose geometry satisfies Eq. (11.14).

The quantity

$$K_g = \frac{A_c^2 W_A}{(MLT)} \quad (11.15)$$

is called the core geometrical constant. It is a figure-of-merit that describes the effective electrical size of magnetic cores, in applications where copper loss and maximum flux density are specified. Tables are included in Appendix B that lists the values of K_g for several standard families of ferrite cores. K_g has dimensions of length to the fifth power.

Equation (11.14) reveals how the specifications affect the core size. Increasing the inductance or peak current requires an increase in core size. Increasing the peak flux density allows a decrease in core size, and hence it is advantageous to use a core material that exhibits a high saturation flux density. Allowing a larger winding resistance R , and hence larger copper loss, leads to a smaller core. Of course, the increased copper loss and smaller core size will lead to a higher temperature rise, which may be unacceptable. The fill factor K_u also influences the core size.

Equation (11.15) reveals how core geometry affects the core capabilities. An inductor capable of meeting increased electrical requirements can be obtained by increasing either the core

area A_c , or the window area W_A . Increase of the core area requires additional iron core material. Increase of the window area implies that additional copper winding material is employed. We can trade iron for copper, or vice versa, by changing the core geometry in a way that maintains the K_g of Eq. (11.15).

11.2 The K_g Method: A First-Pass Design

The procedure developed in Sect. 11.1 is summarized below. This simple filter inductor design procedure should be regarded as a first-pass approach. Numerous issues have been neglected, including detailed insulation requirements, conductor eddy current losses, temperature rise, roundoff of number of turns, etc.

The following quantities are specified, using the units noted:

Wire resistivity	ρ	($\Omega\text{-cm}$)
Peak winding current	I_{max}	(A)
Inductance	L	(H)
Winding resistance	R	(Ω)
Winding fill factor	K_u	
Maximum operating flux density	B_{max}	(T)

The core dimensions are expressed in cm:

Core cross-sectional area	A_c	(cm^2)
Core window area	W_A	(cm^2)
Mean length per turn	MLT	(cm)

The use of centimeters rather than meters requires that appropriate factors be added to the design equations.

1. Determine core size

$$K_g \geq \frac{\rho L^2 I_{max}^2}{B_{max}^2 R K_u} 10^8 \quad (\text{cm}^5) \quad (11.16)$$

Choose a core which is large enough to satisfy this inequality. Note the values of A_c , W_A , and MLT for this core. The resistivity ρ of copper wire is $1.724 \cdot 10^{-6} \Omega\text{-cm}$ at room temperature, and $2.3 \cdot 10^{-6} \Omega\text{-cm}$ at 100°C .

2. Determine number of turns

$$n = \frac{LI_{max}}{B_{max}A_c} 10^4 \quad (11.17)$$

with A_c expressed in cm^2 and B_{max} expressed in T.

3. Determine air gap length

$$\ell_g = \frac{\mu_0 A_c n^2}{L} 10^{-4} \quad (\text{m}) \quad (11.18)$$

with A_c expressed in cm^2 . The permeability of free space is $\mu_0 = 4\pi \cdot 10^{-7} \text{ H/m}$. The air gap length is given in meters. The value expressed in Eq. (11.18) is approximate, and neglects fringing flux and other nonidealities. Generally fringing flux increases the inductance, and hence a somewhat longer gap would be needed to achieve the specified inductance.

Core manufacturers sell gapped cores. Rather than specifying the air gap length, the equivalent quantity A_L is used. A_L is equal to the inductance, in mH, obtained with a winding of 1000 turns. When A_L is specified, it is the core manufacturer's responsibility to obtain the correct gap length. Equation (11.18) can be modified to yield the required A_L , as follows:

$$A_L = \frac{10B_{max}^2 A_c^2}{LI_{max}^2} \quad (\text{mH}/1000 \text{ turns}) \quad (11.19)$$

where A_c is given in cm^2 , L is given in Henries, and B_{max} is given in Tesla.

4. Evaluate wire size

$$A_W \leq \frac{K_u W_A}{n} \quad (\text{cm}^2) \quad (11.20)$$

Select wire with bare copper area less than or equal to this value. An American Wire Gauge table is included in Appendix B.

As a check, the winding resistance can be computed:

$$R = \frac{\rho n(MLT)}{A_w} \quad (\Omega) \quad (11.21)$$

11.3 Multiple-Winding Magnetics Design via the K_g Method

The K_g method can be extended to the case of multiple-winding magnetics, such as the transformers and coupled inductors described in Sects. 10.5.3 to 10.5.5. The desired turns ratios, as well as the desired winding voltage and current waveforms, are specified. In the case of a coupled inductor or flyback transformer, the magnetizing inductance is also specified. It is desired to select a core size, number of turns for each winding, and wire sizes. It is also assumed that the maximum flux density B_{max} is given.

With the K_g method, a desired copper loss is attained. In the multiple-winding case, each winding contributes some copper loss, and it is necessary to allocate the available window area among the various windings. In Sect. 11.3.1 below, it is found that total copper loss is minimized if the window area is divided between the windings according to their apparent powers. This result is employed in the following sections, in which an optimized K_g method for coupled inductor design is developed.

11.3.1 Window Area Allocation

The first issue to settle in design of a multiple-winding magnetic device is the allocation of the window area A_W among the various windings. It is desired to design a device having k windings with turns ratios $n_1 : n_2 : \dots : n_k$. These windings must conduct rms currents I_1, I_2, \dots, I_k respectively. It should be noted that the windings are effectively in parallel: the winding voltages are ideally related by the turns ratios

$$\frac{v_1(t)}{n_1} = \frac{v_2(t)}{n_2} = \dots = \frac{v_k(t)}{n_k} \quad (11.22)$$

However, the winding rms currents are determined by the loads, and in general are not related to the turns ratios. The device is represented schematically in Fig. 11.6.

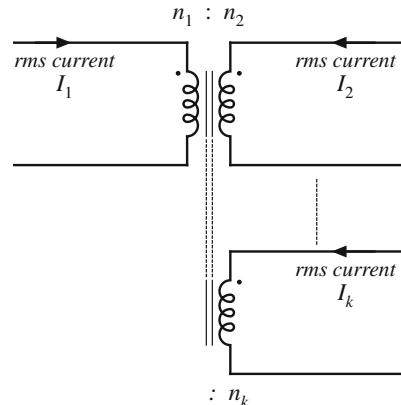


Fig. 11.6 It is desired to optimally allocate the window area of a k -winding magnetic element to minimize low-frequency copper losses, with given rms winding currents and turns ratios

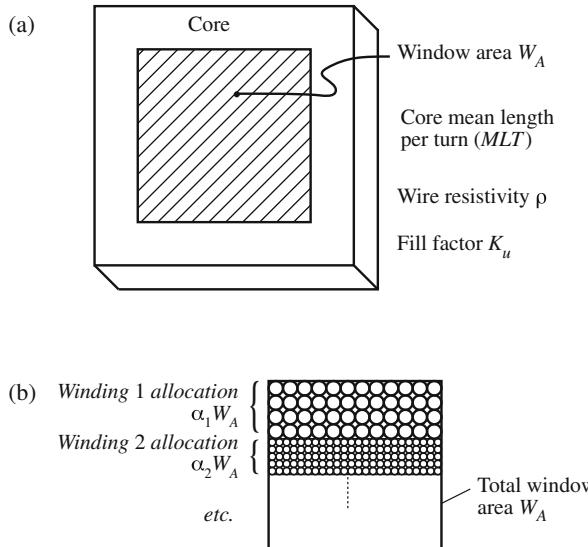


Fig. 11.7 Basic core topology, including window area W_A enclosed by core (a). The window is allocated to the various windings (b) to minimize low-frequency copper loss

The relevant geometrical parameters are summarized in Fig. 11.7a. It is necessary to allocate a portion of the total window area W_A to each winding, as illustrated in Fig. 11.7b. Let α_j be the fraction of the window area allocated to winding j , where

$$\begin{aligned} 0 < \alpha_j < 1 \\ \alpha_1 + \alpha_2 + \dots + \alpha_k = 1 \end{aligned} \quad (11.23)$$

The low-frequency copper loss $P_{cu,j}$ in winding j depends on the dc resistance R_j of winding j , as follows:

$$P_{cu,j} = I_j^2 R_j \quad (11.24)$$

The resistance of winding j is

$$R_j = \rho \frac{\ell_j}{A_{W,j}} \quad (11.25)$$

where ρ is the wire resistivity, ℓ_j is the length of the wire used for winding j , and $A_{W,j}$ is the cross-sectional area of the wire used for winding j . These quantities can be expressed as

$$\ell_j = n_j(MLT) \quad (11.26)$$

$$A_{W,j} = \frac{W_A K_u \alpha_j}{n_j} \quad (11.27)$$

where (MLT) is the winding mean-length-per-turn, and K_u is the winding fill factor. Substitution of these expressions into Eq. (11.25) leads to

$$R_j = \rho \frac{n_j^2(MLT)}{W_A K_u \alpha_j} \quad (11.28)$$

The copper loss of winding j is therefore

$$P_{cu,j} = \frac{n_j^2 i_j^2 \rho(MLT)}{W_A K_u \alpha_j} \quad (11.29)$$

The total copper loss of the k windings is

$$P_{cu,tot} = P_{cu,1} + P_{cu,2} + \dots + P_{cu,k} = \frac{\rho(MLT)}{W_A K_u} \sum_{j=1}^k \left(\frac{n_j^2 I_j^2}{\alpha_j} \right) \quad (11.30)$$

It is desired to choose the α_j s such that the total copper loss $P_{cu,tot}$ is minimized. Let us consider what happens when we vary one of the α s, say α_1 , between 0 and 1.

When $\alpha_1 = 0$, then we allocate zero area to winding 1. In consequence, the resistance of winding 1 tends to infinity. The copper loss of winding 1 also tends to infinity. On the other hand, the other windings are given maximum area, and hence their copper losses can be reduced. Nonetheless, the total copper loss tends to infinity.

When $\alpha_1 = 1$, then we allocate all of the window area to winding 1, and none to the other windings. Hence, the resistance of winding 1, as well as its low-frequency copper loss, is minimized. But the copper losses of the remaining windings tend to infinity.

As illustrated in Fig. 11.8, there must be an optimum value of α_1 that lies between these two extremes, where the total copper loss is minimized. Let us compute the optimum values of $\alpha_1, \alpha_2, \dots, \alpha_k$ using the method of Lagrange multipliers. It is desired to minimize Eq. (11.30), subject to the constraint of Eq. (11.23). Hence, we define the function

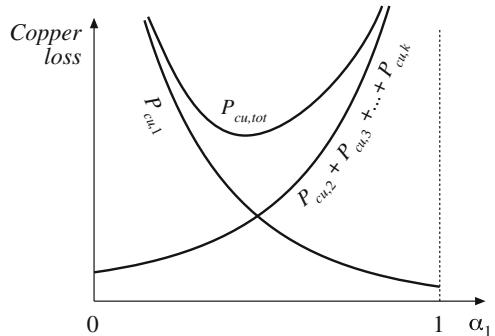


Fig. 11.8 Variation of copper losses with α_1

$$f(\alpha_1, \alpha_2, \dots, \alpha_k, \xi) = P_{cu,tot}(\alpha_1, \alpha_2, \dots, \alpha_k) + \xi g(\alpha_1, \alpha_2, \dots, \alpha_k) \quad (11.31)$$

where

$$g(\alpha_1, \alpha_2, \dots, \alpha_k) = 1 - \sum_{j=1}^k \alpha_j \quad (11.32)$$

is the constraint that must equal zero, and ξ is the Lagrange multiplier. The optimum point is the solution of the system of equations

$$\begin{aligned} \frac{\partial f(\alpha_1, \alpha_2, \dots, \alpha_k, \xi)}{\partial \alpha_1} &= 0 \\ \frac{\partial f(\alpha_1, \alpha_2, \dots, \alpha_k, \xi)}{\partial \alpha_2} &= 0 \\ &\vdots \\ \frac{\partial f(\alpha_1, \alpha_2, \dots, \alpha_k, \xi)}{\partial \alpha_k} &= 0 \\ \frac{\partial f(\alpha_1, \alpha_2, \dots, \alpha_k, \xi)}{\partial \xi} &= 0 \end{aligned} \quad (11.33)$$

The solution is

$$\xi = \frac{\rho(MLT)}{W_A K_u} \left(\sum_{j=1}^k n_j I_j \right)^2 = P_{cu,tot} \quad (11.34)$$

$$\alpha_m = \frac{n_m I_m}{\sum_{j=1}^k n_j I_j} \quad (11.35)$$

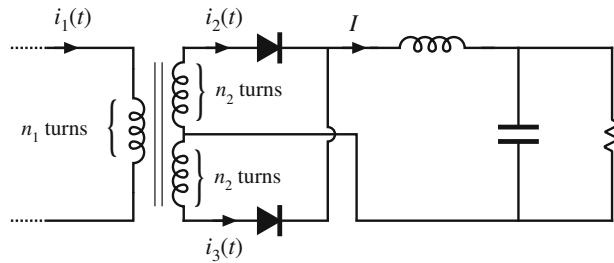
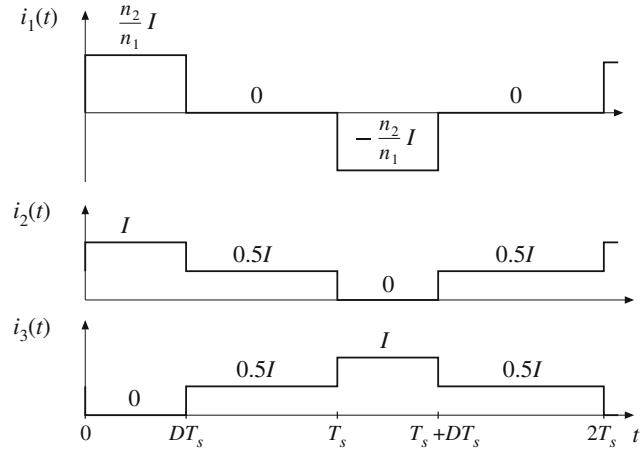
This is the optimal choice for the α s, and the resulting minimum value of $P_{cu,tot}$.

According to Eq. (11.22), the winding voltages are proportional to the turns ratios. Hence, we can express the α_m s in the alternate form

$$\alpha_m = \frac{V_m I_m}{\sum_{j=1}^k V_j I_j} \quad (11.36)$$

by multiplying and dividing Eq. (11.35) by the quantity V_m/n_m . It is irrelevant whether rms or peak voltages are used. Equation (11.36) is the desired result. It states that the window area should be allocated to the various windings in proportion to their apparent powers. The numerator of Eq. (11.36) is the apparent power of winding m , equal to the product of the rms current and the voltage. The denominator is the sum of the apparent powers of all windings.

As an example, consider the PWM full-bridge transformer having a center-tapped secondary, as illustrated in Fig. 11.9. This can be viewed as a three-winding transformer, having a single primary-side winding of n_1 turns, and two secondary-side windings, each of n_2 turns. The winding current waveforms $i_1(t)$, $i_2(t)$, and $i_3(t)$ are illustrated in Fig. 11.10. Their rms values are

**Fig. 11.9** PWM full-bridge transformer example**Fig. 11.10** Transformer waveforms, PWM full-bridge transformer example

$$I_1 = \sqrt{\frac{1}{2T_s} \int_0^{2T_s} i_1^2(t) dt} = \frac{n_2}{n_1} I \sqrt{D} \quad (11.37)$$

$$I_2 = I_3 = \sqrt{\frac{1}{2T_s} \int_0^{2T_s} i_2^2(t) dt} = \frac{1}{2} I \sqrt{1+D} \quad (11.38)$$

Substitution of these expressions into Eq. (11.35) yields

$$\alpha_1 = \frac{1}{\left(1 + \sqrt{\frac{1+D}{D}}\right)} \quad (11.39)$$

$$\alpha_2 = \alpha_3 = \frac{1}{2} \frac{1}{\left(1 + \sqrt{\frac{D}{1+D}}\right)} \quad (11.40)$$

If the design is to be optimized at the operating point $D = 0.75$, then one obtains

$$\begin{aligned} \alpha_1 &= 0.396 \\ \alpha_2 &= 0.302 \\ \alpha_3 &= 0.302 \end{aligned} \quad (11.41)$$

So approximately 40% of the window area should be allocated to the primary winding, and 30% should be allocated to each half of the center-tapped secondary. The total copper loss at this optimal design point is found from evaluation of Eq. (11.34):

$$\begin{aligned} P_{cu,tot} &= \frac{\rho(MLT)}{W_A K_u} \left(\sum_{j=1}^3 n_j I_j \right)^2 \\ &= \frac{\rho(MLT) n_2^2 I^2}{W_A K_u} \left(1 + 2D + 2\sqrt{D(1+D)} \right) \end{aligned} \quad (11.42)$$

11.3.2 Coupled Inductor Design Constraints

Let us now consider how to design a k -winding coupled inductor, as discussed in Sect. 10.5.4 and illustrated in Fig. 11.11. It is desired that the magnetizing inductance be a specified value L_M , referred to winding 1. It is also desired that the numbers of turns for the other windings be chosen according to desired turns ratios. When the magnetizing current $i_M(t)$ reaches its maximum value $I_{M,max}$, the coupled inductor should operate with a given maximum flux density B_{max} . With rms currents I_1, I_2, \dots, I_k applied to the respective windings, the total copper loss should be a desired value P_{cu} given by Eq. (11.34). Hence, the design procedure involves selecting the core size and number of primary turns so that the desired magnetizing inductance, the desired flux density, and the desired total copper loss are achieved. Other quantities, such as air gap length, secondary turns, and wire sizes, can then be selected. The derivation follows the derivation for the single-winding case (Sect. 11.1), and incorporates the window area optimization of Sect. 11.3.1.

The magnetizing current $i_M(t)$ can be expressed in terms of the winding currents $i_1(t), i_2(t), \dots, i_k(t)$ by solution of Fig. 11.11a (or by use of Ampere's Law), as follows:

$$i_M(t) = i_1(t) + \frac{n_2}{n_1} i_2(t) + \dots + \frac{n_k}{n_1} i_k(t) \quad (11.43)$$

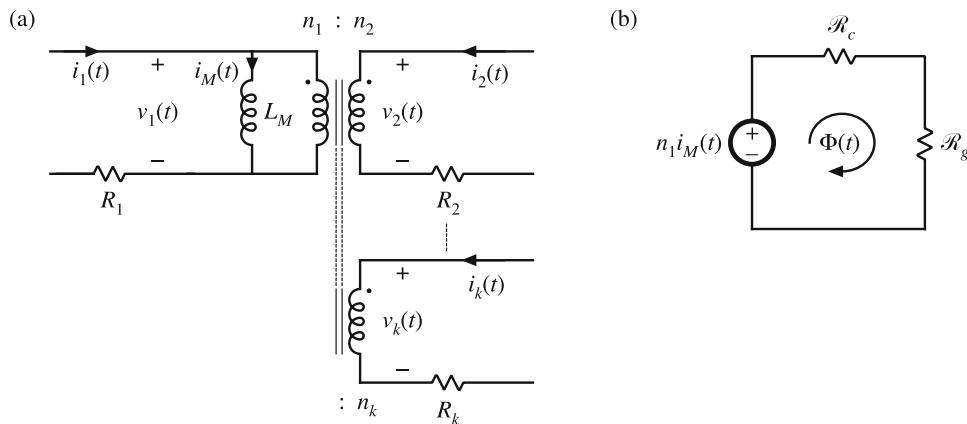


Fig. 11.11 A k -winding magnetic device, with specified turns ratios and waveforms: (a) electrical circuit model, (b) magnetic circuit model

By solution of the magnetic circuit model of Fig. 11.11b, we can write

$$n_1 i_M(t) = B(t) A_c \cdot \mathcal{R}_g \quad (11.44)$$

This equation is analogous to Eq. (11.4), and assumes that the reluctance \mathcal{R}_g of the air gap is much larger than the reluctance \mathcal{R}_c of the core. As usual, the total flux $\Phi(t)$ is equal to $B(t)A_c$. Leakage inductances are ignored.

To avoid saturation of the core, the instantaneous flux density $B(t)$ must be less than the saturation flux density of the core material, B_{sat} . Let us define $I_{M,max}$ as the maximum value of the magnetizing current $i_M(t)$. According to Eq. (11.44), this will lead to a maximum flux density B_{max} given by

$$n_1 I_{M,max} = B_{max} A_c \cdot \mathcal{R}_g = B_{max} \frac{\ell_g}{\mu_0} \quad (11.45)$$

For a value of $I_{M,max}$ given by the circuit application, we should use Eq. (11.45) to choose the turns n_1 and gap length ℓ_g such that the maximum flux density B_{max} is less than the saturation density B_{sat} . Equation (11.45) is similar to Eq. (11.6), but accounts for the magnetizations produced by multiple-winding currents.

The magnetizing inductance L_M , referred to winding 1, is equal to

$$L_M = \frac{n_1^2}{\mathcal{R}_g} = n_1^2 \frac{\mu_0 A_c}{\ell_g} \quad (11.46)$$

This equation is analogous to Eq. (11.7).

As shown in Sect. 11.3.1, the total copper loss is minimized when the core window area W_A is allocated to the various windings according to Eq. (11.35) or (11.36). The total copper loss is then given by Eq. (11.34). Equation (11.34) can be expressed in the form

$$P_{cu} = \frac{\rho(MLT)n_1^2 I_{tot}^2}{W_A K_u} \quad (11.47)$$

where

$$I_{tot} = \sum_{j=1}^k \frac{n_j}{n_1} I_j \quad (11.48)$$

is the sum of the rms winding currents, referred to winding 1.

We can now eliminate the unknown quantities ℓ_g and n_1 from Eqs. (11.45), (11.46), and (11.47). Equation (11.47) then becomes

$$P_{cu} = \frac{\rho(MLT)L_M^2 I_{tot}^2 I_{M,max}^2}{B_{max}^2 A_c^2 W_A K_u} \quad (11.49)$$

We can now rearrange this equation, by grouping terms that involve the core geometry on the left-hand side, and specifications on the right-hand side:

$$\frac{A_c^2 W_A}{(MLT)} = \frac{\rho L_M^2 I_{tot}^2 I_{M,max}^2}{B_{max}^2 K_u P_{cu}} \quad (11.50)$$

The left-hand side of the equation can be recognized as the same K_g term defined in Eq. (11.15). Therefore, to design a coupled inductor that meets the requirements of operating with a given

maximum flux density B_{max} , given primary magnetizing inductance L_M , and with a given total copper loss P_{cu} , we must select a core that satisfies

$$K_g \geq \frac{\rho L_M^2 I_{tot}^2 I_{M,max}^2}{B_{max}^2 K_u P_{cu}} \quad (11.51)$$

Once such a core is found, then the winding 1 turns and gap length can be selected to satisfy Eqs. (11.45) and (11.46). The turns of windings 2 through k are selected according to the desired turns ratios. The window area is allocated among the windings according to Eq. (11.35), and the wire gauges are chosen using Eq. (11.27).

The procedure above is applicable to design of coupled inductors. The results are applicable to design of flyback and SEPIC transformers as well, although it should be noted that the procedure does not account for the effects of core or proximity loss. It also can be extended to design of other devices, such as conventional transformers—doing so is left as a homework problem.

11.3.3 First-Pass Design Procedure

The following quantities are specified, using the units noted:

Wire effective resistivity	ρ	($\Omega \cdot \text{cm}$)
Total rms winding currents, referred to winding 1	$I_{tot} = \sum_{j=1}^k \frac{n_j}{n_i} I_j$	(A)
Peak magnetizing current, referred to winding 1	$I_{M,max}$	(A)
Desired turns ratios	$n_2/n_1, n_3/n_1, \text{etc.}$	
Magnetizing inductance, referred to winding 1	L_M	(H)
Allowed total copper loss	P_{cu}	(W)
Winding fill factor	K_u	
Maximum operating flux density	B_{max}	(T)

The core dimensions are expressed in cm:

Core cross-sectional area	A_c	(cm^2)
Core window area	W_A	(cm^2)
Mean length per turn	MLT	(cm)

The use of centimeters rather than meters requires that appropriate factors be added to the design equations.

1. Determine core size

$$K_g \geq \frac{\rho L_M^2 I_{tot}^2 I_{M,max}^2}{B_{max}^2 P_{cu} K_u} 10^8 \quad (\text{cm}^5) \quad (11.52)$$

Choose a core which is large enough to satisfy this inequality. Note the values of A_c , W_A , and MLT for this core. The resistivity ρ of copper wire is $1.724 \cdot 10^{-6} \Omega \cdot \text{cm}$ at room temperature, and $2.3 \cdot 10^{-6} \Omega \cdot \text{cm}$ at 100°C .

2. Determine air gap length

$$\ell_g = \frac{\mu_0 L_M I_{M,max}^2}{B_{max}^2 A_c} 10^4 \quad (\text{m}) \quad (11.53)$$

Here, B_{max} is expressed in Tesla, A_c is expressed in cm^2 , and ℓ_g is expressed in meters. The permeability of free space is $\mu_0 = 4\pi \cdot 10^{-7} \text{ H/m}$. This value is approximate, and neglects fringing flux and other nonidealities.

3. Determine number of winding 1 turns

$$n_1 = \frac{L_M I_{M,max}}{B_{max} A_c} 10^4 \quad (11.54)$$

Here, B_{max} is expressed in Tesla and A_c is expressed in cm^2 .

4. Determine number of secondary turns

Use the desired turns ratios:

$$\begin{aligned} n_2 &= \left(\frac{n_2}{n_1} \right) n_1 \\ n_3 &= \left(\frac{n_3}{n_1} \right) n_1 \\ &\vdots \end{aligned} \quad (11.55)$$

5. Evaluate fraction of window area allocated to each winding

$$\begin{aligned} \alpha_1 &= \frac{n_1 I_1}{n_1 I_{tot}} \\ \alpha_2 &= \frac{n_2 I_2}{n_1 I_{tot}} \\ &\vdots \\ \alpha_k &= \frac{n_k I_k}{n_1 I_{tot}} \end{aligned} \quad (11.56)$$

6. Evaluate wire sizes

$$\begin{aligned} A_{w1} &\leq \frac{\alpha_1 K_u W_A}{n_1} \\ A_{w2} &\leq \frac{\alpha_2 K_u W_A}{n_2} \\ &\vdots \end{aligned} \quad (11.57)$$

Select wire with bare copper area less than or equal to these values. An American Wire Gauge table is included in Appendix B.

11.4 Examples

11.4.1 Coupled Inductor for a Two-Output Forward Converter

As a first example, let us consider the design of coupled inductors for the two-output forward converter illustrated in Fig. 11.12. This element can be viewed as two filter inductors that are wound on the same core. The turns ratio is chosen to be the same as the ratio of the output voltages. The magnetizing inductance performs the function of filtering the switching harmonics for both outputs, and the magnetizing current is equal to the sum of the reflected winding currents.

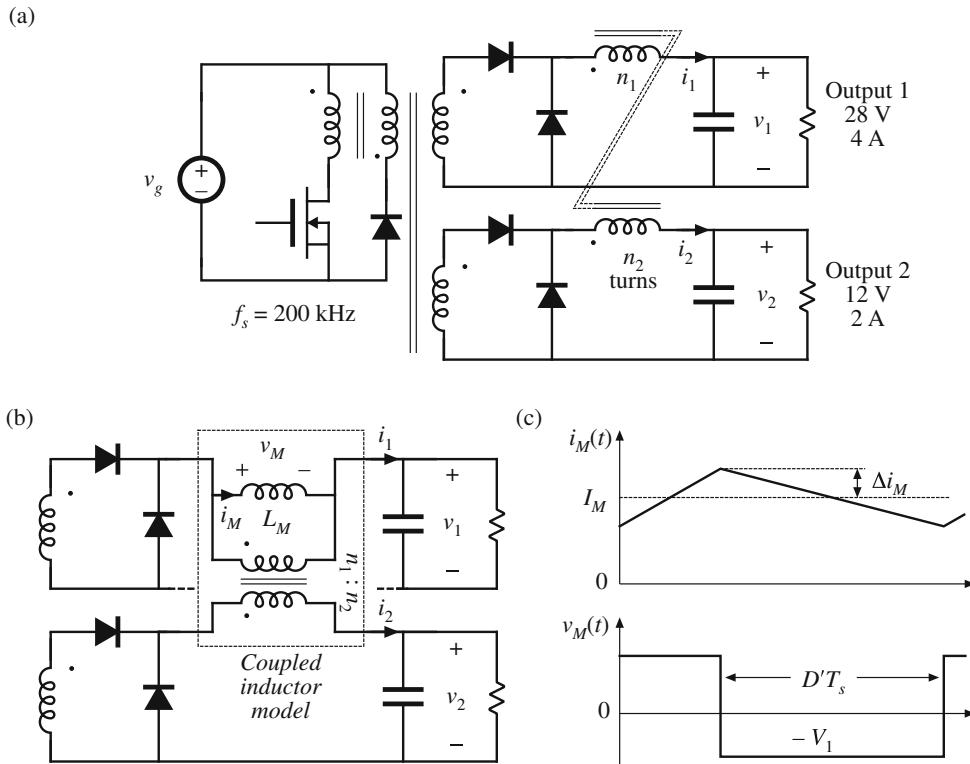


Fig. 11.12 Two-output forward converter example: (a) circuit schematic, (b) coupled inductor model inserted into converter secondary-side circuit, (c) magnetizing current and voltage waveforms of coupled inductor, referred to winding 1

At the nominal full-load operating point, the converter operates in the continuous conduction mode with a duty cycle of $D = 0.35$. The switching frequency is 200 kHz. At this operating point, it is desired that the ripple in the magnetizing current have a peak magnitude equal to 20% of the dc component of magnetizing current.

The dc component of the magnetizing current I_M is

$$\begin{aligned} I_M &= I_1 + \frac{n_2}{n_1} I_2 \\ &= (4 \text{ A}) + \frac{12}{28} (2 \text{ A}) \\ &= 4.86 \text{ A} \end{aligned} \quad (11.58)$$

The magnetizing current ripple Δi_M can be expressed as

$$\Delta i_M = \frac{V_1 D' T_s}{2L_M} \quad (11.59)$$

Since we want Δi_M to be equal to 20% of I_M , we should choose L_M as follows:

$$\begin{aligned} L_M &= \frac{V_1 D' T_s}{2\Delta i_M} \\ &= \frac{(28 \text{ V})(1 - 0.35)(5 \mu\text{s})}{2(4.86 \text{ A})(20\%)} \\ &= 47 \mu\text{H} \end{aligned} \quad (11.60)$$

The peak magnetizing current, referred to winding 1, is therefore

$$I_{M,max} = I_M + \Delta i_M = 5.83 \text{ A} \quad (11.61)$$

Since the current ripples of the winding currents are small compared to the respective dc components, the rms values of the winding currents are approximately equal to the dc components: $I_1 = 4 \text{ A}$, $I_2 = 2 \text{ A}$. Therefore, the sum of the rms winding currents, referred to winding 1, is

$$I_{tot} = I_1 + \frac{n_2}{n_1} I_2 = 4.86 \text{ A} \quad (11.62)$$

For this design, it is decided to allow 0.75 W of copper loss, and to operate the core at a maximum flux density of 0.25 Tesla. A fill factor of 0.4 is assumed. The required K_g is found by evaluation of Eq. (11.52), as follows:

$$\begin{aligned} K_g &\geq \frac{(1.724 \cdot 10^{-6} \Omega \cdot \text{cm})(47 \mu\text{H})^2 (4.86 \text{ A})^2 (5.83 \text{ A})^2}{(0.25 \text{ T})^2 (0.75 \text{ W})(0.4)} 10^8 \\ &= 16 \cdot 10^{-3} \text{ cm}^5 \end{aligned} \quad (11.63)$$

A ferrite PQ 20/16 core is selected, which has a K_g of $22.4 \cdot 10^{-3} \text{ cm}^5$. From Appendix B, the geometrical parameters for this core are $A_c = 0.62 \text{ cm}^2$, $W_A = 0.256 \text{ cm}^2$, and $MLT = 4.4 \text{ cm}$.

The air gap is found by evaluation of Eq. (11.53) as follows:

$$\begin{aligned} \ell_g &= \frac{\mu_0 L_M I_{M,max}^2}{B_{max}^2 A_c} 10^4 \\ &= \frac{(4\pi \cdot 10^{-7} \text{ H/m})(47 \mu\text{H})(5.83 \text{ A})^2}{(0.25 \text{ T})^2 (0.62 \text{ cm}^2)} 10^4 \\ &= 0.52 \text{ mm} \end{aligned} \quad (11.64)$$

In practice, a slightly longer air gap would be necessary, to allow for the effects of fringing flux and other nonidealities. The winding 1 turns are found by evaluation of Eq. (11.54):

$$\begin{aligned} n_1 &= \frac{L_M I_{M,\max}}{B_{\max} A_c} 10^4 \\ &= \frac{(47 \mu\text{H})(5.83 \text{ A})}{(0.25 \text{ T})(0.62 \text{ cm}^2)} 10^4 \\ &= 17.6 \text{ turns} \end{aligned} \quad (11.65)$$

The winding 2 turns are chosen according to the desired turns ratio:

$$\begin{aligned} n_2 &= \left(\frac{n_2}{n_1} \right) n_1 \\ &= \left(\frac{12}{28} \right) (17.6) \\ &= 7.54 \text{ turns} \end{aligned} \quad (11.66)$$

The numbers of turns are rounded off to $n_1 = 17$ turns, $n_2 = 7$ turns (18:8 would be another possible choice). The window area W_A is allocated to the windings according to the fractions from Eq. (11.56):

$$\begin{aligned} \alpha_1 &= \frac{n_1 I_1}{n_1 I_{tot}} = \frac{(17)(4 \text{ A})}{(17)(4.86 \text{ A})} = 0.8235 \\ \alpha_2 &= \frac{n_2 I_2}{n_1 I_{tot}} = \frac{(7)(2 \text{ A})}{(17)(4.86 \text{ A})} = 0.1695 \end{aligned} \quad (11.67)$$

The wire sizes can therefore be chosen as follows:

$$\begin{aligned} A_{w1} &\leq \frac{\alpha_1 K_u W_A}{n_1} = \frac{(0.8235)(0.4)(0.256 \text{ cm}^2)}{(17)} = 4.96 \cdot 10^{-3} \text{ cm}^2 \\ &\quad \text{use AWG #21} \\ A_{w2} &\leq \frac{\alpha_2 K_u W_A}{n_2} = \frac{(0.1695)(0.4)(0.256 \text{ cm}^2)}{(7)} = 2.48 \cdot 10^{-3} \text{ cm}^2 \\ &\quad \text{use AWG #24} \end{aligned} \quad (11.68)$$

11.4.2 CCM Flyback Transformer

As a second example, let us design the flyback transformer for the converter illustrated in Fig. 11.13. This converter operates with an input voltage of 200 V, and produces an full-load output of 20 V at 5 A. The switching frequency is 150 kHz. Under these operating conditions, it is desired that the converter operate in the continuous conduction mode, with a magnetizing current ripple equal to 20% of the dc component of magnetizing current. The duty cycle is chosen to be $D = 0.4$, and the turns ratio is $n_2/n_1 = 0.15$. A copper loss of 1.5 W is allowed, not including proximity effect losses. To allow room for isolation between the primary and secondary

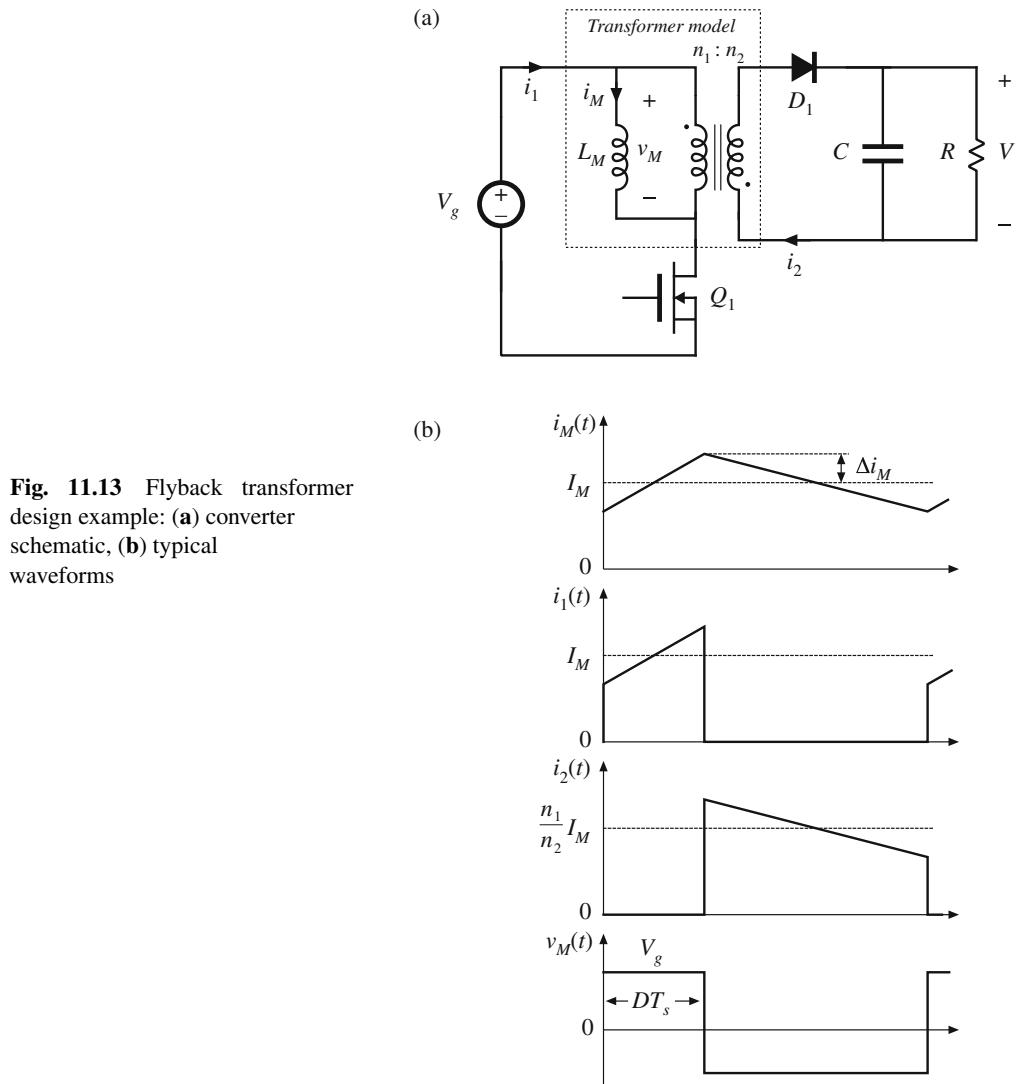


Fig. 11.13 Flyback transformer design example: (a) converter schematic, (b) typical waveforms

windings, a fill factor of $K_u = 0.3$ is assumed. A maximum flux density of $B_{max} = 0.25$ T is used; this value is less than the worst-case saturation flux density B_{sat} of the ferrite core material.

By solution of the converter using capacitor charge balance, the dc component of the magnetizing current can be found to be

$$I_M = \left(\frac{n_2}{n_1} \right) \frac{1}{D'} \frac{V}{R} = 1.25 \text{ A} \quad (11.69)$$

Hence, the magnetizing current ripple should be

$$\Delta i_M = (20\%)I_M = 0.25 \text{ A} \quad (11.70)$$

and the maximum value of the magnetizing current is

$$I_{M,max} = I_M + \Delta i_M = 1.5 \text{ A} \quad (11.71)$$

To obtain this ripple, the magnetizing inductance should be

$$\begin{aligned} L_M &= \frac{V_g D T_s}{2 \Delta i_M} \\ &= 1.07 \text{ mH} \end{aligned} \quad (11.72)$$

The rms value of the primary winding current is found using Eq. (A.6) of Appendix A, as follows:

$$I_1 = I_M \sqrt{D} \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i_M}{I_M} \right)^2} = 0.796 \text{ A} \quad (11.73)$$

The rms value of the secondary winding current is found in a similar manner:

$$I_2 = \frac{n_1}{n_2} I_M \sqrt{D'} \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i_M}{I_M} \right)^2} = 6.50 \text{ A} \quad (11.74)$$

Note that I_2 is not simply equal to the turns ratio multiplied by I_1 . The total rms winding current is equal to:

$$I_{tot} = I_1 + \frac{n_2}{n_1} I_2 = 1.77 \text{ A} \quad (11.75)$$

We can now determine the necessary core size. Evaluation of Eq. (11.52) yields

$$\begin{aligned} K_g &\geq \frac{\rho L_M^2 I_{tot}^2 I_{M,max}^2}{B_{max}^2 P_{cu} K_u} 10^8 \\ &= \frac{(1.724 \cdot 10^{-6} \Omega \cdot \text{cm})(1.07 \cdot 10^{-3} \text{ H})^2 (1.77 \text{ A})^2 (1.5 \text{ A})^2}{(0.25 \text{ T})^2 (1.5 \text{ W})(0.3)} 10^8 \\ &= 0.049 \text{ cm}^5 \end{aligned} \quad (11.76)$$

The smallest EE core listed in Appendix B that satisfies this inequality is the EE30, which has $K_g = 0.0857 \text{ cm}^5$. The dimensions of this core are

$$\begin{aligned} A_c &1.09 \text{ cm}^2 \\ W_A &0.476 \text{ cm}^2 \\ MLT &6.6 \text{ cm} \\ \ell_m &5.77 \text{ cm} \end{aligned} \quad (11.77)$$

The air gap length ℓ_g is chosen according to Eq. (11.53):

$$\begin{aligned} \ell_g &= \frac{\mu_0 L_M I_{M,max}^2}{B_{max}^2 A_c} 10^4 \\ &= \frac{(4\pi \cdot 10^{-7} \text{ H/m})(1.07 \cdot 10^{-3} \text{ H})(1.5 \text{ A})^2}{(0.25 \text{ T})^2 (1.09 \text{ cm}^2)} 10^4 \\ &= 0.44 \text{ mm} \end{aligned} \quad (11.78)$$

The number of winding 1 turns is chosen according to Eq. (11.54), as follows:

$$\begin{aligned} n_1 &= \frac{L_M I_{M,\max}}{B_{\max} A_c} 10^4 \\ &= \frac{(1.07 \cdot 10^{-3} \text{ H})(1.5 \text{ A})}{(0.25 \text{ T})(1.09 \text{ cm}^2)} 10^4 \\ &= 58.7 \text{ turns} \end{aligned} \quad (11.79)$$

Since an integral number of turns is required, we roundoff this value to

$$n_1 = 59 \quad (11.80)$$

To obtain the desired turns ratio, n_2 should be chosen as follows:

$$\begin{aligned} n_2 &= \left(\frac{n_2}{n_1} \right) n_1 \\ &= (0.15)59 \\ &= 8.81 \end{aligned} \quad (11.81)$$

We again round this value off, to

$$n_2 = 9 \quad (11.82)$$

The fractions of the window area allocated to windings 1 and 2 are selected in accordance with Eq. (11.56):

$$\begin{aligned} \alpha_1 &= \frac{I_1}{I_{tot}} = \frac{(0.796 \text{ A})}{(1.77 \text{ A})} = 0.45 \\ \alpha_2 &= \frac{n_2 I_2}{n_1 I_{tot}} = \frac{(9)(6.5 \text{ A})}{(59)(1.77 \text{ A})} = 0.55 \end{aligned} \quad (11.83)$$

The wire gauges should therefore be

$$\begin{aligned} A_{W1} &\leq \frac{\alpha_1 K_u W_A}{n_1} = 1.09 \cdot 10^{-3} \text{ cm}^2 \quad \text{—use #28 AWG} \\ A_{W2} &\leq \frac{\alpha_2 K_u W_A}{n_2} = 8.88 \cdot 10^{-3} \text{ cm}^2 \quad \text{—use #19 AWG} \end{aligned} \quad (11.84)$$

The above American Wire Gauges are selected using the wire gauge table given at the end of Appendix B.

The above design does not account for core loss or copper loss caused by the proximity effect. Let us compute the core loss for this design. Figure Fig. 11.14 contains a sketch of the B - H loop for this design. The flux density $B(t)$ can be expressed as a dc component (determined by the dc value of the magnetizing current I_M), plus an ac variation of peak amplitude ΔB that is determined by the current ripple Δi_M . The maximum value of $B(t)$ is labeled B_{\max} ; this value is determined by the sum of the dc component and the ac ripple component. The core material saturates when the applied $B(t)$ exceeds B_{sat} ; hence, to avoid saturation, B_{\max} should be less than B_{sat} . The core loss is determined by the amplitude of the ac variations in $B(t)$, i.e., by ΔB .

Fig. 11.14 B - H loop for the flyback transformer design example

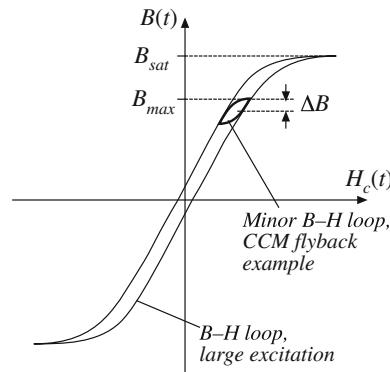
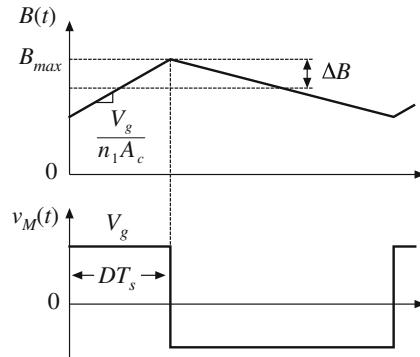


Fig. 11.15 Variation of flux density $B(t)$, flyback transformer example



The ac component ΔB is determined using Faraday's law, as follows. Solution of Faraday's law for the derivative of $B(t)$ leads to

$$\frac{dB(t)}{dt} = \frac{v_M(t)}{n_1 A_c} \quad (11.85)$$

As illustrated in Fig. 11.15, the voltage applied during the first subinterval is $v_M(t) = V_g$. This causes the flux density to increase with slope

$$\frac{dB(t)}{dt} = \frac{V_g}{n_1 A_c} \quad (11.86)$$

Over the first subinterval $0 < t < DT_s$, the flux density $B(t)$ changes by the net amount $2\Delta B$. This net change is equal to the slope given by Eq. (11.86), multiplied by the interval length DT_s :

$$\Delta B = \left(\frac{V_g}{2n_1 A_c} \right) (DT_s) \quad (11.87)$$

Upon solving for ΔB and expressing A_c in cm^2 , we obtain

$$\Delta B = \frac{V_g DT_s}{2n_1 A_c} 10^4 \quad (11.88)$$

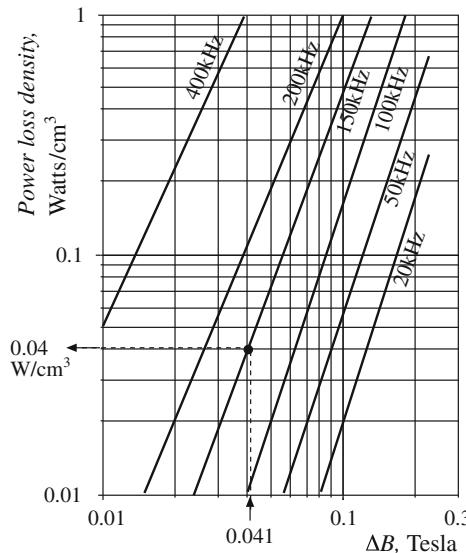


Fig. 11.16 Determination of core loss density for the flyback transformer design example

For the flyback transformer example, the peak ac flux density is found to be

$$\begin{aligned}\Delta B &= \frac{(200 \text{ V})(0.4)(6.67 \mu\text{s})}{2(59)(1.09 \text{ cm}^2)} 10^4 \\ &= 0.041 \text{ T}\end{aligned}\quad (11.89)$$

To determine the core loss, we next examine the data provided by the manufacturer for the given core material. A typical plot of core loss is illustrated in Fig. 11.16. For the values of ΔB and switching frequency of the flyback transformer design, this plot indicates that 0.04 W will be lost in every cm^3 of the core material. Of course, this value neglects the effects of harmonics on core loss. The total core loss P_{fe} will therefore be equal to this loss density, multiplied by the volume of the core:

$$\begin{aligned}P_{fe} &= (0.04 \text{ W}/\text{cm}^3)(A_c \ell_m) \\ &= (0.04 \text{ W}/\text{cm}^3)(1.09 \text{ cm}^2)(5.77 \text{ cm}) \\ &= 0.25 \text{ W}\end{aligned}\quad (11.90)$$

This core loss is less than the copper loss of 1.5 W, and neglecting the core loss is often warranted in designs that operate in the continuous conduction mode and that employ ferrite core materials.

11.5 Summary of Key Points

1. A variety of magnetic devices are commonly used in switching converters. These devices differ in their core flux density variations, as well as in the magnitudes of the ac winding currents. When the flux density variations are small, core loss can be neglected. Alternatively, a low-frequency material can be used, having higher saturation flux density.

2. The core geometrical constant K_g is a measure of the magnetic size of a core, for applications in which copper loss is dominant. In the K_g design method, flux density and total copper loss are specified. Design procedures for single-winding filter inductors and for conventional multiple-winding transformers are derived.

PROBLEMS

- 11.1** A simple buck converter operates with a 50 kHz switching frequency and a dc input voltage of $V_g = 40$ V. The output voltage is $V = 20$ V. The load resistance is $R \geq 4 \Omega$.
- (a) Determine the value of the output filter inductance L such that the peak-to-average inductor current ripple Δi is 10% of the dc component I .
 - (b) Determine the peak steady-state inductor current I_{max} .
 - (c) Design an inductor which has the values of L and I_{max} from parts (a) and (b). Use a ferrite EE core, with $B_{max} = 0.25$ T. Choose a value of winding resistance such that the inductor copper loss is less than or equal to 1 W at room temperature. Assume $K_u = 0.5$. Specify: core size, gap length, wire size (AWG), and number of turns.
- 11.2** A boost converter operates at the following quiescent point: $V_g = 28$ V, $V = 48$ V, $P_{load} = 150$ W, $f_s = 100$ kHz. Design the inductor for this converter. Choose the inductance value such that the peak current ripple is 10% of the dc inductor current. Use a peak flux density of 0.225 T, and assume a fill factor of 0.5. Allow copper loss equal to 0.5% of the load power, at room temperature. Use a ferrite PQ core. Specify: core size, air gap length, wire gauge, and number of turns.
- 11.3** Extension of the K_g approach to design of two-winding transformers. It is desired to design a transformer having a turns ratio of $1 : n$. The transformer stores negligible energy, no air gap is required, and the ratio of the winding currents $i_2(t)/i_1(t)$ is essentially equal to the turns ratio n . The applied primary volt-seconds λ_1 are defined for a typical PWM voltage waveform $v_1(t)$ in Fig. 10.45b; these volt-seconds should cause the maximum flux density to be equal to a specified value $B_{max} = \Delta B$. You may assume that the flux density $B(t)$ contains no dc bias, as in Fig. 10.46. You should allocate half of the core window area to each winding. The total copper loss P_{cu} is also specified. You may neglect proximity losses.
- (a) Derive a transformer design procedure, in which the following quantities are specified: total copper loss P_{cu} , maximum flux density B_{max} , fill factor K_u , wire resistivity ρ , rms primary current I_1 , applied primary volt-seconds λ_1 , and turns ratio $1:n$. Your procedure should yield the following data: required core geometrical constant K_g , primary and secondary turns n_1 and n_2 , and primary and secondary wire areas A_{w1} and A_{w2} .
 - (b) The voltage waveform applied to the transformer primary winding of the Ćuk converter (Fig. 6.42c) is equal to the converter input voltage V_g while the transistor conducts, and is equal to $-V_g D/(1 - D)$ while the diode conducts. This converter operates with a switching frequency of 100 kHz, and a transistor duty cycle D equal to 0.4. The dc input voltage is $V_g = 120$ V, the dc output voltage is $V = 24$ V, and the load power is 200 W. You may assume a fill factor of $K_u = 0.3$. Use your procedure of part (a) to design a transformer for this application, in which $B_{max} = 0.15$ T, and $P_{cu} = 0.25$ W at 100°C. Use a ferrite PQ core. Specify: core size, primary and secondary turns, and wire gauges.

- 11.4** Coupled inductor design. The two-output forward converter of Fig. 10.47a employs secondary-side coupled inductors. An air gap is employed.

Design a coupled inductor for the following application: $V_1 = 5 \text{ V}$, $V_2 = 15 \text{ V}$, $I_1 = 20 \text{ A}$, $I_2 = 4 \text{ A}$, $D = 0.4$. The magnetizing inductance should be equal to $8 \mu\text{H}$, referred to the 5 V winding. You may assume a fill factor K_u of 0.5. Allow a total of 1 W of copper loss at 100°C , and use a peak flux density of $B_{max} = 0.2 \text{ T}$. Use a ferrite EE core. Specify: core size, air gap length, number of turns, and wire gauge for each winding.

- 11.5** Flyback transformer design. A flyback converter operates with a 160 Vdc input, and produces a 28 Vdc output. The maximum load current is 2 A. The transformer turns ratio is 8:1. The switching frequency is 100 kHz. The converter should be designed to operate in the discontinuous conduction mode at all load currents. The total copper loss should be less than 0.75 W.

- (a) Choose the value of transformer magnetizing inductance L_M such that, at maximum load current, $D_3 = 0.1$ (the duty cycle of subinterval 3, in which all semiconductors are off). Please indicate whether your value of L_M is referred to the primary or secondary winding. What is the peak transistor current? The peak diode current?
- (b) Design a flyback transformer for this application. Use a ferrite pot core with $B_{max} = 0.25 \text{ Tesla}$, and with fill factor $K_u = 0.4$. Specify: core size, primary and secondary turns and wire sizes, and air gap length.
- (c) For your design of part (b), compute the copper losses in the primary and secondary windings. You may neglect proximity loss.
- (d) For your design of part (b), compute the core loss. Loss data for the core material is given by Fig. 10.20. Is the core loss less than the copper loss computed in Part (c)?



Transformer Design

In the design methods of the previous chapter, copper loss P_{cu} and maximum flux density B_{max} are specified, while core loss P_{fe} is not specifically addressed. This approach is appropriate for a number of applications, such as the filter inductor in which the dominant design constraints are copper loss and saturation flux density. However, in a substantial class of applications, the operating flux density is limited by core loss rather than saturation. For example, in a conventional high-frequency transformer, it is usually necessary to limit the core loss by operating at a reduced value of the peak ac flux density ΔB .

Design of core loss-limited magnetic devices is characterized by finding the ac flux density that minimizes total core plus copper loss. Typically, this optimization problem also involves optimization of the winding geometry to control ac proximity losses, and possibly incorporation of other constraints such as galvanic isolation. Consequently, multiple design iterations are required. In this chapter, the basic design equations are developed, and a first-pass design that minimizes the total core loss plus dc copper loss is found. The winding geometry can then be estimated, and ac proximity losses can be analyzed as described in Sect. 10.4. The design can then be iterated as needed.

This chapter covers the general transformer design problem. It is desired to design a k -winding transformer as illustrated in Fig. 12.1. Both copper loss P_{cu} and core loss P_{fe} are modeled. As the operating flux density is increased (by decreasing the number of turns), the copper loss is decreased but the core loss is increased. We will determine the operating flux density that minimizes the total power loss $P_{tot} = P_{fe} + P_{cu}$.

It is possible to generalize the core geometrical constant K_g design method, derived in the previous chapter, to treat the design of magnetic devices when both copper loss and core loss are significant. This leads to the geometrical constant K_{gfe} , a measure of the effective magnetic size of core in a transformer design application. Several examples of transformer designs via the K_{gfe} method are given in this chapter. A similar procedure is also derived, for design of single-winding inductors in which core loss is significant.

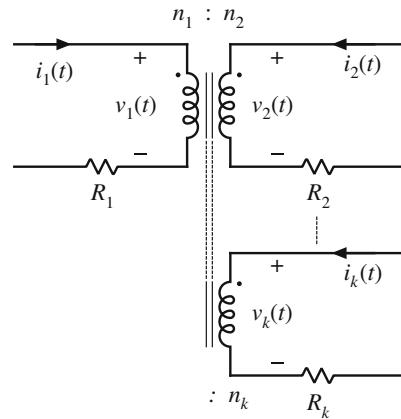


Fig. 12.1 A k -winding transformer, in which both core loss and copper loss are significant

12.1 Transformer Design: Basic Constraints

As in the case of the filter inductor design, we can write several basic constraining equations. These equations can then be combined into a single equation for selection of the core size. In the case of transformer design, the basic constraints describe the core loss, flux density, copper loss, and total power loss vs. flux density. The flux density is then chosen to optimize the total power loss.

12.1.1 Core Loss

As described in Chap. 10, the total core loss P_{fe} depends on the peak ac flux density ΔB , the operating frequency f , and the volume of the core. At a given frequency, we can approximate the core loss by a function of the form

$$P_{fe} = K_{fe}(\Delta B)^\beta A_c \ell_m \quad (12.1)$$

Again, A_c is the core cross-sectional area, ℓ_m is the core mean magnetic path length, and hence $A_c \ell_m$ is the volume of the core. K_{fe} is a constant of proportionality which depends on the operating frequency. The exponent β is determined from the core manufacturer's published data. Typically, the value of β for ferrite power materials is approximately 2.6; for other core materials, this exponent lies in the range 2 to 3. Equation (12.1) generally assumes that the applied waveforms are sinusoidal; effects of waveform harmonic content are ignored here.

12.1.2 Flux Density

An arbitrary periodic primary voltage waveform $v_1(t)$ is illustrated in Fig. 12.2. The volt-seconds applied during the positive portion of the waveform is denoted λ_1 :

$$\lambda_1 = \int_{t_1}^{t_2} v_1(t) dt \quad (12.2)$$

These volt-seconds, or flux-linkages, cause the flux density to change from its negative peak to its positive peak value. Hence, from Faraday's law, the peak value of the ac component of the flux density is

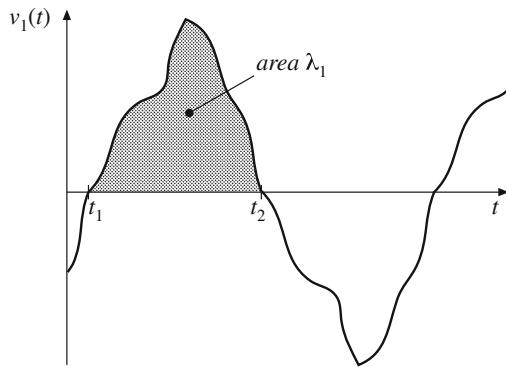


Fig. 12.2 An arbitrary transformer primary voltage waveform, illustrating the volt-seconds applied during the positive portion of the cycle

$$\Delta B = \frac{\lambda_1}{2n_1 A_c} \quad (12.3)$$

Note that, for a given applied voltage waveform and λ_1 , we can reduce ΔB by increasing the primary turns n_1 . This has the effect of decreasing the core loss according to Eq. (12.1). However, it also causes the copper loss to increase, since the new windings will be comprised of more turns of smaller wire. As a result, there is an optimal choice for ΔB , in which the total loss is minimized. In the next sections, we will determine the optimal ΔB . Having done so, we can then use Eq. (12.3) to determine the primary turns n_1 , as follows:

$$n_1 = \frac{\lambda_1}{2\Delta B A_c} \quad (12.4)$$

It should also be noted that, in some converter topologies such as the forward converter with conventional reset winding, the flux density $B(t)$ and the magnetizing current $i_M(t)$ are not allowed to be negative. In consequence, the instantaneous flux density $B(t)$ contains a dc bias. Provided that the core does not approach saturation, this dc bias does not significantly affect the core loss: core loss is determined by the ac component of $B(t)$. Equations (12.2) to (12.4) continue to apply to this case, since ΔB is the peak value of the ac component of $B(t)$.

12.1.3 Copper Loss

As shown in Sect. 11.3.1, the total copper loss is minimized when the core window area W_A is allocated to the various windings according to their relative apparent powers. The total copper loss is then given by Eq. (11.34). This equation can be expressed in the form

$$P_{cu} = \frac{\rho(MLT)n_1^2 I_{tot}^2}{W_A K_u} \quad (12.5)$$

where

$$I_{tot} = \sum_{j=1}^k \frac{n_j}{n_1} I_j \quad (12.6)$$

is the sum of the rms winding currents, referred to winding 1. Use of Eq. (12.4) to eliminate n_1 from Eq. (12.5) leads to

$$P_{cu} = \left(\frac{\rho \lambda_1^2 I_{tot}^2}{4K_u} \right) \left(\frac{MLT}{WAA_c^2} \right) \left(\frac{1}{\Delta B} \right)^2 \quad (12.7)$$

The right-hand side of Eq. (12.7) is grouped into three terms. The first group contains specifications, while the second group is a function of the core geometry. The last term is a function of ΔB , to be chosen to optimize the design. It can be seen that copper loss varies as the inverse square of ΔB ; increasing ΔB reduces P_{cu} .

The increased copper loss due to the proximity effect is not explicitly accounted for in this design procedure. In practice, the proximity loss must be estimated after the core and winding geometries are known. However, the increased ac resistance due to proximity loss can be accounted for in the design procedure. The effective value of the wire resistivity ρ is increased by a factor equal to the estimated ratio R_{ac}/R_{dc} . When the core geometry is known, the engineer can attempt to implement the windings such that the estimated R_{ac}/R_{dc} is obtained. Several design iterations may be needed.

12.1.4 Total Power Loss vs. ΔB

The total power loss P_{tot} is found by adding Eqs. (12.1) and (12.7):

$$P_{tot} = P_{fe} + P_{cu} \quad (12.8)$$

The dependence of P_{fe} , P_{cu} , and P_{tot} on ΔB is sketched in Fig. 12.3.

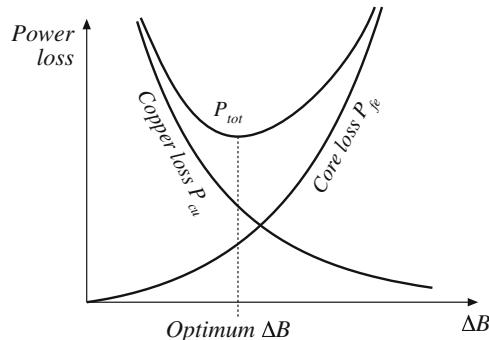


Fig. 12.3 Dependence of copper loss, core loss, and total loss on peak ac flux density

12.1.5 Optimum Flux Density

Let us now choose the value of ΔB that minimizes Eq. (12.8). At the optimum ΔB , we can write

$$\frac{dP_{tot}}{d(\Delta B)} = \frac{dP_{fe}}{d(\Delta B)} + \frac{dP_{cu}}{d(\Delta B)} = 0 \quad (12.9)$$

Note that the optimum does not necessarily occur where $P_{fe} = P_{cu}$. Rather, it occurs where

$$\frac{dP_{fe}}{d(\Delta B)} = -\frac{dP_{cu}}{d(\Delta B)} \quad (12.10)$$

The derivatives of the core and copper losses with respect to ΔB are given by

$$\frac{dP_{fe}}{d(\Delta B)} = \beta K_{fe} (\Delta B)^{(\beta-1)} A_c \ell_m \quad (12.11)$$

$$\frac{dP_{cu}}{d(\Delta B)} = -2 \left(\frac{\rho \lambda_1^2 I_{tot}^2}{4K_u} \right) \left(\frac{(MLT)}{W_A A_c^2} \right) (\Delta B)^{-3} \quad (12.12)$$

Substitution of Eqs. (12.11) and (12.12) into Eq. (12.10), and solution for ΔB , leads to the optimum flux density

$$\Delta B = \left[\frac{\rho \lambda_1^2 I_{tot}^2}{2K_u} \frac{(MLT)}{W_A A_c^3 \ell_m} \frac{1}{\beta K_{fe}} \right]^{\left(\frac{1}{\beta+2}\right)} \quad (12.13)$$

The resulting total power loss is found by substitution of Eq. (12.13) into (12.1), (12.8), and (12.9). Simplification of the resulting expression leads to

$$P_{tot} = [A_c \ell_m K_{fe}]^{\left(\frac{2}{\beta+2}\right)} \left[\frac{\rho \lambda_1^2 I_{tot}^2 (MLT)}{4K_u W_A A_c^2} \right]^{\left(\frac{\beta}{\beta+2}\right)} \left[\left(\frac{\beta}{2}\right)^{-\left(\frac{\beta}{\beta+2}\right)} + \left(\frac{\beta}{2}\right)^{\left(\frac{2}{\beta+2}\right)} \right] \quad (12.14)$$

This expression can be regrouped, as follows:

$$\frac{W_A (A_c)^{(2(\beta-1)/\beta)}}{(MLT) \ell_m^{(2/\beta)}} \left[\left(\frac{\beta}{2}\right)^{-\left(\frac{\beta}{\beta+2}\right)} + \left(\frac{\beta}{2}\right)^{\left(\frac{2}{\beta+2}\right)} \right]^{-\left(\frac{\beta+2}{\beta}\right)} = \frac{\rho \lambda_1^2 I_{tot}^2 K_{fe}^{(2/\beta)}}{4K_u (P_{tot})^{((\beta+2)/\beta)}} \quad (12.15)$$

The terms on the left side of Eq. (12.15) depend on the core geometry, while the terms on the right side depend on specifications regarding the application (ρ , I_{tot} , λ_1 , K_u , P_{tot}) and the desired core material (K_{fe} , β). The left side of Eq. (12.15) can be defined as the core geometrical constant K_{gfe} :

$$K_{gfe} = \frac{W_A (A_c)^{(2(\beta-1)/\beta)}}{(MLT) \ell_m^{(2/\beta)}} \left[\left(\frac{\beta}{2}\right)^{-\left(\frac{\beta}{\beta+2}\right)} + \left(\frac{\beta}{2}\right)^{\left(\frac{2}{\beta+2}\right)} \right]^{-\left(\frac{\beta+2}{\beta}\right)} \quad (12.16)$$

Hence, to design a transformer, the right side of Eq. (12.15) is evaluated. A core is selected whose K_{gfe} exceeds this value:

$$K_{gfe} \geq \frac{\rho \lambda_1^2 I_{tot}^2 K_{fe}^{(2/\beta)}}{4K_u (P_{tot})^{((\beta+2)/\beta)}} \quad (12.17)$$

The quantity K_{gfe} is similar to the geometrical constant K_g used in the previous chapter to design magnetics when core loss is negligible. K_{gfe} is a measure of the magnetic size of a core, for applications in which core loss is significant. Unfortunately, K_{gfe} depends on β , and hence the choice of core material affects the value of K_{gfe} . However, the β of most high-frequency ferrite materials lies in the narrow range 2.6 to 2.8, and K_{gfe} varies by no more than $\pm 5\%$ over this range. Appendix B lists the values of K_{gfe} for various standard ferrite cores, for the value $\beta = 2.7$.

Once a core has been selected, then the values of A_c , W_A , ℓ_m , and MLT are known. The peak ac flux density ΔB can then be evaluated using Eq. (12.13), and the primary turns n_1 can be found using Eq. (12.4). The number of turns for the remaining windings can be computed using

the desired turns ratios. The various window area allocations are found using Eq. (11.35). The wire sizes for the various windings can then be computed as discussed in the previous chapter,

$$A_{w,j} = \frac{K_u W_A \alpha_j}{n_j} \quad (12.18)$$

where $A_{w,j}$ is the wire area for winding j .

12.2 A First-Pass Transformer Design Procedure

The procedure developed in the previous sections is summarized below. As in the filter inductor design procedure of the previous chapter, this simple transformer design procedure should be regarded as a first-pass approach. Numerous issues have been neglected, including detailed insulation requirements, conductor eddy current losses, temperature rise, roundoff of number of turns, etc.

The following quantities are specified, using the units noted:

Wire effective resistivity	ρ	($\Omega\text{-cm}$)
Total rms winding currents, referred to primary	$I_{tot} = \sum_{j=1}^k \frac{n_j}{n_i} I_j$	(A)
Desired turns ratios	$n_2/n_1, n_3/n_1, \text{etc.}$	
Applied primary volt-seconds	$\lambda_1 = \int v_1(t) dt$	(V-sec) <small>positive portion of cycle</small>
Allowed total power dissipation	P_{tot}	(W)
Winding fill factor	K_u	
Core loss exponent	β	
Core loss coefficient	K_{fe}	($\text{W/cm}^3 \text{T}^\beta$)

The core dimensions are expressed in cm:

Core cross-sectional area	A_c	(cm^2)
Core window area	W_A	(cm^2)
Mean length per turn	MLT	(cm)
Magnetic path length	ℓ_m	(cm)
Peak ac flux density	ΔB	(Tesla)
Wire areas	A_{w1}, A_{w2}, \dots	(cm^2)

The use of centimeters rather than meters requires that appropriate factors be added to the design equations.

12.2.1 Procedure

1. Determine core size.

$$K_{gfe} \geq \frac{\rho \lambda_1^2 I_{tot}^2 K_{fe}^{(2/\beta)}}{4K_u(P_{tot})^{((\beta+2)/\beta)}} 10^8 \quad (12.19)$$

Choose a core that is large enough to satisfy this inequality. If necessary, it may be possible to use a smaller core by choosing a core material having lower loss, i.e., smaller K_{fe} .

2. Evaluate peak ac flux density.

$$\Delta B = \left[10^8 \frac{\rho \lambda_1^2 I_{tot}^2}{2K_u} \frac{(MLT)}{W_A A_c^3 \ell_m} \frac{1}{\beta K_{fe}} \right]^{\left(\frac{1}{\beta+2}\right)} \quad (12.20)$$

Check whether ΔB is greater than the core material saturation flux density. If the core operates with a flux dc bias, then the dc bias plus ΔB should not exceed the saturation flux density. Proceed to the next step if adequate margins exist to prevent saturation. Otherwise, (1) repeat the procedure using a core material having greater core loss, or (2) use the K_g design method, in which the maximum flux density is specified.

3. Evaluate primary turns.

$$n_1 = \frac{\lambda_1}{2\Delta B A_c} 10^4 \quad (12.21)$$

4. Choose numbers of turns for other windings.

According to the desired turns ratios:

$$\begin{aligned} n_2 &= n_1 \left(\frac{n_2}{n_1} \right) \\ n_3 &= n_1 \left(\frac{n_3}{n_1} \right) \\ &\vdots \end{aligned} \quad (12.22)$$

5. Evaluate fraction of window area allocated to each winding.

$$\begin{aligned} \alpha_1 &= \frac{n_1 I_1}{n_1 I_{tot}} \\ \alpha_2 &= \frac{n_2 I_2}{n_1 I_{tot}} \\ &\vdots \\ \alpha_k &= \frac{n_k I_k}{n_1 I_{tot}} \end{aligned} \quad (12.23)$$

6. Evaluate wire sizes.

$$\begin{aligned} A_{w1} &\leq \frac{\alpha_1 K_u W_A}{n_1} \\ A_{w2} &\leq \frac{\alpha_2 K_u W_A}{n_2} \\ &\vdots \end{aligned} \quad (12.24)$$

Choose wire gauges to satisfy these criteria.

A winding geometry can now be determined, and copper losses due to the proximity effect can be evaluated. If these losses are significant, it may be desirable to further optimize the design by reiterating the above steps, accounting for proximity losses by increasing the effective

wire resistivity to the value $\rho_{eff} = \rho_{cu}P_{cu}/P_{dc}$, where P_{cu} is the actual copper loss including proximity effects, and P_{dc} is the copper loss obtained when the proximity effect is negligible.

If desired, the power losses and transformer model parameters can now be checked. For the simple model of Fig. 12.4, the following parameters are estimated:

$$\text{Magnetizing inductance, referred to winding 1: } L_M = \frac{\mu n_1^2 A_c}{\ell_m}$$

$$\text{Peak ac magnetizing current, referred to winding 1: } i_{M,pk} = \frac{\lambda_1}{2L_M}$$

Winding resistances:

$$R_1 = \frac{\rho n_1 (MLT)}{A_{w1}}$$

$$R_2 = \frac{\rho n_2 (MLT)}{A_{w2}}$$

$$\vdots$$

The core loss, copper loss, and total power loss can be determined using Eqs. (12.1), (12.7), and (12.8), respectively.

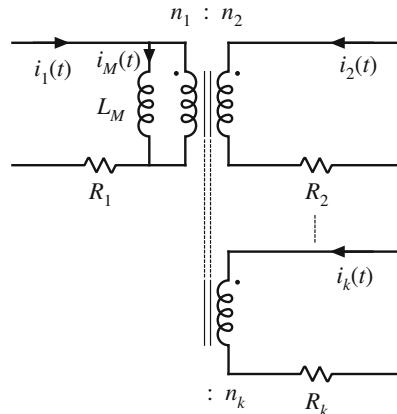


Fig. 12.4 Computed elements of simple transformer model

12.3 Examples

12.3.1 Example 1: Single-Output Isolated Ćuk Converter

As an example, let us consider the design of a simple two-winding transformer for the Ćuk converter of Fig. 12.5. This transformer is to be optimized at the operating point shown, corresponding to $D = 0.5$. The steady-state converter solution is $V_{c1} = V_g$, $V_{c2} = V$. The desired

transformer turns ratio is $n = n_1/n_2 = 5$. The switching frequency is $f_s = 200$ kHz, corresponding to $T_s = 5 \mu\text{s}$. A ferrite pot core is to be used; at 200 kHz, the chosen ferrite core material is described by the following parameters: $K_{fe} = 24.7 \text{ W/T}^3\text{cm}^3$, $\beta = 2.6$. A fill factor of $K_u = 0.5$ is assumed. Total power loss of $P_{tot} = 0.25 \text{ W}$ is allowed. Copper wire, having a resistivity of $\rho = 1.724 \cdot 10^{-6} \Omega\text{-cm}$, is to be used.

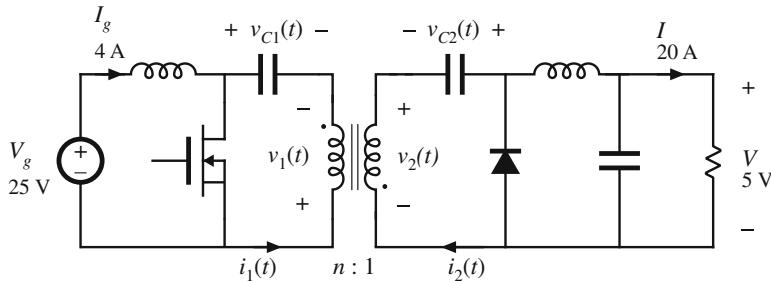
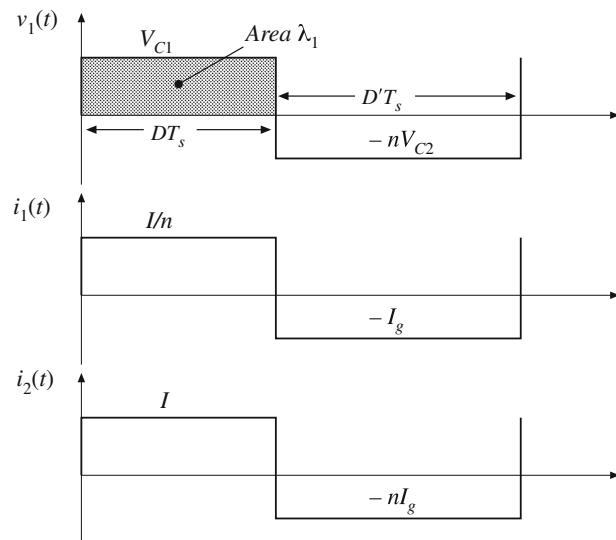


Fig. 12.5 Isolated Ćuk converter example

Fig. 12.6 Waveforms, Ćuk converter transformer design example



Transformer waveforms are illustrated in Fig. 12.6. The applied primary volt-seconds are

$$\begin{aligned}\lambda_1 &= DT_s V_{c1} = (0.5)(5 \mu\text{s})(25 \text{ V}) \\ &= 62.5 \text{ V} \cdot \mu\text{sec}\end{aligned}\quad (12.25)$$

The primary rms current is

$$I_1 = \sqrt{D \left(\frac{I}{n} \right)^2 + D'(I_g)^2} = 4\text{A} \quad (12.26)$$

It is assumed that the rms magnetizing current is much smaller than the rms winding currents. Since the transformer contains only two windings, the secondary rms current is equal to

$$I_2 = nI_1 = 20 \text{ A} \quad (12.27)$$

The total rms winding current, referred to the primary, is

$$I_{tot} = I_1 + \frac{1}{n}I_2 = 8 \text{ A} \quad (12.28)$$

The core size is evaluated using Eq. (12.19):

$$\begin{aligned} K_{gfe} &\geq \frac{(1.724 \cdot 10^{-6})(62.5 \cdot 10^{-6})^2(8)^2(24.7)^{(2/26)}}{4(0.5)(0.25)^{(4.6/2.6)}} 10^8 \\ &= 0.00295 \end{aligned} \quad (12.29)$$

The pot core data of Appendix B lists the 2213 pot core with $K_{gfe} = 0.0049$ for $\beta = 2.7$. Evaluation of Eq. (12.16) shows that $K_{gfe} = 0.0047$ for this core, when $\beta = 2.6$. In any event, 2213 is the smallest standard pot core size having $K_{gfe} \leq 0.00295$. The increased value of K_{gfe} should lead to lower total power loss. The peak ac flux density is found by evaluation of Eq. (12.20), using the geometrical data for the 2213 pot core:

$$\begin{aligned} \Delta B &= \left[10^8 \frac{(1.724 \cdot 10^{-6})(62.5 \cdot 10^{-6})^2(8)^2}{2(0.5)} \frac{(4.42)}{(0.297)(0.635)^3(3.15)} \frac{1}{(2.6)(24.7)} \right]^{(1/4.6)} \\ &= 0.0858 \text{ Tesla} \end{aligned} \quad (12.30)$$

This flux density is considerably less than the saturation flux density of approximately 0.35 Tesla. The primary turns are determined by evaluation of Eq. (12.21):

$$\begin{aligned} n_1 &= 10^4 \frac{(62.5 \cdot 10^{-6})}{2(0.0858)(0.635)} \\ &= 5.74 \text{ turns} \end{aligned} \quad (12.31)$$

The secondary turns are found by evaluation of Eq. (12.22). It is desired that the transformer have a 5:1 turns ratio, and hence

$$n_2 = \frac{n_1}{n} = 1.15 \text{ turns} \quad (12.32)$$

In practice, we might select $n_1 = 5$ and $n_2 = 1$. This would lead to a slightly higher ΔB and slightly higher loss.

The fraction of the window area allocated to windings 1 and 2 are determined using Eq. (12.23):

$$\begin{aligned} \alpha_1 &= \frac{(4A)}{(8A)} = 0.5 \\ \alpha_2 &= \frac{(\frac{1}{5})(20A)}{(8A)} = 0.5 \end{aligned} \quad (12.33)$$

For this example, the window area is divided equally between the primary and secondary windings, since the ratio of their rms currents is equal to the turns ratio. We can now evaluate the primary and secondary wire areas, via Eq. (12.24):

$$A_{w1} = \frac{(0.5)(0.5)(0.297)}{(5)} = 14.8 \cdot 10^{-3} \text{cm}^2$$

$$A_{w2} = \frac{(0.5)(0.5)(0.297)}{(1)} = 74.2 \cdot 10^{-3} \text{cm}^2 \quad (12.34)$$

The wire gauge is selected using the wire table of Appendix B. AWG #16 has area $13.07 \cdot 10^{-3} \text{cm}^2$, and is suitable for the primary winding. AWG #9 is suitable for the secondary winding, with area $66.3 \cdot 10^{-3} \text{cm}^2$. These are very large conductors, and one turn of AWG #9 is not a practical solution! We can also expect significant proximity losses, and significant leakage inductance. In practice, interleaved foil windings might be used. Alternatively, Litz wire or several parallel strands of smaller wire could be employed.

It is a worthwhile exercise to repeat the above design at several different switching frequencies, to determine how transformer size varies with switching frequency. As the switching frequency is increased, the core loss coefficient K_{fe} increases. Figure 12.7 illustrates the transformer pot core size, for various switching frequencies over the range 25 kHz to 1 MHz, for this Ćuk converter example using P material with $P_{tot} < 0.25 \text{ W}$. Peak flux densities in Tesla are also plotted. For switching frequencies below 250 kHz, increasing the frequency causes the core size to decrease. This occurs because of the decreased applied volt-seconds λ_1 . Over this range, the optimal ΔB is essentially independent of switching frequency; the ΔB variations shown occur owing to quantization of core sizes.

For switching frequencies greater than 250 kHz, increasing frequency causes greatly increased core loss. Maintaining $P_{tot} \leq 0.25 \text{ W}$ then requires that ΔB be reduced, and hence the core size is increased. The minimum transformer size for this example is apparently obtained at 250 kHz.

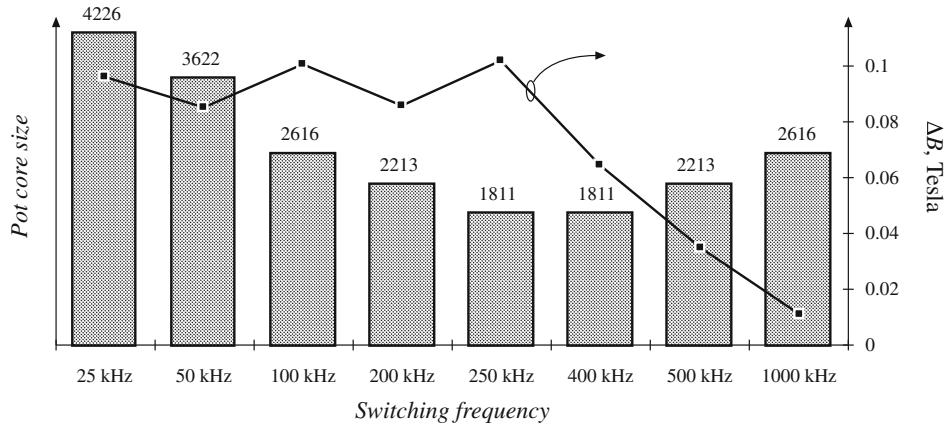


Fig. 12.7 Variation of transformer size (bar chart) with switching frequency, Ćuk converter example. Optimum peak ac flux density (data points) is also plotted

In practice, several matters complicate the dependence of transformer size on switching frequency. Figure 12.7 ignores the winding geometry and copper losses due to winding eddy currents. Greater power losses can be allowed in larger cores. Use of a different core material

may allow higher or lower switching frequencies. The same core material, used in a different application with different specifications, may lead to a different optimal frequency. Nonetheless, examples have been reported in the literature [100–103] in which ferrite transformer size is minimized at frequencies ranging from several hundred kilohertz to several megahertz. More detailed design optimizations can be performed using computer optimization programs [104, 105].

12.3.2 Example 2: Multiple-Output Full-Bridge Buck Converter

As a second example, let us consider the design of transformer T_1 for the multiple-output full-bridge buck converter of Fig. 12.8. This converter has a 5 V and a 15 V output, with maximum loads as shown. The transformer is to be optimized at the full-load operating point shown, corresponding to $D = 0.75$. Waveforms are illustrated in Fig. 12.9. The converter switching frequency is $f_s = 150$ kHz. In the full-bridge configuration, the transformer waveforms have fundamental frequency equal to one-half of the switching frequency, so the effective transformer frequency is 75 kHz. Upon accounting for losses caused by diode forward voltage drops, one finds that the desired transformer turns ratios $n_1 : n_2 : n_3$ are 110:5: 15. A ferrite EE consisting of Magnetics, Inc. P-material is to be used in this example; at 75 kHz, this material is described by the following parameters: $K_{fe} = 7.6 \text{ W/T}^\beta \text{cm}^3$, $\beta = 2.6$. A fill factor of $K_u = 0.25$ is assumed in this isolated multiple-output application. Total power loss of $P_{tot} = 4 \text{ W}$, or approximately 0.5% of the load power, is allowed. Copper wire, having a resistivity of $\rho = 1.724 \cdot 10^{-6} \Omega\text{-cm}$, is to be used.

The applied primary volt-seconds are

$$\lambda_1 = DT_s V_g = (0.75)(6.67 \mu \text{sec})(160 \text{ V}) = 800 \text{ V} - \mu \text{ sec} \quad (12.35)$$

The primary rms current is

$$I_1 = \left(\frac{n_2}{n_1} I_{5V} + \frac{n_3}{n_1} I_{15V} \right) \sqrt{D} = 5.7 \text{ A} \quad (12.36)$$

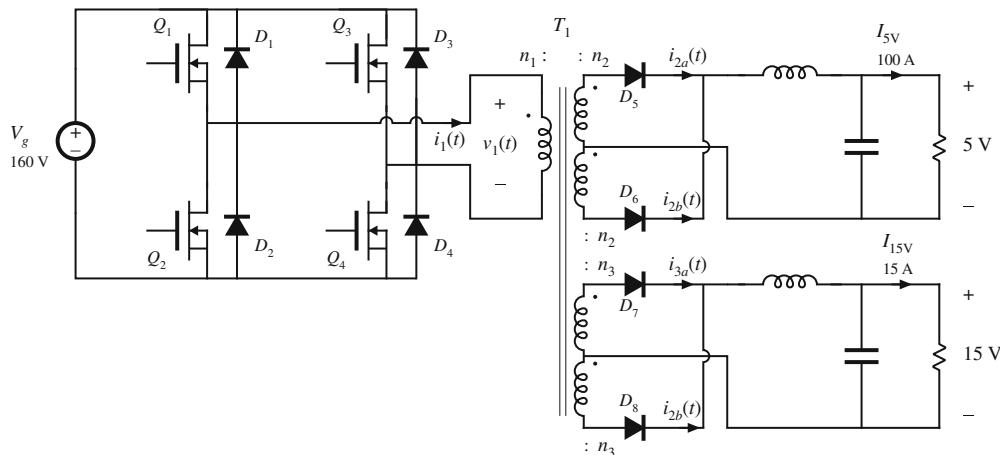


Fig. 12.8 Multiple-output full-bridge isolated buck converter example

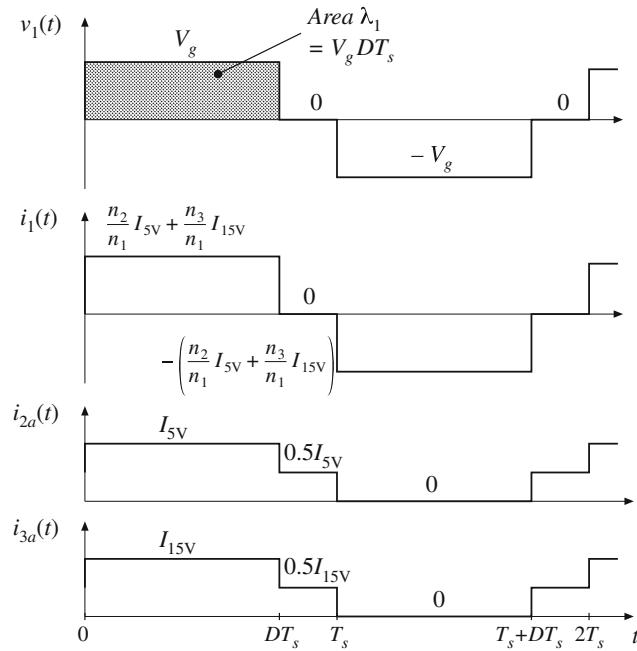


Fig. 12.9 Transformer waveforms, full-bridge converter example

The 5 V secondary windings carry rms current

$$I_2 = \frac{1}{2} I_{5V} \sqrt{1+D} = 66.1A \quad (12.37)$$

The 15 V secondary windings carry rms current

$$I_3 = \frac{1}{2} I_{15V} \sqrt{1+D} = 9.9A \quad (12.38)$$

The total rms winding current, referred to the primary, is

$$\begin{aligned} I_{tot} &= \sum_{\substack{\text{all 5} \\ \text{windings}}} \frac{n_j}{n_1} I_j = I_1 + 2 \frac{n_2}{n_1} I_2 + 2 \frac{n_3}{n_1} I_3 \\ &= 14.4A \end{aligned} \quad (12.39)$$

The core size is evaluated using Eq. (12.19):

$$\begin{aligned} K_{gfe} &\geq \frac{(1.724 \cdot 10^{-6})(800 \cdot 10^{-6})^2(14.4)^2(7.6)^{(2/2.6)}}{4(0.25)(4)^{(4.6/2.6)}} 10^8 \\ &= 0.00937 \end{aligned} \quad (12.40)$$

The EE core data of Appendix B lists the EE40 core with $K_{gfe} = 0.0118$ for $\beta = 2.7$. Evaluation of Eq. (12.16) shows that $K_{gfe} = 0.0108$ for this core, when $\beta = 2.6$. In any event, EE40 is the

smallest standard EE core size having $K_{gfe} \leq 0.00937$. The peak ac flux density is found by evaluation of Eq. (12.20), using the geometrical data for the EE40 core:

$$\Delta B = \left[10^8 \frac{(1.724 \cdot 10^{-6})(800 \cdot 10^{-6})^2(14.4)^2}{2(0.25)} \frac{(8.5)}{(1.1)(1.27)^3(7.7)} \frac{1}{(2.6)(7.6)} \right]^{(1/46)} \quad (12.41)$$

$$= 0.23 \text{ Tesla}$$

This flux density is less than the saturation flux density of approximately 0.35 Tesla. The primary turns are determined by evaluation of Eq. (12.21):

$$n_1 = 10^4 \frac{(800 \cdot 10^{-6})}{2(0.23)(1.27)} \quad (12.42)$$

$$= 13.7 \text{ turns}$$

The secondary turns are found by evaluation of Eq. (12.22). It is desired that the transformer have a 110:5:15 turns ratio, and hence

$$n_2 = \frac{5}{110} n_1 = 0.62 \text{ turns} \quad (12.43)$$

$$n_3 = \frac{5}{110} n_1 = 1.87 \text{ turns} \quad (12.44)$$

In practice, we might select $n_1 = 22$, $n_2 = 1$, and $n_3 = 3$. This would lead to a reduced ΔB with reduced core loss and increased copper loss. Since the resulting ΔB is suboptimal, the total power loss will be increased. According to Eq. (12.3), the peak ac flux density for the EE40 core will be

$$\Delta B = \frac{(800 \cdot 10^{-6})}{2(22)(1.27)} 10^4 = 0.143 \text{ Tesla} \quad (12.45)$$

The resulting core and copper loss can be computed using Eqs. (12.1) and (12.7):

$$P_{fe} = (7.6)(0.143)^{2.6}(1.27)(7.7) = 0.47 \text{ W} \quad (12.46)$$

$$P_{cu} = \frac{(1.724 \cdot 10^{-6})(800 \cdot 10^{-6})^2(14.4)^2}{4(0.25)} \frac{(8.5)}{(1.1)(1.27)^2} \frac{1}{(0.143)^2} 10^8 \quad (12.47)$$

$$= 5.4 \text{ W}$$

Hence, the total power loss would be

$$P_{tot} = P_{fe} + P_{cu} = 5.9 \text{ W} \quad (12.48)$$

Since this is 50% greater than the design goal of 4 W, it is necessary to increase the core size. The next larger EE core is the EE50 core, having K_{gfe} of 0.0284. The optimum ac flux density for this core, given by Eq. (12.3), is $\Delta B = 0.14$ T; operation at this flux density would require

$n_1 = 12$ and would lead to a total power loss of 2.3 W. With $n_1 = 22$, calculations similar to Eqs. (12.45) to (12.48) lead to a peak flux density of $\Delta B = 0.08$ T. The resulting power losses would then be $P_{fe} = 0.23$ W, $P_{cu} = 3.89$ W, $P_{tot} = 4.12$ W.

With the EE50 core and $n_1 = 22$, the fraction of the available window area allocated to the primary winding is given by Eq. (12.23) as

$$\alpha_1 = \frac{I_1}{I_{tot}} = \frac{5.7}{14.4} = 0.396 \quad (12.49)$$

The fraction of the available window area allocated to each half of the 5 V secondary winding should be

$$\alpha_2 = \frac{n_2 I_2}{n_1 I_{tot}} = \frac{5}{110} \frac{66.1}{14.4} = 0.209 \quad (12.50)$$

The fraction of the available window area allocated to each half of the 15 V secondary winding should be

$$\alpha_3 = \frac{n_3 I_3}{n_1 I_{tot}} = \frac{15}{110} \frac{9.9}{14.4} = 0.094 \quad (12.51)$$

The primary wire area A_{w1} , 5 V secondary wire area A_{w2} , and 15 V secondary wire area A_{w3} are then given by Eq. (12.24) as

$$\begin{aligned} A_{w1} &= \frac{\alpha_1 K_u W_A}{n_1} = \frac{(0.396)(0.25)(1.78)}{(22)} = 8.0 \cdot 10^{-3} \text{cm}^2 \\ &\Rightarrow \text{AWG\#19} \\ A_{w2} &= \frac{\alpha_2 K_u W_A}{n_2} = \frac{(0.209)(0.25)(1.78)}{(1)} = 930 \cdot 10^{-3} \text{cm}^2 \\ &\Rightarrow \text{AWG\#8} \\ A_{w3} &= \frac{\alpha_3 K_u W_A}{n_3} = \frac{(0.094)(0.25)(1.78)}{(3)} = 13.9 \cdot 10^{-3} \text{cm}^2 \\ &\Rightarrow \text{AWG\#16} \end{aligned} \quad (12.52)$$

It may be preferable to wind the 15 V outputs using two #19 wires in parallel; this would lead to the same area A_{w3} but would be easier to wind. The 5 V windings could be wound using many turns of smaller paralleled wires, but it would probably be easier to use a flat copper foil winding. If insulation requirements allow, proximity losses could be minimized by interleaving several thin layers of foil with the primary winding.

12.4 AC Inductor Design

The transformer design procedure of the previous sections can be adapted to handle the design of other magnetic devices in which both core loss and copper loss are significant. A procedure is outlined here for design of single-winding inductors whose waveforms contain significant high-frequency ac components (Fig. 12.10). An optimal value of ΔB is found, which leads to minimum total core plus copper loss. The major difference is that we must design to obtain a given inductance, using a core with an air gap. The constraints and a step-by-step procedure are briefly outlined below.

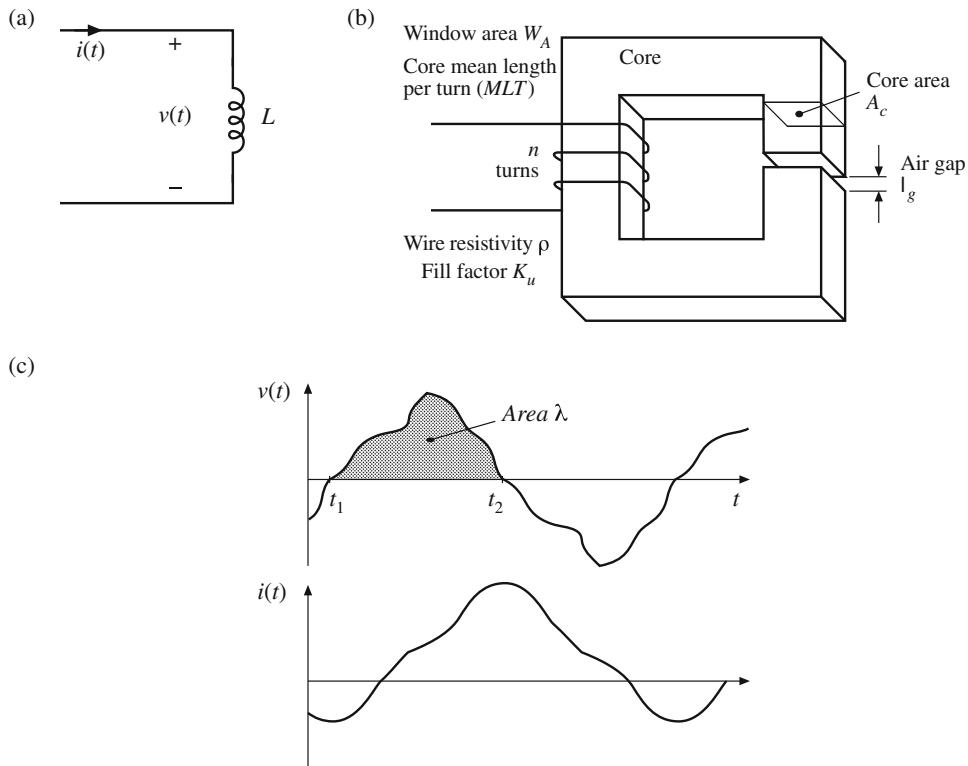


Fig. 12.10 Ac inductor, in which copper loss and core loss are significant: (a) definition of terminal quantities, (b) core geometry, (c) arbitrary terminal waveforms

12.4.1 Outline of Derivation

As in the filter inductor design procedure of the previous chapter, the desired inductance L must be obtained, given by

$$L = \frac{\mu_0 A_c n^2}{l_g} \quad (12.53)$$

The applied voltage waveform and the peak ac component of the flux density ΔB are related according to

$$\Delta B = \frac{\lambda}{2nA_c} \quad (12.54)$$

The copper loss is given by

$$P_{cu} = \frac{\rho n^2 (MLT)}{K_u W_A} I^2 \quad (12.55)$$

where I is the rms value of $i(t)$. The core loss P_{fe} is given by Eq. (12.1).

The value of ΔB that minimizes the total power loss $P_{tot} = P_{cu} + P_{fe}$ is found in a manner similar to the transformer design derivation. Equation (12.54) is used to eliminate n from the

expression for P_{cu} . The optimal ΔB is then computed by setting the derivative of P_{tot} to zero. The result is

$$\Delta B = \left[\frac{\rho \lambda^2 I^2}{2K_u} \frac{(MLT)}{W_A A_c^3 \ell_m} \frac{1}{\beta K_{fe}} \right]^{\left(\frac{1}{\beta+2}\right)} \quad (12.56)$$

which is essentially the same as Eq. (12.13). The total power loss P_{tot} is evaluated at this value of ΔB , and the resulting expression is manipulated to find K_{gfe} . The result is

$$K_{gfe} \geq \frac{\rho \lambda^2 I^2 K_{fe}^{(2/\beta)}}{2K_u (P_{tot})^{((\beta+2)/\beta)}} \quad (12.57)$$

where K_{gfe} is defined as in Eq. (12.16). A core that satisfies this inequality is selected.

12.4.2 First-Pass AC Inductor Design Procedure

The units of Sect. 12.2 are employed here.

1. Determine core size.

$$K_{gfe} \geq \frac{\rho \lambda^2 I^2 K_{fe}^{(2/\beta)}}{2K_u (P_{tot})^{((\beta+2)/\beta)}} 10^8 \quad (12.58)$$

Choose a core that is large enough to satisfy this inequality. If necessary, it may be possible to use a smaller core by choosing a core material having lower loss, that is, smaller K_{fe} .

2. Evaluate peak ac flux density.

$$\Delta B = \left[10^8 \frac{\rho \lambda^2 I^2}{2K_u} \frac{(MLT)}{W_4 A_c^3 \ell_m} \frac{1}{\beta K_{fe}} \right]^{\left(\frac{1}{\beta+2}\right)} \quad (12.59)$$

3. Number of turns.

$$n = \frac{\lambda}{2\Delta B A_c} 10^4 \quad (12.60)$$

4. Air gap length.

$$\ell_g = \frac{\mu_0 A_c n^2}{L} 10^{-4} \quad (12.61)$$

with A_c specified in cm^2 and ℓ_g expressed in meters. Alternatively, the air gap can be indirectly expressed via A_L (mH/1000 turns):

$$A_L = \frac{L}{n^2} 10^9 \quad (12.62)$$

5. Check for saturation.

If the inductor current contains a dc component I_{dc} , then the maximum total flux density B_{max} is greater than the peak ac flux density ΔB . The maximum total flux density, in Tesla, is given by

$$B_{max} = \Delta B + \frac{LI_{dc}}{nA_c} 10^4 \quad (12.63)$$

If B_{max} is close to or greater than the saturation flux density B_{sat} , then the core may saturate. The filter inductor design procedure of the previous chapter should then be used, to operate at a lower flux density.

6. Evaluate wire size.

$$A_w \leq \frac{K_u W_A}{n} \quad (12.64)$$

A winding geometry can now be determined, and copper losses due to the proximity effect can be evaluated. If these losses are significant, it may be desirable to further optimize the design by reiterating the above steps, accounting for proximity losses by increasing the effective wire resistivity to the value $\rho_{eff} = \rho_{cu} P_{cu}/P_{dc}$, where P_{cu} is the actual copper loss including proximity effects, and P_{dc} is the copper loss predicted when the proximity effect is ignored.

7. Check power loss.

$$\begin{aligned} P_{cu} &= \frac{\rho n(MLT)}{A_w} I^2 \\ P_{fe} &= K_{fe}(\Delta B)^\beta A_c \ell_m \\ P_{tot} &= P_{cu} + P_{fe} \end{aligned} \quad (12.65)$$

12.5 Summary

1. In a multiple-winding transformer, the low-frequency copper losses are minimized when the available window area is allocated to the windings according to their apparent powers, or ampere-turns.
2. As peak ac flux density is increased, core loss increases while copper losses decrease. There is an optimum flux density that leads to minimum total power loss. Provided that the core material is operated near its intended frequency, then the optimum flux density is less than the saturation flux density. Minimization of total loss then determines the choice of peak ac flux density.
3. The core geometrical constant K_{gfe} is a measure of the magnetic size of a core, for applications in which core loss is significant. In the K_{gfe} design method, the peak flux density is optimized to yield minimum total loss, as opposed to the K_g design method where peak flux density is a given specification.

PROBLEMS

- 12.1** Forward converter inductor and transformer design. The objective of this problem set is to design the magnetics (two inductors and one transformer) of the two-transistor, two-output forward converter shown in Fig. 12.11. The ferrite core material to be used for all three devices has a saturation flux density of approximately 0.3 T at 120°C. To provide a safety margin for your designs, you should use a maximum flux density B_{max} that is no greater than 75% of this value. The core loss at 100 kHz is described by Eq. (12.1), with the parameter values $\beta = 2.6$ and $K_{fe} = 50\text{W/T}^\beta\text{cm}^3$. Calculate copper loss at 100°C.

Steady-state converter analysis and design. You may assume 100% efficiency and ideal lossless components for this section.

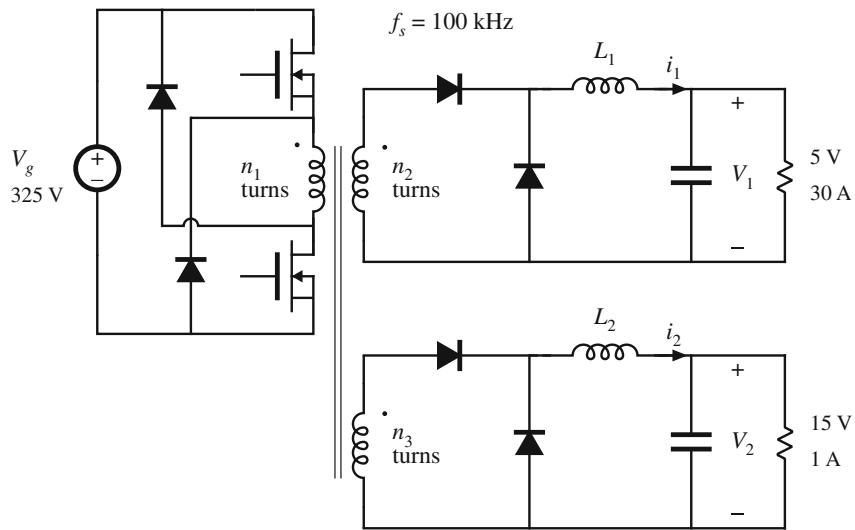


Fig. 12.11 Two-output forward converter of Problem 12.1

- (a) Select the transformer turns ratios so that the desired output voltages are obtained when the duty cycle is $D = 0.4$.
- (b) Specify values of L_1 and L_2 such that their current ripples Δi_1 and Δi_2 are 10% of their respective full-load current dc components I_1 and I_2 .
- (c) Determine the peak and rms currents in each inductor and transformer winding.

Inductor design. Allow copper loss of 1 W in L_1 and 0.4 W in L_2 . Assume a fill factor of $K_u = 0.5$. Use ferrite EE cores—tables of geometrical data for standard EE core sizes are given in Appendix B. Design the output filter inductors L_1 and L_2 . For each inductor, specify:

- (i) EE core size
- (ii) Air gap length
- (iii) Number of turns
- (iv) AWG wire size

Transformer design. Allow a total power loss of 1 W. Assume a fill factor of $K_u = 0.35$ (lower than for the filter inductors, to allow space for insulation between the windings). Use a ferrite EE core. You may neglect losses due to the skin and proximity effects, but you should include core and copper losses. Design the transformer, and specify the following:

- (i) EE core size
- (ii) Turns n_1 , n_2 , and n_3
- (iii) AWG wire size for the three windings

Check your transformer design:

- (iv) Compute the maximum flux density. Will the core saturate?
- (v) Compute the core loss, the copper loss of each winding, and the total power loss

12.2 A single-transistor forward converter operates with an input voltage $V_g = 160$ V, and supplies two outputs: 24 V at 2 A, and 15 V at 6 A. The duty cycle is $D = 0.4$. The turns ratio between the primary winding and the reset winding is 1:1. The switching frequency is 100 kHz. The core material loss equation parameters are $\beta = 2.7$, $K_{fe} = 50$. You may assume a fill factor of 0.25. Do not allow the core maximum flux density to exceed 0.3 T. Design a transformer for this application, having a total power loss no greater than 1.5 W at 100°C. Neglect proximity losses. You may neglect the reset winding. Use a ferrite PQ core. Specify: core size, peak ac flux density, wire sizes, and number of turns for each winding. Compute the core and copper losses for your design.

12.3 Flyback/SEPIC transformer design. The “transformer” of the flyback and SEPIC converters is an energy storage device, which might be more accurately described as a multiple-winding inductor. The magnetizing inductance L_p functions as an energy-transferring inductor of the converter, and therefore the “transformer” normally contains an air gap. The converter may be designed to operate in either the continuous or discontinuous conduction mode. Core loss may be significant. It is also important to ensure that the peak current in the magnetizing inductance does not cause saturation.

A flyback transformer is to be designed for the following two-output flyback converter application:

Input:	160 Vdc
Output 1:	5 Vdc at 10 A
Output 2:	15 Vdc at 1 A
Switching frequency:	100 kHz
Magnetizing inductance L_p :	1.33 mH, referred to primary
Turns ratio:	160: 5: 15
Transformer power loss:	Allow 1 W total

- (a) Does the converter operate in CCM or DCM? Referred to the primary winding, how large are (i) the magnetizing current ripple Δi , (ii) the magnetizing current dc component I , and (iii) the peak magnetizing current I_{pk} ?
- (b) Determine (i) the rms winding currents, and (ii) the applied primary volt-seconds λ_1 . Is λ_1 proportional to I_{pk} ?
- (c) Modify the transformer and ac inductor design procedures of this chapter, to derive a general procedure for designing flyback transformers that explicitly accounts for both core and copper loss, and that employs the optimum ac flux density that minimizes the total loss.
- (d) Give a general step-by-step design procedure, with all specifications and units clearly stated.
- (e) Design the flyback transformer for the converter of part (a), using your step-by-step procedure of Part (d). Use a ferrite EE core, with $\beta = 2.7$ and $K_{fe} = 50\text{W/T}^{\beta}\text{cm}^3$. Specify: core size, air gap length, turns, and wire sizes for all windings.
- (f) For your final design of part (e), what are (i) the core loss, (ii) the total copper loss, and (iii) the peak flux density?

12.4 Over the intended range of operating frequencies, the frequency dependence of the core loss coefficient K_{fe} of a certain ferrite core material can be approximated using a monotonically increasing fourth-order polynomial of the form

$$K_{fe}(f) = K_{fe0} \left(1 + a_1 \left(\frac{f}{f_0} \right) + a_2 \left(\frac{f}{f_0} \right)^2 + a_3 \left(\frac{f}{f_0} \right)^3 + a_4 \left(\frac{f}{f_0} \right)^4 \right)$$

where K_{fe0} , a_1 , a_2 , a_3 , a_4 , and f_0 are constants. In a typical converter transformer application, the applied primary volt-seconds λ_1 varies directly with the switching period $T_s = 1/f$. It is desired to choose the optimum switching frequency such that K_{gfe} , and therefore the transformer size, are minimized.

- (a) Show that the optimum switching frequency is a root of the polynomial

$$1 + a_1 \left(\frac{\beta - 1}{\beta} \right) \left(\frac{f}{f_0} \right) + a_2 \left(\frac{\beta - 2}{\beta} \right) \left(\frac{f}{f_0} \right)^2 + a_3 \left(\frac{\beta - 3}{\beta} \right) \left(\frac{f}{f_0} \right)^3 + a_4 \left(\frac{\beta - 4}{\beta} \right) \left(\frac{f}{f_0} \right)^4$$

Next, a core material is chosen whose core loss parameters are

$$\begin{aligned} \beta &= 2.7 & K_{fe0} &= 7.6 \\ f_0 &= 100 \text{ kHz} \\ a_1 &= -1.3 & a_2 &= 5.3 \\ a_3 &= -0.5 & a_4 &= 0.075 \end{aligned}$$

The polynomial fits the manufacturer's published data over the range 10 kHz < f < 1 MHz.

- (b) Sketch K_{fe} vs. f .
(c) Determine the value of f that minimizes K_{gfe} .
(d) Sketch $K_{gfe}(f)/K_{gfe}(100 \text{ kHz})$, over the range $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$. How sensitive is the transformer size to the choice of switching frequency?

- 12.5** Transformer design to attain a given temperature rise. The temperature rise ΔT of the center leg of a ferrite core is directly proportional to the total power loss P_{tot} of a transformer: $\Delta T = R_{th}P_{tot}$, where R_{th} is the thermal resistance of the transformer under given environmental conditions. You may assume that this temperature rise has minimal dependence on the distribution of losses within the transformer. It is desired to modify the K_{gfe} transformer design method, such that temperature rise ΔT replaces total power loss P_{tot} as a specification. You may neglect the dependence of the wire resistivity ρ on temperature.

- (a) Modify the n -winding transformer K_{gfe} design method, as necessary. Define a new core geometrical constant K_{th} that includes R_{th} .
(b) Thermal resistances of ferrite EC cores are listed in Sect. B.3 of Appendix B. Tabulate K_{th} for these cores, using $\beta = 2.7$.
(c) A 750 W single-output full-bridge isolated buck dc–dc converter operates with converter switching frequency $f_s = 200 \text{ kHz}$, dc input voltage $V_g = 400 \text{ V}$, and dc output voltage $V = 48 \text{ V}$. The turns ratio is 6:1. The core loss equation parameters at 100 kHz are $K_{fe} = 10 \text{ W/T}^\beta \text{cm}^3$ and $\beta = 2.7$. Assume a fill factor of $K_u = 0.3$. You may neglect proximity losses. Use your design procedure of parts (a) and (b) to design a transformer for this application, in which the temperature rise is limited to 20°C . Specify: EC core size, primary and secondary turns, wire sizes, and peak ac flux density.