

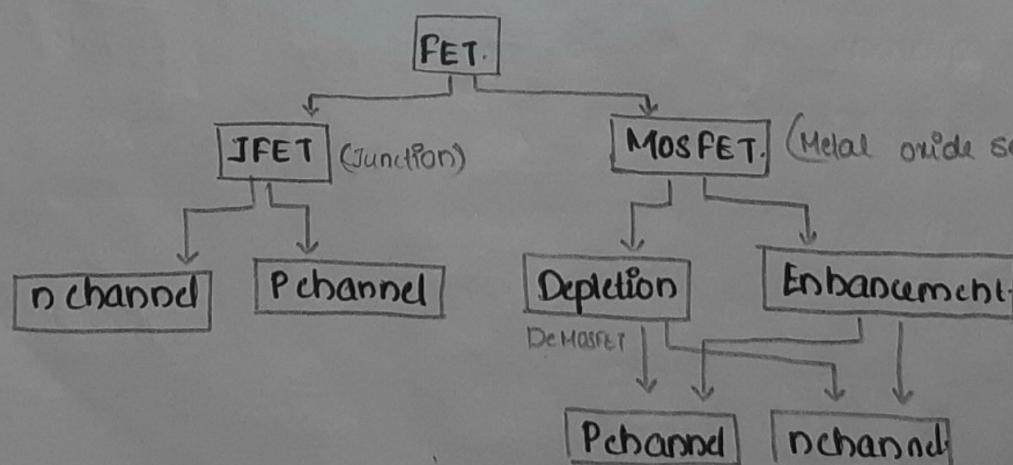
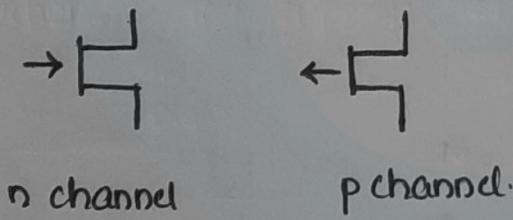
19.9.20

## Field effect transistor (FET).

It is a semiconductor device which depends for its operation on the control of current by an electric field.

Advantages of FET than BJT

- \* current flow due to majority carriers only not due to holes and electrons like BJT.
- \* immune to radiation
- \* high input resistance
- \* less noisy than BJT
- \* high thermal stability



# Construction and characteristics of JFET

It is a three terminal device capable of controlling the current between the other two.

3 terminals:

→ Drain (D)

→ source (S)

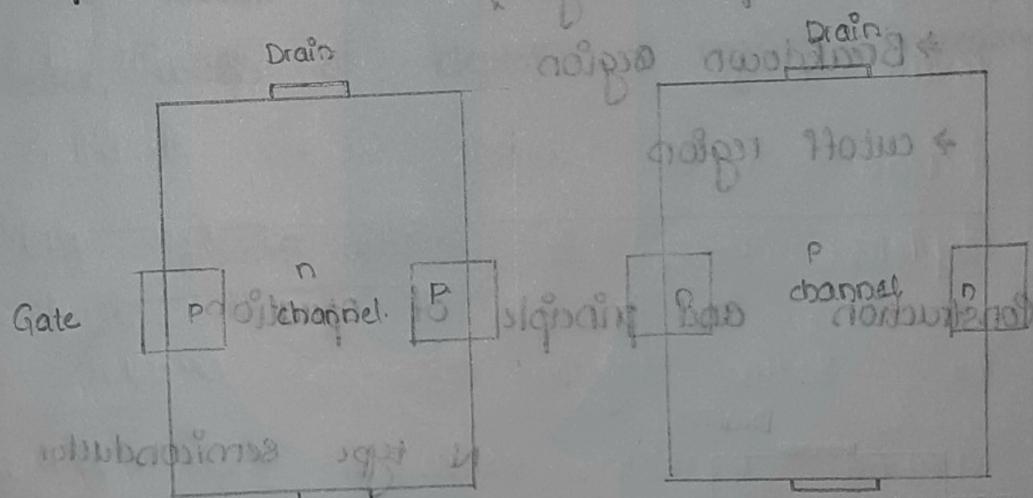
→ Gate (G)

## Construction:

2 types:

1. n-channel (mostly used)

2. p-channel



Gate

Drain

Drain

n channel

p channel

p channel

control

Observe

source

Source

Source

Source

Source

Source

Source

Source

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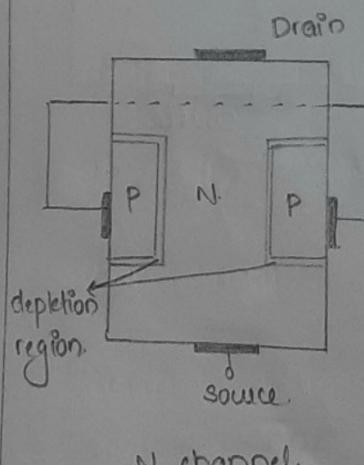
Source

## Difference between FET and BJT

FET	BJT
* voltage control device	* current controlled device
* high input impedance	* low input impedance
* unipolar device	* bipolar device
* less sensitive to temperature	* highly sensitive to temperature
* regions → Ohmic region / linear region (behaves like ordinary resistor). → Pinch off → Pinch off region / saturation or amplification region) → Breakdown region. → cutoff region	* active, saturation, cutoff and reverse active.

Q. 9. a)

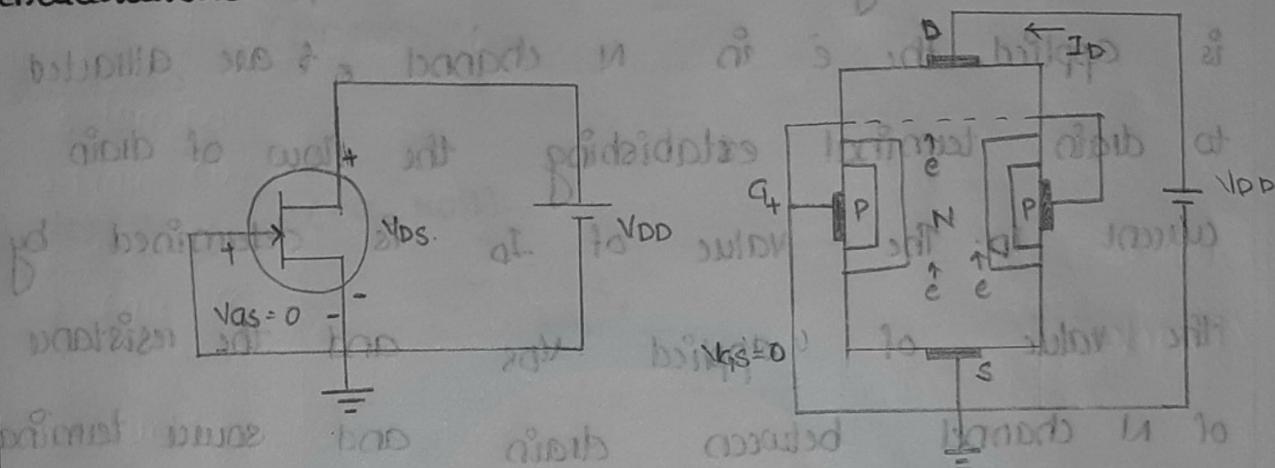
### Construction and principle of operation



N type semiconductor forms a channel between embedded layers of P type material. Therefore 2 P-N junctions are formed between the semiconductor channel and the embedded semiconductor layers. Ohmic contacts are made at the top and bottom

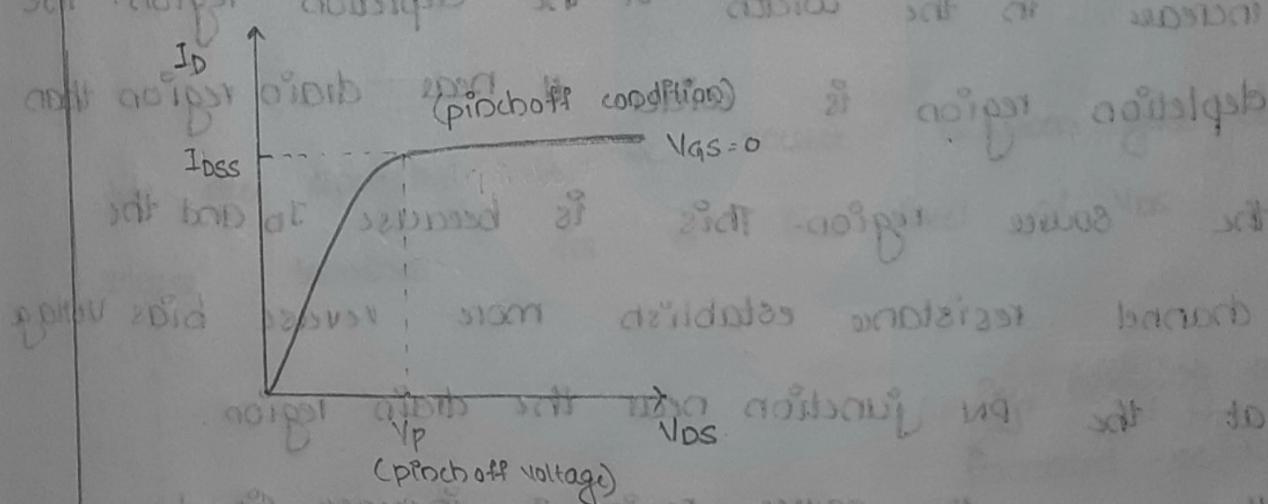
of the channel and are referred to as drain and source terminals.

Characteristic curve



① N channel JFET with  $V_{GS} = 0$  and positive value of  $V_{DS}$

since it is reverse biased and as the voltage drop increases, width of depletion region increases



After  $V_P$ ,  $I_D$  becomes constant

This current is referred as drain to source current

for short circuit connection between gate and source and the voltage is called pinchoff region.

$V_{DS} > V_P \rightarrow I_D$  constant

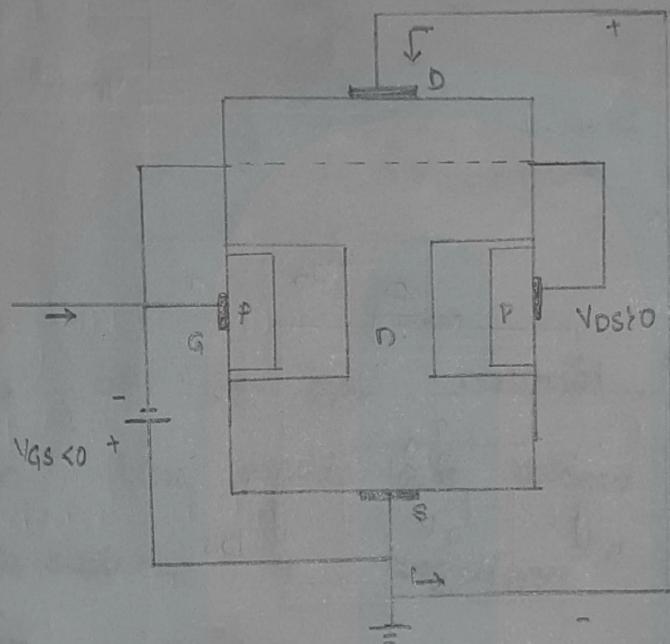
Let us consider when both a positive drain source voltage  $V_{DS}$  is applied to JFET in which gate source & bias voltage is shorted and  $V_{GS} = 0$ . When  $V_{DS}$  is applied, the electrons in N channel are attracted to drain terminal establishing the flow of drain current  $I_D$ . The value of  $I_D$  is determined by the value of applied  $V_{DS}$  and the resistance of N channel between drain and source terminal.

According to the flow of  $I_D$ , there is a uniform voltage drop across the channel resistance, which reverse biases the two P-N junctions. This results in increase in the width of the depletion region. The depletion region is wider near drain region than the source region. This is because  $I_D$  and the channel resistance establish more reverse bias voltage at the PN junction near the drain region than near the source region.  $I_D$  increases linearly with increase in  $V_{DS}$  till the  $V_{DS}$  reaches a value when the saturation effect sets in. The value of  $V_{DS}$  at which the saturation effect sets in is referred to as pinch off voltage ( $V_P$ ).

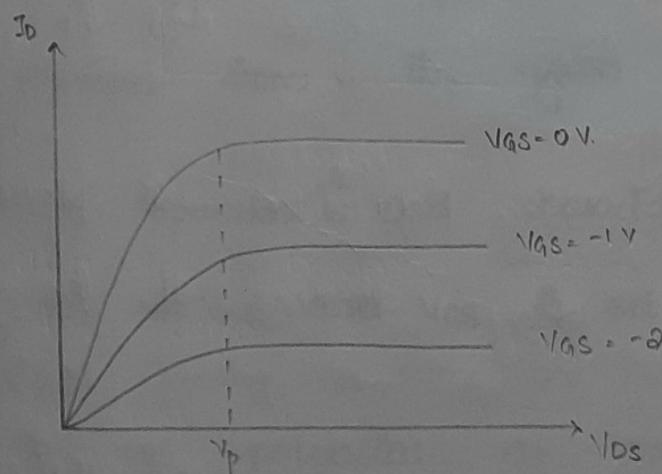
When  $V_{DS}$  reaches up, the value of  $I_D$  does not change with further increase in the value of  $V_{DS}$ . This condition is referred to as pinch off condition.

Q. 20  
@  $V_{GS} < 0$

(-ve volt).

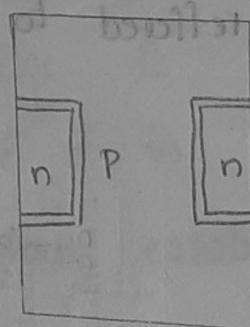


We are applying a -ve source between gate and source terminal for a low level of  $V_{DS}$ .



By applying an increased -ve voltage, we are able to reach saturation level more fast.

P channel JFET

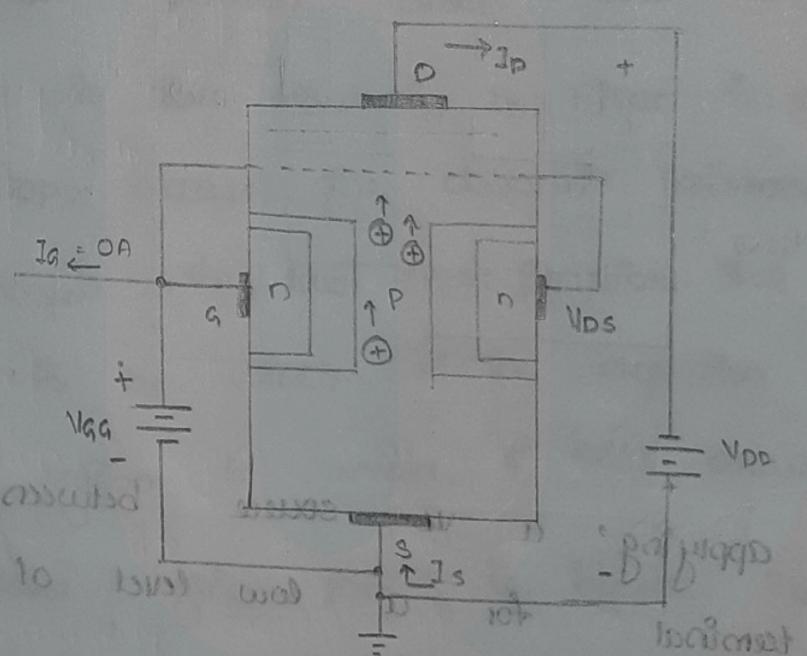


(construction similar to

$N$  channel)

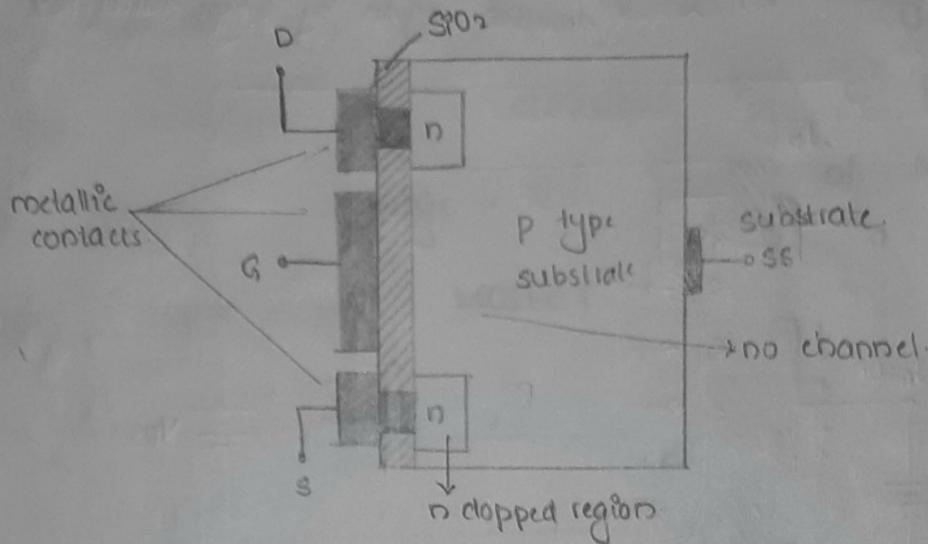
(SLOW M-)

## Characteristics



( same as  $n$  type)

## Enhancement type p-n-p MOSFET

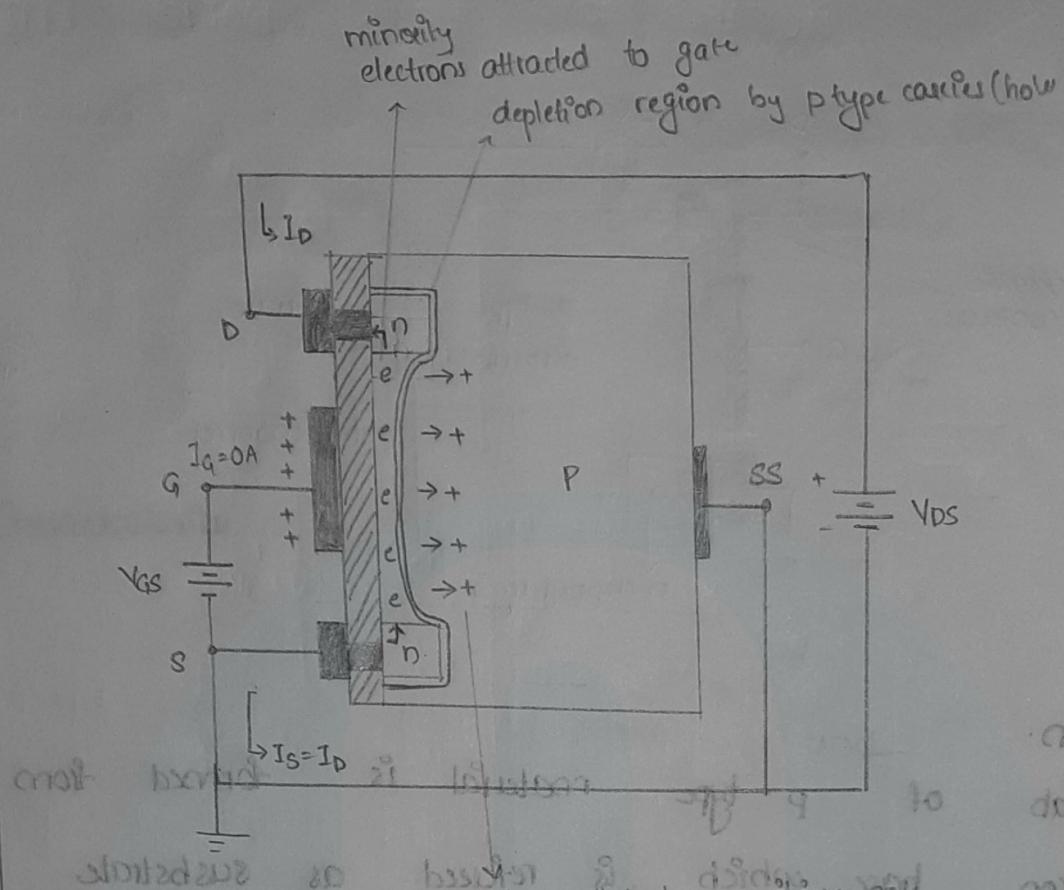


## Construction.

- \* a slab of p type material is formed from a silicon base, which is referred as substrate
- \* The substrate is sometimes internally connected to source terminal.
- \* The source and drain terminals are connected through metallic contacts to n doped regions.
- \*  $\text{SiO}_2$  layer is present to isolate the gate metal from the region between drain and source.

## Basic operation and characteristics.

- \* both  $V_{DS}$  and  $V_{GS}$  is set to a positive voltage ( $> 0$ ) (keeping  $V_{DS}$  same and increasing  $V_{GS}$ )
- \* The +ve potential at gate will repel the holes in the p substrate along the edge of  $\text{SiO}_2$  layer to leave the area and enter deeper regions of

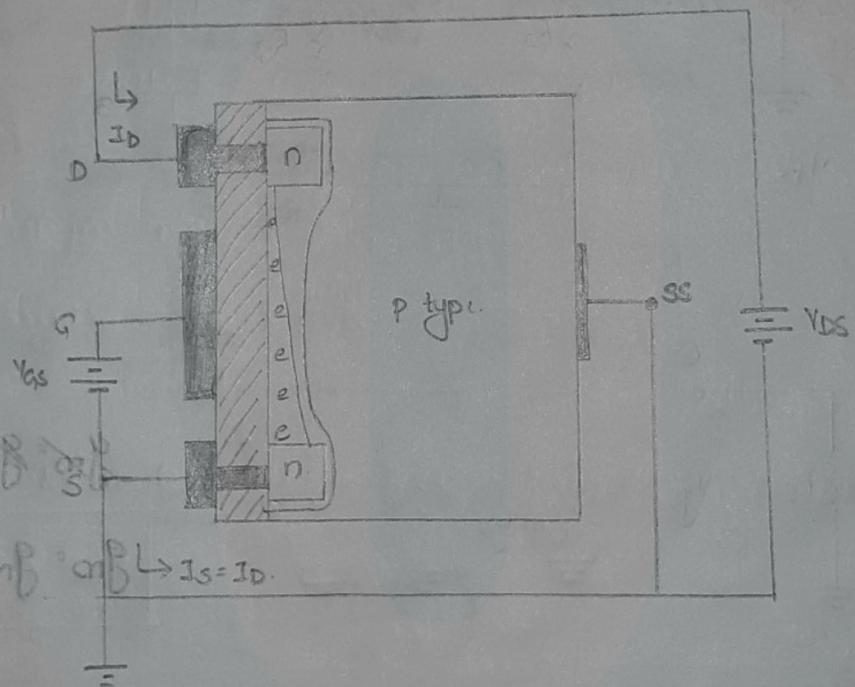


- \* A depletion region near  $\text{SiO}_2$  layer is formed which is free of holes. The electrons in P substrate (minority carriers) will be attracted to positive gate bias and accumulate in the region near the surface of  $\text{SiO}_2$  layer.
- \* The  $\text{SiO}_2$  layer and insulating quantities will prevent the -ve carriers from being absorbed at the gate terminal.
- \* As  $V_{GS}$  increases in magnitude, the concentration of e- in  $\text{SiO}_2$  surface increases until the induced n-type region can support a measurable flow between

drain and source

- \* The level of  $V_{GS}$  that results in significant increase in drain current ( $I_D$ ) is the threshold voltage.
- \* since the channel is enhanced by a positive gate to source voltage, this type of MOSFET is called an enhancement MOSFET.

(keeping  $V_{DS}$  same and varying  $V_{GS}$ )

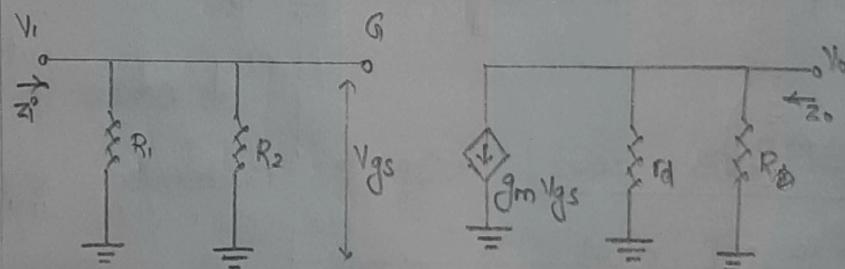
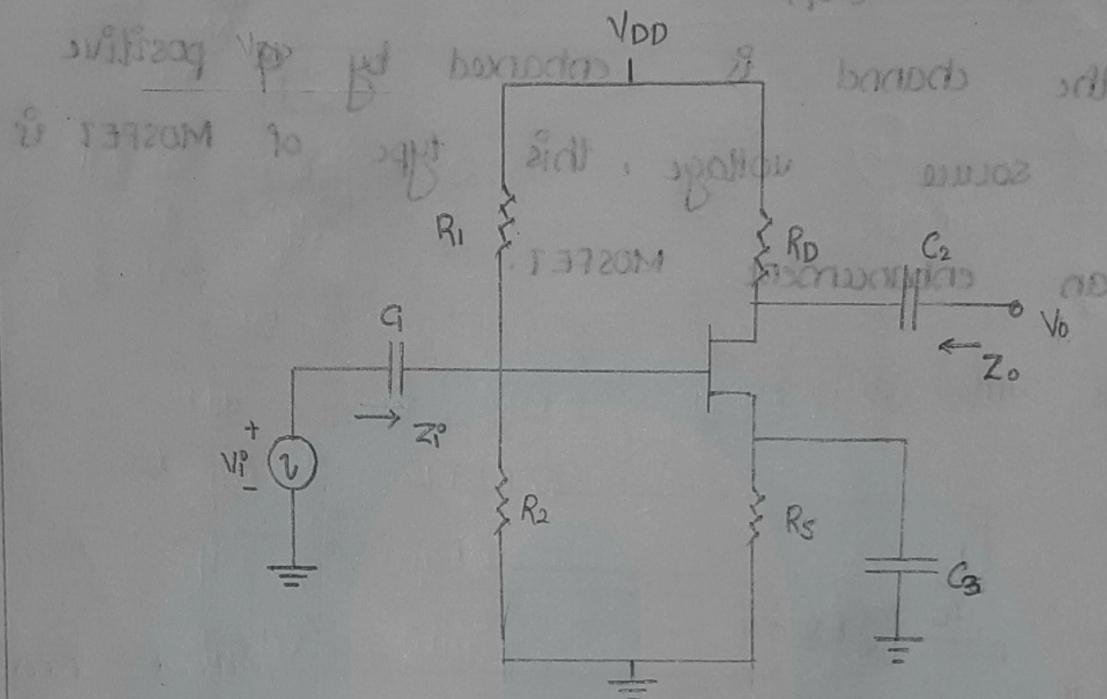


If  $V_{GS}$  is held fixed, say 8V and  $V_{DS}$  is increased from -5V to -16V and  $V_{DG}$  will drop from 17V to -3V and gate will become less and less positive with drain.

$$(0.8/16) \cdot 10^6 = 50$$

26.9.20

## JFET VOLTAGE DIVIDER CONFIGURATION.



$$g_{ds} = g_{mo} \times k$$

$$g_{mo} = g_{mo} \left( 1 - \frac{V_{GS}}{V_P} \right)$$

$$g_{mo} = \frac{2ID_{SS}}{IV_P}$$

$$A_V = \frac{V_D}{V_I}$$

$$Z_1 = R_1 \parallel R_2$$

$$= -\frac{g_m V_{GS} (r_d \parallel R_D)}{V_{GS}}$$

$$Z_0 = r_d \parallel R_D$$

$$A_V = -\frac{g_m (r_d \parallel R_D)}{V_{GS}}$$

Determine input impedance, output impedance and  $V_o$  for

the network if  $V_i = 28mV$ ,  $R_1 = 82M\Omega$ ,  $R_2 = 11M\Omega$ ,  $R_D = 2k\Omega$

$$R_s = 610\Omega, I_{DSS} = 10mA, V_p = -3V, r_d = 100k\Omega$$

$$Z_i = \frac{1}{82 \times 10^3} + \frac{1}{11} = \underline{\underline{108M\Omega}} = \frac{1}{R_1} + \frac{1}{R_2} = 9.7M\Omega$$

$$Z_o = \frac{1}{2 \times 10^3} + \frac{1}{100 \times 10^3} = \underline{\underline{50k\Omega || 1.96k\Omega}}$$

$$V_o = -g_m V_{AS} (r_d || R_D)$$

$$g_m = g_{mo} \times \left( 1 - \frac{V_{AS}}{|V_p|} \right)$$

$$g_{mo} = \frac{2I_{DSS}}{|V_p|}$$

$$= \underline{\underline{8 \times 10^{-3}}}$$

$$g_m = 8 \times 10^{-3} \times \left( 1 - \frac{20 \times 10^{-3}}{3} \right)$$

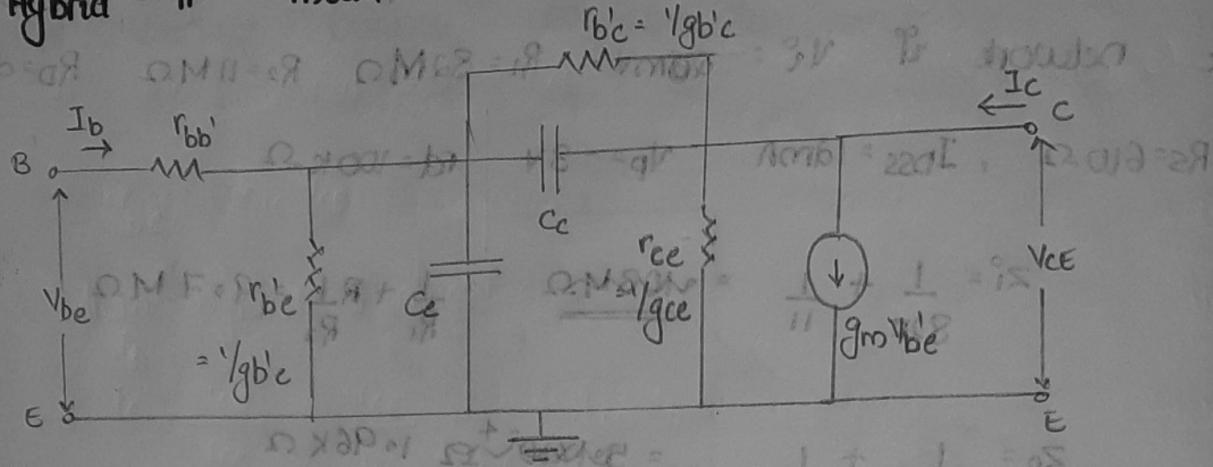
$$= \underline{\underline{7.9 \times 10^{-3}}}$$

$$V_o = -g_m V_{AS} (r_d || R_D)$$

$$= -7.9 \times 10^{-3} \times 20 \times 10^{-3} \times 1.96 \times 10^3$$

$$= \underline{\underline{-309V}}$$

# Hybrid Pi model for CE transistor amplifier



$r_{bb'}$  - base spreading resistance

$g_{be}$  - conductance between B' and E

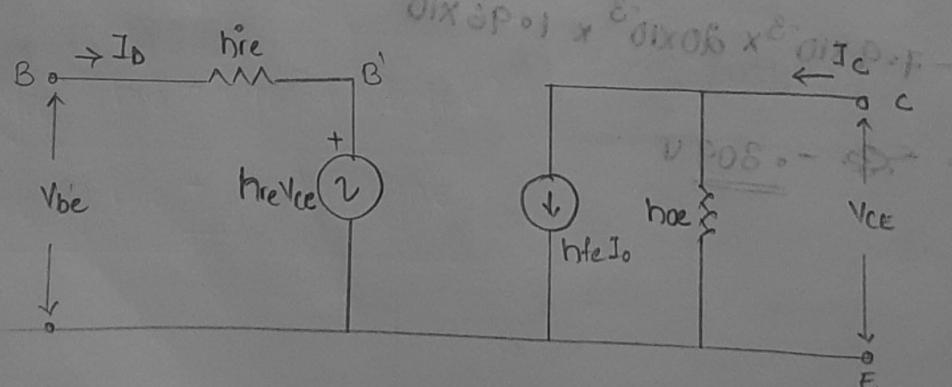
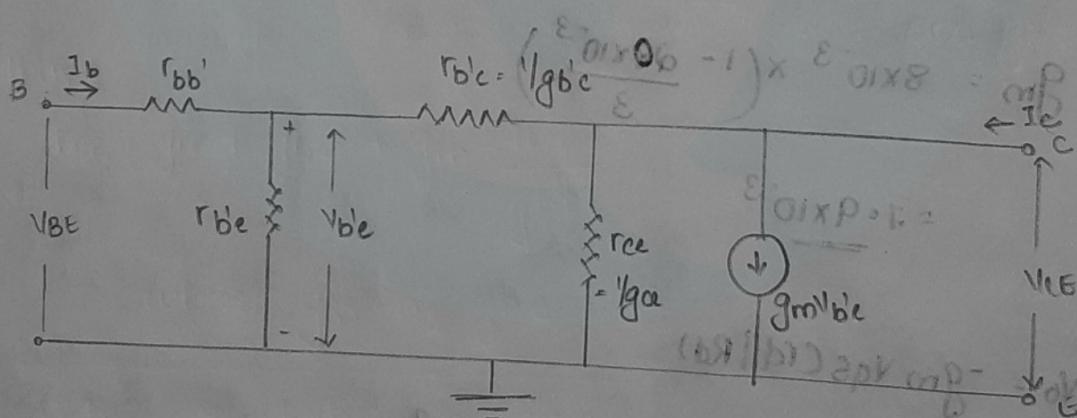
$g_{bc}$  - conductance between B' and C

$g_m V_{be}'$  - current between C and E

$C_c$  - collector junction barrier capacitance

$C_e$  - diffusion capacitance between B' and E

for deriving the expression all capacitors are removed



Q. 9. d)

$$Z_0 = r_{bb'} + (r_{b'e} \parallel r_{bc}) \quad (\text{base spreading resistance})$$

in terms of h. orgo no. electronic Engg. at II

$$h_{ie} = r_{bb'} + (r_{b'e} \parallel r_{bc})$$

as  $r_{bc} \gg r_{b'e}$

$$h_{ie} = \frac{r_{bb'}}{r_{bb'} + r_{b'e}}$$

conductance between terminals B' and c or feedback conductance ( $g_{bc}$ )

$\frac{h_{re}}{h_{ie}} \Rightarrow$  reverse voltage gain if the input terminals are open,  $I_b = 0$

$$h_{re} = \frac{V_{b'e}}{V_{cc}}$$

$$(r_{b'e} + r_{bc}) \cdot h_{re} = r_{b'e}$$

$$r_{b'e} (1 - h_{re}) = h_{re} \cdot r_{b'e}$$

since the value of  $h_{re} \ll 1$

$$r_{b'e} = h_{re} \cdot r_{b'e}$$

$$\frac{1}{g_{bc}} = h_{re} \cdot \frac{1}{g_{bc}}$$

$$g_{bc} = \frac{g_{bc}}{h_{re} \cdot g_{bc}}$$

Conductance between terminals C and E ( $g_{ce}$ )

If the input terminals are open circuit ( $I_b = 0$ )

$$V_{be}' = h_{re} V_{ce}$$

from hybrid  $\pi$  model,

$$I_c = \frac{V_{ce}}{r_{ce}} + \frac{V_{ce}}{r_{b'e} + r_{b'c}} + g_m V_{be}'$$

$$h_{oe} = \frac{I_c}{V_{ce}}$$

$$= \frac{1}{r_{ce}} + \frac{1}{r_{b'e} + r_{b'c}} + g_m \frac{V_{be}'}{V_{ce}}, \text{ where } h_{re} = \frac{V_{be}'}{V_{ce}}$$

$$\therefore h_{oe} = \frac{1}{r_{ce}} + \frac{1}{r_{b'e} + r_{b'c}} + g_m h_{re}$$

writing in terms of conductance,

$$\therefore h_{oe} = g_{ce} + g_{b'e} + g_{b'c} + g_m \frac{g_{b'c}}{g_{b'e}}$$

thus

$$h_{oe} = g_{ce} + g_{b'c} + g_m \frac{g_{b'c}}{g_{b'e}}$$

$$\text{where } g_m = h_{fe} g_{b'e}$$

$$\therefore h_{oe} = g_{ce} + g_{b'c} + h_{fe} g_{b'c}$$

$$+ g_{ce} = h_{oe} - (g_{b'c} + h_{fe} g_{b'c})$$

$$g_{ce} = h_{oe} - (1 + h_{fe}) g_{b'c}$$

Conductance between B' and E or input conductance ( $g_{b'e}$ )

as the value of resistance  $r_{b'e} \gg r_{b'e}$  most of the current flows through  $r_{b'e}$  and value of voltage  $V_{b'e}$  is given by

$$V_{b'e} \approx I_B \times r_{b'e}$$

The short circuit collector current  $I_C$

$$I_C = g_m \times V_{b'e}$$

$$I_C = g_m \times I_B \times r_{b'e}$$

but  $b_{pe} = \frac{I_C}{I_B}$  with  $V_{CE} = \text{constant}$

$$I_C = b_{pe} \times g_m I_B \times r_{b'e}$$

$$b_{pe} = \frac{g_m r_{b'e}}{I_B} \Rightarrow b_{pe} = \frac{g_m}{I_B} \times r_{b'e}$$

i.e., but  $g_m = b_{pe} g_{b'e}$

$$\therefore b_{pe} = \frac{g_m}{I_B}$$

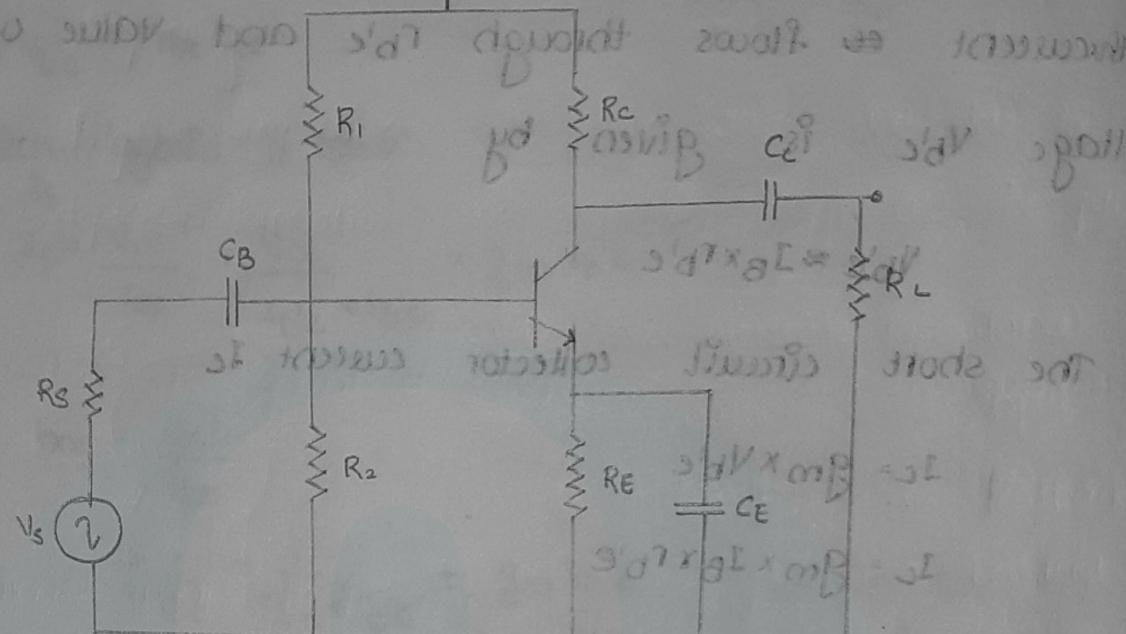
$$\therefore g_{b'e} = \frac{g_m}{b_{pe}}$$

$$\therefore g_{b'e} = g_m \times r_{b'e}$$

30.9.09

# Frequency response of a CE amplifier

## RC coupled amplifier



~~(AC)~~ Single stage amplifier

$R_1$  and  $R_2$  are biasing resistors

$R_E$  provided for temperature stability

$R_E$  and  $R_L$  acts as load

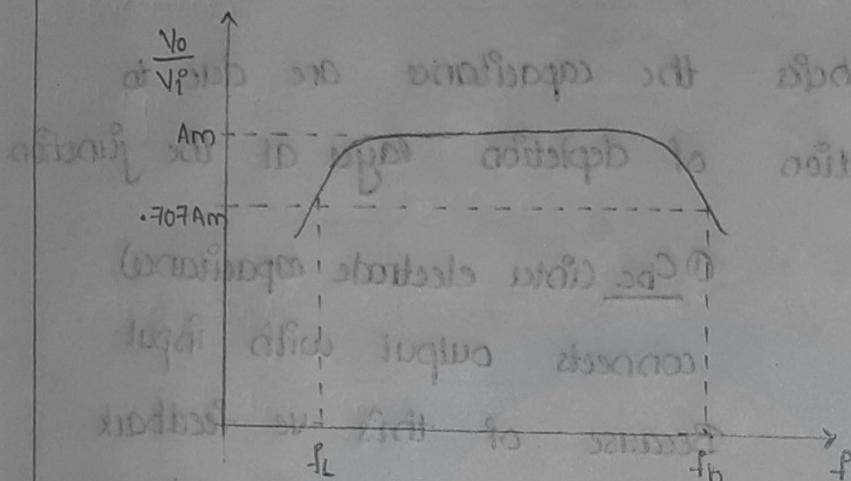
The capacitors  $C_B$  and  $C_C$  are coupling capacitor and  $C_E$  is bypass capacitor which provide easy bypass for AC signal at emitter node.

This is also known as RC coupled amplifier

If one or more stages is to be connected, we can connect the output terminal of first stage to the input terminal of second stage.

Since the coupling is done by resistors and capacitors, the circuit is named as RC coupled

amplifier.

Frequency response

Frequency response gives that gain of amplifier varies with signal frequencies. The response is gain for different signal frequencies. The response is gain uniform (constant) only in middle frequency range.

The gain in this frequency range is known as mid band gain (Am).

Reduction in gain at very low and high frequencies.

## a) Low frequency.

$$X_C = \frac{1}{2\pi f C}$$

- \* The reactance of coupling capacitors  $C_B$  and  $C_E$  are very high at low frequencies. So there is an increase in the voltage drop across it. Thus the gain varies.

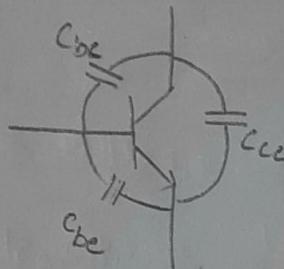
- \* The bypass capacitor cannot act as a perfect bypass capacitor at low frequency. Therefore a small amount

of -ve feedback is introduced which further reduces the gain.

negative feedback

### b. High frequency

- \* at high frequencies the capacitance are due to the depletion formation of depletion layer at the junction.



①  $C_{bc}$  (base electrode capacitance)

connects output with input.

Because of this -ve feedback occurs and gain is reduced.

The feedback effect increases with increase in frequency ( $\text{since } f_c \propto \frac{1}{X_C}$ ) because capacitive reactance decreases.

### ② $C_{be}$

It occurs a low impedance path at input side

at high frequency. This decreases the input impedance of the device and consequently effective input signal is reduced.

and thus gain falls.

### ③ $C_{ce}$

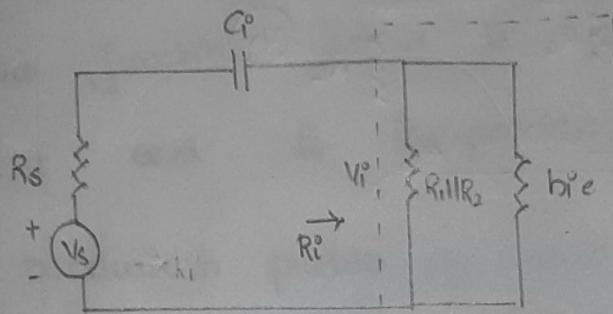
This produces shunting effect at high frequency

on output side.  $C_{bc}$  is most important capacitance

because feedback takes place from output to input and is called as Miller effect.

Low frequency response of BJT amplifier to JFET Q

### ① Effect of input coupling capacitor.



(draw the main diagram too)

$$R_i^o = R_1 \parallel R_2 \parallel h_{ie}$$

$$V_P = V_S \times \frac{R_i^o}{R_S + R_i^o - jX_C} \quad (\text{by voltage divider rule})$$

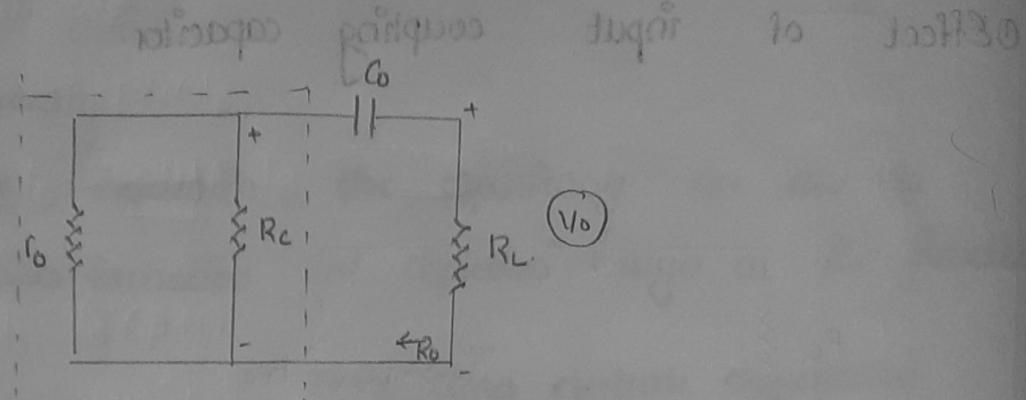
at mid and very high frequency, the reactance of capacitors,  $C_1$  and  $C_0$  will be sufficiently small to neglect. Therefore the input voltage is given by,

$$V_P = \frac{V_S \times R_i^o}{R_S + R_i^o}$$

At cut off frequency  $f_{C1}$  ( $f_L$ ) the voltage will be at the time of the original gain. Assuming that  $C_1$  is the only capacitance affecting the low frequency response curve of the circuit, we have

$$f_L = \frac{1}{2\pi (R_S + R_P) C_1}$$

## Effect of output coupling capacitor



$$R_o = R_C \parallel r_o$$

$$f_{C_0} / f_{\text{th}} = \frac{1}{2\pi (R_o + R_L) C_0}$$

The output voltage  $V_o$  will be  $\frac{1}{2}$  of its mid band value. Assuming that  $C_0$  is the only capacitive element controlling the low frequency response.

### Effect of bypass capacitor

Effect of bypass capacitor  $C_E$  can be explained by considering at low frequency the capacitor  $C_E$  acts as open circuit and the resistor  $R_E$  appears in gain eqn resulting in 0. As frequency increases the reactance of  $C_E$  decreases, resulting in decrease in value of parallel impedance of resistor  $R_E$  and  $C_E$ . The gain is max. when impedance of capacitor  $C_E$  reduces very much that it can be considered as a short circuit.

$C_C$  and  $C_E$  (Balance of hybrid  $\pi$  model)

$C_C$  is collector junction capacitance and is the output capacitance with the input current zero.

$C_E$  is the depletion capacitance of forward biased emitter junction and is proportional to emitter current and is independent of temperature.

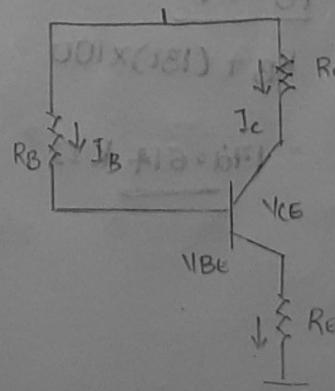
Gain bandwidth product (RC coupled amplifier)

It is the frequency  $f_T$  is the frequency at which the magnitude of short circuit current gain of  $C_E$  amplifier becomes unity. As the value of  $h_{fe}$  greater than 1 the magnitude of current gain AP becomes unity at the frequency given by the product of  $h_{fe}$  and  $f_B$  and

$$f_T = \frac{g_m}{2\pi C_C C_E} \quad (\text{transconductance})$$

at  $C_C + C_E$

? Design an emitter bias circuit.  $I_C = 10mA$   $V_{CE} = 4V$   
 Q.  $V_{CC} = 15V$   $\frac{R_C}{R_E} = 10$ . It is given that  $\beta = 130$  and  $V_{BE} = 0.7V$



$$\begin{aligned} R_C &= 1K \\ R_B &= 172.073 \\ R_E &= 0.1K \end{aligned}$$

$$V_{CC} = I_C R_B + V_B$$

$$I_C = \beta I_B$$

$$10 \times 10^{-3} = 130 \times I_B$$

$$I_B = 7.7 \times 10^{-5} \text{ A}$$

$$I_E = I_B (\beta + 1)$$

$$= 1.1 \times 10^{-2} \text{ A}$$

$$V_{CE} - I_C R_E - V_{BE} - I_E R_E = 0$$

$$V_{CE} =$$

$$4 = 15 - (10 \times 10^{-3} (R_C + 10 R_E) (10 R_E + R_E))$$

$$4 = 15 - (10 \times 10^{-3} \times 11 R_E)$$

$$10 \times 10^{-3} \times 11 R_E = 15 - 4$$

$$\therefore R_E = \frac{11}{100} \Omega$$

$$\therefore R_C = 10 R_E = 10 \times 100$$

$$= \underline{\underline{1000 \Omega}}$$

$$I_B = \frac{V_{CC} - V_{CE}}{R_B + \beta (1 + \beta) R_E}$$

$$7.7 \times 10^{-5} = \frac{15 - 7}{R_B + (131) \times 100}$$

$$= \underline{\underline{172.614 \text{ k}\Omega}}$$