Analog Electronics

EET205

Course Outcomes

- CO 1 Design biasing scheme for transistor circuits.[K3]
- CO 2 Analyse BJT and FET amplifier circuits.[K4]
- CO 3 Choose a power amplifier with appropriate specifications for electronic circuit applications.[K2]
- CO 4 Design oscillator circuits using BJT. [K3]
- CO 5 Develop competence in design of circuits for various applications using Opamp and timer IC's. [K3]
- CO 6 Acquire knowledge on fundamental concepts of transistor and Opamp.[K2]

Module 1

Bipolar Junction Transistors: Review of BJT characteristics- Operating point of BJT – Factors affecting stability of Q point. DC Biasing–Biasing circuits: fixed bias, collector to base bias, voltage divider bias, role of emitter resistance in bias stabilisation. Stability factor (Derivation of stability factors for Voltage Divider Biasing only).Numerical problems. Bias compensation using diode and thermistor. BJT Model- h-parameter model of BJT in CE configuration. Small signal low frequency ac equivalent circuit of CE amplifier –Role of coupling capacitors and emitter bypass capacitor. Calculation of amplifier gains and impedances using h parameter equivalent circuit.

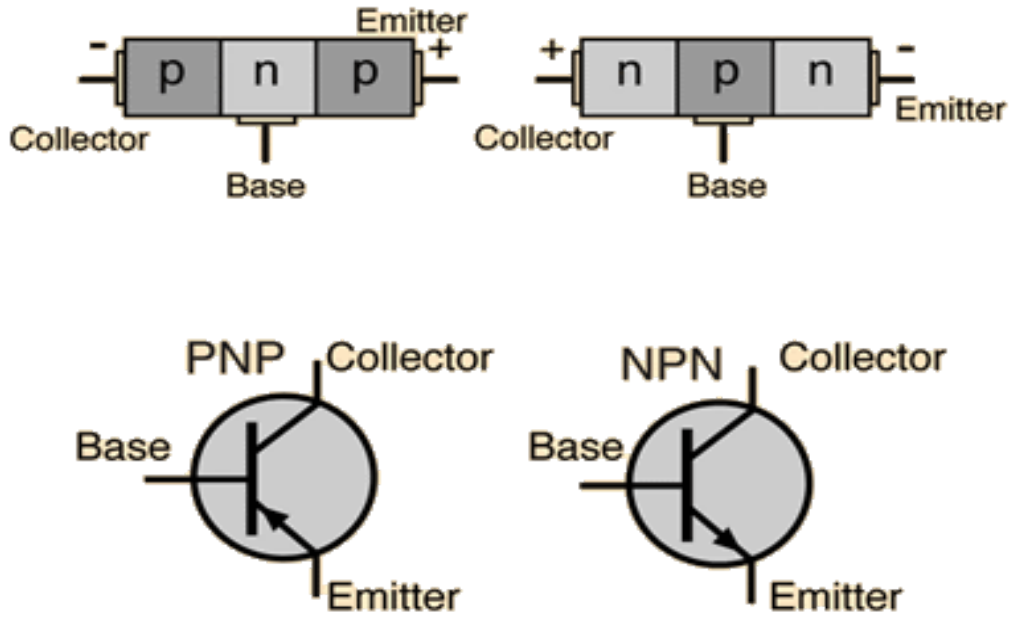
Text books

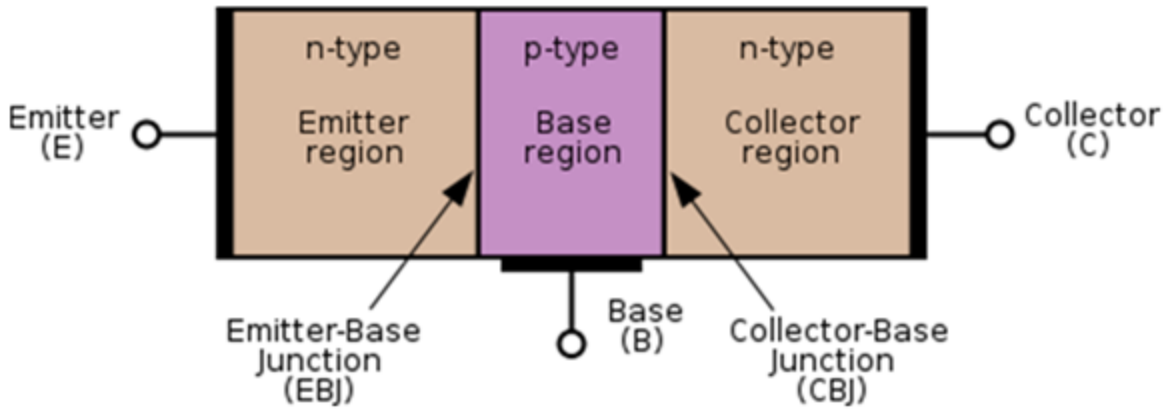
1. Bell D. A., Electronic Devices and Circuits, Prentice Hall of India, 2007.
2. Malvino A. and D. J. Bates, Electronic Principles7/e, Tata McGraw Hill, 2010.
3. Boylestad R. L. and L. Nashelsky, Electronic Devices and Circuit Theory, 10/e, Pearson Education India, 2009.
4. Choudhury R., Linear Integrated Circuits, New Age International Publishers. 2008.

Reference Books

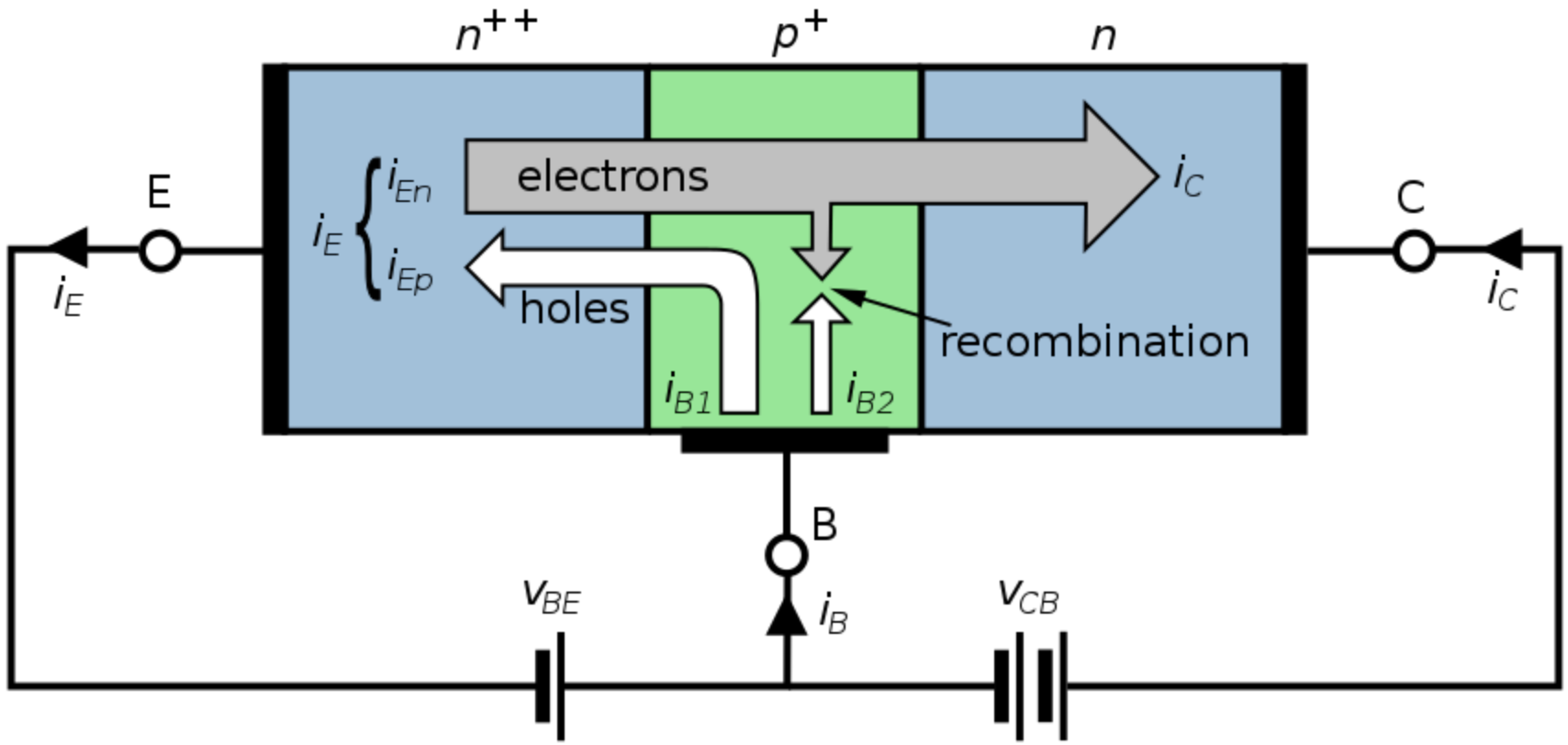
1. Floyd T.L., Fundamentals of Analog Circuits,, Pearson Education, 2012.
2. Robert T. Paynter and John Clemons, Paynter's Introductory electronic devices & circuits, Prentice Hall Career & Technology, New Jersey.
3. Millman J. and C. C. Halkias, Integrated Electronics: Analog and Digital Circuits and Systems, Tata McGraw-Hill, 2010.
4. Streetman B. G. and S. Banerjee, Solid State Electronic Devices, Pearson Education Asia,2006.
5. Gayakward R. A., Op-Amps and Linear Integrated Circuits, PHI Learning Pvt. Ltd., 2012.

BJT (Bipolar Junction Transistor)





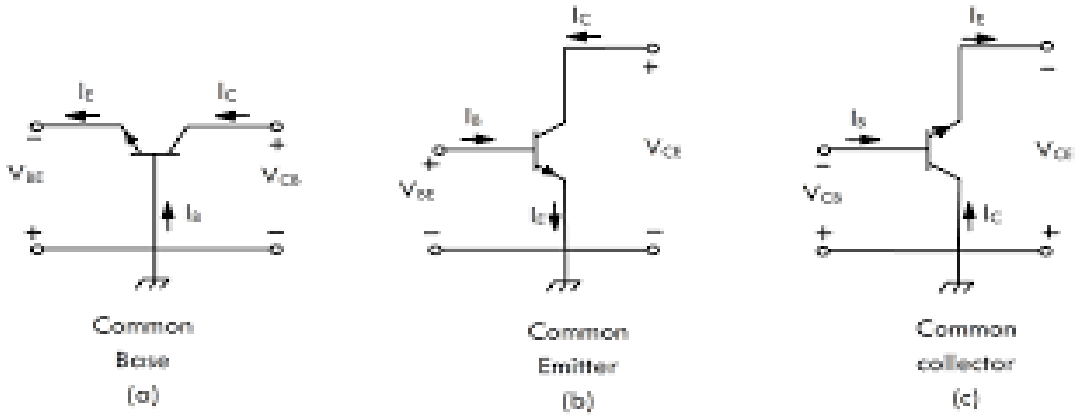
Working of BJT



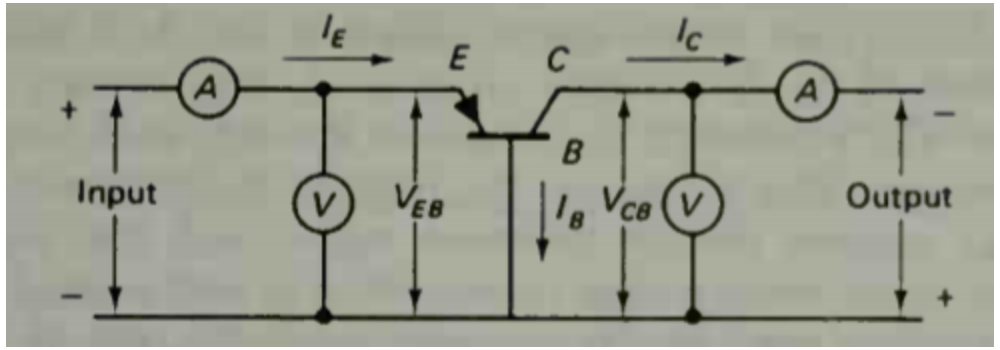
BJT configurations

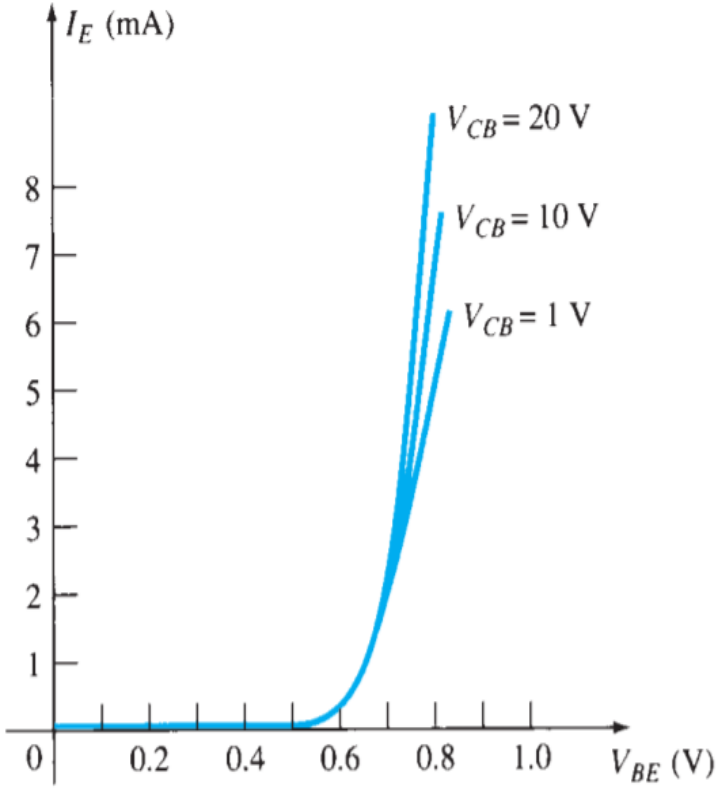
There are three configurations of BJT.

- Common Base configuration
- Common Emitter configuration
- Common collector configuration

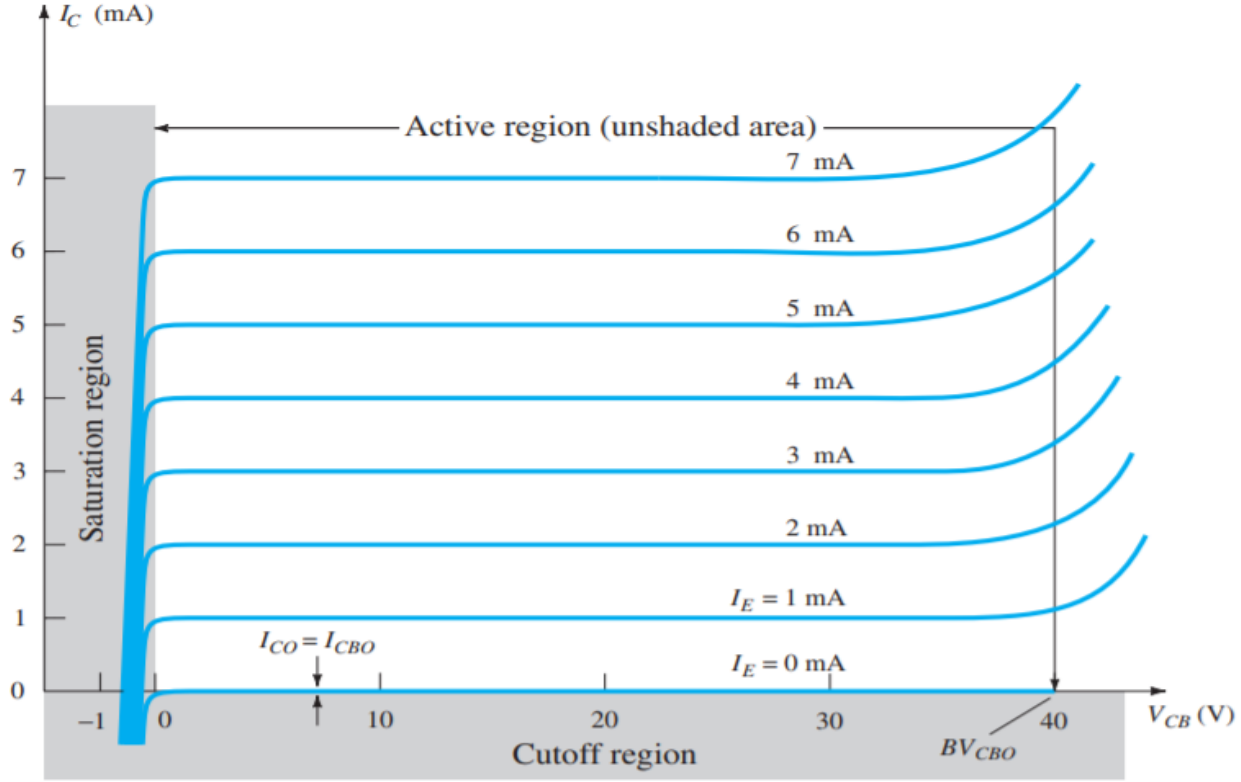


CB configuration



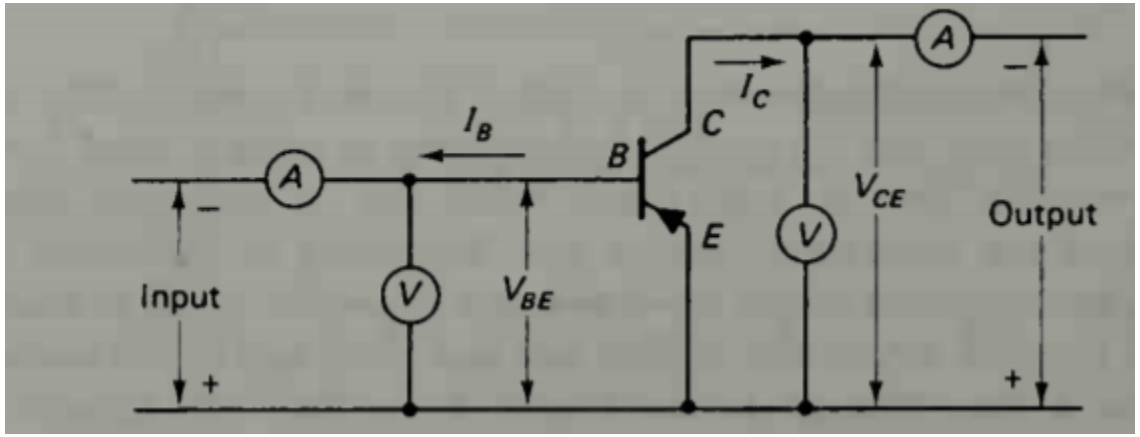


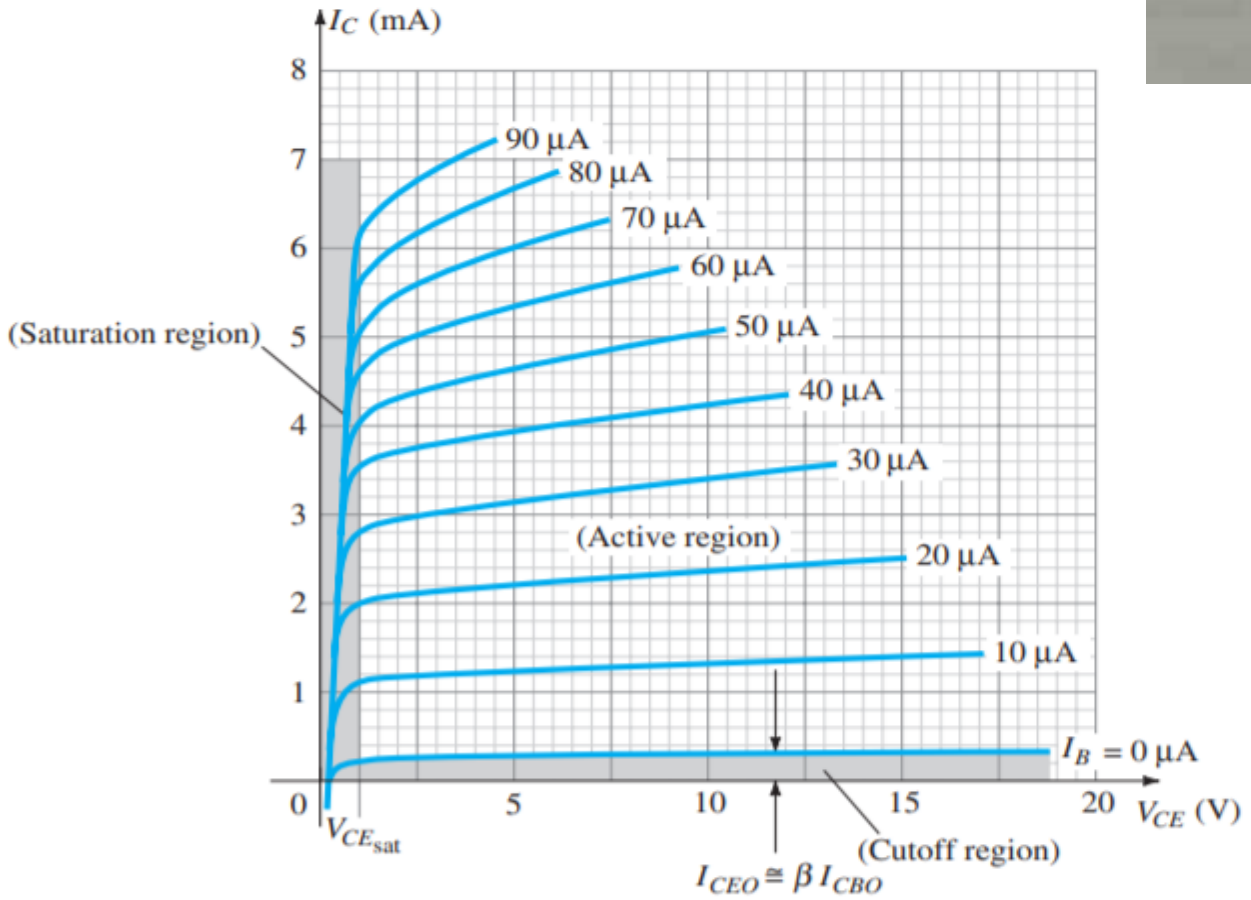
Input characteristics



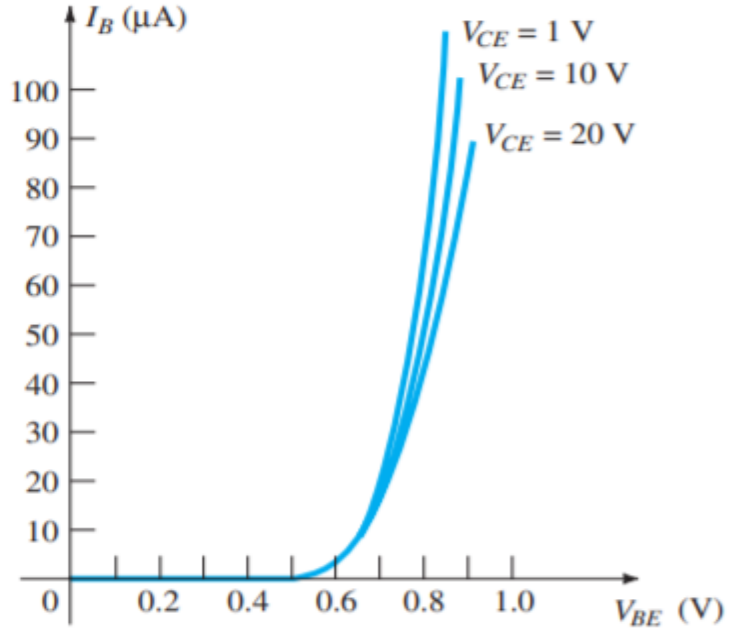
Output characteristics

CE configuration



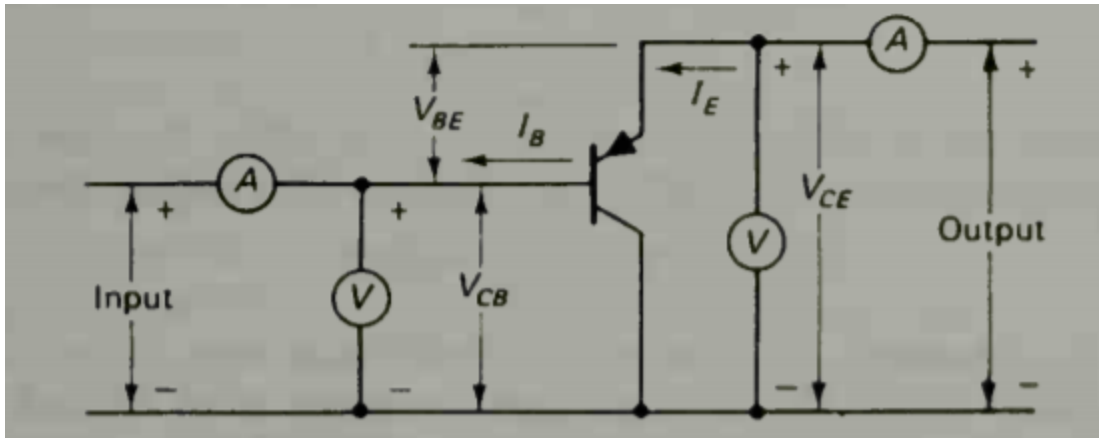


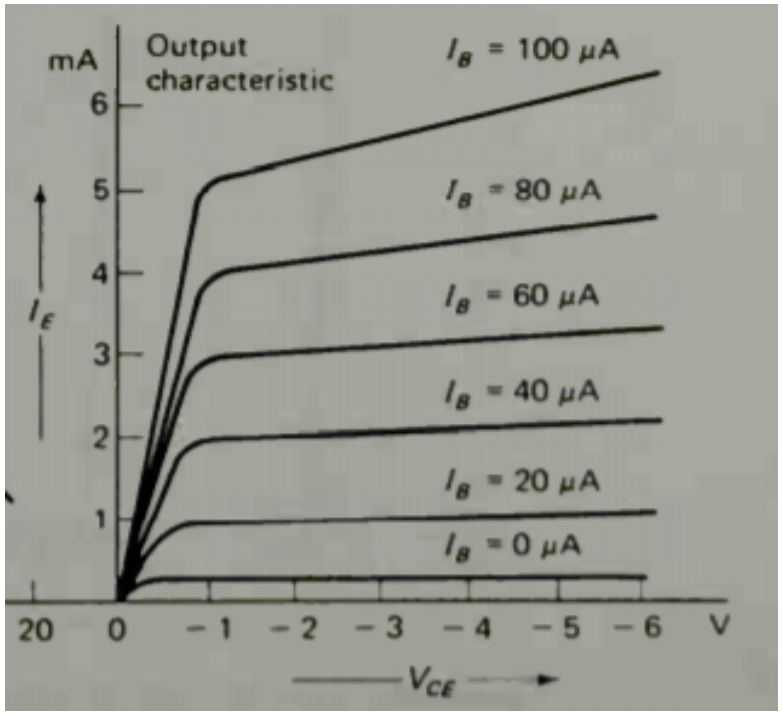
Output characteristics



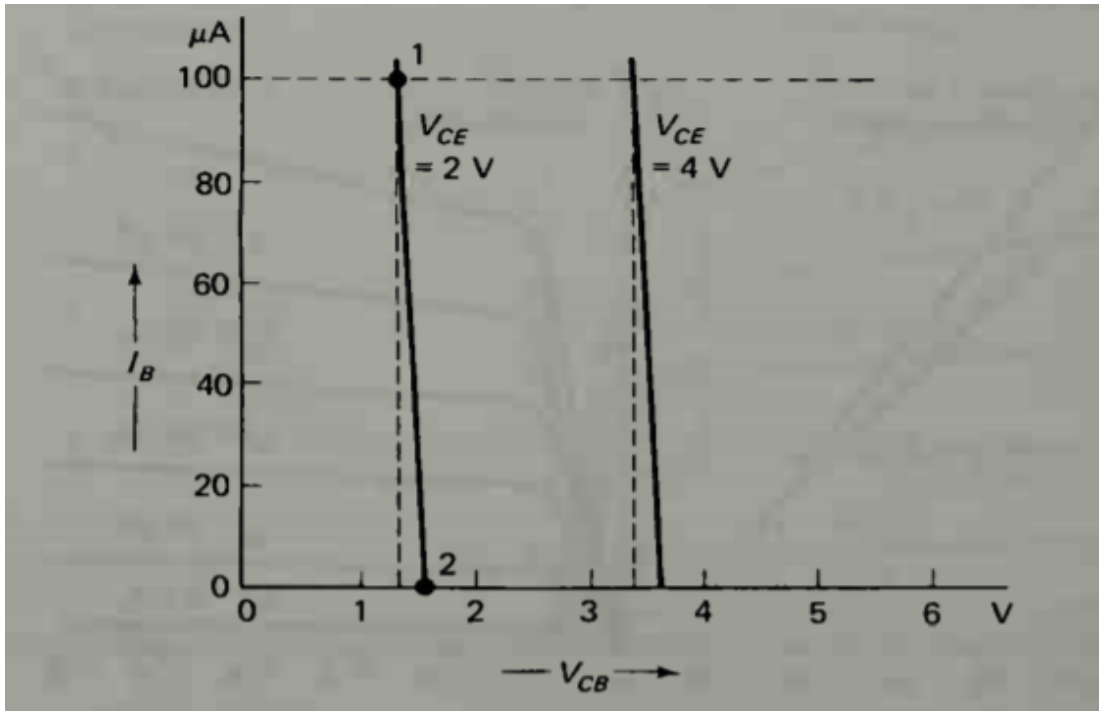
Input characteristics

CC configuration





Output characteristics

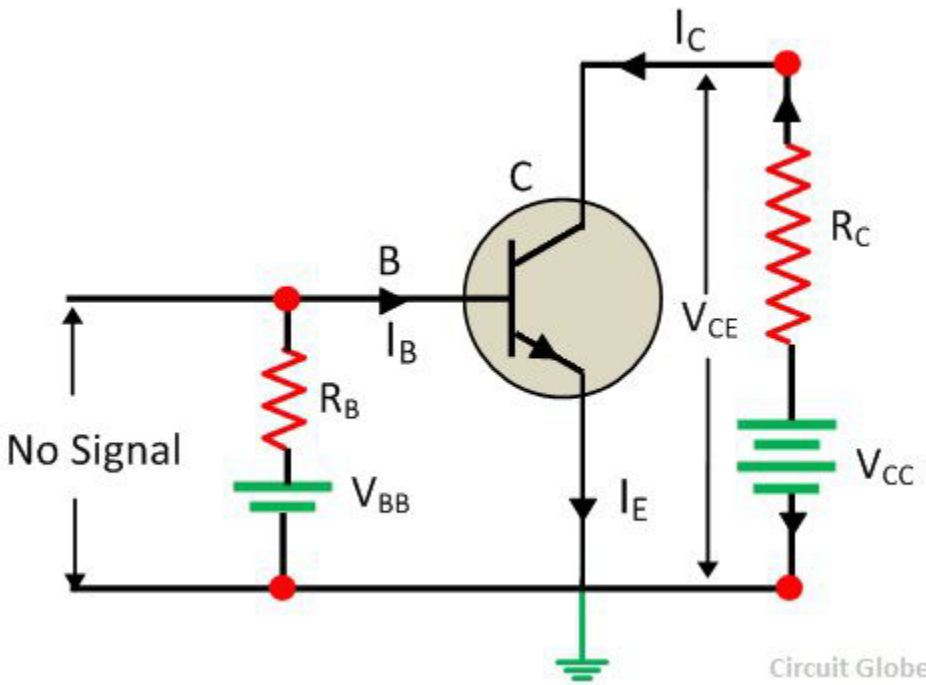


Input characteristics

Transistor biasing

- Biasing is the application of dc voltages to establish a fixed level of current and voltage.
- For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal.
- Because the operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q -point). By definition, quiescent means quiet, still, inactive.

DC load line



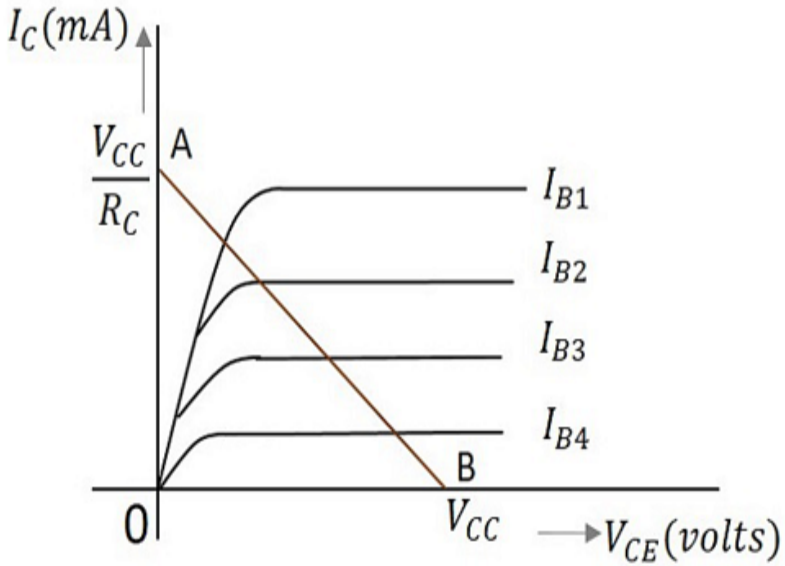
Applying KVL for output loop,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

When I_C=0, V_{CE}= V_{CC}

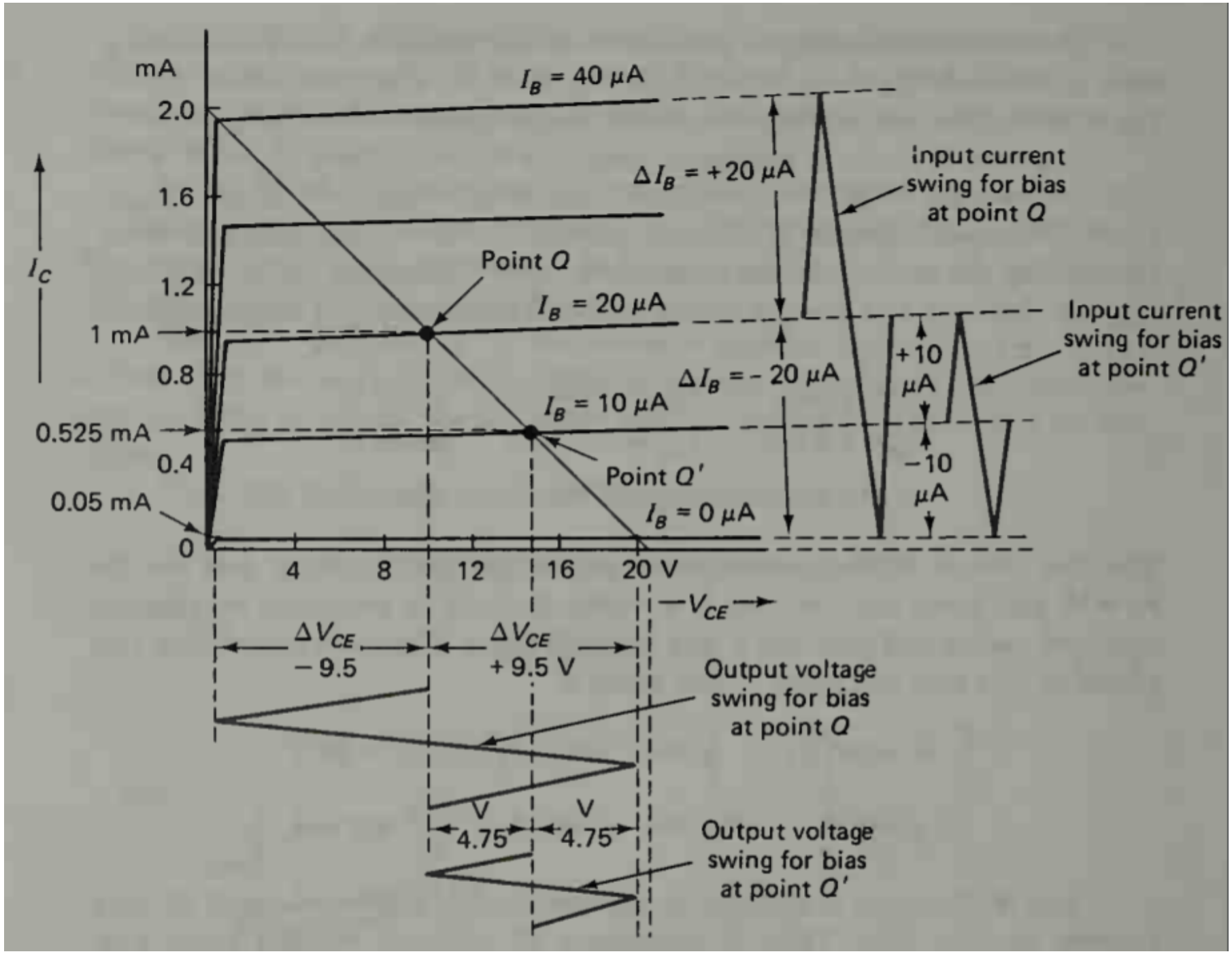
V_{CE}=0, $I_C = \frac{V_{CC}}{R_C}$



The line obtained by joining the points A and B gives the DC load line.

Operating point

- Q point is a point on the DC load line representing I_C and V_{CE} in the absence of input signal.
- Dc load line is the locus of operating point on the output characteristics of transistor.


mA
2.0
1.6
1.2
1 mA
0.8
0.525 mA
0.4
0.05 mA
0
I_C
I_B = 40 μA
I_B = 20 μA
I_B = 10 μA
I_B = 0 μA
Point Q
Point Q′
ΔI_B = +20 μA
ΔI_B = - 20 μA
Input current swing for bias at point Q
Input current swing for bias at point Q′
+10 μA
−10 μA
4
8
12
16
20 V
$-V_{CE}$
ΔV_{CE} − 9.5
ΔV_{CE} + 9.5 V
Output voltage swing for bias at point Q
V 4.75
V 4.75
Output voltage swing for bias at point Q′

Transistor biasing

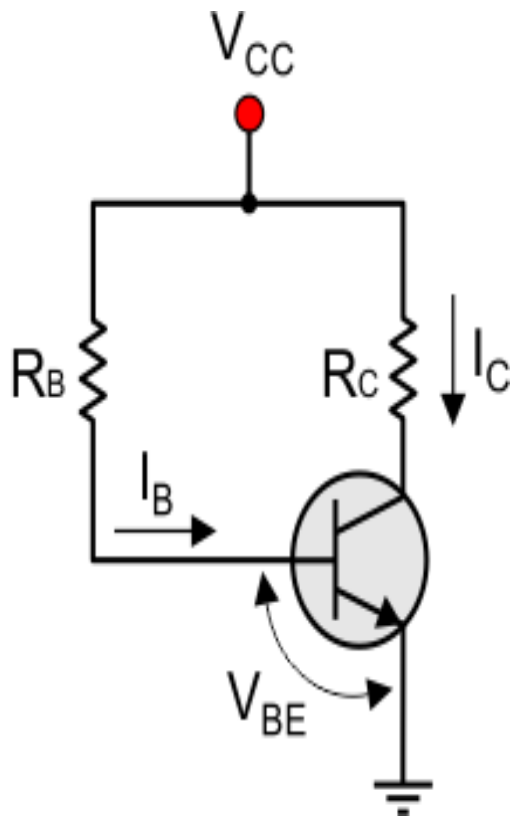
- The main aim of biasing a transistor is to fix the operating point properly such that any variations in input signal will be properly amplified and reproduced at the output terminal. If the biasing is not proper, it can go into saturation or cutoff when an input signal is applied.
- Requirements of a biasing circuit
  - ✔ Establish operating point in the middle of active region of the characteristics.
  - ✔ Stabilise collector current against temperature variations.
  - ✔ Make the operating point independent of transistor parameters.

Biasing circuits

Different biasing circuits are:

- Fixed bias circuit
- Collector to base bias circuit
- Voltage divider bias circuit

1.Fixed bias circuit



Input Loop

Applying KVL for input loop,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

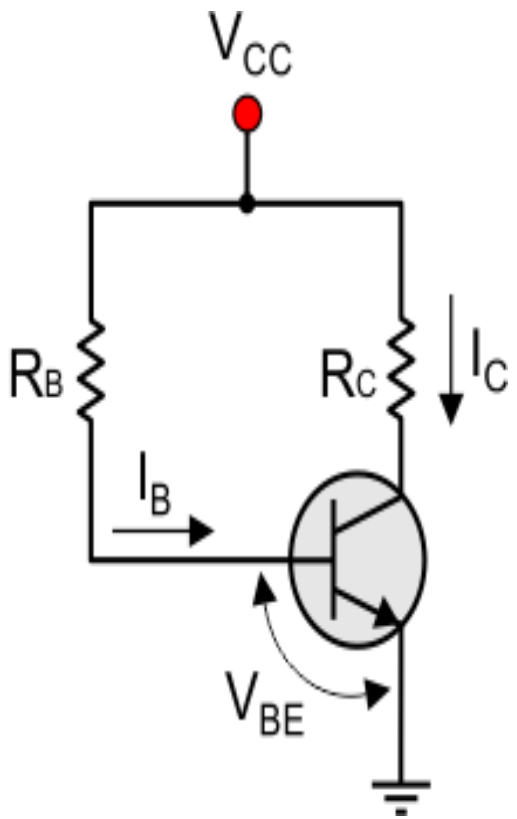
$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Once R_B is selected, I_B is fixed.

Hence the name fixed bias circuit

$$I_C = \beta I_B$$

Fixed bias circuit contd..



Output Loop

Applying KVL for output loop,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

Q point is given by I_C and V_{CE}

$$V_{CE} = V_C - V_E$$

Since $V_E = 0$, $V_{CE} = V_C$

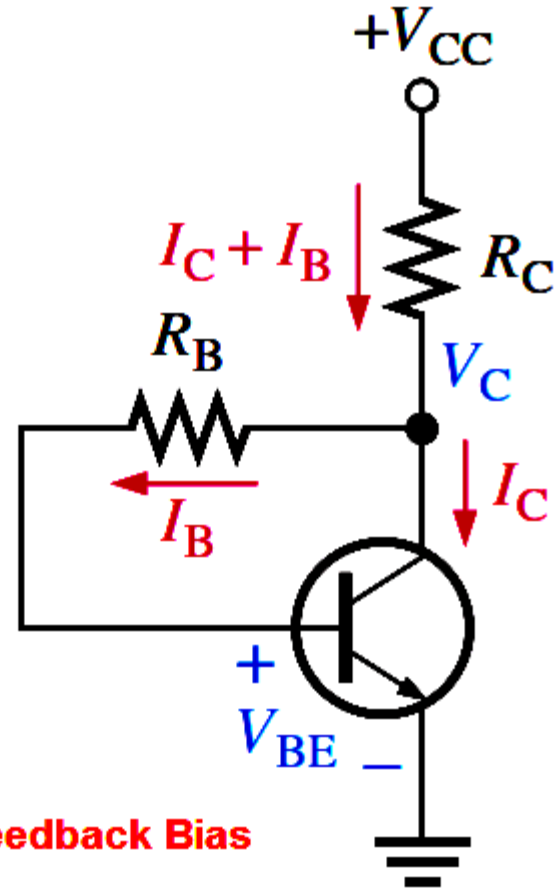
$$V_{BE} = V_B - V_E$$

Since $V_E = 0$, $V_{BE} = V_B$

Fixed bias circuit contd..

- Fixed bias technique is not a satisfactory method of obtaining good bias point stability.
- Collector current depends on the value of β and changes with change in β.
- Collector current is also dependent on temperature.

Collector to base bias circuit



Collector Feedback Bias

Input Loop

Applying KVL for output loop,

$$V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - (I_C + I_B) R_C$$

Applying KVL for input loop,

$$V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CE} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CE} - V_{BE}}{R_B}$$

$$I_C = \beta I_B$$

Collector to base bias circuit contd..

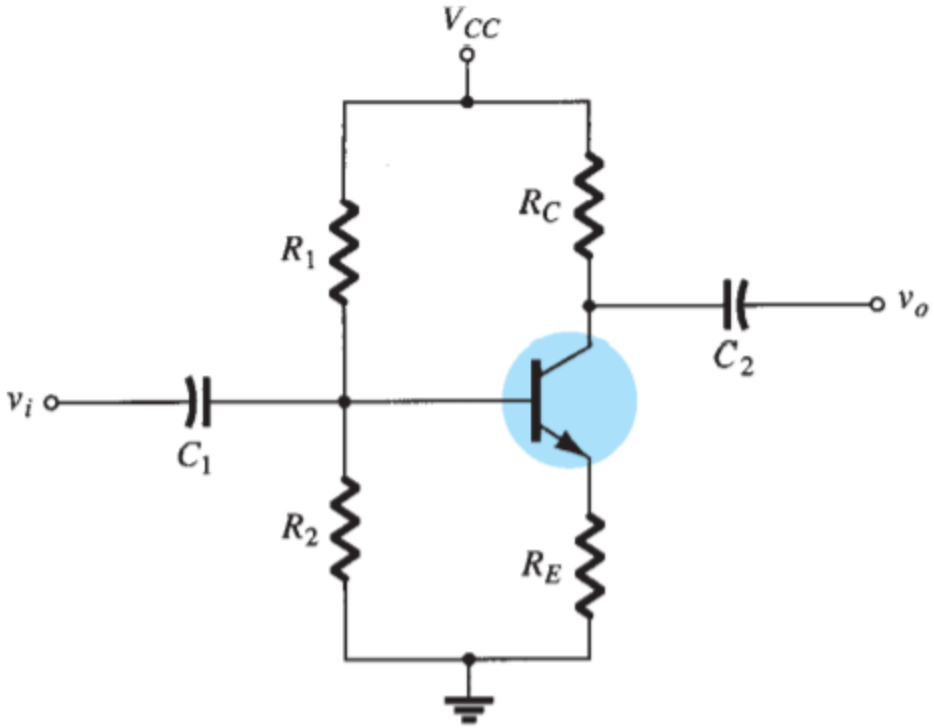
•• More stable than fixed biasing circuit.

- Collector current depends on the value of β and changes with change in β.As β increases, collector current increases , V_{CE} decreases, base current decreases and tends to reduce collector current.
- Collector current is also dependent on temperature.

Class work 1

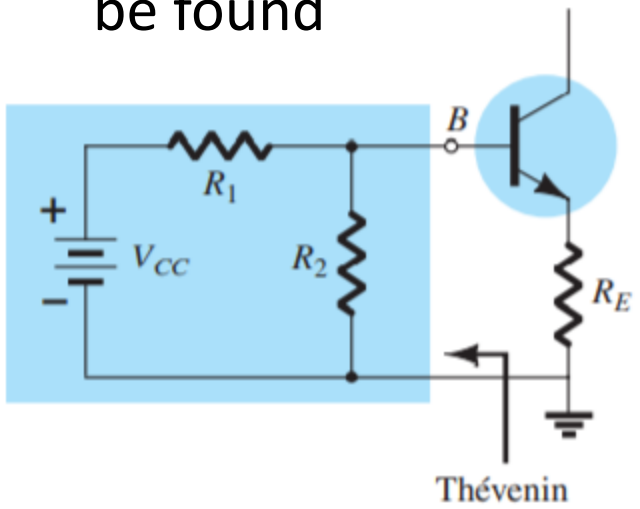
1. Design a fixed bias circuit using a silicon transistor with β =50, V_{cc} = 10V, and dc bias conditions are V_{CE}= 5 V and I_C= 5mA. Also calculate the operating point when β =25 and β =100.
2. Design a collector to base bias circuit using a silicon transistor with β =50, V_{cc} = 10V, and dc bias conditions are V_{CE}= 5 V and I_C= 5mA. . Also calculate the operating point when β =25 and β =100.
3. Compare the stability of two biasing circuits.

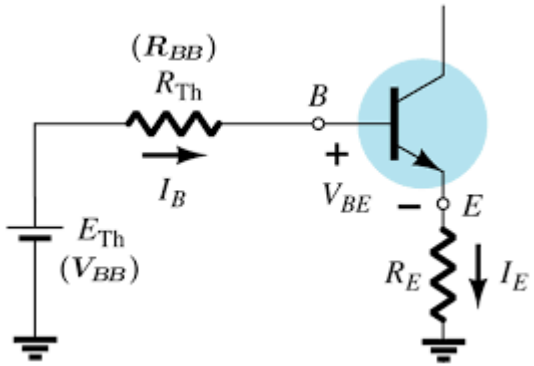
Voltage divider biasing



Exact Analysis

The Thevenin equivalent network for the network to the left of the base terminal can be found

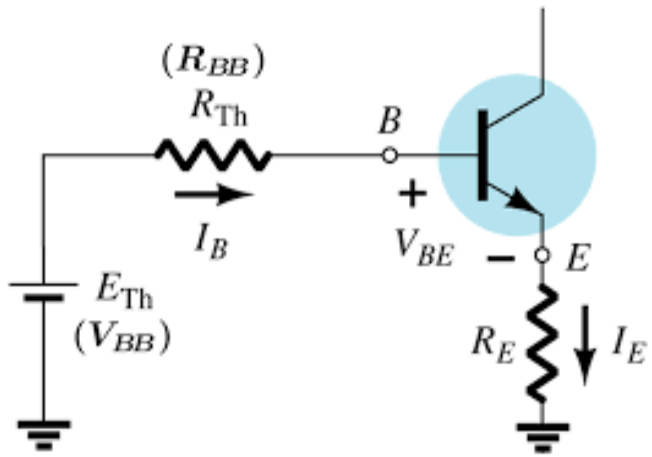




$$E_{Th} = V_{CC}\frac{R_2}{R_1 + R_2}$$

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$

Voltage divider biasing contd..



$$E_{Th} = V_{CC}\frac{R_2}{R_1 + R_2}$$

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$

Exact Analysis

Applying KVL for input loop

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$I_E = I_B + I_C$$

$$I_E = (1 + \beta) I_B$$

Substituting

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (1+\beta) R_E}$$

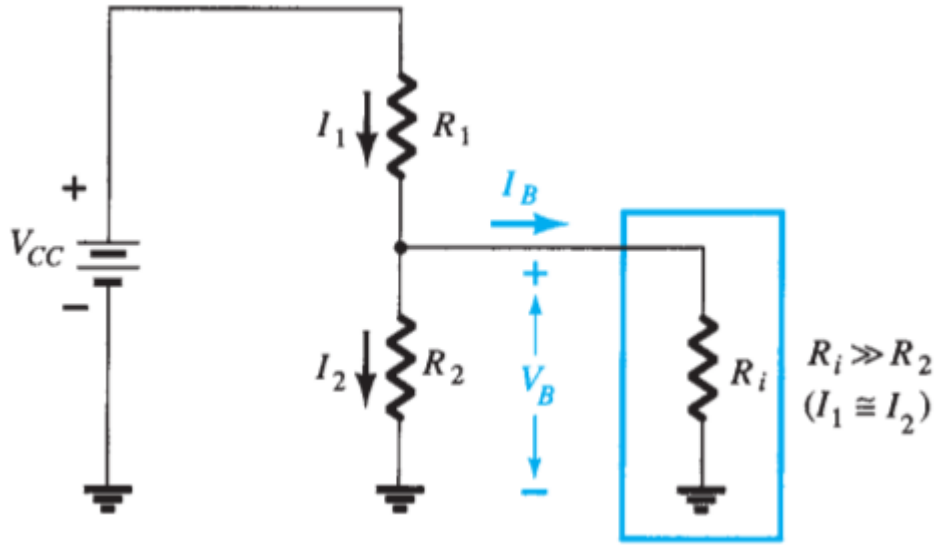
$$I_C = \beta I_B$$

Applying KVL for output loop

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

Voltage divider biasing contd..



Condition for approximate analysis

$$\beta R_E \geq 10R_2$$

Approximate Analysis

Resistor R_E is reflected back to the input base circuit by a factor $(1 + \beta)$

$$R_i = (1+\beta)R_E$$

If $R_i \gg R_2$, then we can approximate $I_B = 0$

Therefore $I_1 = I_2$

$$V_B = V_{CC}\frac{R_2}{R_1 + R_2}$$

$$V_E = V_B - V_{BE}$$

$$I_E = \frac{V_E}{R_E}$$

$$I_C \cong I_E$$

Applying KVL for output loop

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Role of emitter resistor

- The need for including a resistor from emitter to ground was to provide a means of dc bias stabilization so that the change of collector current due to leakage currents in the transistor and the transistor beta would not cause a large shift in the operating point.
- The emitter resistor cannot be unreasonably large because the voltage across it limits the range of swing of the voltage from collector to emitter .
- The voltage from emitter to ground is typically around one-fourth to one-tenth of the supply voltage.

Voltage divider biasing contd..

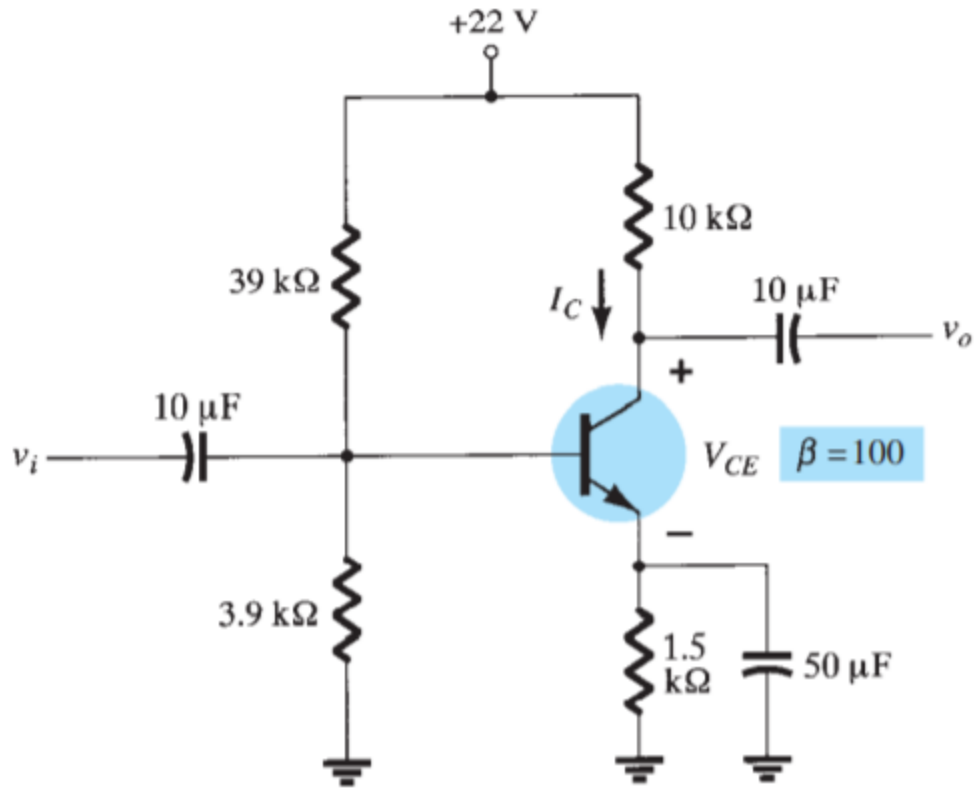
- More stable biasing circuit.
- Collector current is independent on the value of β.
- Collector current is also stabilised against temperature variations. As temperature increases, collector current increases , emitter current increases, $I_E R_E$ drop increases, base current decreases and tends to reduce collector current.

Class work 2

1.Determine the operating point for the voltage divider bias circuit by

s

analysis

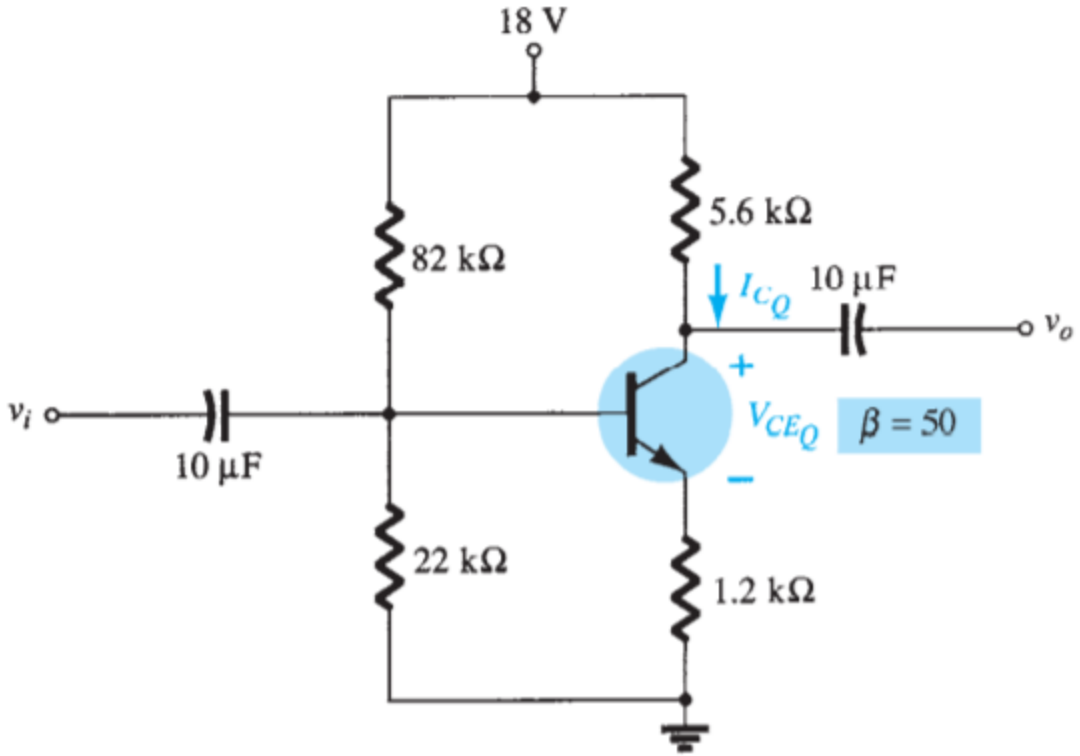


Class work 2

2.Determine the operating point for the voltage divider bias circuit by

a) Exact analysis

nalysis



Bias Stabilization

The stability of a system is a measure of the sensitivity of a network to variations in its parameters. The collector current I_C is sensitive to each of the following parameters:

β: increases with increase in temperature

V_{BE}: decreases about 2.5 mV per degree Celsius (°C) increase in temperature

I_{CO} (reverse saturation current): doubles in value for every 10°C increase in temperature

Variation of Silicon Transistor Parameters with Temperature

T (°C)	I_{CO} (nA)	β	V_{BE} (V)
−65	0.2×10^{-3}	20	0.85
25	0.1	50	0.65
100	20	80	0.48
175	3.3×10^{3}	120	0.3

Stability factor

- A stability factor S is defined for each of the parameters affecting bias stability as follows:

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}$$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$

Expression for $S(I_{CO})$

- $$I_C = \beta I_B + (1+\beta) I_{CO}$$

Differentiating with respect to I_C

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta) \frac{dI_{CO}}{dI_C}$$

$$1 - \beta \frac{dI_B}{dI_C} = \frac{(1+\beta)}{S(I_{CO})}$$

$$S(I_{CO}) = \frac{(1+\beta)}{1 - \beta \frac{dI_B}{dI_C}}$$

Expression for $S(I_{CO})$ -Voltage divider biasing circuit

- Applying KVL for input loop

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$
$$E_{Th} - I_B R_{Th} - V_{BE} - (I_B + I_C) R_E = 0$$

Differentiating with respect to I_C

$$0 = (R_{Th} + R_E)\frac{dI_B}{dI_C} + R_E$$
$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_{Th} + R_E}$$

$$\boldsymbol{S(I_{CO}) = \frac{(1+\beta)}{1+\beta\frac{R_E}{R_{Th}+R_E}} = \frac{(1+\beta)(R_{Th}+R_E)}{R_E(1+\beta)+R_{Th}}}$$

$$\boldsymbol{= \frac{(1+\beta)\left(\frac{R_{Th}}{R_E}+1\right)}{(1+\beta)+\frac{R_{Th}}{R_E}}}$$

Expression for $S(V_{BE})$ -Voltage divider biasing circuit

- Applying KVL for input loop

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$E_{Th} - \frac{I_C}{\beta} R_{Th} - V_{BE} - (1 + \beta)\frac{I_C}{\beta} R_E = 0$$

$$E_{Th} - V_{BE} = \frac{I_C}{\beta} R_{Th} + (1 + \beta)\frac{I_C}{\beta} R_E$$

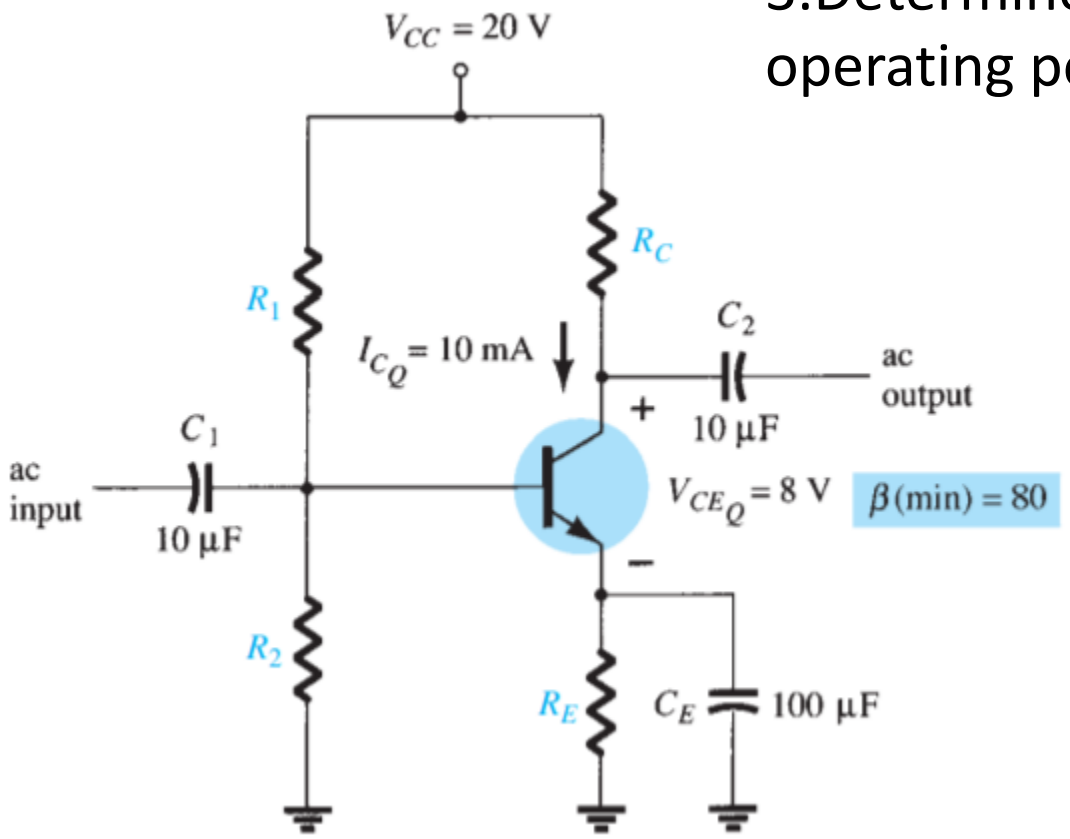
Differentiating with respect to I_C

$$\frac{-dV_{BE}}{dI_C} = \frac{R_{Th} + (1 + \beta)R_E}{\beta}$$

$$S(V_{BE}) = \frac{-\beta}{R_{Th} + (1 + \beta)R_E}$$

$$S(V_{BE}) = \frac{-\frac{\beta}{R_E}}{\frac{R_{Th}}{R_E} + 1 + \beta}$$

Class work 2



3.Determine the values of R_C, R_E, R_1, and R_2 for the operating point indicated.

Class work 2

4. Design a voltage-divider bias network using a supply of 24 V, a transistor with a beta of 110, and an operating point of I_{CQ} = 4 mA and V_{CEQ} = 8 V.

Bias compensation using diode

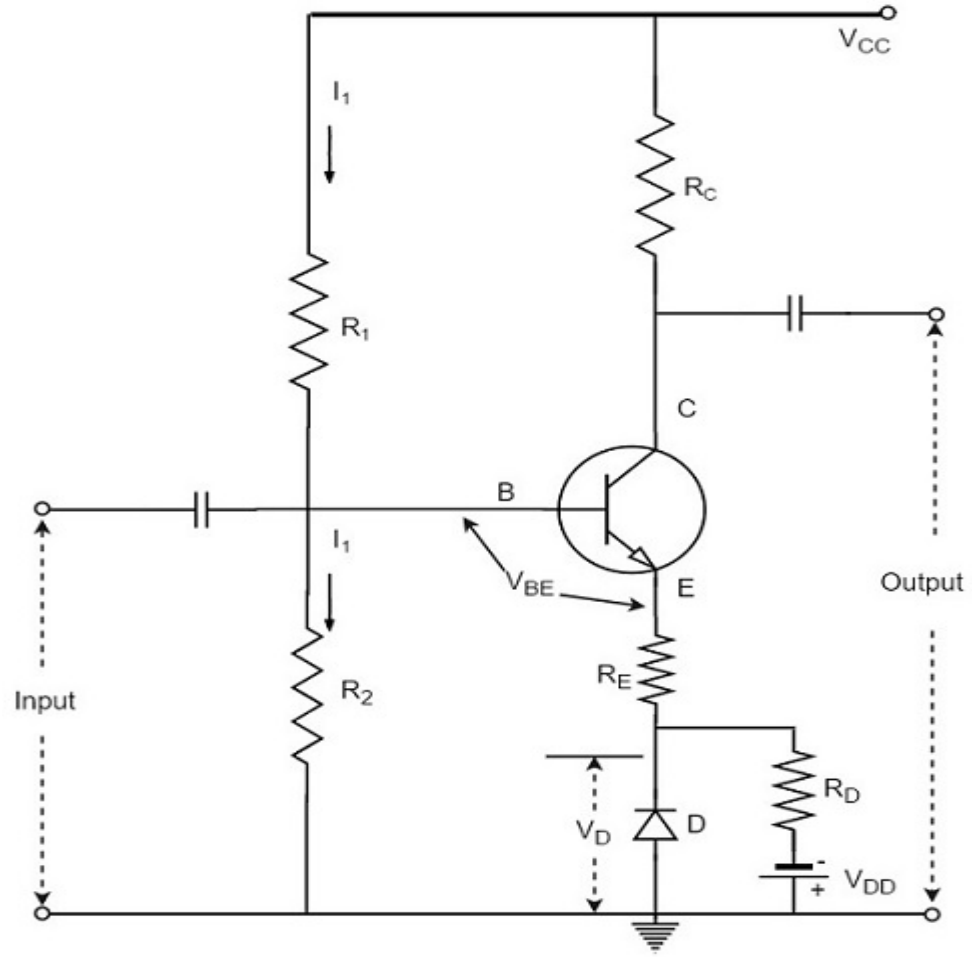
- These are the circuits that implement compensation techniques using diodes to deal with biasing instability. The stabilization techniques refer to the use of resistive biasing circuits which permit I_B to vary so as to keep I_C relatively constant.

There are two types of diode compensation methods.

They are −

- Diode compensation for instability due to V_{BE} variation
- Diode compensation for instability due to I_{CO} variation

Diode Compensation for Instability due to VBE Variation:



Diode Compensation for Instability due to VBE Variation:

In a Silicon transistor, the changes in the value of V_{BE} results in the changes in I_C.

A diode can be employed in the emitter circuit in order to compensate the variations in V_{BE} or I_{CO}.

As the diode and transistor used are of same material, the voltage V_D across the diode has same temperature coefficient as V_{BE} of the transistor.

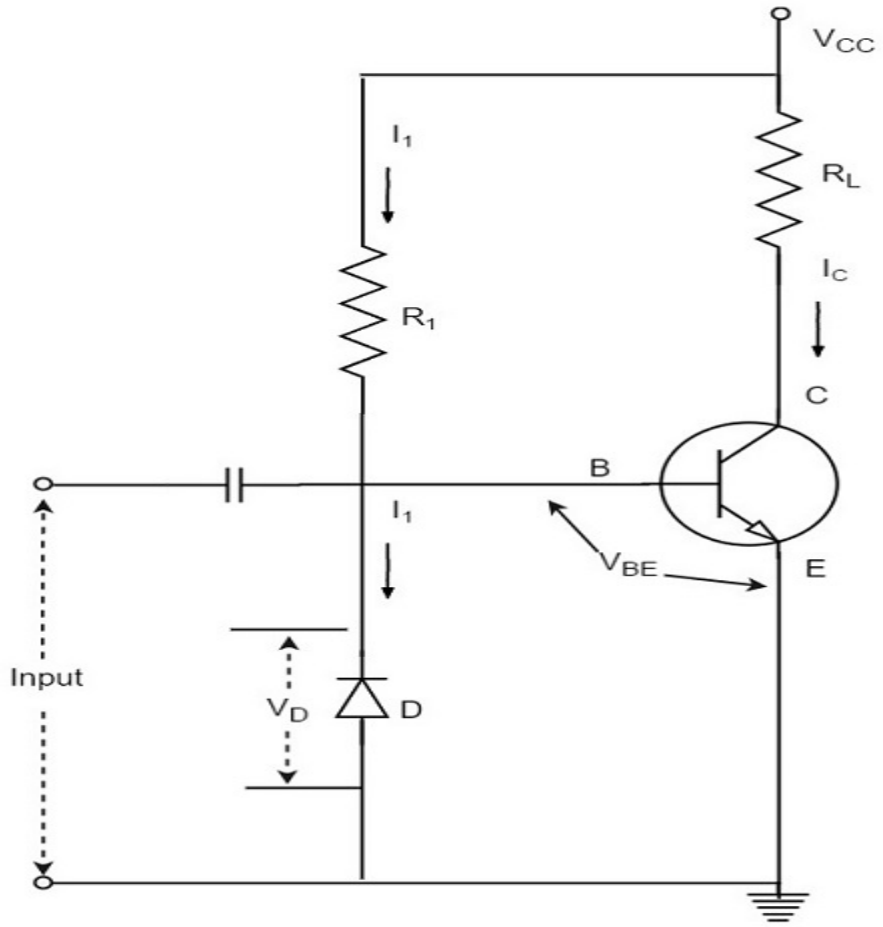
The diode D is forward biased by the source V_{DD} and the resistor R_D.

The variation in V_{BE} with temperature is same as the variation in V_D with temperature, hence the quantity $(V_{BE} – V_D)$ remains constant.

So the current I_C remains constant in spite of the variation in V_{BE}.

Diode Compensation for Instability due to ICO Variation

- The following figure shows the circuit diagram of a transistor amplifier with diode D used for compensation of variation in ICO



- The reverse saturation current I_O of the diode will increase with temperature at the same rate as the transistor collector saturation current I_{CO}.

The diode D is reverse biased by V_{BE} and the current through it is the reverse saturation current I_O.

Now the base current is,

$$I_B = I - I_0$$

Substituting the above value in the expression for collector current.

$$I_C = \beta(I - I_0) + (1 + \beta)I_{CO}$$

If $\beta \gg 1$,

$$I_C = \beta I - \beta I_0 + \beta I_{CO}$$

I is almost constant and if I_O of diode and I_{CO} of transistor track each other over the operating temperature range, then I_C remains constant.

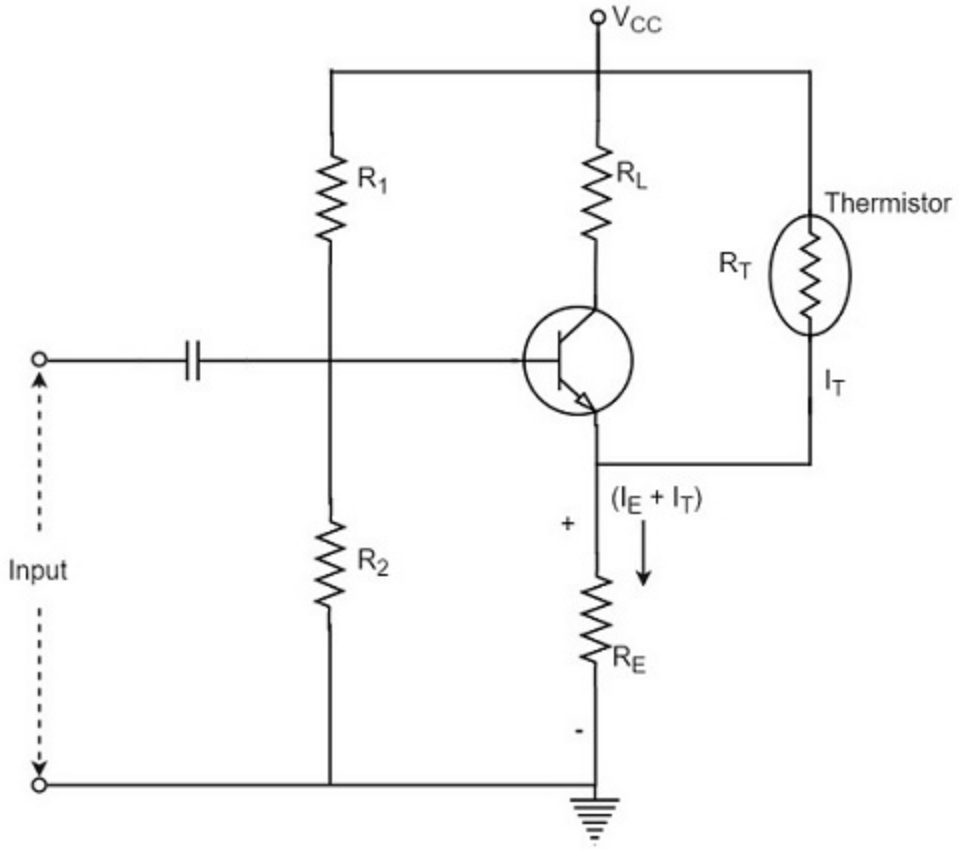
Thermistor compensation

Thermistor is a temperature sensitive device. It has negative temperature coefficient. The resistance of a thermistor increases when the temperature decreases and it decreases when the temperature increases. The below figure shows a self-bias amplifier with thermistor compensation.

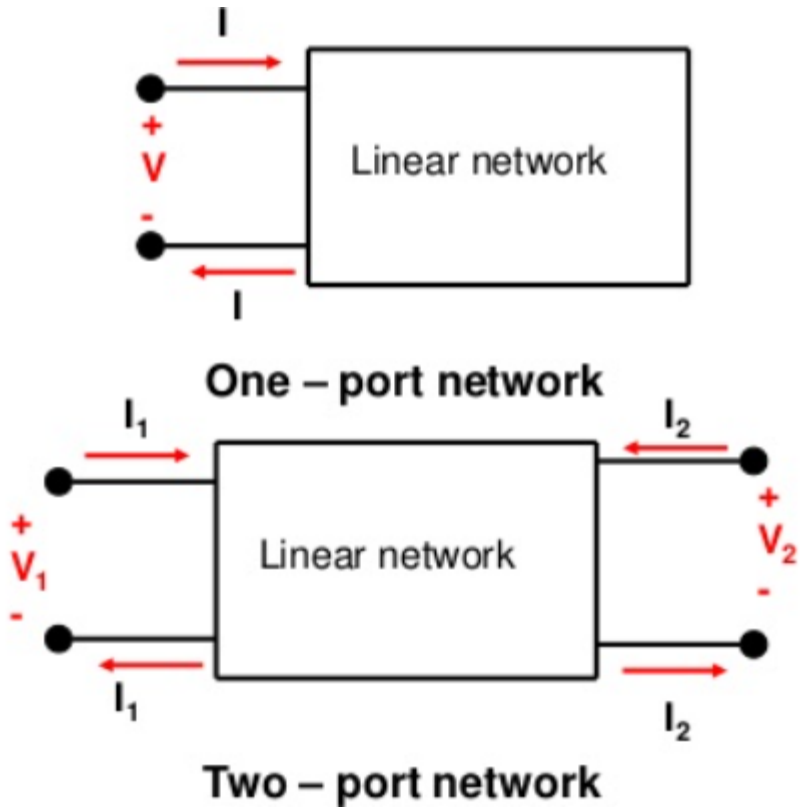
In an amplifier circuit, the changes that occur in I_{CO}, V_{BE} and β with temperature, increases the collector current. Thermistor is employed to minimize the increase in collector current. As the temperature increases, the resistance R_T of thermistor decreases, which increases the current through it and the resistor R_E. Now, the voltage developed across R_E increases, which reverse biases the emitter junction. This reverse bias is so high that the effect of resistors R_1 and R_2 providing forward bias also gets reduced. This action reduces the rise in collector current.

Thus the temperature sensitivity of thermistor compensates the increase in collector current, occurred due to temperature.

Thermistor compensation

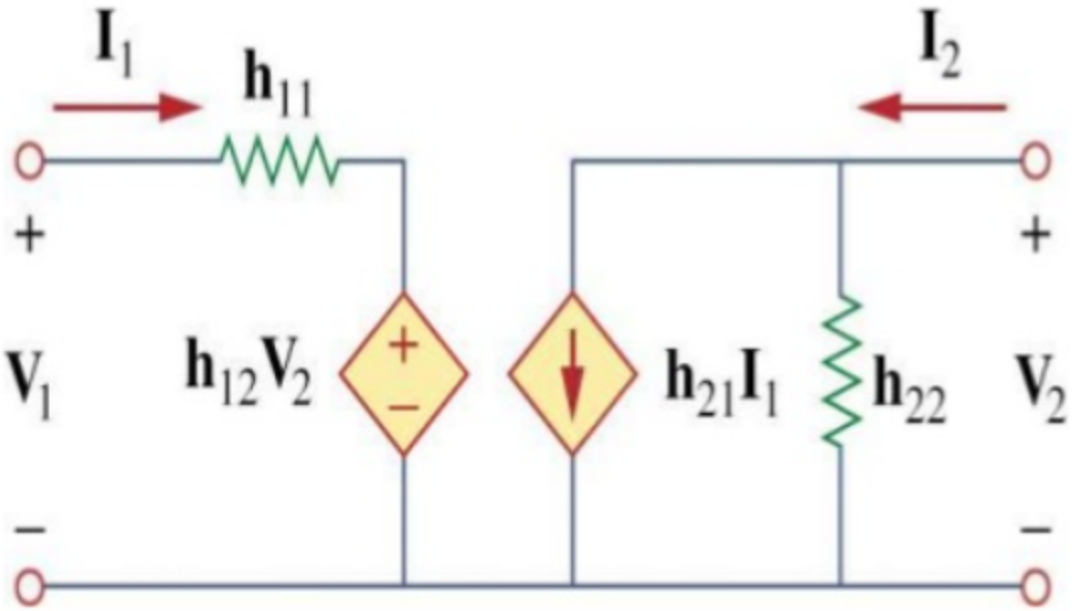


Two port network



- A pair of terminals through which current may enter or leave the network is called port.
- A two port network is a network with two separate ports for input and output.
- It has 2 terminal pairs acting as access points.
- The current enters one terminal pair and leaves through the other terminal pair.

H parameters



$$\mathbf{V}_1 = \mathbf{h}_{11}\mathbf{I}_1 + \mathbf{h}_{12}\mathbf{V}_2$$
$$\mathbf{I}_2 = \mathbf{h}_{21}\mathbf{I}_1 + \mathbf{h}_{22}\mathbf{V}_2$$

$$\begin{bmatrix}\mathbf{V}_1\\ \mathbf{I}_2\end{bmatrix} = \begin{bmatrix}\mathbf{h}_{11} & \mathbf{h}_{12}\\ \mathbf{h}_{21} & \mathbf{h}_{22}\end{bmatrix}\begin{bmatrix}\mathbf{I}_1\\ \mathbf{V}_2\end{bmatrix} = [\mathbf{h}]\begin{bmatrix}\mathbf{I}_1\\ \mathbf{V}_2\end{bmatrix}$$

$$\mathbf{h}_{11} = \left.\frac{\mathbf{V}_1}{\mathbf{I}_1}\right|_{\mathbf{V}_2=0}, \quad \mathbf{h}_{12} = \left.\frac{\mathbf{V}_1}{\mathbf{V}_2}\right|_{\mathbf{I}_1=0}$$
$$\mathbf{h}_{21} = \left.\frac{\mathbf{I}_2}{\mathbf{I}_1}\right|_{\mathbf{V}_2=0}, \quad \mathbf{h}_{22} = \left.\frac{\mathbf{I}_2}{\mathbf{V}_2}\right|_{\mathbf{I}_1=0}$$

h_{11} = Short-circuit input impedance

h_{12} = Open-circuit reverse voltage gain

h_{21} = Short-circuit forward current gain

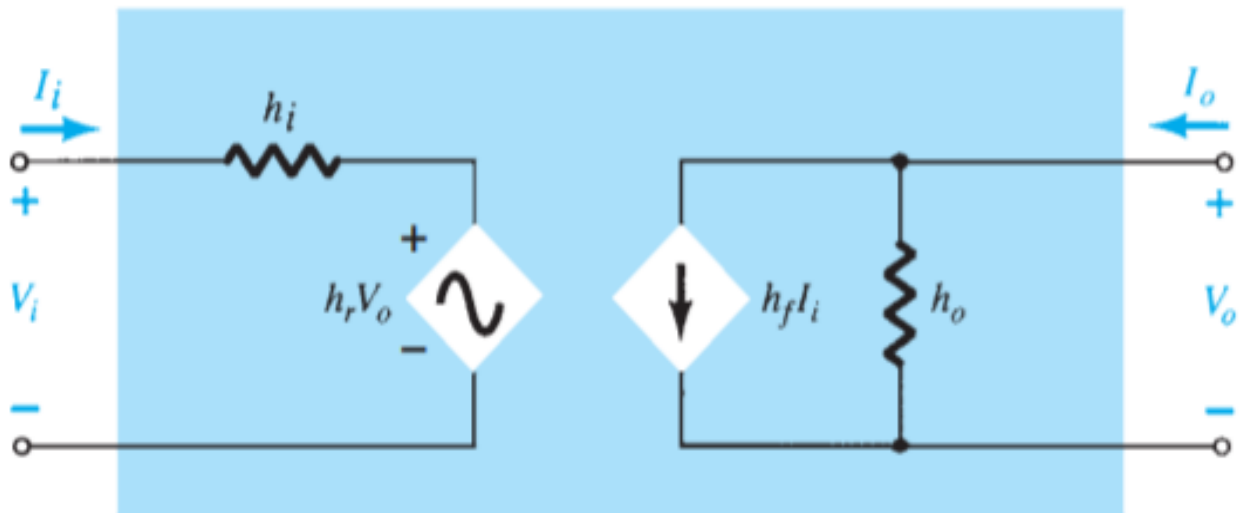
h_{22} = Open-circuit output admittance

$h_{11} \rightarrow$ *i*nput resistance $\rightarrow h_i$

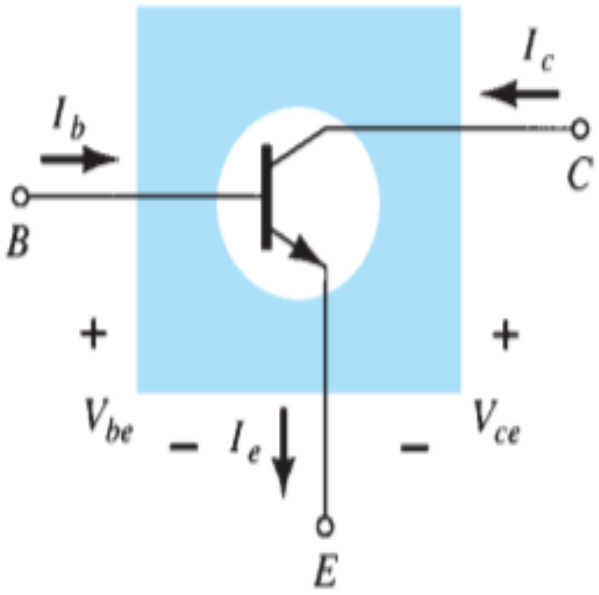
$h_{12} \rightarrow$ *r*everse transfer voltage ratio $\rightarrow h_r$

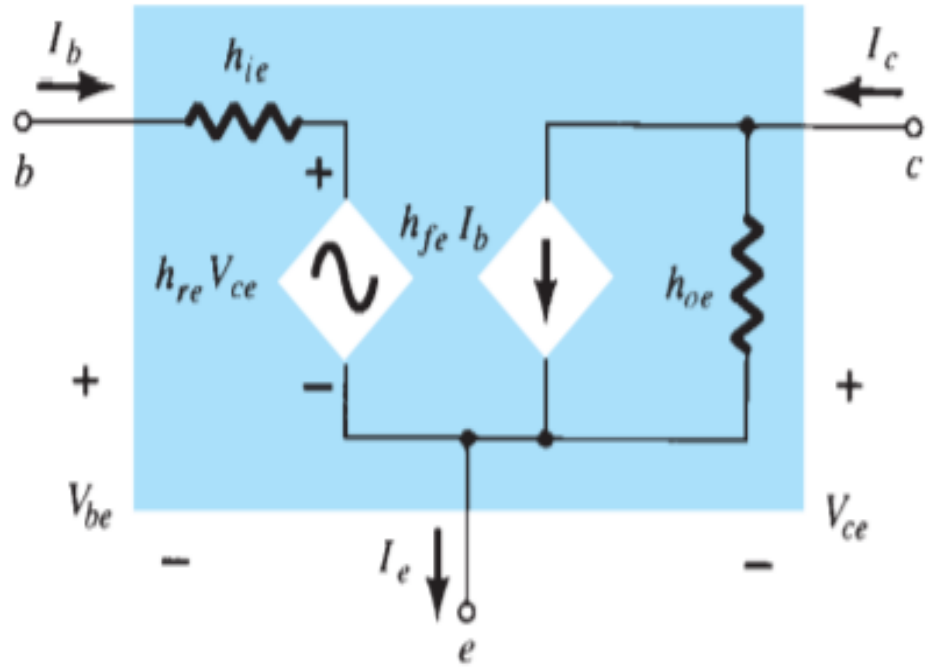
$h_{21} \rightarrow$ *f*orward transfer current ratio $\rightarrow h_f$

$h_{22} \rightarrow$ *o*utput conductance $\rightarrow h_o$

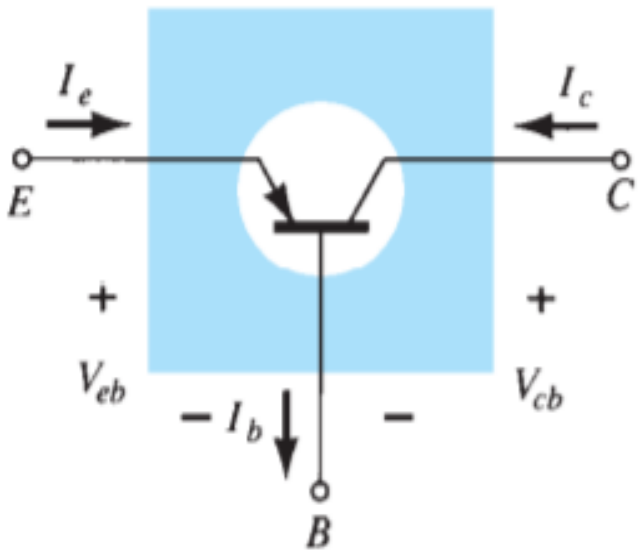


H parameter model of transistor in CE configuration

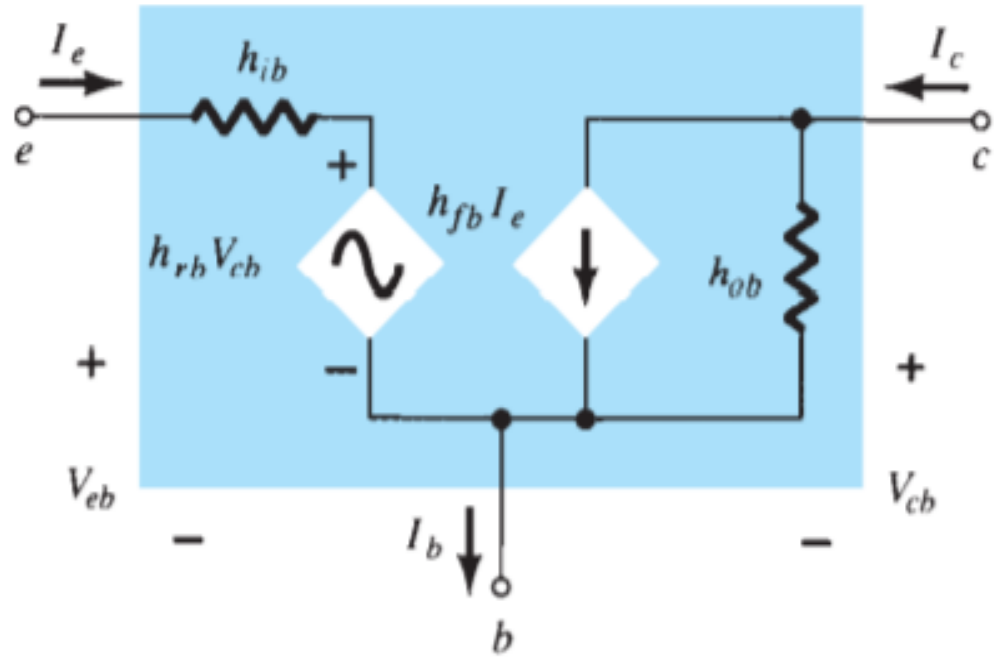




H parameter model of transistor in CB configuration

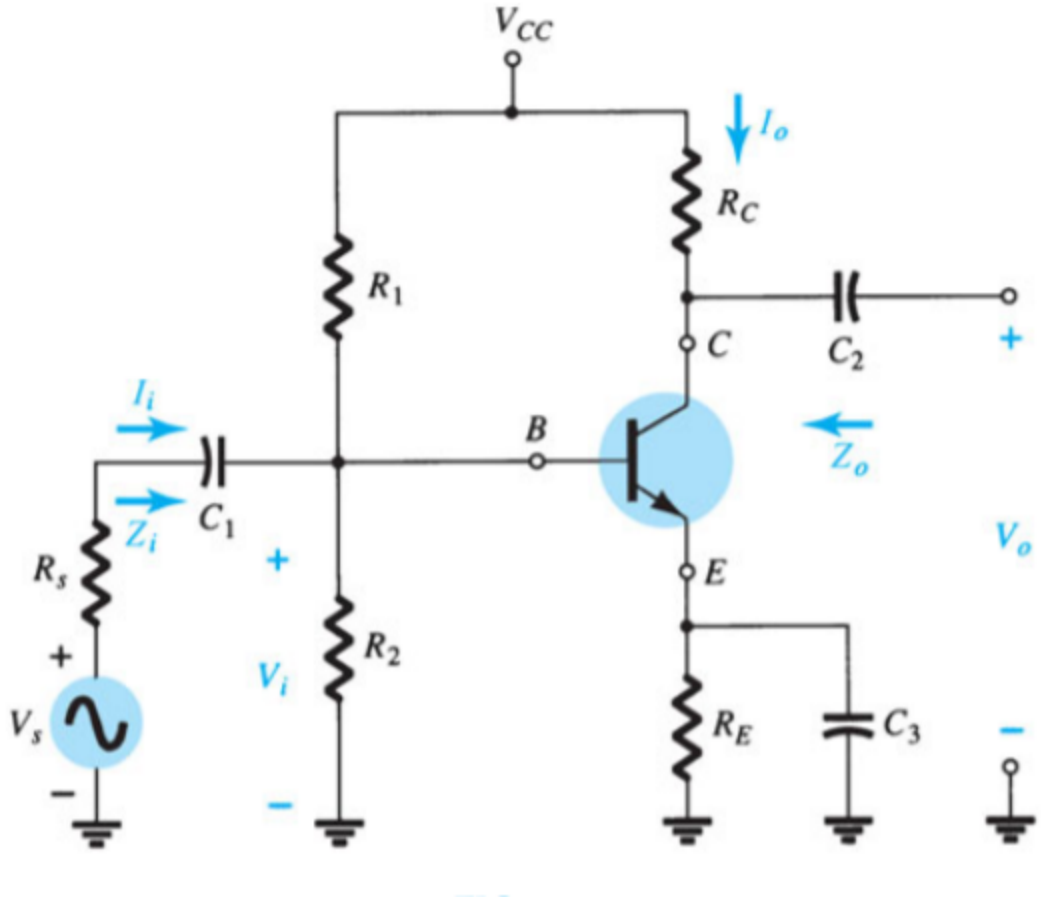


(a)



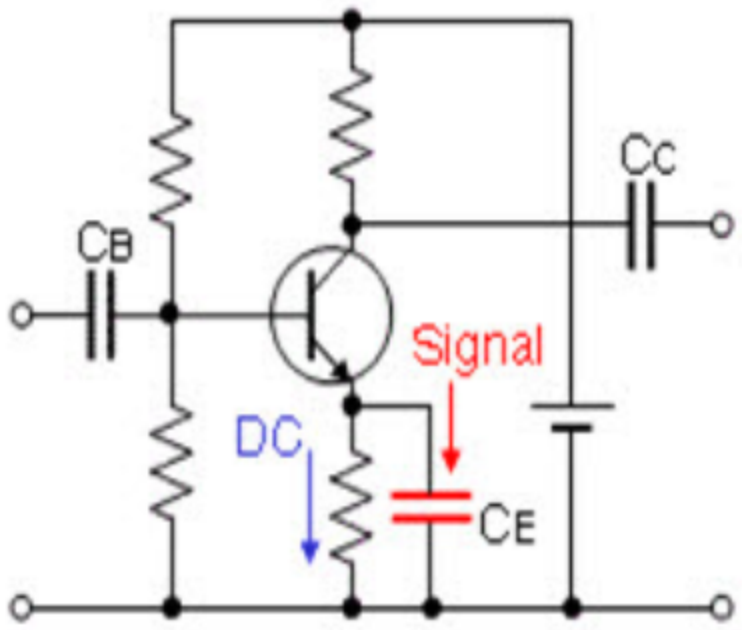
(b)

CE Amplifier

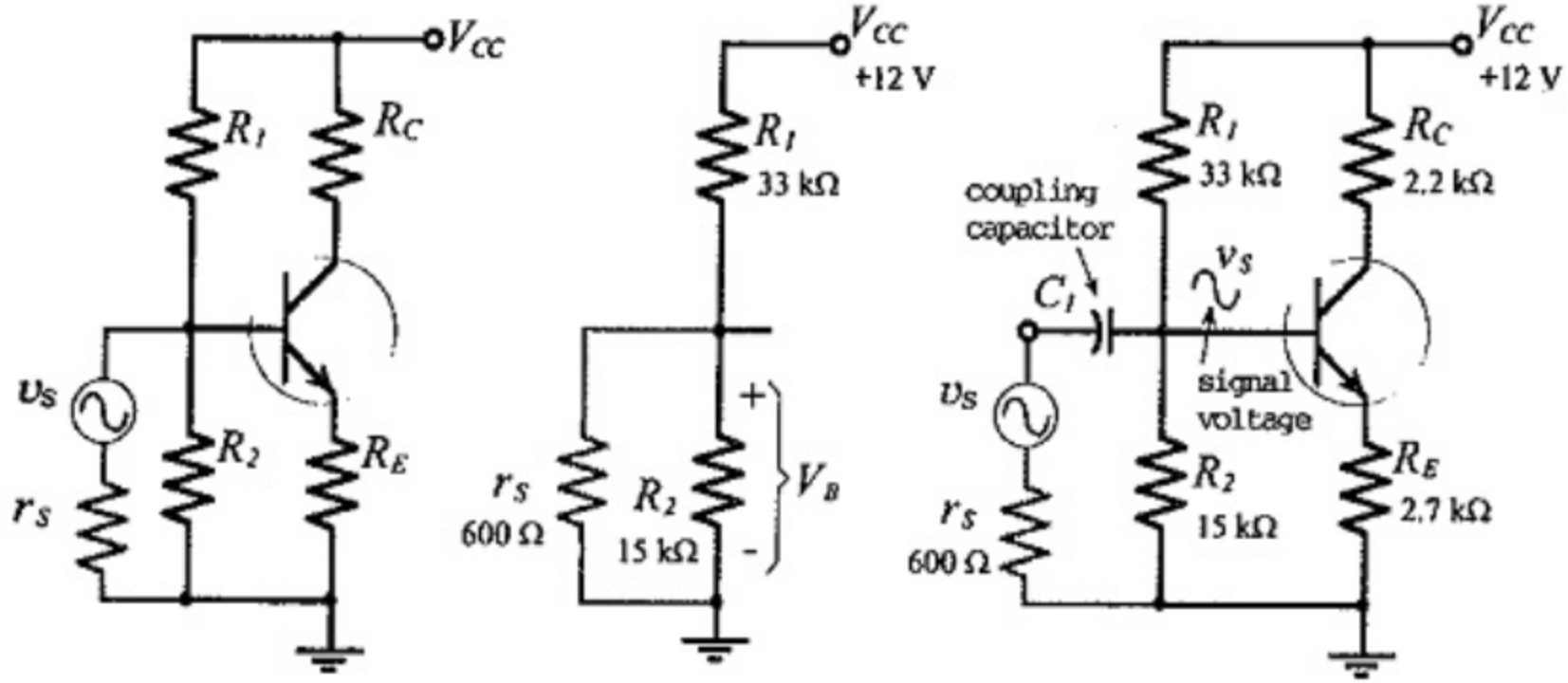


Role of Emitter bypass capacitor

When an emitter resistance is added in a CE (Common Emitter) amplifier, its voltage gain is reduced, but the input impedance increases. Whenever bypass capacitor is connected in parallel with an emitter resistance, the voltage gain of CE amplifier increases. If the bypass capacitor is removed, an extreme degeneration is produced in the amplifier circuit and the voltage gained will be reduced.



Role of Coupling capacitor

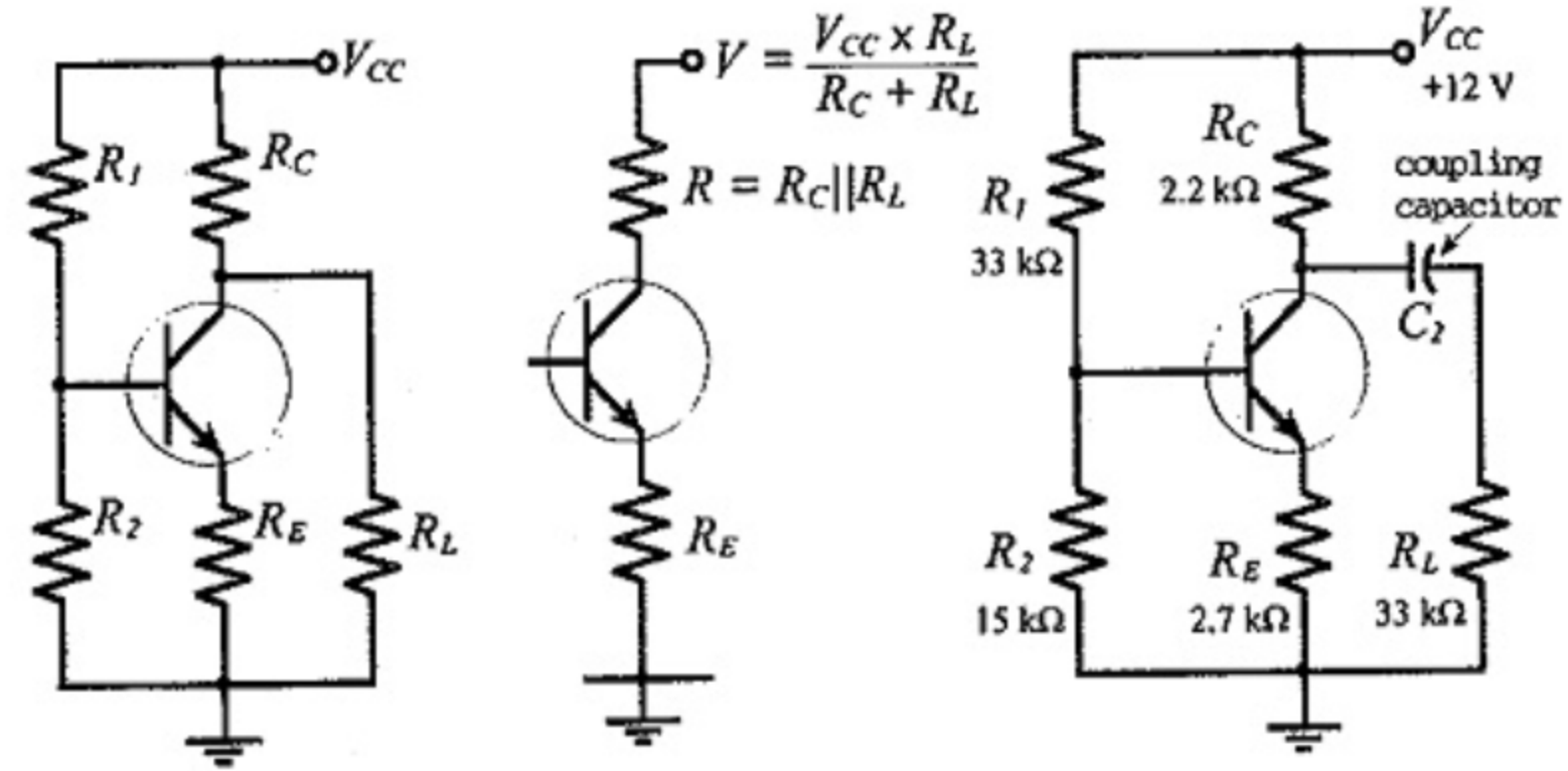


(a) Signal source **incorrectly** *direct-coupled* to the circuit

(b) V_B is altered by the *dc-coupled* signal source

(c) Signal source *capacitor-coupled* to the circuit

Role of Coupling capacitor



(a) Load resistor **incorrectly** direct-coupled to the circuit

(b) The collector voltage is altered by the direct-coupled load

(c) Load resistor *capacitor-coupled* to the circuit

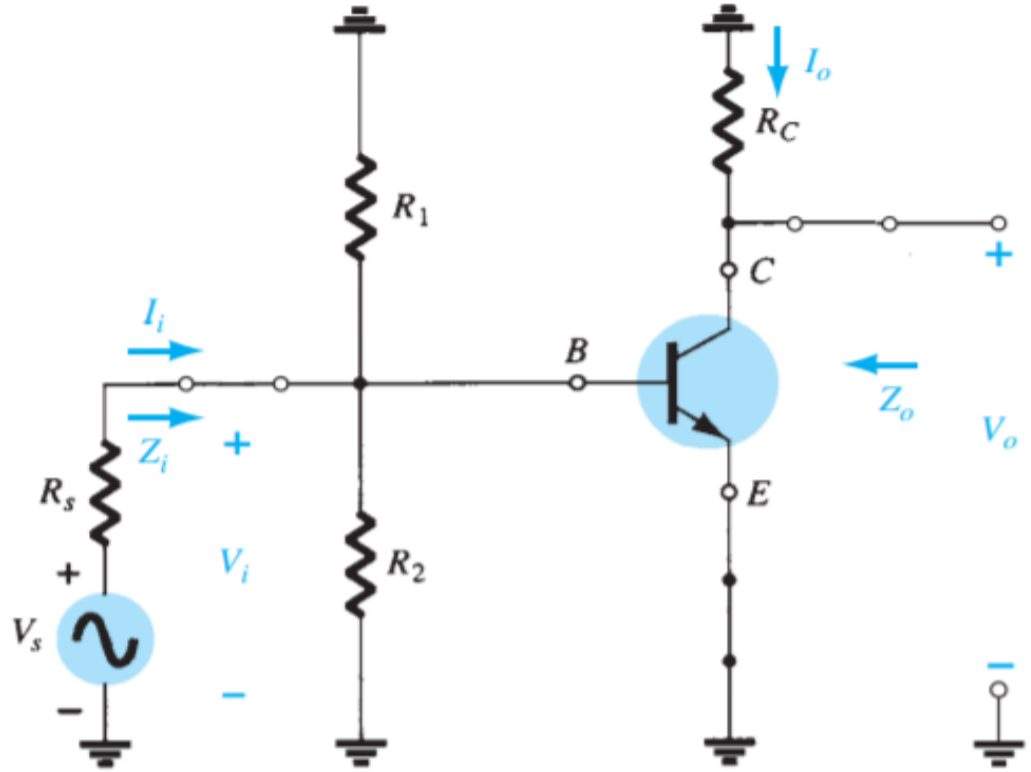
Small signal AC equivalent circuit of CE amplifier

1.Setting all dc sources to zero and replacing them by a short-circuit equivalent

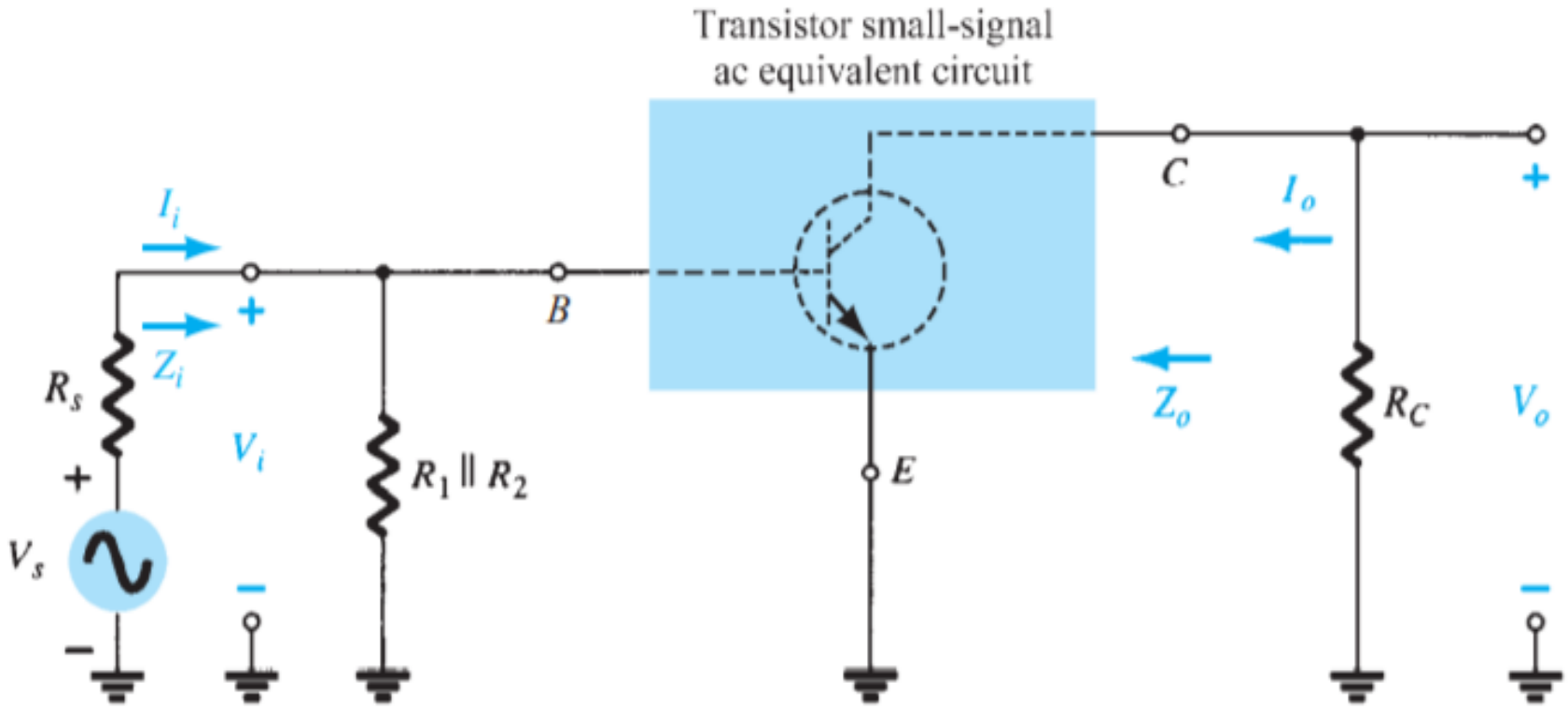
2. Replacing all capacitors by a short-circuit equivalent

3. Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2

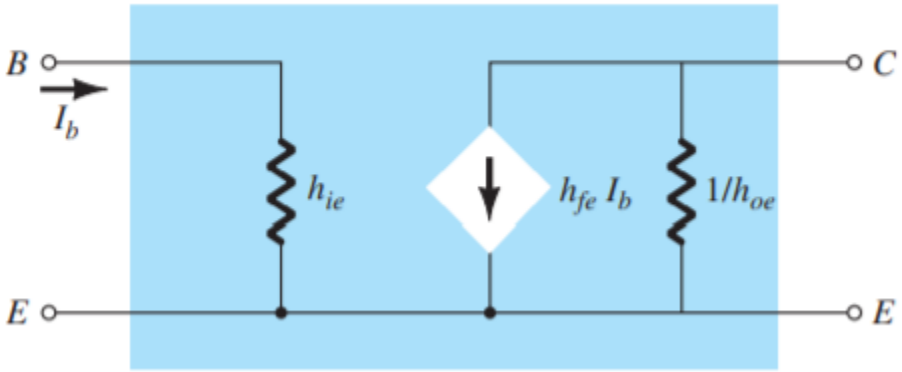
4. Redrawing the network in a more convenient and logical form



Small signal AC equivalent circuit of CE amplifier



Approximate hybrid equivalent circuit of transistor in CE configuration



CE Amplifier Circuit

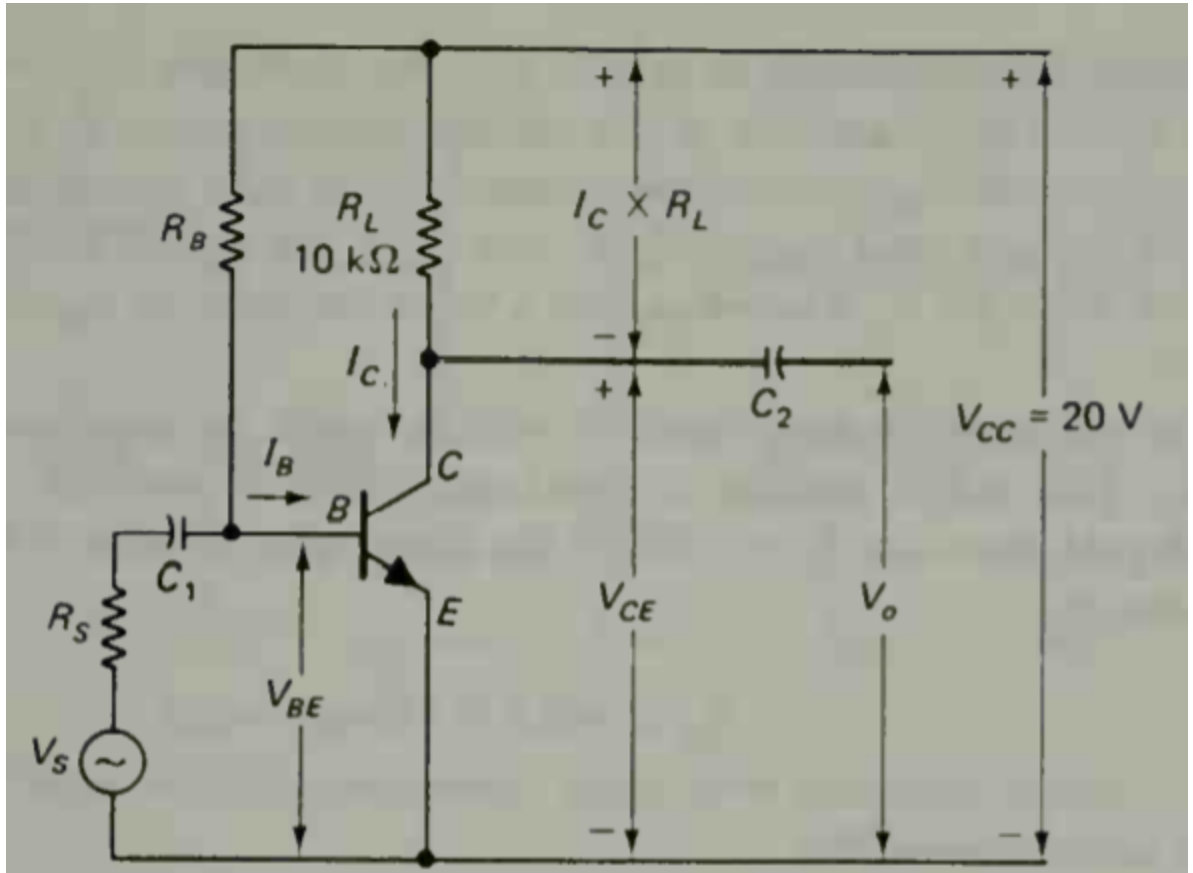


Figure 6-1. Common emitter circuit.

CE Amplifier AC equivalent Circuit

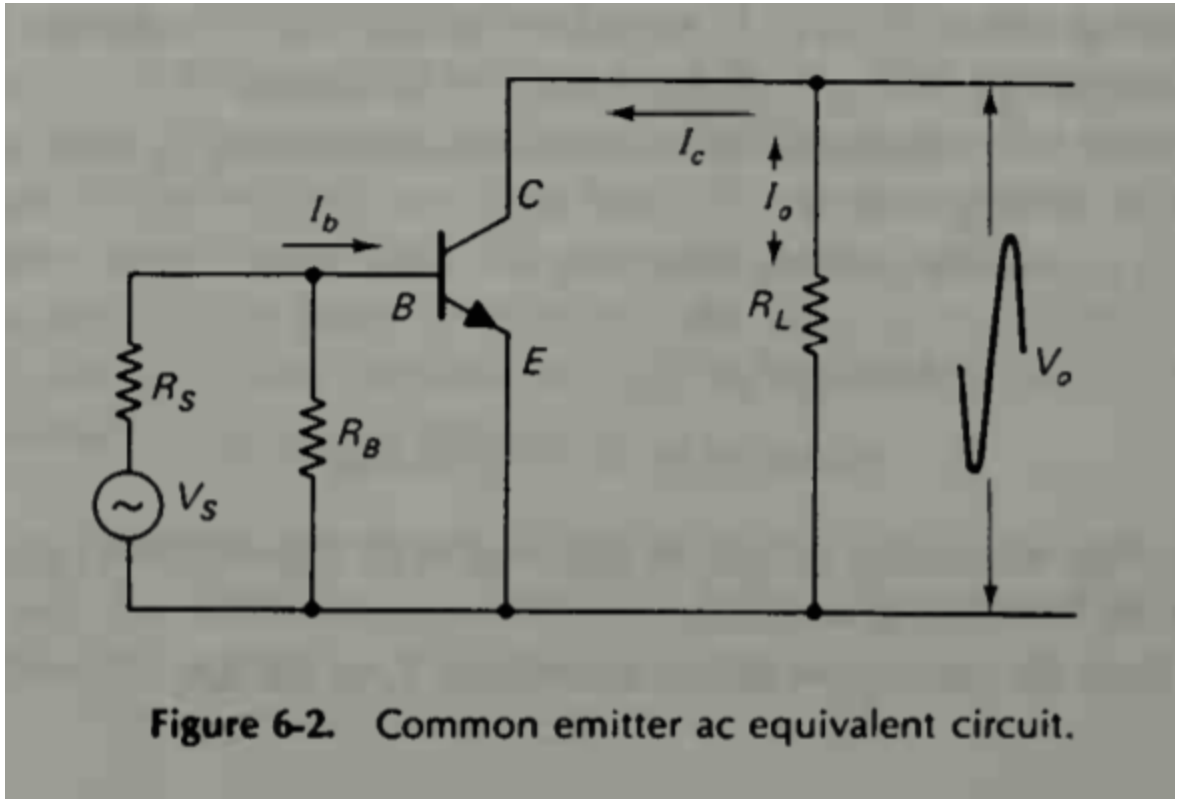


Figure 6-2. Common emitter ac equivalent circuit.

CE Amplifier AC equivalent Circuit using h-parameters

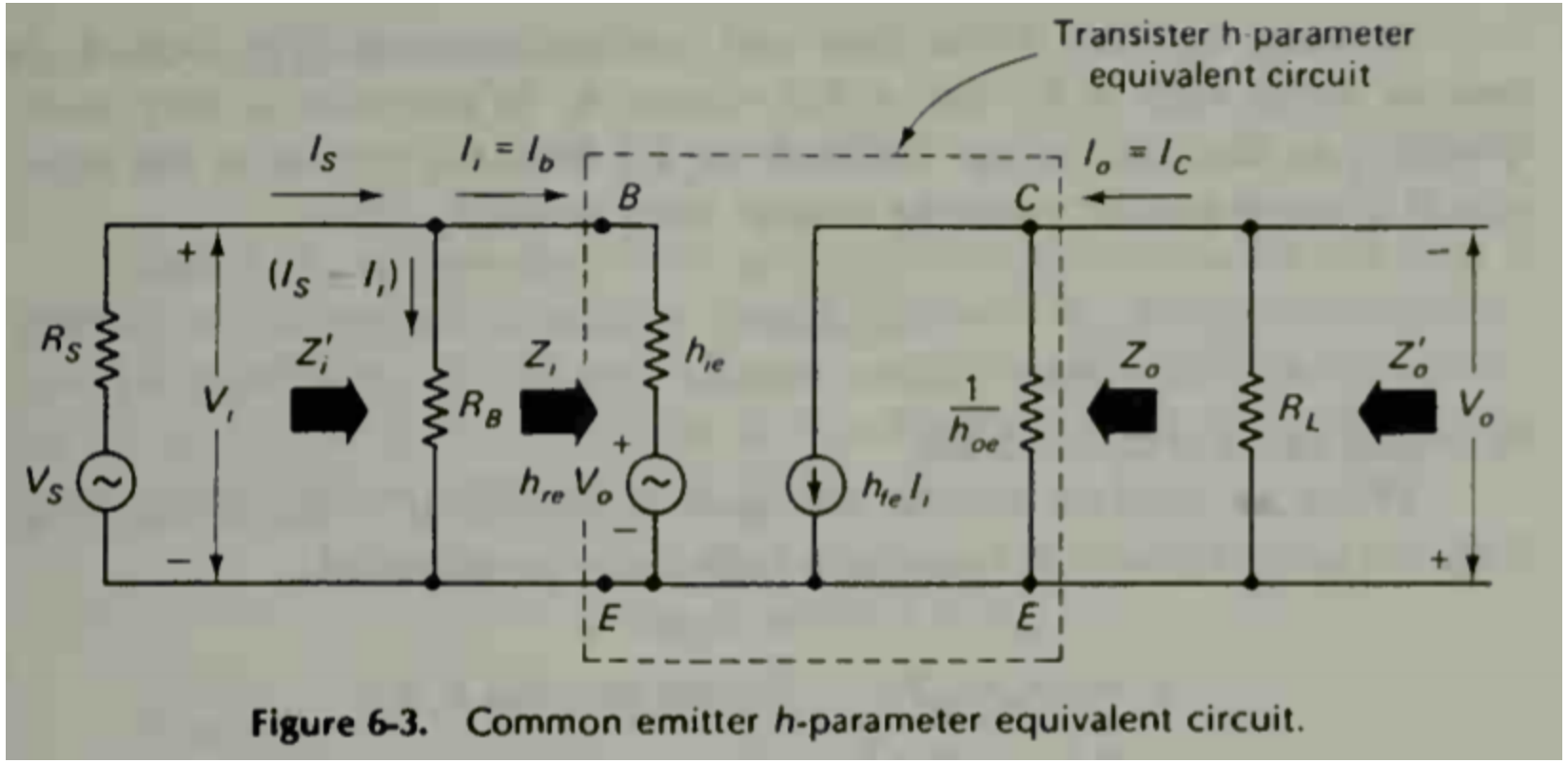


Figure 6-3. Common emitter *h*-parameter equivalent circuit.

Derivation of input impedance, output impedance, voltage gain and current gain

For a CE circuit, h_{re} is normally a very small quantity so that $h_{re}V_o$ is much smaller than the voltage drop across h_{ie}.

Input impedance

Input impedance to base of transistor = $Z_i = h_{ie}$

Input impedance of the circuit = $Z_i' = R_B \parallel Z_i$

Output impedance

To determine output impedance, set $V_i = 0, I_b = 0, h_{fe}I_b = 0$, Therefore

Output impedance of transistor = $Z_o = {}^{1}/_{h_{oe}}$

Output impedance of circuit = $Z_o' = {}^{1}/_{h_{oe}} \parallel R_L \cong R_L$

Derivation of input impedance, output impedance, voltage gain and current gain

Voltage gain

Voltage gain = $A_V = \frac{V_o}{V_i}$

$V_o = -I_C R_L$, $V_i = h_{ie} I_b$, $I_C = h_{fe} I_b$

$A_V = \frac{-I_C R_L}{h_{ie} I_b} = \frac{-h_{fe} R_L}{h_{ie}}$

Current gain

Current gain of transistor = $\frac{I_C}{I_b} = h_{fe}$

Circuit current gain = $A_i = \frac{I_C}{I_S}$

$$I_b = I_S \frac{R_B}{R_B + Z_i}$$

$$\frac{I_b}{I_S} = \frac{R_B}{R_B + Z_i}$$

$$A_i = \frac{I_C}{I_b} \times \frac{I_b}{I_S}$$

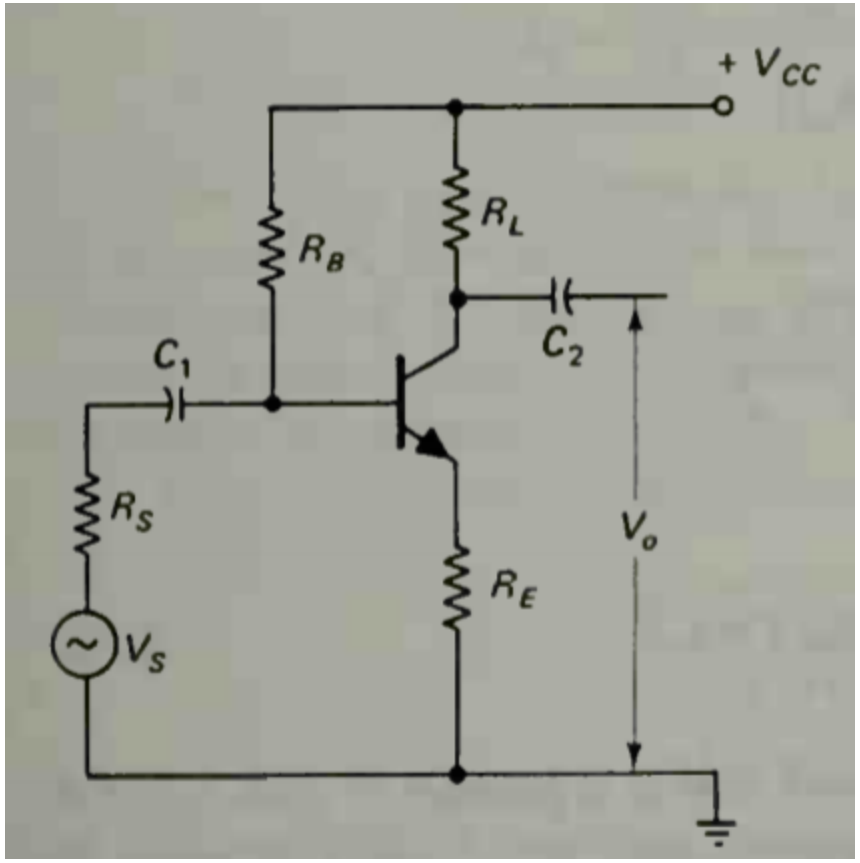
$$A_i = h_{fe} \frac{R_B}{R_B + Z_i}$$

Power gain

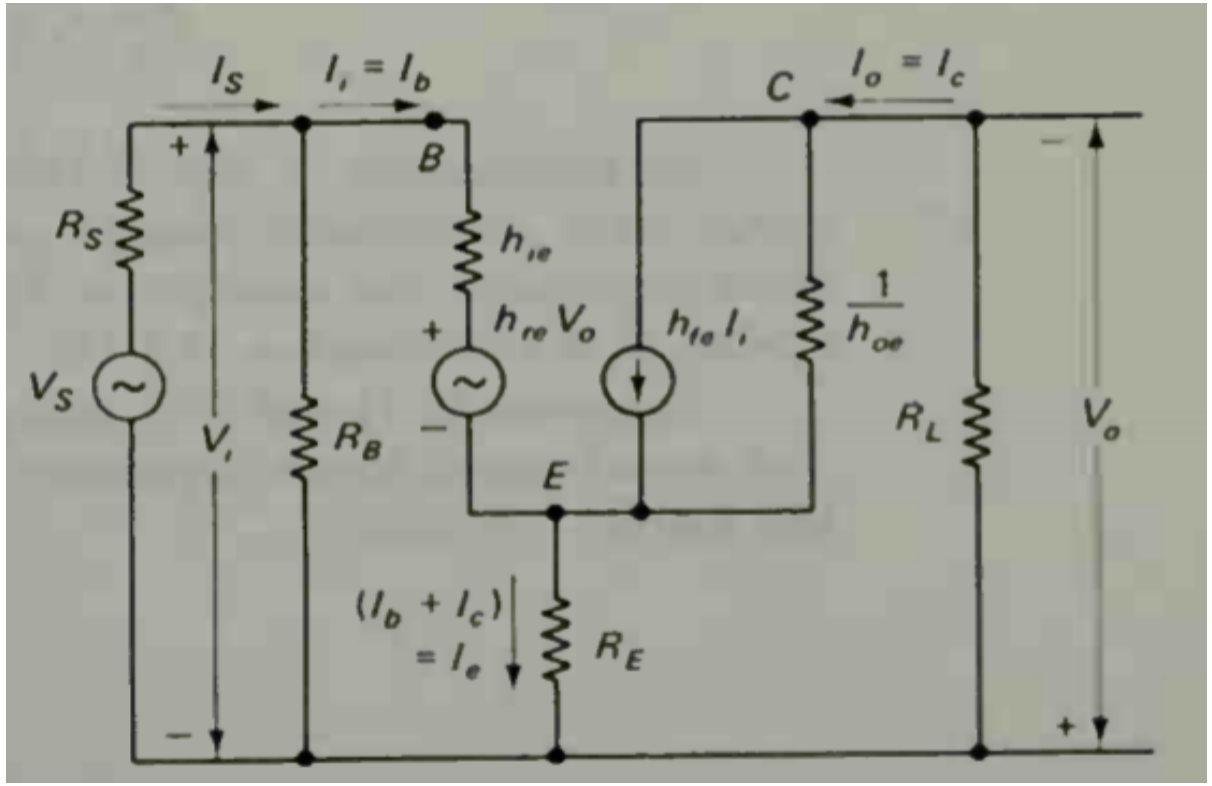
Power gain = $A_p = \frac{P_o}{P_i} = \frac{V_o I_o}{V_i I_i}$

$$A_p = A_V \times A_i$$

CE Amplifier Circuit with emitter unbypassed



CE Amplifier AC equivalent Circuit using h-parameters with emitter unbypassed



Derivation of input impedance, output impedance, voltage gain and current gain with emitter unbypassed

Input impedance

$$V_i = h_{ie}I_b + I_eR_E$$

$$V_i = h_{ie}I_b + (I_b+I_c)R_E$$

$$V_i = h_{ie}I_b + I_bR_E + h_{fe}I_bR_E$$

$$V_i = I_b\left[h_{ie} + R_E(1 + h_{fe})\right]$$

Input impedance to base of transistor = $Z_i = \frac{V_i}{I_b} = h_{ie} + R_E(1 + h_{fe})$

$$Z_i \cong h_{fe}R_E$$

Input impedance of the circuit = $Z_i' = R_B \parallel Z_i$

Output impedance

To determine output impedance, set $V_i = 0, I_b = 0, h_{fe}I_b = 0$, Therefore

Output impedance of transistor = $Z_o = {}^{1}/_{h_{oe}}$

Output impedance of circuit = $Z_o' = {}^{1}/_{h_{oe}} \parallel R_L \cong R_L$

Voltage gain

Voltage gain = $A_V = \frac{V_o}{V_i}$

$V_o = -I_C R_L$, $V_i = I_b\left[h_{ie} + R_E\left(1 + h_{fe}\right)\right]$, $I_C = h_{fe}I_b$

$$A_V = -\frac{h_{fe}R_L}{h_{ie} + R_E\left(1 + h_{fe}\right)}$$

$R_E\left(1 + h_{fe}\right) \ggg h_{ie}$,

$$A_V = -\frac{h_{fe}R_L}{h_{fe}R_E} = -\frac{R_L}{R_E}$$

Current gain

Current gain of transistor = $\frac{I_C}{I_b} = h_{fe}$

Circuit current gain = $A_i = \frac{I_C}{I_S}$ $; I_b = I_S \frac{R_B}{R_B + Z_i}$

$$\frac{I_b}{I_S} = \frac{R_B}{R_B + Z_i}$$

$$A_i = \frac{I_C}{I_b} \times \frac{I_b}{I_S}$$

$$A_i = h_{fe} \frac{R_B}{R_B + Z_i}$$

Power gain

Power gain = $A_p = \frac{P_o}{P_i} = \frac{V_o I_o}{V_i I_i}$

$$A_p = A_V \times A_i$$

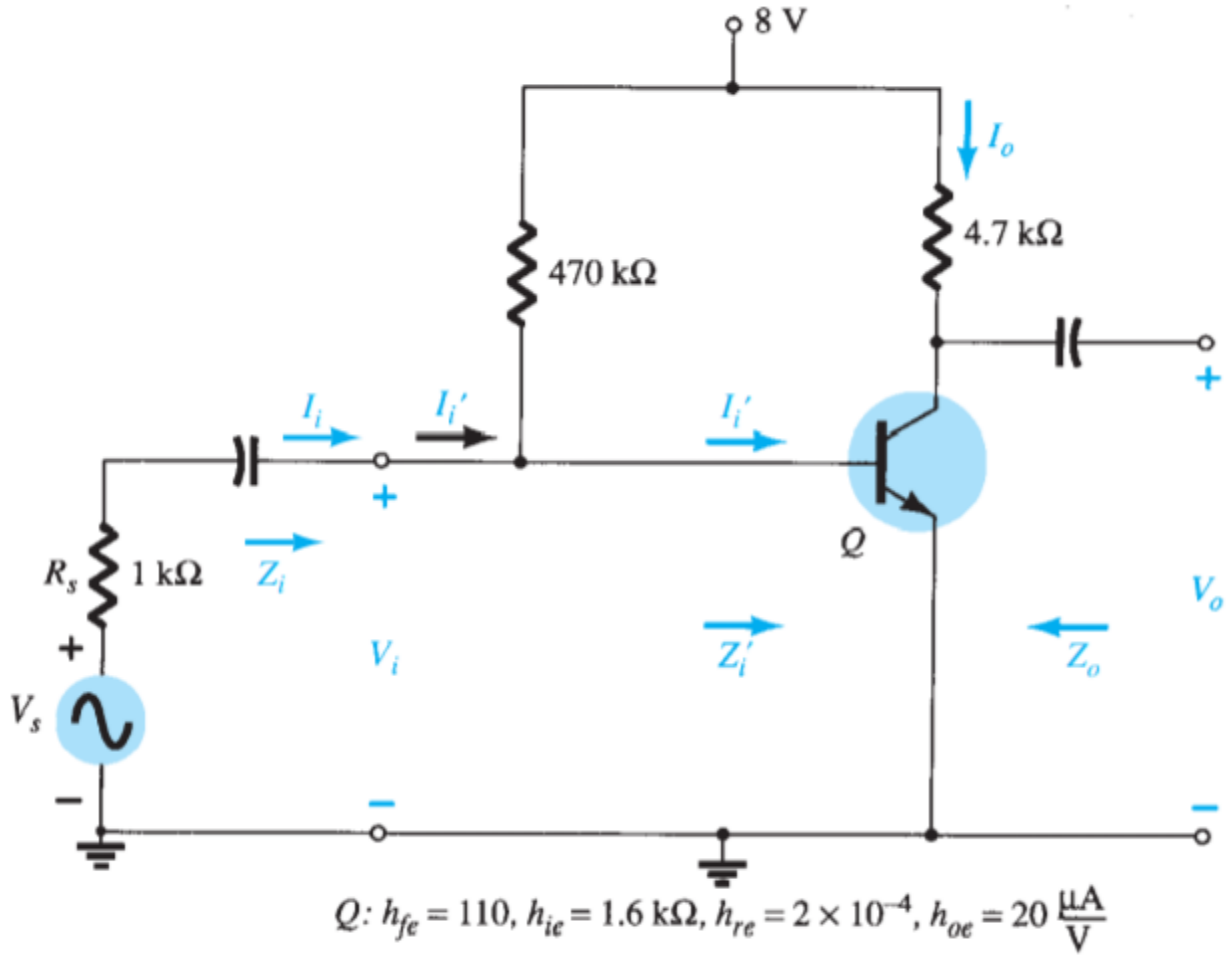
Class work 3

1. A common emitter circuit uses a transistor with $h_{fe} = 40$, $h_{ie} = 1\ K\Omega$ and $h_{oe} = 10^{-6}$ S. Load resistance $R_L = 3.3\ K\Omega$ and bias resistance $R_B = 120\ K\Omega$. Calculate the input impedance, output impedance, voltage gain, current gain and power gain.

2. In the above circuit, if an emitter resistance of 330 Ω is included, then calculate the input impedance, output impedance, voltage gain, current gain and power gain.

Class work 3

3. Determine the input impedance, output impedance, voltage gain, current gain for the following network. Also draw the complete hybrid ac equivalent circuit.



Class work 3

4. Determine the input impedance, output impedance, voltage gain, current gain for the following network. Also draw the complete hybrid ac equivalent circuit. Given $h_{fe} = 100$, $h_{ie} = 1\ K\Omega$ and $h_{oe} = 25 \times 10^{-6}$ S. $R_1 = 20\ K\Omega$ and $R_2 = 10\ K\Omega$.