

MODULE ISyllabus

Bipolar Junction Transistors: Review of BJT characteristics -

Operating point of BJT - Factors affecting stability

of Q Point. DC Biasing - Biasing circuits: fixed bias, collector to base bias, voltage divider bias, role of emitter resistance in bias stabilisation.

Stability factors (Derivation of stability factors for Voltage Divider Biasing only). Numerical problems.

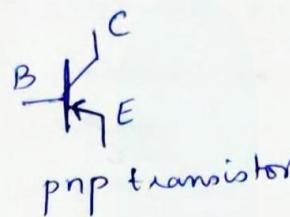
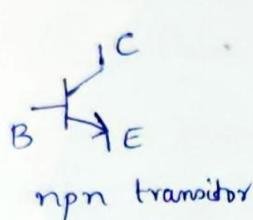
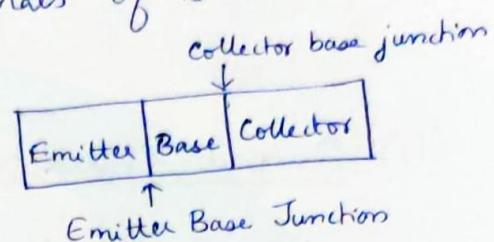
Bias compensation using diode & thermistor.

BJT Model - h parameter model of BJT in CE configuration. Small signal low frequency ac equivalent circuit of CE amplifier. - Role of coupling capacitors & emitter bypass capacitor. Calculations of amplifier gains & impedances using h parameter equivalent circuit.

Bipolar Junction Transistor (BJT)

BJT is a type of transistor that uses both electrons and holes as charge carriers.

BJT is a 3 terminal device consisting of 2 pn junctions. The 3 terminals of BJT are Base (B), Emitter (E) & Collector (C).



Characteristics of BJT in CE (Common Emitter) Configuration.

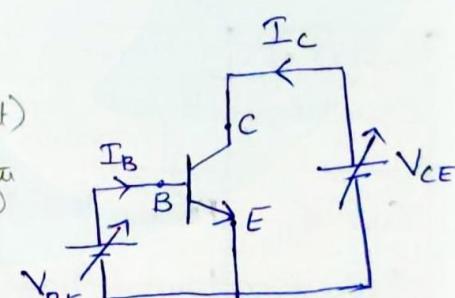
In CE configuration:

i/p current is I_B (Base current)

i/p voltage " V_{BE} (Base Emitter voltage)

o/p current " I_C (Collector current)

o/p voltage is V_{CE} (Collector-Emitter voltage)



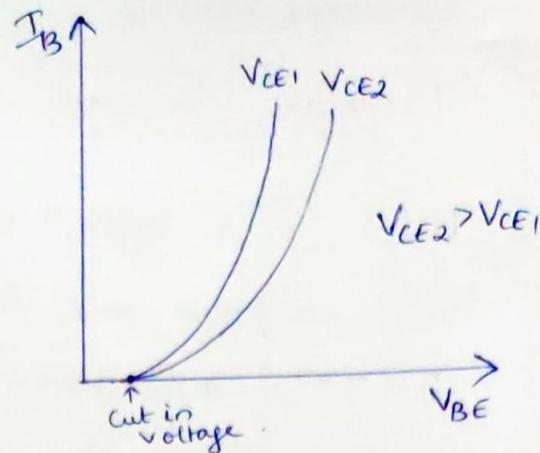
a) Input Characteristics

It is the curve between i/p current (I_B)

& i/p voltage (V_{BE}) at constant o/p voltage (V_{CE}).

If V_{BE} is less than cut-in voltage then $I_B = 0$.

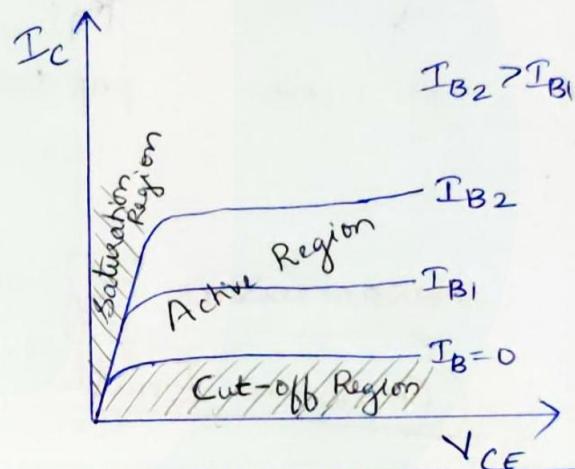
For $V_{BE} >$ cut-in voltage, I_B increases as shown.



(b) Output Characteristics.

It is the curve between o/p current (I_C) & o/p voltage (V_{CE}) at constant i/p current (I_B).

O/p chara can be divided into 3 regions:



Region of Operation	Biassing of Base Emitter Junction	Collector Base Jn.	Transistor is	Application
Cut-off	Reverse Biased	Reverse Biased	Off	Open Switch
Saturation	Forward Biased	Forward Biased	On	Closed Switch
Active	Forward Biased	Reverse Biased	On	Amplifier. $\rightarrow I_C \propto$

DC Load Line & Q-point

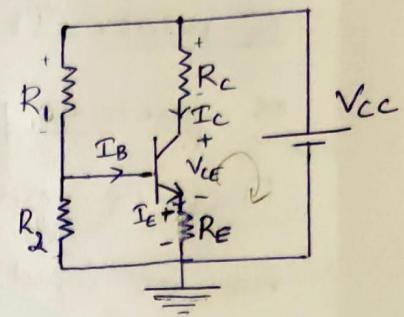
Consider a voltage divider bias circuit:

Collector loop eq is

$$-I_E R_E - V_{CE} - I_C R_C + V_{CC} = 0 \quad (\text{But } I_E \approx I_C)$$

$$-I_C R_E - V_{CE} - I_C R_C + V_{CC} = 0$$

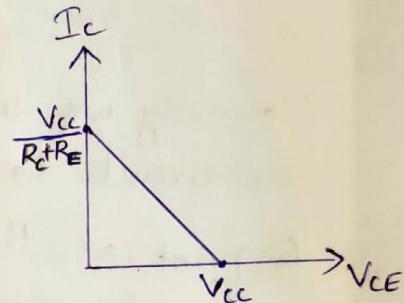
$$V_{CC} = V_{CE} + I_C (R_C + R_E) \quad \text{---(1)}$$



$$\text{When } I_C = 0, \text{ eq (1)} \Rightarrow V_{CE} = V_{CC}$$

$$\text{When } V_{CE} = 0, \quad I_C = \frac{V_{CC}}{R_C + R_E}$$

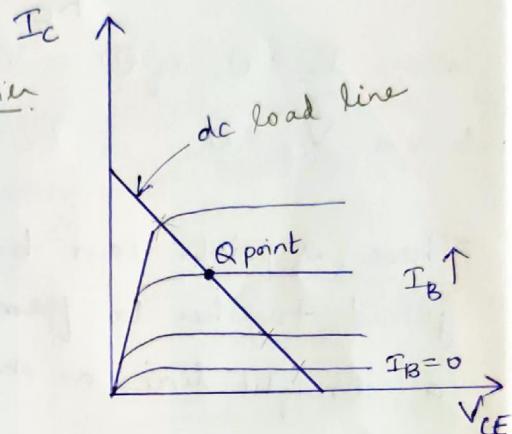
These 2 points can be joined together to form a straight line as shown.



- The straight line on the output characteristics that represents all the possible combinations of I_C & V_{CE} is known as load line.
- If load line is drawn, only when DC biasing is given to the transistor then such a load line is called DC load line
- The load line drawn when ac i/p signal is also applied along with dc voltages is known as AC load line.

Q. The intersection of the dc bias value of I_B with the dc load line determines the Q point. It is also known as dc bias point or quiescent point or dc operating point.

This Q point identifies I_C & V_{CE} when no ac input signal is applied at the base terminal.



(July 2017) Factors for selecting Q point for an amplifier.

Normally we design the circuit to have

Q point at the centre to obtain

optimum ac operation known as midpoint biasing.

When an ac signal is applied to the base of the transistor, I_C & V_{CE} will both vary around this Q point values.

When Q point is centered, I_C & V_{CE} can make the max possible transitions above & below their initial dc values.

When Q point is above (or below) the center of the load line, if signal may cause the transistor to saturate (or cut-off). This may cause a portion of the ip signal to be clipped.

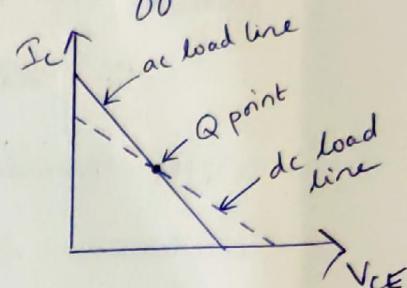
If the signal gets clipped then it is not suitable for amplification. So Q-point has to be at the centre of dc load line.

AC Load line

The load line drawn when an ac i/p signal is also applied along with dc voltages is known as AC load line.

It will not follow the plot of the dc load line because dc load of an amplifier is different from the ac load.

Q -point is common to both dc & ac load lines.



The ac load line will give the max possible o/p voltage swing (max peak to peak o/p voltage V_{pp}) for a given amplifier. This max V_{pp} is known as the compliance of the amplifier.

Why Stability of Q-point is important?

Once the Q-point is designed & fixed, it should remain constant irrespective of internal or external variations like variations in temperature, power supply fluctuations, aging of components & replacement of elements.

Any variation in Q point may cause transistor to deviate from its designed region of operation & will distort the o/p waveform. If thermal

Thermal Runaway.

The leakage current I_{Co} doubles for every 10° rise in temperature, i.e. it is extremely temperature dependent.

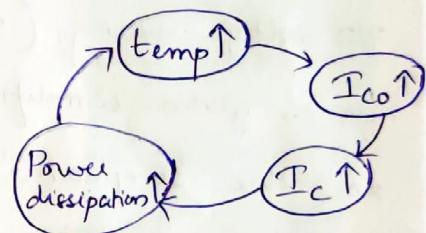
$$\text{Collector current, } I_C = \beta I_B + (1+\beta) I_{Co}$$

$I_B \rightarrow$ Base current, $\beta \rightarrow$ Current gain.

With increase in temp, I_{Co} increases & $\therefore I_C$ increases. \therefore Collector power dissipation increases which raises the junction temp that leads to further increase in I_C .

The process is cumulative & may lead to eventual destructions

of transistor. This phenomenon is known as thermal runaway.



KtuQbank Factors Affecting Stability of Q-point.

In an amplifier the collector current, I_c is sensitive to each of the following parameters:

- (i) β
 - (ii) V_{BE} (Base emitter voltage)
 - (iii) I_{CO} (Reverse saturation current)
- } Temperature sensitive quantities.

- I_{CO} doubles for every $10^\circ C$ rise in temperature.
- V_{BE} decreases by 2.5mV per $^\circ C$ rise in temperature.

So the most important one is Thermal stability.

- Thermal stability means how stable I_c & V_{CE} remain when circuit temperature changes.

- V_{BE} largely depends on base current I_B & I_B is related to I_c by the eq

$$I_c = \beta I_B + (1+\beta) I_{CO}$$

If temp \uparrow , $I_{CO} \uparrow$, $\therefore I_c \uparrow$, \therefore power dissipation \uparrow , so temp \uparrow . This is cumulative & can cause thermal runaway.

- The process of making operating point independent of temp changes or inherent variations in transistor parameters is known as stabilization.
- Stabilization of operating point (Q-point) means stabilization of I_c against changes in transistor parameters.

Stability Factor

Stability factor is defined as the rate of change of collector current w.r.t change in various transistor parameters like I_{C0} , V_{BE} & β .

Its value has to be less.

(i) Stability factor, S

- It is the rate of change of collector current w.r.t reverse saturation current while keeping β & V_{BE} constant.

$$S = \frac{dI_c}{dI_{C0}} = \frac{\Delta I_c}{\Delta I_{C0}}$$

$| \beta \& V_{BE} \rightarrow \text{constant}$

(ii) Stability factor, S' or S_v

- It is the rate of change of collector current w.r.t base-emitter voltage while keeping β & I_{C0} constant.

$$S' = \frac{dI_c}{dV_{BE}}$$

$| \beta \& I_{C0} \rightarrow \text{const.}$

(iii) Stability factor, S'' or S_β

- It is the rate of change of collector current w.r.t β while keeping V_{BE} & I_{C0} constant.

$$S'' = \frac{dI_c}{d\beta}$$

$| V_{BE} \& I_{C0} \rightarrow \text{const.}$

General Expression for Stability Factor.

Collector current, $I_C = \beta I_B + (1+\beta) I_{Co}$.

Differentiating it w.r.t I_C

$\beta \rightarrow$ current gain
 $I_B \rightarrow$ Base current
 $I_{Co} \rightarrow$ reverse saturation current.

$$\frac{dI_C}{dI_C} = \frac{d}{dI_C} (\beta I_B) + \frac{d}{dI_C} [(1+\beta) I_{Co}]$$

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta) \frac{dI_{Co}}{dI_C} \quad (\because \beta \rightarrow \text{constant})$$

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta) \times \frac{1}{s} \quad (\because s = \frac{dI_C}{dI_{Co}})$$

$$1 - \beta \frac{dI_B}{dI_C} = \frac{(1+\beta)}{s}$$

✓

$$\therefore \boxed{s = \frac{1+\beta}{1 - \beta \cdot \frac{dI_B}{dI_C}}}$$

Need of Biasing Circuit / Biasing

The circuit used for transistor biasing is called the biasing circuit. Biasing of BJT means applying external voltages to it. To use BJT for any application (e.g. amplification), the 2 junctions have to be properly biased. The most basic application of transistor is amplification for which BE junction is forward biased & CB jn is reverse biased.

Ktu Q bank

The biasing circuit will:

(i) Set the operating point in the middle of the active region of transistor characteristics.

(ii) Stabilize the collector current against temperature variations.

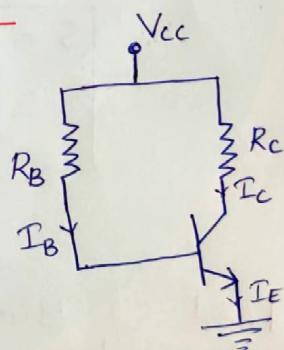
(iii) Ensure that operating point is independent of transistor parameters so that operating point is not shifted if the transistor is replaced by another transistor of the same type.

Different Biasing Circuits

① Fixed Bias (Base Bias) Circuit

- Simplest Biasing ckt

Base current (I_B) is determined by supply voltage (V_{cc}) & base resistance (R_B).

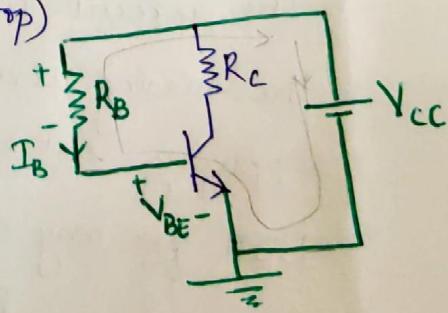


Consider the i/p portion (i.e base loop)

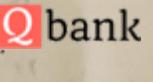
✓

$$V_{cc} - V_{BE} - I_B R_B = 0$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B}$$



If current (i.e base current) is given above

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KtuQbank V_{CC} & V_{BE} are constant & once R_B is fixed,
 I_B will be constant or fixed. \therefore The name
fixed bias ckt.

Stability factor, $s = \frac{1 + \beta}{1 - \frac{dI_B}{dI_C}}$

But $\frac{dI_B}{dI_C} = 0$ ($\because I_B$ is constant).

$\therefore s = \underline{\underline{1 + \beta}} \quad \text{--- } ①$

($\beta \approx 100$)

This is a large quantity, \therefore fixed bias ckt has poor stability, & thermal runaway may occur. \therefore Fixed bias ckt is rarely used.

O/p current, $I_C = \beta I_B$

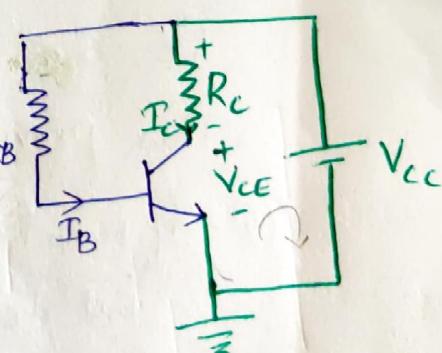
$$= \beta \left[\frac{V_{CC} - V_{BE}}{R_B} \right] \quad \text{--- } ②$$

Consider the o/p portion (i.e collector loop)

$$-V_{CE} - I_C R_C + V_{CC} = 0$$

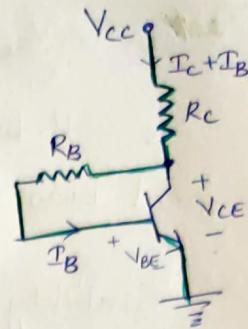
$$V_{CE} = V_{CC} - I_C R_C \quad \text{--- } ③$$

This is the o/p voltage.



② Collector to Base Bias

Here one end of base resistor (R_B) is connected to the base & the other end to the collector.



Consider i/p (or base) loop:

$$\text{Vcc} = (I_C + I_B) R_C + I_B R_B + V_{BE}$$

$$= I_B (R_B + R_C) + I_C R_C + V_{BE}$$

$$I_B = \frac{\text{Vcc} - V_{BE} - I_C R_C}{R_B + R_C} \quad \text{--- } ①$$

$$I_C = \beta I_B$$

$$\therefore \frac{dI_B}{dI_C} = -\frac{R_C}{R_B + R_C}$$

$$\begin{aligned} S &= \frac{1 + \beta}{1 - \beta \cdot \frac{dI_B}{dI_C}} = \frac{1 + \beta}{1 - \beta \left(-\frac{R_C}{R_B + R_C} \right)} \\ &= \frac{1 + \beta}{1 + \beta \left(\frac{R_C}{R_B + R_C} \right)} \end{aligned}$$

i.e $S < (1 + \beta)$.

\therefore This provides better thermal stability than fixed bias ckt.

(OR If temp \uparrow , then $I_C \uparrow$. But from eq ①, as $I_C \uparrow$, $I_B \downarrow$ But $I_C = \beta I_B$. \therefore The reduced base current in turn reduces the original increase in I_C . So stability improves)

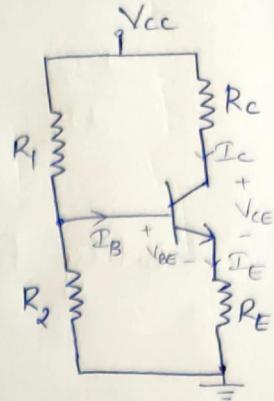
Consider o/p (or collector) loop

$$\text{Vcc} = (I_C + I_B) R_C + V_{CE}$$

\therefore o/p voltage, $V_{CE} = \text{Vcc} - (I_C + I_B) R_C$

③ Voltage Divider Bias & its Stability Factor (Potential Divider Bias / Self Bias)

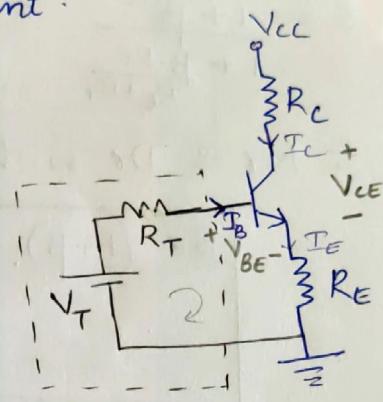
Resistors R_1 & R_2 constitute a voltage divider that divides the supply voltage V_{cc} to produce the base bias voltage.



For analyzing, voltage divider network is replaced with its Thvenin equivalent.

Thvenin equivalent

$$\text{voltage, } V_T = V_{cc} \times \frac{R_2}{R_1 + R_2} \quad \text{--- (1)}$$



Equivalent resistance,

$$R_T = R_1 // R_2$$

$$R_T = \frac{R_1 \cdot R_2}{R_1 + R_2} \quad \text{--- (2)}$$

Apply KVL for i/p (or base) loop.

$$-V_T + I_B R_T + V_{BE} + I_E R_E = 0.$$

But $I_E = I_B + I_C$.

$$\therefore -V_T + I_B R_T + V_{BE} + (I_B + I_C) R_E = 0.$$

$$-V_T + I_B (R_E + R_T) + V_{BE} + I_C R_E = 0$$

$$\therefore I_B = \frac{V_T - V_{BE} - I_C R_E}{R_E + R_T} \quad \text{--- (3)}$$

Differentiating eq (3) w.r.t I_C .

$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_E + R_T}$$

Stability factor, $s = \frac{1 + \beta}{1 - \beta \cdot \frac{dI_B}{dI_C}}$

$$s = \frac{1 + \beta}{1 - \beta \left(\frac{-R_E}{R_E + R_T} \right)}$$

$$s = \frac{1 + \beta}{1 + \frac{\beta \cdot R_E}{R_E + R_T}} = \frac{(1 + \beta) \times (R_E + R_T)}{(R_E + R_T) + \beta R_E}$$

\therefore N_r & D_r with R_E

$$\boxed{s = (1 + \beta) \cdot \frac{1 + \frac{R_T}{R_E}}{1 + \beta + \frac{R_T}{R_E}}} \quad \text{--- (4)}$$

The value of stability factor is considerably improved with voltage divider bias.

If $\frac{R_T}{R_E}$ is very small then $s \approx 1$, i.e. small value of s indicates higher stability. So decrease R_T .

However if $\frac{R_T}{R_E}$ increases, then s will increase & it will result in poor stability.

So the voltage divider bias is relatively stable against changes in β .

Ktu Q bank collector current, $I_C = \beta I_B$

if current: eq ③ becomes
 $I_B = \frac{V_T - V_{BE} - (\beta I_B) R_E}{R_E + R_T}$

$$I_B (R_E + R_T) = V_T - V_{BE} - \beta I_B R_E$$

$$I_B [(1+\beta) R_E + R_T] = V_T - V_{BE}$$

$$\underline{\underline{I_B = \frac{V_T - V_{BE}}{(1+\beta) R_E + R_T}}} \quad \text{is } \underline{\text{i/p current.}}$$

o/p current, $I_C = \beta I_B$

$$= \beta \left[\frac{V_T - V_{BE}}{(1+\beta) R_E + R_T} \right]$$

Apply KVL in collector (or o/p) loop.

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$= I_C R_C + V_{CE} + I_C \left[1 + \frac{1}{\beta} \right] R_E$$

o/p voltage. $V_{CE} = V_{CC} - I_C \left[R_C + R_E \left(1 + \frac{1}{\beta} \right) \right]$

$$\begin{aligned} I_E &= \underline{\underline{I_B + I_C}} \\ &\quad \text{very small.} \\ &= \underline{\underline{\frac{I_C}{\beta} + I_C}} \\ &= \underline{\underline{I_C \left[1 + \frac{1}{\beta} \right]}} \end{aligned}$$

Role of Emitter resistance in Bias Stabilisation.

Stability factor $\underline{\underline{s}}$ of voltage divider bias, i.e. eq ④

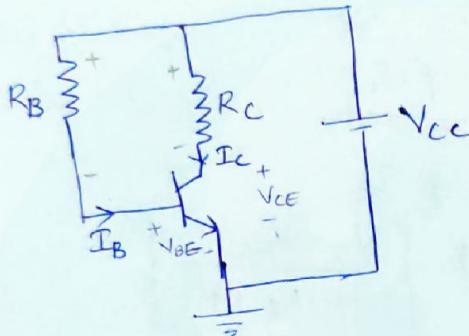
$$s = \frac{1 + \beta}{1 + \left(\frac{\beta \cdot R_E}{R_E + R_T} \right)}$$

If $R_E = 0$, then $s = \underline{\underline{1 + \beta}}$.

So if emitter resistance (R_E) is not present then 's' will have a large value. But due to R_E value of 's' is $\underline{\underline{\text{Ktu Q bank}}}$ to a very small value & so thermal stability is greatly improved.

Q.1. In a fixed bias circuit. $R_B = 280\text{ k}\Omega$, $R_C = 2\text{ k}\Omega$, $V_{CC} = 12\text{ V}$. Transistor is silicon with $h_{FE} = 100$. Find (i) I_B (ii) stability factor, s (iii) Q point values of I_C & V_{CE} (iv) V_C (v) V_B .

Ans.



$$\begin{aligned}
 R_B &= 280\text{ k}\Omega, \\
 R_C &= 2\text{ k}\Omega \\
 V_{CC} &= 12\text{ V} \\
 h_{FE} &= \beta = 100 \\
 \text{Assume } V_{BE} &= \frac{0.7\text{ V}}{(\because \text{Si})}
 \end{aligned}$$

(i)

$$\begin{aligned}
 I_B &= \frac{V_{CC} - V_{BE}}{R_B} \\
 &= \frac{12 - 0.7}{(280 \times 10^3)} = 40.36 \times 10^{-6} \text{ A} \\
 &= \underline{\underline{40.36 \mu\text{A}}}.
 \end{aligned}$$

(ii) $s = 1 + \beta$ (for fixed bias)

$$= 1 + 100 = \underline{\underline{101}}$$

(iii) Q point: $I_C = \beta I_B = 100 \times (40.36 \times 10^{-6})$
 $= \underline{\underline{4.03 \times 10^{-3} \text{ A}}} = \underline{\underline{4.03 \text{ mA}}}$

$$V_{CC} = I_C R_C + V_{CE}$$

$$\begin{aligned}
 V_{CE} &= V_{CC} - I_C R_C \\
 &= 12 - (4.03 \times 10^{-3} \times 2 \times 10^3) \\
 &= \underline{\underline{3.94\text{ V}}}
 \end{aligned}$$

iv) $V_C = ?$

$$V_{CE} = V_C - V_E$$

Emitter (E) is directly connected to ground

$$\therefore V_E = 0$$

$$V_C = V_{CE} + V_E$$

$$= 3.94 + 0 = \underline{\underline{3.94V}}$$

v) $V_B = ?$

$$V_{BE} = V_B - V_E$$

$$0.7 = V_B - 0$$

$$\therefore V_B = \underline{\underline{0.7V}}$$

Q.2. A transistor with $\beta = 100$ is used in CE configuration. The collector resistance is $R_C = 1k\Omega$ & $V_{CC} = 20V$. Assuming $V_{BE} = 0V$, find value of collector to base bias circuit such that quiescent collector emitter voltage is 4V.

Ans. $\beta = 100, R_C = 1k\Omega,$

$$V_{CC} = 20V, V_{BE} = 0$$

$$V_{CE} = 4V.$$

'E' is connected directly to ground.

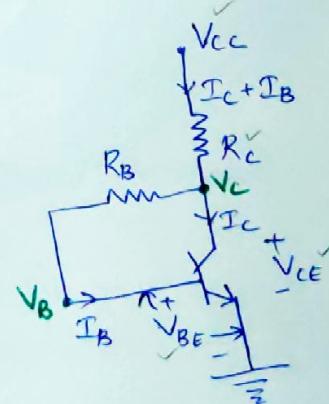
$$\text{so } V_E = 0$$

$$\therefore V_{CE} = V_C - V_E$$

$$V_C = V_{CE} + V_E = \underline{\underline{4V}}.$$

$$V_{BE} = V_B - V_E$$

$$V_B = V_{BE} + V_E = 0 + 0 = \underline{\underline{0V}}$$



KtuQbank

$$V_{CC} - V_C = (I_C + I_B) R_C .$$

$$20 - 4 = (I_C + I_B) \times (1 \times 10^3)$$

$$\begin{aligned} I_C + I_B &= \frac{16 \text{ mA}}{1 \times 10^3} \\ &= 16 \times 10^{-3} \quad \text{--- (1)} \end{aligned}$$

Voltage across R_B

$$V_C - V_B = I_B R_B .$$

$$4 - 0 = I_B \times R_B . \quad \text{--- (2)}$$

$$\text{Eq (1). } I_C = \beta I_B$$

$$\therefore (1 + \beta) I_B = 16 \times 10^{-3}$$

$$101 \times I_B = 16 \times 10^{-3}$$

$$I_B = \frac{1.58 \times 10^{-4}}{\underline{\underline{101}}} \text{ A : --- (3)}$$

$$\begin{aligned} I_C &= \beta I_B \\ &= 100 \times (1.58 \times 10^{-4}) \\ &= \underline{\underline{1.58 \times 10^{-2}}} \text{ A .} \end{aligned}$$

Substitute (3) in eq (2)

$$4 = I_B R_B$$

$$\therefore R_B = \frac{4}{I_B} = \frac{4}{1.58 \times 10^{-4}} = \underline{\underline{25.32 \times 10^5 \Omega}}$$

Q.3] Obtain the operating point set by the voltage divider bias circuit for an NPN CE transistor

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with $\beta = 50$ & $V_{BE} = 0.7V$. Given $V_{CC} = 18V$, $R_1 = 82k\Omega$, $R_2 = 22k\Omega$, $R_C = 5.6k\Omega$ & $R_E = 1.2k\Omega$. [6]

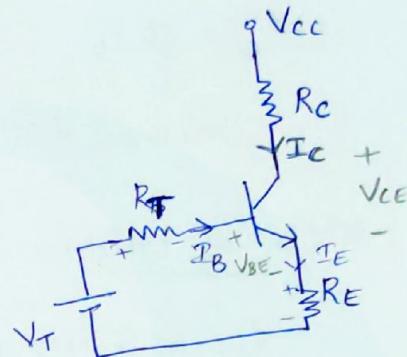
Ans.

$$\beta = 50, V_{BE} = 0.7V$$

$$V_{CC} = 18V, R_1 = 82k\Omega$$

$$R_2 = 22k\Omega, R_C = 5.6k\Omega,$$

$$R_E = 1.2k\Omega.$$



$$R_T = \frac{R_1 \cdot R_2}{R_1 + R_2}$$

$$= \frac{82k \times 22k}{82k + 22k} = \frac{(82 \times 22) \times 10^6}{(82+22) \times 10^3} = \underline{\underline{17.35k\Omega}}$$

$$V_T = V_{CC} \times \frac{R_2}{R_1 + R_2}$$

$$= 18 \times \frac{22k}{(82k+22k)} = \underline{\underline{3.81V}}$$

Operating point $\rightarrow V_{CE}, I_c \sim$

KVL in base loop

$$V_T = I_B R_T + V_{BE} + I_E R_E$$

$$= I_B R_T + V_{BE} + (1+\beta) I_B R_E$$

$$V_T = I_B [R_T + (1+\beta) R_E] + V_{BE}$$

$$3.81 = I_B [17.35 + (1+50) \times 1.2] \times 10^3 + 0.7$$

$$\begin{aligned} I_E &= I_C + I_B \\ &= \beta I_B + I_B \\ &= (1+\beta) I_B \end{aligned}$$

$$= 78.55 I_B \times 10^3 + 0.7$$

$$\begin{aligned} I_B &= \frac{3.81 - 0.7}{78.55 \times 10^3} \\ &= 3.96 \times 10^{-5} \text{ A} \\ &= 39.6 \times 10^{-6} \text{ A} = \underline{\underline{39.6 \mu\text{A}}} \end{aligned}$$

$$\begin{aligned} I_C &= \beta I_B \\ &= 50 \times 3.96 \times 10^{-5} = \underline{\underline{1.98 \text{ mA}}} \end{aligned}$$

KVL of collector loop

$$V_{cc} = I_c R_c + V_{CE} + I_E R_E$$

$$V_{CE} = V_{cc} - I_c R_c - I_E R_E$$

$$= 18 - (1.98 \times 10^3 \times 5.6 \times 10^3)$$

$$- (51 \times 39.6 \times 10^{-6} \times 1.2 \times 10^3)$$

$$= \underline{\underline{4.49 \text{ V}}}$$

$$\left. \begin{aligned} I_E &= (1+\beta) I_B \\ &= 51 \times I_B \end{aligned} \right.$$

∴ Operating point is $V_{CE} = \underline{\underline{4.49 \text{ V}}}, P_C = \underline{\underline{2 \text{ mA}}}$

- Q.4] Design voltage divider bias circuit to operate from a 12V supply. The bias conditions are $V_{CE} = 3\text{V}$, $V_E = 5\text{V}$ & $I_C = 1\text{mA}$. Also calculate the stability factor.

Ans.

$$V_{CC} = 12V$$

$$V_{CE} = 3V, V_E = 5V$$

$$I_C = 1mA$$

(Find $R_1, R_2, R_C, R_E, \beta$)

Assume $\beta = 100$.

$$I_C = \beta I_B$$

$$I_B = \frac{I_C}{\beta} = \frac{1mA}{100}$$

$$= \underline{\underline{0.01mA}} = \underline{\underline{10^{-2} \times 10^{-3}}} = \underline{\underline{10^{-5}A}}$$

$$I_E = I_C + I_B$$

$$= 1mA + 0.01mA = \underline{\underline{1.01 \times 10^{-3}A}}$$

V_E is given.

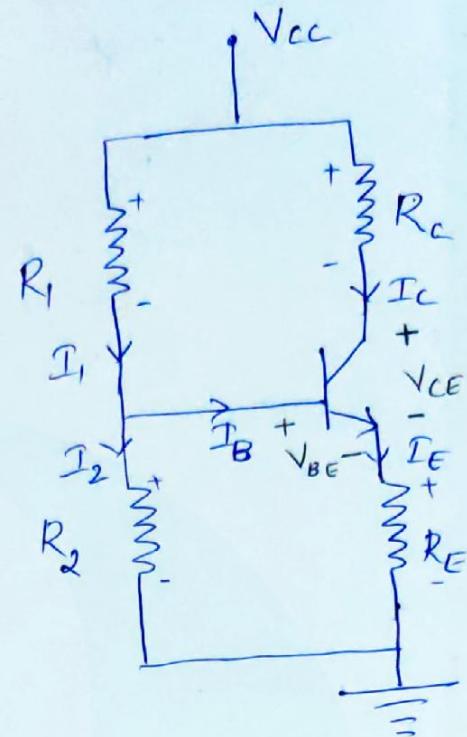
$$\text{Voltage across } R_E = V_E - 0 = V_E$$

$$\text{Also Voltage across } R_E = I_E R_E \quad (\rightarrow \text{ohm's law})$$

$$\therefore \checkmark V_E = \checkmark I_E R_E$$

$$R_E = \frac{V_E}{I_E} = \frac{5}{1.01 \times 10^{-3}} = \underline{\underline{4.95k\Omega}}$$

($R_E, I_E, V_{CE}, I_C, V_C, \therefore R_C \Rightarrow ?$)



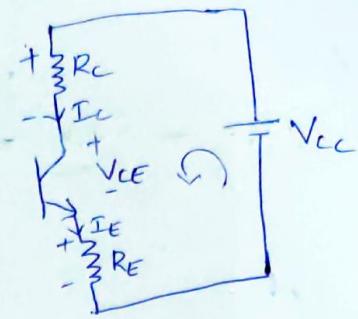
$$KtuQ \text{ bank} + I_C R_C + V_{CE} + I_E R_E = 0$$

$$-V_{CC} + I_C R_C + V_{CE} + V_E = 0$$

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C}$$

$$= \frac{12 - 3 - 5}{1 \times 10^{-3}}$$

$$R_C = \underline{4 k\Omega}$$



$R_1, R_2 \rightarrow ?$

$$\text{Assume } I_2 = 10 I_B$$

$$\begin{aligned} \therefore I_1 &= I_2 + I_B \\ &= 10 I_B + I_B = 11 I_B \end{aligned}$$

$$I_1 = 11 I_B = \underline{11 \times 10^{-5}} \text{ A}$$

$$I_2 = 10 I_B = \underline{10 \times 10^{-5}} \text{ A} = \underline{10^{-4}} \text{ A}$$

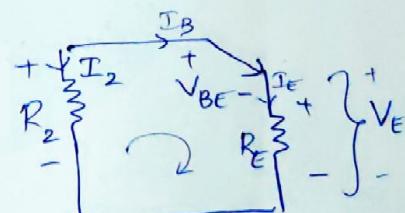
$$\text{Assume } V_{BE} = \underline{0.7 \text{ V}}$$

Apply KVL in R_2, R_E loop.

$$-I_2 R_2 + V_{BE} + I_E R_E = 0$$

$$I_2 R_2 = V_{BE} + V_E$$

$$\begin{aligned} R_2 &= \frac{V_{BE} + V_E}{I_2} = \frac{0.7 + 5}{10^{-4}} = 5.7 \times 10^4 \Omega \\ &= \underline{57 k\Omega} \end{aligned}$$



$R_1 \rightarrow ?$

$$-I_2 R_2 - I_1 R_1 + V_{cc} = 0.$$

$$I_1 R_1 = V_{cc} - I_2 R_2$$

$$R_1 = \frac{V_{cc} - I_2 R_2}{I_1}$$

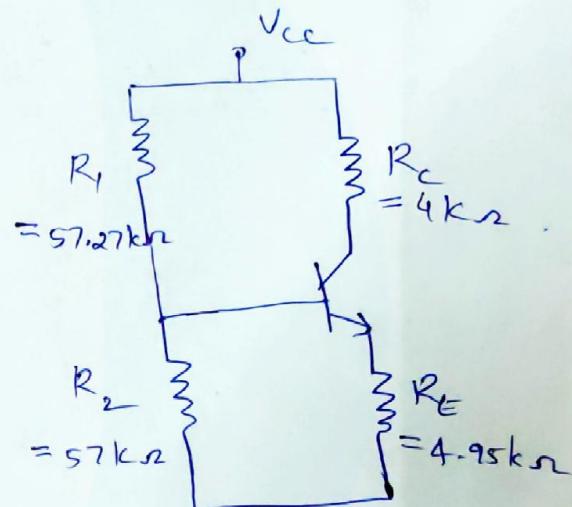
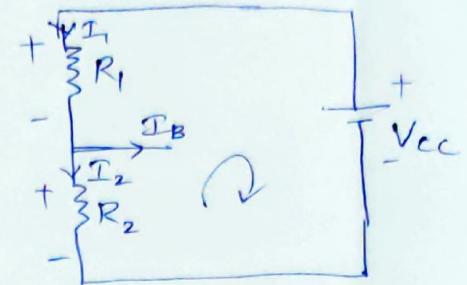
$$= \frac{12 - (10^{-4} \times 57 \times 10^3)}{11 \times 10^{-5}}$$

$$= \underline{\underline{57.27 \text{ k}\Omega}}.$$

$$s = \frac{1 + \beta}{1 + \left(\frac{\beta \times R_E}{R_E + R_T} \right)}$$

$$R_T = \frac{R_1 \cdot R_2}{R_1 + R_2}$$

$$= \frac{57.27 \text{ k} \times 57 \text{ k}}{57.27 \text{ k} + 57 \text{ k}} = \underline{\underline{28.57 \text{ k}\Omega}}$$



$$s = \frac{1 + \beta}{1 + \left(\frac{\beta \cdot R_E}{R_E + R_T} \right)} = \frac{(1 + 100)}{1 + \frac{100 \times 4.95 \times 10^3}{(4.95 \times 10^3) + (28.57 \times 10^3)}}$$

$$= \underline{\underline{6.4}}$$

Q. Design a voltage divider circuit for a
Silicon transistor with $h_{FE} = 100$ & $S \leq 8$.

Dec 2019.

The desired Q-point is $V_{CE} = 5V$, $I_C = 1mA$.
[10].

Assume $V_{CC} = 10V$, $R_E = 1k\Omega$

Ans.

$$h_{FE} = \beta = 100$$

$$S \leq 8$$

$$V_{CE} = 5V, I_C = 1mA$$

$$V_{CC} = 10V, R_E = 1k\Omega$$

Assume $V_{BE} = 0.7V$ (\because Si transistor)

$$I_C = \beta I_B$$

$$\therefore I_B = \frac{I_C}{\beta} = \frac{1mA}{100} = \underline{\underline{10^{-5} A}} = \underline{\underline{0.01mA}}$$

$$I_E = I_B + I_C$$

$$= 0.01mA + 1mA = \underline{\underline{1.01mA}}$$

$$(I_E, R_E, I_C, V_{CC}, V_{CE}, R_C)$$

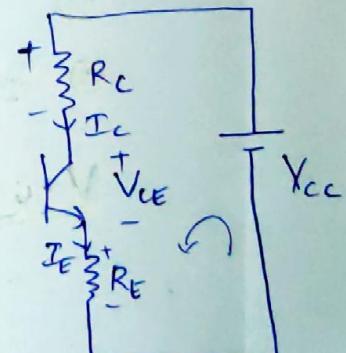
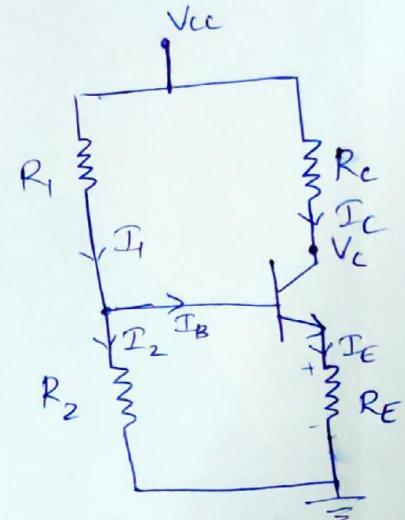
Apply KVL in outer o/p loop

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$$

$$R_C = \frac{V_{CC} - V_{CE} - I_E R_E}{I_C}$$

$$= \frac{10 - 5 - (1.01 \times 10^{-3} \times 1 \times 10^3)}{1 \times 10^{-3}}$$

$$\therefore R_C = \underline{\underline{3.99k\Omega}}$$



Value of 's' is given. (So that needs to be used for finding R_1 & R_2)

$$s = \frac{1 + \beta}{1 + \frac{\beta \cdot R_E}{R_T + R_E}} \quad \text{--- (1)}$$

$s \leq 8 \rightarrow \text{Take } s = 8$

\therefore eq (1) becomes

$$8 = \frac{1 + 100}{1 + \frac{100 \times 1k\Omega}{(R_T + 1k\Omega)}}$$

$$1 + \frac{100 \times 1k\Omega}{(R_T + 1k\Omega)} = \frac{101}{8}$$

$$\frac{100 \times 1k\Omega}{R_T + 1k\Omega} = \frac{101}{8} - 1$$

$$\frac{100 k\Omega}{(R_T + 1k\Omega)} = 11.625$$

$$\therefore R_T + 1k\Omega = \frac{100 k\Omega}{11.625}$$

$$\begin{aligned} R_T &= 8.60 k\Omega - 1k\Omega \\ &= \underline{\underline{7.6 k\Omega}}. \end{aligned}$$

$$R_T = \frac{R_1 \cdot R_2}{R_1 + R_2} \quad \text{--- (2)}$$

$$V_T = V_{cc} \times \frac{R_2}{R_1 + R_2} \quad \text{--- (3)}$$

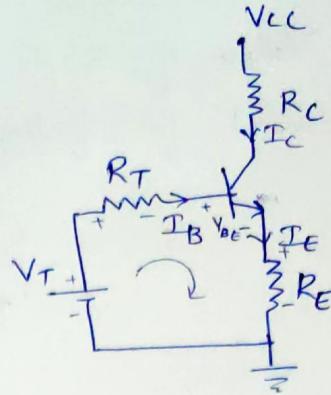
Apply KVL in i/p loop

$$-V_T + I_B R_T + V_{BE} + I_E R_E = 0$$

$$V_T = I_B R_T + V_{BE} + I_E R_E$$

$$= \left(10 \times 7.6 \times 10^3 \right) + 0.7 \\ + \left(1.01 \times 10^3 \times 1 \times 10^3 \right)$$

$$= \underline{1.786} \text{ V}$$



eq ② \div eq ③

$$\frac{R_T}{V_T} = \frac{\frac{R_1 \cdot R_2}{(R_1 + R_2)}}{\frac{V_{CC} \times R_2}{(R_1 + R_2)}} = \frac{R_1}{V_{CC}}$$

$$R_1 = V_{CC} \times \frac{R_T}{V_T} = 10 \times \frac{7.6 \times 10^3}{1.786} \\ = \underline{42.55 \text{ k}\Omega}$$

$$\frac{R_1}{R_2} + 1 = \frac{V_{CC}}{V_T}$$

$$\frac{R_1 + R_2}{R_2} = \frac{V_{CC}}{V_T}$$

$$\frac{R_1}{R_2} + 1 = \frac{V_{CC}}{V_T}$$

$$\frac{R_1}{R_2} = \frac{V_{CC}}{V_T} - 1 = \frac{10}{1.786} - 1 = 4.6$$

$$R_2 = \frac{R_1}{4.6} = \frac{42.55 \text{ k}}{4.6} = \underline{9.2 \text{ k}\Omega}$$

Q.
May
2019.

Design a voltage divider bias circuit to obtain the following specifications & determine the stability factor. Assume ratio of base current to the current through R_{B2} is 1:10.

Given $V_{cc} = 22V$, $\beta = 100$, $V_{CE} = 50\% \text{ of } V_{cc}$, $V_{RE} = 10\% \text{ of } V_{cc}$, $I_c = 0.8mA$ & $V_{BE} = 0.7V$. [6]

Ans. Given:

$$V_{cc} = 22V, \beta = 100.$$

$$V_{CE} = 50\% \times V_{cc} = \frac{50}{100} \times 22 \Rightarrow \\ = 11V.$$

$$V_{RE} = 10\% \times V_{cc}$$

$$= \frac{10}{100} \times 22 = 2.2V = I_E R_E \quad \text{--- ①}$$

$$I_c = 0.8mA$$

$$V_{BE} = 0.7V$$

Base current : Current through $R_{B2} = 1:10$.

$$I_B : I_2 = 1:10$$

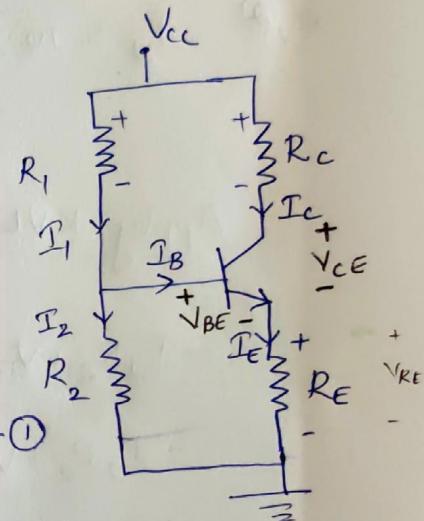
$$\frac{I_B}{I_2} = \frac{1}{10} \Rightarrow I_2 = 10 I_B \quad \text{--- ②}$$

From ckt:

$$I_1 = I_2 + I_B \\ = 10 I_B + I_B = \underline{\underline{11 I_B}} \quad \text{--- ③}$$

I_c is given so we can find I_B

$$I_c = \beta I_B$$



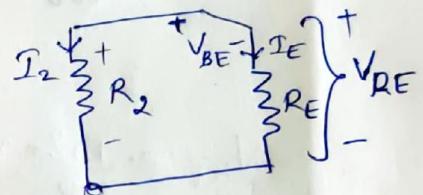
$$\therefore I_B = \frac{I_C}{\beta} = \frac{0.8 \text{ mA}}{100} = 0.8 \times 10^{-2} \text{ mA} \\ = 0.8 \times 10^{-5} \text{ A}$$

Eq 3 $\therefore I_1 = 11 I_B = 11 \times (0.8 \times 10^{-5}) \\ = 8.8 \times 10^{-5} \text{ A}$

Eq 2 $I_2 = 10 I_B = 10 \times (0.8 \times 10^{-5}) \\ = 8 \times 10^{-5} \text{ A}$

Apply KVL in R_2 loop.

$$-I_2 R_2 + V_{BE} + (I_E R_E) = 0$$



$$-I_2 R_2 + V_{BE} + V_{RE} = 0$$

$$R_2 = \frac{V_{BE} + V_{RE}}{I_2}$$

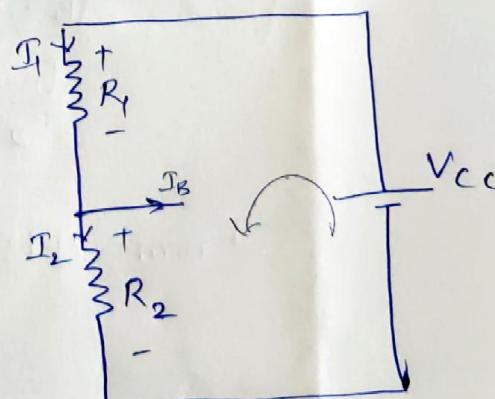
$$= \frac{0.7 + 2.2}{8 \times 10^{-5}} = \underline{\underline{36.25}} \text{ k}\Omega$$

Apply KVL in i/p loop

$$-V_{CC} + I_1 R_1 + I_2 R_2 = 0$$

$$I_1 R_1 = V_{CC} - I_2 R_2$$

$$R_1 = \frac{V_{CC} - I_2 R_2}{I_1}$$



$$= \frac{22 - (8 \times 10^{-5} \times 36.25 \times 10^3)}{(8.8 \times 10^{-5})}$$

$$= \underline{\underline{217.045}} \text{ k}\Omega$$

~~R₁ & R₂~~ ✓

Next R_C & R_E

$$I_E = I_B + I_C$$

$$= (0.8 \times 10^{-5}) + (0.8 \times 10^{-3})$$

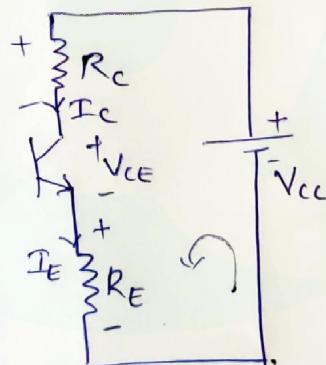
$$= \underline{\underline{8.08 \times 10^{-4}}} \text{ A}$$

Given: V_{RE} = 2.2 V

$$\therefore I_E R_E = 2.2$$

$$\therefore R_E = \frac{2.2}{8.08 \times 10^{-4}} = \underline{\underline{2.722}} \text{ k}\Omega$$

Apply KVL in collector loop

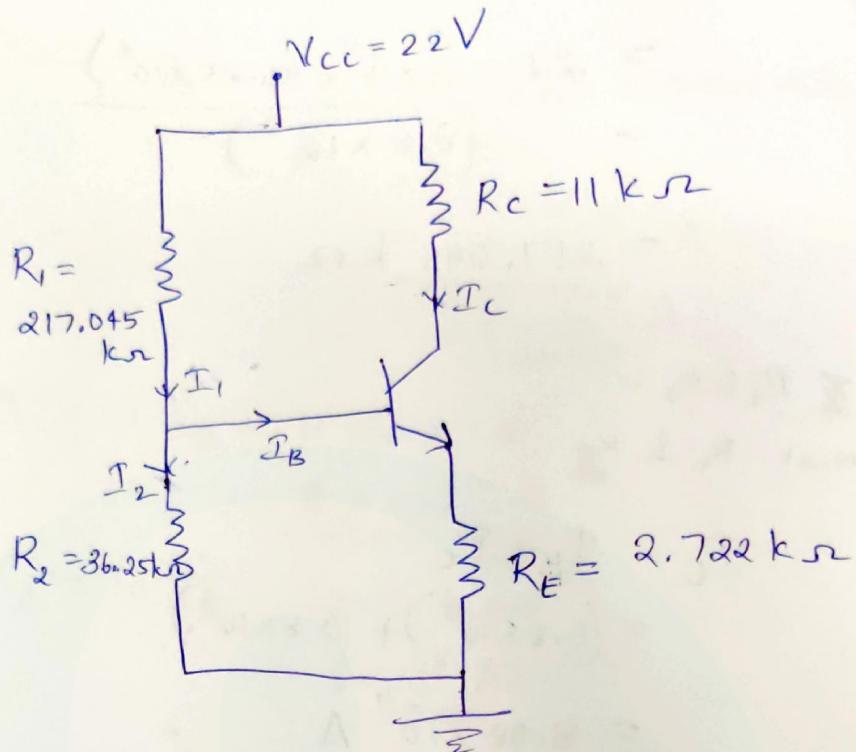


~~Voltage across R_C~~
~~I_C R_C = V_{CC}~~

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0.$$

$$I_C R_C = V_{CC} - \cancel{(I_E R_E)} - V_{CE}$$

$$R_C = \frac{V_{CC} - \cancel{V_{RE}} - V_{CE}}{I_C} = \frac{22 - 2.2 - 11}{0.8 \times 10^{-3}}$$



$$S = \frac{(1 + \beta)}{1 + \left(\frac{\beta \times R_E}{R_E + R_T} \right)}$$

$$R_T = \frac{R_1 \cdot R_2}{R_1 + R_2} = \frac{(217.05 \times 10^3) \times (36.25 \times 10^3)}{(217.05 \times 10^3) + (36.25 \times 10^3)}$$

$$= \underline{\underline{31.06 \text{ k}\Omega}}$$

$$S = \frac{1 + \beta}{1 + \left(\frac{\beta \cdot R_E}{R_E + R_T} \right)} = \frac{1 + 100}{1 + \left(\frac{100 \times 2.722 \times 10^3}{(2.722 \times 10^3) + (31.06 \times 10^3)} \right)}$$

$$= \underline{\underline{11.15}} .$$

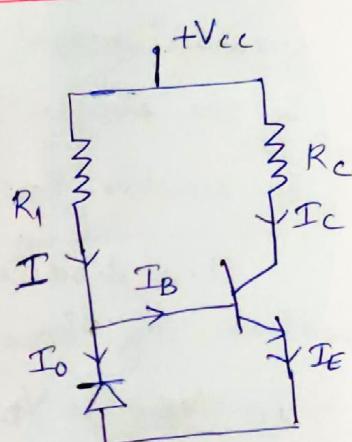
Bias Compensation

Usually diodes, thermistors & transistors are temperature sensitive devices & can be used to compensate the change in collector current (I_c) & the Q-point (operating point) will be stabilised. This method is called bias compensation.

① Diode Compensationa) Diode Compensation for variations in I_{C0}

Diode used in the circuit is reverse biased. So the current through the diode is reverse leakage current (I_o)

The diode is of the same type & material as that of the transistor. So the reverse saturation current of transistor (I_{C0}) & I_o will increase at the same rate with increase in temperature.



$$\text{From ckt: } I = I_B + I_o$$

$$I_B = I - I_o \quad \text{--- (1)}$$

When temp increases, $I_o \uparrow$ & $I_c \uparrow$.

$$\text{As } I_{C0} \uparrow \Rightarrow I_c \uparrow$$

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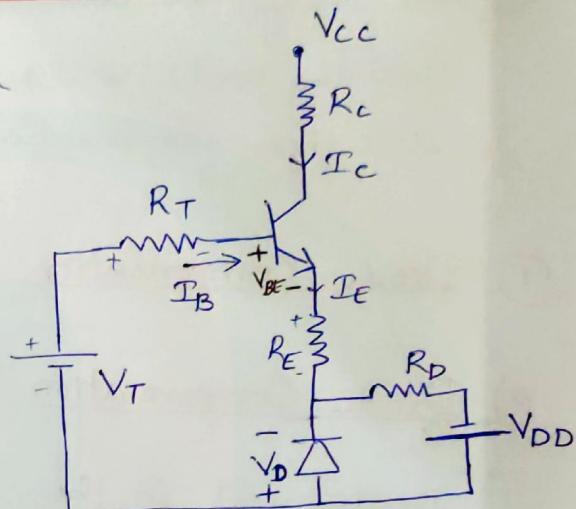
But as $I_o \uparrow$, from eq (1) $I_B \downarrow$

So increase in I_c due to I_{co} can be controlled using diode.

b) Diode Compensation for variation in V_{BE}

Circuit is voltage divider bias circuit (Thermin's equivalent) using diode compensation.

Diode is kept forward biased by the source V_{DD} & resistor R_D .



The diode is of the same type & material as that of the transistor. So the variations in V_{BE} & V_D are same due to temperature rise.

Apply KVL in i/p loop.

$$-V_T + I_B R_T + V_{BE} + I_E R_E - V_D = 0.$$

$$I_E \approx I_c$$

$$I_B = \frac{I_c}{\beta}$$

$$-V_T + \frac{I_c}{\beta} R_T + V_{BE} + I_c R_E - V_D = 0$$

$$\therefore I_c \left[\frac{R_T}{\beta} + R_E \right] = V_T - V_{BE} + V_D$$

$$I_c = \frac{V_T - V_{BE} + V_D}{\left(\frac{R_T}{\beta} + R_E \right)} \quad \text{--- (1)}$$

When temp \uparrow , V_{BE} & V_D varies in the same way. So from eq ①, change in I_c due to V_{BE} gets cancelled.

$$\Delta(V_D - V_{BE}) = 0$$

② Theemistor Compensation

This is a voltage divider bias CE amplifier using theemistor compensation.

Theemistor R_T has a -ve temperature coefficient

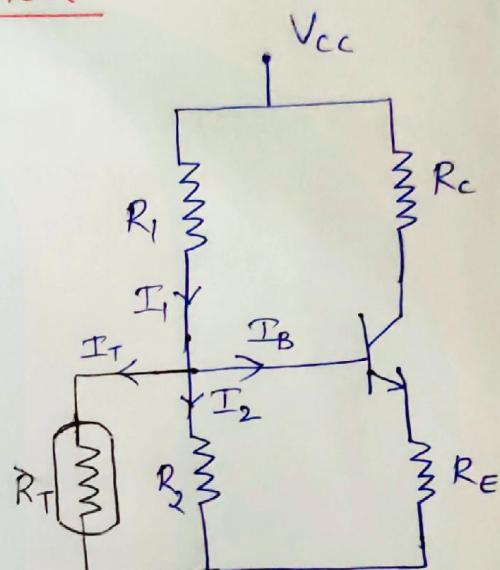
of resistance. i.e Resistance decreases with increase in temperature.

When temp \uparrow , $I_{C\text{tot}} \approx I_{C\text{t}}$

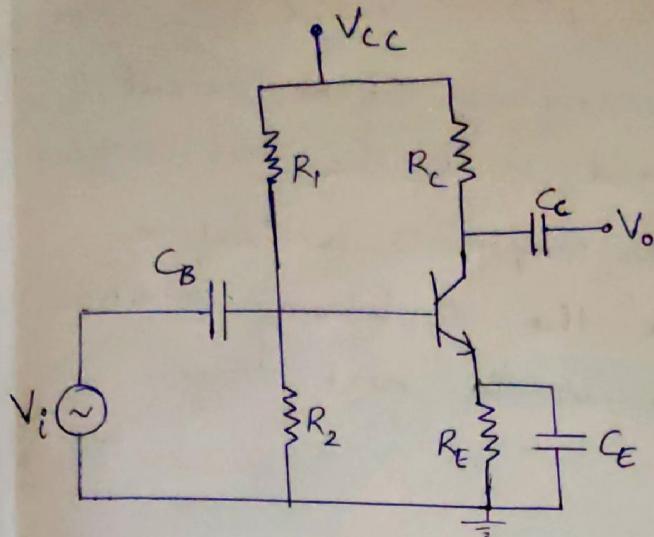
When temperature increases, voltage drop across R_T decreases, $\therefore V_{BE}$ (forward bias voltage) decreases.

As a result I_B (base current) will decrease and $\therefore I_c$ (collector current) will decrease.

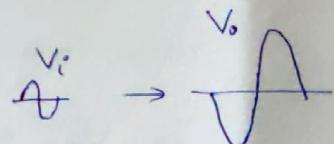
\therefore The theemistor R_T will minimise the increase in collector current.



Ktu Q bank RC Coupled Common Emitter Amplifier



- This is a single stage RC coupled CE amplifier. Transistor is connected in CE configuration.
- Voltage divider biasing is used. R_1, R_2 & R_E are used for properly biasing the transistor.
- For CE amplifier, o/p voltage is 180° shifted & amplified version of i/p signal.



- Role of Different Capacitors used:

(i) Input Coupling Capacitor (C_B)

C_B is used for coupling ac i/p voltage (V_i) to the base of transistor. C_B blocks any dc components present in V_i & allows only ac component. This ensures that dc biasing condition of transistor will remain unchanged.

(ii) Output Coupling Capacitor (C_c):

C_c is used for coupling the ac output voltage to the load or to the next stage.

C_c will block dc components & therefore it won't affect the dc biasing condition of the transistor in the next stage.

(iii) Emitter bypass Capacitor (C_E):

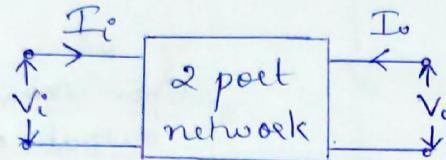
C_E is connected in parallel with R_E (emitter resistance). So it will provide a low reactance path to the amplified ac signal. If C_E is not present, then the amplified ac signal flowing through R_E will cause a voltage drop in R_E to increase.

So V_{BE} will decrease, $\therefore I_B \downarrow$ & $I_C \downarrow$.

So o/p voltage will reduce.

Hybrid Parameters

All the transistor amplifiers are 2 port network having 2 voltages & 2 currents



$V_i \rightarrow$ input voltage $I_i \rightarrow$ " current	$V_o \rightarrow$ output voltage $I_o \rightarrow$ " current
--	---

In hybrid ($\text{or } h$) parameter equivalent circuit:

I_i & V_o are taken as independent variables.

V_i & I_o " " " dependent " .

$$V_i = h_{11} I_i + h_{12} V_o \quad \text{--- (1)}$$

$$I_o = h_{21} I_i + h_{22} V_o \quad \text{--- (2)}$$

Meaning of h parameters.

- 1) If output terminals are short circuited, i.e. $V_o = 0$, then
 (from eq (2))

$$h_{11} = \frac{V_i}{I_i} \Big|_{V_o=0}$$



Short circuited
input impedance.
 (Unit - ohm (Ω))

$$h_{21} = \frac{I_o}{I_i} \Big|_{V_o=0}$$



Forward transfer
current ratio.

Ktu Q bank
 If input terminals are open circuited then $I_i = 0$, then
 (from eq ②)

$$h_{12} = \left. \frac{V_i}{V_o} \right|_{I_i=0}$$



Reverse transfer

Voltage ratio

(Unit less)

$$h_{22} = \left. \frac{I_o}{V_o} \right|_{I_i=0}$$



Open circuited output admittance
 (Unit - mho (ω))

Notations

$i = 11 \rightarrow$ input

$o = 22 \rightarrow$ output

$f = 21 \Rightarrow$ forward transfer

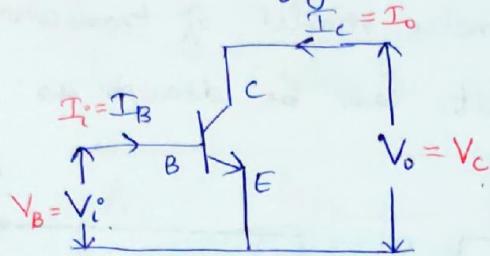
$r = 12 \Rightarrow$ Reverse "

<u>h parameter</u>	<u>CE configuration</u>
$h_{11} (h_i)$	h_{ie}
$h_{12} (h_x)$	h_{ce}
$h_{21} (h_f)$	h_{fe}
$h_{22} (h_o)$	h_{oe}

The units of all h -parameters are different
 i.e why they are called hybrid parameters.

Hybrid Model of BJT in CE Configuration.

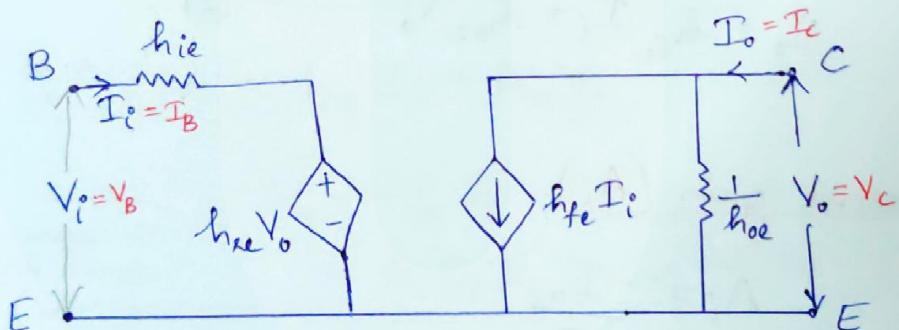
BJT in CE configuration is:



$$V_i = h_{ie} I_i + h_{re} V_o$$

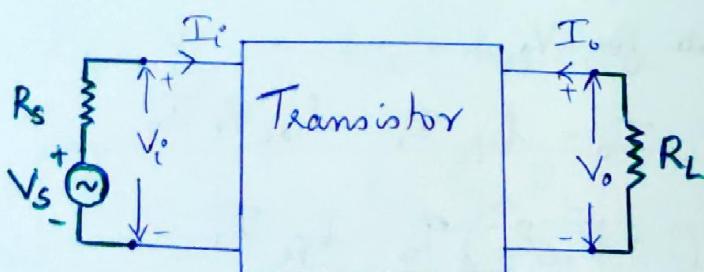
$$I_o = h_{fe} I_i + h_{re} V_o$$

By applying KVL & KCL in reverse, the hybrid model of BJT is shown below:



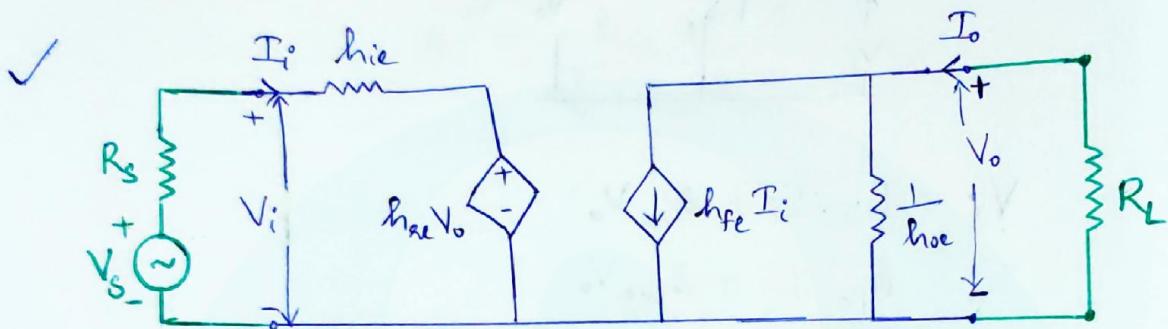
Amplifier gain & impedance calculations

of transistor using h-parameter



$V_s \rightarrow$ source voltage
 $R_s \rightarrow$ " resistance .

Using h-parameter model of transistor the equivalent circuit can be drawn as:



$$V_i = h_{ie} I_i + h_{re} V_o \quad \text{--- (1)}$$

$$I_o = h_{fe} I_i + h_{oe} V_o \quad \text{--- (2)}$$

① Current gain (A_i)

$$A_i = -\frac{I_o}{I_i}$$

(o/p current is opposite direction
 $\therefore -I_o$)

$$\text{eq (2)} \quad I_o = h_{fe} I_i + h_{oe} V_o$$

$$\text{But } V_o = -I_o R_L \quad (\text{from o/p diag.})$$

Substitute for V_o .

$$I_o = h_{fe} I_i - h_{oe} R_L I_o$$

$$(1 + h_{oe} R_L) I_o = h_{fe} I_i$$

$$\frac{I_o}{I_i} = \frac{h_{fe}}{(1+h_{oe}R_L)}$$

$$A_i^o = -\frac{I_o}{I_i} = \frac{-h_{fe}}{1+h_{oe}R_L}$$

** *by heat*

Current gain

$$A_i = -\frac{h_{fe}}{(1+h_{oe}R_L)}$$

— ③

② Input Impedance (Z_i)

$$Z_i = \frac{V_i}{I_i}$$

$$\text{eq } ① \quad V_i = h_{ie} I_i + h_{re} V_o$$

$$V_o = -\underline{I_o} R_L$$

$$= A_i I_i R_L$$

But $A_i = -\frac{I_o}{I_i}$
 $\therefore -I_o = A_i I_i$

Substitute for V_o .

$$\begin{aligned} V_i &= h_{ie} I_i + h_{re} A_i R_L I_i \\ &= I_i [h_{ie} + h_{re} A_i R_L] \end{aligned}$$

$$Z_i = \frac{V_i}{I_i} = h_{ie} + h_{re} A_i R_L$$

Input impedance

$$Z_i = h_{ie} - \frac{h_{fe} h_{re} R_L}{(1+h_{oe}R_L)}$$

From eq ③
 $A_i = \frac{-h_{fe}}{(1+h_{oe}R_L)}$

— ④

Voltage Gain (A_v)

$$A_v = \frac{V_o}{V_i}$$

$$\text{eq } ① \quad V_i = h_{ie} I_i + h_{oe} V_o \quad \text{--- } ⑤$$

$$\text{We know } A_i = -\frac{I_o}{I_i} = \frac{-h_{fe}}{(1+h_{oe}R_L)}$$

$$\therefore I_i = I_o \times \frac{(1+h_{oe}R_L)}{h_{fe}} \quad ⑥$$

$$V_o = -I_o R_L$$

$$\therefore I_o = -\frac{V_o}{R_L} \quad ⑦$$

Substitute eq ⑦ in eq ⑥

$$I_i = -\frac{V_o}{R_L} \frac{(1+h_{oe}R_L)}{h_{fe}}$$

Substitute this in eq ⑤

$$V_i = h_{ie} \times -\frac{(1+h_{oe}R_L)}{R_L \cdot h_{fe}} V_o + h_{oe} V_o$$

$$V_i = V_o \left[\frac{-h_{ie} - h_{ie}h_{oe}R_L + h_{oe}h_{fe}R_L}{h_{fe} R_L} \right]$$

$$\frac{V_o}{V_i} = \frac{h_{fe} R_L}{-h_{ie} - R_L(h_{ie} - h_{oe})}$$

$$A_v = \frac{V_o}{V_i}$$

$$\therefore A_v = \frac{-h_{fe} R_L}{h_{ie} + R_L (h_{ie} h_{oe} - h_{re} h_{fe})}$$

** by heart

or

$$A_v = A_i \times \frac{R_L}{Z_i}$$

④ Output Impedance (Z_o)

$$Z_o = \left. \frac{V_o}{I_o} \right|_{V_s=0}$$

For the input circuit, applying KVL.

$$-V_s + I_i R_s + I_i h_{ie} + h_{re} V_o = 0$$



When $V_s = 0$

$$I_i R_s + I_i h_{ie} + h_{re} V_o = 0$$

$$I_i (R_s + h_{ie}) = -h_{re} V_o$$

$$I_i = \frac{-h_{re} V_o}{(R_s + h_{ie})}$$

$$\text{② } I_o = h_{fe} \underline{I_i} + h_{oe} V_o$$

Substitute the above equation.

$$I_o = h_{fe} \times \frac{-h_{re} V_o}{(R_s + h_{ie})} + h_{oe} V_o$$

$$I_o = V_o \left[\frac{-h_{fe} h_{re}}{R_s + h_{ie}} + h_{oe} \right]$$

$$Z_o = \frac{V_o}{I_o}$$

$$\therefore Z_o = \frac{V_o}{I_o} = \frac{1}{\frac{-h_{fe} h_{re}}{R_s + h_{ie}} + h_{oe}}$$

✓

$$Z_o = \frac{1}{h_{oe} - \frac{h_{fe} h_{re}}{(R_s + h_{ie})}}$$

- Q. h-parameters of a transistor connected in CE configuration is $h_{ie} = 1000 \Omega$, $h_{re} = 10 \times 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 100 \times 10^6 \Omega$. If the load resistance R_L is $1k\Omega$, find (i) The input impedance (ii) Current gain (iii) Voltage gain. [5].

Ans. $h_{ie} = 1000 \Omega$, $h_{re} = 10^{-3}$
 $h_{fe} = 50$, $h_{oe} = 10^{-4} \Omega$

$$R_L = 1k\Omega$$

(i) ifp impedance, $Z_i = h_{ie} - \frac{h_{fe} \cdot h_{re} R_L}{(1 + h_{oe} R_L)}$
 $= 1000 - \frac{(50 \times 10^{-3} \times 10^3)}{(1 + (10^{-4} \times 10^3))}$

$$= \underline{954.54} \Omega$$

(ii) Current gain, $A_i = \frac{-h_{fe}}{(1+h_{oe}R_L)}$

$$= \frac{-50}{(1 + 10^{-4} \times 10^3)} = \underline{\underline{-45.45}}$$

(iii) Voltage gain, $A_v = A_i \times \frac{R_L}{Z_i}$

$$= -45.45 \times \frac{10^3}{954.54}$$

$$= \underline{\underline{-47.61}}$$