EET303

Microprocessors and microcontrollers

COURSE OUTCOMES

CO 1 Describe the architecture and timing diagram of 8085 microprocessor.

CO 2 Develop assembly language programs in 8085 microprocessor.

CO 3 Identify the different ways of interfacing memory and I/O with 8085 microprocessor.

CO 4 Understand the architecture of 8051 microcontroller and embedded systems.

CO 5 Develop assembly level and embedded C programs in 8051 microcontroller

SYLLABUS

Module 1

Internal architecture of 8085 microprocessor–Functional block diagram Instruction set-Addressing modes - Classification of instructions - Status flags. Machine cycles and T states – Fetch and execute cycles- Timing diagram for instruction and data flow.

Module 2

Introduction to assembly language programming- Data transfer operations, arithmetic operations, logic operations, branching operations, I/O and machine control operations. Assembly language programmes (ALP) in 8085 microprocessor- Data handling/Data transfer, Arithmetic operations, Code conversion- BCD to Binary - Binary to BCD, Sorting - Ascending and descending including bubble sorting. Stack and subroutines – Conditional CALL and Return instructions Time delay subroutines using 8 bit register, 16 bit register pair and Nested loop control.

Module 3

Interrupt & interrupt handling - Hardware and Software interrupts. I/O and memory interfacing – Address decoding– Interfacing I/O ports -Programmable Peripheral Interface PPI 8255 - Modes of operation- Interfacing of seven segment LED. Introduction to embedded systems, Current trends and challenges, Applications of **embedded systems**- Hard and soft real time systems. Introduction to microcontrollers- Microprocessor Vs Microcontroller- **8051 Microcontrollers** – Hardware - Microcontroller architecture and programming model - I/O port structure - Register organization -General purpose RAM - Bit addressable RAM - Special Function Registers (SFRs).

Module 4

Instruction set - Instruction types - Addressing modes of 8051 microcontrollers. 8051 microcontroller data types and directives - Time delay programmes and I/O port programming. Introduction to embedded C Programming - time delay in C - I/O port programming in embedded C.

Module 5

8051 Timer/counter programming - Serial port programming - Interrupt programming in assembly language and embedded C. Interfacing –ADC - DAC and temperature sensor

Text Books

1. Ramesh Gaonkar, “Microprocessor Architecture Programming and Applications”, Penram International Publishing; Sixth edition, 2014.
2. Mohamed Ali Mazidi, Janice GillispieMazidi, “The 8051 microcontroller and embedded systems using Assembly and C”, second edition, Pearson/Prentice hall of India.
3. Kenneth J. Ayala, “The 8051 microcontroller”, 3rd edition, Cengage Learning, 2010
4. Lyla B Das, “Embedded Systems - An Integrated Approach”, Pearson Education India

Reference Books

1. B Ram, “Fundamentals of Microprocessors and Microcontrollers”, 9e, DhanpatRai Publications, 2019.
2. Wadhwa, “Microprocessor 8085 microprocessor: Architecture, Programming and Interfacing”, PHI 2010

MICROPROCESSOR

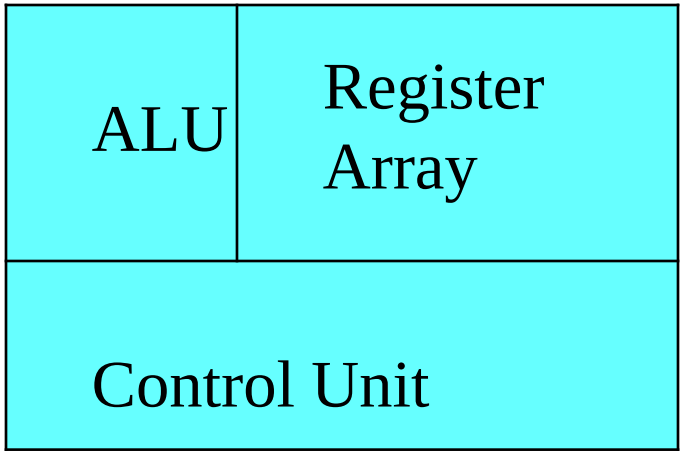
What is a microprocessor?

A Programmable integrated device in a single chip which includes ALU, registers (as a small internal memory) & a control unit.

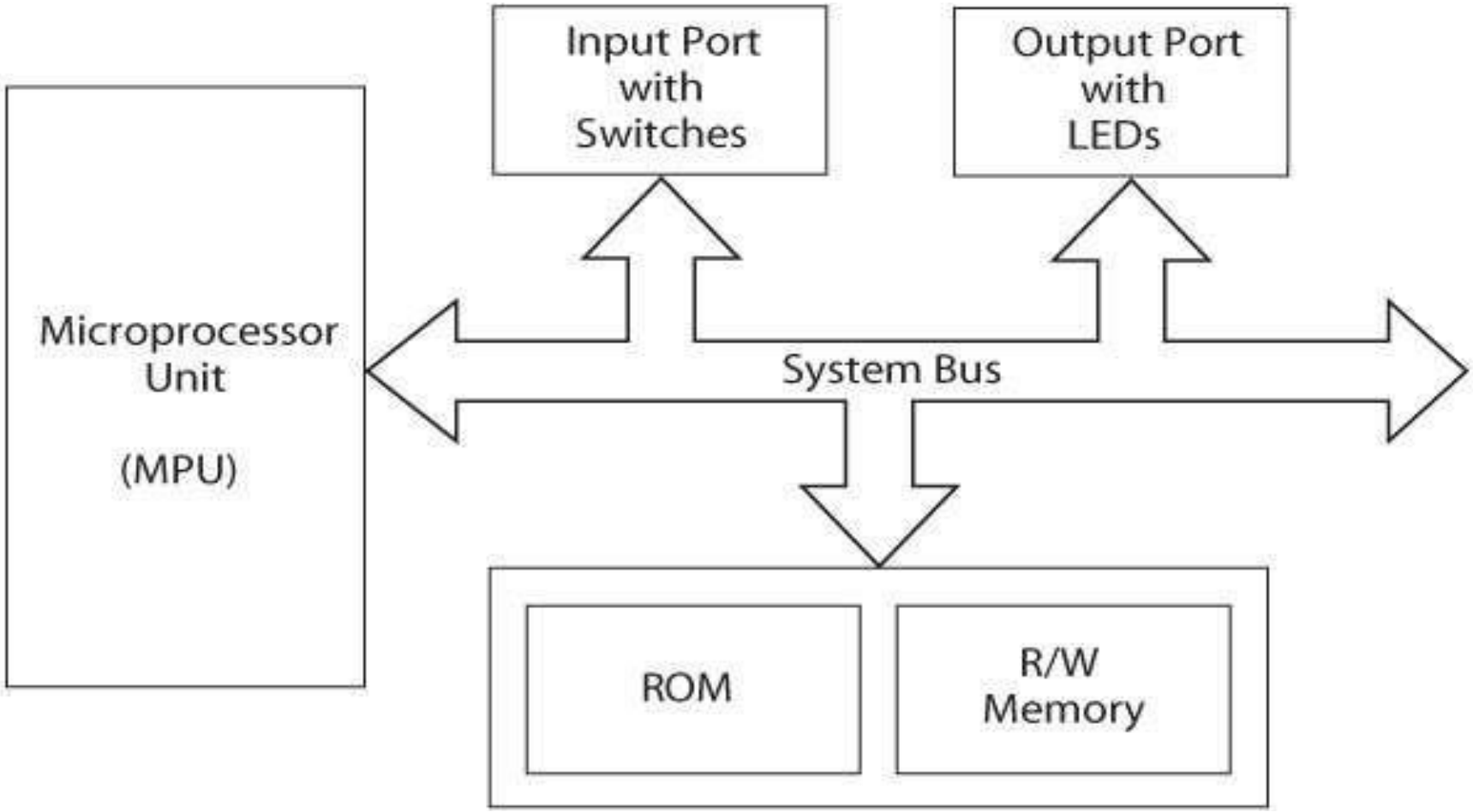
- ✓ A general purpose device (i.e. may be used for different purposes in different applications e.g. as a CPU in a microcomputer)
- ✓ Uses Memory, I/O functions etc. external to the chip
- ✓ Configuration of the system is flexible

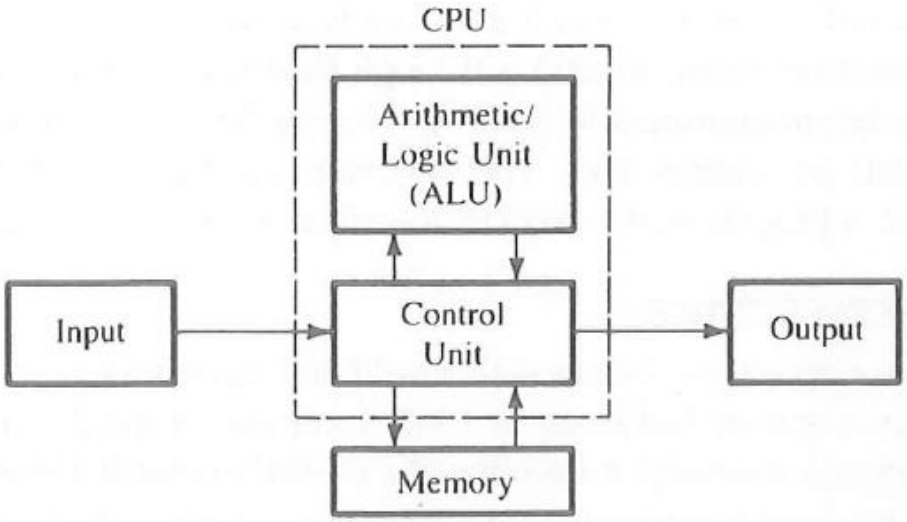
What is inside microprocessor ?

- Internally, the microprocessor is made up of 3 main units.
  - The Arithmetic/Logic Unit (ALU)
  - The Control Unit.
  - An array of Registers as a small internal memory for holding data while it is being manipulated or processed.

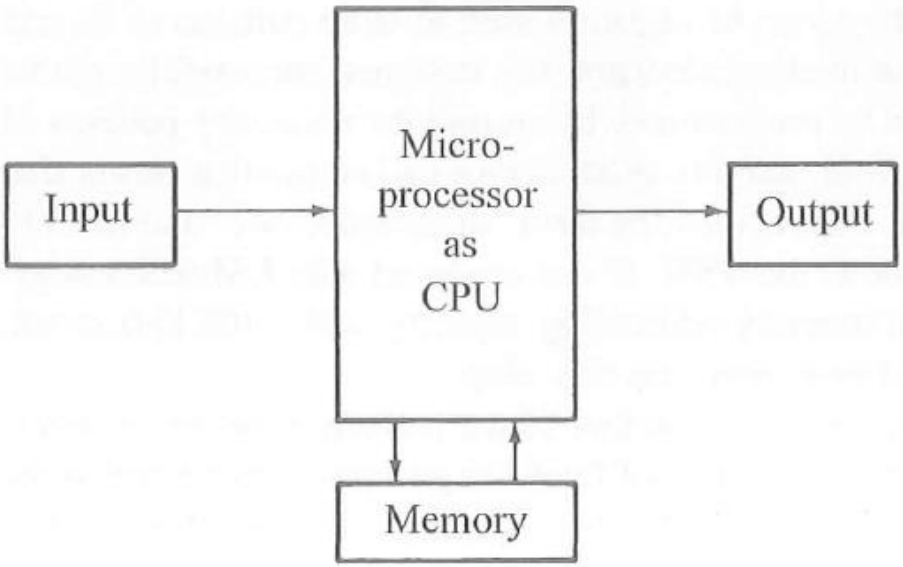


A microprocessor-based system




CPU
Arithmetic/
Logic Unit
(ALU)
Input
Control
Unit
Output
Memory

(a)


Input
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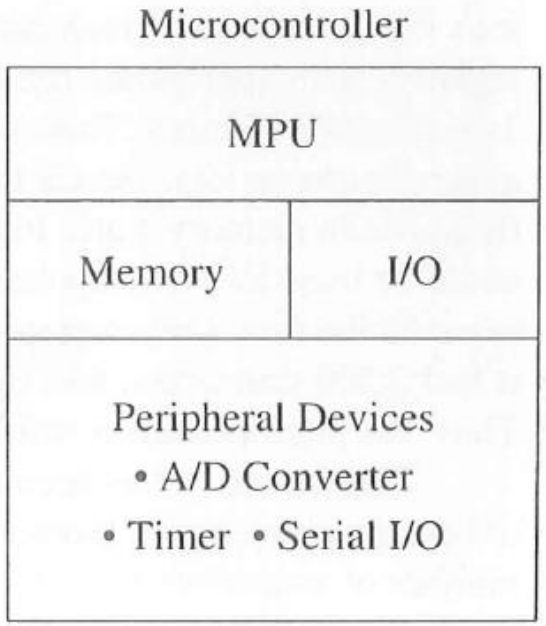
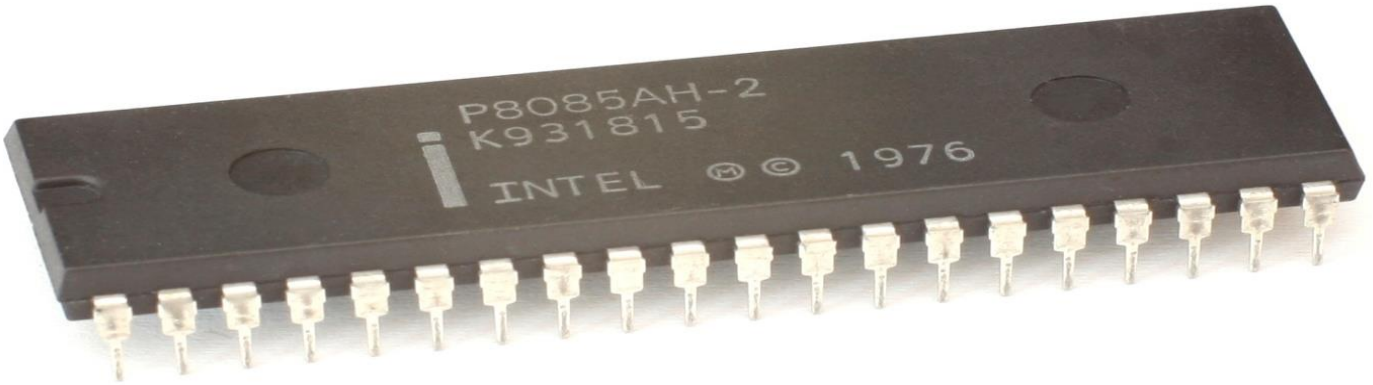
CPU
Output
Memory

(b)


Microcontroller
MPU
Memory
I/O
Peripheral Devices
• A/D Converter
• Timer • Serial I/O

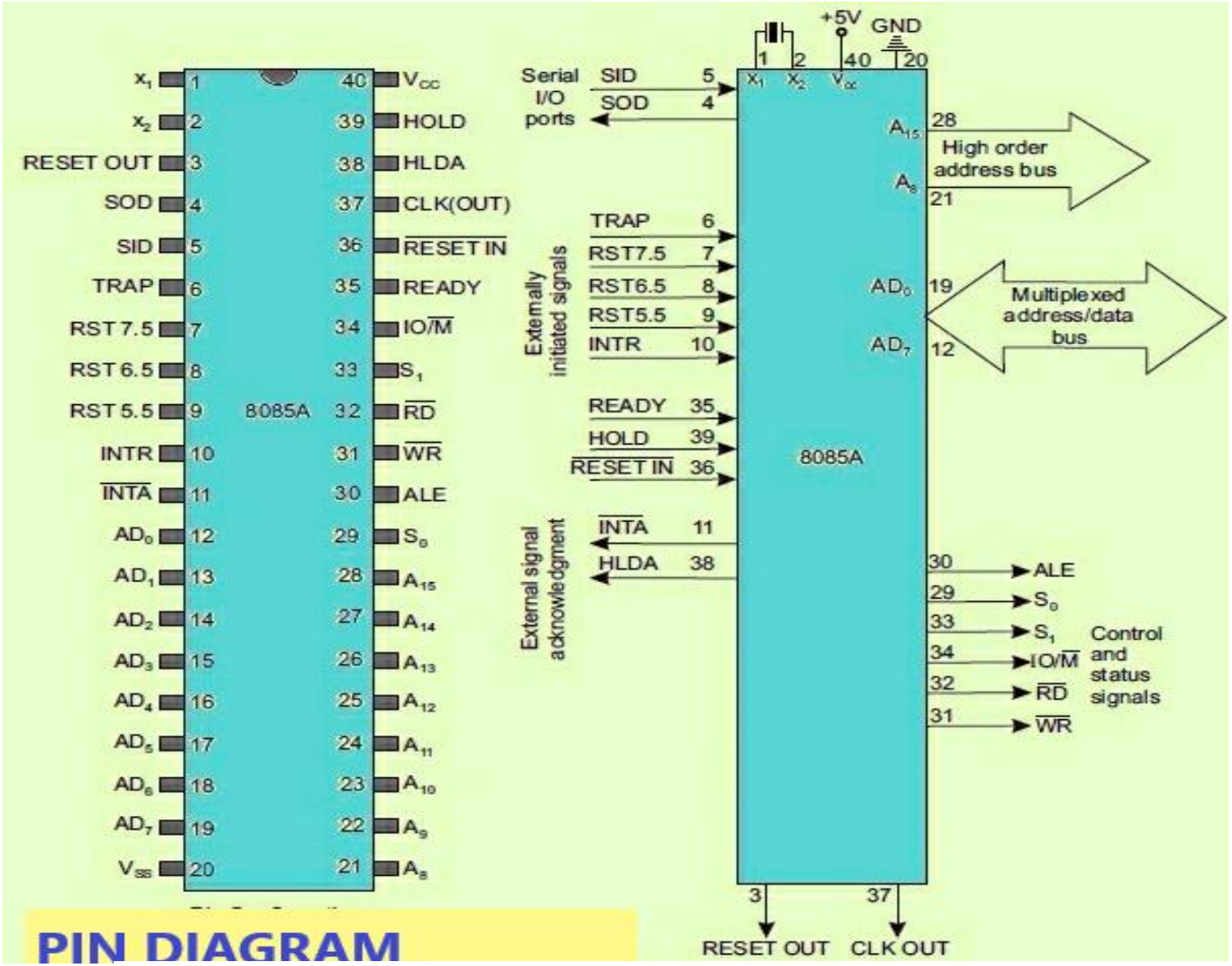
(c)

8085 MICROPROCESSOR

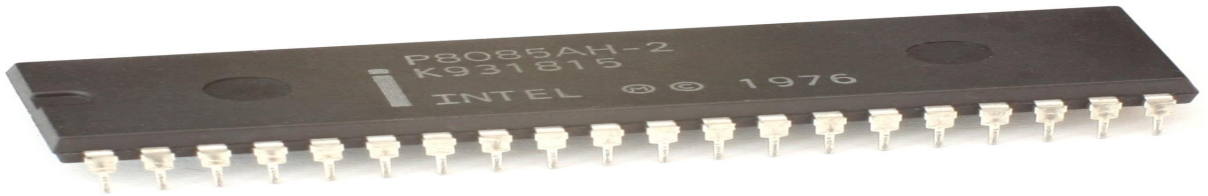


Introduction to 8085 microprocessor

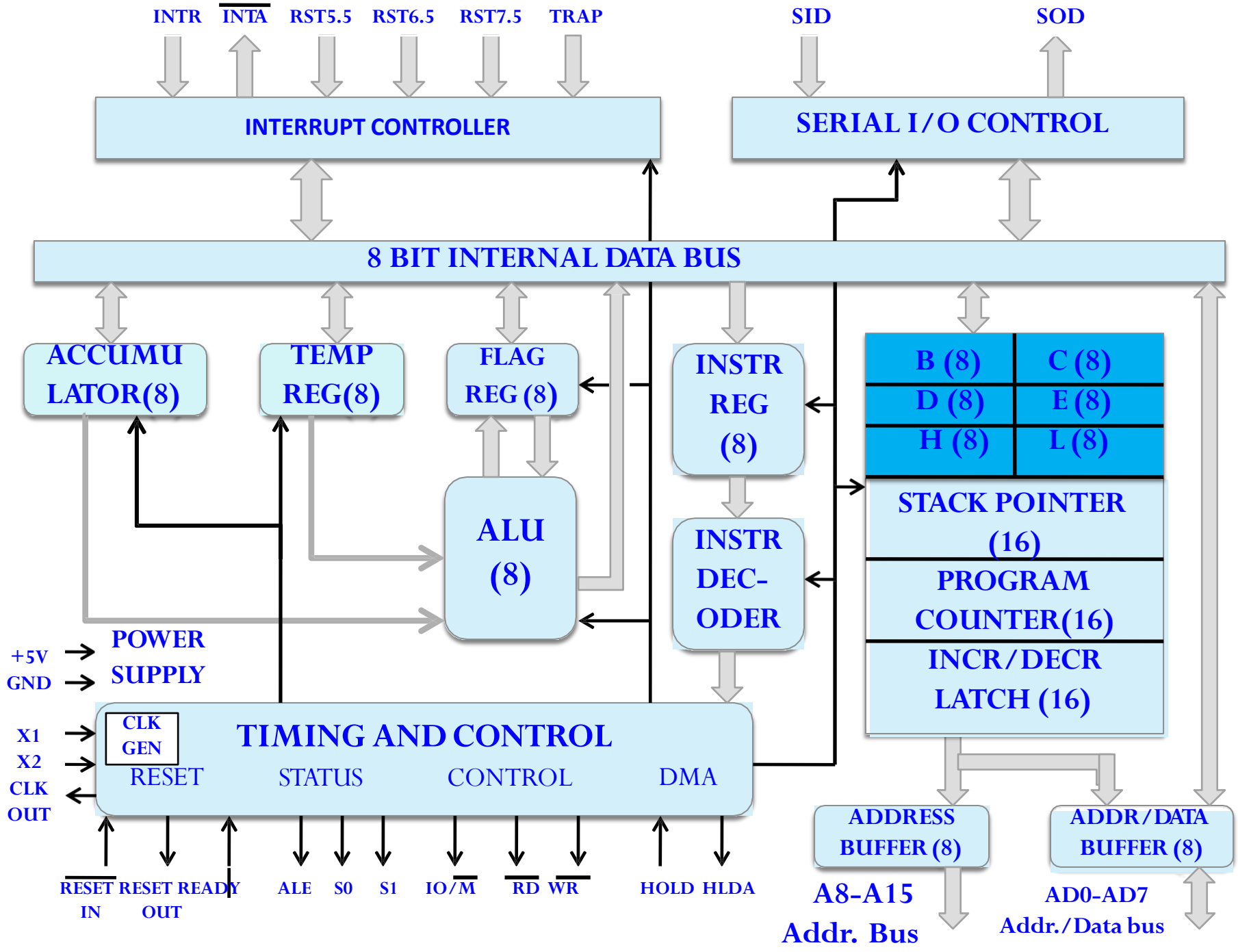
- Introduced in 1976
- It is an 8-bit Microprocessor
- It is a 40 pin IC package
- It has about 6500 transistors
- It uses a single +5V supply for its operations
- Clock speed – 3 to 6 MHz


8085A
x_1 1
x_2 2
RESET OUT 3
SOD 4
SID 5
TRAP 6
RST 7.5 7
RST 6.5 8
RST 5.5 9
INTR 10
$\overline{INTA}$ 11
AD_0 12
AD_1 13
AD_2 14
AD_3 15
AD_4 16
AD_5 17
AD_6 18
AD_7 19
V_{SS} 20
40 V_{CC}
39 HOLD
38 HLDA
37 CLK(OUT)
36 $\overline{RESET\ IN}$
35 READY
34 IO/$\overline{M}$
33 S_1
32 $\overline{RD}$
31 $\overline{WR}$
30 ALE
29 S_0
28 A_{15}
27 A_{14}
26 A_{13}
25 A_{12}
24 A_{11}
23 A_{10}
22 A_9
21 A_8
+5V
GND
1 2 40 20
x_1 x_2 V_{cc}
Serial I/O ports
SID 5
SOD 4
TRAP 6
RST7.5 7
RST6.5 8
RST5.5 9
INTR 10
Externally initiated signals
READY 35
HOLD 39
$\overline{RESET\ IN}$ 36
$\overline{INTA}$ 11
HLDA 38
External signal acknowledgment
A_{15} 28
A_8 21
High order address bus
AD_0 19
AD_7 12
Multiplexed address/data bus
30 ALE
29 S_0
33 S_1
34 IO/$\overline{M}$
32 $\overline{RD}$
31 $\overline{WR}$
Control and status signals
3 RESET OUT
37 CLK OUT

PIN DIAGRAM


P8085AH-2
K931815
INTEL © 1976

ARCHITECTURE OF 8085 MICROPROCESSOR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RST6.5
RST7.5
TRAP
SID
SOD
INTERRUPT CONTROLLER
SERIAL I/O CONTROL
8 BIT INTERNAL DATA BUS
ACCUMU LATOR(8)
TEMP REG(8)
FLAG REG (8)
INSTR REG (8)
B (8)
C (8)
D (8)
E (8)
H (8)
L (8)
ALU (8)
INSTR DEC- ODER
STACK POINTER (16)
PROGRAM COUNTER(16)
INCR/DECR LATCH (16)
+5V
GND
POWER SUPPLY
X1
X2
CLK OUT
CLK GEN
TIMING AND CONTROL
RESET
STATUS
CONTROL
DMA
ADDRESS BUFFER (8)
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RESET IN
RESET OUT
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ALE
S0
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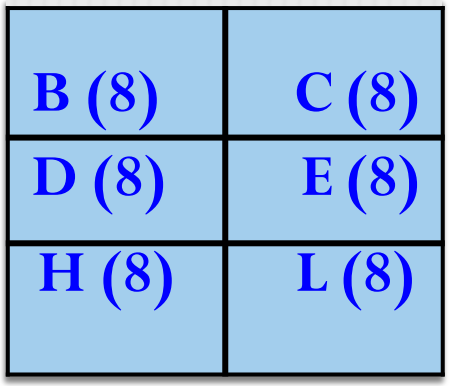
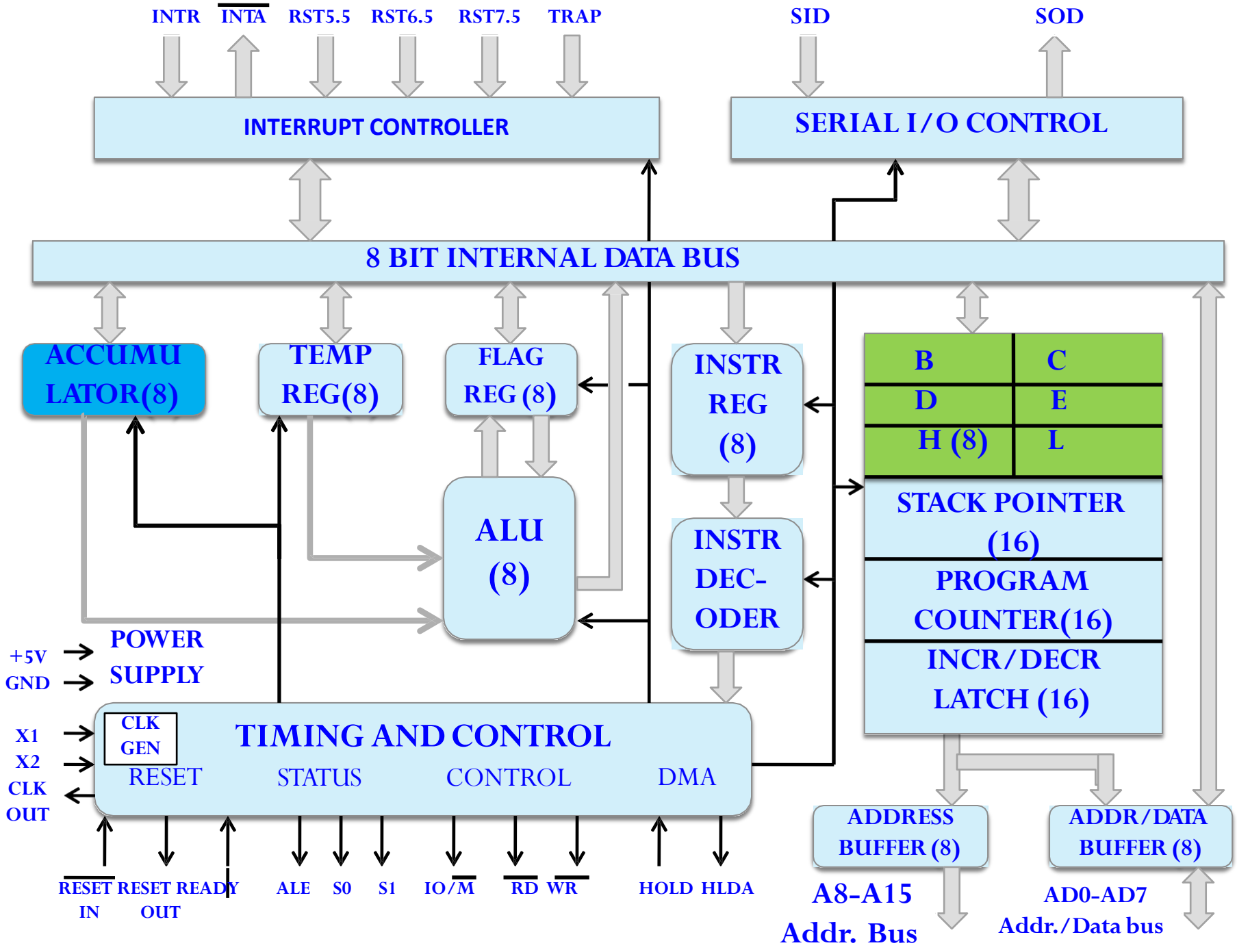
IO/M
RD
WR
HOLD
HLDA
A8-A15
Addr. Bus
AD0-AD7
Addr./Data bus

General purpose registers



- In 8085 general purpose registers are used to hold data like any other registers
- In 8085 there are six general purpose registers
- They are B, C, D, E, H and L
- Each register can hold 8 bit data
- They can work in pairs such as B-C, D-E, H- L to store 16 bit data
- The H-L pair work as a memory pointer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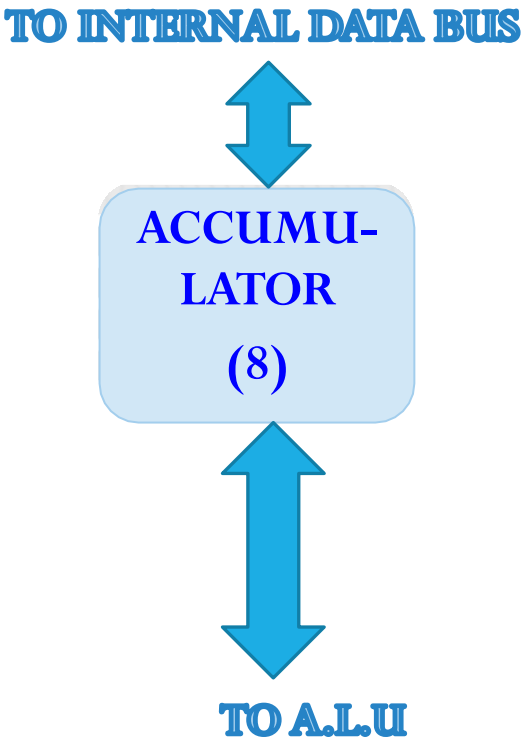
A8-A15
Addr. Bus
AD0-AD7
Addr./Data bus

Accumulator

- It is one of the most important 8 bit register of 8085
- It is connected to internal data bus and ALU
- The primary purpose of accumulator is to store temporary data and for the placement of final values of arithmetic and logical operations
- This accumulator register is mainly used for arithmetic, logical and store & rotate operations



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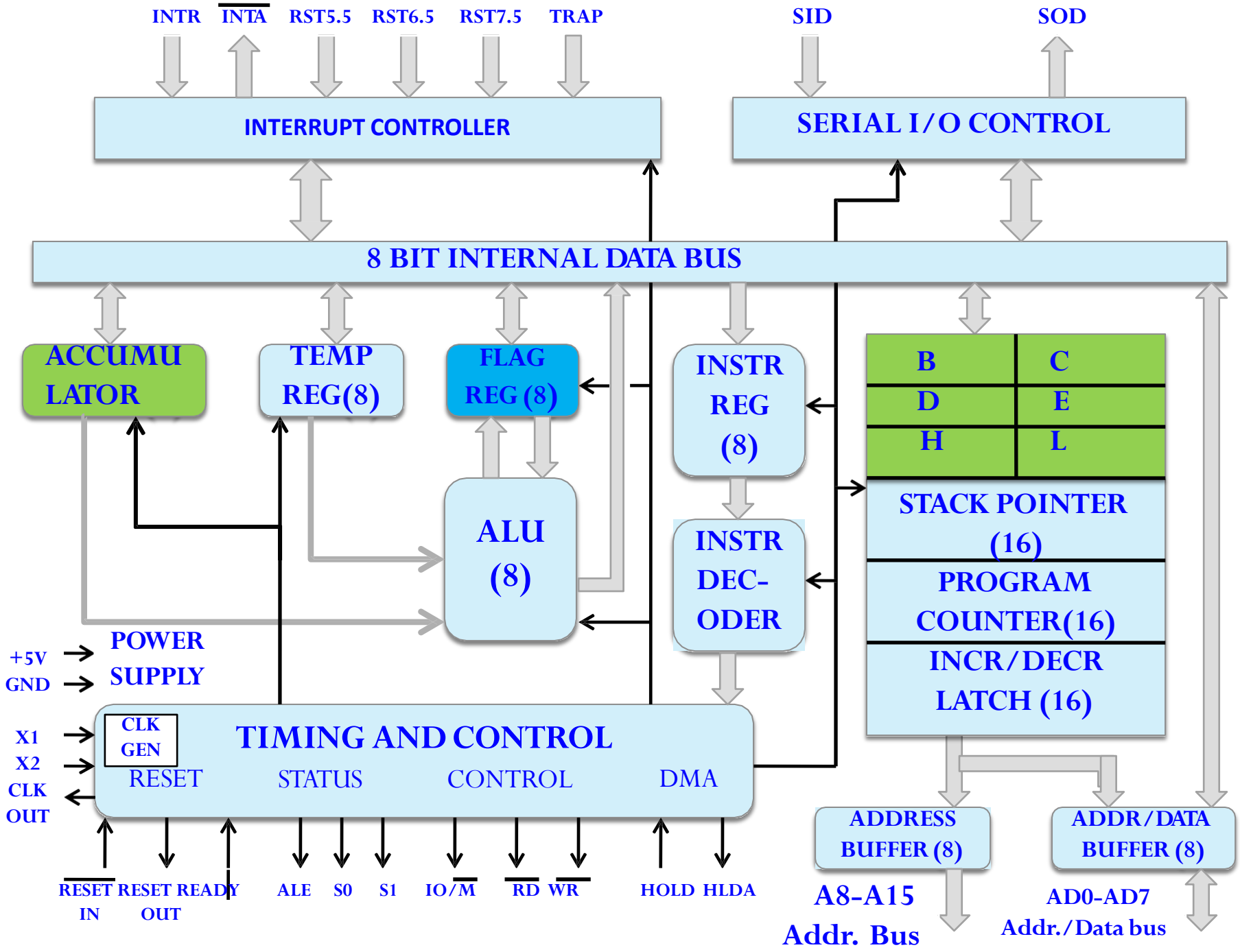
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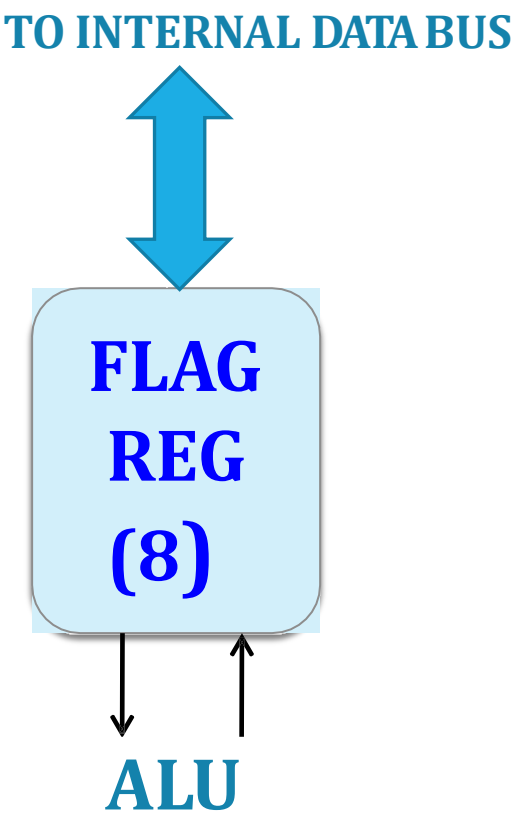
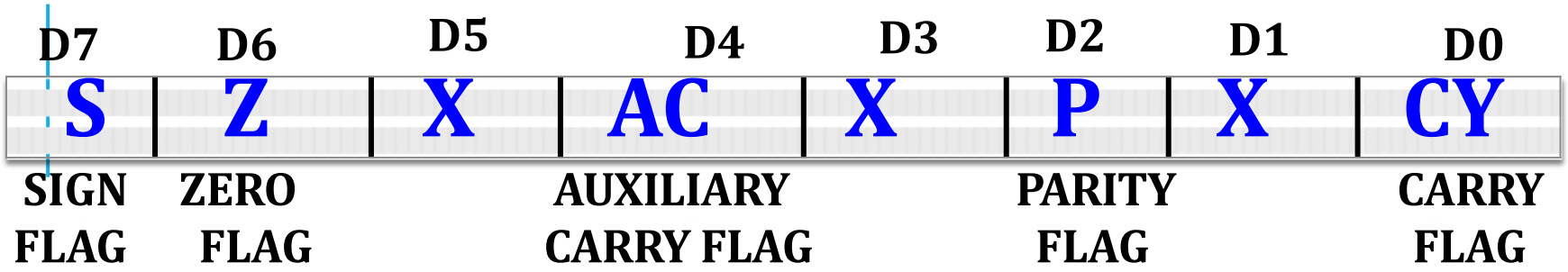
Flag register

- Flag register is a group of flip flops used to give status of result of different operations
- Once an operation is performed by ALU the result is transferred on internal data bus and status of result will be stored in flip flops
- The flag register in 8085 is an 8-bit register which contains 5 bit positions
- These five flags are of 1bit F/F and are known as zero, sign, carry, parity and auxiliary carry
- These are set or reset after an operation according to data conditions of the result in the accumulator and other registers



8085 flag register



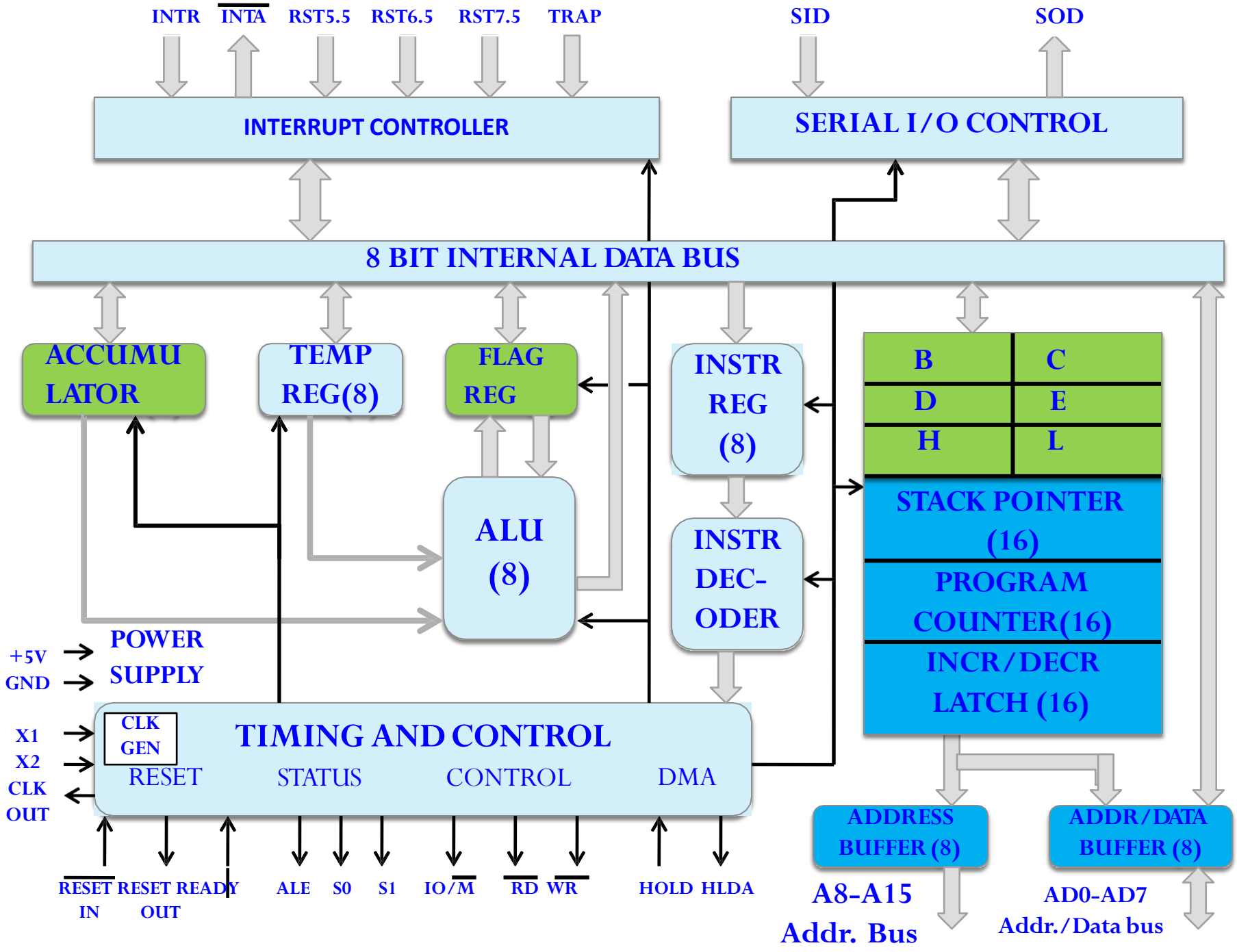
- **CY -** The carry flag is used for carrying and borrowing in case of addition and subtraction operations, it is set when carry is generated and otherwise it is reset
- **P -** The parity flag is used for results containing an even number of one's, it is set for even parity and is reset for odd parity
- **AC -** In an arithmetic operation, when a carry is generated by digit D3 and passed on to digit D4, the AC flag is set. The auxiliary carry flag is used for BCD operations
- **Z -** The zero flag is set if the result of an instruction is zero and otherwise it is reset
- **S –** Signed number is –ve if S = 1 and +ve if S = 0

Use of all flags

```
MVI A, F2H
MVI B, 7AH
ADD B
HLT
```

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	0	1	0
0	1	1	1	1	0	1	0
1	0	1	1	0	1	1	0	0

- **CY=1** - D7 bit of the result generate carry (bit number nine is1), so the Carry flag is set
- **S=0** - Result of arithmetic operation is positive so the sign bit is zero
- **P=1** - The result has an even number of 1s,so the Parity flag is set
- **AC=0** -The carry is not generated by digit D3, so the auxiliary flag is reset
- **Z=0** - The ALU operation result is not 0. So the zero flag is reset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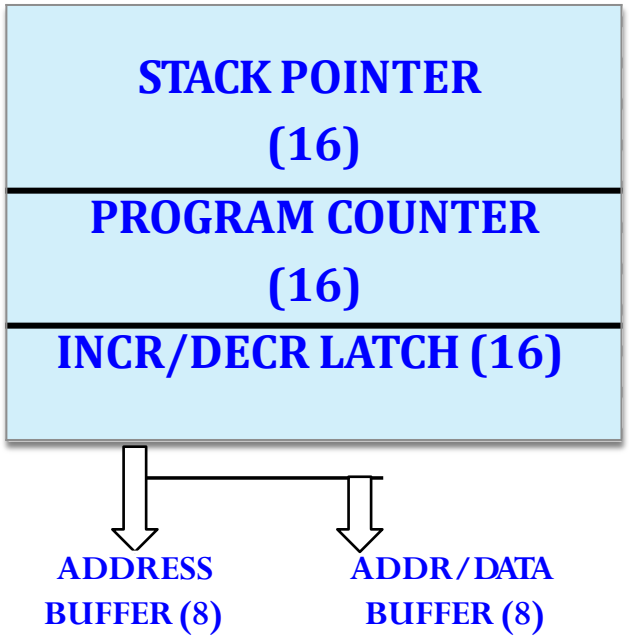
Special purpose registers

- It consists of three 16 bit registers- Program Counter , Stack pointer, Incrementer / Decrementer Latch



SPECIAL PURPOSE REGISTER

Program Counter –

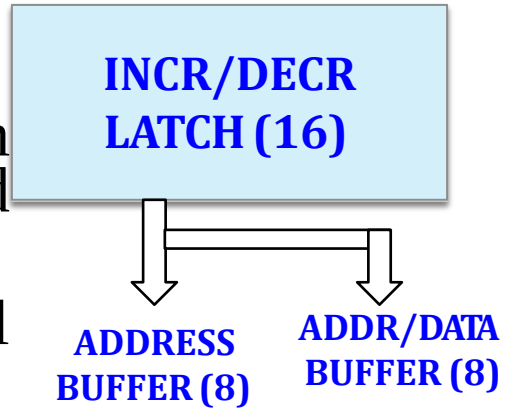
Program counter is a special purpose register. It holds the address of the next instruction to be executed, in order to save time

Stack Pointer -

- A stack is nothing but the portion of RAM
- It works on the LIFO concept
- Stack pointer maintains the address of the last byte that is entered into stack
- Each time when the data is loaded into stack, Stack pointer gets decremented

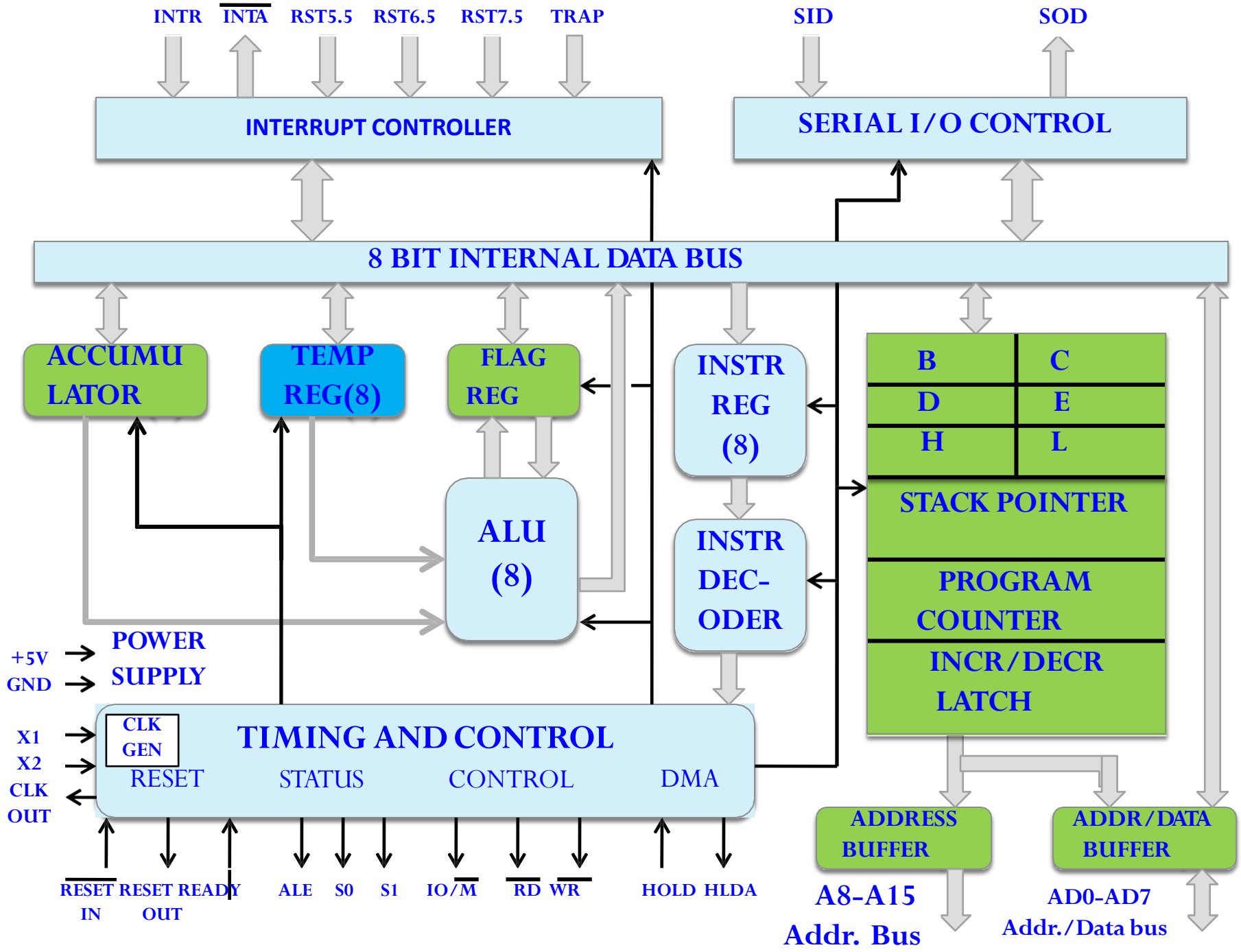
➢ INCR/DECR LATCH :-

It is used to increment or decrement the content of program counter and stack pointer register



➢ Address /data buffer and address buffer:-

- The contents of the stack pointer and program counter are loaded into the address buffer and address-data buffer
- These buffers are then used to drive the external address bus and address-data bus.
- As the memory and I/O chips are connected to these buses, the CPU can exchange desired data to the memory and I/O chips
- The address-data buffer is not only connected to the external data bus but also to the internal data bus which consists of 8-bits
- The address data buffer can both send and receive data from internal data bus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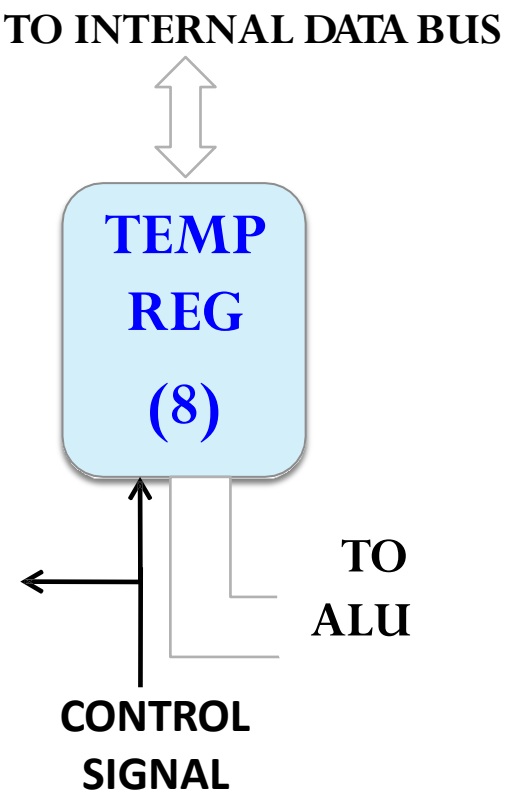
Temporary register

- In 8085 there are 2 temporary registers- w and z registers
- These two registers (w & z) are not available for user
- It is also called as operand register (8 bit)
- It provides operands to ALU. ALU can store immediate result in temporary register
- 8085 uses them internally to hold data temporary during execution of some instruction



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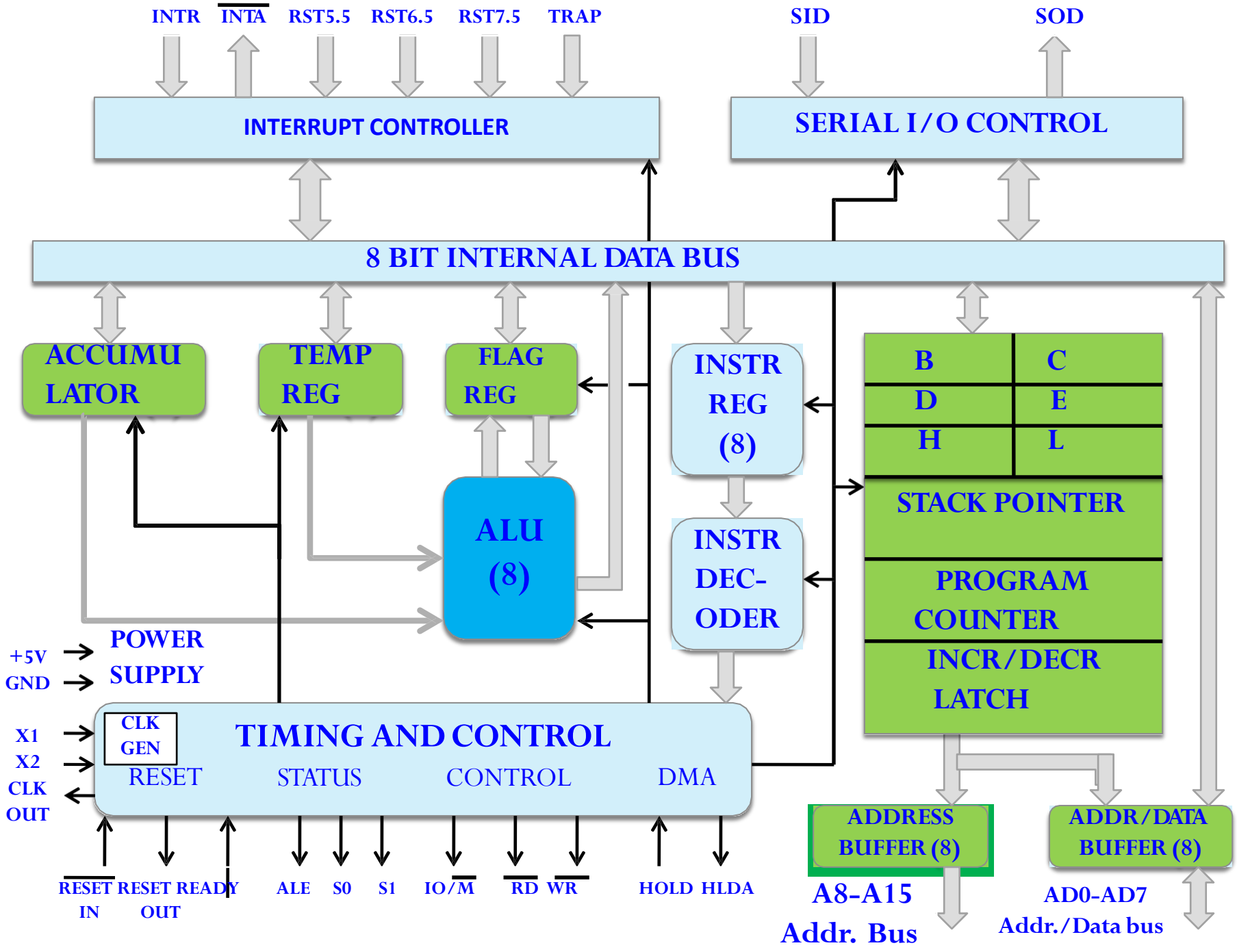
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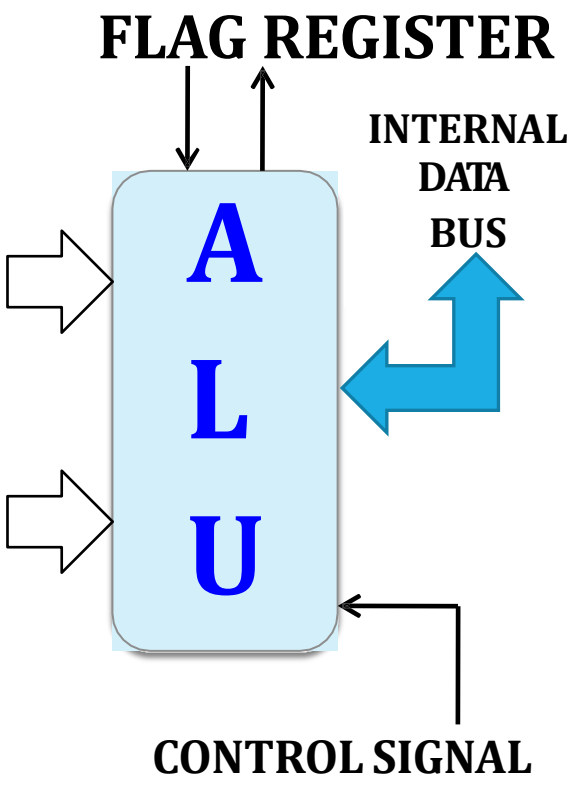
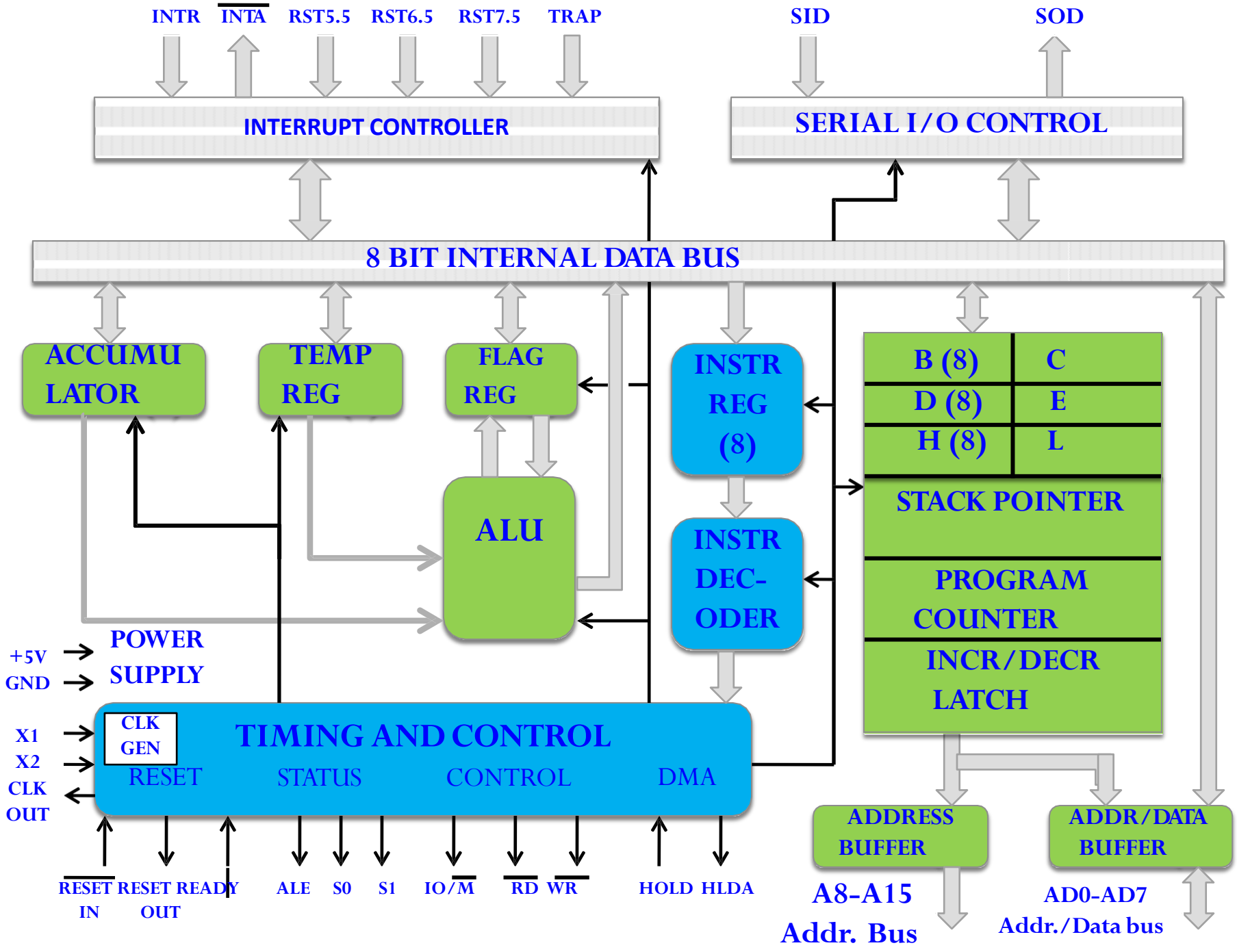
Arithmetic and logic unit

- ALU is a digital circuit that performs arithmetic and bitwise logical operations on integer binary numbers
- ALU is divided into two units, an arithmetic unit (AU) and a logic unit (LU)
- ALU has direct input and output access to the processor controller, main memory, and input/output devices
- It provides status or result of flag register

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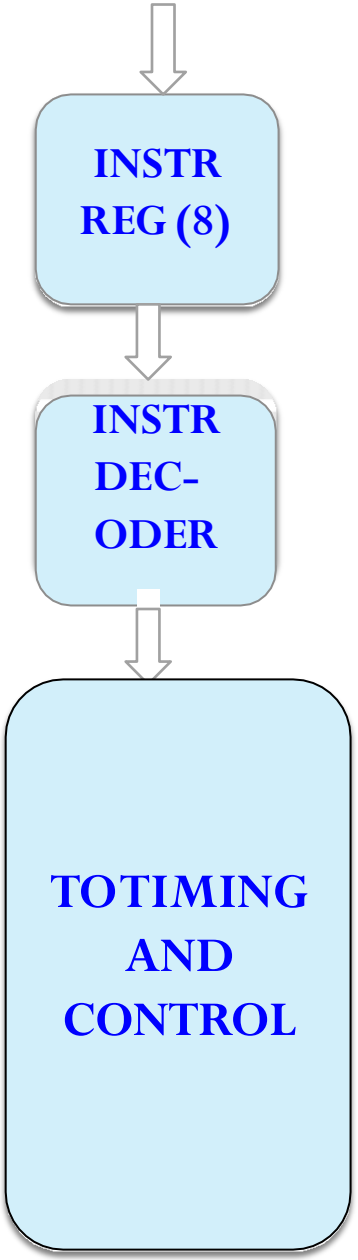
- **Instruction Register:-**
- Instruction register is 8-bit register just like every other register of the microprocessor
- The instruction may be anything like adding two data, moving a data, copying a data etc.
- When such an instruction is fetched from memory, it is directed to Instruction register. So the instruction registers are specifically to store the instructions that are fetched from memory
- **Instruction Decoder:-**
- Instruction decoder decodes the information present in the Instruction register for further processing
- It then send the decoded information to timing and control circuit



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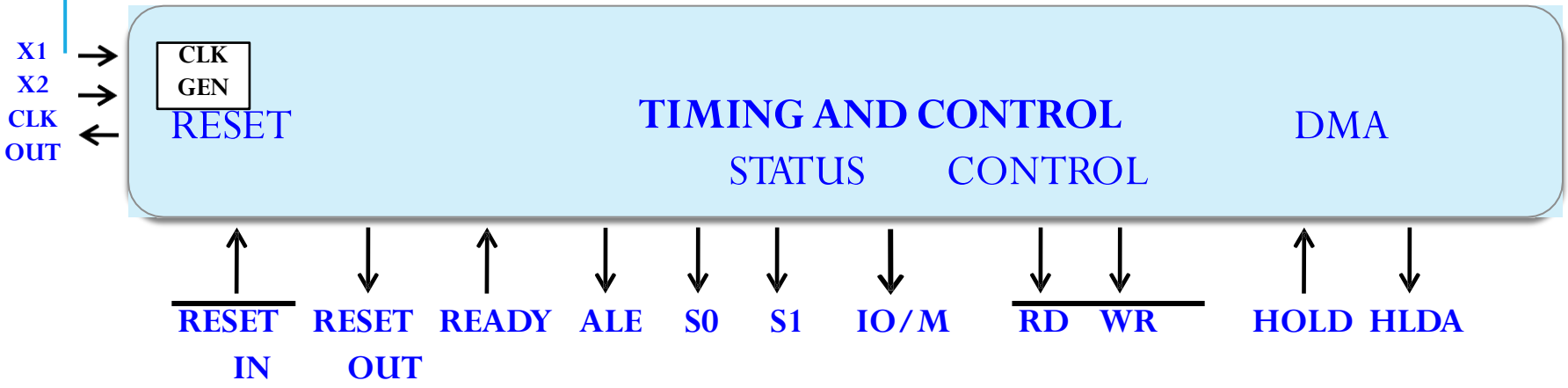
TIMING AND CONTROL UNIT



- Timing and control unit is a very important unit as it synchronizes the registers and flow of data through various registers and other units
- This unit consists of an oscillator and sends control signals needed for internal and external control of data and other units

CONTROL SECTION

- The oscillator generates clock signals which aids in synchronizing all the registers of 8085 microprocessor
- Signals that are associated with Timing and control unit are:
  - **Control Signals:** READY, RD(bar), WR(bar), ALE
  - **Status Signals:** S0, S1, IO/M(bar)
  - **DMA Signals:** HOLD, HLDA
  - **RESET Signals:** RESET IN(bar), RESET OUT

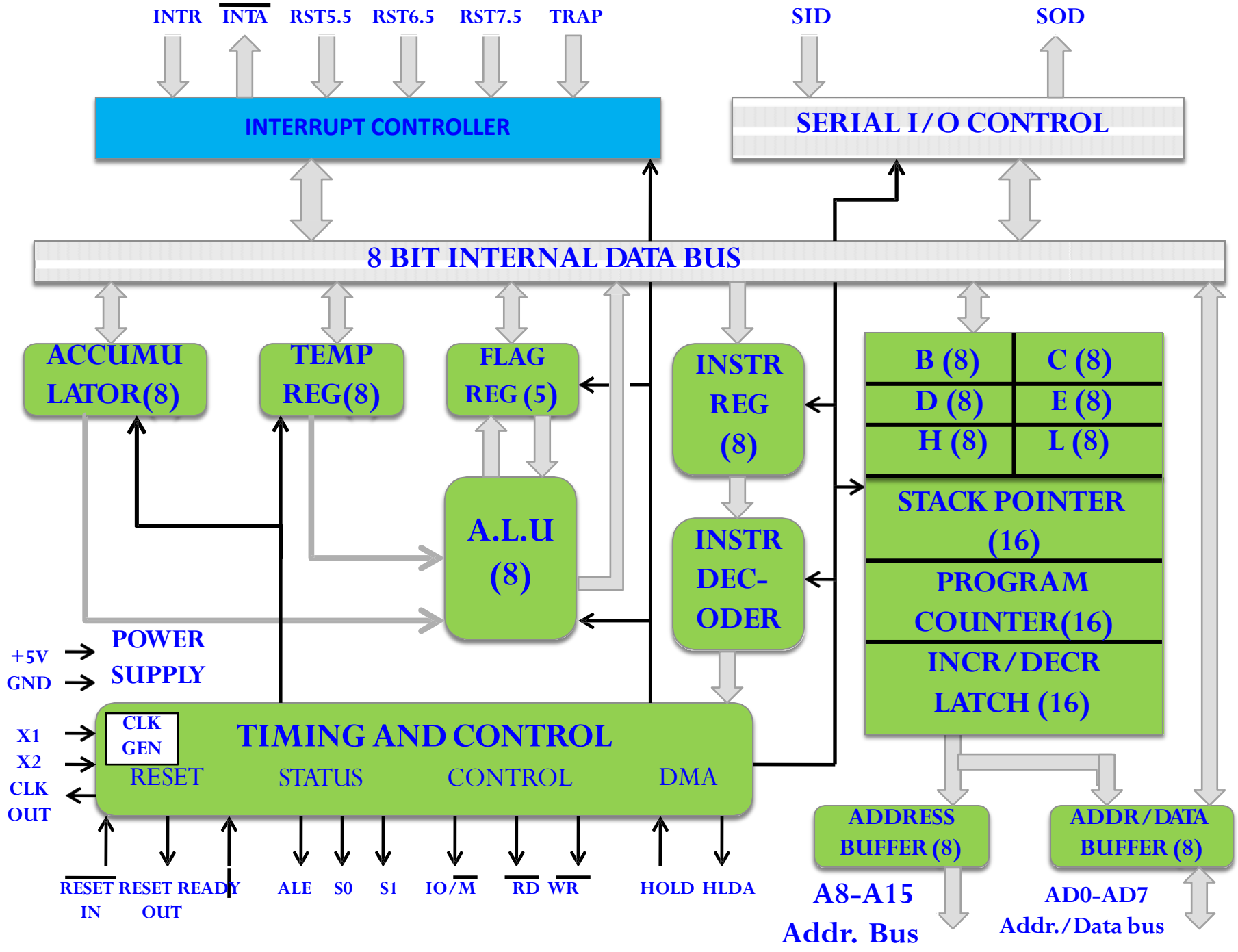
"

CONTROL AND STATUS SIGNALS

- RD – Read (active low). To indicate that the I/O or memory selected is to be read and data are available on the bus.
- WR – Write(Active low). This is to indicate that the data available on the bus are to be written to memory or I/O ports.
- IO/$\overline{M}$ – To differentiate I/O operation or memory operations.
  - '0' - indicates a memory operation.
  - '1'-indicates an I/O operation.
- IO/$\overline{M}$ combined with RD and WR to generate I/O and memory control signals.
- S1 and S0: Status signals can identify various operations as shown on the following table :

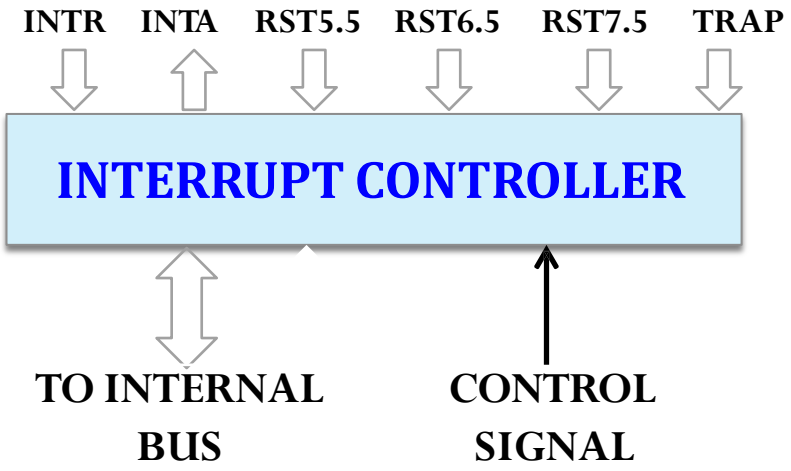
CONTROL AND STATUS SIGNALS

Operation	IO/M(bar)	S1	S0	Control Signal
Opcode Fetch	0	1	1	RD(bar)=0
Memory Read	0	1	0	RD(bar)=0
MemoryWrite	0	0	1	WR(bar)=0
I/O Read	1	1	0	RD(bar)=0
I/OWrite	1	0	1	WR(bar)=0
InterruptAck.	1	1	1	INTA(bar)=0
Halt	High Impedance	0	0	


INTR
INTA
RST5.5
RST6.5
RST7.5
TRAP
SID
SOD
INTERRUPT CONTROLLER
SERIAL I/O CONTROL
8 BIT INTERNAL DATA BUS
ACCUMU LATOR(8)
TEMP REG(8)
FLAG REG (5)
INSTR REG (8)
B (8)
C (8)
D (8)
E (8)
H (8)
L (8)
STACK POINTER (16)
PROGRAM COUNTER(16)
INCR/DECR LATCH (16)
A.L.U (8)
INSTR DEC- ODER
+5V
GND
POWER SUPPLY
X1
X2
CLK OUT
CLK GEN
TIMING AND CONTROL
RESET
STATUS
CONTROL
DMA
RESET IN
RESET OUT
READY
ALE
S0
S1
IO/M
RD
WR
HOLD
HLDA
ADDRESS BUFFER (8)
ADDR/DATA BUFFER (8)
A8-A15
Addr. Bus
AD0-AD7
Addr./Data bus

INTERRUPT CONTROLLER

- Interrupt signals present in 8085 are:
  1. INTR
  2. RST 7.5
  3. RST 6.5
  4. RST 5.5
  5. TRAP
- Whenever the interrupt signal is enabled or requested the microprocessor shifts the control from main program to process the incoming request and after the completion of request, the control goes back to the main program.



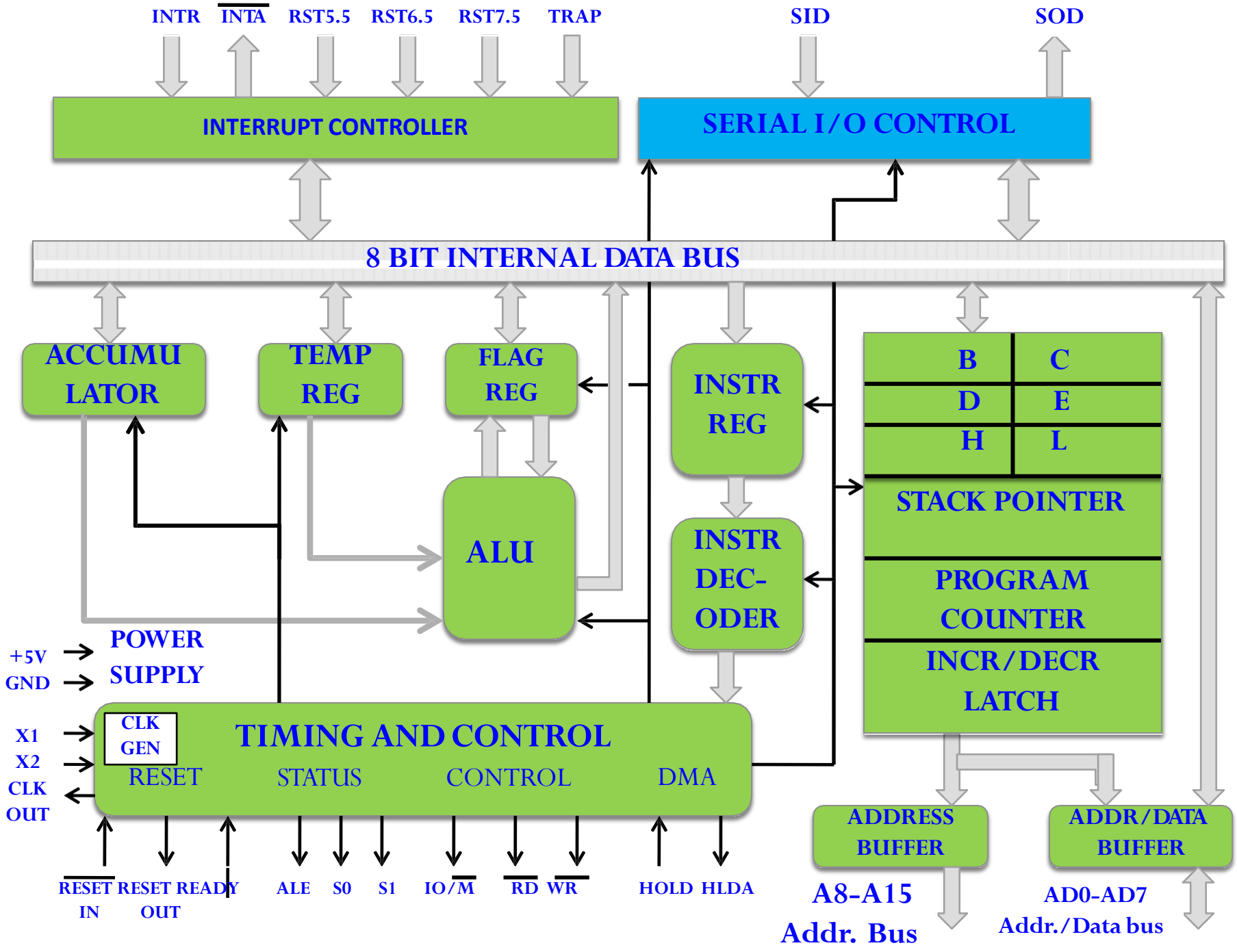
- Of the four interrupts TRAP is a NON-MASKABLE interrupt control and other three are maskable interrupts.
- A non-maskable interrupt is an interrupt which is given the highest priority in the order of interrupts.
- Suppose you want an instruction to be processed immediately, then you can give the instruction as a non- maskable interrupt.
- Further the non-maskable interrupt cannot be disabled by programmer at any point of time.
- Whereas the maskable interrupts can be disabled and enabled using EI(Enable interrupt) and DI (Disable interrupt) instructions.
- Among the maskable interrupts RST 7.5 is given the highest priority above RST 6.5 and least priority is given to INTR.

INTERRUPT SIGNALS

- An interrupt is a hardware-initiated subroutine CALL. When interrupt pin is activated, an ISR will be called interrupting the program that is currently executing

PIN	Subroutine Location
TRAP	0024
RST 5.5	002C
RST 6.5	0034
RST 7.5	003C

- **TRAP>RST7.5>RST 6.5>RST 5.5**
- TRAP is also called RST 4.5. This is nonmaskable interrupt and has the highest priority
- **RST 7.5, 6.5, 5.5 - Restart interrupt:** These are vectored interrupts that transfer the program control to specific memory locations. They have higher priorities than the INTR interrupt among of these three. Because INTR is non vectored it does not have any address.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Addr. Bus
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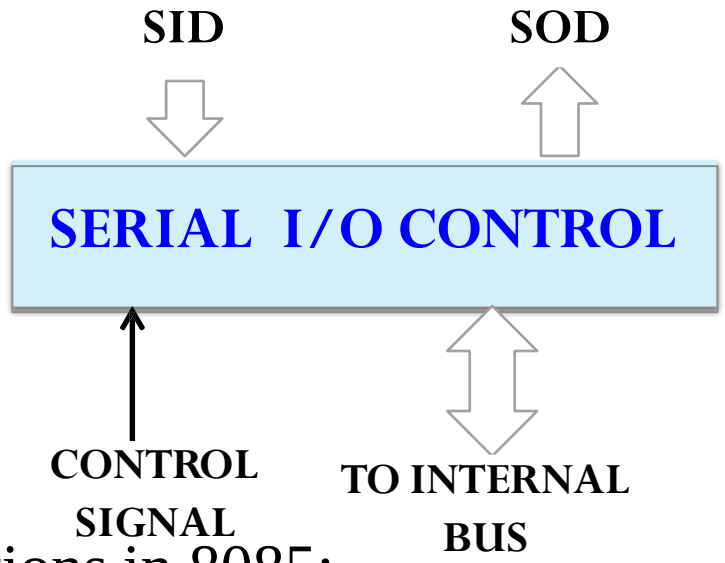
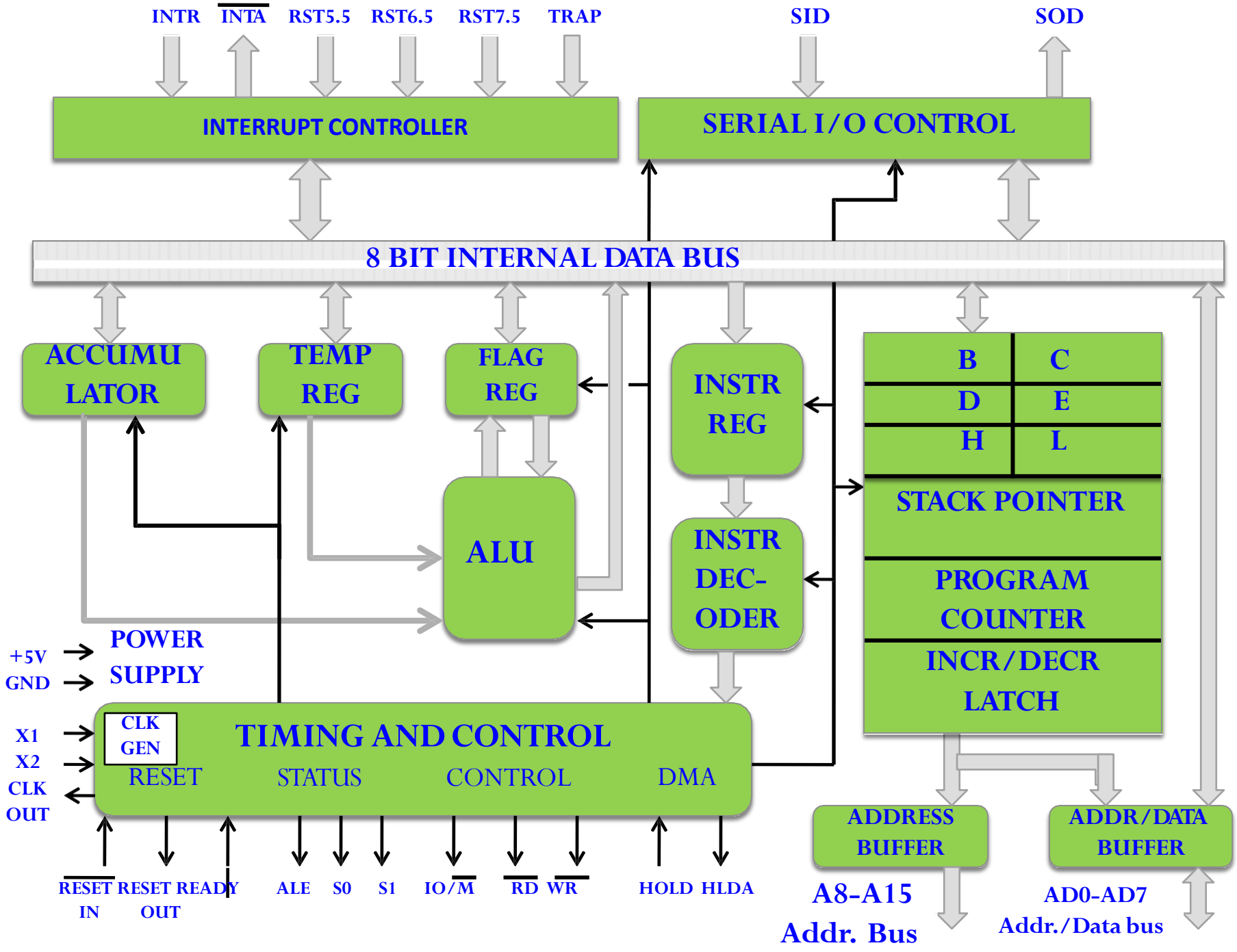
SERIAL I/O CONTROL



- The input and output of serial data can be carried out using two instructions in 8085:

1. SID-Serial Input Data
2. SOD-Serial Output Data

- Data on these line is accepted or transferred under software control by serial I/O control block, by using special instructions RIM & SIM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