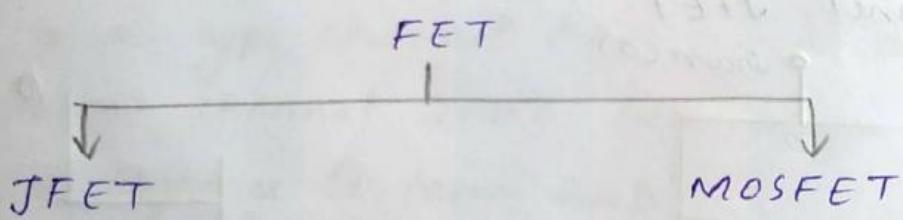


FIELD EFFECT TRANSISTORS

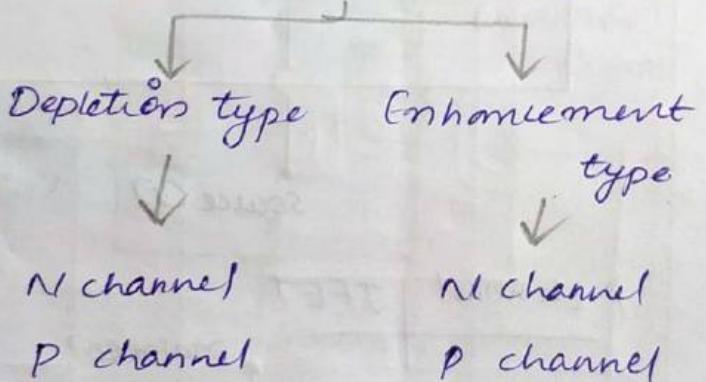
FET is a three terminal active semiconductor device where the flow of current (output current) is controlled by an electric field setup in the device by an externally applied voltage. Hence the name field effect transistor (FET). Here the current conduction is only by majority carriers. So FET is called a unipolar device. The three terminals of FET are source, drain and gate.



Junction Field Effect Transistor

N channel
P channel

Metal oxide semiconductor
field effect transistor



KtuQbank Principle of JFET

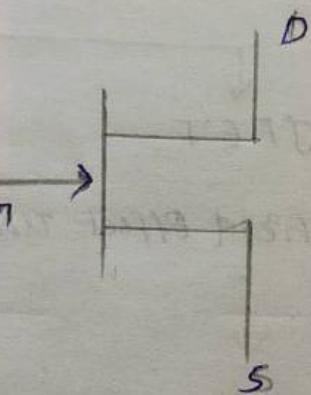
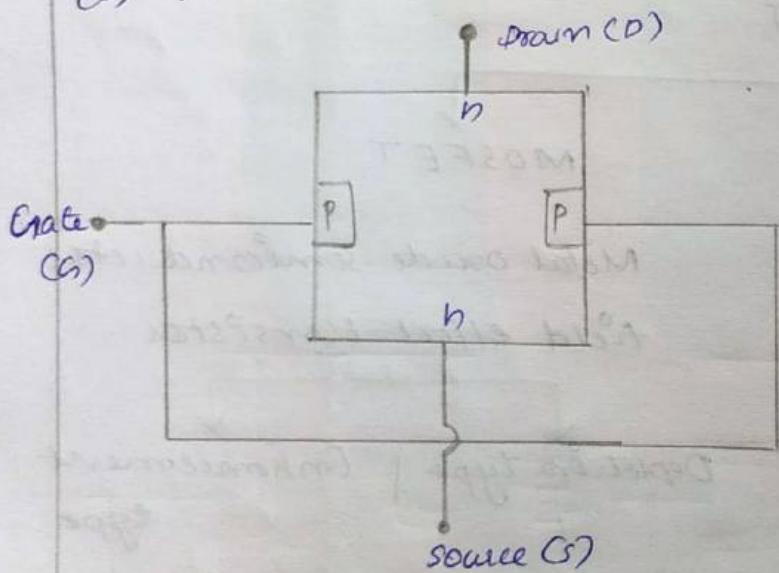
JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS} . In other words the magnitude of drain current (I_D) can be changed by altering V_{GS} .

Types of JFET

There are two types JFET

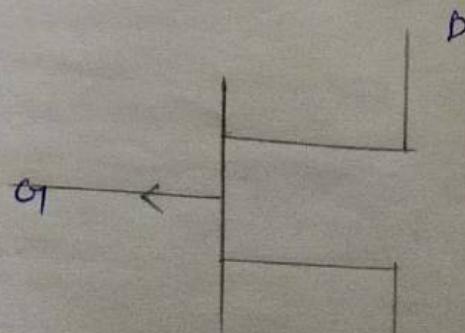
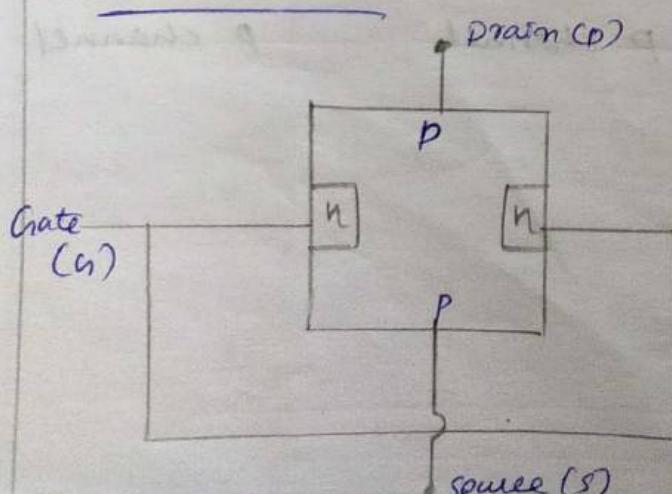
(a) n-channel JFET

(b) p-channel JFET



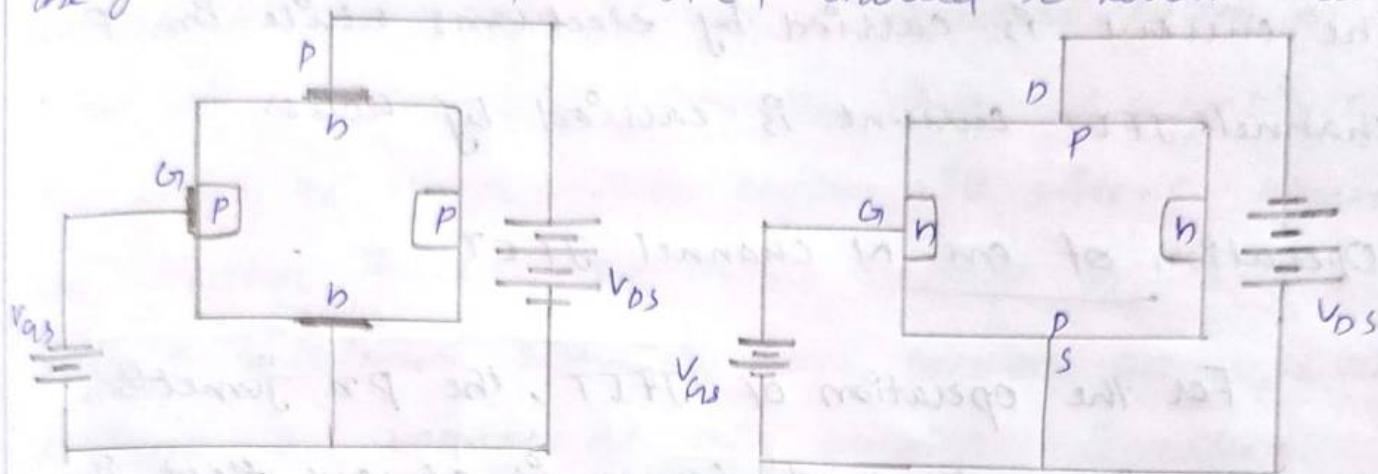
Symbol of n-channel JFET

P channel JFET



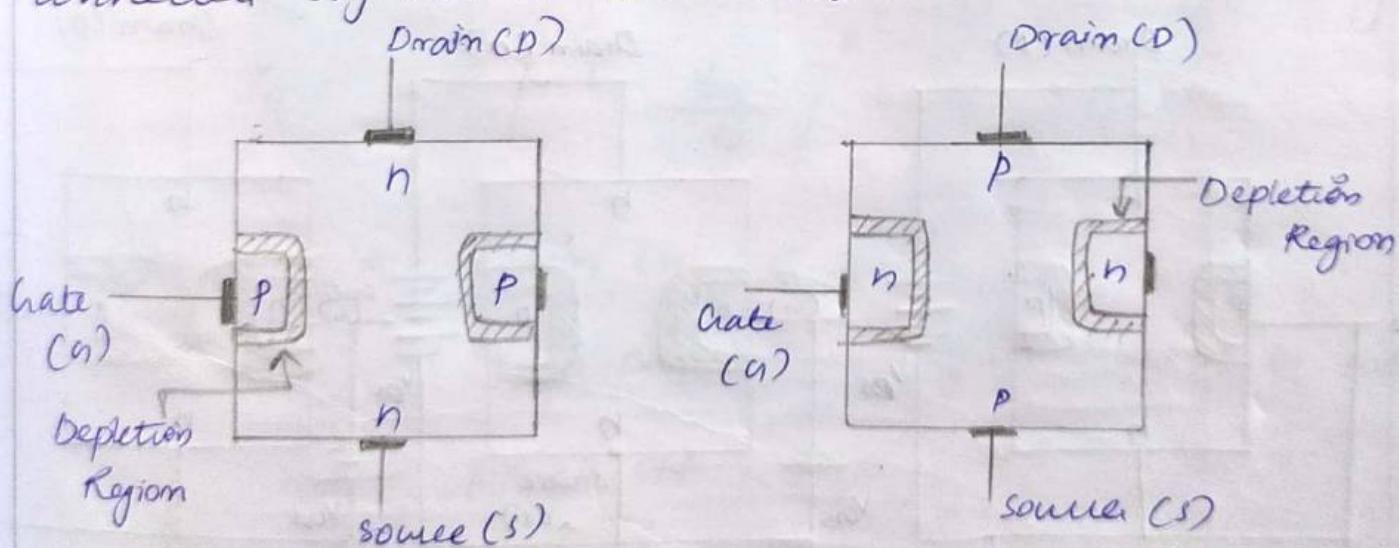
Symbol of p-channel JFET

→ The gate to source of a JFET should be reverse biased.



Construction or structure of JFET

The n-channel JFET consists of an n-type semiconductor with p-type semiconductor diffused regions. So there is a n-type channel from source to drain. Hence the name n-channel JFET. Both p type materials are connected together to form gate.



n channel JFET

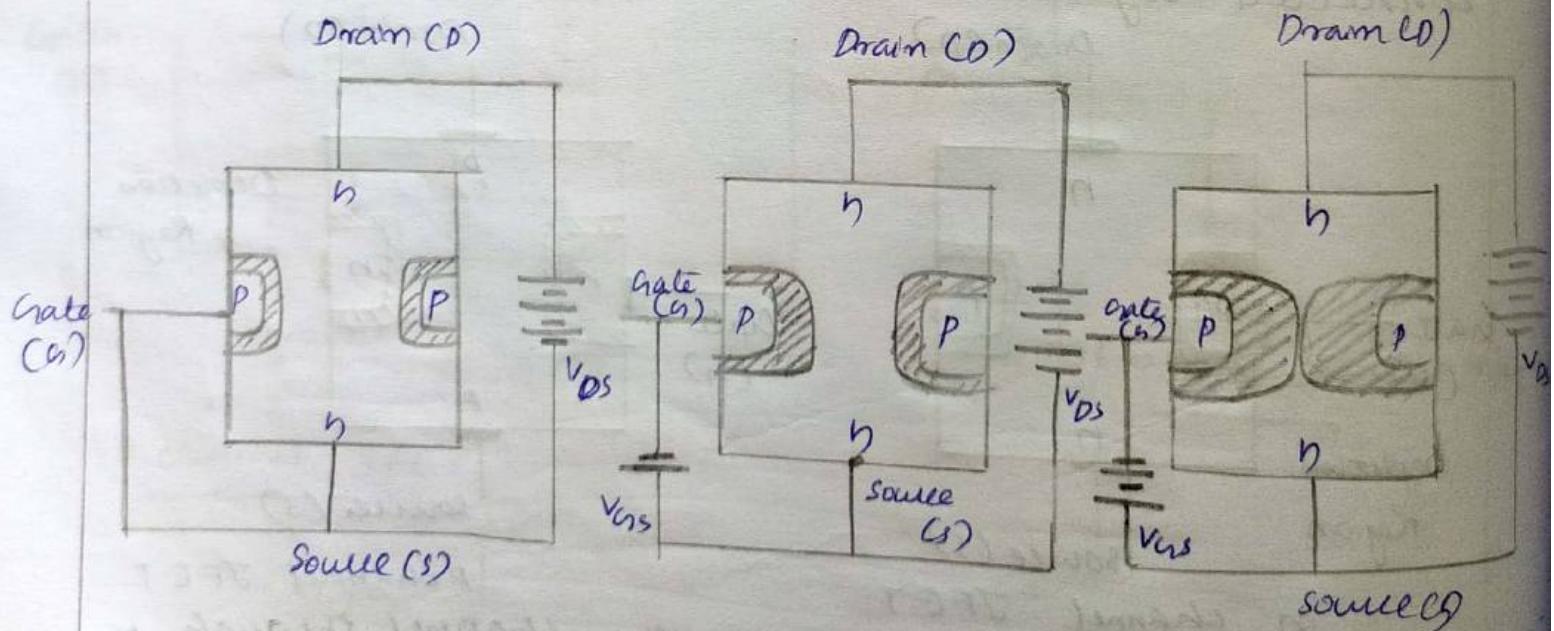
P channel JFET

The electrons enter the channel through the terminal called source and leave through the terminal called drain. If the gate is of n type and source, drain are p type, then the JFET

Ktu Q bank
 is called p-channel JFET. In n channel JFET the current is carried by electrons while for p channel JFET current is carried by holes.

Operation of an N channel JFET

For the operation of JFET, the pn junction between the gate and source is always kept in reverse biased condition. A bias source V_{GS} is connected between drain and source. The width of the depletion region can be varied by varying the negative gate voltage (V_{GS}).



- ① when $V_{GS} = 0$
- ② with small negative V_{GS}
- ③ with large negative V_{GS}

When the junction between gate and source is reverse biased. Then will be a depletion region on both sides of the channel. When V_{GS} increased negatively the width of the depletion region will widens. When we further increase the reverse voltage V_{GS} there will only a minimum separation (≈ 0) between two depletion regions. The voltage at this condition is called pinch off voltage V_p .

Thus for a given fixed drain to source voltage V_{DS} , the drain current I_D will be a function of gate to source voltage V_{GS} . In otherwords, the voltage applied to the gate controls the drain current.

Drain current for the pinch-off region is given by

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^2$$

where I_D = Drain current

I_{DSS} = Drain current with gate shorted to source

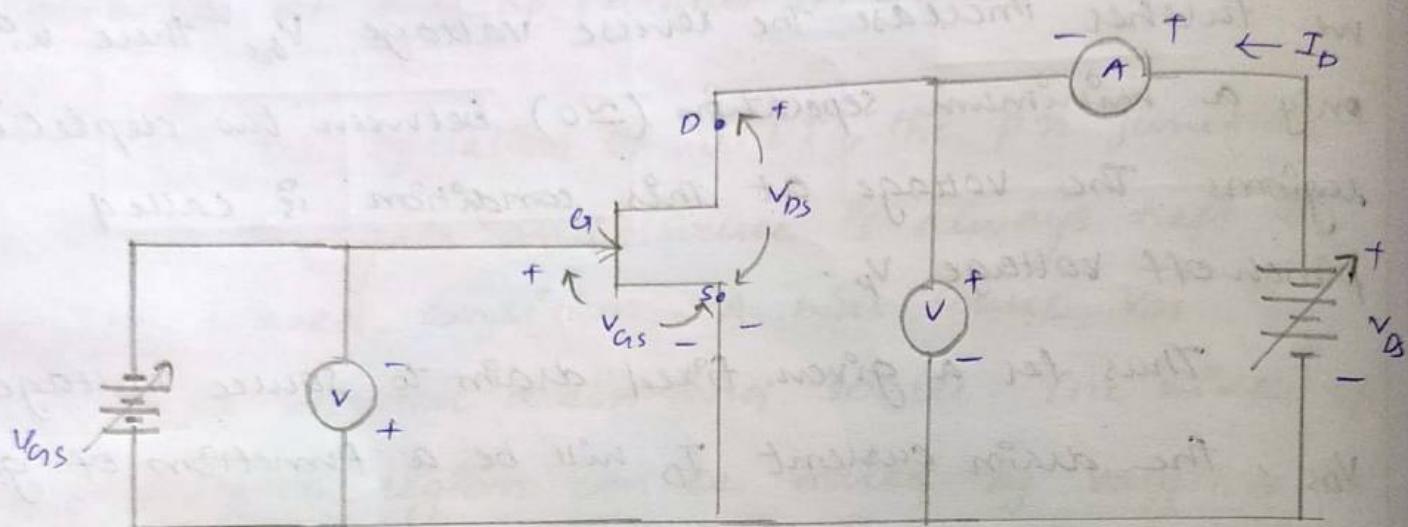
V_p = Pinch off voltage

JFET CHARACTERISTICS

The important characteristics of a JFET are

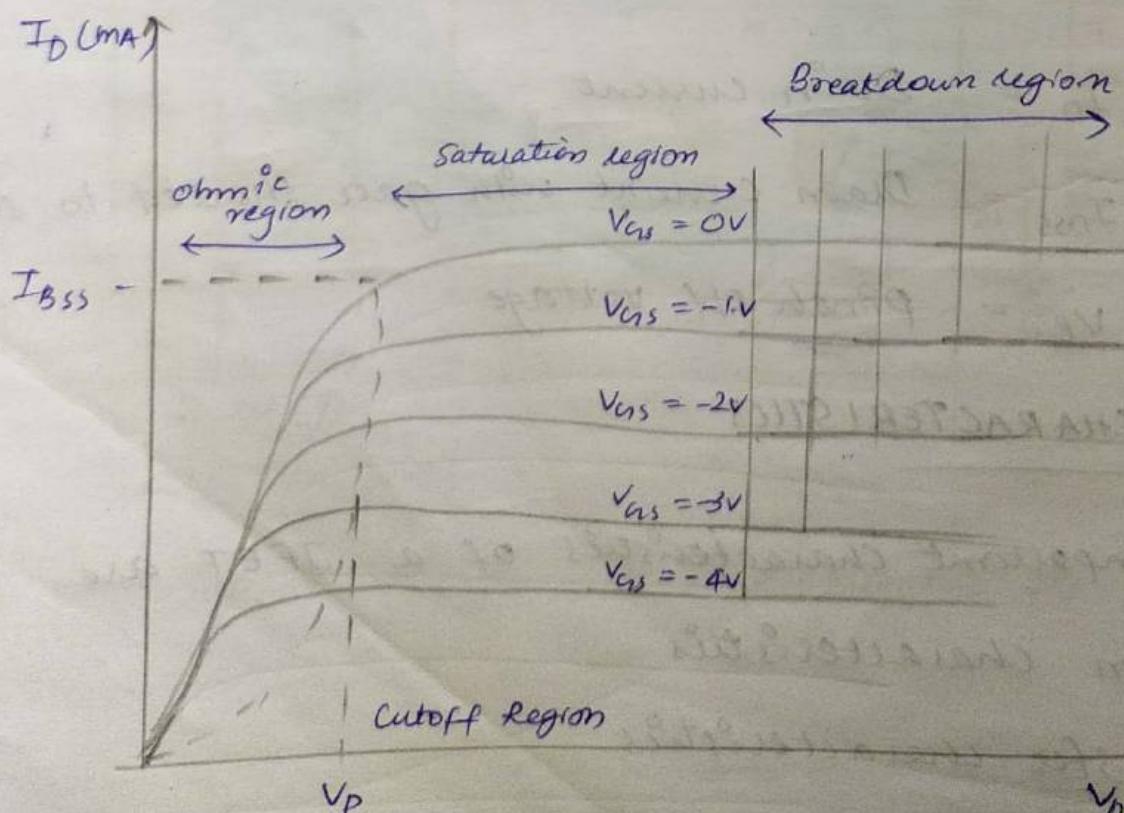
- 1) Drain characteristics
- 2) Transfer characteristics

The experimental setup to plot these two characteristic are shown in the figure below:



DRAIN CHARACTERISTICS

The drain characteristics is the plot of I_D versus V_{DS} for different values of V_{GS} .



Ktu Q bank : When V_{GS} and V_{DS} both equal to 0V.

Case 1 : When $V_{GS} = 0$, the channel is open. But $V_{DS} = 0$, so there is no attractive forces for the majority carriers and hence the drain current $I_D = 0$.

Case 2 : When $V_{GS} = 0$, $V_{DS} > 0$

At $V_{GS} = 0$, with small voltage V_{DS} , the drain current I_D increases linearly with V_{DS} . With increasing V_{DS} , the drain current I_D approaches the constant saturation value. The voltage V_{DS} at which the drain current I_D reaches its maximum value called pinch off voltage V_p . I_D is max at $V_{GS} = 0$.

Case 3 : When $V_{GS} < 0$

When an external bias (-IV) is applied to the gate the channel width reduces. The drain current I_D will reduce and pinch off voltage is reached at a lower drain current than when $V_{GS} = 0$.

Case 4 : Breakdown region

If we increase the value of V_{DS} beyond the pinch off voltage V_p , the drain current I_D remains constant upto a certain value of V_{DS} . If we further increase V_{DS} , the junction breakdown to

KtuQbank
due to avalanche effect and the drain current increases very sharply.

Case 5 : Saturation Region

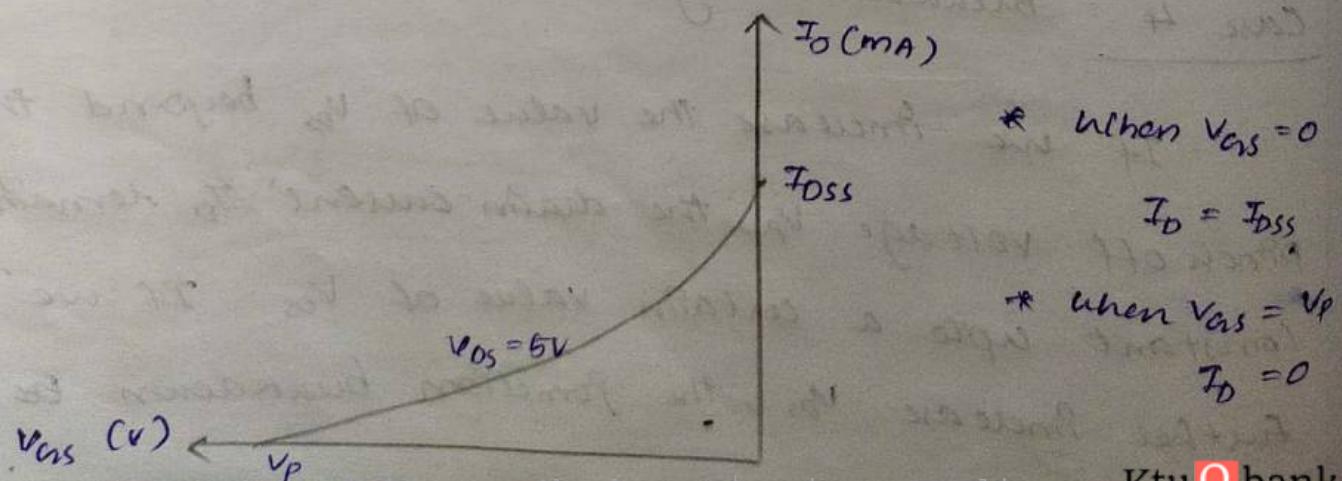
In this region the drain current I_D remains constant and does not vary with V_{DS} . To use FET as an amplifier, it is operated in the saturation region.

Case 6 : Cut off Region

The cut-off voltage is the value of V_{GS} at which the drain current is zero.

TRANSFER CHARACTERISTICS

It gives the relationship between the drain current I_D and gate to source voltage V_{GS} when V_{DS} kept constant. When V_{GS} is increased in the negative direction the drain current I_D will reduced and finally becomes zero.



Comparison between n-channel JFET and p channel JFET

n channel JFET	P channel JFET
1. Current carriers are electrons	Current carriers are holes.
2. Mobility of electrons are high	Mobility of holes are small.
3. Less noise	Noise is more than n-channel
4. High transconductance	Low transconductance.

Comparison between BJT and FET

BJT	FET
1. Bipolar device (operation depends on the flow of both majority and minority carriers).	Unipolar device (operation depends on the flow of majority carriers only).
2. Current controlled device (input current controls output current)	Voltage controlled device (input voltage controls output current).
3. Noisy (since current carriers has to cross two junctions)	Less noisy (No junction on the way of current carriers).
4. Low Input Impedance (input circuit is forward biased)	High Input Impedance (input circuit is reverse biased).

5.	Operation is temperature dependent.	Almost temperature independent
6.	Neutron radiation is more.	Immune to radiation
7.	High gain and band width	low gain bandwidth product.
8.	Fabrication is not easy.	Easy to fabricate

MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

A MOSFET is a type of FET which can be operated on both depletion and enhancement modes.

(1) Enhancement MOSFET (EMOSFET)

→ n channel E MOSFET

→ p channel E MOSFET

(2) Depletion MOSFET (DMOSFET) or DE MOSFET

→ n channel D MOSFET

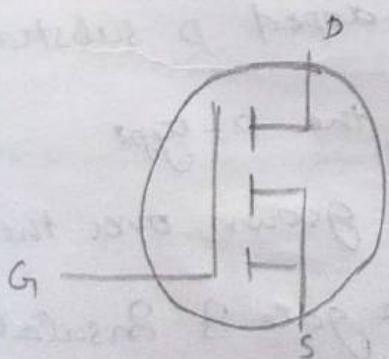
→ p channel D MOSFET

enhancement MOSFET (E MOSFET)

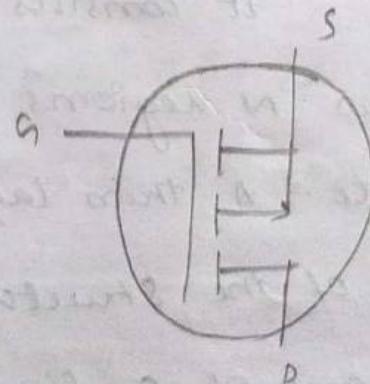
In this type of MOSFET there exists no channel between the source and drain. It does not conduct when $V_{GS} = 0$. It works with large positive gate voltages only. It is also called normally OFF MOSFET.

Depletion Enhancement MOSFET (DE MOSFET)

This type of MOSFET can be operated in both depletion mode and enhancement mode by changing the polarity of V_{GS} . When negative V_{GS} is applied, the DE MOSFET will operate in the depletion mode. With positive gate voltage, it operates in the enhancement mode. A channel is exists between drain and source and I_D flows even when $V_{GS} = 0$. DE MOSFET is also called normally on MOSFET.

SYMBOLS1) Enhancement MOSFET (E MOSFET)

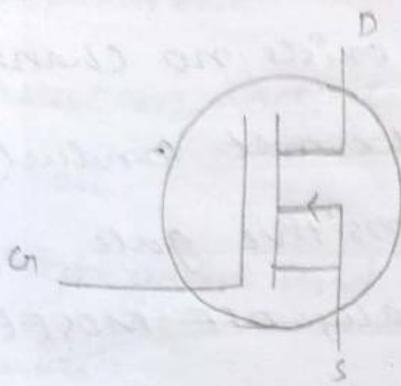
n channel EMOSFET



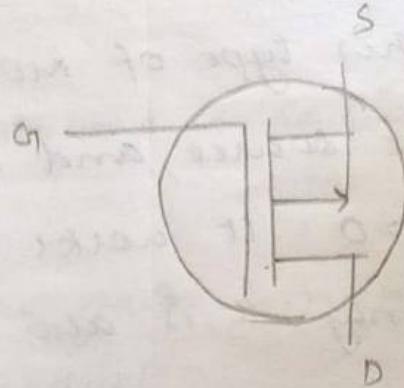
p channel E MOSFET

G - gate
S - source
D - drain

2) Depletion MOSFET (DE MOSFET)



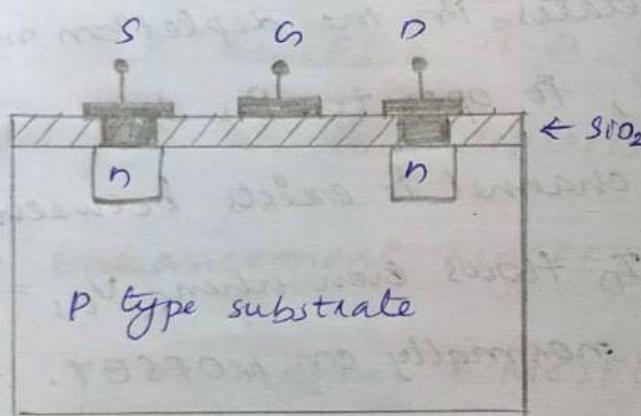
n channel DE MOSFET



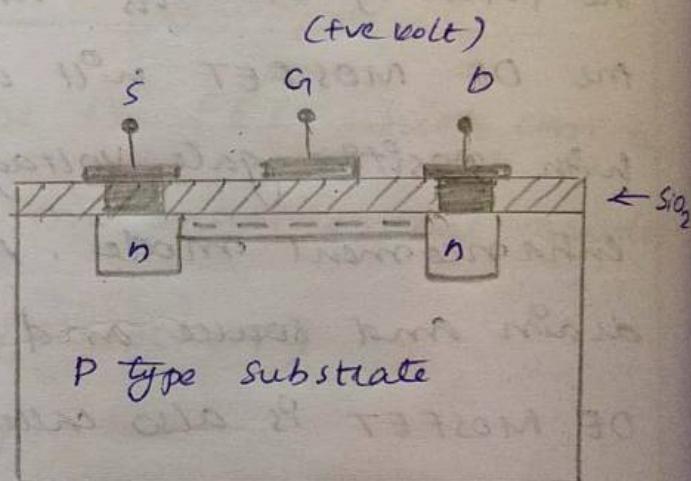
P channel DE MOSFET

Structure and working of MOSFET

Enhancement MOSFET



EMOSFET without channel

when $V_{GS} = 0$ 

EMOSFET with induced negative

channel when $V_{GS} = +ve \text{ volt}$

It consists of a lightly-doped P substrate and two N regions diffused into the P-type substrate. A thin layer of SiO_2 is grown over the surface of the structure. Since the gate is insulated by means of a SiO_2 layer, this type of FET is also called Insulated Gate FET.

Ktu Q bank

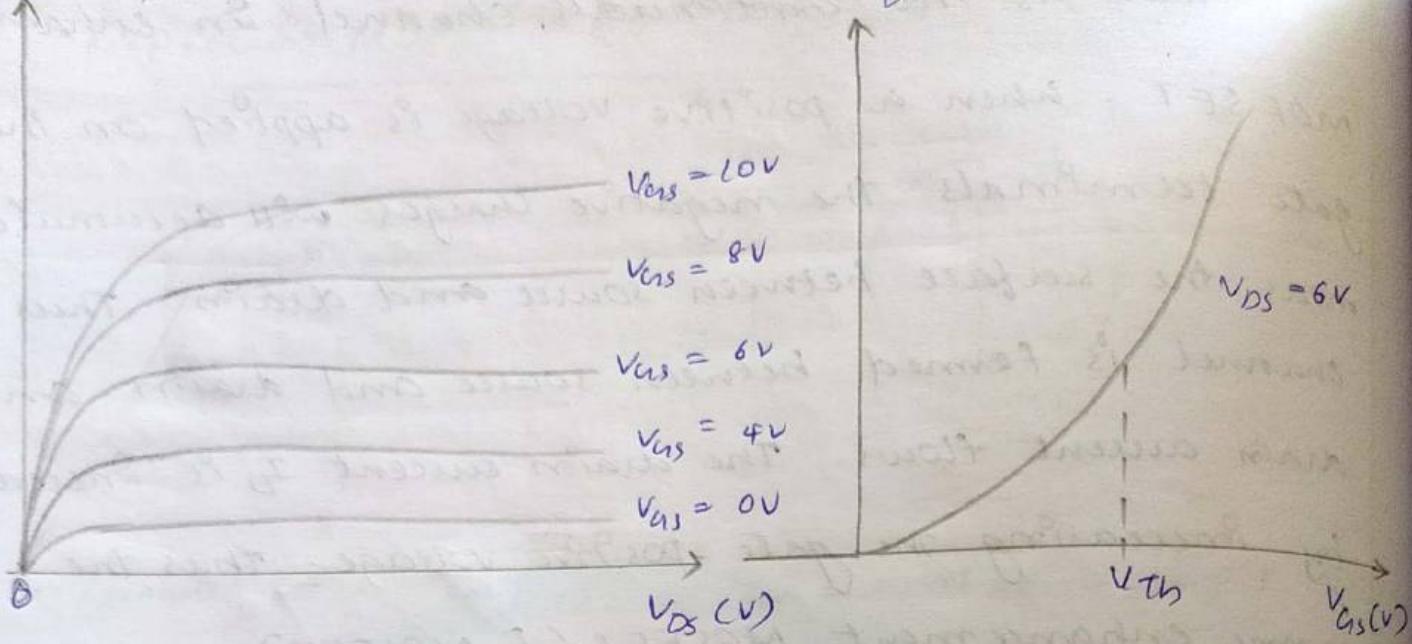
There is no continuous channel in enhancement MOSFET. When a positive voltage is applied on the gate terminals the negative charges will accumulate near the surface between source and drain. Thus a channel is formed between source and drain and drain current flows. The drain current I_D is increased by increasing the gate positive voltage thus the name enhancement MOSFET (E MOSFET).

Drain Characteristics of N channel E MOSFET

Drain characteristics is the plot of drain current I_D versus drain source voltage V_{DS} for different values of V_{GS} . If $V_{GS} = 0$, the drain current is negligible. But if V_{GS} is increased positively, a strong negative channel is induced between source and drain and drain current increases.

Transfer characteristics of N channel E MOSFET

Transfer chara shows the variations of drain current I_D with gate voltage V_{GS} for constant V_{DS} .



Drain chara of E MOSFET

Transfer chara of E MOSFET

Comparison between JFET and MOSFET

	JFET	MOSFET
1.	operates in the depletion mode only.	Operated in both enhancement mode or depletion mode.
2.	Leakage current is more.	Leakage current is less.
3.	Larger gate current	Lower gate current
4.	High drain resistance	Low drain resistance
5.	Manufacturing is not easy.	Easy to manufacture.
6.	Input resistance is less than MOSFET (10^8 ohms).	Input resistance is more than JFET (10^{10} ohms to 10^{15} ohms)

FET PARAMETERS

1) Drain saturation current (I_{DSS}) :-

It is the value of I_D max when $V_{GS} = 0$

2) Drain resistance (R_d) :-

It is defined as the ratio of small change in V_{DS} to the small change in I_D keeping the gate to source voltage constant.

$$R_d = \frac{\Delta V_{DS}}{\Delta I_D} \quad \text{keeping } V_{GS} \text{ constant}$$

Typical range of R_d : $15\text{ k}\Omega$ to $1M\Omega$

3) Mutual Conductance or Transconductance (g_m) :-

It is defined as the ratio of small change in I_D to small change in V_{GS} , keeping V_{DS} constant.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad \text{keeping } V_{DS} \text{ constant}$$

Typical range of g_m : 200 mho to 800 mho

$$g_m = g_{m0} \left[1 - \frac{V_{GS}}{V_p} \right] = g_{m0} \sqrt{\frac{I_D}{I_{DSS}}}$$

(4) Amplification factor (μ) :-

It is defined as $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$ keeping I_D constant

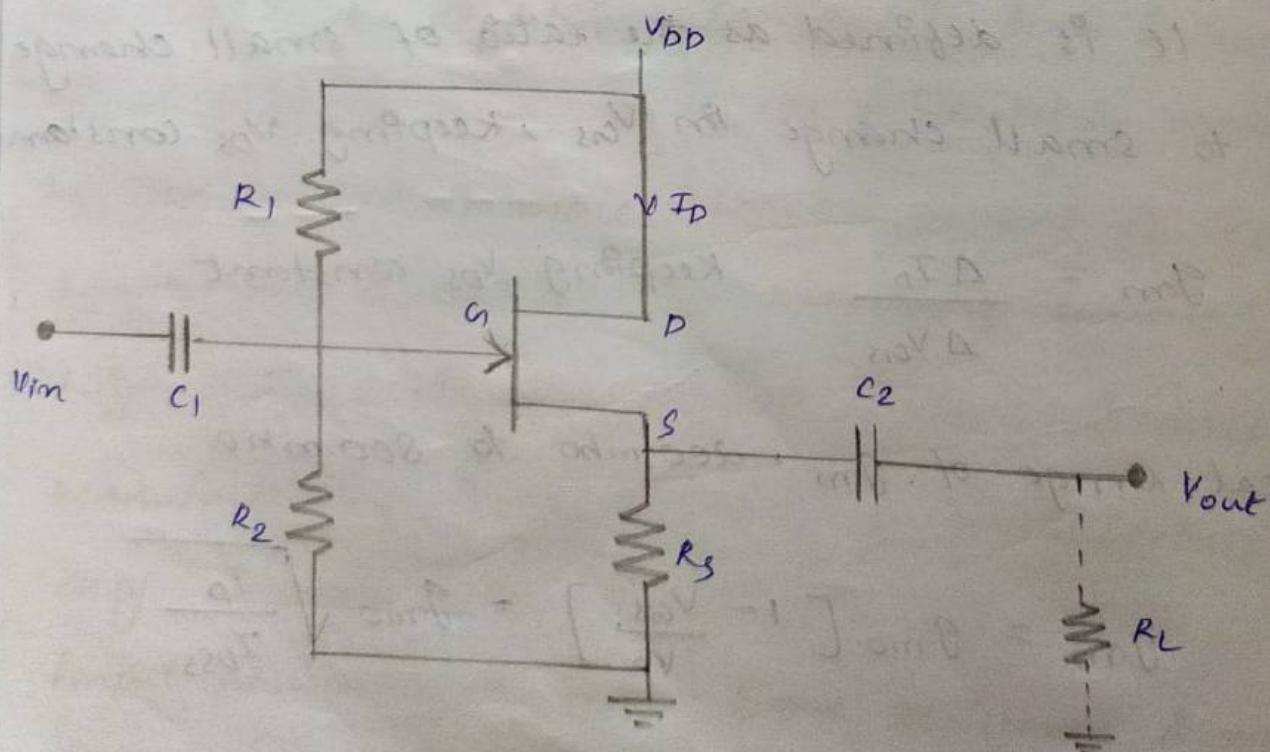
$$\mu = r_d \times g_m$$

$$\text{Proof : } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \quad g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$r_d \times g_m = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \mu$$

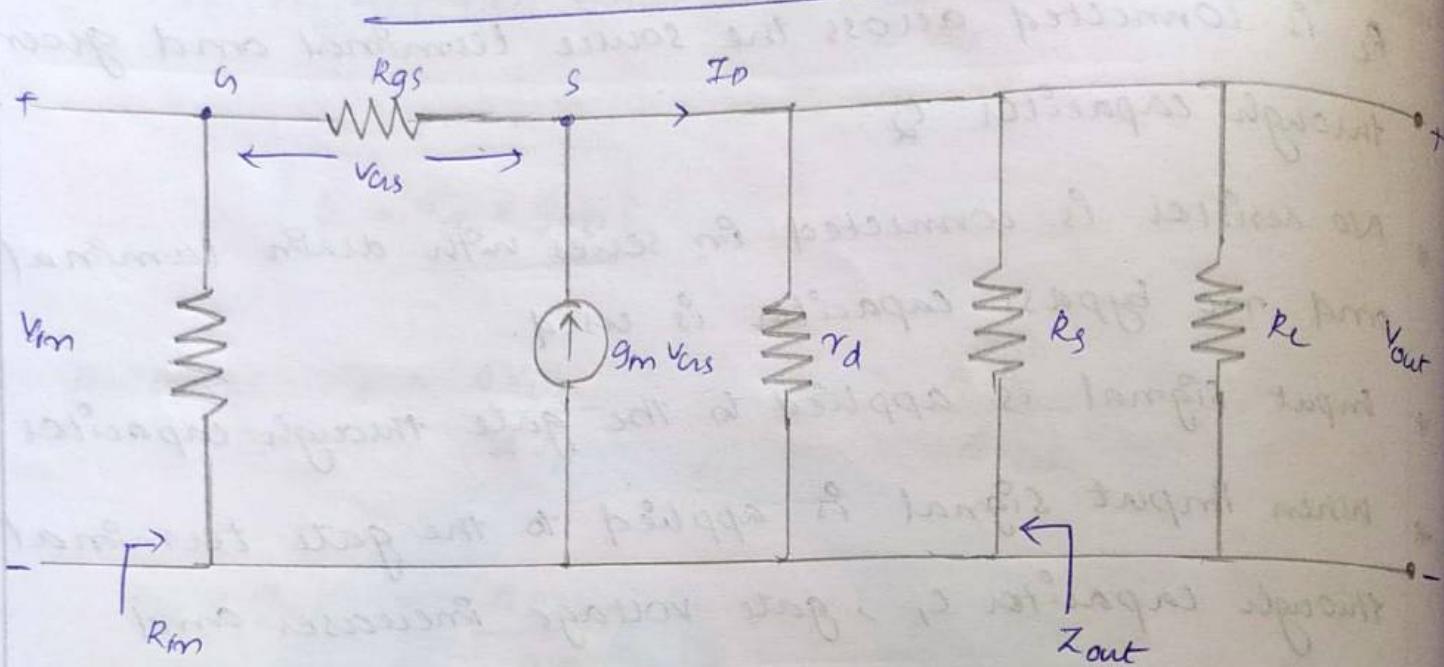
$$\therefore \mu = r_d \times g_m$$

Common Drain JFET-amplifier (source follower)



- * In a common drain or source follower circuit, output voltage is developed across R_S . External load resistor R_L is connected across the source terminal and ground through capacitor C_2 .
- * No resistor is connected in series with drain terminal and no bypass capacitor is used.
- * Input signal is applied to the gate through capacitor C_1 .
- * When input signal is applied to the gate terminal through capacitor C_1 , gate voltage increases and decreases as the input signal goes positive and negative respectively.
- * Since output is taken from source terminal, output voltage is approximately same as the V_D voltage. Thus the common drain circuit can be said to have approximately unit gain.
- * Output voltage at the FET source terminal follows the variations in the signal voltage applied to the gate. Hence common drain circuit is also called source follower.

KtuQbank equivalent circuit or small signal analysis of common drain JFET amplifier



① Input impedance :-

$$R_{in} = R_G = R_1 \parallel R_2$$

② Output impedance :-

$$Z_{out} = \frac{1}{g_m} \parallel r_d \parallel R_s$$

$$\text{Usually } r_d \gg \frac{1}{g_m}$$

$$\therefore Z_{out} = \frac{1}{g_m} \parallel R_s$$

③ Voltage gain :-

$$V_{out} = I_D [R_s \parallel r_d \parallel R_L]$$

$$= g_m V_{gs} [R_s \parallel r_d \parallel R_L]$$

$$V_{in} = V_{gs} + V_{out}$$

$$= V_{gs} + g_m V_{gs} [R_s \parallel r_d \parallel R_L]$$

$$= V_{gs} [1 + g_m [R_s \parallel r_d \parallel R_L]]$$

$$\text{Voltage gain } A_v = \frac{V_{out}}{V_{in}} = \frac{g_m V_{gs} [R_s \parallel r_d \parallel R_L]}{V_{gs} [1 + g_m [R_s \parallel r_d \parallel R_L]]}$$

$$= \frac{g_m [R_s \parallel r_d \parallel R_L]}{1 + g_m [R_s \parallel r_d \parallel R_L]}$$

Usually r_d is very high

$$A_v = \frac{g_m [R_s \parallel R_L]}{1 + g_m [R_s \parallel R_L]}$$

PROBLEMS

1. The common drain circuit has $R_1 = 4M\Omega$, $R_2 = 2M\Omega$

$R_s = 2.5 k\Omega$, $R_L = 25 k\Omega$ and $g_m = 2500 \mu A/V$.

Determine

(i) Input impedance

(ii) Output impedance

(iii) Voltage gain.

Ans - (i) Input Impedance

$$R_{in} = R_{in} = R_1 \parallel R_2$$

$$= 4 \times 10^6 \parallel 2 \times 10^6$$

$$= \underline{1.33 \text{ M}\Omega}$$

(ii) Output Impedance

$$R_o = Z_o = R_s \parallel \frac{1}{g_m}$$

$$= 2.5 \text{ k}\Omega \parallel \frac{1}{2500 \times 10^{-6}}$$

$$= \underline{345 \Omega}$$

(iii) Voltage gain

$$A_v = \frac{g_m [R_s \parallel R_L]}{1 + g_m [R_s \parallel R_L]}$$

$$= \frac{2500 \times 10^{-6} [2.5 \times 10^3 \parallel 25 \times 10^3]}{1 + 2500 \times 10^{-6} [2.5 \times 10^3 \parallel 25 \times 10^3]}$$

$$= \underline{0.85}$$

d. The data sheet of an n channel JFET gives the following circuit details. $I_{DSS} = 9 \text{ mA}$ and pinch off voltage $V_P = -4.5 \text{ V}$.

- At what values of V_{GS} will I_D equal to 3 mA .
- What is its g_m at this I_D .

$$(i) I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

$$I_D = 3 \text{ mA}$$

$$= 3 \times 10^{-3} = 9 \times 10^{-3} \left[1 - \frac{V_{GS}}{-4.5} \right]^2$$

$$I_{DSS} = 9 \text{ mA}$$

$$V_P = -4.5$$

$$V_{GS} = \underline{\underline{-1.9 \text{ V}}}$$

$$V_{GS} = ?$$

$$(ii) g_m = g_{mo} \left[1 - \frac{V_{GS}}{V_P} \right]$$

$$g_{mo} = \frac{-2 I_{DSS}}{V_P} = \frac{-2 \times 9 \times 10^{-3}}{-4.5} = \underline{\underline{4 \text{ ms}}}$$

$$g_m = 4 \left[1 + \frac{1.9}{-4.5} \right] = \underline{\underline{2.31}}$$

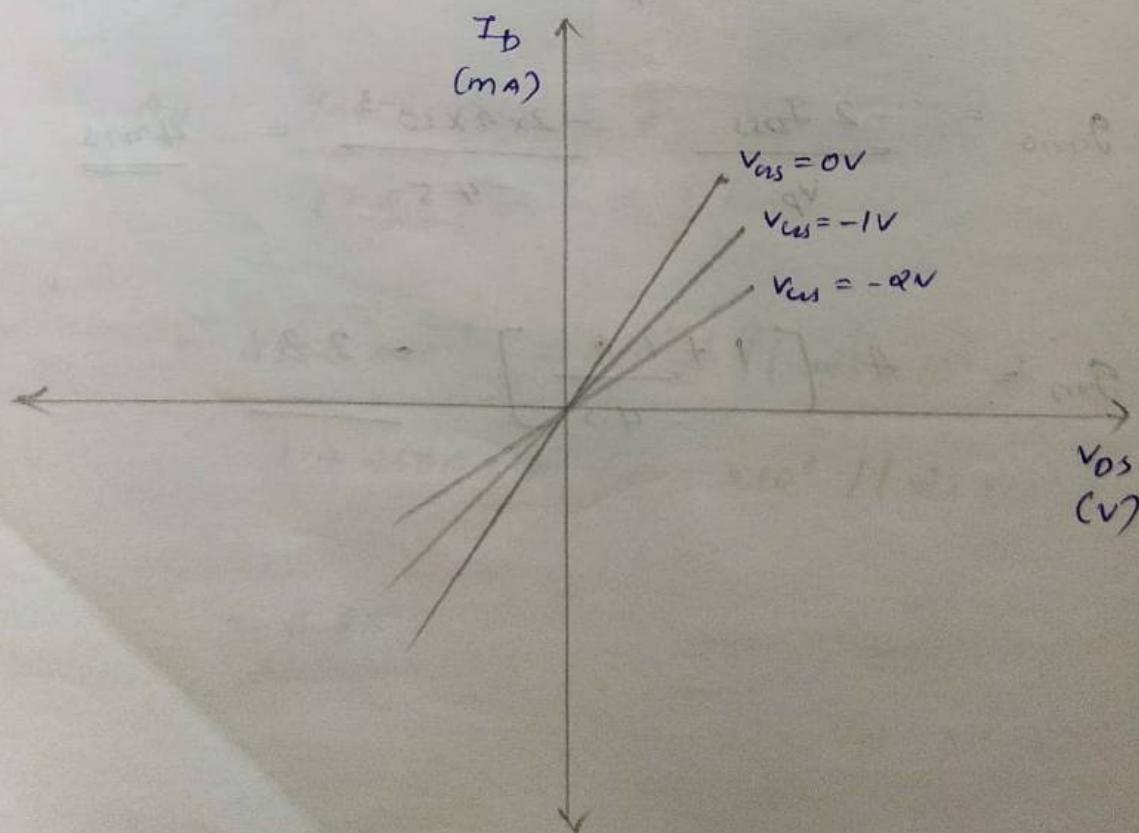
APPLICATIONS OF FET

1. FET as a voltage variable Resistor (VVR) :

* FET is usually operated in the constant current portion of its output characteristics i.e saturation region.

* If it is operated in the region prior to pinch off it behaves as a voltage variable resistor (VVR) i.e in the ohmic region.

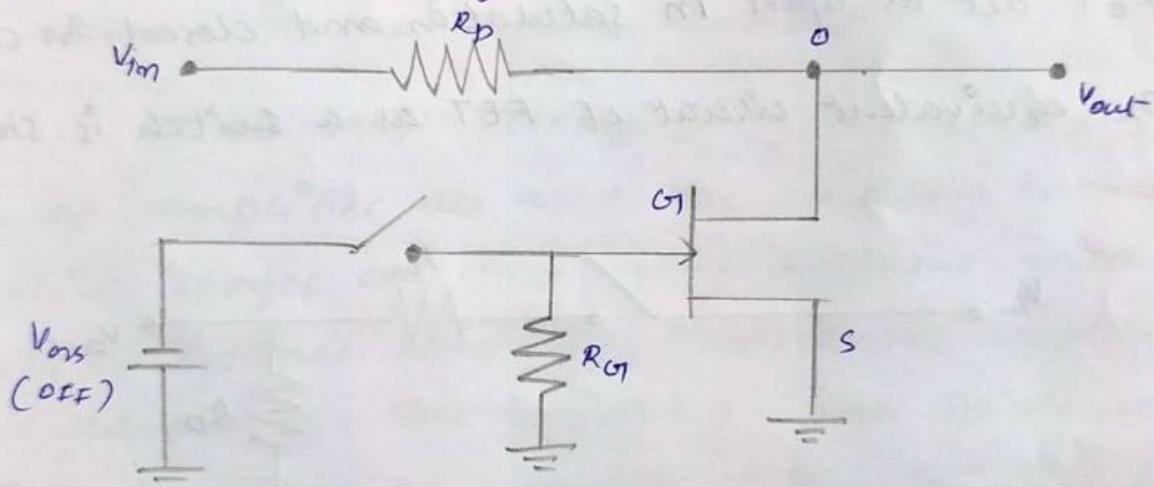
It is due to the fact that in this region drain to source resistance R_{DS} can be controlled by varying the gate bias voltage V_{GS} .



In such applications FET is also referred as a voltage variable resistor or voltage dependent resistor. In the figure the drain curves extended on both sides of the origin. This means that JFET can be employed as a voltage variable resistors for small ac signals.

2. FET as a switch :

FET as an analog switch is shown below



→ when no gate voltage is applied to the FET i.e $V_{GS} = 0$, FET will become saturated and it behaves like a small resistance (less than 100Ω)

$$\therefore \text{The o/p voltage } V_{out} = \frac{V_{in} R_{DS(\text{ON})}}{R_D + R_{DS(\text{ON})}}$$

If $R_D \gg R_{DS(\text{ON})}$

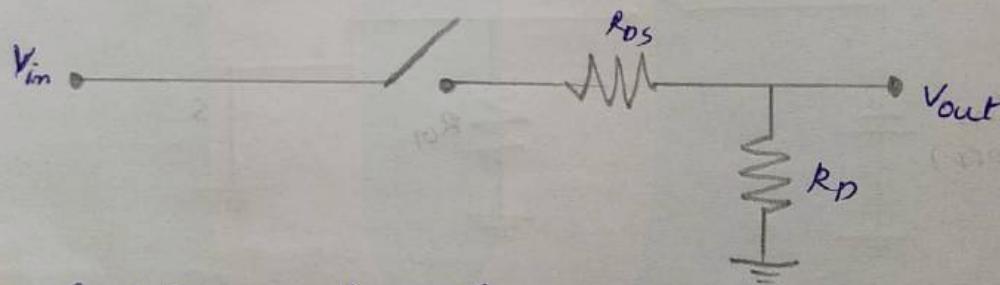
$$\therefore V_{out} = V_{in} \cdot \frac{R_{DS(\text{ON})}}{R_D} \cong 0$$

→ When a -ve voltage equal to $V_{DS(OFF)}$ is applied to the gate, the FET operates in the cutoff region i.e. $I_D = 0$.
It acts a very high resistance. Hence the output voltage become nearly equal to input voltage.

$$R_{DS(ON)} \gg R_D$$

$$V_{out} = V_{in} \frac{R_{DS(ON)}}{R_{DS(ON)}} = V_{in}$$

→ FET act as open in saturation and closed in cutoff mode.
∴ The equivalent circuit of FET as a switch is shown below



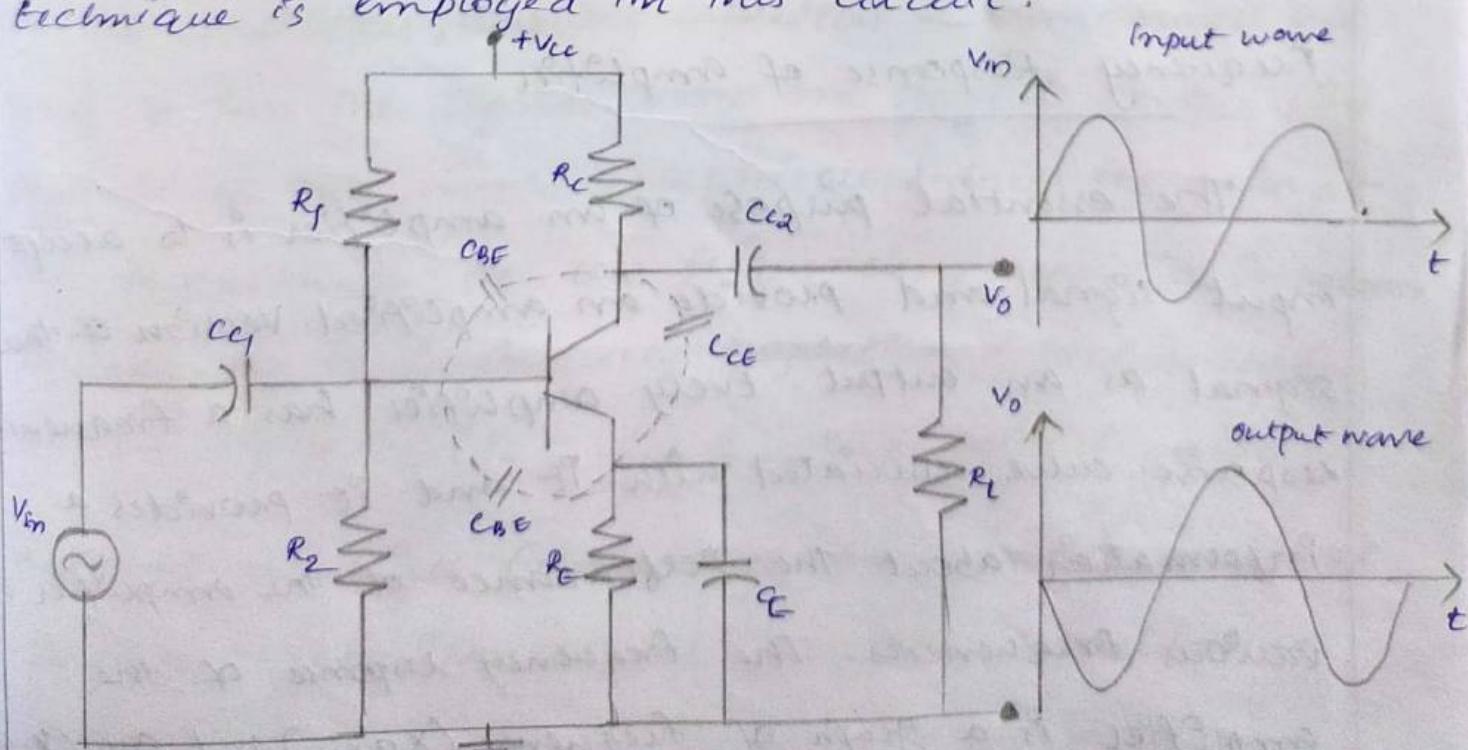
When V_{DS} is high, switch is closed, JFET output voltage is equivalent to input voltage.

When V_{DS} is low, switch is open, JFET output voltage is approximately 0.

RC COUPLED AMPLIFIER

common emitter (CE) amplifier is widely used in audio frequency applications in radio and TV receivers. It provides current, voltage and power gains. For the proper functioning of an amplifier, the transistor must be biased in the active region where the base current has complete control over the collector current. Thus a small increase in the base current results in a relatively large increase in the collector current and a small decrease in the base current is followed by a large decrease in the collector current.

When large voltage gain is required, many stages of amplifier are used. The coupling between successive stages are done using different methods namely resistance coupling, transformer coupling and direct coupling. The coupling stage in RC coupled amplifier forms an RC network. Voltage divider bias technique is employed in this circuit.



Resistors R_1 and R_2 are called potential divider resistors because they develop certain fixed voltage across them, derived from V_{cc} supply. Resistor R_E stabilizes the operating point against temperature variation.

The purpose of the coupling capacitors is to couple the ac signal and block dc. Coupling capacitor C_1 , couples the input ac signal V_{in} to the input of the amplifier. Coupling capacitor C_2 is very used to block the dc component of the output voltage from reaching the load resistor R_L . The purpose of bypass capacitor C_E is to bypass the ac signal developed across R_E to ground. Presence of C_E raises the gain of the amplifier but reduces its band width. The output voltage is

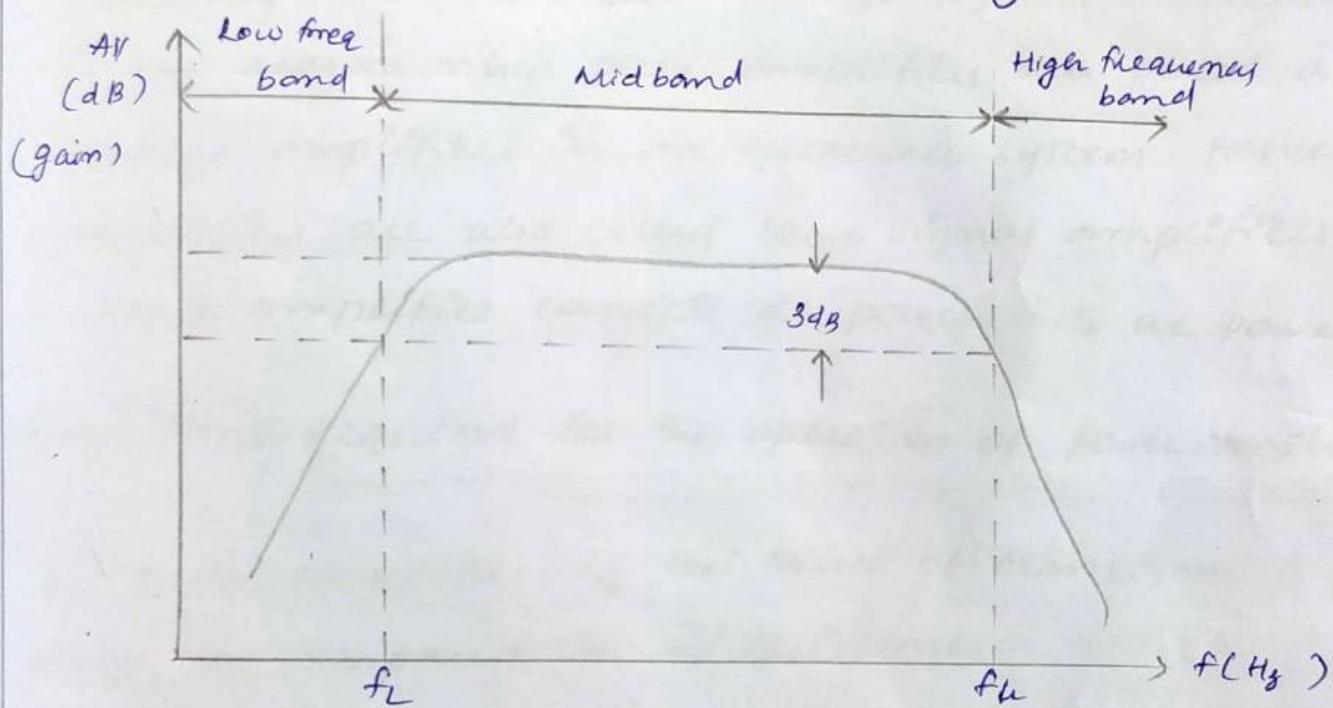
$$V_o = V_{cc} - I_C R_C$$

Frequency Response of amplifier

The essential purpose of an amplifier is to accept an input signal and provide an amplified version of that signal as an output. Every amplifier has a frequency response curve associated with it and it provides a information about the performance of the amplifier at various frequencies. The frequency response of the amplifier is a graph of frequency (x-axis) and gain (Y-axis)

Ktu Q bank No real amplifier has equal gain at all frequencies.

For an amplifier there will be mid band gain, that is the gain of the amplifier in the middle of its normal operating frequency range. In this range, the gain will be normally constant. The frequencies at which the gain falls by 3dB from the mid-band gain are termed as lower cutoff frequency (f_L) and upper cutoff frequency (f_H).



In ~~an~~ amplifiers, coupling capacitors or transformers are used to pass the signal from one stage to another. The presence of these coupling capacitors reduces the gain at low frequencies. At low frequencies, capacitive impedance increases as it is inversely proportional to frequency of the signal. ($X_C = \frac{1}{2\pi f_C}$). This gain is also reduced at high frequencies due to the presence of internal capacitances such as stray capacitance.

These capacitances are parasitic capacitances potentially formed at transistor junctions. The gain will be constant over a mid frequency range.

$$\text{Band width } BW = f_R - f_L$$