Timing diagram of 8085

Instruction cycle

- Instruction: A command given to the microprocessor to perform an operation
- Program : A set of instructions given in a sequential manner to perform a particular task

- The time required to execute an instruction is called instruction cycle.
- The CPU fetches one instruction from memory at a time & executes it.
- Instruction cycle = Fetch cycle + Execute cycle

Fetch Cycle : The steps taken by CPU to fetch the opcode from the memory

The time taken for fetch cycle is fixed.

Execute Cycle : The steps taken by CPU to fetch data & to perform the operation specified in the instruction

The time taken for execute cycle is variable which depends on the type of instruction ,i.e. 3 –byte , 2-byte & 1-byte instruction.

Machine cycle

The time required by the micro processor to complete the operation of accessing memory or I/O device .

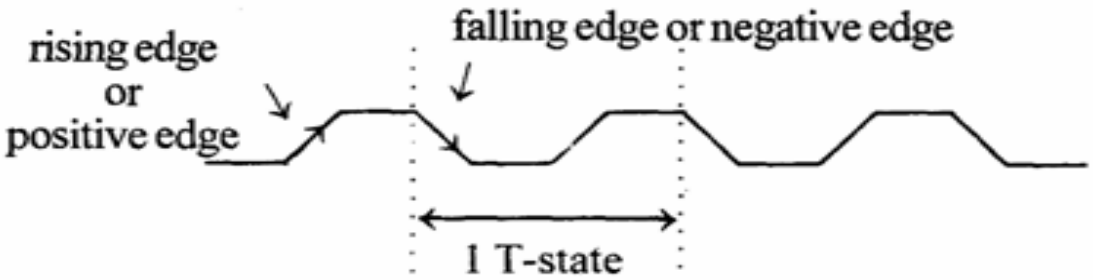
Operations like :

- Opcode fetch
- Memory read
- Memory write
- I/O read
- I/O write

T - states

- Microprocessor performs an operation in specific clock cycles.
- One T-state is equal to the time period of the internal clock signal of the processor. A portion of an operation carried out in one system clock period is called as T-state.
- The time taken by the processor to execute a machine cycle is expressed in T-states.

Note : *Time period, T = 1/f ; where f = Internal clock frequency*



Machine cycles of 8085

The 8085 microprocessor has 5 basic machine cycles.

They are

1. Opcode fetch cycle (4T)
2. Memory read cycle (3 T)
3. Memory write cycle (3 T)
4. I/O read cycle (3 T)
5. I/O write cycle (3 T)

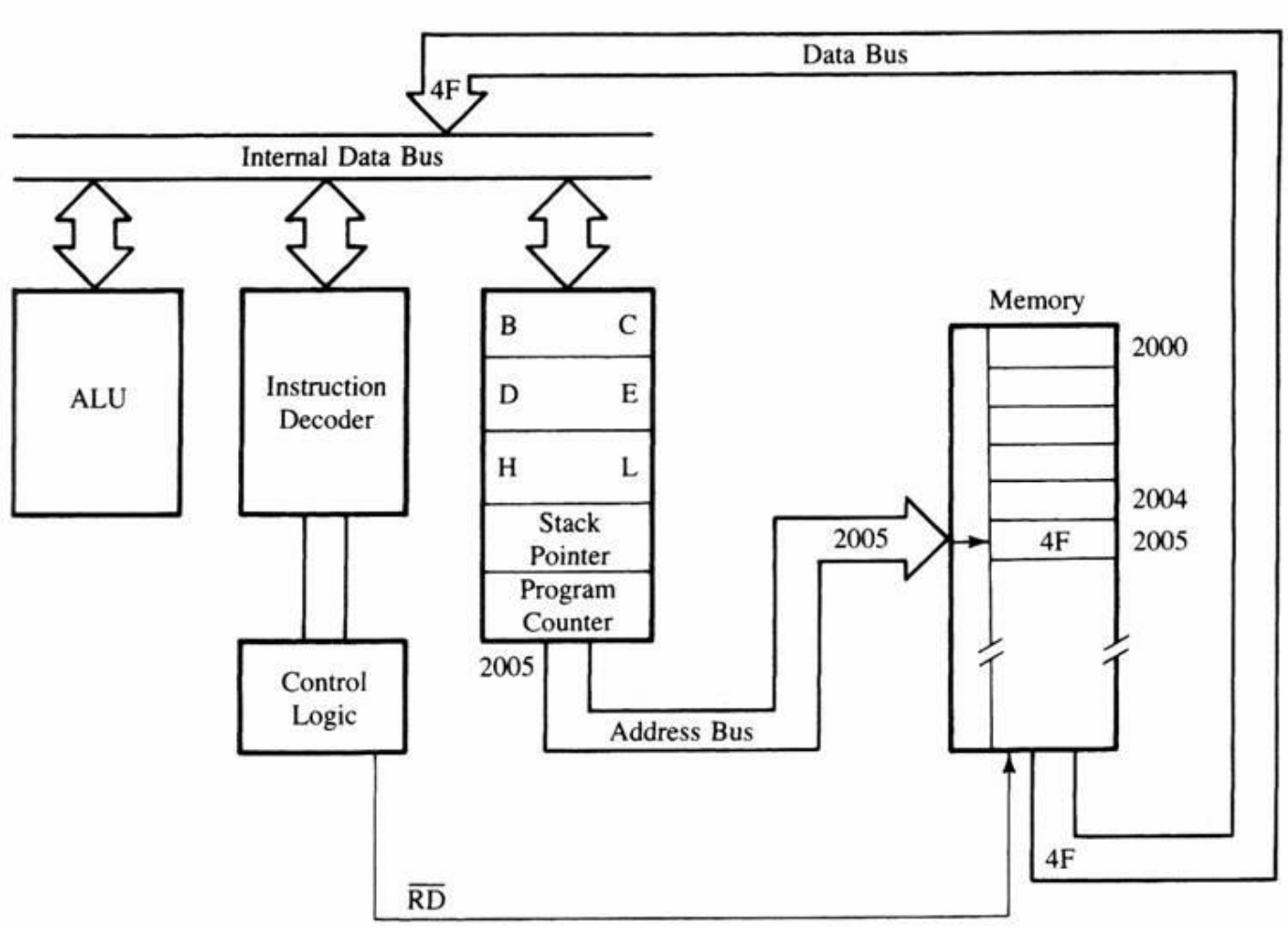
Timing diagram

- Timing Diagram is a graphical representation.
- It represents the execution time taken by each instruction in a graphical format.
- The execution time is represented in T-states.

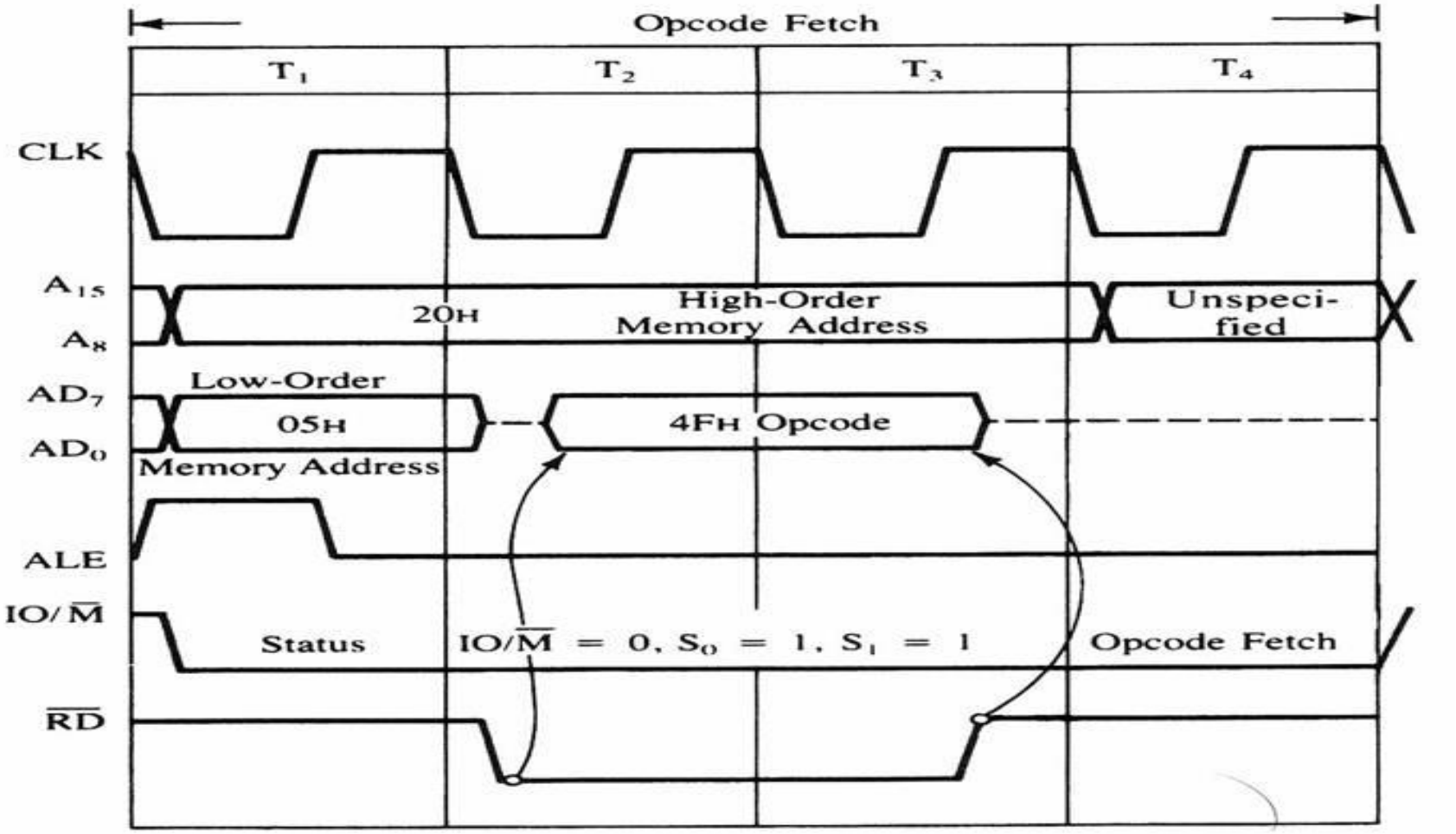
Status signals

S_1	S_0	Operation
0	0	Halt
0	1	Write
1	0	Read
1	1	Opcode Fetch

MOV C, A (opcode 4FH = 0100 1111)

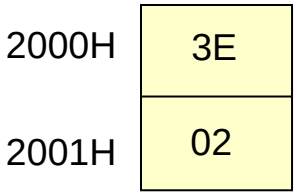


Timing diagram for opcode fetch machine cycle(MOV C,A)



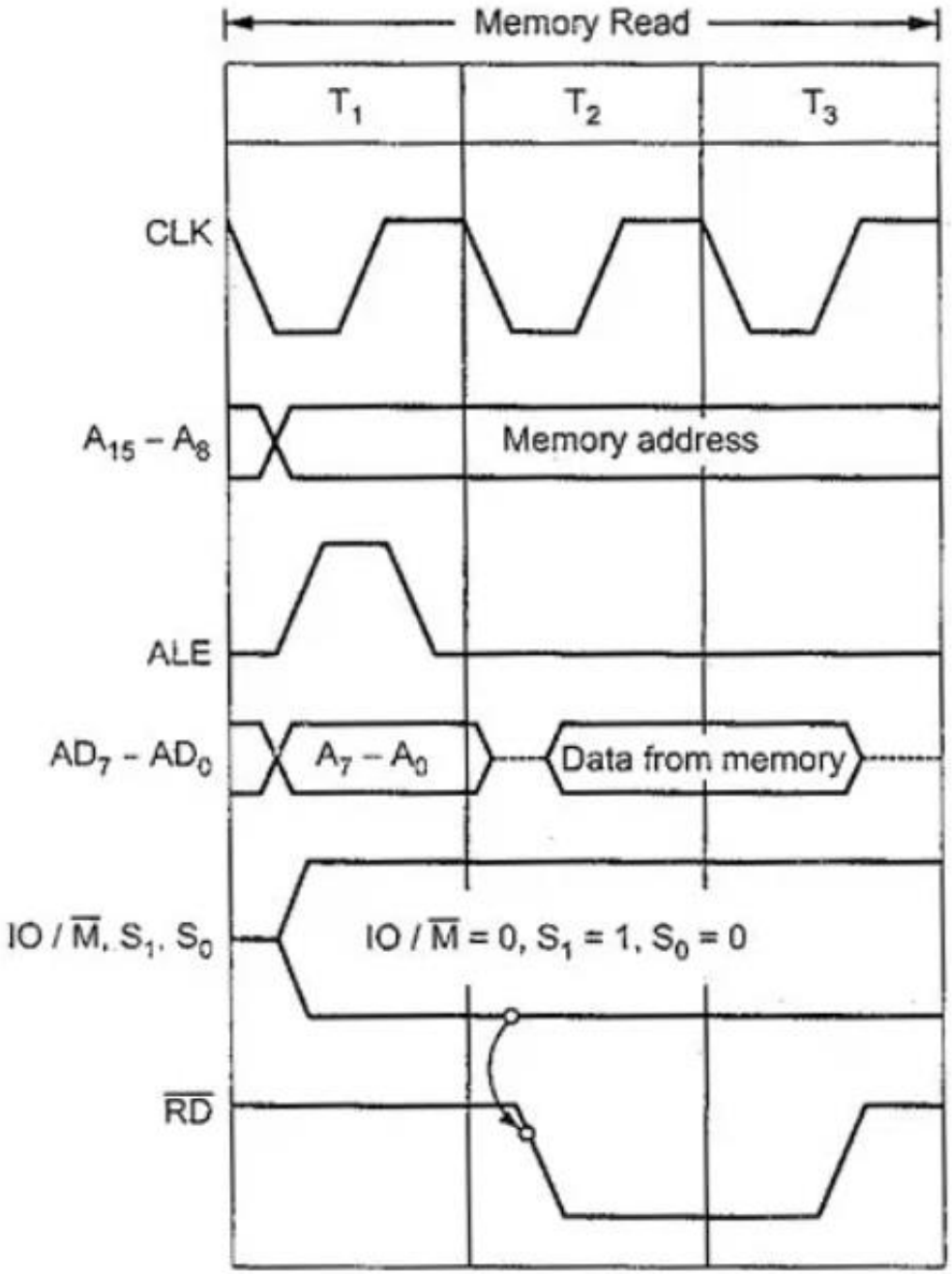
Memory read machine cycle

MVI A, 02 H



- The first byte 3EH represents the opcode for loading a byte into the accumulator (MVI A), the second byte is the data to be loaded.
- The 8085 needs to read these two bytes from memory before it can execute the instruction. Therefore, it will need at least two machine cycles.
  - The first machine cycle is the opcode fetch.
  - The second machine cycle is the Memory Read Cycle.

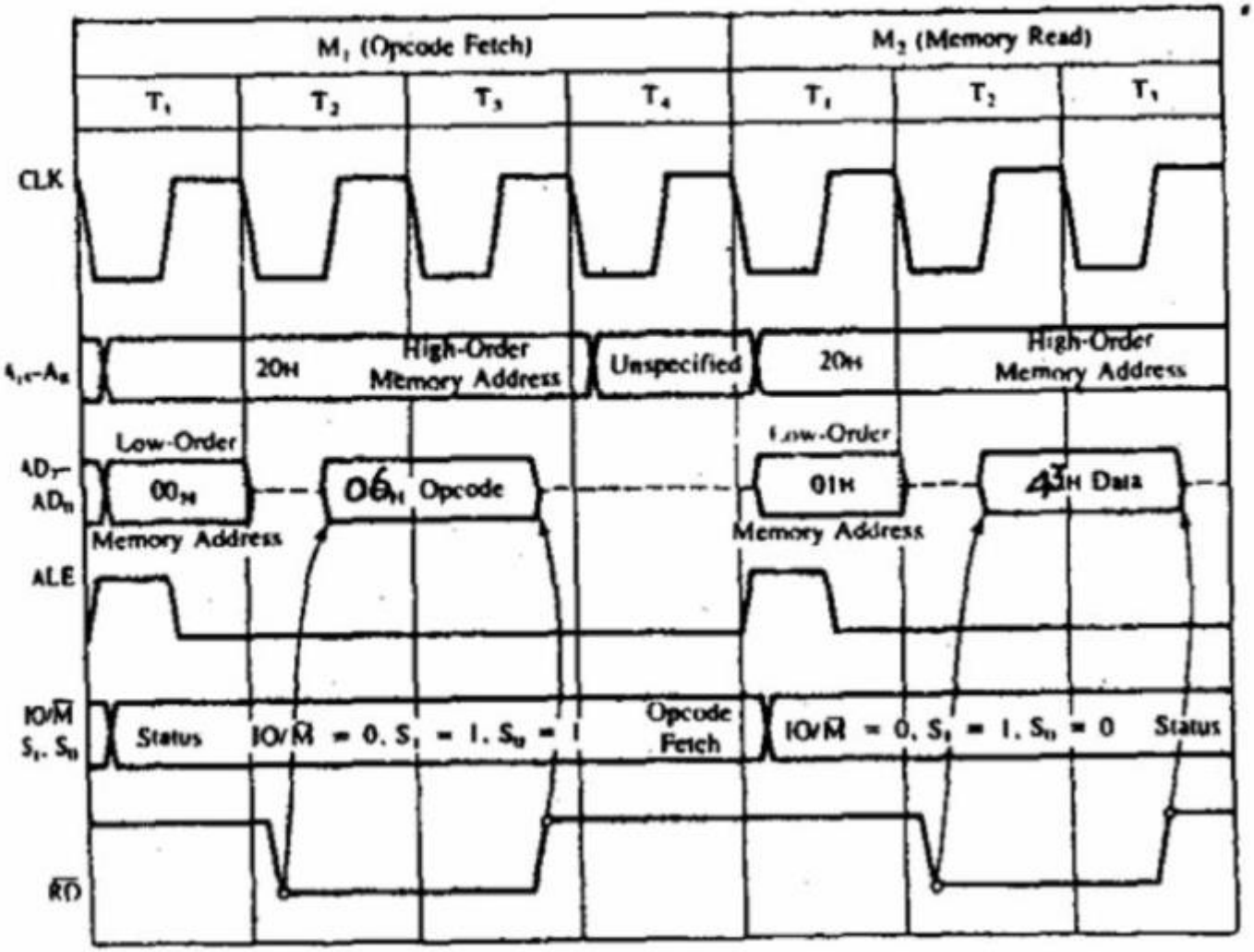
Timing diagram for memory read machine cycle



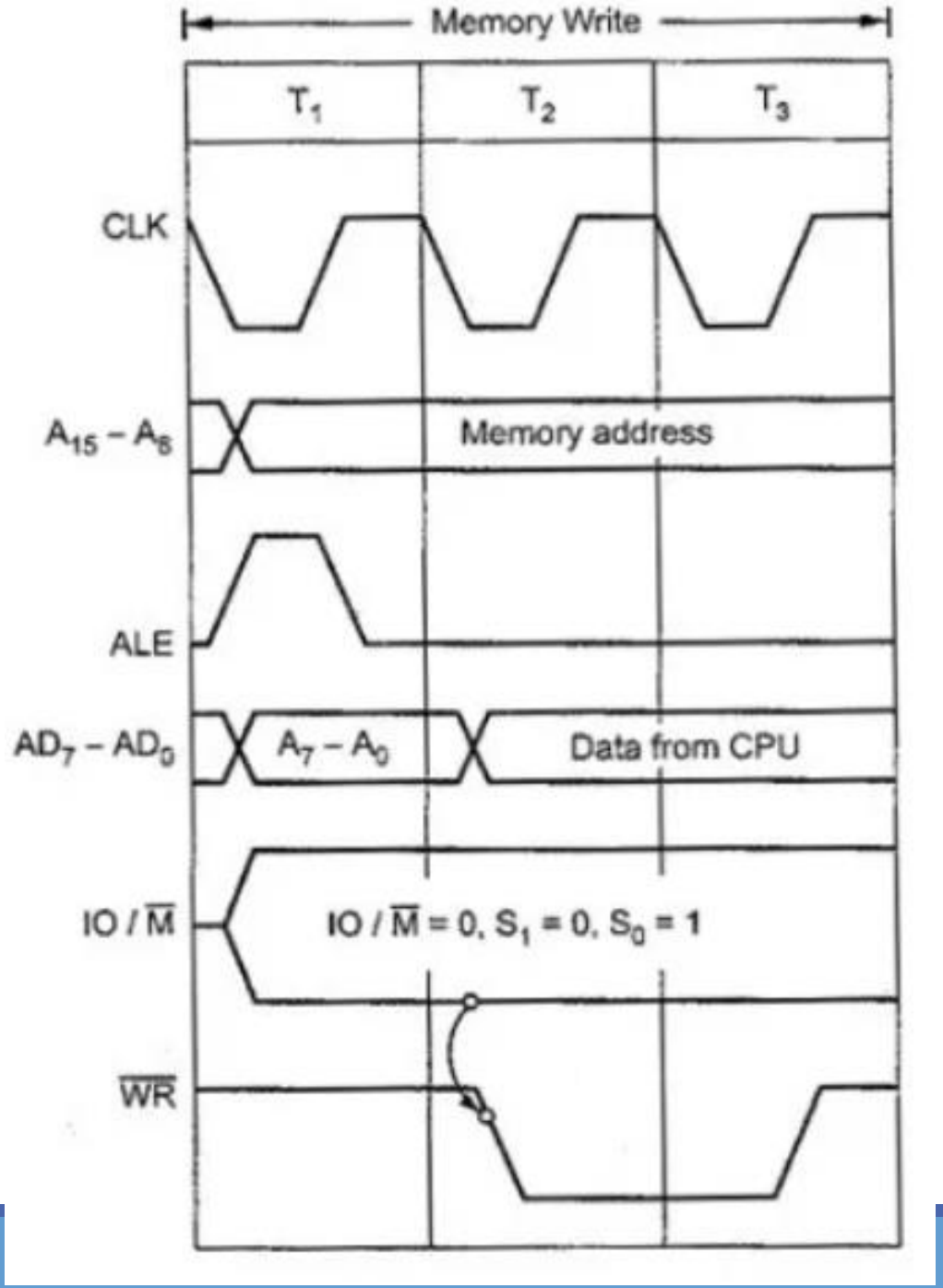
Timing diagram for MVI B, 43H.

Fetching the Opcode 06H from the memory 2000H. (OF machine cycle)
Read (move) the data 43H from memory 2001H. (memory read)

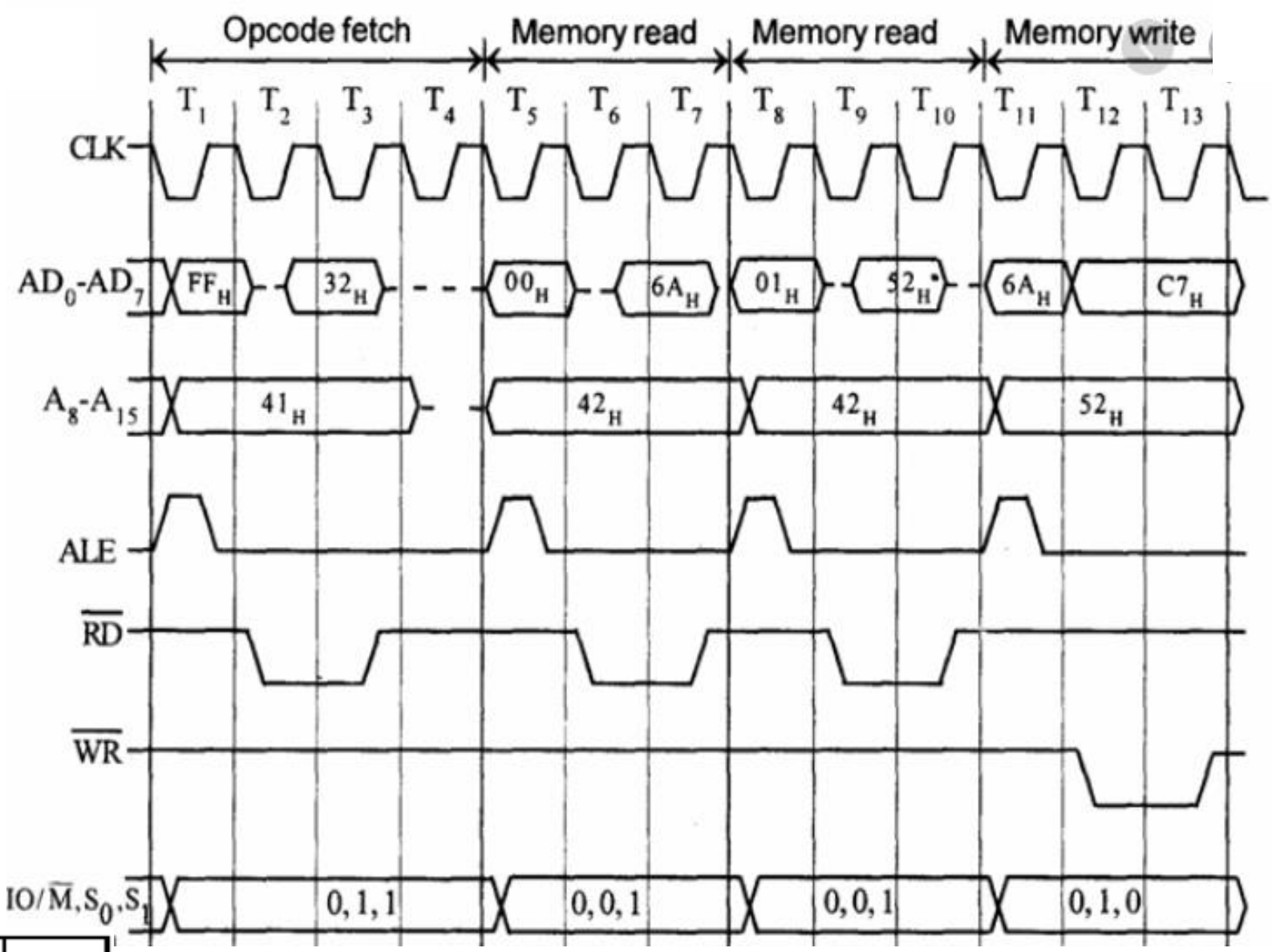
Address	Mnemonics	Opcode
2000	MVI B, 43H	06H
2001		43H



Timing diagram for memory write machine cycle

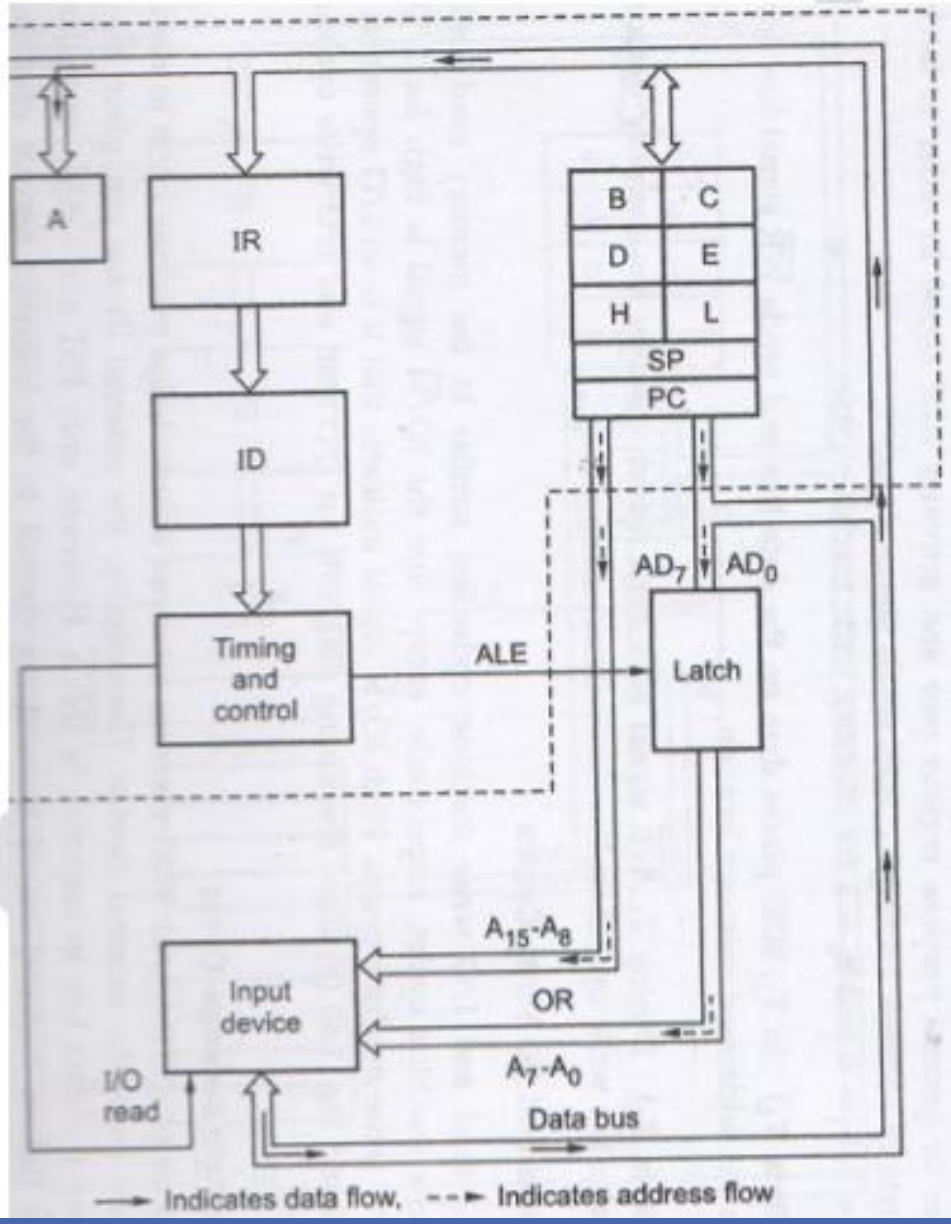


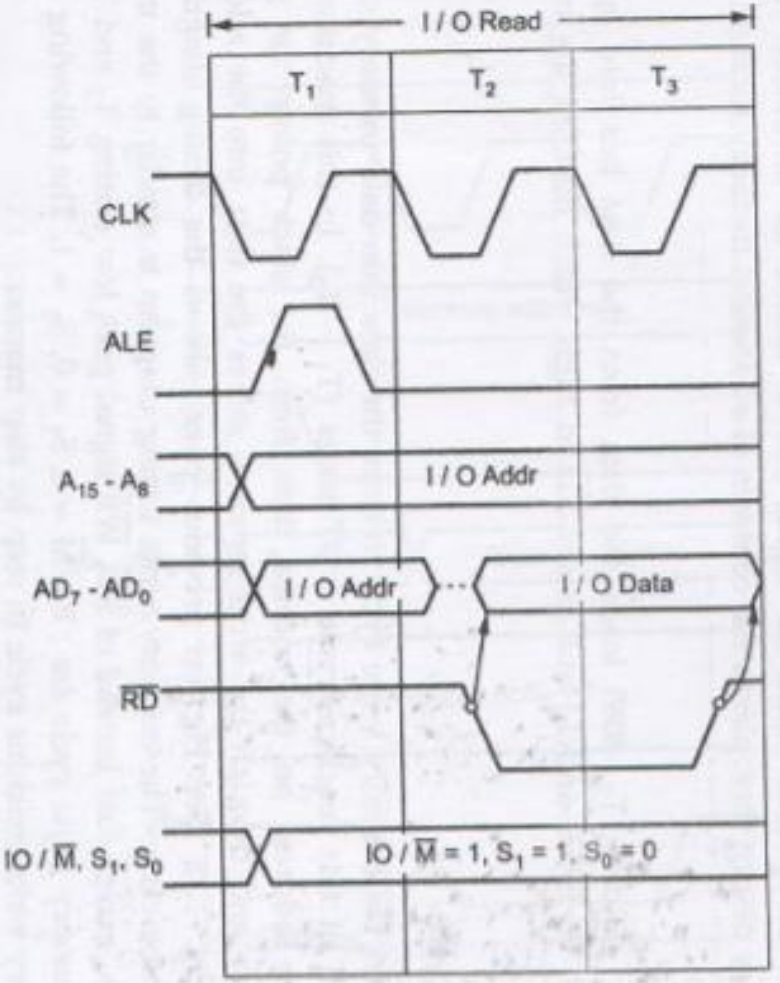
Timing diagram for STA 526A H



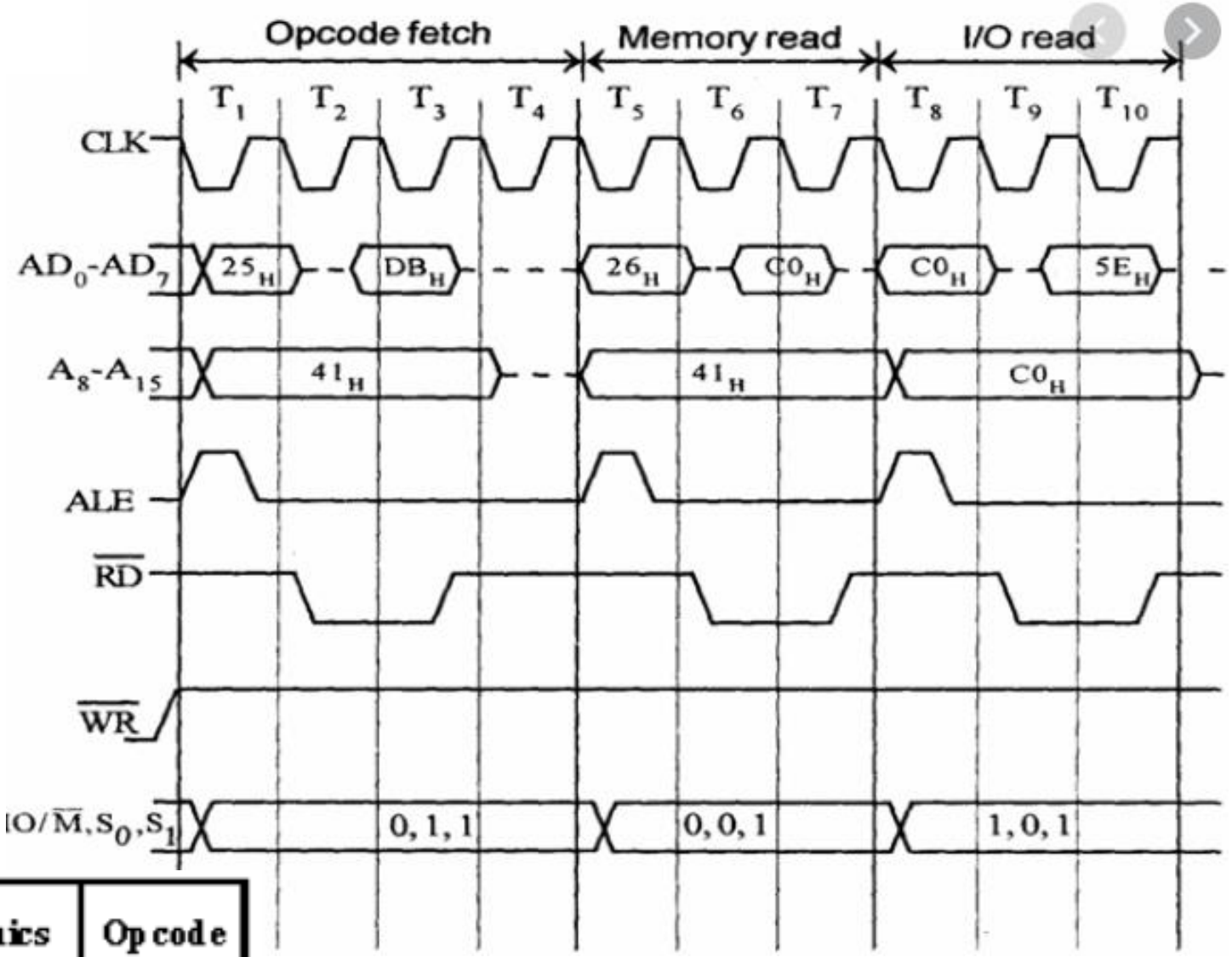
Address	Mnemonics	Opcode
41FF	STA 526AH	32H
4200		6AH
4201		52H

Timing diagram for IO read machine cycle





Timing diagram for IN C0 H



Address	Mnemonics	Opcode
4125	IN C0H	DBH
4126		C0H

Timing diagram for IO write machine cycle