Jiale Liu
liujial@oregonstate.edu

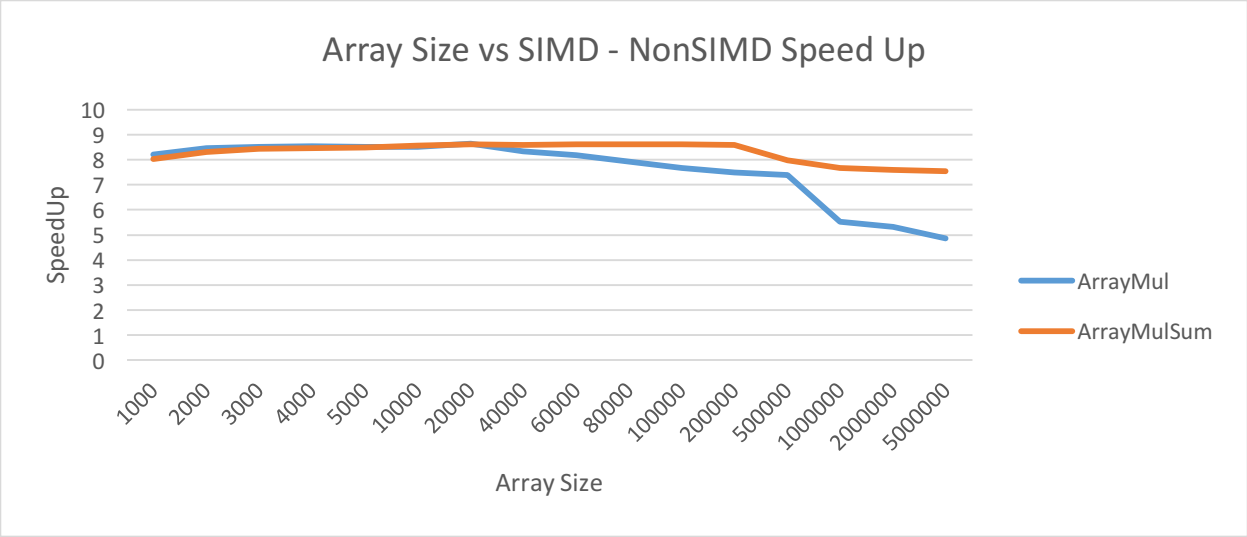
Project#4: Vectorized Array Multiplication and Reduction using SSE

1. What machine you ran this on

   The code was ran on Flip1.

2. Show the table and graph

ArraySize	ArrayMulSpeedUp	ArrayMulSumSpeedUp
1,000	8.21	8.02
2,000	8.46	8.32
3,000	8.52	8.43
4,000	8.53	8.46
5,000	8.52	8.49
10,000	8.51	8.57
20,000	8.61	8.61
40,000	8.34	8.6
60,000	8.19	8.61
80,000	7.93	8.61
100,000	7.68	8.61
200,000	7.48	8.6
500,000	7.39	7.98
1,000,000	5.52	7.67
2,000,000	5.31	7.59
5,000,000	4.85	7.54



3. What patterns are you seeing in the speedups?

   For both array-multiply and array-multiply-reduction experiments, the speed-up increases and reaches at 8.61 when the array size increases. When the array size is more than 20,000, the speed up for both experiments start to decrease. The speed up of the array-multiply drops faster than the speed up of the array-multiply-reduction experiment.

4. Are they consistent across a variety of array sizes?

   For both the array-multiply and the array-multiply-reduction experiment, the speed-up rises and reaches the top when the array size is 20,000, then it begins to drop.

   When the array size is more than 20,000, the speed up of the array-multiply drops faster than the speed up of the array-multiply-reduction.

5. Why or why not, do you think?

   When the array size is small, the SIMD is so fast and the speed up can reaches more than 8.

   When the array size is getting larger, there will be more overhead and the possibility of cache missing will also increase. So the speed up will drop when the array size is too large.

6. Knowing that SSE SIMD is 4-floats-at-a-time, why could you get a speed-up of < 4.0 or > 4.0 in the array-multiplication?

   The speed up can reach at 8.61 when the array size is 20,000. The speed up starts to drop and reaches 4.85 when the array size is 5,000,000.

   One of the reasons that the speed-up is more than 4.0 is that the none SIMD version is not well optimized by complier. But the SIMD version is using assembly language and all the potential speedup are investigated.

7. Knowing that SSE SIMD is 4-floats-at-a-time, why could you get a speed-up of < 4.0 or > 4.0 in the array-multiplication-reduction?

   The speed up can reach at 8.61 when the array size is 20,000. The speed up starts to drop and reaches 7.54 when the array size is 5,000,000.

   One of the reasons that the speed-up is more than 4.0 is that the none SIMD version is not well optimized by complier. But the SIMD version is using assembly language and all the potential speedup are investigated. Especially the ‘adding to the xmm register’ is very efficient, so the speed up drops slower than the array-multiplication experiment.