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August 2016



FDMS86180

N-Channel Shielded Gate PowerTrench® MOSFET

100 V, 151 A, 3.2 mΩ

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 3.2 mΩ at $V_{GS} = 10$ V, $I_D = 67$ A
- Max $r_{DS(on)}$ = 7.9 mΩ at $V_{GS} = 6$ V, $I_D = 33$ A
- 50% Lower Qrr than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

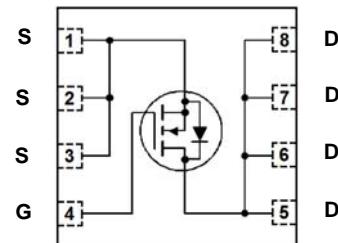
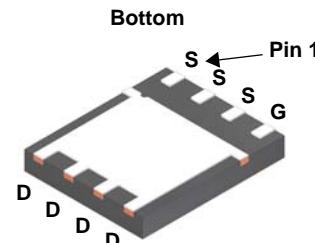
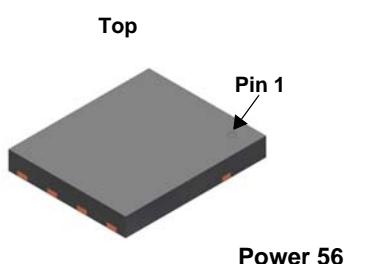


General Description

This N-Channel MV MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Applications

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous $T_C = 25$ °C	151	A
	-Continuous $T_C = 100$ °C	95	
	-Continuous $T_A = 25$ °C (Note 1a)	21	
	-Pulsed (Note 4)	775	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	mJ
P_D	Power Dissipation $T_C = 25$ °C	138	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	2.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta,JC}$	Thermal Resistance, Junction to Case	0.9	°C/W
$R_{\theta,JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	45	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86180	FDMS86180	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100			V
$\Delta \text{BV}_{\text{DSS}} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		73		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA

On Characteristics

$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 370 \mu\text{A}$	2.0	3.2	4.0	V
$\Delta V_{GS(\text{th})} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 370 \mu\text{A}$, referenced to 25°C		-8		$\text{mV}/^\circ\text{C}$
$r_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 67 \text{ A}$		2.4	3.2	$\text{m}\Omega$
		$V_{GS} = 6 \text{ V}, I_D = 33 \text{ A}$		3.8	7.9	
		$V_{GS} = 10 \text{ V}, I_D = 67 \text{ A}, T_J = 125^\circ\text{C}$		4.0	5.4	
g_{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_D = 67 \text{ A}$		144		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		4439	6215	pF
C_{oss}	Output Capacitance			2663	3730	pF
C_{rss}	Reverse Transfer Capacitance			24	55	pF
R_g	Gate Resistance		0.1	0.8	1.6	Ω

Switching Characteristics

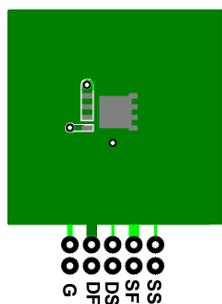
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, I_D = 67 \text{ A}, V_{GS} = 10 \text{ V}, R_{\text{GEN}} = 6 \Omega$		24	39	ns
t_r	Rise Time			12	22	ns
$t_{d(off)}$	Turn-Off Delay Time			30	48	ns
t_f	Fall Time			7	14	ns
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V} \text{ to } 10 \text{ V}$		60	84	nC
Q_g	Total Gate Charge		$V_{GS} = 0 \text{ V} \text{ to } 6 \text{ V}$	38	54	nC
Q_{gs}	Gate to Source Charge		$I_D = 67 \text{ A}$	20		nC
Q_{gd}	Gate to Drain "Miller" Charge			12		nC
Q_{oss}	Output Charge	$V_{DD} = 50 \text{ V}, V_{GS} = 0 \text{ V}$		175		nC

Drain-Source Diode Characteristics

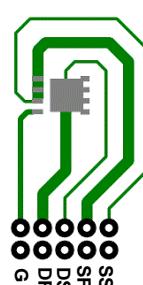
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.1 \text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0 \text{ V}, I_S = 67 \text{ A}$ (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 33 \text{ A}, di/dt = 300 \text{ A}/\mu\text{s}$		44	71	ns
Q_{rr}	Reverse Recovery Charge			109	207	nC
t_{rr}	Reverse Recovery Time	$I_F = 33 \text{ A}, di/dt = 1000 \text{ A}/\mu\text{s}$		33	53	ns
Q_{rr}	Reverse Recovery Charge			235	376	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a) 45 °C/W when mounted on a 1 in² pad of 2 oz copper



b) 115 °C/W when mounted on a minimum pad of 2 oz copper.

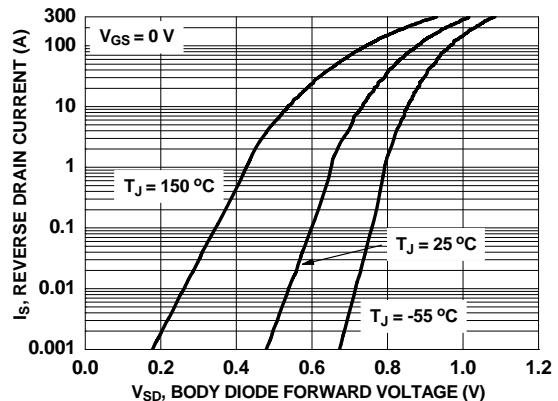
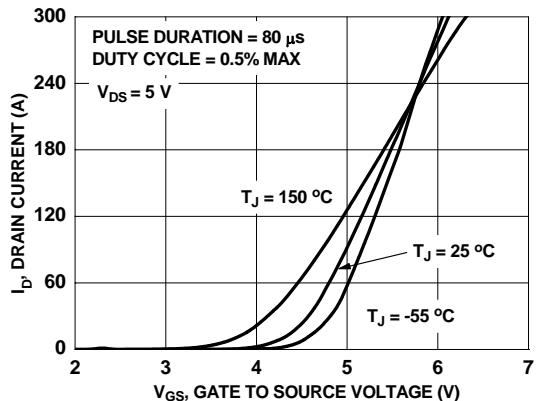
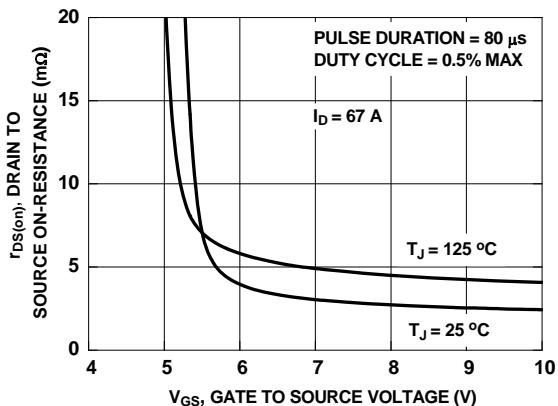
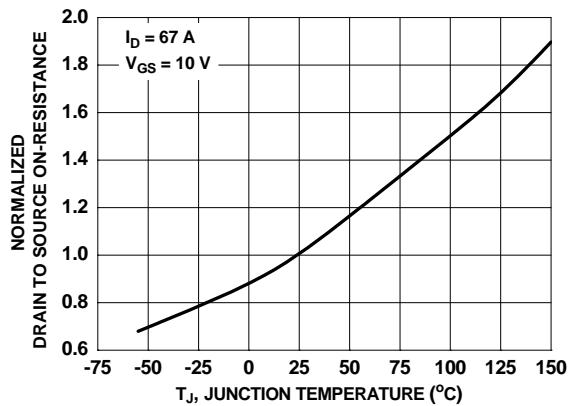
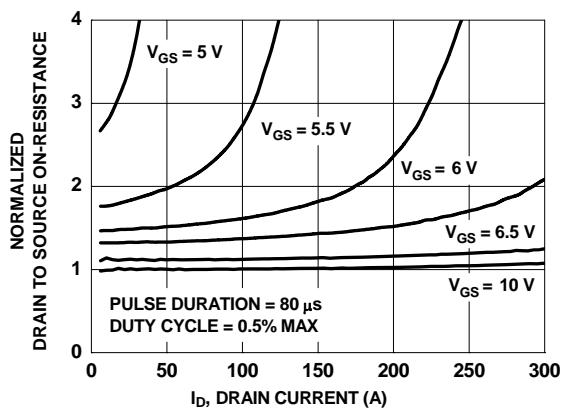
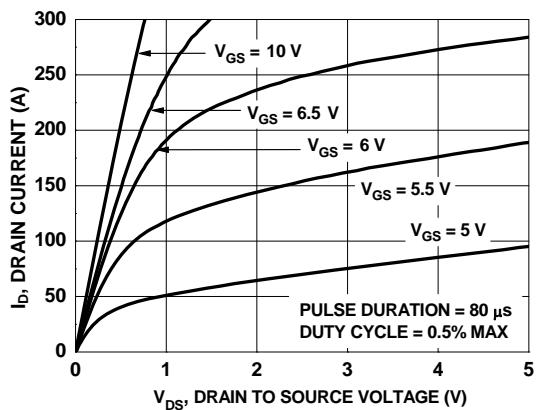
2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. E_{AS} of 486 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: L = 3 mH, $I_{AS} = 18 \text{ A}$, $V_{DD} = 100 \text{ V}$, $V_{GS} = 10 \text{ V}$. 100% test at L = 0.1 mH, $I_{AS} = 58 \text{ A}$.

4. Pulsed Id please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.



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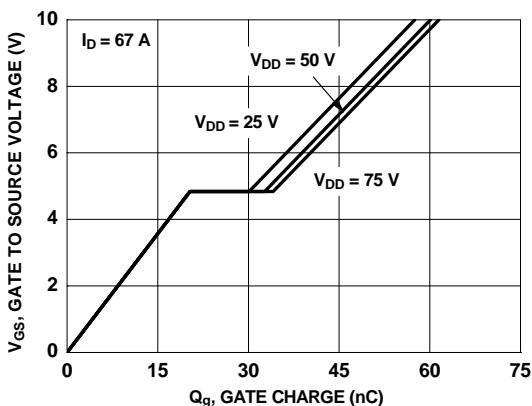


Figure 7. Gate Charge Characteristics

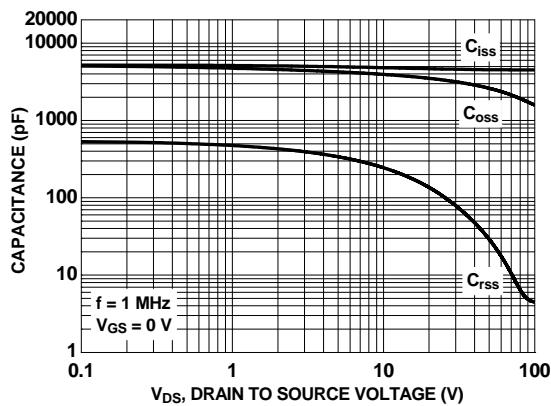


Figure 8. Capacitance vs. Drain to Source Voltage

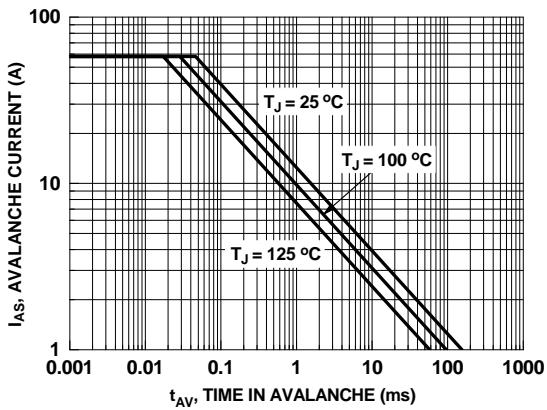


Figure 9. Unclamped Inductive Switching Capability

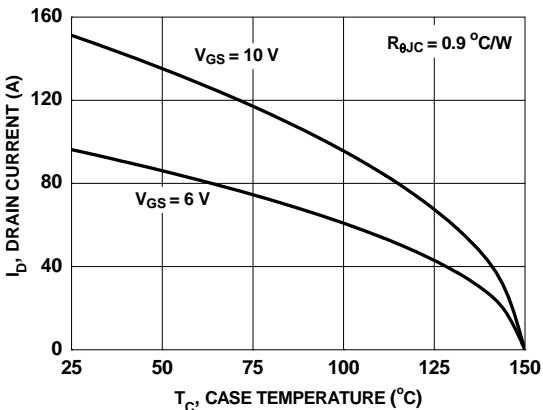


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

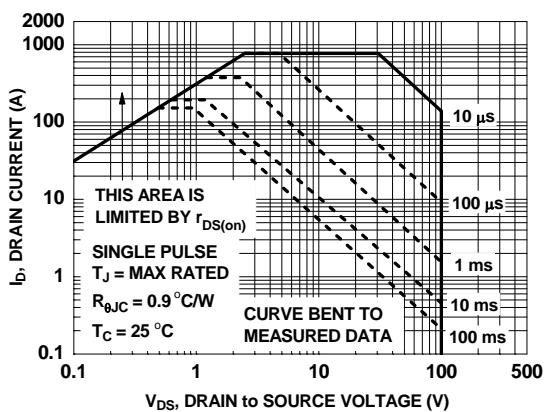


Figure 11. Forward Bias Safe Operating Area

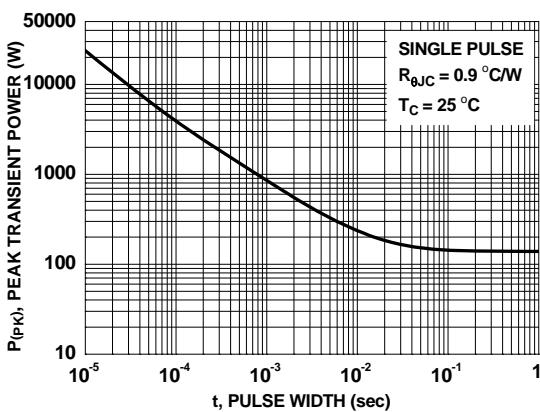


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

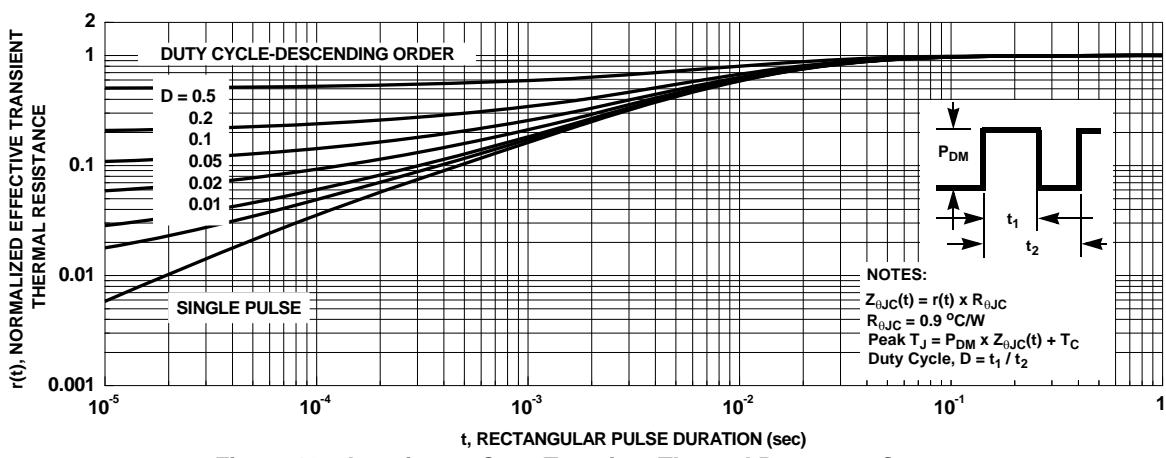
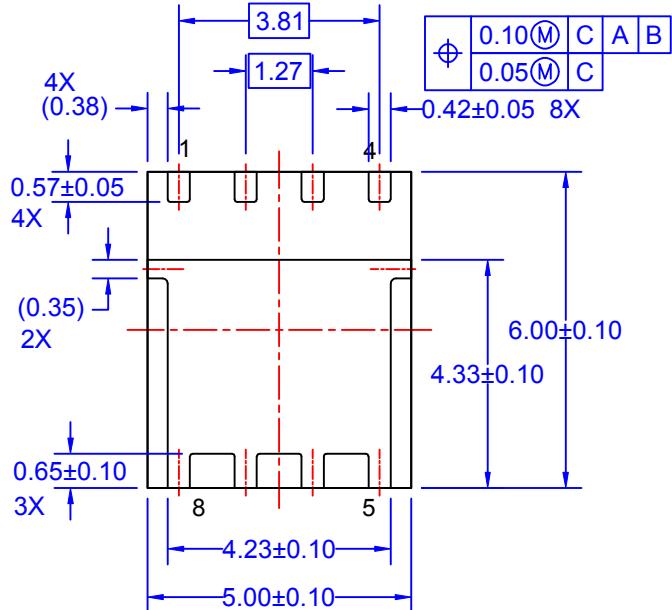
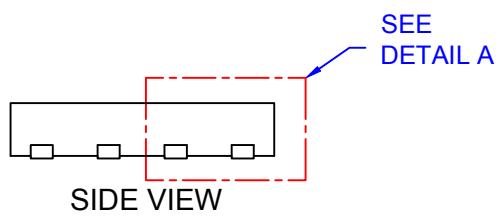
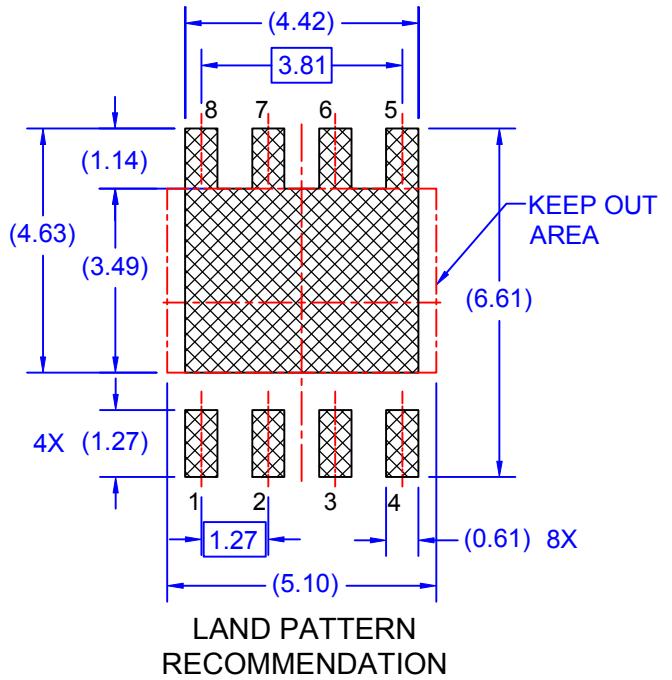
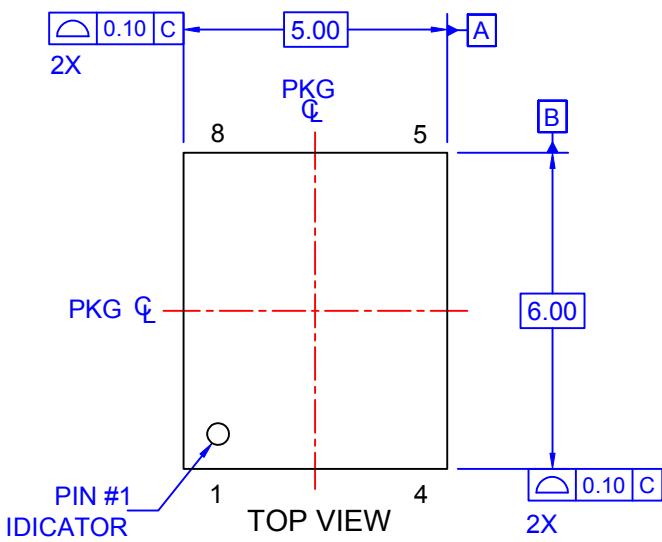


Figure 13. Junction-to-Case Transient Thermal Response Curve



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- PACKAGE STANDARD REFERENCE:
JEDEC MO-240, ISSUE A, VAR. AA,
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- DRAWING FILE NAME: PQFN08TREV1.



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