
STM32
CubeMX

1. Description

1.1. Project

Project Name	WordClock_Rev_3
Board Name	custom
Generated with:	STM32CubeMX 6.11.0
Date	03/26/2024

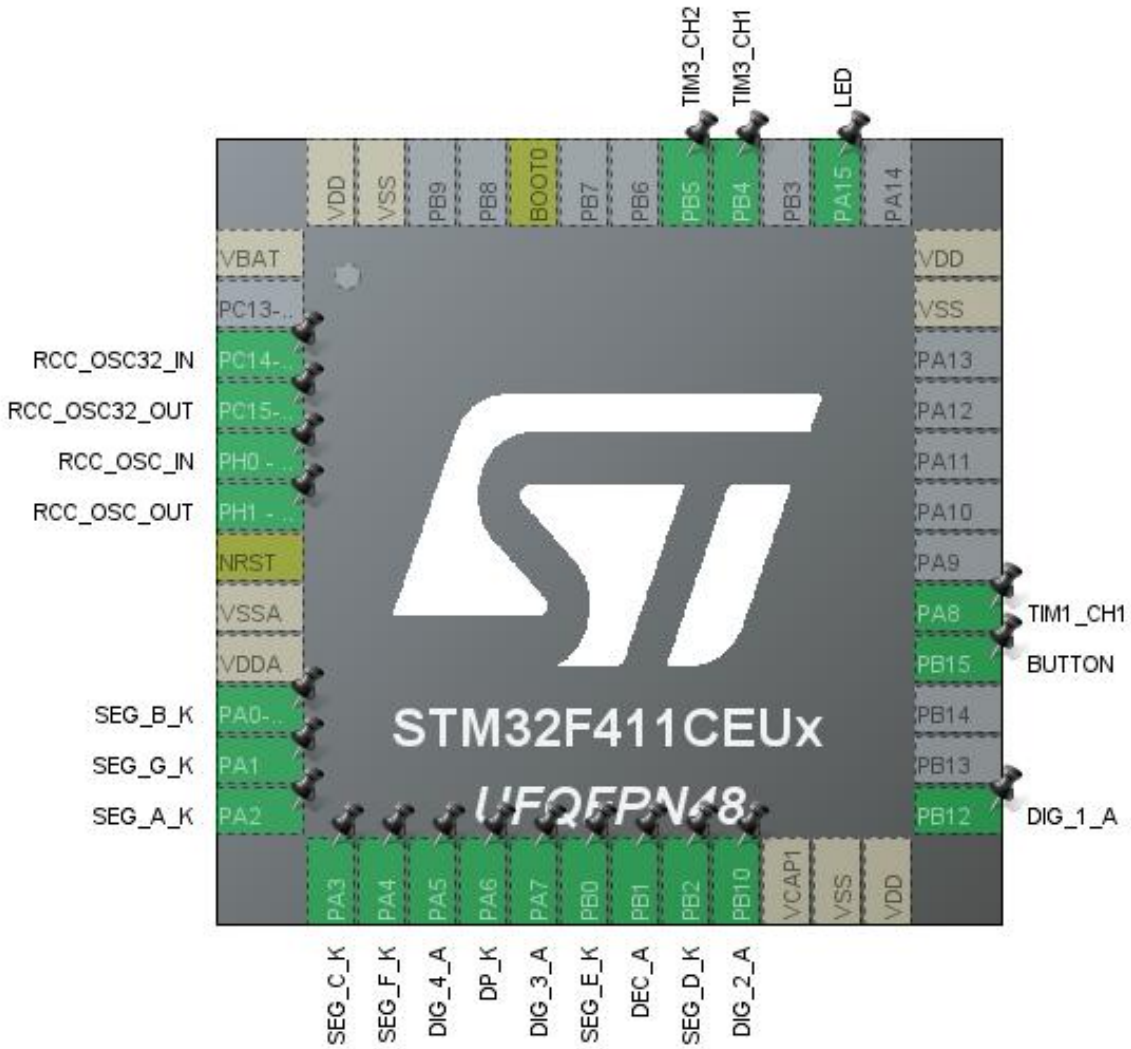
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F411
MCU name	STM32F411CEUx
MCU Package	UFQFPN48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration

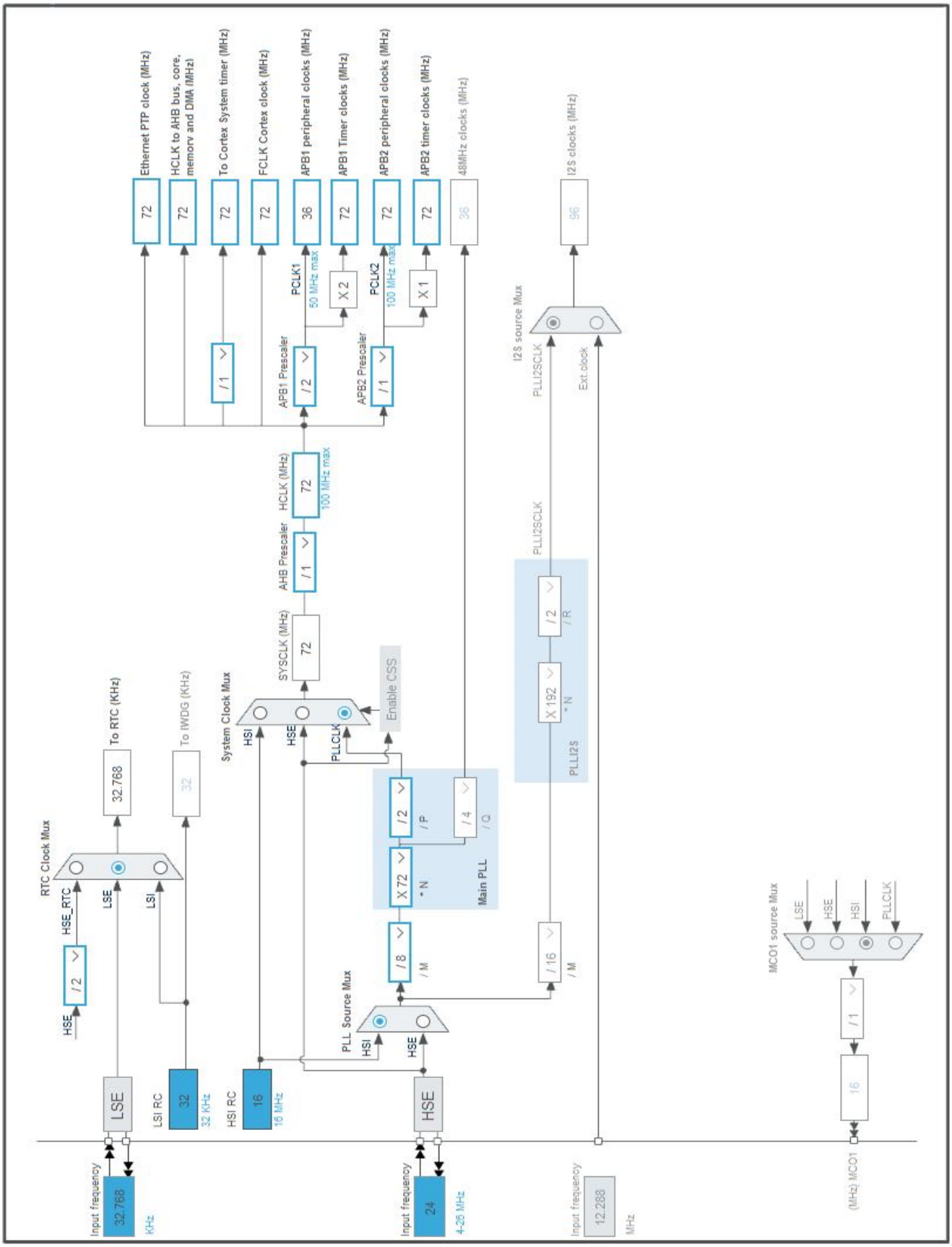


3. Pins Configuration

Pin Number UFQFPN48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PH0 - OSC_IN	I/O	RCC_OSC_IN	
6	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP *	I/O	GPIO_Output	SEG_B_K
11	PA1 *	I/O	GPIO_Output	SEG_G_K
12	PA2 *	I/O	GPIO_Output	SEG_A_K
13	PA3 *	I/O	GPIO_Output	SEG_C_K
14	PA4 *	I/O	GPIO_Output	SEG_F_K
15	PA5 *	I/O	GPIO_Output	DIG_4_A
16	PA6 *	I/O	GPIO_Output	DP_K
17	PA7 *	I/O	GPIO_Output	DIG_3_A
18	PB0 *	I/O	GPIO_Output	SEG_E_K
19	PB1 *	I/O	GPIO_Output	DEC_A
20	PB2 *	I/O	GPIO_Output	SEG_D_K
21	PB10 *	I/O	GPIO_Output	DIG_2_A
22	VCAP1	Power		
23	VSS	Power		
24	VDD	Power		
25	PB12 *	I/O	GPIO_Output	DIG_1_A
28	PB15 *	I/O	GPIO_Input	BUTTON
29	PA8	I/O	TIM1_CH1	
35	VSS	Power		
36	VDD	Power		
38	PA15 *	I/O	GPIO_Output	LED
40	PB4	I/O	TIM3_CH1	
41	PB5	I/O	TIM3_CH2	
44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	WordClock_Rev_3
Project Folder	C:\Users\dsava\STM32CubeIDE\workspace_1.11.0\WordClock_Rev_3
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x10000
Minimum Stack Size	0x10000

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_TIM1_Init	TIM1
5	MX_RTC_Init	RTC
6	MX_TIM3_Init	TIM3

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F411
MCU	STM32F411CEUx
Datasheet	DS10314_Rev6

1.2. Parameter Selection

Temperature	25
Vdd	1.7

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

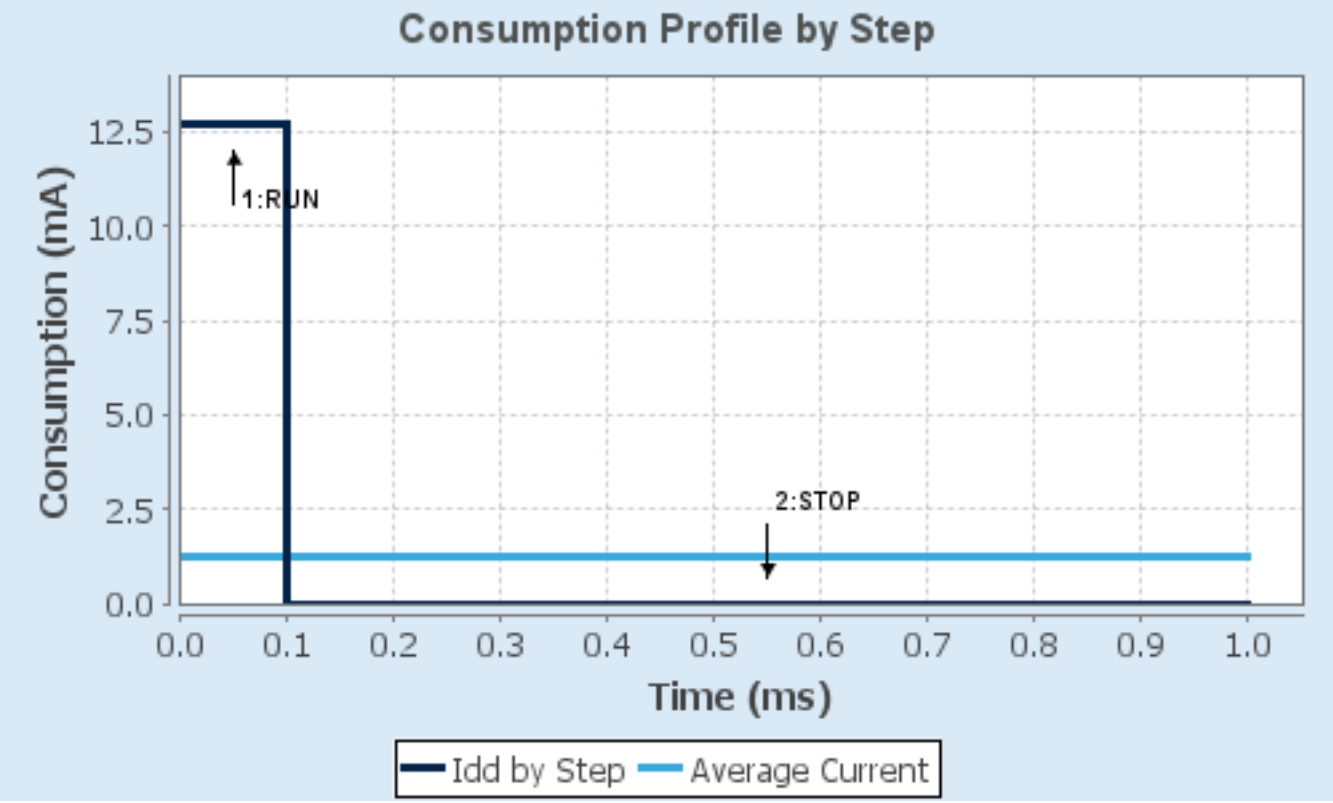
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	1.7	1.7
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	SRAM	n/a
CPU Frequency	100 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	12.7 mA	9 µA
Duration	0.1 ms	0.9 ms
DMIPS	125.0	0.0
Ta Max	104.31	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	1.28 mA
Battery Life	3 months, 19 days, 6 hours	Average DMIPS	125.0 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
12.5
10.0
7.5
5.0
2.5
0.0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Peripherals and Middlewares Configuration

2.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

2.1.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

2.2. RTC

mode: Activate Clock Source

mode: Activate Calendar

2.2.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	**Binary data format ***
Hours	**2 ***
Minutes	**20 ***
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	**Tuesday ***
Month	January
Date	**23 ***
Year	**24 ***

2.3. TIM1

Channel1: PWM Generation CH1

2.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**90-1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

2.4. TIM3

Combined Channels: Encoder Mode

2.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

*** User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PA0-WKUP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEG_B_K
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEG_G_K
	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEG_A_K
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEG_C_K
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEG_F_K
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIG_4_A
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DP_K
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIG_3_A
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEG_E_K
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DEC_A
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEG_D_K
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIG_2_A
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIG_1_A
	PB15	GPIO_Input	Input mode	**Pull-up ***	n/a	BUTTON
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED

3.2. DMA configuration

DMA request	Stream	Direction	Priority
TIM1_CH1	DMA2_Stream3	Memory To Peripheral	Low

TIM1_CH1: DMA2_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

3.3. NVIC configuration

3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	1	0
Pre-fetch fault, memory access fault	true	2	0
Undefined instruction or illegal state	true	3	0
System service call via SWI instruction	true	4	0
Debug monitor	true	5	0
Pendable request for system service	true	6	0
System tick timer	true	15	0
TIM1 break interrupt and TIM9 global interrupt	true	0	0
TIM1 update interrupt and TIM10 global interrupt	true	0	0
TIM1 trigger and commutation interrupts and TIM11 global interrupt	true	0	0
TIM1 capture compare interrupt	true	0	0
TIM3 global interrupt	true	9	0
DMA2 stream3 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
FPU global interrupt	unused		

3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM1 break interrupt and TIM9 global interrupt	false	true	true
TIM1 update interrupt and TIM10 global interrupt	false	true	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
TIM1 trigger and commutation interrupts and TIM11 global interrupt	false	true	true
TIM1 capture compare interrupt	false	true	true
TIM3 global interrupt	false	true	true
DMA2 stream3 global interrupt	false	true	true

*** User modified value**

4. System Views

4.1. Category view

4.1.1. Current

5. Docs & Resources

Type	Link