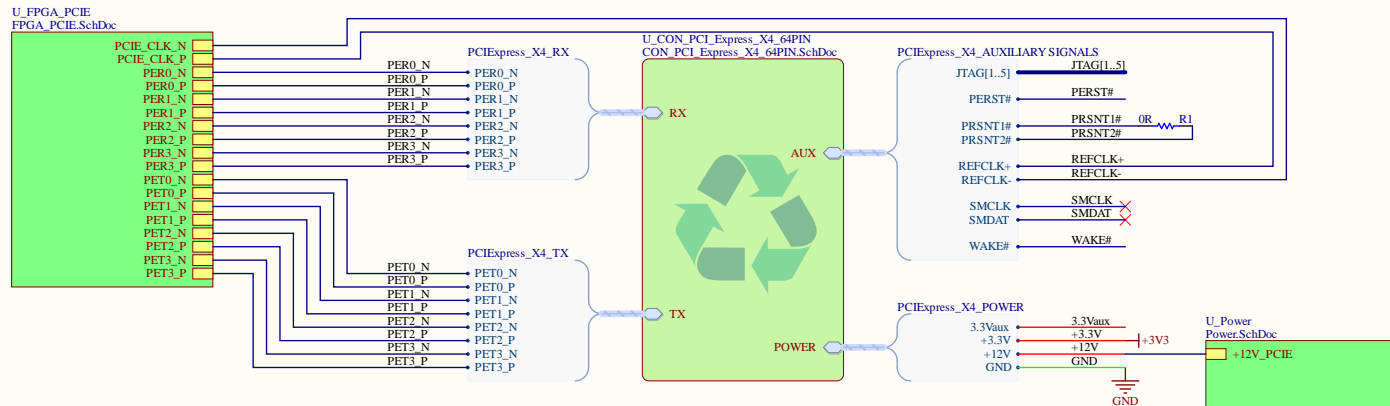
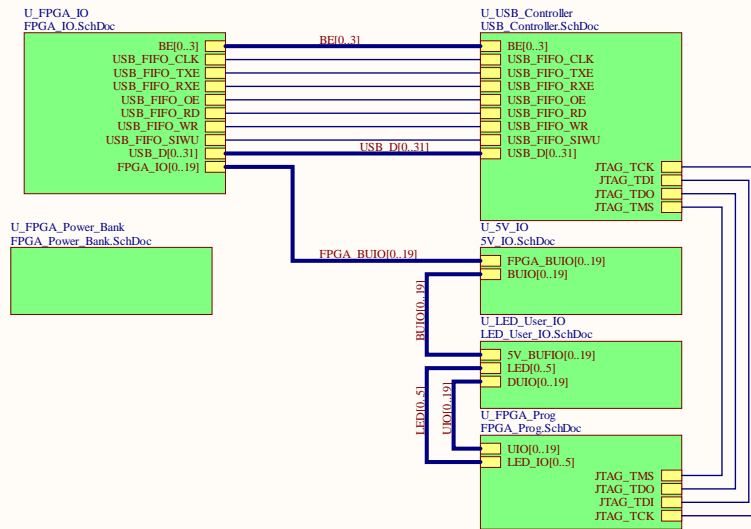
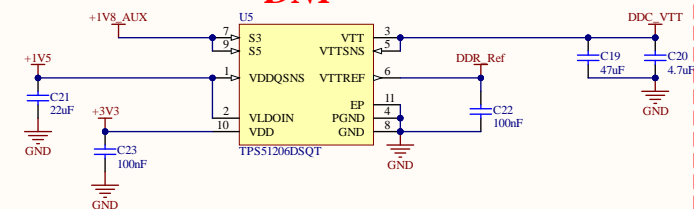
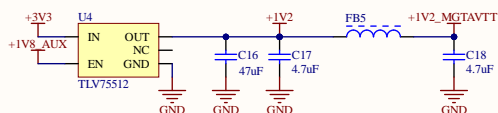
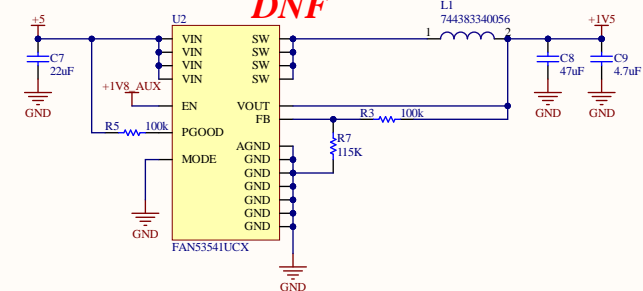


This version does not support DDR3. A DDR3 version of this board is planned





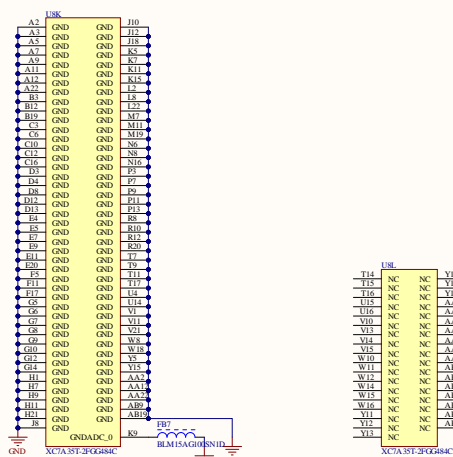
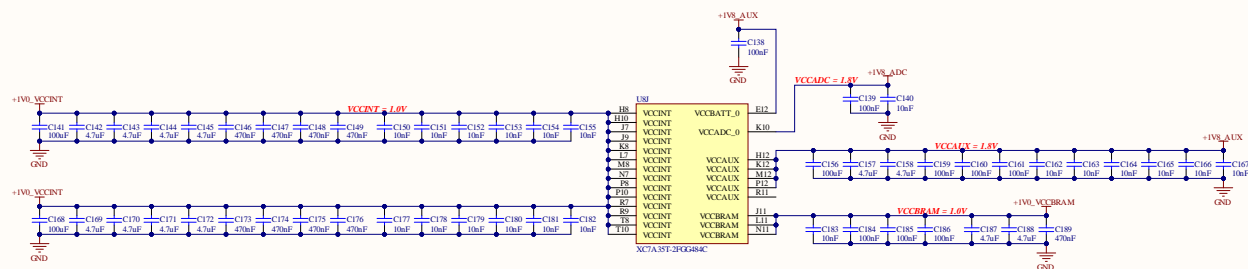
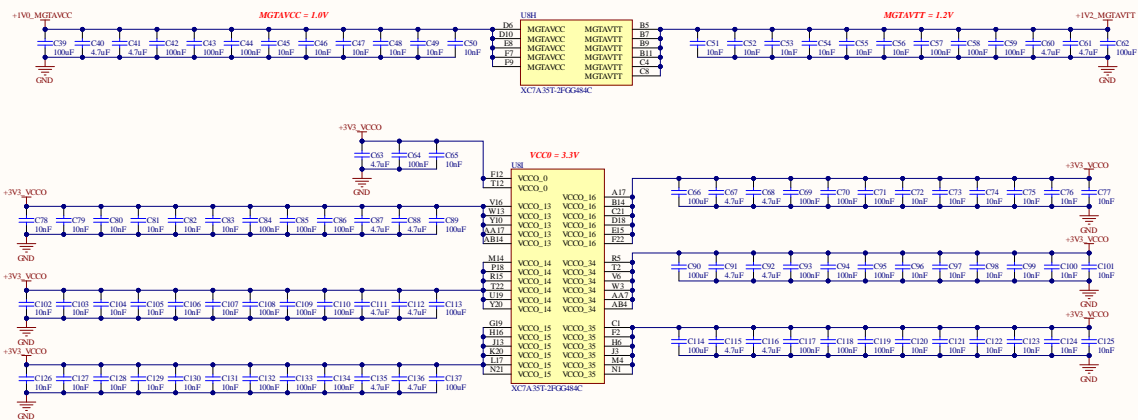
MGTAVCC = 1.0V
MGTAVTT = 1.2V
VCC0 = 3.3V or 1.5V
VCCINT = 1.0V
VCCADC = 1.8V
VCCAUX = 1.8V
VCCBRAM = 1.0V

Power On Sequence: VCCINT -> VCC_AUX -> 3.3V + 1.5V + 1.2V

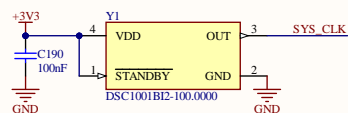
The Power Supply Controller

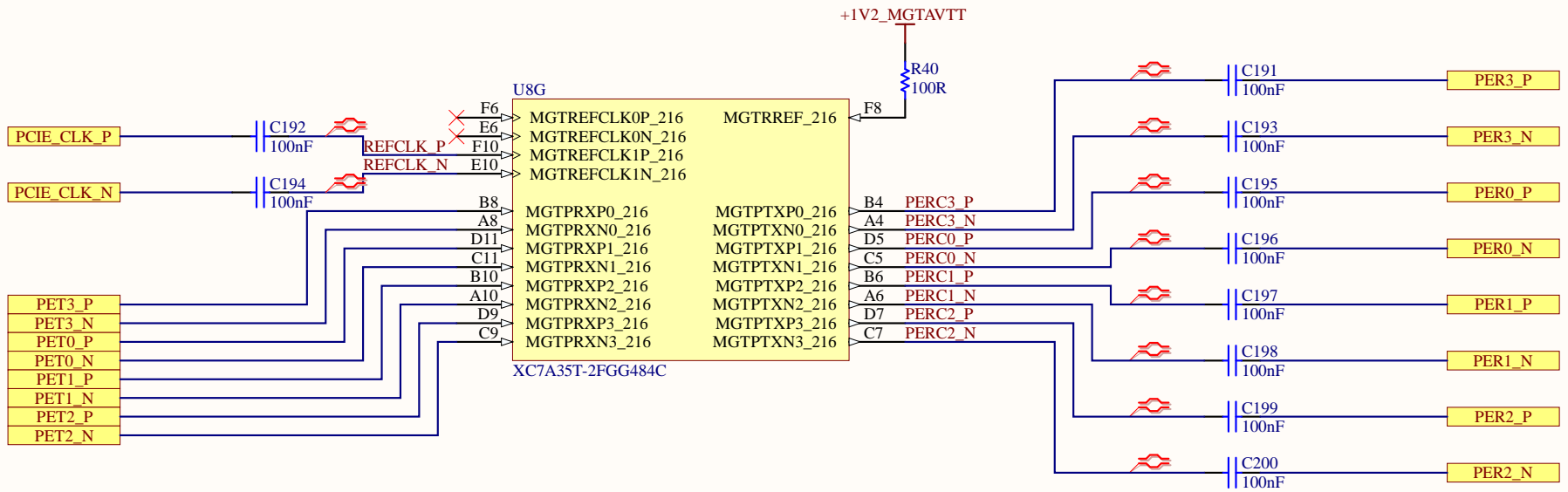
Size A3	Number	Revision 3
Date:	10/28/2020	Sheet 2 of 10
File:	C:\Users\...Power.SchDoc	Drawn By: FotatoPotato

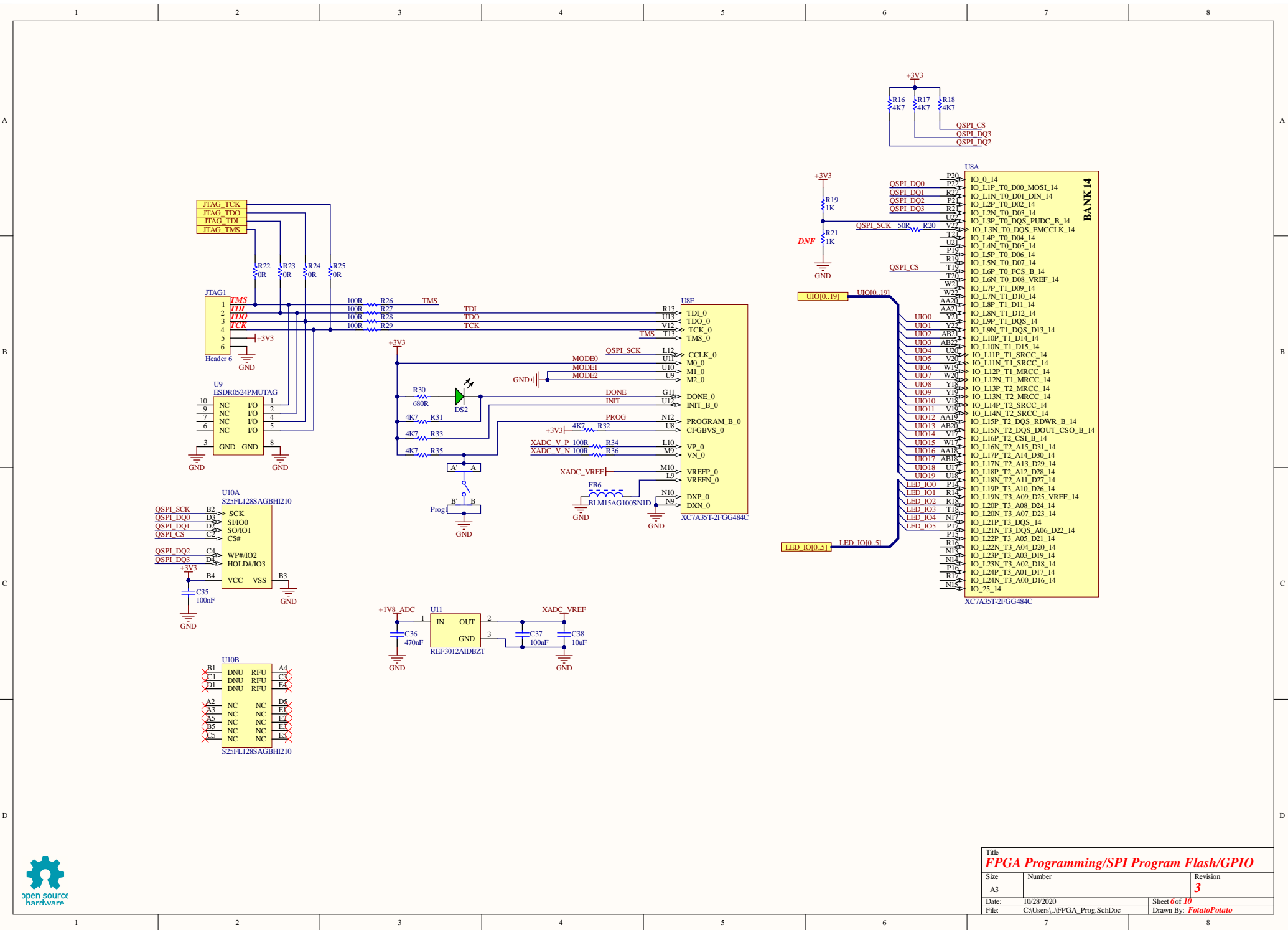




Title			FPGA System Power
Size	Number	Revision	3
Date	10/26/2020	Sheet of 40	
Doc	C:\Users\FPGA_Power\Desktop\Drawn By: FPGAPower	Drawn By: FPGAPower	

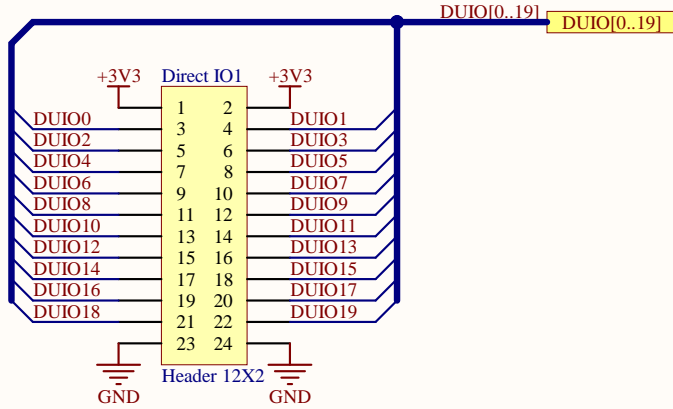




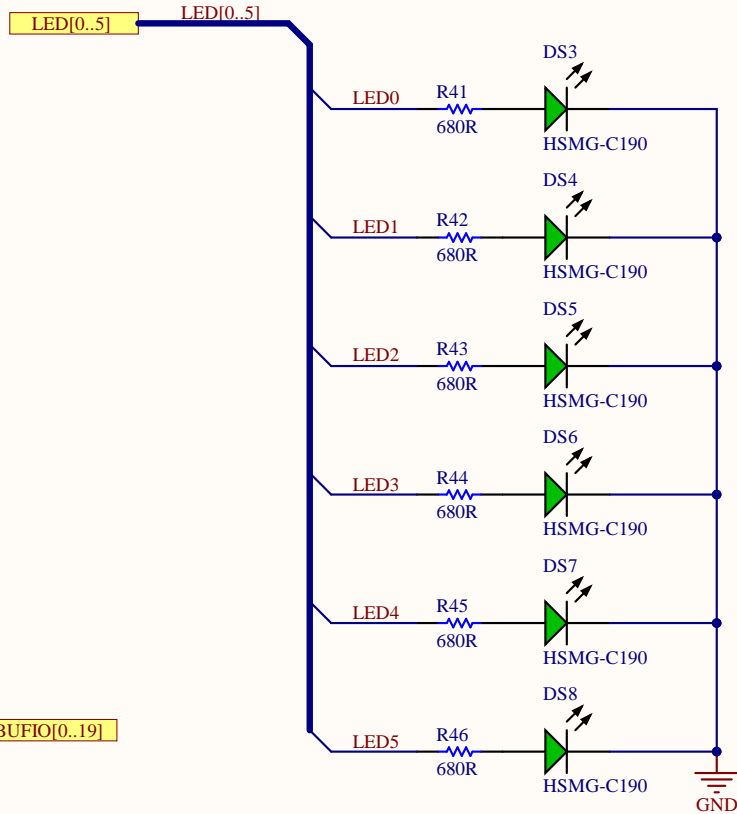
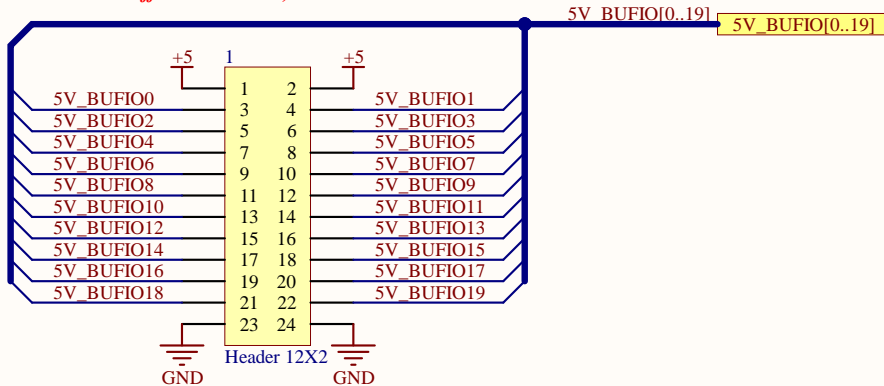


Title		
FPGA Programming/SPI Program Flash/GPIO		
Size	Number	Revision
A3		3
Date:	10/28/2020	Sheet 6 of 10
File:	C:\Users\... \FPGA_Prog.SchDoc	Drawn By: PotatoPotato

Direct FPGA IO 3.3V ONLY

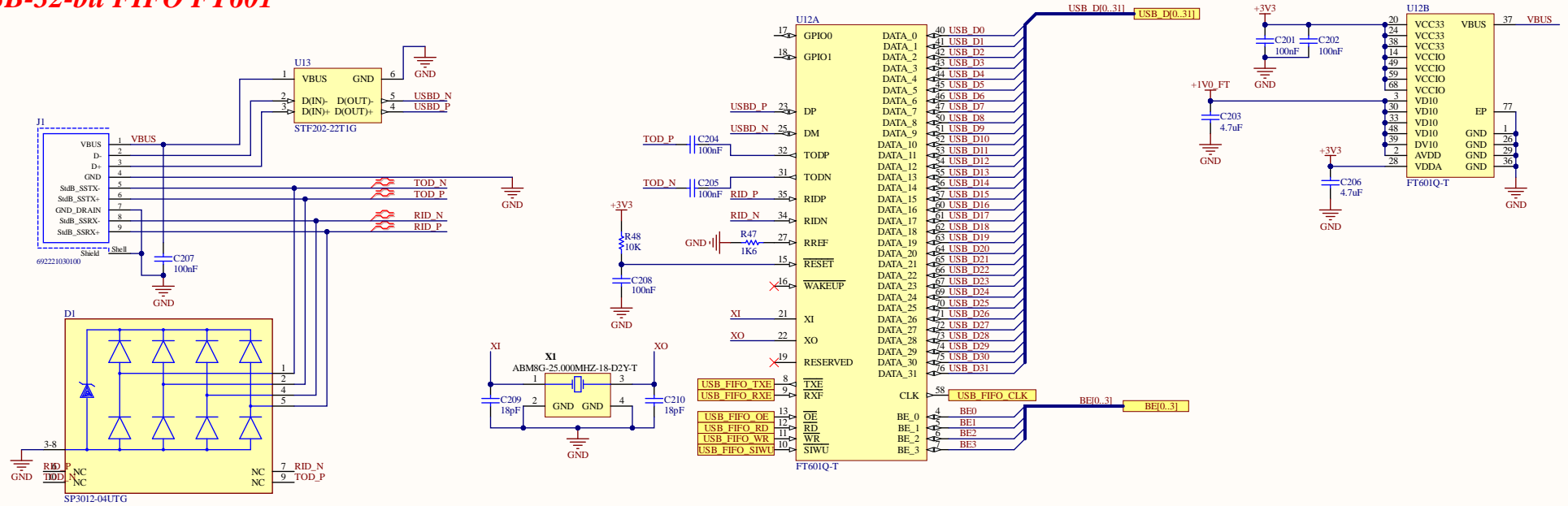


Buffered FPGA IO, 5V Tolerant

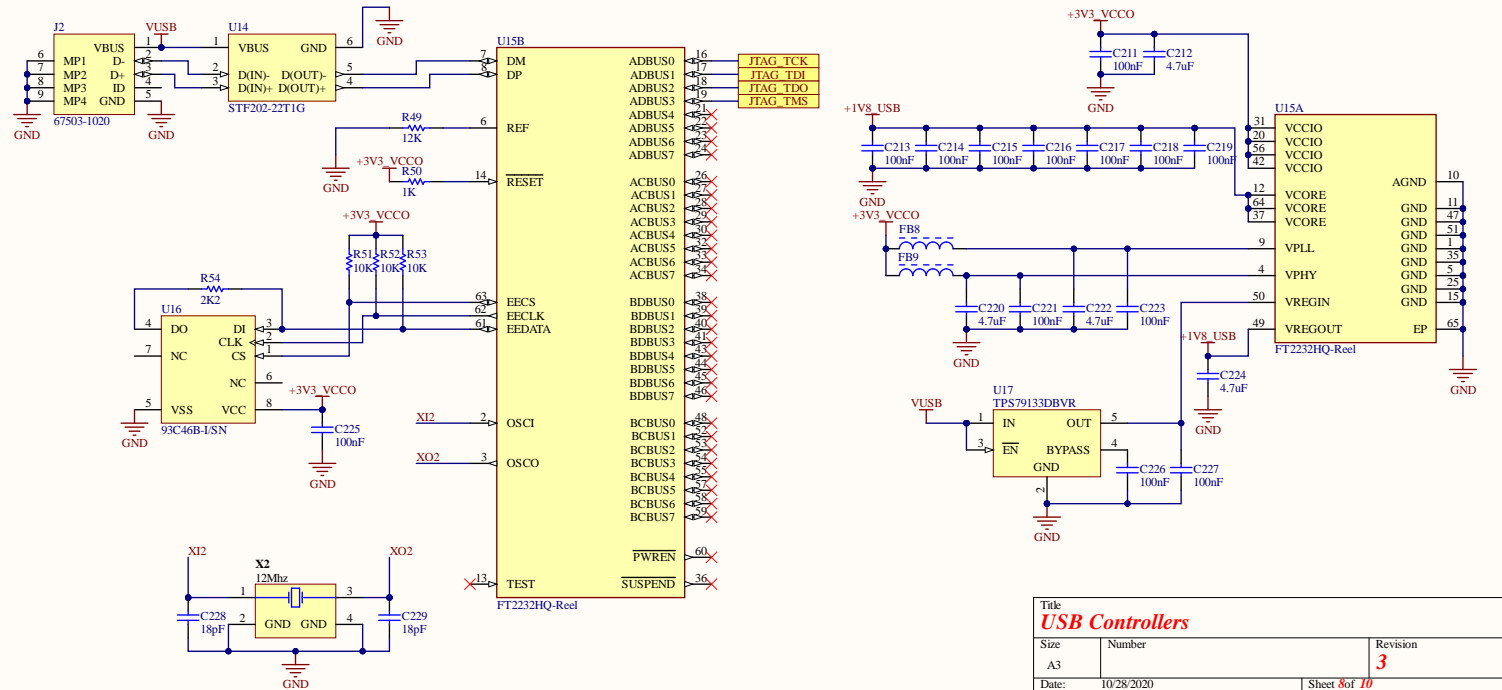


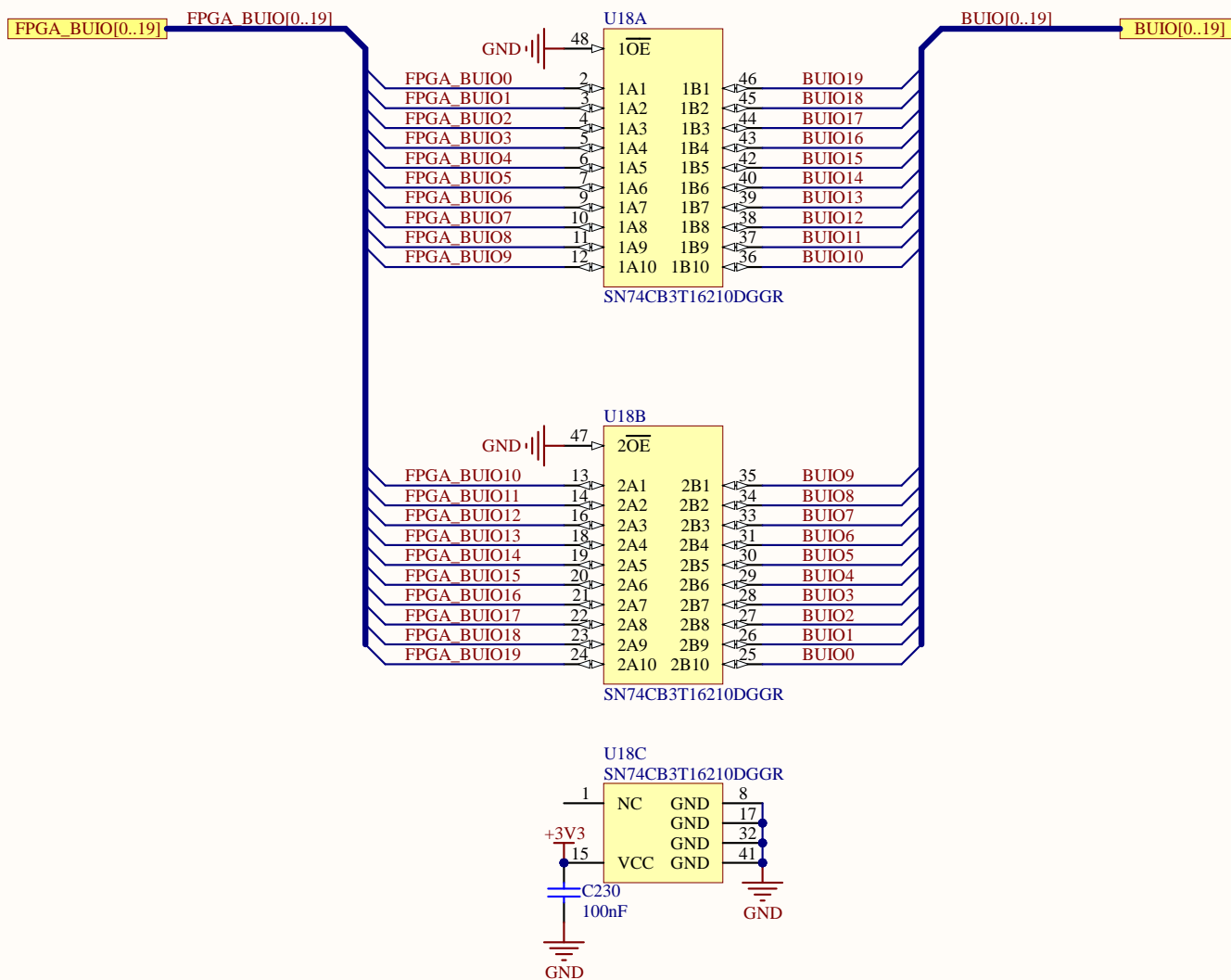
Title		
User GPIO and LED's		
Size	Number	Revision
A		1
Date:	10/28/2020	Sheet 7 of 10
File:	C:\Users\...\LED_User_IO.SchDoc	Drawn By: FotatoPotato

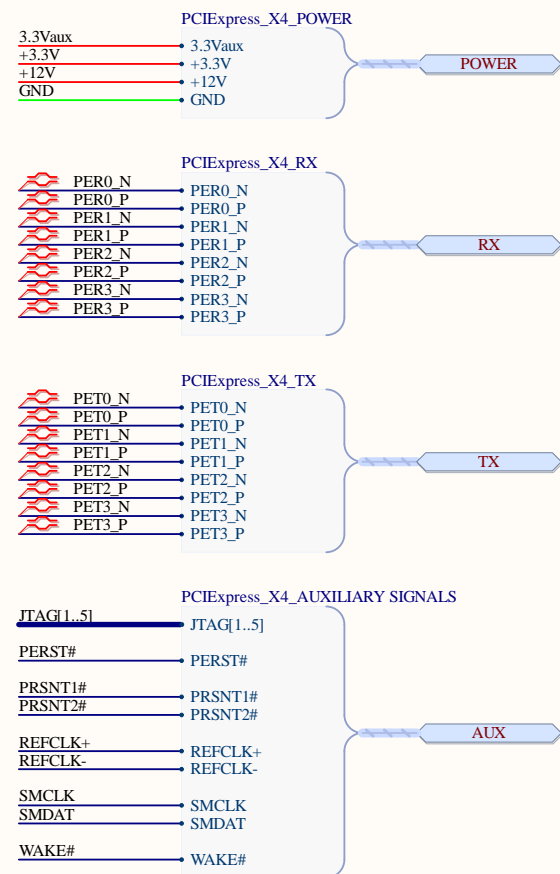
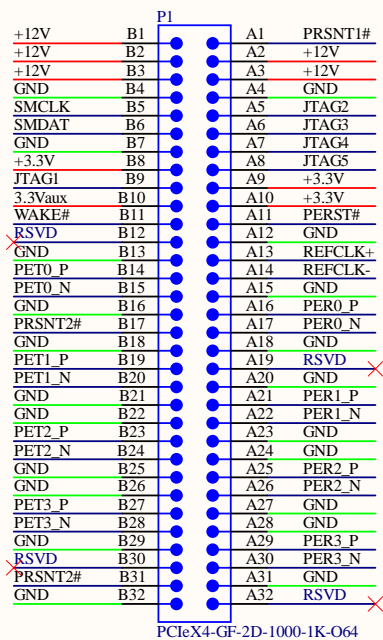
USB-32-bit FIFO FT601



USB-JTAG FT2232







Sheet Title **PCI Express x4 64Pin**

Project Title **PCI Express x4 Low profile card**

Size: **A4** Item: Revision:

Date: 10/28/2020 Time: 1:38:31 AM Sheet * of *

File: CON_PCI_Express_X4_64PIN.SchDoc

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