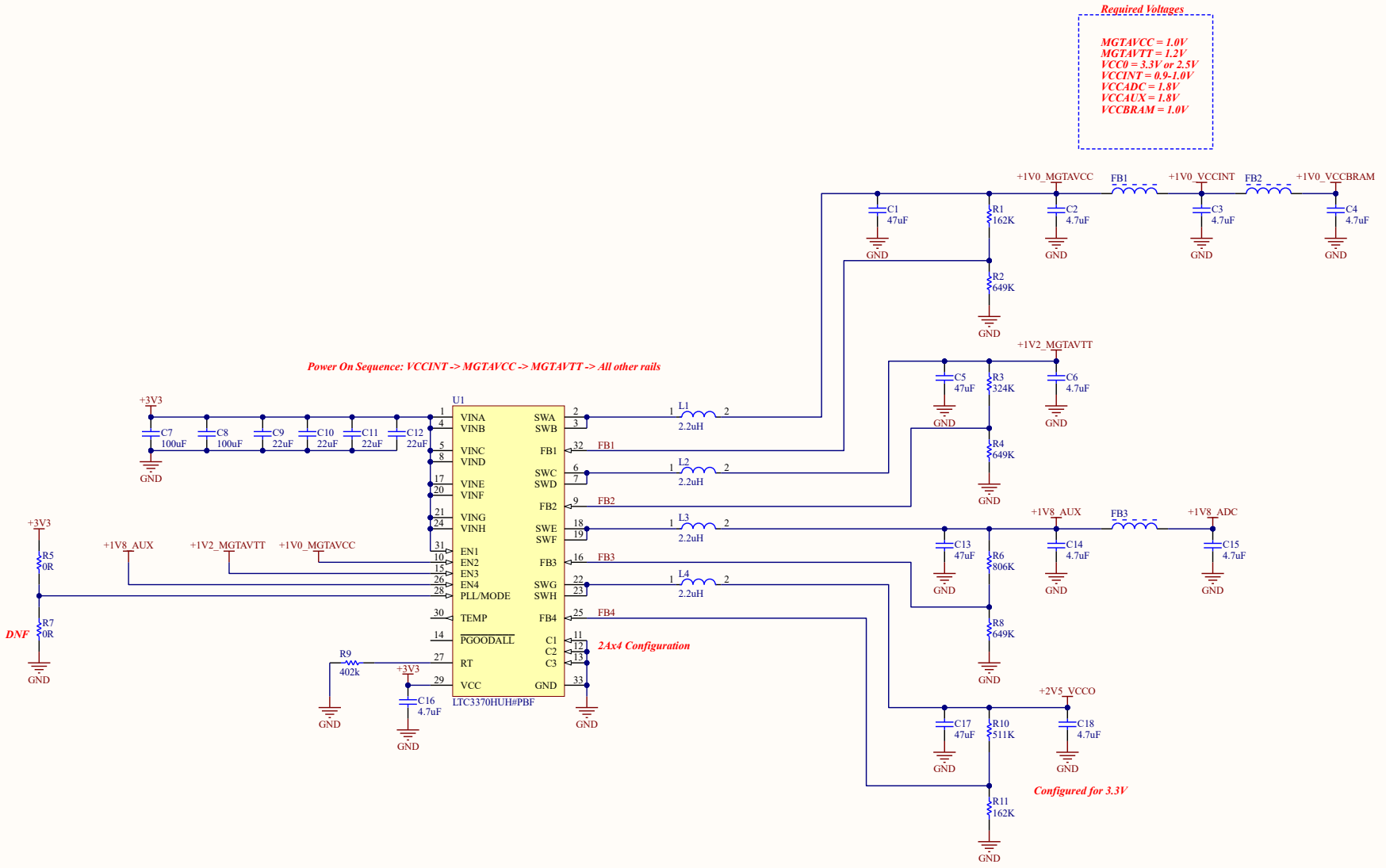
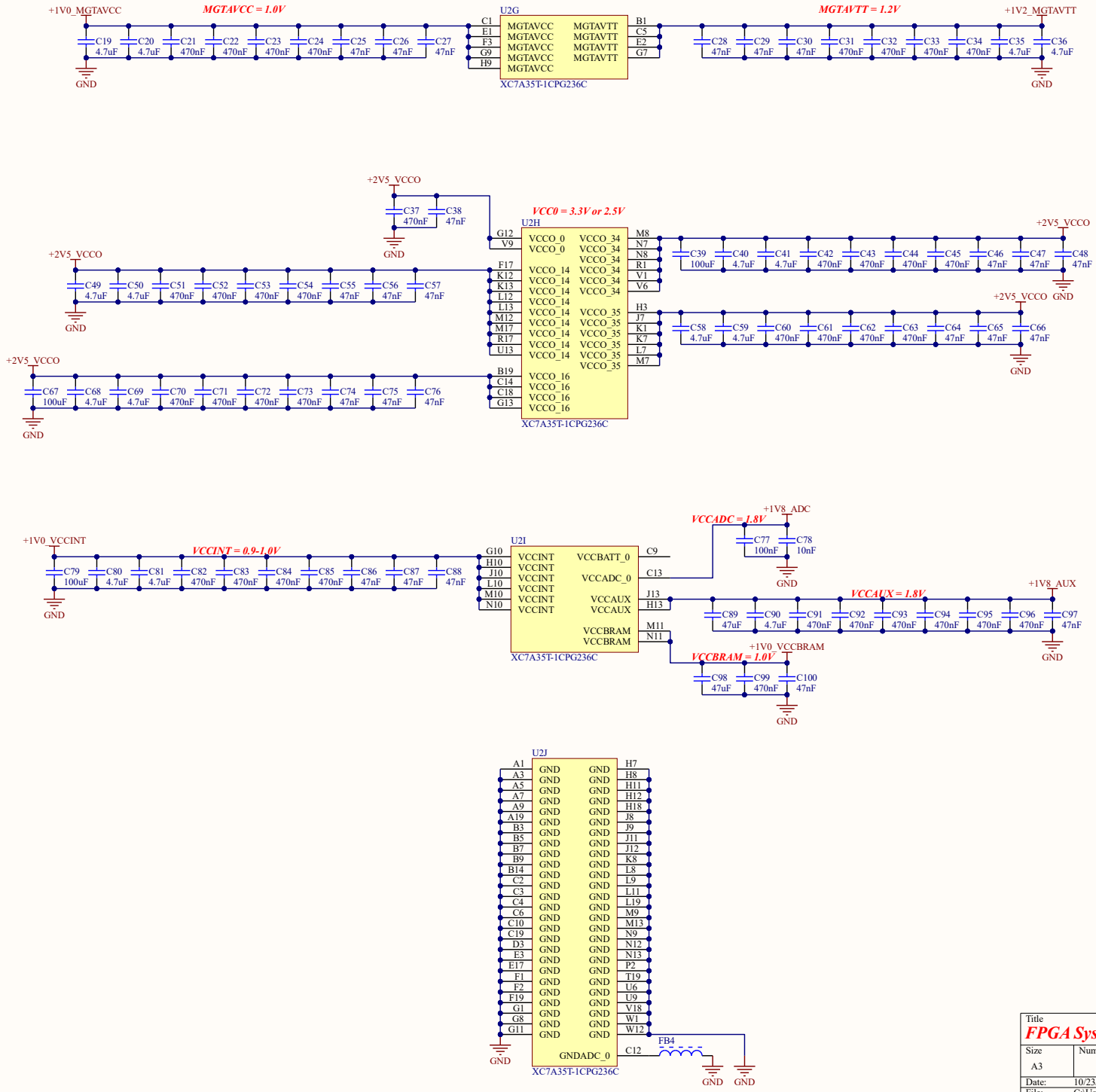
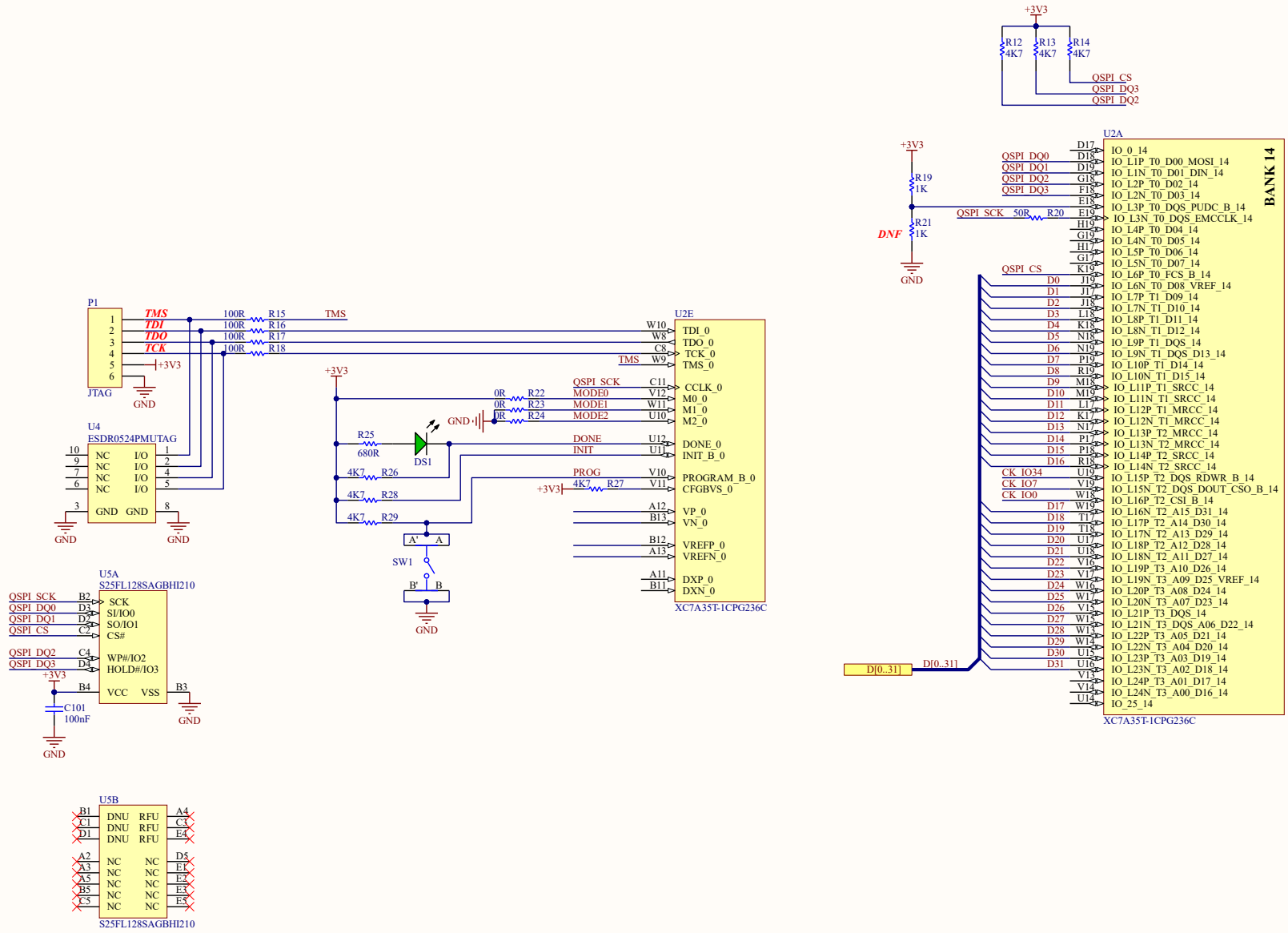


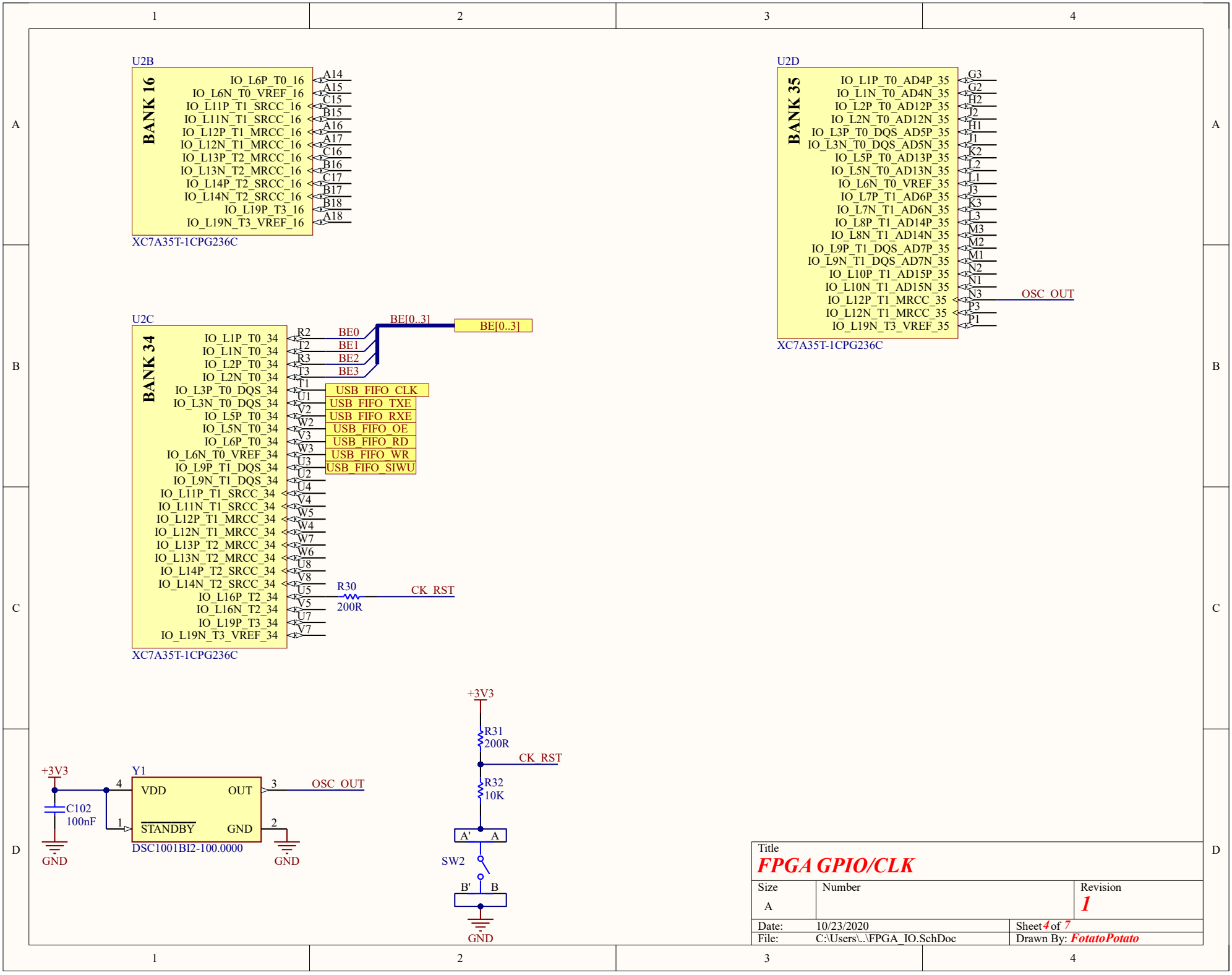
Title	**Power Supply Controller**	
Size: A3	Number:	Revision: 1
Date: 10/23/2020		Sheet 1 of 7
File: C:\Users\..\Power.SchDoc		Drawn By: FotatoPotato

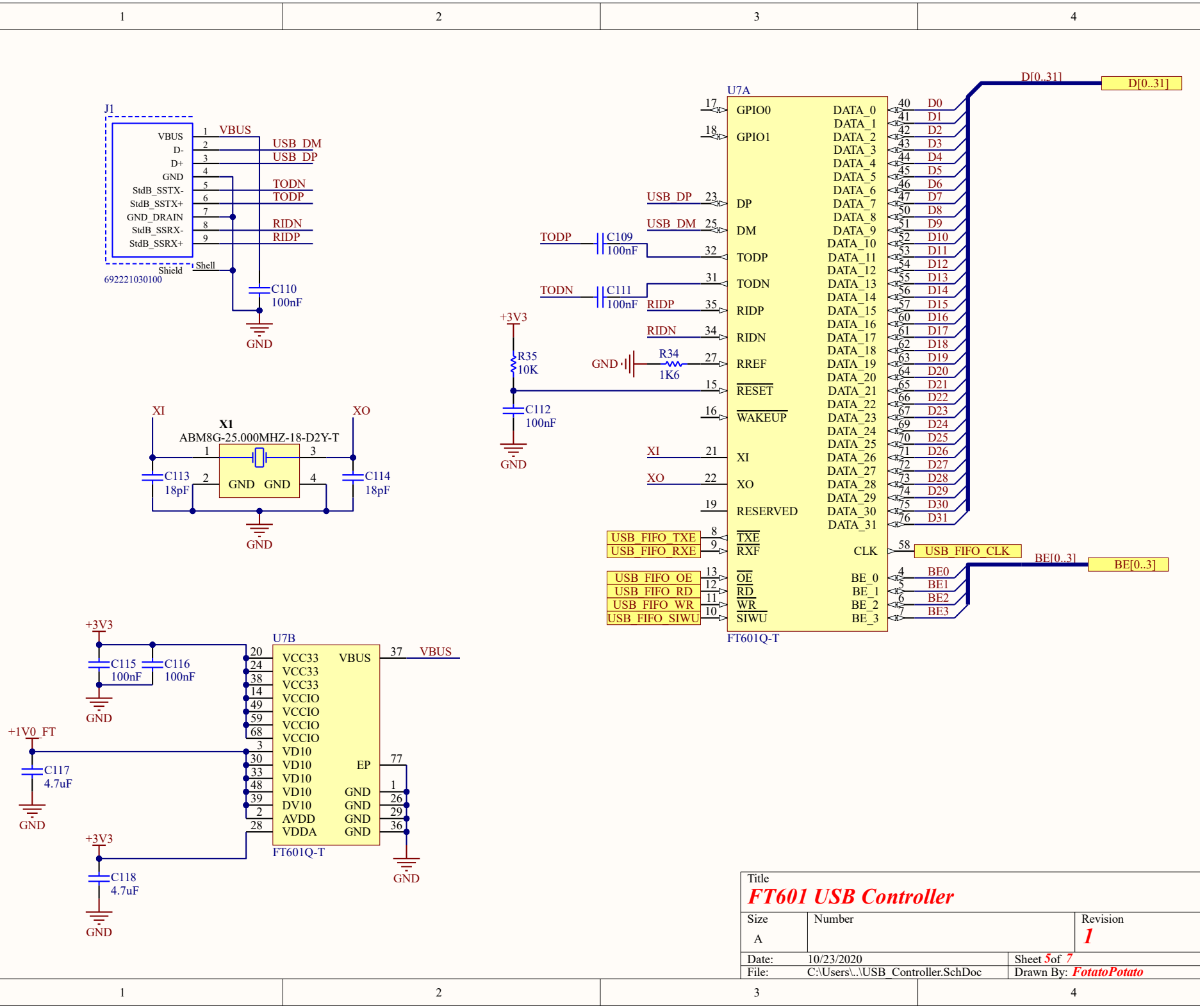


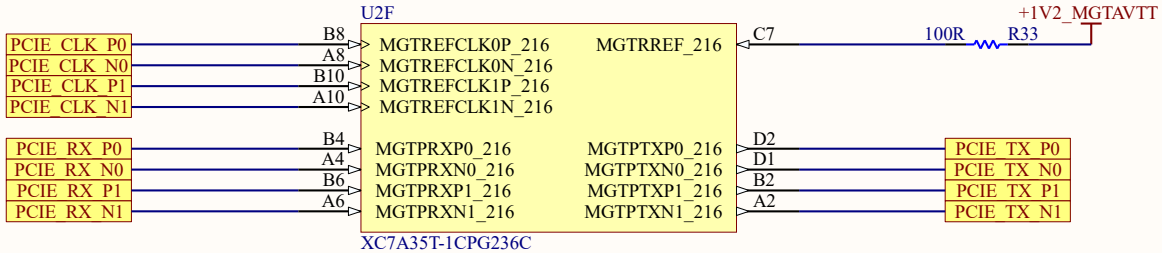
Title	**FPGA System Power**	
Size: A3	Number	Revision: *1*
Date: 10/23/2020	Sheet *2* of *7*	
File: C:\Users\..\FPGA_Power_Bank.SchDoc	Drawn By: *FotatoPotato*	



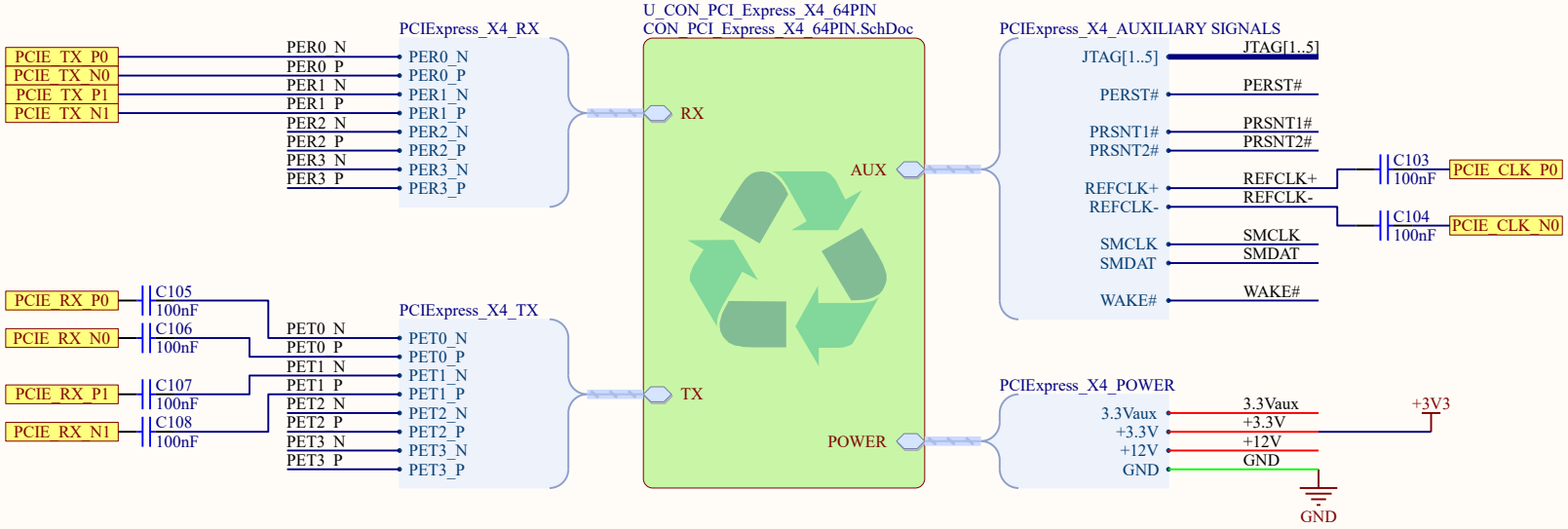
Title	**FPGA Programming/SPI**	
Size: A3	Number:	Revision: 1
Date: 10/23/2020	Sheet 3 of 7	
File: C:\Users\..\FPGA_Prog.SchDoc	Drawn By: FotatoPotato	


U2B
BANK 16
IO_L6P_T0_16 A14
IO_L6N_T0_VREF_16 A15
IO_L11P_T1_SRCC_16 C15
IO_L11N_T1_SRCC_16 B15
IO_L12P_T1_MRCC_16 A16
IO_L12N_T1_MRCC_16 A17
IO_L13P_T2_MRCC_16 C16
IO_L13N_T2_MRCC_16 B16
IO_L14P_T2_SRCC_16 C17
IO_L14N_T2_SRCC_16 B17
IO_L19P_T3_16 B18
IO_L19N_T3_VREF_16 A18
XC7A35T-1CPG236C
U2C
BANK 34
IO_L1P_T0_34 R2 BE0
IO_L1N_T0_34 T2 BE1
IO_L2P_T0_34 R3 BE2
IO_L2N_T0_34 T3 BE3
BE[0..3]
BE[0..3]
IO_L3P_T0_DQS_34 T1 USB_FIFO_CLK
IO_L3N_T0_DQS_34 U1 USB_FIFO_TXE
IO_L5P_T0_34 V2 USB_FIFO_RXE
IO_L5N_T0_34 W2 USB_FIFO_OE
IO_L6P_T0_34 V3 USB_FIFO_RD
IO_L6N_T0_VREF_34 W3 USB_FIFO_WR
IO_L9P_T1_DQS_34 U3 USB_FIFO_SIWU
IO_L9N_T1_DQS_34 U2
IO_L11P_T1_SRCC_34 U4
IO_L11N_T1_SRCC_34 V4
IO_L12P_T1_MRCC_34 W5
IO_L12N_T1_MRCC_34 W4
IO_L13P_T2_MRCC_34 W7
IO_L13N_T2_MRCC_34 W6
IO_L14P_T2_SRCC_34 U8
IO_L14N_T2_SRCC_34 V8
IO_L16P_T2_34 U5 R30 200R CK_RST
IO_L16N_T2_34 V5
IO_L19P_T3_34 U7
IO_L19N_T3_VREF_34 V7
XC7A35T-1CPG236C
U2D
BANK 35
IO_L1P_T0_AD4P_35 G3
IO_L1N_T0_AD4N_35 G2
IO_L2P_T0_AD12P_35 H2
IO_L2N_T0_AD12N_35 J2
IO_L3P_T0_DQS_AD5P_35 H1
IO_L3N_T0_DQS_AD5N_35 J1
IO_L5P_T0_AD13P_35 K2
IO_L5N_T0_AD13N_35 L2
IO_L6N_T0_VREF_35 L1
IO_L7P_T1_AD6P_35 J3
IO_L7N_T1_AD6N_35 K3
IO_L8P_T1_AD14P_35 L3
IO_L8N_T1_AD14N_35 M3
IO_L9P_T1_DQS_AD7P_35 M2
IO_L9N_T1_DQS_AD7N_35 M1
IO_L10P_T1_AD15P_35 N2
IO_L10N_T1_AD15N_35 N1
IO_L12P_T1_MRCC_35 N3 OSC_OUT
IO_L12N_T1_MRCC_35 P3
IO_L19N_T3_VREF_35 P1
XC7A35T-1CPG236C
+3V3
C102 100nF
GND
Y1
VDD OUT 4 3 OSC_OUT
STANDBY GND 1 2
DSC1001BI2-100.0000
GND
+3V3
R31 200R
CK_RST
R32 10K
A' A
SW2
B' B
GND
Title
FPGA GPIO/CLK
Size A
Number
Revision 1
Date: 10/23/2020
Sheet 4 of 7
File: C:\Users\..\FPGA_IO.SchDoc
Drawn By: FotatoPotato


J1
VBUS
D-
D+
GND
StdB_SSTX-
StdB_SSTX+
GND_DRAIN
StdB_SSRX-
StdB_SSRX+
Shell
692221030100
VBUS
USB_DM
USB_DP
TODN
TODP
RIDN
RIDP
C110
100nF
GND
XI
XO
X1
ABM8G-25.000MHZ-18-D2Y-T
C113
18pF
C114
18pF
GND GND
GND
+3V3
C115
100nF
C116
100nF
GND
+1V0_FT
C117
4.7uF
GND
+3V3
C118
4.7uF
GND
U7B
VCC33
VCC33
VCC33
VCCIO
VCCIO
VCCIO
VCCIO
VD10
VD10
VD10
VD10
DV10
AVDD
VDDA
VBUS
EP
GND
GND
GND
GND
FT601Q-T
GND
U7A
GPIO0
GPIO1
DP
DM
TODP
TODN
RIDP
RIDN
RREF
RESET
WAKEUP
XI
XO
RESERVED
TXE
RXF
OE
RD
WR
SIWU
DATA_0
DATA_1
DATA_2
DATA_3
DATA_4
DATA_5
DATA_6
DATA_7
DATA_8
DATA_9
DATA_10
DATA_11
DATA_12
DATA_13
DATA_14
DATA_15
DATA_16
DATA_17
DATA_18
DATA_19
DATA_20
DATA_21
DATA_22
DATA_23
DATA_24
DATA_25
DATA_26
DATA_27
DATA_28
DATA_29
DATA_30
DATA_31
CLK
BE_0
BE_1
BE_2
BE_3
USB_DP
USB_DM
TODP
C109
100nF
TODN
C111
100nF
+3V3
R35
10K
C112
100nF
GND
GND
R34
1K6
RIDP
RIDN
XI
XO
USB_FIFO_TXE
USB_FIFO_RXE
USB_FIFO_OE
USB_FIFO_RD
USB_FIFO_WR
USB_FIFO_SIWU
D[0..31]
D[0..31]
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
USB_FIFO_CLK
BE[0..3]
BE[0..3]
BE0
BE1
BE2
BE3
FT601Q-T
Title
FT601 USB Controller
Size
A
Number
Revision
1
Date: 10/23/2020
Sheet 5 of 7
File: C:\Users\..\USB_Controller.SchDoc
Drawn By: FotatoPotato



Title	**FPGA PCIE**	
Size: A	Number:	Revision: 1
Date: 10/23/2020		Sheet 6 of 7
File: C:\Users\..\FPGA_PCIE.SchDoc		Drawn By: FotatoPotato



- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.

Sheet Title	***PCI Express x4 Top Sheet***		
Project Title	***PCI Express x4 Low profile card***		
Size: A4	Item:	Revision:	
Date: 10/23/2020	Time: 8:31:20 PM	Sheet 1 of 2	
File: PCI Express_16765X6890_64PIN_Low profile.schdoc			

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