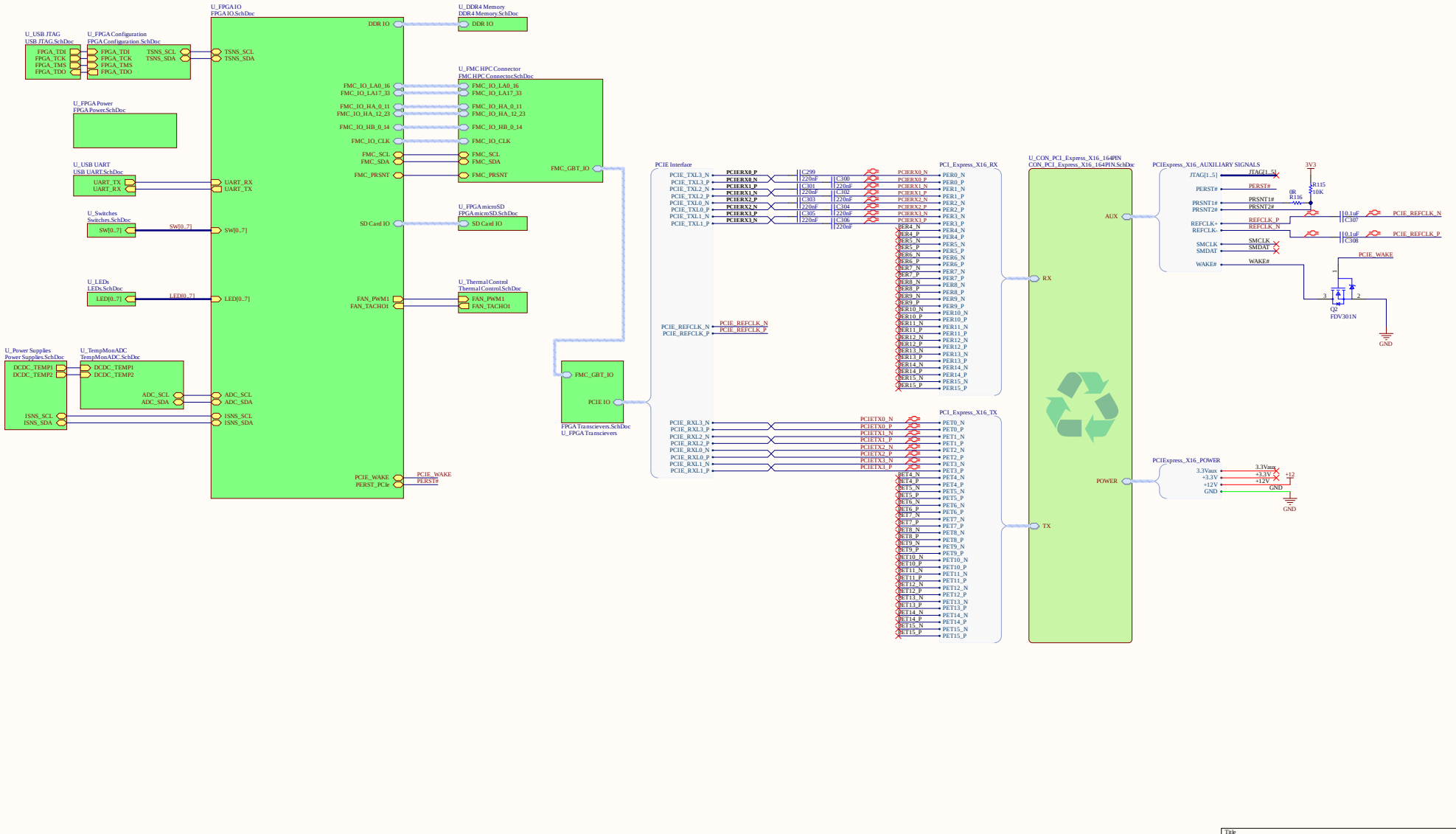
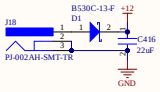
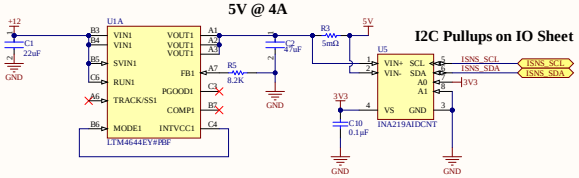
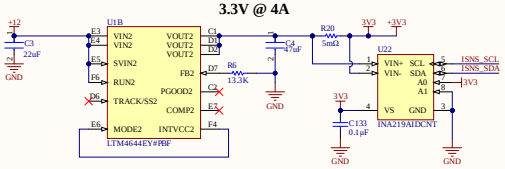

U_FPGA IO
FPGAIO.SchDoc
DDR IO
U_DDR4 Memory
DDR4 Memory.SchDoc
U_USB JTAG
USB JTAG.SchDoc
U_FPGA Configuration
FPGA Configuration.SchDoc
FPGA_TDI
FPGA_TCK
FPGA_TMS
FPGA_TDO
TSNS_SCL
TSNS_SDA
U_FMC HPC Connector
FMC HPC ConnectorSchDoc
FMC_IO_LA0_16
FMC_IO_LA17_33
FMC_IO_HA_0_11
FMC_IO_HA_12_23
FMC_IO_HB_0_14
FMC_IO_CLK
FMC_SCL
FMC_SDA
FMC_PRSNT
FMC_GBT_IO
U_FPGA Power
FPGA Power.SchDoc
U_USB UART
USB UART.SchDoc
UART_TX
UART_RX
U_Switches
Switches.SchDoc
SW[0..7]
U_FPGA microSD
FPGA microSD.SchDoc
SD Card IO
U_LEDs
LEDs.SchDoc
LED[0..7]
U_Thermal Control
Thermal Control.SchDoc
FAN_PWM1
FAN_TACHO1
U_Power Supplies
Power Supplies.SchDoc
DCDC_TEMP1
DCDC_TEMP2
U_TempMonADC
TempMonADC.SchDoc
ADC_SCL
ADC_SDA
ISNS_SCL
ISNS_SDA
PCIE_WAKE
PERST_PCIe
PERST#
PCIE Interface
PCIE_TXL3_N
PCIE_TXL3_P
PCIE_TXL2_N
PCIE_TXL2_P
PCIE_TXL0_N
PCIE_TXL0_P
PCIE_TXL1_N
PCIE_TXL1_P
PCIERX0_P
PCIERX0_N
PCIERX1_P
PCIERX1_N
PCIERX2_P
PCIERX2_N
PCIERX3_P
PCIERX3_N
C299
C300
C301
C302
C303
C304
C305
C306
220nF
PCIE_REFCLK_N
PCIE_REFCLK_P
FPGA Transcievers.SchDoc
U_FPGA Transcievers
PCIE IO
PCI_Express_X16_RX
PCI_Express_X16_TX
PCIETX0_N
PCIETX0_P
PCIETX1_N
PCIETX1_P
PCIETX2_N
PCIETX2_P
PCIETX3_N
PCIETX3_P
U_CON_PCI_Express_X16_164PIN
CON_PCI_Express_X16_164PIN.SchDoc
RX
TX
AUX
POWER
PCIExpress_X16_AUXILIARY SIGNALS
JTAG[1..5]
PERST#
PRSNT1#
PRSNT2#
REFCLK+
REFCLK-
SMCLK
SMDAT
WAKE#
3V3
R115
10K
R116
0R
0.1uF
C307
C308
PCIE_REFCLK_N
PCIE_REFCLK_P
PCIE_WAKE
Q2
FDV301N
GND
PCIExpress_X16_POWER
3.3Vaux
+3.3V
+12V
+12
Title
Top Sheet
Size
A2
Number
Revision
A
Date:
2/28/2023
Sheet 1 of 15
File:
C:\Users\..\TopSheet.SchDoc
Drawn By:
DragonEnjoyer



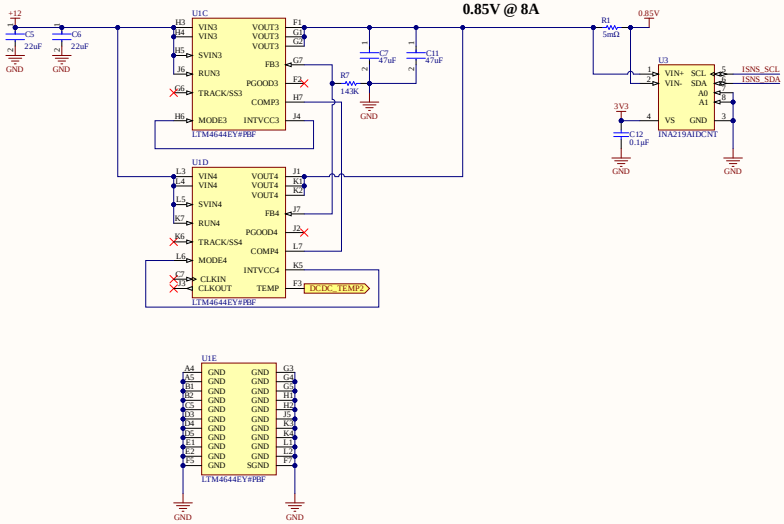
VIO
5V @ 4A



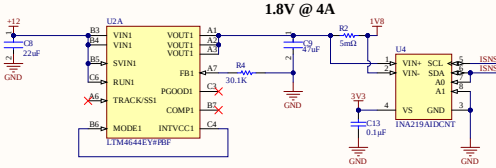
VIO
3.3V @ 4A



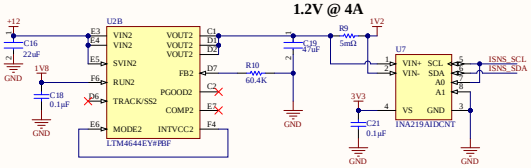
VCore
0.85V @ 8A



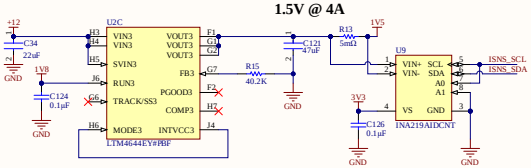
1.8V @ 4A



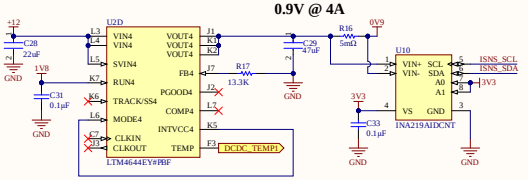
1.2V @ 4A



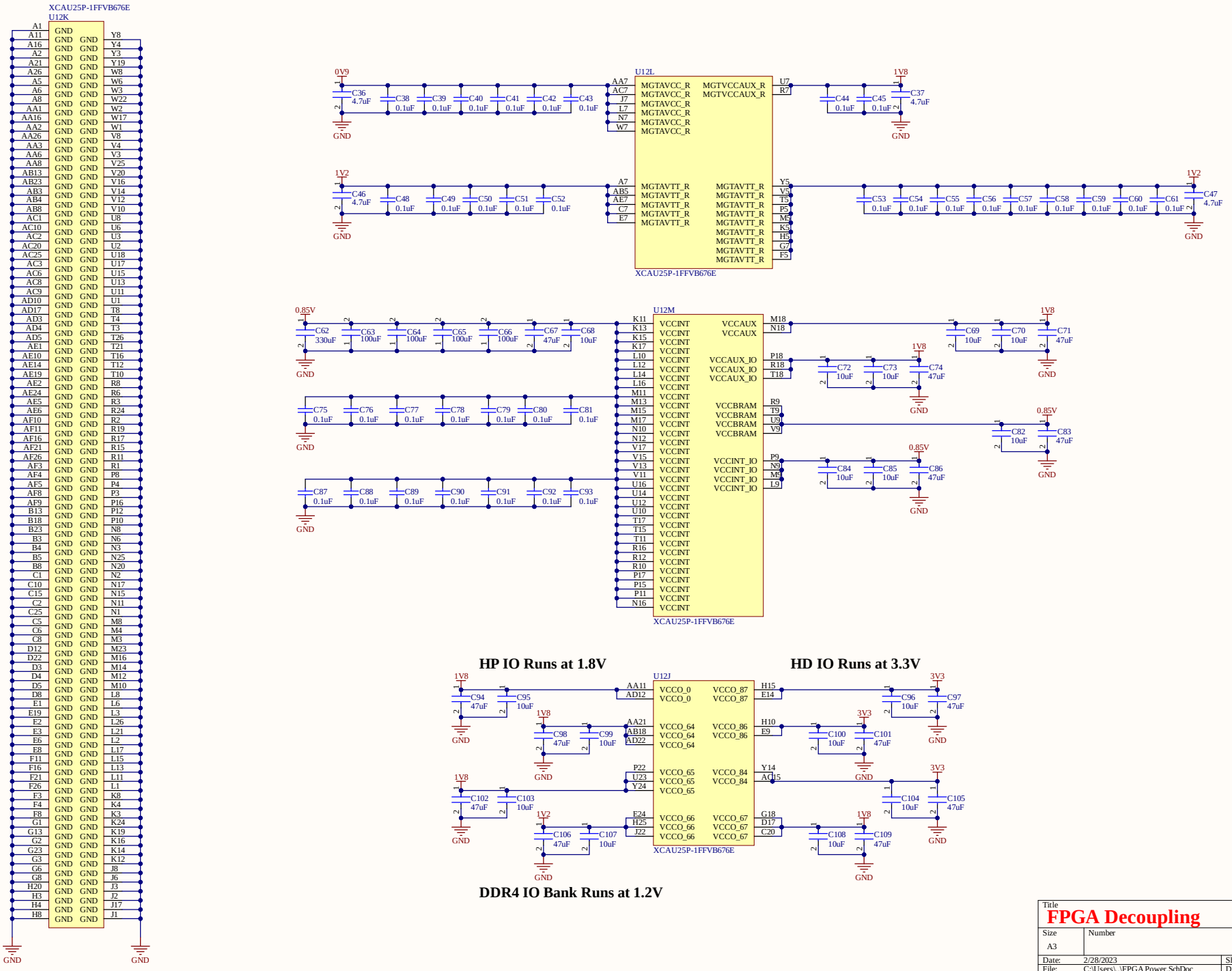
1.5V @ 4A



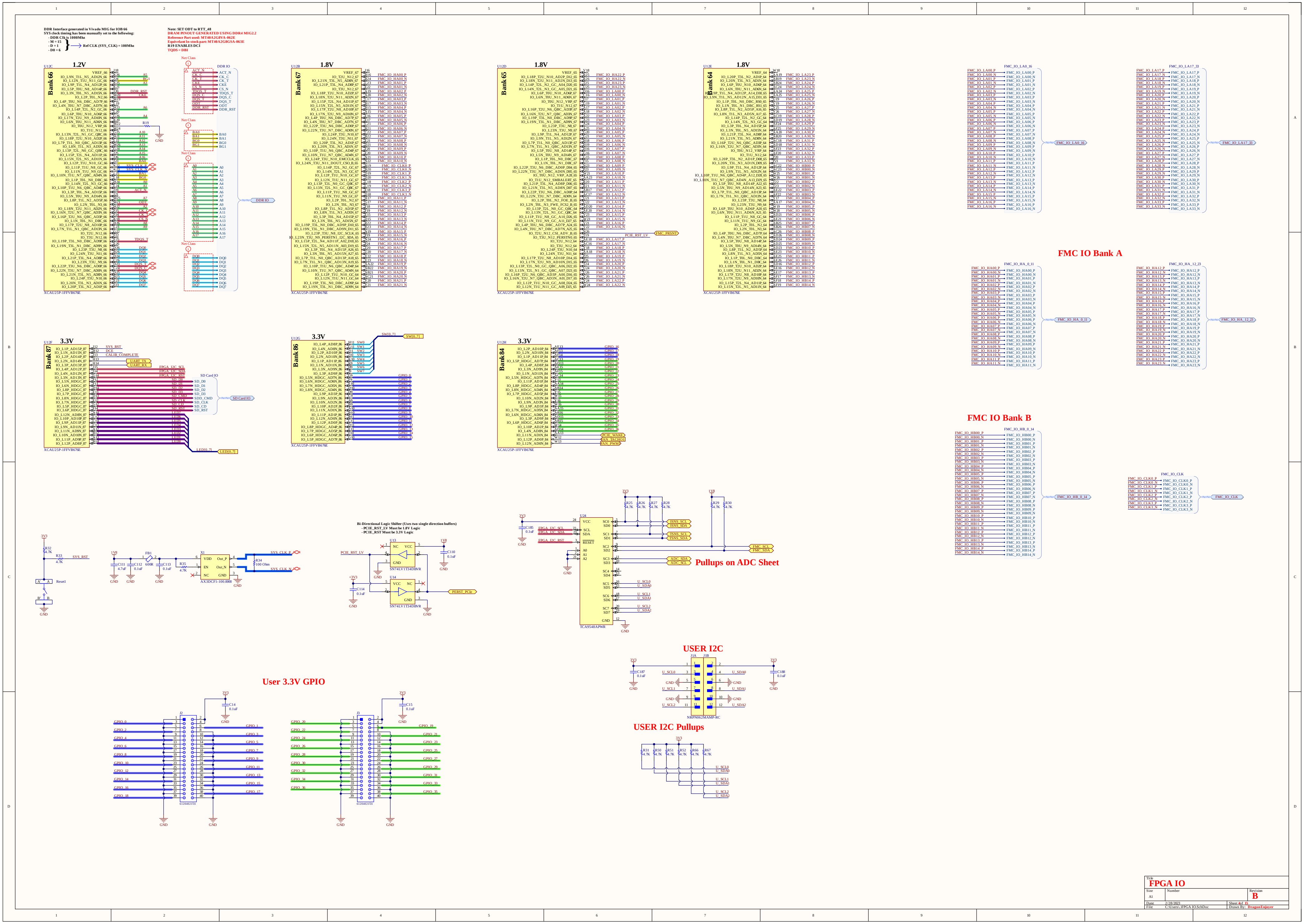
0.9V @ 4A

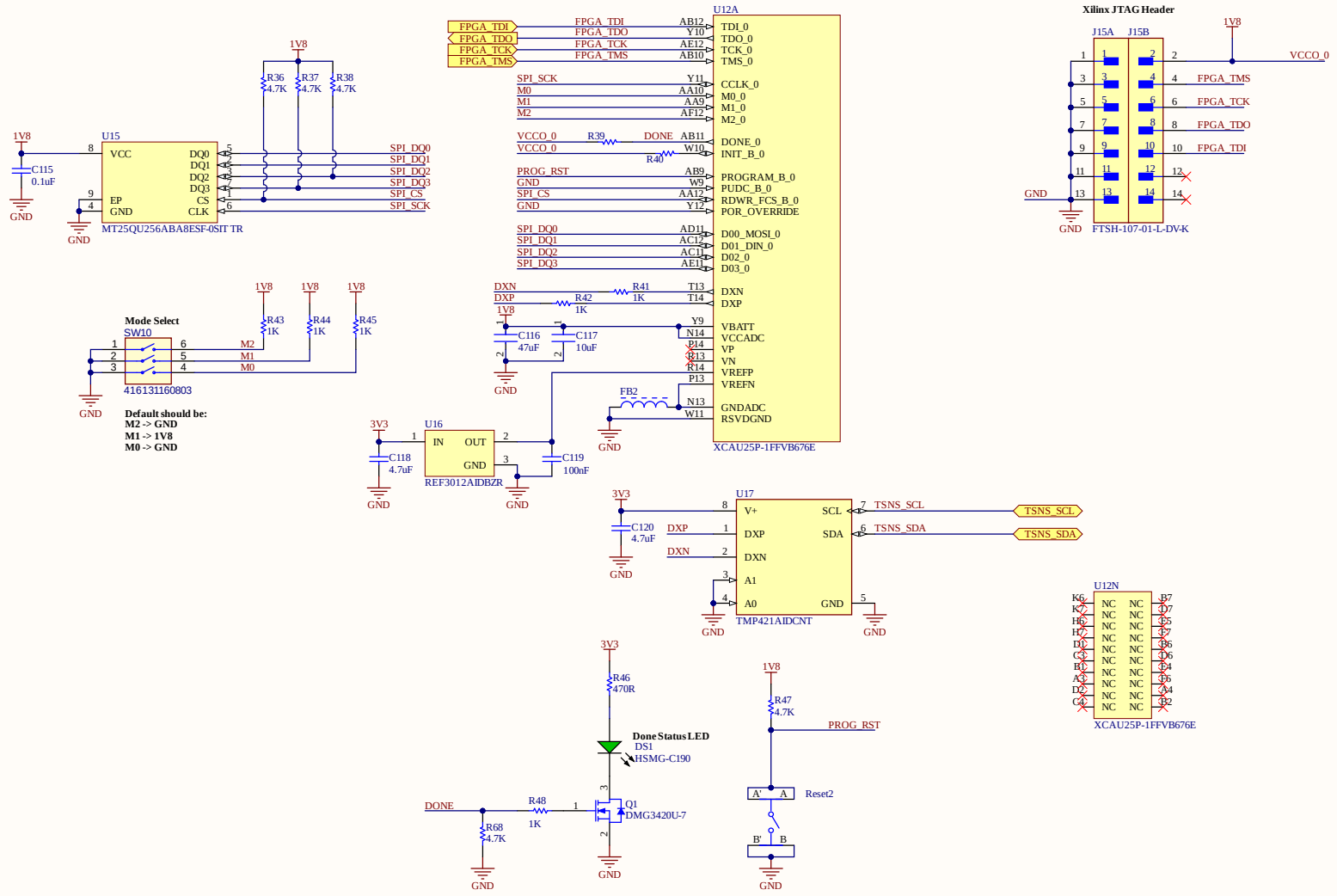


Title: **Power Supplies**		
Size: A2	Number:	Revision: **B**
Date: 2/28/2023		Sheet 2 of 15
File: C:\Users\...\Power Supplies.SchDoc		Drawn By: Dragon Enjoyer



Title	**FPGA Decoupling**		
Size: A3	Number:	Revision: **A**	
Date: 2/28/2023		Sheet 3 of 15	
File: C:\Users\..\FPGA Power.SchDoc		Drawn By: Dragon Enjoyer	


DDR Interface generated in Vivado MIG for IOB 66
SYS clock timing has been manually set to the following:
- DDR Clk is 1000Mhz
- M = 15
- D = 1
- D0 = 6
Ref CLK (SYS_CLK) = 100Mhz
Note: SET ODT to RTT_48
DRAM PINOUT GENERATED USING DDR4 MIG2.2
Reference Part used: MT40A2G8VA-062E
Equivelant In-stock part: MT40A2G8GSA-063E
R19 ENABLES DCI
TQDS = DBI
Net Class
DDR IO
U12C
1.2V
Bank 66
U12B
1.8V
Bank 67
U12D
Bank 65
U12E
Bank 64
U12F
3.3V
Bank 87
U12G
Bank 86
U12H
Bank 84
XCAU25P-1FFVB676E
SD Card IO
FMC IO Bank A
FMC IO Bank B
FMC_IO_LA0_16
FMC_IO_LA17_33
FMC_IO_HA_0_11
FMC_IO_HA_12_23
FMC_IO_HB_0_14
FMC_IO_CLK
Bi-Directional Logic Shifter (Uses two single direction buffers)
- PCIE_RST_LV Must be 1.8V Logic
- PCIE_RST Must be 3.3V Logic
SN74LV1T34DBVR
AX3DCF1-100.0000
TCA9548APWR
Pullups on ADC Sheet
User 3.3V GPIO
USER I2C
NRPN062MAMP-RC
USER I2C Pullups
Title
FPGA IO
Size
A1
Number
Revision
B
Date: 2/28/2023
Sheet 4 of 15
File: C:\Users\..\FPGA IO.SchDoc
Drawn By: DragonEnjoyer

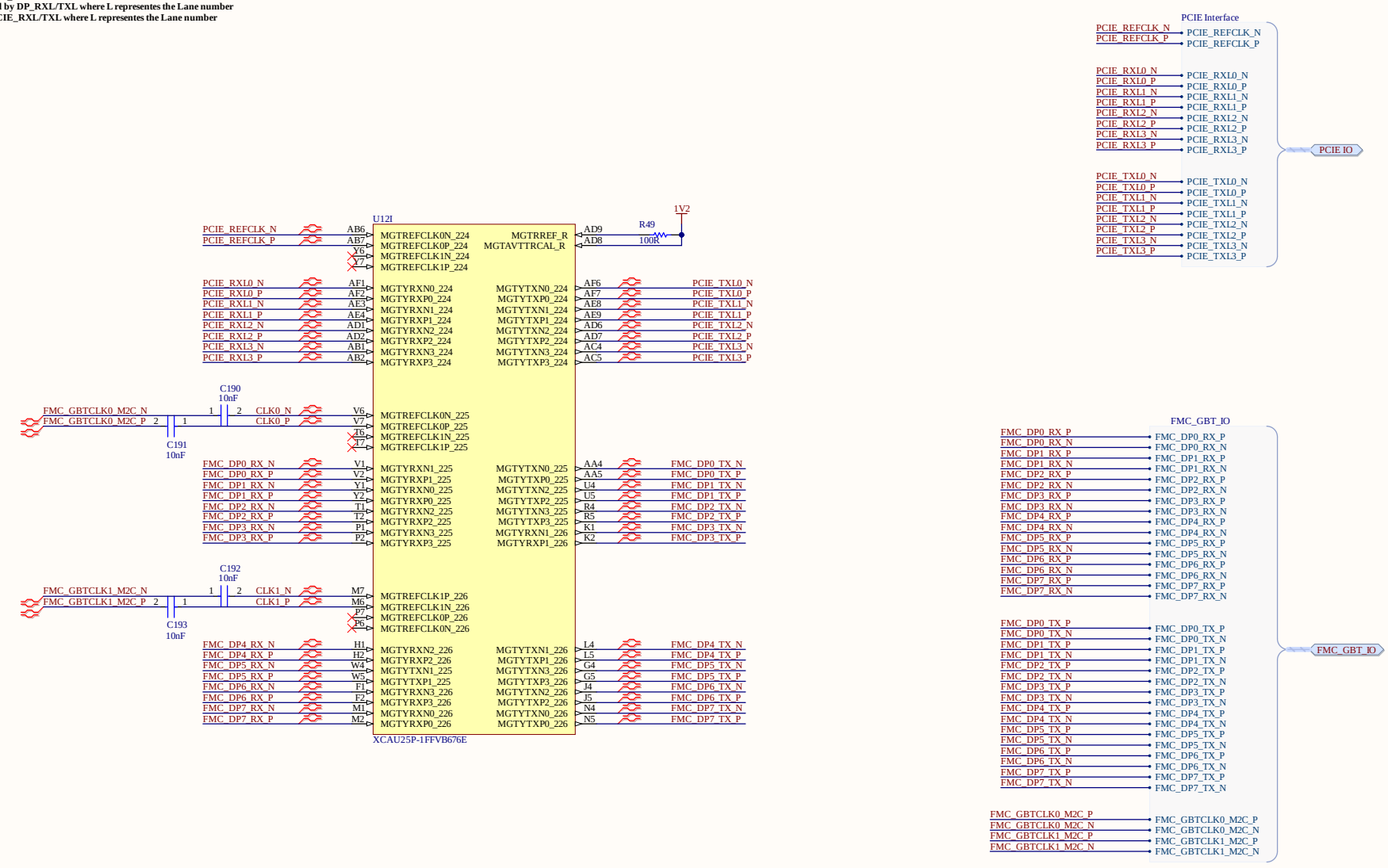


Title
FPGA Configuration

Size	Number	Revision
A3		A

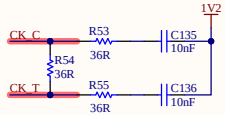
Date: 2/28/2023	Sheet 5 of 15
File: C:\Users\..\FPGA Configuration.SchDoc	Drawn By: Dragon Enjoyer

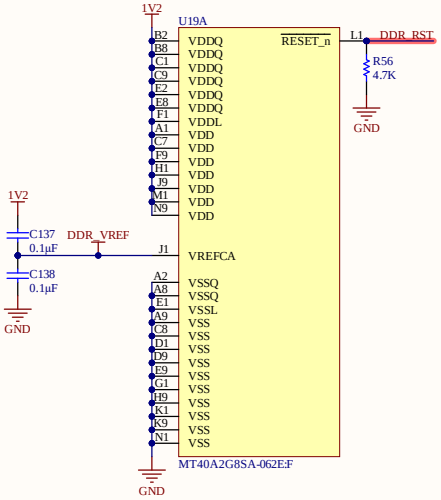
Note:
GTY Quad 224 used for PCIe Gen 3 x4
GTY Quad 225 Used for DP IN and Out
GTY Quad 226 Used for Free High Speed IO
Each GTY is capable of 16Gb/s
User GTY's are denoted by GTY_URX/UTX
Displayport GTY's are denoted by DP_RXL/TXL where L represents the Lane number
PCIE GTY's are denoted by PCIE_RXL/TXL where L represents the Lane number

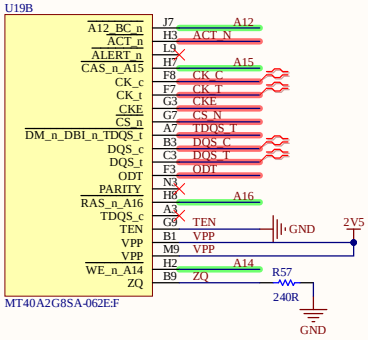


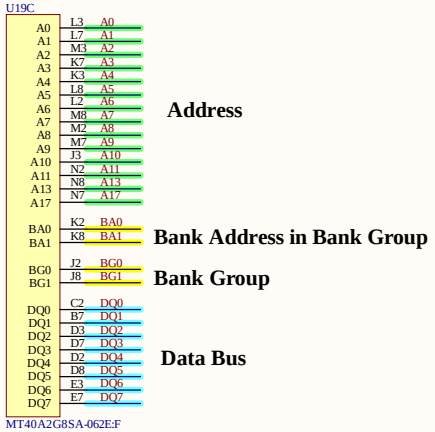
Title	**FPGA Transcievers**
Size	A3
Number	
Revision	**A**
Date:	2/28/2023
Sheet 6 of 15	
File:	C:\Users\..\FPGA Transcievers.SchDoc
Drawn By:	**Dragon Enjoyer**

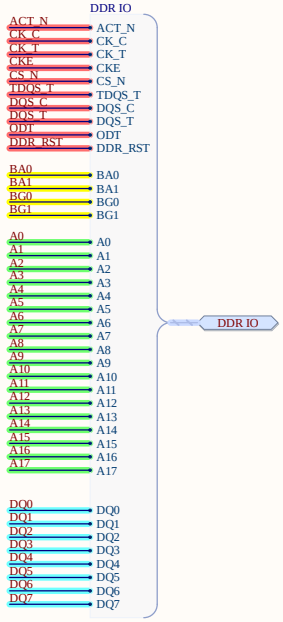
Termination Resistors not needed
Keep DRAM Close to FPGA and use ODT

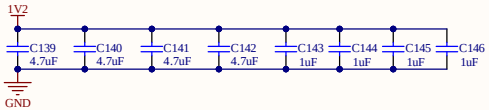


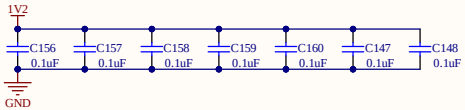


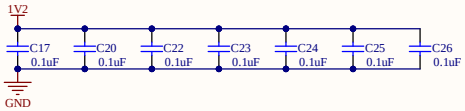


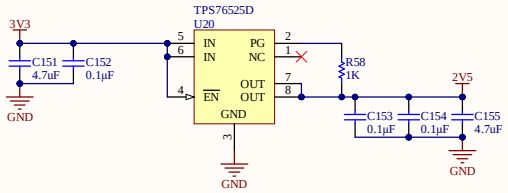


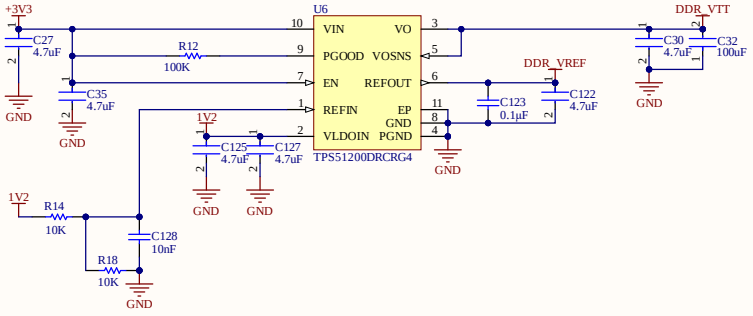




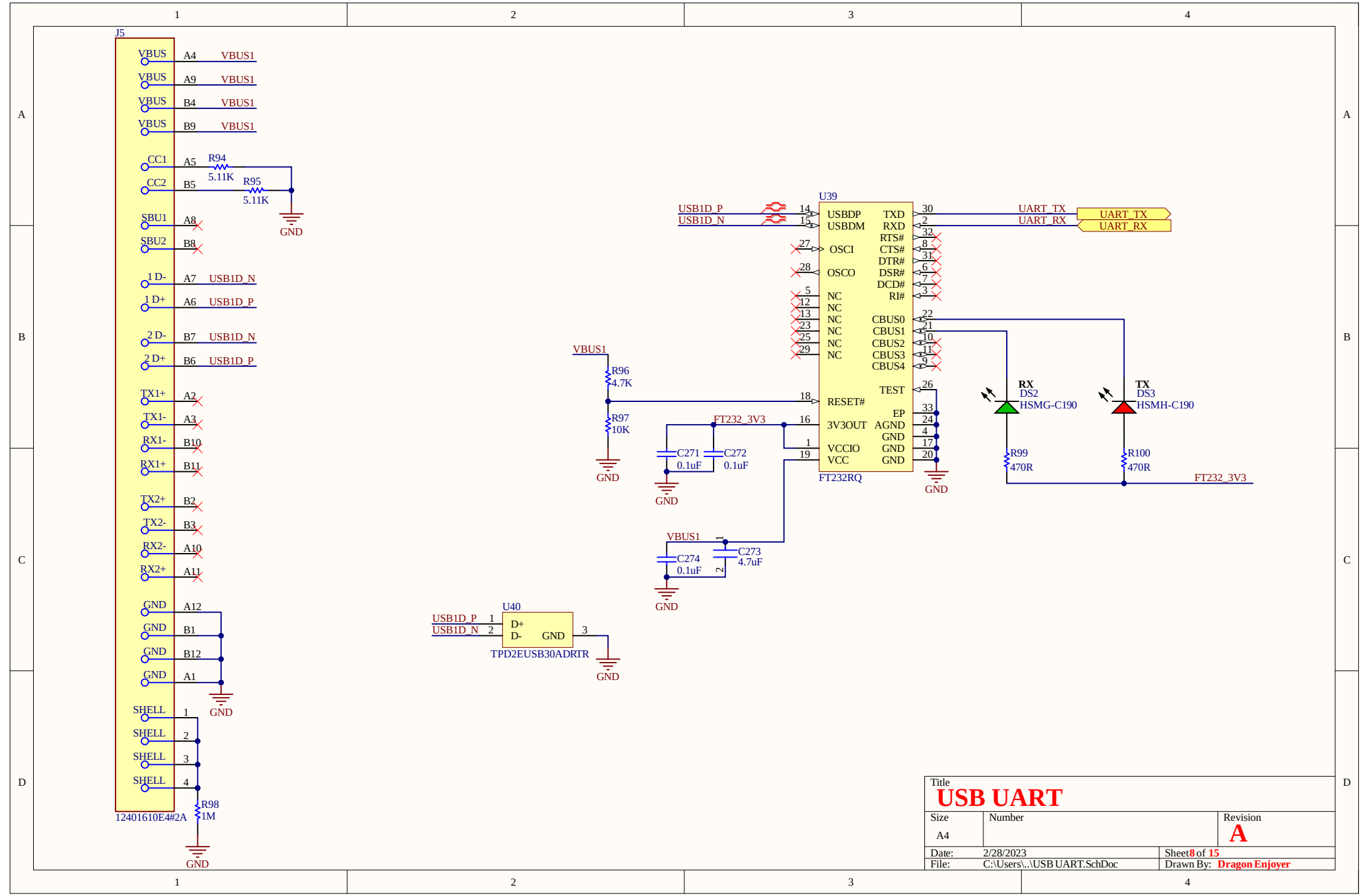




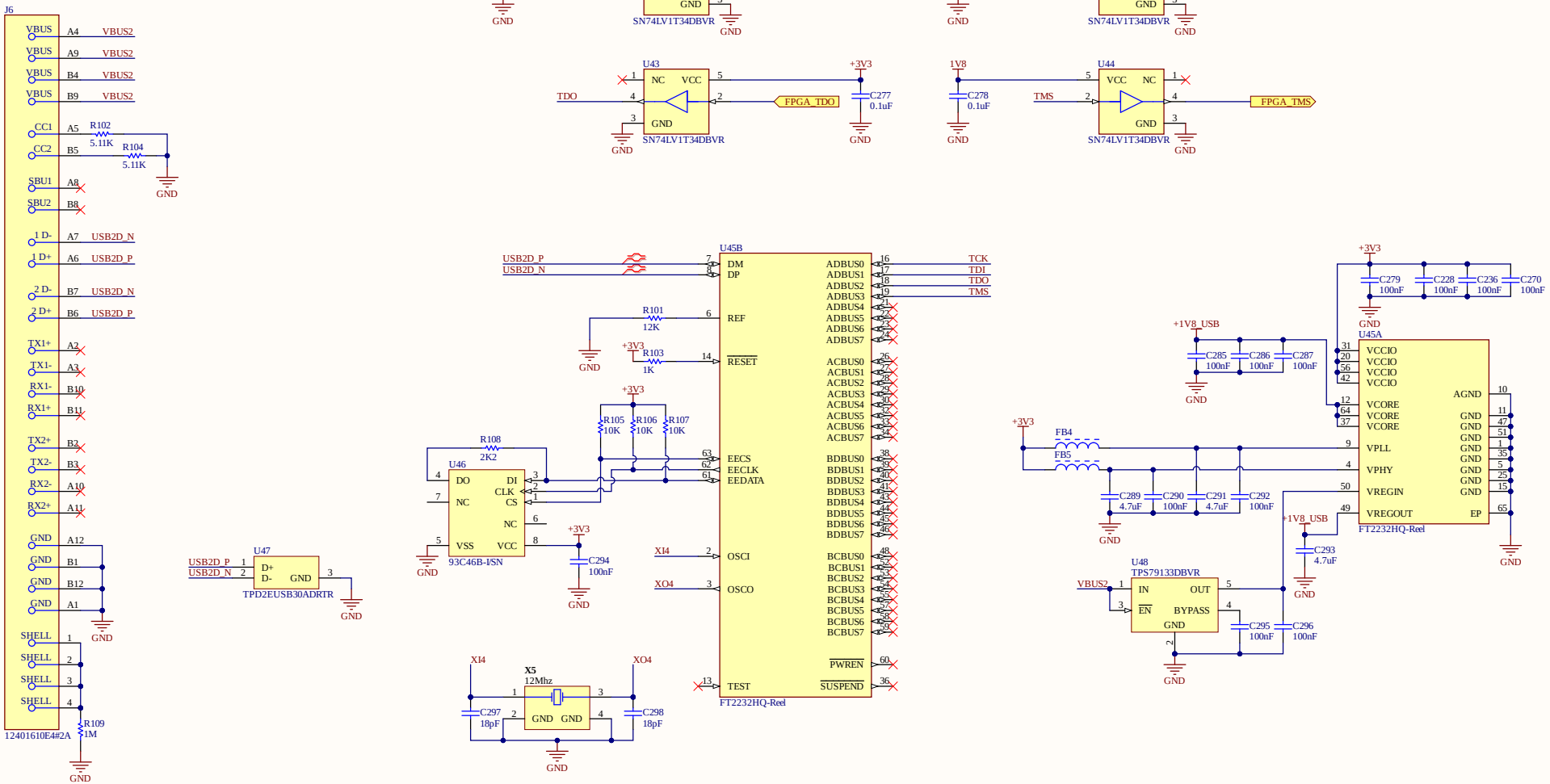




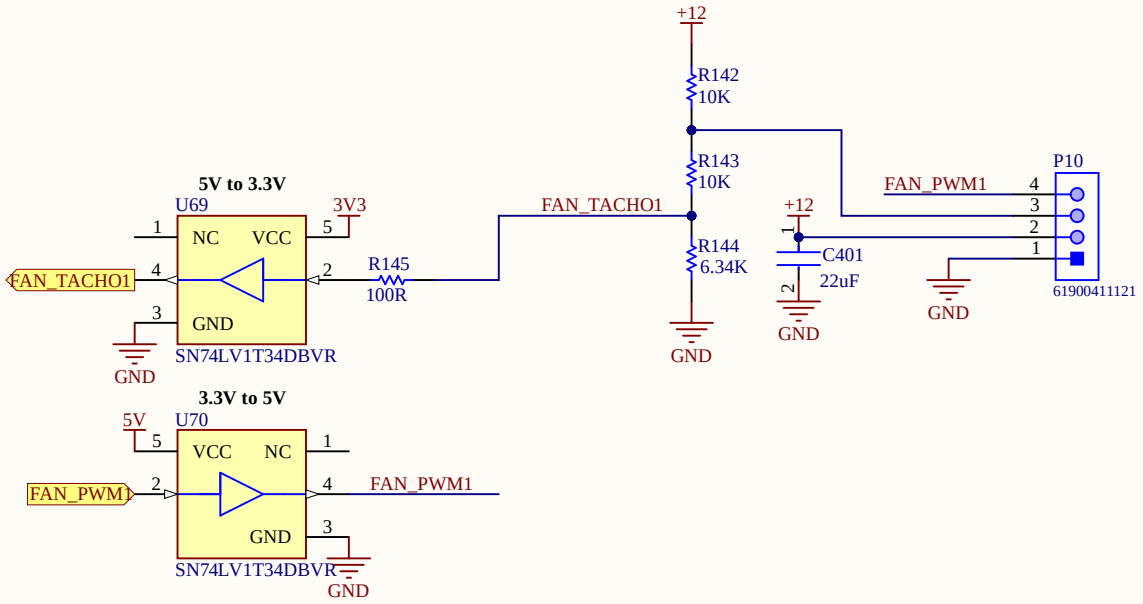
Title: **DDR4 RAM**		
Size: A3	Number:	Revision: **B**
Date: 2/28/2023		Sheet 7of 15
File: C:\Users\..\DDR4 Memory.SchDoc		Drawn By: Dragon Enjoyer



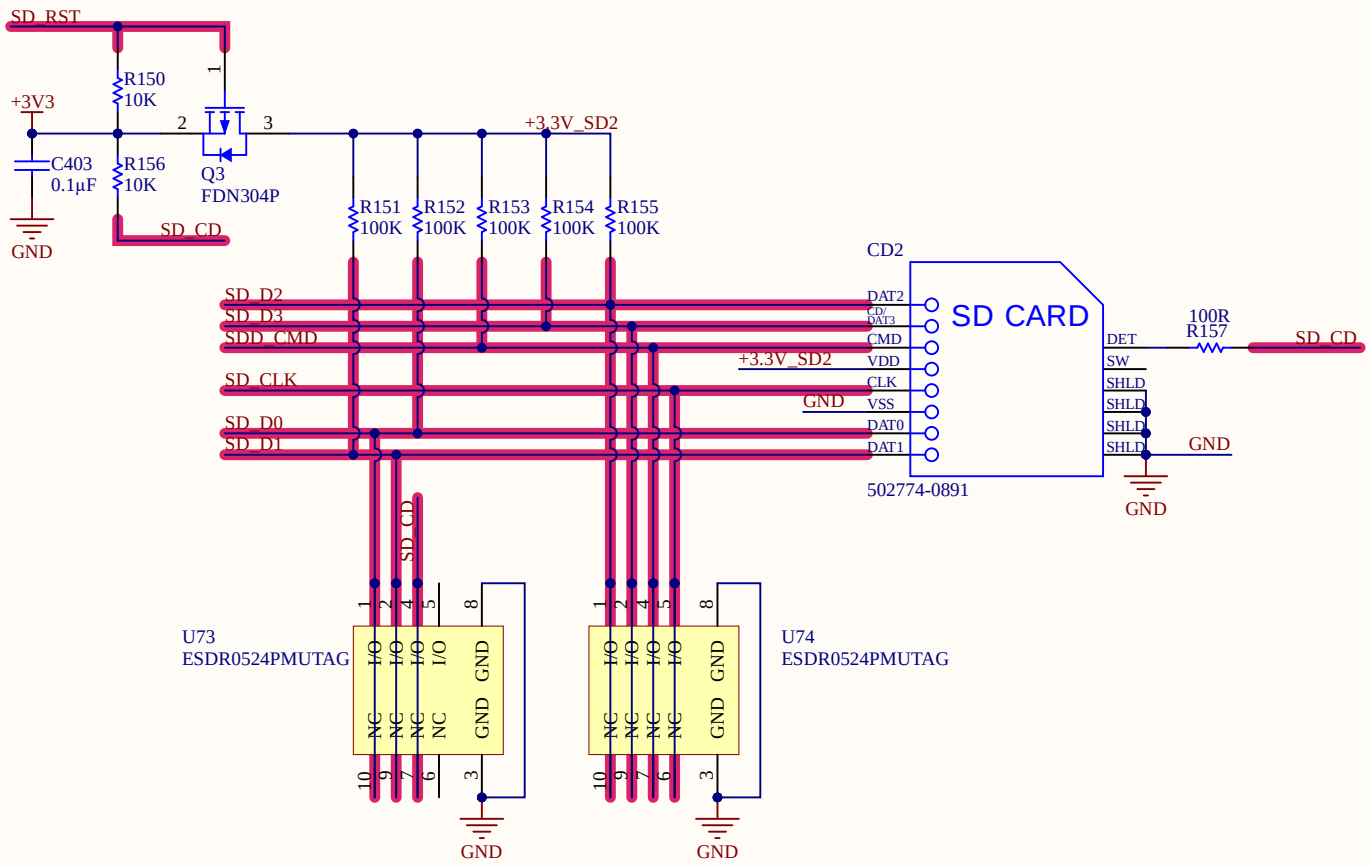
Title	**USB UART**	
Size: A4	Number:	Revision: **A**
Date: 2/28/2023		Sheet 8 of 15
File: C:\Users\..\USB UART.SchDoc		Drawn By: Dragon Enjoyer



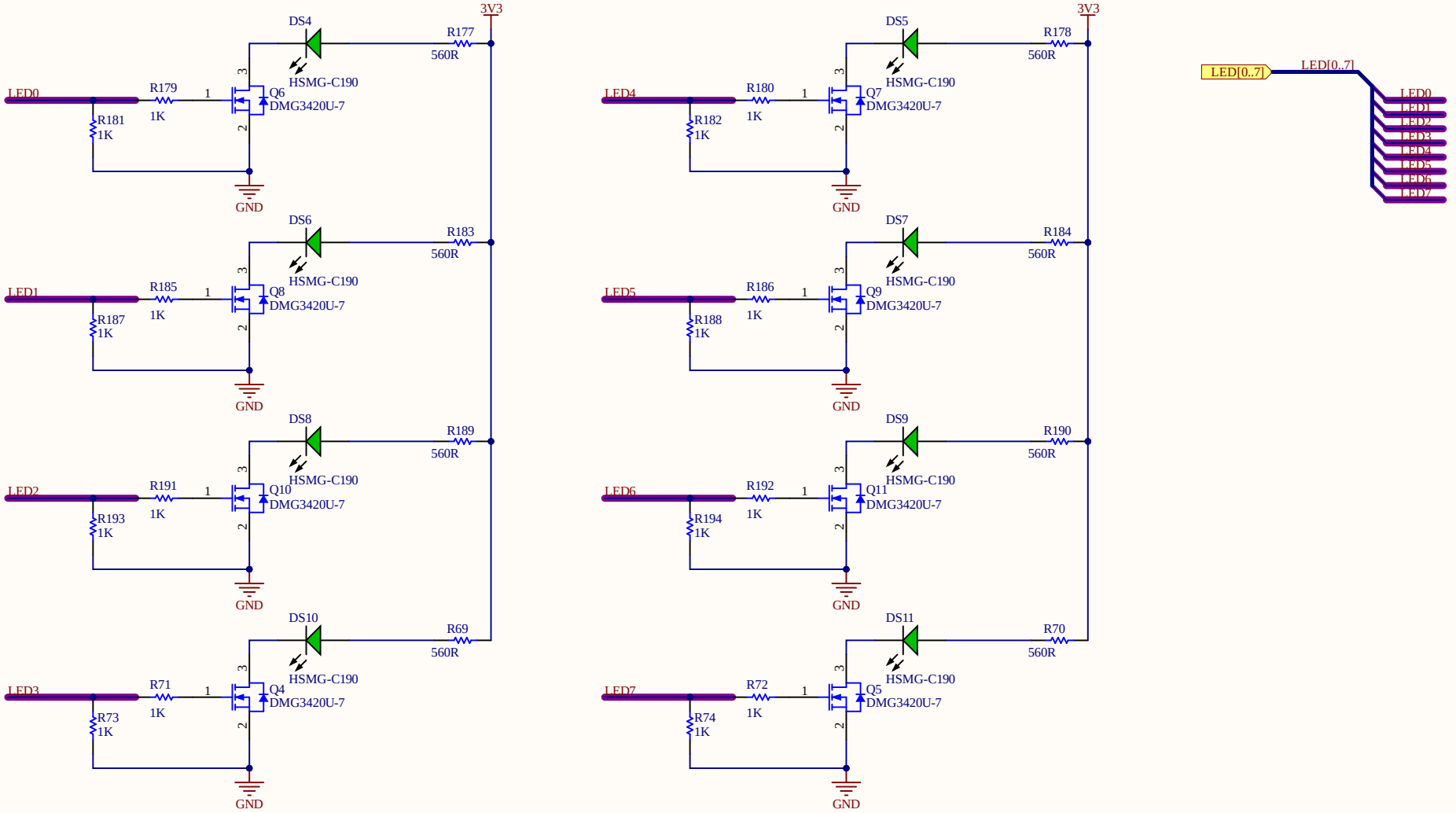
Title	**USB JTAG**	
Size: A3	Number:	Revision: **A**
Date: 2/28/2023		Sheet 9 of 15
File: C:\Users\..\USB JTAG.SchDoc		Drawn By: **Dragon Enjoyer**



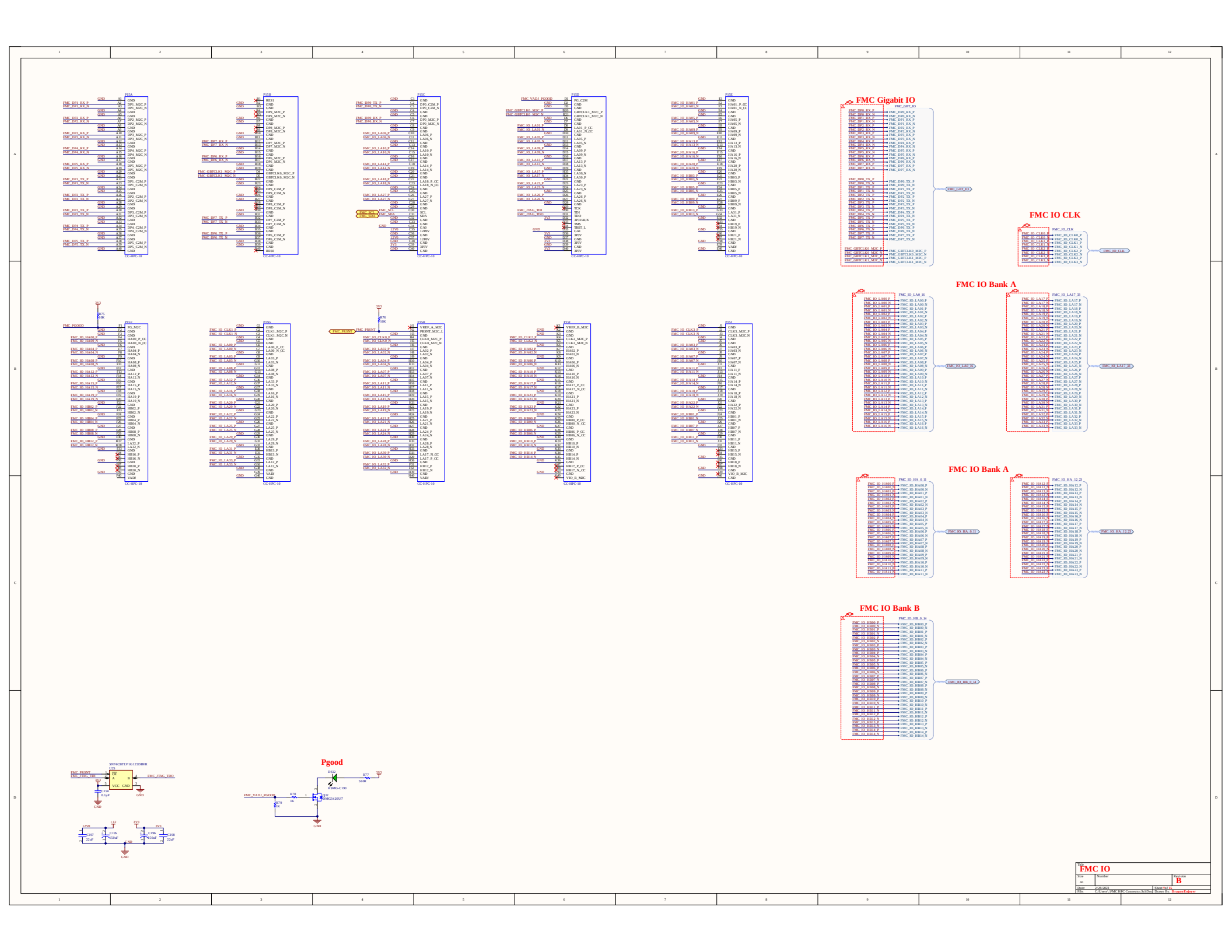
Title: **Fan Control**		
Size: A	Number:	Revision: **B**
Date: 2/28/2023		Sheet 10 of 15
File: C:\Users\..\Thermal Control.SchDoc		Drawn By: **Dragon Enjoyer**

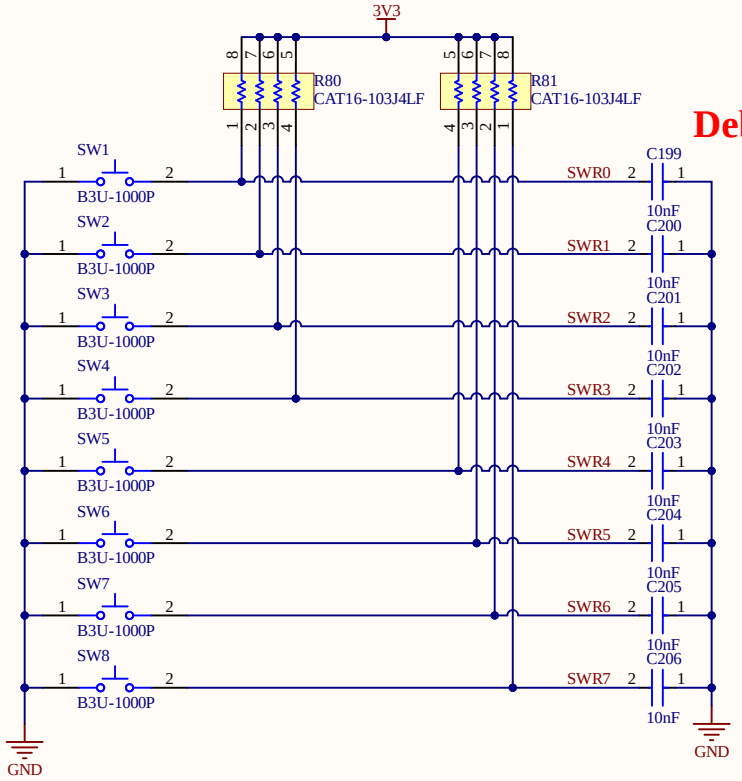


Title: **MicroSD**		
Size: A	Number:	Revision: **A**
Date: 2/28/2023		Sheet 11 of 15
File: C:\Users\..\FPGA microSD.SchDoc		Drawn By: **Dragon Enjoyer**

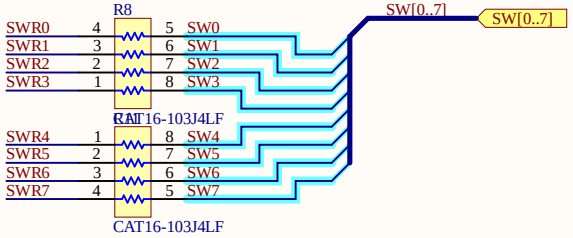


Title: **User LED's**		
Size: A4	Number:	Revision: **A**
Date: 2/28/2023		Sheet 12 of 15
File: C:\Users\..\LEDs.SchDoc		Drawn By: Dragon Enjoyer

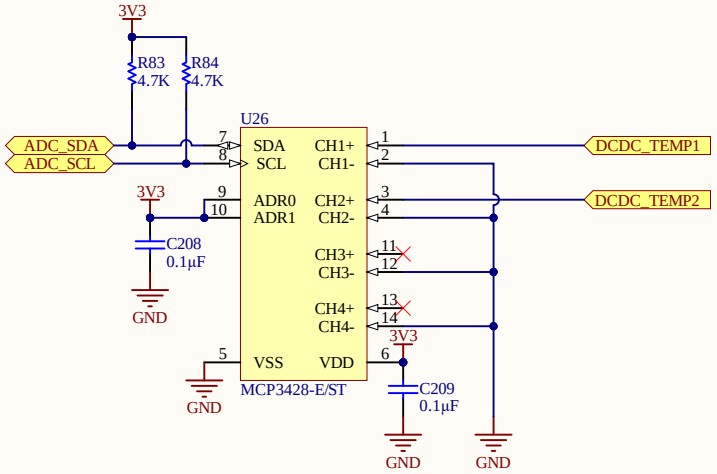

FMC Gigabit IO
FMC IO CLK
FMC IO Bank A
FMC IO Bank A
FMC IO Bank B
Pgood
FMC IO
Size
A1
Number
Revision
B
Date:
2/20/2021
Sheet 1 of 10
File:
C:\Users\...\FMC HPC Connector.SchDoc
Drawn By:
DragonEdgeer



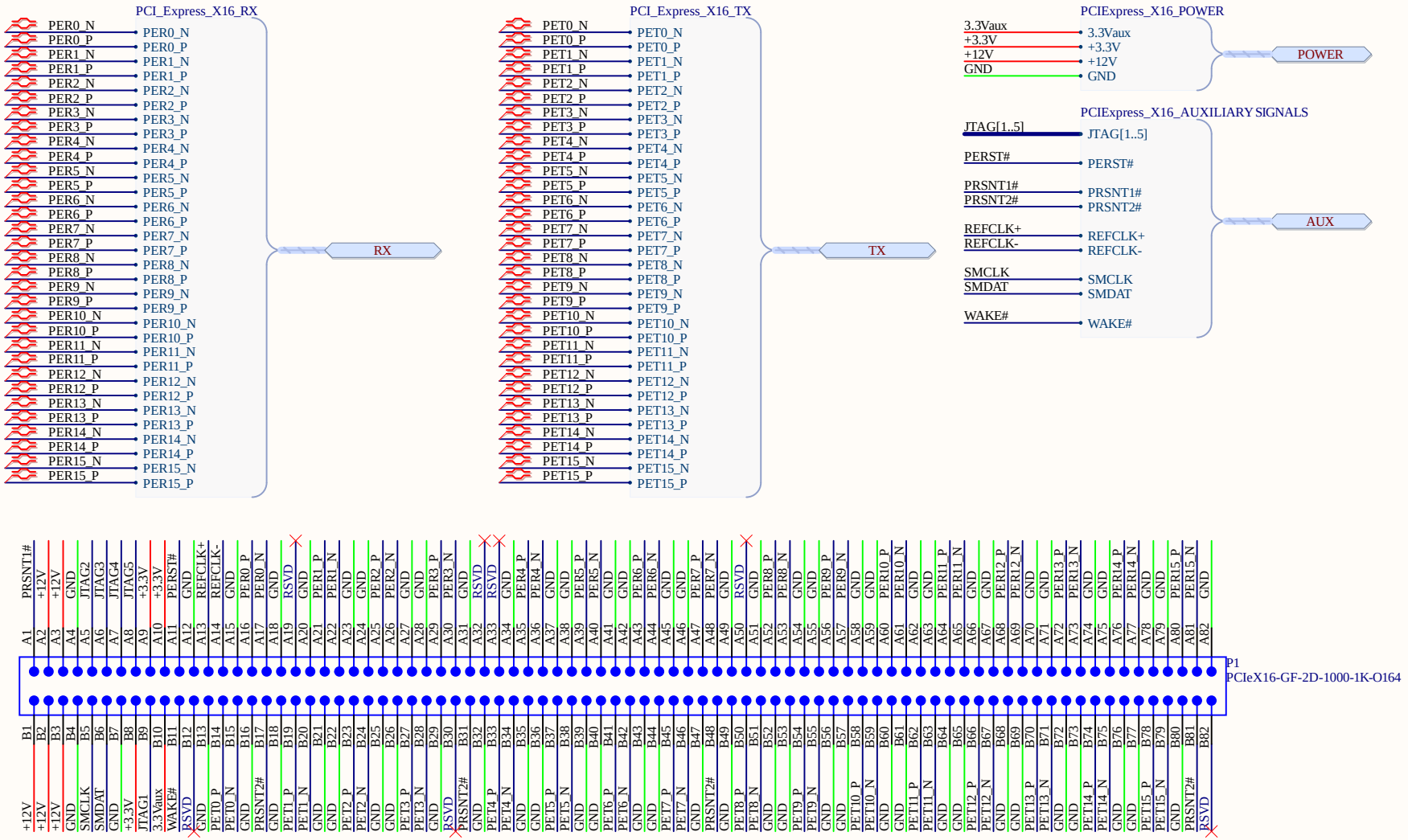
Debounce Caps



Title: **User Switches**		
Size: A4	Number:	Revision: **A**
Date: 2/28/2023		Sheet 14 of 15
File: C:\Users\..\Switches.SchDoc		Drawn By: Dragon Enjoyer



Title	**Temp SNS ADC**	
Size: A4	Number:	Revision: **A**
Date: 2/28/2023		Sheet 15 of 15
File: C:\Users\..\TempMonADC.SchDoc		Drawn By: **Dragon Enjoyer**



Sheet Title	***PCI Express x16 164Pin***		
Project Title	***PCI Express x16 Recommended Length card***		
Size: A4	Item:	Revision:	
Date: 2/28/2023	Time: 1:11:49 AM	Sheet * of *	
File: CON_PCI_Express_X16_164PIN.SchDoc			

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