AMD
XILINX

Artix UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics (DS931)

Revision History

Please Read: Important Legal Notices

Summary

The Xilinx® Artix® UltraScale+™ FPGAs are available in -2 and -1 speed grades, with -2E and -2I devices having the highest performance. The -1LI devices can operate at a V_{CCINT} voltage at 0.85V or 0.72V and provide lower maximum static power. When operated at V_{CCINT} = 0.85V, using a -1LI device, the speed specification for the L devices is the same as the -1I speed grade. When operated at V_{CCINT} = 0.72V, the -1LI performance and static and dynamic power is reduced.
DC and AC characteristics are specified in extended (E) and industrial (I) temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade extended device are the same as for a -1 speed grade industrial device). However, only selected speed grades and/or devices are available in each temperature range.
All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.
This data sheet, part of an overall set of documentation on the Artix UltraScale+ FPGAs, is available on the Xilinx website at www.xilinx.com/documentation .

DC Characteristics

Absolute Maximum Ratings

Table: Absolute Maximum Ratings

Symbol	Description [1]	Min	Max	Units
FPGA Logic				
V_{CCINT}	Internal supply voltage	–0.500	1.000	V
V_{CCINT_IO} [2]	Internal supply voltage for the I/O banks	–0.500	1.000	V
V_{CCAUX}	Auxiliary supply voltage	–0.500	2.000	V
V_{CCBRAM}	Supply voltage for the block RAM memories	–0.500	1.000	V
V_{CCO}	Output drivers supply voltage for HD I/O banks	–0.500	3.400	V
	Output drivers supply voltage for HP I/O banks	–0.500	2.000	V
V_{CCAUX_IO} [3]	Auxiliary supply voltage for the I/O banks	–0.500	2.000	V
V_{REF}	Input reference voltage	–0.500	2.000	V
V_{IN} [4, 5 , 6]	I/O input voltage for HD I/O banks	–0.550	V_{CCO} + 0.550	V

Symbol	Description [1]	Min	Max	Units
	I/O input voltage for HP I/O banks	–0.550	V_{CCO} + 0.550	V
V_{BATT}	Key memory battery backup supply	–0.500	2.000	V
I_{DC}	Available output current at the pad	–20	20	mA
I_{RMS}	Available RMS output current at the pad	–20	20	mA
GTH or GTY Transceiver [7]				
$V_{MGTAVCC}$	Analog supply voltage for transceiver circuits	–0.500	1.000	V
$V_{MGTAVTT}$	Analog supply voltage for transceiver termination circuits	–0.500	1.300	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers	–0.500	1.900	V
$V_{MGTREFCLK}$	Transceiver reference clock absolute input voltage	–0.500	1.300	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the transceiver column	–0.500	1.300	V
V_{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage	–0.500	1.200	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating [8]	–	10	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$	–	10	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND [9]	–	0	mA
$I_{DCIN-PROG}$	DC input current for receiver input pins DC coupled RX termination = programmable [10]	–	0	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating	–	6	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$	–	6	mA
System Monitor				
V_{CCADC}	System Monitor supply relative to GNDADC	–0.500	2.000	V

Symbol	Description [1]	Min	Max	Units
V_{REFP}	System Monitor reference input relative to GNDADC	–0.500	2.000	V
Temperature [11]				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum dry rework soldering temperature	–	260	°C
	Maximum reflow soldering temperature for SBVB484, SFVB784, and FFVB676 packages	–	250	°C
	Maximum reflow soldering temperature for UBVA368 package	–	245	°C
T_j	Maximum junction temperature	–	125	°C

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. V_{CCINT_IO} must be connected to V_{CCBRAM}.
3. V_{CCAUX_IO} must be connected to V_{CCAUX}.
4. The lower absolute voltage specification always applies.
5. For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
6. When operating outside of the recommended operating conditions, refer to Table 1 and Table 2 for maximum overshoot and undershoot specifications.
7. For more information on supported GTH or GTY transceiver terminations see the *UltraScale Architecture GTH Transceivers User Guide* (UG576) or *UltraScale Architecture GTY Transceivers User Guide* (UG578).
8. AC coupled operation is not supported for RX termination = floating.
9. For GTY transceivers, DC coupled operation is not supported for RX termination = GND.
10. DC coupled operation is not supported for RX termination = programmable.
11. For soldering guidelines and thermal considerations, see the *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification* (UG575).

Recommended Operating Conditions

Table: Recommended Operating Conditions

Symbol	Description [1, 2]	Min	Typ	Max	Units
FPGA Logic					

Symbol	Description [1, 2]	Min	Typ	Max	Units
V_{CCINT}	Internal supply voltage	0.825	0.850	0.876	V
	For -1LI (V_{CCINT} = 0.72V) devices: internal supply voltage	0.698	0.720	0.742	V
V_{CCINT_IO} [3]	Internal supply voltage for the I/O banks	0.825	0.850	0.876	V
	For -1LI (V_{CCINT} = 0.72V) devices: internal supply voltage for the I/O banks	0.825	0.850	0.876	V
V_{CCBRAM}	Block RAM supply voltage	0.825	0.850	0.876	V
V_{CCAUX}	Auxiliary supply voltage	1.746	1.800	1.854	V
V_{CCO} [4, 5]	Supply voltage for HD I/O banks	1.140	–	3.400	V
	Supply voltage for HP I/O banks	0.950	–	1.900	V
V_{CCAUX_IO} [6]	Auxiliary I/O supply voltage	1.746	1.800	1.854	V
V_{IN} [7]	I/O input voltage	– 0.200	–	V_{CCO} + 0.200	V
I_{IN} [8]	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode	–	–	10	mA
V_{BATT} [9]	Battery voltage	1.000	–	1.890	V
GTH or GTY Transceiver					
$V_{MGTAVCC}$ [10]	Analog supply voltage for the GTH or GTY transceiver	0.873	0.900	0.927	V
$V_{MGTAVTT}$ [10]	Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits	1.164	1.200	1.236	V
$V_{MGTVCCAUX}$ [10]	Auxiliary analog QPLL voltage supply for the transceivers	1.746	1.800	1.854	V
$V_{MGTAVTTRCAL}$ [10]	Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column	1.164	1.200	1.236	V
System Monitor					
V_{CCADC}	System Monitor supply relative to GNDADC	1.746	1.800	1.854	V
V_{REFP}	System Monitor externally supplied reference voltage relative to GNDADC	1.200	1.250	1.300	V

Symbol	Description [1, 2]	Min	Typ	Max	Units
Temperature					
T_j [11]	Junction temperature operating range for extended (E) temperature devices [12]	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C
	Junction temperature operating range for eFUSE programming [13]	–40	–	125	°C

1. All voltages are relative to GND, assuming supplies are present.
2. For the design of the power distribution system consult the *UltraScale Architecture PCB Design User Guide* (UG583).
3. V_{CCINT_IO} must be connected to V_{CCBRAM}.
4. For V_{CCO_0}, the recommended nominal operating voltage is 1.5V or 1.8V, and the minimum voltage for power on and during configuration is 1.425V. After configuration, data is retained even if V_{CCO} drops to 0V.
5. Includes V_{CCO} of 1.0V (HP I/O only), 1.2V, 1.35V, 1.5V, 1.8V, 2.5V (HD I/O only) at ±5%, and 3.3V (HD I/O only) at +3/–5%.
6. V_{CCAUX_IO} must be connected to V_{CCAUX}.
7. The lower absolute voltage specification always applies.
8. A total of 200 mA per bank should not be exceeded.
9. If battery is not used, connect V_{BATT} to either GND or V_{CCAUX}.
10. Each voltage listed requires filtering as described in the *UltraScale Architecture GTH Transceivers User Guide* (UG576) or the *UltraScale Architecture GTY Transceivers User Guide* (UG578) .
11. Xilinx recommends measuring the T_j of a device using the system monitor as described in the *UltraScale Architecture System Monitor User Guide* (UG580). The system monitor temperature measurement errors (that are described in Table 1) must be accounted for in your design. For example, when using the system monitor with an external reference of 1.25V, and when the system monitor reports 97°C, there is a measurement error ±3°C. A reading of 97°C is considered the maximum adjusted T_j (100°C – 3°C = 97°C).
12. Devices labeled with the speed/temperature grade of -2LE can operate for a limited time at a junction temperature between 100°C and 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation up to T_j = 110°C is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.
13. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).

DC Characteristics Over Recommended Operating Conditions

Table: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ [1]	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.68	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	µA
C_{IN} [3]	Die input capacitance at the pad (HP I/O)	–	–	3.1	pF
	Die input capacitance at the pad (HD I/O)	–	–	4.75	pF
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 3.3V	75	–	190	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 2.5V	50	–	169	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.8V	60	–	120	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.5V	30	–	120	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.2V	10	–	100	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V	60	–	200	µA
	Pad pull-down (when selected) at V_{IN} = 1.8V	29	–	120	µA
$I_{CCADCON}$	Analog supply current for the SYSMON circuits in the power-up state	–	–	8	mA
$I_{CCADCOFF}$	Analog supply current for the SYSMON circuits in the power-down state	–	–	1.5	mA
I_{BATT} [4, 5]	Battery supply current at V_{BATT} = 1.89V	–	–	650	nA
	Battery supply current at V_{BATT} = 1.20V	–	–	150	nA
I_{PFS} [6]	V_{CCAUX} additional supply current during eFUSE programming	–	–	115	mA

Symbol	Description	Min	Typ [1]	Max	Units
Internal V_{REF}	50% V_{CCO}	V_{CCO} x 0.49	V_{CCO} x 0.50	V_{CCO} x 0.51	V
	70% V_{CCO}	V_{CCO} x 0.69	V_{CCO} x 0.70	V_{CCO} x 0.71	V
Differential termination	Programmable differential termination (TERM_100) for HP I/O banks	–35%	100	+35%	Ω
n	Temperature diode ideality factor	–	1.026	–	–
r	Temperature diode series resistance	–	2	–	Ω
Calibrated programmable on-die termination (DCI) in HP I/O banks [7] (measured per JEDEC specification)					
R [9]	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_40	–10% [8]	40	+10% [8]	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_48	–10% [8]	48	+10% [8]	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_60	–10% [8]	60	+10% [8]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40	–10% [8]	40	+10% [8]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48	–10% [8]	48	+10% [8]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60	–10% [8]	60	+10% [8]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120	–10% [8]	120	+10% [8]	Ω
	Programmable input termination to $V_{CCO}$where ODT = RTT_240	–10% [8]	240	+10% [8]	Ω
Uncalibrated programmable on-die termination in HP I/Os banks (measured per JEDEC specification)					

Symbol	Description	Min	Typ [1]	Max	Units
R_{TT} [9]	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_40	–50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48	–50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_60	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40	–50%	40	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48	–50%	48	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120	–50%	120	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240	–50%	240	+50%	Ω
Uncalibrated programmable on-die termination in HD I/O banks (measured per JEDEC specification)					
R_{TT} [9]	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48	–50%	48	+50%	Ω

Symbol	Description	Min	Typ [1]	Max	Units

1. Typical values are specified at nominal voltage, 25°C.
2. For the HP I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 μA.
3. This measurement represents the die capacitance at the pad, not including the package.
4. Maximum value specified for worst case process at 25°C.
5. I_{BATT} is measured when the battery-backed RAM (BBRAM) is enabled.
6. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).
7. VRP resistor tolerance is (240Ω ±1%).
8. If VRP resides at a different bank (DCI cascade), the range increases to ±15%.
9. On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

VIN Maximum Allowed AC Voltage Overshoot and Undershoot

Table: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HD I/O Banks

AC Voltage Overshoot	% of UI [1] [2] at –40°C to 100°C	AC Voltage Undershoot	% of UI [1] [2] at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	90%
V_{CCO} + 0.40	100%	–0.40	78%
V_{CCO} + 0.45	100%	–0.45	40%
V_{CCO} + 0.50	100%	–0.50	24%
V_{CCO} + 0.55	100%	–0.55	18.0%
V_{CCO} + 0.60	100%	–0.60	13.0%
V_{CCO} + 0.65	100%	–0.65	10.8%
V_{CCO} + 0.70	92%	–0.70	9.0%
V_{CCO} + 0.75	92%	–0.75	7.0%
V_{CCO} + 0.80	92%	–0.80	6.0%
V_{CCO} + 0.85	92%	–0.85	5.0%
V_{CCO} + 0.90	92%	–0.90	4.0%

AC Voltage Overshoot	% of UI [1] [2] at –40°C to 100°C	AC Voltage Undershoot	% of UI [1] [2] at –40°C to 100°C
V_{CCO} + 0.95	92%	–0.95	2.5%

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Table: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks

AC Voltage Overshoot	% of UI [1] [2] at –40°C to 100°C	AC Voltage Undershoot	% of UI [1] [2] at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	100%
V_{CCO} + 0.40	92%	–0.40	92%
V_{CCO} + 0.45	50%	–0.45	50%
V_{CCO} + 0.50	20%	–0.50	20%
V_{CCO} + 0.55	10%	–0.55	10%
V_{CCO} + 0.60	6%	–0.60	6%
V_{CCO} + 0.65	2%	–0.65	2%
V_{CCO} + 0.70	2%	–0.70	2%

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Quiescent Supply Current

Table: Typical Quiescent Supply Current

Symbol	Description [1, 2, 3]	Device	Speed Grade and V_{CCINT} Operating Voltages			Units
			0.85V		0.72V	
			-2	-1	-1	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XCAU10P	424	424	372	mA
		XCAU15P	424	424	372	mA
		XCAU20P	1181	1181	1037	mA
		XCAU25P	1181	1181	1037	mA

Symbol	Description [1, 2, 3]	Device	Speed Grade and V_{CCINT} Operating Voltages			Units
			0.85V		0.72V	
			-2	-1	-1	
I_{CCINT_IOQ}	Quiescent V_{CCINT_IO} supply current	XCAU10P	44	44	44	mA
		XCAU15P	44	44	44	mA
		XCAU20P	59	59	59	mA
		XCAU25P	59	59	59	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	All devices	1	1	1	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XCAU10P	55	55	55	mA
		XCAU15P	55	55	55	mA
		XCAU20P	153	153	153	mA
		XCAU25P	153	153	153	mA
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current	XCAU10P	24	24	24	mA
		XCAU15P	24	24	24	mA
		XCAU20P	32	32	32	mA
		XCAU25P	32	32	32	mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XCAU10P	5	5	5	mA
		XCAU15P	5	5	5	mA
		XCAU20P	17	17	17	mA
		XCAU25P	17	17	17	mA

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, and all I/O pins are 3-state and floating.
3. Use the Xilinx® Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate static power consumption for conditions or supplies other than those specified.

Power Supply Sequencing

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCINT_IO}/V_{CCBRAM} , V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM}. If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.
The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

Power Supply Requirements

Table 1 shows the minimum current, in addition to I_{CCQ} maximum, required by each Artix UltraScale+ FPGA for proper power-on and configuration. If these current minimums are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) to estimate current drain on these supplies. The XPE tool (download at https://www.xilinx.com/power) is also used to estimate power-on current for all supplies.

Table: Power-on Current by Device

Device	$I_{CCINTMIN}$	$I_{CCBRAMMIN}$ + I_{CCINT_IOMIN}	I_{CCOMIN}	$I_{CCAUXMIN}$ + I_{CCAUX_IOMIN}	Units
XCAU10P	I_{CCINTQ} + 770	$I_{CCBRAMQ}$ + I_{CCINT_IOQ} + 409	I_{CCOQ} + 50	I_{CCAUXQ} + I_{CCAUX_IOQ} + 386	mA
XCAU15P	I_{CCINTQ} + 770	$I_{CCBRAMQ}$ + I_{CCINT_IOQ} + 409	I_{CCOQ} + 50	I_{CCAUXQ} + I_{CCAUX_IOQ} + 386	mA
XCAU20P	I_{CCINTQ} + 770	$I_{CCBRAMQ}$ + I_{CCINT_IOQ} + 476	I_{CCOQ} + 50	I_{CCAUXQ} + I_{CCAUX_IOQ} + 515	mA
XCAU25P	I_{CCINTQ} + 770	$I_{CCBRAMQ}$ + I_{CCINT_IOQ} + 476	I_{CCOQ} + 50	I_{CCAUXQ} + I_{CCAUX_IOQ} + 515	mA

Table: Power Supply Ramp Time

Symbol	Description	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 95% of V_{CCINT}	0.2	40	ms
T_{VCCINT_IO}	Ramp time from GND to 95% of V_{CCINT_IO}	0.2	40	ms

Symbol	Description	Min	Max	Units
T_{VCCO}	Ramp time from GND to 95% of V_{CCO}	0.2	40	ms
T_{VCCAUX}	Ramp time from GND to 95% of V_{CCAUX}	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 95% of V_{CCBRAM}	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 95% of $V_{MGTAVCC}$	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 95% of $V_{MGTAVTT}$	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 95% of $V_{MGTVCCAUX}$	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

I/O Levels

Table: SelectIO DC Input and Output Levels For HD I/O Banks

I/O Standard [1, 2]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.0	–8.0
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.0	–8.0
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 4	Note 4
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 4	Note 4

I/O Standard [1, 2]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS25	–0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS33	–0.300	0.800	2.000	3.400	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVTTL	–0.300	0.800	2.000	3.400	0.400	2.400	Note 4	Note 4
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	14.25	–14.25
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	8.9	–8.9
SSTL135_II	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	13.0	–13.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175	8.9	–8.9
SSTL15_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175	13.0	–13.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.470	$V_{CCO}/2$ + 0.470	8.0	–8.0
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.600	$V_{CCO}/2$ + 0.600	13.4	–13.4

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. Supported drive strengths of 4, 8, or 12 mA in HD I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HD I/O banks.

Table: SelectIO DC Input and Output Levels for HP I/O Banks

I/O Standard [1, 2, 3]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	5.8	–5.8

I/O Standard [1, 2, 3]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	4.1	–4.1
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	6.2	–6.2
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	8.0	–8.0
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	9.0	–9.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175	10.0	–10.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.470	$V_{CCO}/2$ + 0.470	7.0	–7.0
MIPI_DPHY_DCI_LP [6]	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

I/O Standard [1, 2, 3]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 3, Table 8, and Table 9.
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table: DC Input Levels for Single-ended POD10 and POD12 I/O Standards

I/O Standard [1, 2]	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300
POD12	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table: Differential SelectIO DC Input and Output Levels

I/O Standard	V_{ICM} (V) [1]			V_{ID} (V) [2]			V_{ILHS} [3]	V_{IHHS} [3]	V_{OCM} (V) [4]			V_{OD} (V) [5]		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
SUB_LVDS [8]	0.500	0.900	1.300	0.070	–	–	–	–	0.700	0.900	1.100	0.100	0.150	0.200
LVPECL	0.300	1.200	1.425	0.100	0.350	0.600	–	–	–	–	–	–	–	–
SLVS_400_18	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
SLVS_400_25	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
MIPI_DPHY_DCI_HS [9]	0.070	–	0.330	0.070	–	–	– 0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270

I/O Standard	V_{ICM} (V) [1]			V_{ID} (V) [2]			V_{ILHS} [3]	V_{IHHS} [3]	V_{OCM} (V) [4]			V_{OD} (V) [5]		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
4. V_{OCM} is the output common mode voltage.
5. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
6. LVDS_25 is specified in Table 1.
7. LVDS is specified in Table 1.
8. The SUB_LVDS receiver is supported in HP I/O and HD I/O banks. The SUB_LVDS transmitter is supported only in HP I/O banks.
9. High-speed option for MIPI_DPHY_DCI. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.

Table: Complementary Differential SelectIO DC Input and Output Levels for HD I/O Banks

I/O Standard	V_{ICM} (V) [1]			V_{ID} (V) [2]		V_{OL} (V) [3]	V_{OH} (V) [4]	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL135_II	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL15_II	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.0	–8.0

I/O Standard	V_{ICM} (V) [1]			V_{ID} (V) [2]		V_{OL} (V) [3]	V_{OH} (V) [4]	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	$(V_{CCO}/2) – 0.600$	$(V_{CCO}/2) + 0.600$	13.4	–13.4

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table: Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks

I/O Standard [1]	V_{ICM} (V) [2]			V_{ID} (V) [3]		V_{OL} (V) [4]	V_{OH} (V) [5]	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	0.400	$V_{CCO} – 0.400$	5.8	–5.8
DIFF_HSTL_I_12	0.400 x V_{CCO}	$V_{CCO}/2$	0.600 x V_{CCO}	0.100	–	0.250 x V_{CCO}	0.750 x V_{CCO}	4.1	–4.1
DIFF_HSTL_I_18	$(V_{CCO}/2) – 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	0.400	$V_{CCO} – 0.400$	6.2	–6.2
DIFF_HSUL_12	$(V_{CCO}/2) – 0.120$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.120$	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL12	$(V_{CCO}/2) – 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) – 0.150$	$(V_{CCO}/2) + 0.150$	8.0	–8.0
DIFF_SSTL135	$(V_{CCO}/2) – 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) – 0.150$	$(V_{CCO}/2) + 0.150$	9.0	–9.0
DIFF_SSTL15	$(V_{CCO}/2) – 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) – 0.175$	$(V_{CCO}/2) + 0.175$	10.0	–10.0
DIFF_SSTL18_I	$(V_{CCO}/2) – 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) – 0.470$	$(V_{CCO}/2) + 0.470$	7.0	–7.0

I/O Standard [1]	V_{ICM} (V) [2]			V_{ID} (V) [3]		V_{OL} (V) [4]	V_{OH} (V) [5]	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in Table 7, Table 8, and Table 9.
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table: DC Input Levels for Differential POD10 and POD12 I/O Standards

I/O Standard [1, 2]	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.63	0.70	0.77	0.14	–
DIFF_POD12	0.76	0.84	0.92	0.16	–

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table: DC Output Levels for Single-ended and Differential POD10 and POD12 Standards

Symbol	Description [1, 2]	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance	V_{OM_DC} (as described in Table 9)	36	40	44	Ω
R_{OH}	Pull-up resistance	V_{OM_DC} (as described in Table 9)	36	40	44	Ω

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table: Definitions for DC Output Levels for Single-ended and Differential POD10 and POD12 Standards

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity)	0.8 x V_{CCO}	V

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HD I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

Table: LVDS_25 DC Specifications

Symbol	DC Parameter	Min	Typ	Max	Units
V_{CCO} [1]	Supply voltage	2.375	2.500	2.625	V
V_{IDIFF}	Differential input voltage: $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High	100	350	600 [2]	mV
V_{ICM}	Input common-mode voltage	0.300	1.200	1.425	V

1. LVDS_25 in HD I/O banks supports inputs only. LVDS_25 inputs without internal termination have no V_{CCO} requirements. Any V_{CCO} can be chosen as long as the input voltage levels do not violate the *Recommended Operating Condition* (Table 1) specification for the V_{IN} I/O pin voltage.
2. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

Table: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO} [1]	Supply voltage		1.710	1.800	1.890	V
V_{ODIFF} [2]	Differential output voltage: $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	454	mV
V_{OCM} [2]	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF} [3]	Differential input voltage: $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High		100	350	600 [3]	mV

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{ICM_DC} [4]	Input common-mode voltage (DC coupling)		0.300	1.200	1.425	V
V_{ICM_AC} [5]	Input common-mode voltage (AC coupling)		0.600	–	1.100	V

1. In HP I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the Recommended Operating Condition (Table 1) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in the following table.

Table: Speed Specification Version By Device

2022.1	Device
1.28	XCAU20P, XCAU25P
1.29	XCAU10P, XCAU15P

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Artix UltraScale+ FPGAs.

Speed Grade Designations

Because individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 1 correlates the current status of the Artix UltraScale+ FPGAs on a per speed grade basis.

Table: Speed Grade Designations by Device

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCAU10P [1]			-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) [2] -1LI (V_{CCINT} = 0.72V) [2]
XCAU15P [1]			-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) [2] -1LI (V_{CCINT} = 0.72V) [2]

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCAU20P			-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) [2] -1LI (V_{CCINT} = 0.72V) [2]
XCAU25P			-2E (V_{CCINT} = 0.85V), -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) [2] -1LI (V_{CCINT} = 0.72V) [2]

1. The XCAU10P and XCAU15P in the UBVA368 package is pending characterization.
2. The lowest power -1L devices, where V_{CCINT} = 0.72V, are listed in the Vivado Design Suite as -1LV. Otherwise, the -1L devices, where V_{CCINT} = 0.85V, are listed in the Vivado Design Suite as -1L.

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.
Table 1 lists the production released Artix UltraScale+ FPGA, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table: Artix UltraScale+ FPGA Device Production Software and Speed Specification Release

Device	Speed Grade and V_{CCINT} Operating Voltages			
	0.85V			0.72V
	-2	-1	-1L	-1L
XCAU10P [1]	Vivado tools 2022.1 v1.29	Vivado tools 2022.1 v1.29	Vivado tools 2022.1 v1.29	Vivado tools 2022.1 v1.29

Device	Speed Grade and V_{CCINT} Operating Voltages			
	0.85V			0.72V
	-2	-1	-1L	-1L
XCAU15P [1]	Vivado tools 2022.1 v1.29	Vivado tools 2022.1 v1.29	Vivado tools 2022.1 v1.29	Vivado tools 2022.1 v1.29
XCAU20P	Vivado tools 2021.2 v1.28	Vivado tools 2021.2 v1.28	Vivado tools 2021.2 v1.28	Vivado tools 2021.2 v1.28
XCAU25P	Vivado tools 2021.1.1 v1.28	Vivado tools 2021.1.1 v1.28	Vivado tools 2021.1.1 v1.28	Vivado tools 2021.2 v1.28

1. The XCAU10P and XCAU15P in the UBVA368 package is pending characterization.

FPGA Logic Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the Artix UltraScale+ FPGAs. These values are subject to the same guidelines as the AC Switching Characteristics section.
In each of the following LVDS performance tables, the I/O bank type is either high performance (HP) or high density (HD).
In LVDS component mode:

- For the input/output registers in HP I/O banks, the Vivado tools limit clock frequencies to 312.9 MHz for all speed grades.
- For IDDR in HP I/O banks, Vivado tools limit clock frequencies to 625.0 MHz for all speed grades.
- For ODDR in HP I/O banks, Vivado tools limit clock frequencies to 625.0 MHz for all speed grades.

Table: LVDS Component Mode Performance

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages						Units
		0.85V				0.72V		
		-2		-1		-1		
		Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	HP	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	HP	0	625	0	625	0	625	Mb/s

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages						Units
		0.85V				0.72V		
		-2		-1		-1		
		Min	Max	Min	Max	Min	Max	
LVDS RX DDR (ISERDES 1:4, 1:8) [1]	HP	0	1250	0	1250	0	1250	Mb/s
LVDS RX DDR	HD	0	250	0	250	0	250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4) [1]	HP	0	625	0	625	0	625	Mb/s
LVDS RX SDR	HD	0	125	0	125	0	125	Mb/s

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table: LVDS Native Mode Performance

Description [1, 2]	DATA_WIDTH	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages						Units
			0.85V				0.72V		
			-2 [3]		-1 [3]		-1 [3]		
			Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	HP	375	1600	375	1600	375	1260	Mb/s
	8		375	1600	375	1600	375	1600	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	HP	187.5	800	187.5	800	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	800	Mb/s
LVDS RX DDR (RX_BITSLICE) [4]	4	HP	375	1600 [5]	375	1600 [5]	375	1260 [5]	Mb/s
	8		375	1600 [5]	375	1600 [5]	375	1600 [5]	Mb/s
LVDS RX SDR (RX_BITSLICE) [4]	4	HP	187.5	800	187.5	800	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	800	Mb/s

Description [1, 2]	DATA_WIDTH	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages						Units
			0.85V				0.72V		
			-2 [3]		-1 [3]		-1 [3]		
			Min	Max	Min	Max	Min	Max	

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite. The performance values assume a source-synchronous interface.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_F_{VCOMIN}/2.
3. In the UBVA368 and SBVB484 packages, the maximum data rate is 1260 Mb/s for DDR interfaces and 630 Mb/s for SDR interfaces.
4. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.
5. Asynchronous receiver performance is limited to 1300 Mb/s for -2 speed grades and to 1250 Mb/s for -1 speed grades.

Table: MIPI D-PHY Performance

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
Maximum MIPI D-PHY transmitter or receiver data rate per lane	HP	2500	2500	1260	Mb/s
	All devices in UBVA368 and SBVB484 packages	1260	1260	1260	Mb/s

Table: LVDS Native-Mode 1000BASE-X Support

Description [1]	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages		
		0.85V		0.72V
		-2	-1	-1
1000BASE-X	HP	Yes		

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

The following table provides the maximum data rates for applicable memory standards using the Artix UltraScale+ FPGA memory PHY. Refer to Memory Interfaces for the complete list of memory interface

standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design User Guide* (UG583), electrical analysis, and characterization of the system.

Table: Maximum Physical Interface (PHY) Rate for Memory Interfaces

Memory Standard	Packages	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages			Units
			0.85V		0.72V	
			-2	-1	-1	
DDR4	FFVB676 packages	Single rank component	2400	2133	1866	Mb/s
		1 rank DIMM [1, 2]	2133	1866	1600	Mb/s
		2 rank DIMM [1, 3]	1866	1600	1333	Mb/s
		4 rank DIMM [1, 4]	1333	N/A	N/A	Mb/s
	SFVB784 packages	Single rank component	2400	2133	1866	Mb/s
		1 rank DIMM [1, 2]	2133	1866	1600	Mb/s
		2 rank DIMM [1, 3]	1866	1600	1333	Mb/s
		4 rank DIMM [1, 4]	1333	N/A	N/A	Mb/s
	SBVB484 and UBVA368 packages	Single rank component	1600	1600	1600	Mb/s
		1 rank DIMM [1, 2]	1333	1333	1333	Mb/s
		2 rank DIMM [1, 3]	1333	1333	N/A	Mb/s
DDR3	FFVB676 packages	Single rank component	1866	1866	1600	Mb/s
		1 rank DIMM [1, 2]	1600	1600	1600	Mb/s
		2 rank DIMM [1, 3]	1600	1600	1333	Mb/s
		4 rank DIMM [1, 4]	1066	1066	800	Mb/s
	SFVB784 packages	Single rank component	1866	1866	1600	Mb/s
		1 rank DIMM [1, 2]	1600	1600	1600	Mb/s
		2 rank DIMM [1, 3]	1600	1600	1333	Mb/s

Memory Standard	Packages	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages			Units
			0.85V		0.72V	
			-2	-1	-1	
		4 rank DIMM [1, 4]	1066	1066	800	Mb/s
	SBVB484 and UBVA368 packages	Single rank component	1600	1600	1333	Mb/s
		1 rank DIMM [1, 2]	1333	1333	1066	Mb/s
		2 rank DIMM [1, 3]	1333	1333	800	Mb/s
		4 rank DIMM [1, 4]	800	800	N/A	Mb/s
DDR3L	FFVB676 packages	Single rank component	1600	1600	1600	Mb/s
		1 rank DIMM [1, 2]	1600	1600	1333	Mb/s
		2 rank DIMM [1, 3]	1333	1333	1066	Mb/s
		4 rank DIMM [1, 4]	800	800	606	Mb/s
	SFVB784 packages	Single rank component	1600	1600	1600	Mb/s
		1 rank DIMM [1, 2]	1600	1600	1333	Mb/s
		2 rank DIMM [1, 3]	1333	1333	1066	Mb/s
		4 rank DIMM [1, 4]	800	800	606	Mb/s
	SBVB484 and UBVA368 packages	Single rank component	1333	1333	1066	Mb/s
		1 rank DIMM [1, 2]	1066	1066	800	Mb/s
		2 rank DIMM [1, 3]	800	800	606	Mb/s
		4 rank DIMM [1, 4]	N/A	N/A	N/A	Mb/s
QDR II+	All	Single rank component [5]	633	600	550	MHz
QDR IV XP	FFVB676 and SFVB784 packages	Single rank component	1066	1066	933	MHz

Memory Standard	Packages	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages			Units
			0.85V		0.72V	
			-2	-1	-1	
	SBVB484 and UBVA368 packages	Single rank component	800	800	800	MHz
RLDRAM 3	FFVB676 packages	Single rank component	1066	1066	933	MHz
	SFVB784 packages	Single rank component	1066	933	800	MHz
	SBVB484 and UBVA368 packages	Single rank component	933	800	667	MHz
LPDDR3	FFVB676	Single rank component	1600	1600	1600	Mb/s
	SFVB784	Single rank component	1600	1600	1600	Mb/s
	SBVB484 and UBVA368	Single rank component	1600	1600	1600	Mb/s

1. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
2. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
3. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
4. Includes: 2 rank 2 slot, 4 rank 1 slot.
5. The QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.

FPGA Logic Switching Characteristics

The following IOB high-density (HD) and IOB high-performance (HP) tables summarize the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{INBUF\_DELAY\_PAD\_I}$ is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{OUTBUF\_DELAY\_O\_PAD}$ is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{OUTBUF\_DELAY\_TD\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{OUTBUF\_DELAY\_TD\_PAD}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the on-die termination turn-on time is always faster than $T_{OUTBUF\_DELAY\_TD\_PAD}$ when the INTERMDISABLE pin is used.

IOB High Density (HD) Switching Characteristics

Table: IOB High Density (HD) Switching Characteristics

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$			$T_{OUTBUF\_DELAY\_O\_PAD}$			$T_{OUTBUF\_DELAY\_TD\_PAD}$			Units
	0.85V		0.72V	0.85V		0.72V	0.85V		0.72V	
	-2	-1	-1	-2	-1	-1	-2	-1	-1	
DIFF_HSTL_I_18_F	0.978	1.058	1.058	1.574	1.718	2.101	1.160	1.271	1.544	ns
DIFF_HSTL_I_18_S	0.978	1.058	1.058	1.805	1.950	2.333	1.748	1.867	2.104	ns
DIFF_HSTL_I_F	0.978	1.058	1.058	1.611	1.762	2.145	1.313	1.417	1.668	ns
DIFF_HSTL_I_S	0.978	1.058	1.058	1.798	1.913	2.296	1.630	1.780	1.986	ns
DIFF_HSUL_12_F	0.911	0.977	0.977	1.573	1.703	2.086	1.222	1.335	1.578	ns
DIFF_HSUL_12_S	0.911	0.977	0.977	1.711	1.864	2.247	1.536	1.665	1.891	ns
DIFF_SSTL12_F	0.906	0.977	0.977	1.643	1.792	2.175	1.285	1.423	1.640	ns
DIFF_SSTL12_S	0.906	0.977	0.977	1.784	1.948	2.331	1.567	1.706	1.922	ns
DIFF_SSTL135_F	0.927	0.995	0.995	1.625	1.765	2.148	1.341	1.458	1.696	ns
DIFF_SSTL135_II_F	0.927	0.995	0.995	1.623	1.770	2.153	1.325	1.470	1.689	ns
DIFF_SSTL135_II_S	0.927	0.995	0.995	1.768	1.916	2.299	1.722	1.911	2.078	ns
DIFF_SSTL135_S	0.927	0.995	0.995	1.869	2.025	2.408	1.814	1.976	2.169	ns
DIFF_SSTL15_F	0.928	1.020	1.020	1.628	1.771	2.154	1.374	1.483	1.729	ns
DIFF_SSTL15_II_F	0.928	1.020	1.020	1.622	1.778	2.161	1.356	1.442	1.712	ns
DIFF_SSTL15_II_S	0.928	1.020	1.020	1.821	1.987	2.370	1.895	2.047	2.250	ns
DIFF_SSTL15_S	0.928	1.020	1.020	1.824	1.977	2.360	1.743	1.907	2.098	ns

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$			$T_{OUTBUF\_DELAY\_O\_PAD}$			$T_{OUTBUF\_DELAY\_TD\_PAD}$			Units
	0.85V		0.72V	0.85V		0.72V	0.85V		0.72V	
	-2	-1	-1	-2	-1	-1	-2	-1	-1	
DIFF_SSTL18_II_F	0.961	1.038	1.038	1.729	1.880	2.263	1.377	1.492	1.732	ns
DIFF_SSTL18_II_S	0.961	1.038	1.038	1.796	1.965	2.348	1.616	1.800	1.972	ns
DIFF_SSTL18_I_F	0.961	1.038	1.038	1.609	1.755	2.138	1.220	1.313	1.575	ns
DIFF_SSTL18_I_S	0.961	1.038	1.038	1.786	1.942	2.325	1.677	1.836	2.033	ns
HSTL_I_18_F	0.947	1.021	1.021	1.574	1.718	2.101	1.160	1.271	1.544	ns
HSTL_I_18_S	0.947	1.021	1.021	1.805	1.950	2.333	1.748	1.867	2.104	ns
HSTL_I_F	0.856	0.900	0.900	1.611	1.762	2.145	1.313	1.417	1.668	ns
HSTL_I_S	0.856	0.900	0.900	1.798	1.913	2.296	1.630	1.780	1.986	ns
HSUL_12_F	0.780	0.867	0.867	1.573	1.703	2.086	1.222	1.335	1.578	ns
HSUL_12_S	0.780	0.867	0.867	1.711	1.864	2.247	1.536	1.665	1.891	ns
LVCMOS12_F_12	0.918	0.976	0.976	1.689	1.856	2.239	1.202	1.317	1.557	ns
LVCMOS12_F_4	0.918	0.976	0.976	1.742	1.922	2.305	1.353	1.478	1.708	ns
LVCMOS12_F_8	0.918	0.976	0.976	1.714	1.879	2.262	1.292	1.432	1.647	ns
LVCMOS12_S_12	0.918	0.976	0.976	2.073	2.247	2.630	1.581	1.717	1.937	ns
LVCMOS12_S_4	0.918	0.976	0.976	1.979	2.182	2.565	1.633	1.772	1.989	ns
LVCMOS12_S_8	0.918	0.976	0.976	2.205	2.406	2.789	1.767	1.928	2.123	ns
LVCMOS15_F_12	0.905	0.958	0.958	1.713	1.892	2.275	1.275	1.428	1.630	ns
LVCMOS15_F_16	0.905	0.958	0.958	1.722	1.881	2.264	1.260	1.407	1.615	ns
LVCMOS15_F_4	0.905	0.958	0.958	1.825	1.959	2.342	1.453	1.557	1.809	ns
LVCMOS15_F_8	0.905	0.958	0.958	1.778	1.930	2.313	1.378	1.458	1.733	ns
LVCMOS15_S_12	0.905	0.958	0.958	1.991	2.139	2.522	1.516	1.648	1.871	ns
LVCMOS15_S_16	0.905	0.958	0.958	2.172	2.389	2.772	1.707	1.888	2.062	ns
LVCMOS15_S_4	0.905	0.958	0.958	2.313	2.483	2.866	1.952	2.123	2.307	ns
LVCMOS15_S_8	0.905	0.958	0.958	2.170	2.400	2.783	1.817	1.984	2.173	ns
LVCMOS18_F_12	0.915	0.958	0.958	1.805	1.962	2.345	1.383	1.471	1.738	ns
LVCMOS18_F_16	0.915	0.958	0.958	1.785	1.917	2.300	1.338	1.446	1.693	ns

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$			$T_{OUTBUF\_DELAY\_O\_PAD}$			$T_{OUTBUF\_DELAY\_TD\_PAD}$			Units
	0.85V		0.72V	0.85V		0.72V	0.85V		0.72V	
	-2	-1	-1	-2	-1	-1	-2	-1	-1	
LVCMOS18_F_4	0.915	0.958	0.958	1.868	2.013	2.396	1.472	1.599	1.832	ns
LVCMOS18_F_8	0.915	0.958	0.958	1.797	1.979	2.362	1.384	1.487	1.739	ns
LVCMOS18_S_12	0.915	0.958	0.958	2.201	2.408	2.791	1.762	1.894	2.118	ns
LVCMOS18_S_16	0.915	0.958	0.958	2.173	2.362	2.745	1.702	1.834	2.057	ns
LVCMOS18_S_4	0.915	0.958	0.958	2.346	2.567	2.950	1.951	2.092	2.306	ns
LVCMOS18_S_8	0.915	0.958	0.958	2.292	2.511	2.894	1.848	2.008	2.204	ns
LVCMOS25_F_12	0.988	1.042	1.042	2.153	2.453	2.836	1.692	1.856	2.047	ns
LVCMOS25_F_16	0.988	1.042	1.042	2.105	2.406	2.789	1.623	1.786	1.979	ns
LVCMOS25_F_4	0.988	1.042	1.042	2.344	2.554	2.937	1.842	2.039	2.197	ns
LVCMOS25_F_8	0.988	1.042	1.042	2.184	2.516	2.899	1.726	1.910	2.081	ns
LVCMOS25_S_12	0.988	1.042	1.042	2.558	2.840	3.223	1.971	2.194	2.327	ns
LVCMOS25_S_16	0.988	1.042	1.042	2.449	2.740	3.123	1.852	2.063	2.207	ns
LVCMOS25_S_4	0.988	1.042	1.042	2.770	3.066	3.449	2.224	2.458	2.579	ns
LVCMOS25_S_8	0.988	1.042	1.042	2.663	2.963	3.346	2.091	2.373	2.446	ns
LVCMOS33_F_12	1.154	1.213	1.213	2.415	2.651	3.034	1.754	1.915	2.109	ns
LVCMOS33_F_16	1.154	1.213	1.213	2.383	2.603	2.986	1.734	1.869	2.089	ns
LVCMOS33_F_4	1.154	1.213	1.213	2.541	2.765	3.148	1.932	2.135	2.287	ns
LVCMOS33_F_8	1.154	1.213	1.213	2.603	2.822	3.205	1.937	2.130	2.294	ns
LVCMOS33_S_12	1.154	1.213	1.213	2.705	3.047	3.430	2.049	2.318	2.404	ns
LVCMOS33_S_16	1.154	1.213	1.213	2.714	3.024	3.407	2.028	2.232	2.383	ns
LVCMOS33_S_4	1.154	1.213	1.213	2.999	3.340	3.723	2.320	2.610	2.675	ns
LVCMOS33_S_8	1.154	1.213	1.213	2.929	3.260	3.643	2.260	2.532	2.616	ns
LVDS_25	1.003	1.116	1.116	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL	1.003	1.116	1.116	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVTTL_F_12	1.164	1.223	1.223	2.415	2.651	3.034	1.754	1.915	2.109	ns
LVTTL_F_16	1.164	1.223	1.223	2.464	2.732	3.115	1.750	1.986	2.117	ns

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$			$T_{OUTBUF\_DELAY\_O\_PAD}$			$T_{OUTBUF\_DELAY\_TD\_PAD}$			Units
	0.85V		0.72V	0.85V		0.72V	0.85V		0.72V	
	-2	-1	-1	-2	-1	-1	-2	-1	-1	
LVTTL_F_4	1.164	1.223	1.223	2.541	2.765	3.148	1.932	2.135	2.287	ns
LVTTL_F_8	1.164	1.223	1.223	2.582	2.787	3.170	1.910	2.063	2.265	ns
LVTTL_S_12	1.164	1.223	1.223	2.731	3.075	3.458	2.072	2.343	2.427	ns
LVTTL_S_16	1.164	1.223	1.223	2.714	3.024	3.407	2.028	2.232	2.383	ns
LVTTL_S_4	1.164	1.223	1.223	2.999	3.340	3.723	2.320	2.610	2.675	ns
LVTTL_S_8	1.164	1.223	1.223	2.929	3.260	3.643	2.260	2.532	2.616	ns
SLVS_400_25	1.020	1.136	1.136	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_F	0.780	0.867	0.867	1.643	1.792	2.175	1.285	1.423	1.640	ns
SSTL12_S	0.780	0.867	0.867	1.784	1.948	2.331	1.567	1.706	1.922	ns
SSTL135_F	0.798	0.881	0.881	1.625	1.765	2.148	1.341	1.458	1.696	ns
SSTL135_II_F	0.798	0.881	0.881	1.623	1.770	2.153	1.325	1.470	1.689	ns
SSTL135_II_S	0.798	0.881	0.881	1.768	1.916	2.299	1.722	1.911	2.078	ns
SSTL135_S	0.798	0.881	0.881	1.869	2.025	2.408	1.814	1.976	2.169	ns
SSTL15_F	0.838	0.880	0.880	1.612	1.754	2.137	1.357	1.464	1.713	ns
SSTL15_II_F	0.838	0.880	0.880	1.622	1.778	2.161	1.356	1.442	1.712	ns
SSTL15_II_S	0.838	0.880	0.880	1.821	1.987	2.370	1.895	2.047	2.250	ns
SSTL15_S	0.838	0.880	0.880	1.824	1.977	2.360	1.743	1.907	2.098	ns
SSTL18_II_F	0.947	1.021	1.021	1.729	1.880	2.263	1.377	1.492	1.732	ns
SSTL18_II_S	0.947	1.021	1.021	1.796	1.965	2.348	1.616	1.800	1.972	ns
SSTL18_I_F	0.947	1.021	1.021	1.609	1.755	2.138	1.220	1.313	1.575	ns
SSTL18_I_S	0.947	1.021	1.021	1.786	1.942	2.325	1.677	1.836	2.033	ns
SUB_LVDS	1.002	1.036	1.036	N/A	N/A	N/A	N/A	N/A	N/A	ns

IOB High Performance (HP) Switching Characteristics

Table: IOB High Performance (HP) Switching Characteristics

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$	$T_{OUTBUF\_DELAY\_O\_PAD}$	$T_{OUTBUF\_DELAY\_TD\_PAD}$	Units

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$			$T_{OUTBUF\_DELAY\_O\_PAD}$			$T_{OUTBUF\_DELAY\_TD\_PAD}$			Units
	0.85V		0.72V	0.85V		0.72V	0.85V		0.72V	
	-2	-1	-1	-2	-1	-1	-2	-1	-1	
DIFF_HSTL_I_12_F	0.394	0.402	0.402	0.423	0.443	0.443	0.553	0.582	0.582	ns
DIFF_HSTL_I_12_M	0.394	0.402	0.402	0.552	0.583	0.583	0.641	0.679	0.679	ns
DIFF_HSTL_I_12_S	0.394	0.402	0.402	0.752	0.800	0.800	0.813	0.868	0.868	ns
DIFF_HSTL_I_18_F	0.319	0.339	0.339	0.456	0.474	0.474	0.576	0.606	0.606	ns
DIFF_HSTL_I_18_M	0.319	0.339	0.339	0.570	0.603	0.603	0.653	0.692	0.692	ns
DIFF_HSTL_I_18_S	0.319	0.339	0.339	0.782	0.834	0.834	0.816	0.871	0.871	ns
DIFF_HSTL_I_DCI_12_F	0.394	0.402	0.402	0.406	0.429	0.429	0.534	0.564	0.564	ns
DIFF_HSTL_I_DCI_12_M	0.394	0.402	0.402	0.557	0.587	0.587	0.653	0.694	0.694	ns
DIFF_HSTL_I_DCI_12_S	0.394	0.402	0.402	0.755	0.806	0.806	0.842	0.907	0.907	ns
DIFF_HSTL_I_DCI_18_F	0.323	0.339	0.339	0.445	0.461	0.461	0.566	0.595	0.595	ns
DIFF_HSTL_I_DCI_18_M	0.323	0.339	0.339	0.555	0.586	0.586	0.643	0.684	0.684	ns
DIFF_HSTL_I_DCI_18_S	0.323	0.339	0.339	0.762	0.818	0.818	0.836	0.900	0.900	ns
DIFF_HSTL_I_DCI_F	0.397	0.417	0.417	0.431	0.445	0.445	0.555	0.575	0.575	ns
DIFF_HSTL_I_DCI_M	0.397	0.417	0.417	0.553	0.583	0.583	0.644	0.684	0.684	ns
DIFF_HSTL_I_DCI_S	0.397	0.417	0.417	0.767	0.823	0.823	0.848	0.912	0.912	ns
DIFF_HSTL_I_F	0.404	0.417	0.417	0.423	0.443	0.443	0.549	0.581	0.581	ns
DIFF_HSTL_I_M	0.404	0.417	0.417	0.555	0.586	0.586	0.640	0.677	0.677	ns
DIFF_HSTL_I_S	0.404	0.417	0.417	0.767	0.818	0.818	0.811	0.866	0.866	ns
DIFF_HSUL_12_DCI_F	0.381	0.400	0.400	0.425	0.443	0.443	0.558	0.586	0.586	ns
DIFF_HSUL_12_DCI_M	0.381	0.400	0.400	0.557	0.587	0.587	0.653	0.694	0.694	ns
DIFF_HSUL_12_DCI_S	0.381	0.400	0.400	0.737	0.787	0.787	0.822	0.885	0.885	ns
DIFF_HSUL_12_F	0.394	0.402	0.402	0.412	0.430	0.430	0.538	0.566	0.566	ns
DIFF_HSUL_12_M	0.394	0.402	0.402	0.552	0.583	0.583	0.641	0.679	0.679	ns
DIFF_HSUL_12_S	0.394	0.402	0.402	0.752	0.800	0.800	0.813	0.868	0.868	ns
DIFF_POD10_DCI_F	0.411	0.430	0.430	0.425	0.444	0.444	0.555	0.584	0.584	ns

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$			$T_{OUTBUF\_DELAY\_O\_PAD}$			$T_{OUTBUF\_DELAY\_TD\_PAD}$			Units
	0.85V		0.72V	0.85V		0.72V	0.85V		0.72V	
	-2	-1	-1	-2	-1	-1	-2	-1	-1	
DIFF_POD10_DCI_M	0.411	0.430	0.430	0.542	0.571	0.571	0.640	0.681	0.681	ns
DIFF_POD10_DCI_S	0.411	0.430	0.430	0.754	0.815	0.815	0.850	0.917	0.917	ns
DIFF_POD10_F	0.411	0.433	0.433	0.438	0.459	0.459	0.569	0.601	0.601	ns
DIFF_POD10_M	0.411	0.433	0.433	0.538	0.568	0.568	0.630	0.667	0.667	ns
DIFF_POD10_S	0.411	0.433	0.433	0.766	0.821	0.821	0.836	0.894	0.894	ns
DIFF_POD12_DCI_F	0.407	0.432	0.432	0.425	0.443	0.443	0.558	0.586	0.586	ns
DIFF_POD12_DCI_M	0.407	0.432	0.432	0.543	0.572	0.572	0.638	0.678	0.678	ns
DIFF_POD12_DCI_S	0.407	0.432	0.432	0.772	0.822	0.822	0.862	0.929	0.929	ns
DIFF_POD12_F	0.409	0.430	0.430	0.455	0.476	0.476	0.595	0.626	0.626	ns
DIFF_POD12_M	0.409	0.430	0.430	0.551	0.582	0.582	0.641	0.679	0.679	ns
DIFF_POD12_S	0.409	0.430	0.430	0.767	0.817	0.817	0.832	0.889	0.889	ns
DIFF_SSTL12_DCI_F	0.381	0.400	0.400	0.425	0.443	0.443	0.558	0.586	0.586	ns
DIFF_SSTL12_DCI_M	0.381	0.400	0.400	0.557	0.587	0.587	0.654	0.694	0.694	ns
DIFF_SSTL12_DCI_S	0.381	0.400	0.400	0.754	0.803	0.803	0.842	0.908	0.908	ns
DIFF_SSTL12_F	0.394	0.402	0.402	0.412	0.430	0.430	0.538	0.566	0.566	ns
DIFF_SSTL12_M	0.394	0.402	0.402	0.553	0.584	0.584	0.641	0.676	0.676	ns
DIFF_SSTL12_S	0.394	0.402	0.402	0.758	0.808	0.808	0.823	0.879	0.879	ns
DIFF_SSTL135_DCI_F	0.371	0.402	0.402	0.411	0.428	0.428	0.537	0.565	0.565	ns
DIFF_SSTL135_DCI_M	0.371	0.402	0.402	0.551	0.582	0.582	0.645	0.685	0.685	ns
DIFF_SSTL135_DCI_S	0.371	0.402	0.402	0.746	0.799	0.799	0.829	0.893	0.893	ns
DIFF_SSTL135_F	0.375	0.402	0.402	0.408	0.428	0.428	0.528	0.561	0.561	ns
DIFF_SSTL135_M	0.375	0.402	0.402	0.555	0.585	0.585	0.641	0.679	0.679	ns
DIFF_SSTL135_S	0.375	0.402	0.402	0.772	0.823	0.823	0.827	0.878	0.878	ns
DIFF_SSTL15_DCI_F	0.397	0.417	0.417	0.412	0.429	0.429	0.531	0.563	0.563	ns
DIFF_SSTL15_DCI_M	0.397	0.417	0.417	0.553	0.583	0.583	0.645	0.685	0.685	ns

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$			$T_{OUTBUF\_DELAY\_O\_PAD}$			$T_{OUTBUF\_DELAY\_TD\_PAD}$			Units
	0.85V		0.72V	0.85V		0.72V	0.85V		0.72V	
	-2	-1	-1	-2	-1	-1	-2	-1	-1	
DIFF_SSTL15_DCI_S	0.397	0.417	0.417	0.768	0.822	0.822	0.847	0.912	0.912	ns
DIFF_SSTL15_F	0.404	0.417	0.417	0.424	0.445	0.445	0.551	0.577	0.577	ns
DIFF_SSTL15_M	0.404	0.417	0.417	0.554	0.585	0.585	0.639	0.677	0.677	ns
DIFF_SSTL15_S	0.404	0.417	0.417	0.767	0.817	0.817	0.813	0.867	0.867	ns
DIFF_SSTL18_I_DCI_F	0.320	0.336	0.336	0.445	0.461	0.461	0.566	0.595	0.595	ns
DIFF_SSTL18_I_DCI_M	0.320	0.336	0.336	0.554	0.585	0.585	0.644	0.683	0.683	ns
DIFF_SSTL18_I_DCI_S	0.320	0.336	0.336	0.762	0.818	0.818	0.837	0.899	0.899	ns
DIFF_SSTL18_I_F	0.316	0.336	0.336	0.454	0.476	0.476	0.578	0.608	0.608	ns
DIFF_SSTL18_I_M	0.316	0.336	0.336	0.571	0.603	0.603	0.652	0.692	0.692	ns
DIFF_SSTL18_I_S	0.316	0.336	0.336	0.782	0.835	0.835	0.816	0.870	0.870	ns
HSLVDCI_15_F	0.393	0.415	0.415	0.425	0.443	0.443	0.548	0.579	0.579	ns
HSLVDCI_15_M	0.393	0.415	0.415	0.552	0.581	0.581	0.644	0.684	0.684	ns
HSLVDCI_15_S	0.393	0.415	0.415	0.748	0.802	0.802	0.827	0.890	0.890	ns
HSLVDCI_18_F	0.424	0.447	0.447	0.445	0.461	0.461	0.566	0.595	0.595	ns
HSLVDCI_18_M	0.424	0.447	0.447	0.567	0.598	0.598	0.658	0.699	0.699	ns
HSLVDCI_18_S	0.424	0.447	0.447	0.761	0.817	0.817	0.836	0.900	0.900	ns
HSTL_I_12_F	0.378	0.399	0.399	0.423	0.443	0.443	0.553	0.582	0.582	ns
HSTL_I_12_M	0.378	0.399	0.399	0.551	0.582	0.582	0.642	0.679	0.679	ns
HSTL_I_12_S	0.378	0.399	0.399	0.750	0.799	0.799	0.813	0.868	0.868	ns
HSTL_I_18_F	0.322	0.339	0.339	0.456	0.474	0.474	0.576	0.606	0.606	ns
HSTL_I_18_M	0.322	0.339	0.339	0.569	0.602	0.602	0.653	0.692	0.692	ns
HSTL_I_18_S	0.322	0.339	0.339	0.781	0.833	0.833	0.816	0.871	0.871	ns
HSTL_I_DCI_12_F	0.378	0.399	0.399	0.406	0.429	0.429	0.534	0.564	0.564	ns
HSTL_I_DCI_12_M	0.378	0.399	0.399	0.556	0.586	0.586	0.654	0.694	0.694	ns
HSTL_I_DCI_12_S	0.378	0.399	0.399	0.754	0.803	0.803	0.842	0.907	0.907	ns

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$			$T_{OUTBUF\_DELAY\_O\_PAD}$			$T_{OUTBUF\_DELAY\_TD\_PAD}$			Units
	0.85V		0.72V	0.85V		0.72V	0.85V		0.72V	
	-2	-1	-1	-2	-1	-1	-2	-1	-1	
HSTL_I_DCI_18_F	0.321	0.339	0.339	0.445	0.461	0.461	0.566	0.595	0.595	ns
HSTL_I_DCI_18_M	0.321	0.339	0.339	0.554	0.585	0.585	0.643	0.684	0.684	ns
HSTL_I_DCI_18_S	0.321	0.339	0.339	0.761	0.817	0.817	0.836	0.900	0.900	ns
HSTL_I_DCI_F	0.393	0.415	0.415	0.431	0.445	0.445	0.555	0.575	0.575	ns
HSTL_I_DCI_M	0.393	0.415	0.415	0.552	0.581	0.581	0.644	0.684	0.684	ns
HSTL_I_DCI_S	0.393	0.415	0.415	0.766	0.821	0.821	0.847	0.912	0.912	ns
HSTL_I_F	0.378	0.399	0.399	0.423	0.443	0.443	0.549	0.581	0.581	ns
HSTL_I_M	0.378	0.399	0.399	0.554	0.585	0.585	0.640	0.677	0.677	ns
HSTL_I_S	0.378	0.399	0.399	0.766	0.816	0.816	0.811	0.866	0.866	ns
HSUL_12_DCI_F	0.378	0.399	0.399	0.425	0.443	0.443	0.558	0.586	0.586	ns
HSUL_12_DCI_M	0.378	0.399	0.399	0.556	0.586	0.586	0.654	0.694	0.694	ns
HSUL_12_DCI_S	0.378	0.399	0.399	0.736	0.784	0.784	0.821	0.886	0.886	ns
HSUL_12_F	0.378	0.399	0.399	0.412	0.430	0.430	0.538	0.566	0.566	ns
HSUL_12_M	0.378	0.399	0.399	0.551	0.582	0.582	0.642	0.679	0.679	ns
HSUL_12_S	0.378	0.399	0.399	0.750	0.799	0.799	0.813	0.868	0.868	ns
LVCMOS12_F_2	0.512	0.555	0.555	0.672	0.692	0.692	0.898	0.922	0.922	ns
LVCMOS12_F_4	0.512	0.555	0.555	0.504	0.521	0.521	0.664	0.693	0.693	ns
LVCMOS12_F_6	0.512	0.555	0.555	0.485	0.507	0.507	0.634	0.669	0.669	ns
LVCMOS12_F_8	0.512	0.555	0.555	0.465	0.489	0.489	0.611	0.666	0.666	ns
LVCMOS12_M_2	0.512	0.555	0.555	0.708	0.727	0.727	0.916	0.945	0.945	ns
LVCMOS12_M_4	0.512	0.555	0.555	0.550	0.573	0.573	0.664	0.690	0.690	ns
LVCMOS12_M_6	0.512	0.555	0.555	0.527	0.554	0.554	0.622	0.652	0.652	ns
LVCMOS12_M_8	0.512	0.555	0.555	0.540	0.571	0.571	0.614	0.649	0.649	ns
LVCMOS12_S_2	0.512	0.555	0.555	0.767	0.803	0.803	0.990	1.024	1.024	ns
LVCMOS12_S_4	0.512	0.555	0.555	0.666	0.704	0.704	0.803	0.848	0.848	ns

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$			$T_{OUTBUF\_DELAY\_O\_PAD}$			$T_{OUTBUF\_DELAY\_TD\_PAD}$			Units
	0.85V		0.72V	0.85V		0.72V	0.85V		0.72V	
	-2	-1	-1	-2	-1	-1	-2	-1	-1	
LVCMOS12_S_6	0.512	0.555	0.555	0.657	0.695	0.695	0.732	0.774	0.774	ns
LVCMOS12_S_8	0.512	0.555	0.555	0.708	0.761	0.761	0.745	0.790	0.790	ns
LVCMOS15_F_12	0.414	0.445	0.445	0.500	0.522	0.522	0.647	0.682	0.682	ns
LVCMOS15_F_2	0.414	0.445	0.445	0.702	0.722	0.722	0.919	0.940	0.940	ns
LVCMOS15_F_4	0.414	0.445	0.445	0.579	0.601	0.601	0.755	0.781	0.781	ns
LVCMOS15_F_6	0.414	0.445	0.445	0.547	0.569	0.569	0.711	0.742	0.742	ns
LVCMOS15_F_8	0.414	0.445	0.445	0.518	0.538	0.538	0.686	0.703	0.703	ns
LVCMOS15_M_12	0.414	0.445	0.445	0.607	0.644	0.644	0.637	0.676	0.676	ns
LVCMOS15_M_2	0.414	0.445	0.445	0.741	0.770	0.770	0.938	0.962	0.962	ns
LVCMOS15_M_4	0.414	0.445	0.445	0.625	0.651	0.651	0.754	0.786	0.786	ns
LVCMOS15_M_6	0.414	0.445	0.445	0.576	0.604	0.604	0.674	0.710	0.710	ns
LVCMOS15_M_8	0.414	0.445	0.445	0.568	0.601	0.601	0.639	0.681	0.681	ns
LVCMOS15_S_12	0.414	0.445	0.445	0.788	0.855	0.855	0.695	0.733	0.733	ns
LVCMOS15_S_2	0.414	0.445	0.445	0.829	0.864	0.864	1.039	1.079	1.079	ns
LVCMOS15_S_4	0.414	0.445	0.445	0.687	0.725	0.725	0.813	0.851	0.851	ns
LVCMOS15_S_6	0.414	0.445	0.445	0.671	0.710	0.710	0.726	0.763	0.763	ns
LVCMOS15_S_8	0.414	0.445	0.445	0.704	0.755	0.755	0.721	0.758	0.758	ns
LVCMOS18_F_12	0.418	0.445	0.445	0.573	0.601	0.601	0.731	0.769	0.769	ns
LVCMOS18_F_2	0.418	0.445	0.445	0.739	0.760	0.760	0.945	0.971	0.971	ns
LVCMOS18_F_4	0.418	0.445	0.445	0.609	0.630	0.630	0.778	0.802	0.802	ns
LVCMOS18_F_6	0.418	0.445	0.445	0.603	0.633	0.633	0.781	0.808	0.808	ns
LVCMOS18_F_8	0.418	0.445	0.445	0.573	0.600	0.600	0.733	0.767	0.767	ns
LVCMOS18_M_12	0.418	0.445	0.445	0.640	0.678	0.678	0.670	0.709	0.709	ns
LVCMOS18_M_2	0.418	0.445	0.445	0.798	0.822	0.822	0.991	1.016	1.016	ns
LVCMOS18_M_4	0.418	0.445	0.445	0.664	0.693	0.693	0.798	0.836	0.836	ns

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$			$T_{OUTBUF\_DELAY\_O\_PAD}$			$T_{OUTBUF\_DELAY\_TD\_PAD}$			Units
	0.85V		0.72V	0.85V		0.72V	0.85V		0.72V	
	-2	-1	-1	-2	-1	-1	-2	-1	-1	
LVCMOS18_M_6	0.418	0.445	0.445	0.629	0.663	0.663	0.735	0.775	0.775	ns
LVCMOS18_M_8	0.418	0.445	0.445	0.626	0.661	0.661	0.705	0.746	0.746	ns
LVCMOS18_S_12	0.418	0.445	0.445	0.795	0.861	0.861	0.683	0.721	0.721	ns
LVCMOS18_S_2	0.418	0.445	0.445	0.862	0.897	0.897	1.076	1.098	1.098	ns
LVCMOS18_S_4	0.418	0.445	0.445	0.716	0.758	0.758	0.829	0.872	0.872	ns
LVCMOS18_S_6	0.418	0.445	0.445	0.682	0.724	0.724	0.724	0.762	0.762	ns
LVCMOS18_S_8	0.418	0.445	0.445	0.707	0.760	0.760	0.709	0.745	0.745	ns
LVDCI_15_F	0.425	0.462	0.462	0.426	0.443	0.443	0.548	0.581	0.581	ns
LVDCI_15_M	0.425	0.462	0.462	0.553	0.582	0.582	0.645	0.685	0.685	ns
LVDCI_15_S	0.425	0.462	0.462	0.749	0.803	0.803	0.821	0.890	0.890	ns
LVDCI_18_F	0.414	0.447	0.447	0.441	0.459	0.459	0.560	0.589	0.589	ns
LVDCI_18_M	0.414	0.447	0.447	0.554	0.585	0.585	0.644	0.683	0.683	ns
LVDCI_18_S	0.414	0.447	0.447	0.760	0.818	0.818	0.837	0.899	0.899	ns
LVDS	0.539	0.620	0.620	0.626	0.662	0.662	960.447			ns
MIPI_DPHY_DCI_HS	0.386	0.415	0.415	0.502	0.522	0.522	N/A	N/A	N/A	ns
MIPI_DPHY_DCI_LP	8.438	8.792	8.792	0.914	0.937	0.937	N/A	N/A	N/A	ns
POD10_DCI_F	0.408	0.430	0.430	0.425	0.444	0.444	0.555	0.584	0.584	ns
POD10_DCI_M	0.408	0.430	0.430	0.542	0.571	0.571	0.640	0.681	0.681	ns
POD10_DCI_S	0.408	0.430	0.430	0.754	0.815	0.815	0.850	0.917	0.917	ns
POD10_F	0.407	0.430	0.430	0.438	0.459	0.459	0.569	0.601	0.601	ns
POD10_M	0.407	0.430	0.430	0.538	0.568	0.568	0.630	0.667	0.667	ns
POD10_S	0.407	0.430	0.430	0.766	0.821	0.821	0.836	0.894	0.894	ns
POD12_DCI_F	0.409	0.431	0.431	0.425	0.443	0.443	0.558	0.586	0.586	ns
POD12_DCI_M	0.409	0.431	0.431	0.543	0.572	0.572	0.638	0.678	0.678	ns
POD12_DCI_S	0.409	0.431	0.431	0.772	0.822	0.822	0.862	0.929	0.929	ns

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$			$T_{OUTBUF\_DELAY\_O\_PAD}$			$T_{OUTBUF\_DELAY\_TD\_PAD}$			Units
	0.85V		0.72V	0.85V		0.72V	0.85V		0.72V	
	-2	-1	-1	-2	-1	-1	-2	-1	-1	
POD12_F	0.409	0.431	0.431	0.455	0.476	0.476	0.595	0.626	0.626	ns
POD12_M	0.409	0.431	0.431	0.551	0.582	0.582	0.641	0.679	0.679	ns
POD12_S	0.409	0.431	0.431	0.767	0.817	0.817	0.832	0.889	0.889	ns
SLVS_400_18	0.539	0.620	0.620	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.381	0.399	0.399	0.425	0.443	0.443	0.558	0.586	0.586	ns
SSTL12_DCI_M	0.381	0.399	0.399	0.557	0.587	0.587	0.654	0.694	0.694	ns
SSTL12_DCI_S	0.381	0.399	0.399	0.754	0.803	0.803	0.842	0.908	0.908	ns
SSTL12_F	0.403	0.403	0.403	0.412	0.430	0.430	0.538	0.566	0.566	ns
SSTL12_M	0.403	0.403	0.403	0.553	0.584	0.584	0.641	0.676	0.676	ns
SSTL12_S	0.403	0.403	0.403	0.758	0.808	0.808	0.823	0.879	0.879	ns
SSTL135_DCI_F	0.366	0.399	0.399	0.411	0.428	0.428	0.537	0.565	0.565	ns
SSTL135_DCI_M	0.366	0.399	0.399	0.551	0.582	0.582	0.645	0.685	0.685	ns
SSTL135_DCI_S	0.366	0.399	0.399	0.746	0.799	0.799	0.829	0.893	0.893	ns
SSTL135_F	0.378	0.399	0.399	0.408	0.428	0.428	0.528	0.561	0.561	ns
SSTL135_M	0.378	0.399	0.399	0.555	0.585	0.585	0.641	0.679	0.679	ns
SSTL135_S	0.378	0.399	0.399	0.772	0.823	0.823	0.827	0.878	0.878	ns
SSTL15_DCI_F	0.402	0.417	0.417	0.412	0.429	0.429	0.531	0.563	0.563	ns
SSTL15_DCI_M	0.402	0.417	0.417	0.553	0.583	0.583	0.645	0.685	0.685	ns
SSTL15_DCI_S	0.402	0.417	0.417	0.768	0.822	0.822	0.847	0.912	0.912	ns
SSTL15_F	0.371	0.400	0.400	0.408	0.428	0.428	0.530	0.556	0.556	ns
SSTL15_M	0.371	0.400	0.400	0.554	0.585	0.585	0.639	0.677	0.677	ns
SSTL15_S	0.371	0.400	0.400	0.767	0.817	0.817	0.813	0.867	0.867	ns
SSTL18_I_DCI_F	0.329	0.336	0.336	0.445	0.461	0.461	0.566	0.595	0.595	ns
SSTL18_I_DCI_M	0.329	0.336	0.336	0.554	0.585	0.585	0.644	0.683	0.683	ns
SSTL18_I_DCI_S	0.329	0.336	0.336	0.762	0.818	0.818	0.837	0.899	0.899	ns

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$			$T_{OUTBUF\_DELAY\_O\_PAD}$			$T_{OUTBUF\_DELAY\_TD\_PAD}$			Units
	0.85V		0.72V	0.85V		0.72V	0.85V		0.72V	
	-2	-1	-1	-2	-1	-1	-2	-1	-1	
SSTL18_I_F	0.316	0.337	0.337	0.454	0.476	0.476	0.578	0.608	0.608	ns
SSTL18_I_M	0.316	0.337	0.337	0.571	0.603	0.603	0.652	0.692	0.692	ns
SSTL18_I_S	0.316	0.337	0.337	0.782	0.835	0.835	0.816	0.870	0.870	ns
SUB_LVDS	0.539	0.620	0.620	0.660	0.692	0.692	969.863			ns

IOB 3-state Output Switching Characteristics

Table 1 specifies the values of $T_{OUTBUF\_DELAY\_TE\_PAD}$ and $T_{INBUF\_DELAY\_IBUFDIS\_O}$.

- $T_{OUTBUF\_DELAY\_TE\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).
- $T_{INBUF\_DELAY\_IBUFDIS\_O}$ is the IOB delay from IBUFDISABLE to O output.
- In HP I/O banks, the internal DCI termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the DCITERMDISABLE pin is used.
- In HD I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the INTERMDISABLE pin is used.

Table: IOB 3-state Output Switching Characteristics

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
$T_{OUTBUF\_DELAY\_TE\_PAD}$	T input to pad high-impedance for HD I/O banks				ns
	T input to pad high-impedance for HP I/O banks				ns
$T_{INBUF\_DELAY\_IBUFDIS\_O}$	IBUF turn-on time from IBUFDISABLE to O output for HD I/O banks				ns
	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks				ns

Input Delay Measurement Methodology

The following table shows the test setup parameters used for measuring input delay.

Table: Input Delay Measurement Methodology

Description	I/O Standard Attribute	V_L [1, 2]	V_H [1, 2]	V_{MEAS} [1, 4]	V_{REF} [1, 3, 5]
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	–
LVCMOS, LVDCI, HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	0.1	1.4	0.75	–
LVCMOS, LVDCI, HSLVDCI, 1.8V	LVCMOS18, LVDCI_18, HSLVDCI_18	0.1	1.7	0.9	–
LVCMOS, 2.5V	LVCMOS25	0.1	2.4	1.25	–
LVCMOS, 3.3V	LVCMOS33	0.1	3.2	1.65	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	–
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	V_{REF} – 0.325	V_{REF} + 0.325	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	V_{REF} – 0.4	V_{REF} + 0.4	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	V_{REF} – 0.2875	V_{REF} + 0.2875	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	V_{REF} – 0.325	V_{REF} + 0.325	V_{REF}	0.75
SSTL18, class I and II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.4	V_{REF} + 0.4	V_{REF}	0.9
POD10, 1.0V	POD10	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.7
POD12, 1.2V	POD12	V_{REF} – 0.24	V_{REF} + 0.24	V_{REF}	0.84

Description	I/O Standard Attribute	V_L [1, 2]	V_H [1, 2]	V_{MEAS} [1, 4]	V_{REF} [1, 3, 5]
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	0.6 – 0.25	0.6 + 0.25	0 [6]	–
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	0.75 – 0.325	0.75 + 0.325	0 [6]	–
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	0.9 – 0.4	0.9 + 0.4	0 [6]	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	0.6 – 0.25	0.6 + 0.25	0 [6]	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	0.6 – 0.25	0.6 + 0.25	0 [6]	–
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	0.675 – 0.2875	0.675 + 0.2875	0 [6]	–
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	0.75 – 0.325	0.75 + 0.325	0 [6]	–
DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	0.9 – 0.4	0.9 + 0.4	0 [6]	–
DIFF_POD10, 1.0V	DIFF_POD10	0.5 – 0.2	0.5 + 0.2	0 [6]	–
DIFF_POD12, 1.2V	DIFF_POD12	0.6 – 0.25	0.6 + 0.25	0 [6]	–
LVDS (low-voltage differential signaling), 1.8V	LVDS	0.9 – 0.125	0.9 + 0.125	0 [6]	–
LVDS_25, 2.5V	LVDS_25	1.25 – 0.125	1.25 + 0.125	0 [6]	–
SUB_LVDS, 1.8V	SUB_LVDS	0.9 – 0.125	0.9 + 0.125	0 [6]	–
SLVS, 1.8V	SLVS_400_18	0.9 – 0.125	0.9 + 0.125	0 [6]	–
SLVS, 2.5V	SLVS_400_25	1.25 – 0.125	1.25 + 0.125	0 [6]	–
LVPECL, 2.5V	LVPECL	1.25 – 0.125	1.25 + 0.125	0 [6]	–
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	0.2 – 0.125	0.2 + 0.125	0 [6]	–
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	0.715 – 0.2	0.715 + 0.2	0 [6]	–

Description	I/O Standard Attribute	V_L [1, 2]	V_H [1, 2]	V_{MEAS} [1, 4]	V_{REF} [1, 3, 5]

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

Figure: Single-Ended Test Setup

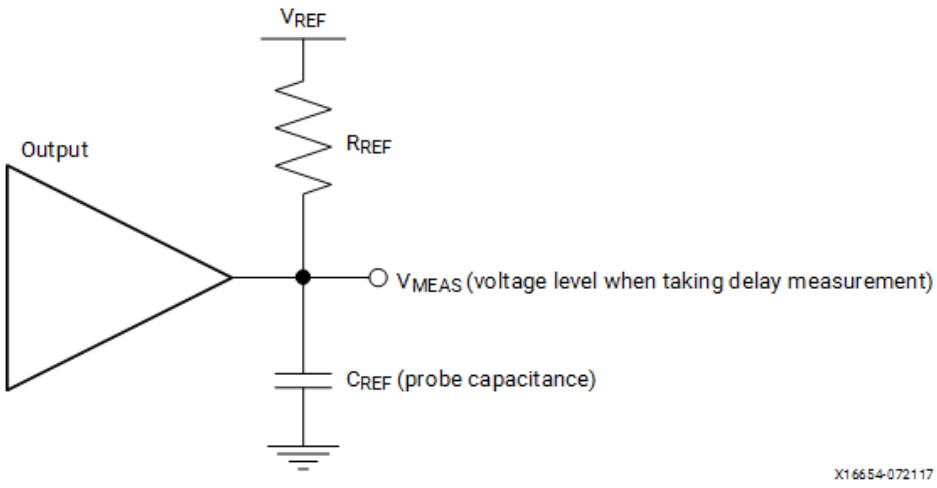
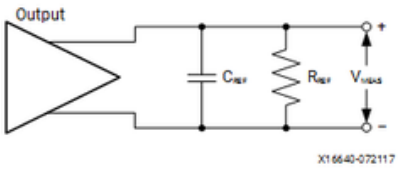


Figure: Differential Test Setup



Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 1.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table: Output Delay Measurement Methodology

Description	I/O Standard Attribute	R_{REF} (Ω) [1]	C_{REF} (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
LVDCI, HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V_{REF}	0.75
LVDCI, HSLVDCI, 1.8V	LVDCI_15, HSLVDCI_18	50	0	V_{REF}	0.9
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	50	0	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	50	0	V_{REF}	0.75
SSTL18, class I and class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF} [1] (pF)	V_{MEAS} (V)	V_{REF} (V)
POD10, 1.0V	POD10	50	0	V_{REF}	1.0
POD12, 1.2V	POD12	50	0	V_{REF}	1.2
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	50	0	V_{REF}	0.75
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	50	0	V_{REF}	0.9
DIFF_HSUL, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	50	0	V_{REF}	0.675
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	50	0	V_{REF}	0.75
DIFF_SSTL18, class I and II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V_{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V_{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0 [2]	0
SUB_LVDS, 1.8V	SUB_LVDS	100	0	0 [2]	0
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	100	0	0 [2]	0
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	1M	0	0.6	0

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Block RAM and FIFO Switching Characteristics

Table: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
Maximum Frequency					
$F_{MAX\_WF\_NC}$	Block RAM (WRITE_FIRST and NO_CHANGE modes)	738	645	516	MHz
F_{MAX_RF}	Block RAM (READ_FIRST mode)	637	575	460	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	738	645	516	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE	637	575	460	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode	738	645	516	MHz
T_{PW} [1]	Minimum pulse width	542	543	578	ps
Block RAM and FIFO Clock-to-Out Delays					
T_{RCKO_DO}	Clock CLK to DOUT output (without output register)	1.02	1.11	1.53	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register)	0.29	0.30	0.44	ns, Max

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

Input/Output Delay Switching Characteristics

Table: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
F_{REFCLK}	Reference clock frequency for IDELAYCTRL (component mode)	300 to 800			MHz

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
	Reference clock frequency when using BITSLICE_CONTROL with REFCLK (in native mode (for RX_BITSLICE only))	300 to 800			MHz
	Reference clock frequency for BITSLICE_CONTROL with PLL_CLK (in native mode) [1]	300 to 2666.67	300 to 2400	300 to 2133	MHz
T_{MINPER_CLK}	Minimum period for IODELAY clock	3.195	3.195	3.195	ns
T_{MINPER_RST}	Minimum reset pulse width	52.00			ns
$T_{IDELAY\_RESOLUTION}$ $T_{ODELAY\_RESOLUTION}$	IDELAY/ODELAY chain resolution	2.1 to 12			ps

1. PLL settings could restrict the minimum allowable data rate. For example, when using a PLL with CLKOUTPHY_MODE = VCO_HALF, the minimum frequency is PLL_F_{VCOMIN}/2.

DSP48 Slice Switching Characteristics

Table: DSP48 Slice Switching Characteristics

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V [1]	
		-2	-1	-1	
Maximum Frequency					
F_{MAX}	With all registers used	775	645	600	MHz
F_{MAX_PATDET}	With pattern detector	687	571	524	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	544	456	413	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	492	410	371	MHz

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V [1]	
		-2	-1	-1	
$F_{MAX\_PREADD\_NOADREG}$	Without ADREG	565	468	423	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	410	338	304	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	379	314	280	MHz

1. For devices operating at the lower power V_{CCINT} = 0.72V voltages, DSP cascades that cross the clock region center might operate below the specified F_{MAX}.

Clock Buffers and Networks

Table: Clock Buffers Switching Characteristics

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
Global Clock Switching Characteristics (Including BUFGCTRL)					
F_{MAX}	Maximum frequency of a global clock tree (BUFG)	775	667	667	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)					
F_{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV)	775	667	667	MHz
Global Clock Buffer with Clock Enable (BUFGCE)					
F_{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE)	775	667	667	MHz
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)					
F_{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF)	775	667	667	MHz
GTH or GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)					

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
F_{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability	512	512	512	MHz

MMCM Switching Characteristics

Table: MMCM Specification

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
MMCM_F_{INMAX}	Maximum input clock frequency	933	800	800	MHz
MMCM_F_{INMIN}	Minimum input clock frequency	10	10	10	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max			
MMCM_F_{INDUTY}	Input duty cycle range: 10–49 MHz	25–75			%
	Input duty cycle range: 50–199 MHz	30–70			%
	Input duty cycle range: 200–399 MHz	35–65			%
	Input duty cycle range: 400–499 MHz	40–60			%
	Input duty cycle range: >500 MHz	45–55			%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase shift clock frequency	500	450	450	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency	800	800	800	MHz

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency	1600	1600	1600	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical [1]	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical [1]	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs [2]	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter.	Note [3]			
MMCM_$T_{OUTDUTY}$	MMCM output clock duty cycle precision [4]	0.20	0.20	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time for MMCM_F_{PFDMIN}	100	100	100	μs
MMCM_F_{OUTMAX}	MMCM maximum output frequency	775	667	667	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency [4, 5]	6.25	6.25	6.25	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max			
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector	500	450	450	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector	10	10	10	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path	5 ns Max or one clock cycle			
MMCM_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	MHz

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

PLL Switching Characteristics

Table: PLL Specification

Symbol	Description [1]	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
PLL_F_{INMAX}	Maximum input clock frequency	933	800	800	MHz
PLL_F_{INMIN}	Minimum input clock frequency	70	70	70	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max			
PLL_F_{INDUTY}	Input duty cycle range: 70–399 MHz	35–65			%
	Input duty cycle range: 400–499 MHz	40–60			%
	Input duty cycle range: >500 MHz	45–55			%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency	750	750	750	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency	1500	1500	1500	MHz
PLL_$T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs [2]	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL output jitter.	Note 3			

Symbol	Description [1]	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
PLL_$T_{OUTDUTY}$	PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision [4]	0.20	0.20	0.20	ns
PLL_$T_{LOCKMAX}$	PLL maximum lock time	100			μs
PLL_F_{OUTMAX}	PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B	775	667	667	MHz
	PLL maximum output frequency at CLKOUTPHY	2667	2400	2133	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B [5]	5.86	5.86	5.86	MHz
	PLL minimum output frequency at CLKOUTPHY	2 x VCO mode: 1500, 1 x VCO mode: 750, 0.5 x VCO mode: 375			MHz
PLL_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector	667.5	667.5	667.5	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector	70	70	70	MHz
PLL_$F_{BANDWIDTH}$	PLL bandwidth at typical	14	14	14	MHz
PLL_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	MHz

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in the following tables are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the

Vivado Design Suite timing report for the actual pin-to-pin values.

Table: Global Clock Input to Output Delay Without MMCM (Near Clock Region)

Symbol	Description [1]	Device	Speed Grade and V_{CCINT} Operating Voltages			Units
			0.85V		0.72V	
			-2	-1	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM						
T_{ICKOF}	Global clock input and output flip-flop *without* MMCM (near clock region)	XCAU10P	4.92	5.31	6.61	ns
		XCAU15P	4.92	5.31	6.61	ns
		XCAU20P	5.09	5.48	6.84	ns
		XCAU25P	5.09	5.48	6.84	ns

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table: Global Clock Input to Output Delay Without MMCM (Far Clock Region)

Symbol	Description [1]	Device	Speed Grade and V_{CCINT} Operating Voltages			Units
			0.85V		0.72V	
			-2	-1	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM						
T_{ICKOF_FAR}	Global clock input and output flip-flop *without* MMCM (far clock region)	XCAU10P	5.13	5.53	6.91	ns
		XCAU15P	5.13	5.53	6.91	ns
		XCAU20P	5.30	5.70	7.14	ns
		XCAU25P	5.30	5.70	7.14	ns

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table: Global Clock Input to Output Delay With MMCM

Symbol	Description [1, 2]	Device	Speed Grade and V_{CCINT} Operating Voltages		Units
			0.85V	0.72V	

Symbol	Description [1, 2]	Device	Speed Grade and V_{CCINT} Operating Voltages			Units
			0.85V		0.72V	
			-2	-1	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM						
$T_{ICKOFMMCMCC}$	Global clock input and output flip-flop *with* MMCM	XCAU10P	2.09	2.30	2.88	ns
		XCAU15P	2.09	2.30	2.88	ns
		XCAU20P	1.98	2.17	2.74	ns
		XCAU25P	1.98	2.17	2.74	ns

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table: Source Synchronous Output Characteristics (Component Mode)

Description	Speed Grade and V_{CCINT} Operating Voltages			Units
	0.85V		0.72V	
	-2	-1	-1	
$T_{OUTPUT\_LOGIC\_DELAY\_VARIATION}$ [1]	80			ps

1. Delay mismatch across a transmit bus when using component mode output logic (ODDRE1, OSERDESE3) within a bank.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in the following tables are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table: Global Clock Input Setup and Hold With 3.3V HD I/O Without MMCM

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages			Units
			0.85V		0.72V	
			-2	-1	-1	

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages			Units
				0.85V		0.72V	
				-2	-1	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard. [1, 2, 3]							
T_{PSFD_AU10P}	Global clock input and input flip-flop (or latch) *without* MMCM	Setup	XCAU10P	2.07	2.14	3.50	ns
T_{PHFD_AU10P}		Hold		–0.23	–0.23	–0.87	ns
T_{PSFD_AU15P}		Setup	XCAU15P	2.07	2.14	3.50	ns
T_{PHFD_AU15P}		Hold		–0.23	–0.23	–0.87	ns
T_{PSFD_AU20P}		Setup	XCAU20P	2.28	2.38	3.83	ns
T_{PHFD_AU20P}		Hold		–0.36	–0.36	–1.04	ns
T_{PSFD_AU25P}		Setup	XCAU25P	2.28	2.38	3.83	ns
T_{PHFD_AU25P}		Hold		–0.36	–0.36	–1.04	ns

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table: Global Clock Input Setup and Hold With MMCM

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages			Units
				0.85V		0.72V	
				-2	-1	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard. [1, 2, 3]							
$T_{PSMMCMCC\_AU10P}$	Global clock input and input flip-flop (or latch) with MMCM	Setup	XCAU10P	1.82	1.95	1.95	ns
$T_{PHMMCMCC\_AU10P}$		Hold		–0.21	–0.21	–0.26	ns
$T_{PSMMCMCC\_AU15P}$		Setup	XCAU15P	1.82	1.95	1.95	ns
$T_{PHMMCMCC\_AU15P}$		Hold		–0.21	–0.21	–0.26	ns

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages			Units
				0.85V		0.72V	
				-2	-1	-1	
$T_{PSMMCMCC\_AU20P}$		Setup	XCAU20P	2.04	2.16	2.16	ns
$T_{PHMMCMCC\_AU20P}$		Hold		–0.17	–0.17	–0.23	ns
$T_{PSMMCMCC\_AU25P}$		Setup	XCAU25P	2.04	2.16	2.16	ns
$T_{PHMMCMCC\_AU25P}$		Hold		–0.17	–0.17	–0.23	ns

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table: Sampling Window

Description	Speed Grade and V_{CCINT} Operating Voltages			Units
	0.85V		0.72V	
	-2	-1	-1	
T_{SAMP_BUFG} [1]	610	610	610	ps
$T_{SAMP\_NATIVE\_DPA}$ [2]	100	125	150	ps
$T_{SAMP\_NATIVE\_BISC}$ [3]	60	85	110	ps

1. This parameter indicates the total sampling error of the Artix UltraScale+ FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew.
2. This parameter is the receive sampling error for RX_BITSLICE when using dynamic phase alignment.
3. This parameter is the receive sampling error for RX_BITSLICE when using built-in self-calibration (BISC).

Table: Input Logic Characteristics for Dynamic Phase Aligned Applications (Component Mode)

Description	Speed Grade and V_{CCINT} Operating Voltages			Units
	0.85V		0.72V	
	-2	-1	-1	
$T_{INPUT\_LOGIC\_UNCERTAINTY}$ [1]	40			ps
T_{CAL_ERROR} [2]	24			ps

1. Input_logic_uncertainty accounts for the setup/hold and any pattern dependent jitter for the input logic (input register, IDDRE1, or ISERDESE3).
2. Calibration error associated with quantization effects based on the IDELAY resolution. Calibration must be performed for each input pin to ensure optimal performance.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table: Package Skew

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew [1, 2]	XCAU10P	UBVA368	59	ps
			SBVB484	87	ps
			FFVB676	81	ps
		XCAU15P	UBVA368	59	ps
			SBVB484	87	ps
			FFVB676	81	ps
		XCAU20P	FFVB676	69	ps
			SFVB784	75	ps
		XCAU25P	FFVB676	69	ps
			SFVB784	75	ps

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTH Transceiver Specifications

The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists the Artix UltraScale+ FPGAs that include the GTH transceivers.

GTH Transceiver DC Input and Output Levels

The following table summarizes the DC specifications of the GTH transceivers in Artix UltraScale+ FPGAs. Consult the *UltraScale Architecture GTH Transceivers User Guide* (UG576) for further details.

Table: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND	DC coupled $V_{MGTAVTT}$ = 1.2V	–400	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage [1]	Transmitter output swing is set to 11111	800	–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 – D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} – D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM} [2]				mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled (equation based)		$V_{MGTAVTT} – D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance		–	100	–	Ω
R_{OUT}	Differential output resistance		–	100	–	Ω

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (all packages)		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor [3]		–	100	–	nF

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceivers User Guide* (UG576), and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

Figure: Single-Ended Peak-to-Peak Voltage

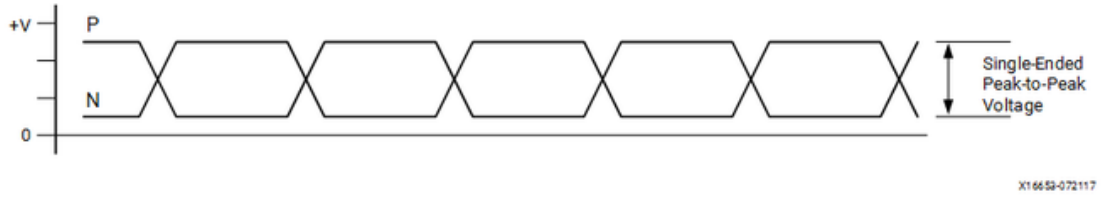


Figure: Differential Peak-to-Peak Voltage

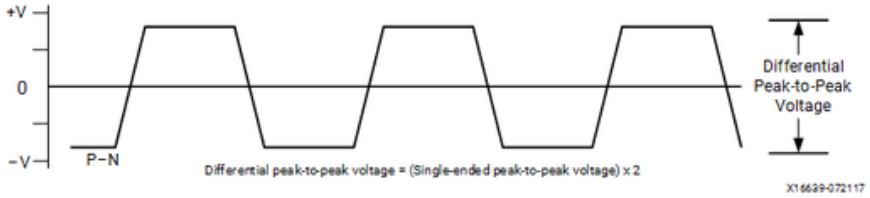


Table 2 and Table 3 summarize the DC specifications of the GTH transceivers input and output clocks in Artix UltraScale+ FPGAs. Consult the *UltraScale Architecture GTH Transceivers User Guide* (UG576) for further details.

Table: GTH Transceiver Clock Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table: GTH Transceiver Clock Output Level Specification

Symbol	Description	Conditions	Min	Typ	Max	Units

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	R_T = 100Ω across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	R_T = 100Ω across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	R_T = 100Ω across P and N signals	300	–	500	mV

GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceivers User Guide* (UG576) for further information.

Table: GTH Transceiver Performance

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltage						Units
			0.85V				0.72V		
			-2		-1		-1		
F_{GTHMAX}	GTH maximum line rate		16.375 [1]		12.5		10.3125		Gb/s
F_{GTHMIN}	GTH minimum line rate		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	
$F_{GTHCRANGE}$	CPLL line rate range [2]	1	4	12.5	4	8.5	4	8.5	Gb/s
		2	2	6.25	2	4.25	2	4.25	Gb/s
		4	1	3.125	1	2.125	1	2.125	Gb/s
		8	0.5	1.5625	0.5	1.0625	0.5	1.0625	Gb/s
		16	N/A						Gb/s
			Min	Max	Min	Max	Min	Max	
$F_{GTHQRANGE1}$	QPLL0 line rate range [3]	1	9.8	16.375	9.8	12.5	9.8	10.3125	Gb/s
		2	4.9	8.1875	4.9	8.15	4.9	8.15	Gb/s
		4	2.45	4.0938	2.45	4.075	2.45	4.075	Gb/s
		8	1.225	2.0469	1.225	2.0375	1.225	2.0375	Gb/s

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages						Units
			0.85V				0.72V		
			-2		-1		-1		
		16	0.6125	1.0234	0.6125	1.0188	0.6125	1.0188	Gb/s
			Min	Max	Min	Max	Min	Max	
$F_{GTHQRANGE2}$	QPLL1 line rate range [4]	1	8.0	13.0	8.0	12.5	8.0	10.3125	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	
$F_{CPLLRANGE}$	CPLL frequency range		2	6.25	2	4.25	2	4.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range		8	13	8	13	8	13	GHz

1. GTH transceiver line rates in the SFVB784, SBVB484, and UBVA368 packages support data rates up to 12.5 Gb/s. 12.5 Gb/s operation in the UBVA368 package is pending characterization.
2. The values listed are the rounded results of the calculated equation (2 × CPLL_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (QPLL0_Frequency)/Output_Divider.
4. The values listed are the rounded results of the calculated equation (QPLL1_Frequency)/Output_Divider.

Table: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	All Speed Grades	Units
$F_{GTHDRPCLK}$	GTHDRPCLK maximum frequency	250	MHz

Table: GTH Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	820	MHz

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

Table: GTH Transceiver Reference Clock Oscillator Selection Phase Noise Mask

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$ 1, 2	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
$CPLL_{REFCLKMASK}$ 1, 2	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
		50 MHz	–	–	–140	

1. For reference clock frequencies other than 312.5 MHz, adjust the phase-noise mask values by 20 × Log(N/312.5) where N is the new reference clock frequency in MHz.
2. This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table: GTH Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE)	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled		–	50,000	2.3×10^6	UI

Table: GTH Transceiver User Clock Switching Characteristics

Symbol	Description [1]	Data Width Conditions (bits)		Speed Grade and V_{CCINT} Operating Vo			Units
				0.85V		0.72V	
		Internal Logic	Interconnect Logic	-2	-1 [3, 4]	-1 [4]	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	390.625	322.266	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	390.625	322.266	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK [5] maximum frequency	16	16, 32	511.719	390.625	322.266	MHz
		32	32, 64	511.719	390.625	322.266	MHz
		20	20, 40	409.375	312.500	257.813	MHz
		40	40, 80	409.375	312.500	257.813	MHz
F_{RXIN}	RXUSRCLK [5] maximum frequency	16	16, 32	511.719	390.625	322.266	MHz
		32	32, 64	511.719	390.625	322.266	MHz
		20	20, 40	409.375	312.500	257.813	MHz
		40	40, 80	409.375	312.500	257.813	MHz
F_{TXIN2}	TXUSRCLK2 [5] maximum frequency	16	16	511.719	390.625	322.266	MHz
		16	32	255.859	195.313	161.133	MHz
		32	32	511.719	390.625	322.266	MHz
		32	64	255.859	195.313	161.133	MHz

Symbol	Description [1]	Data Width Conditions (bit)		Speed Grade and V_{CCINT} Operating Vo			
				0.85V		0.72V	
		Internal Logic	Interconnect Logic	-2 [2]	-1 [3, 4]	-1 [4]	
		20	20	409.375	312.500	257.813	MHz
		20	40	204.688	156.250	128.906	MHz
		40	40	409.375	312.500	257.813	MHz
		40	80	204.688	156.250	128.906	MHz
F_{RXIN2}	RXUSRCLK2 [5] maximum frequency	16	16	511.719	390.625	322.266	MHz
		16	32	255.859	195.313	161.133	MHz
		32	32	511.719	390.625	322.266	MHz
		32	64	255.859	195.313	161.133	MHz
		20	20	409.375	312.500	257.813	MHz
		20	40	204.688	156.250	128.906	MHz
		40	40	409.375	312.500	257.813	MHz
		40	80	204.688	156.250	128.906	MHz

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceivers User Guide* (UG576).
2. For speed grades -2E and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grades -1E, -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
4. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
5. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *UltraScale Architecture GTH Transceivers User Guide* (UG576).

Table: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTHTX}	Serial data rate range		0.500	–	F_{GTHMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps

Symbol	Description	Condition	Min	Typ	Max	Units
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew [1]		–	–	500.00	ps
$T_{J16.375}$	Total jitter [2, 4]	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J15.0}$	Total jitter [2, 4]	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J14.1}$	Total jitter [2, 4]	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J14.1}$	Total jitter [2, 4]	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J13.1}$	Total jitter [2, 4]	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J12.5\_QPLL}$	Total jitter [2, 4]	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter [3, 4]	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter [3, 4]		–	–	0.17	UI
$T_{J11.3\_QPLL}$	Total jitter [2, 4]	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3\_QPLL}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J10.3125\_QPLL}$	Total jitter [2, 4]	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter [3, 4]	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter [3, 4]		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter [2, 4]	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J9.953\_CPLL}$	Total jitter [3, 4]	9.953 Gb/s	–	–	0.33	UI

Symbol	Description	Condition	Min	Typ	Max	Units
$D_{J9.953\_CPLL}$	Deterministic jitter [3, 4]		–	–	0.17	UI
$T_{J8.0}$	Total jitter [3, 4]	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter [3, 4]		–	–	0.17	UI
$T_{J6.6}$	Total jitter [3, 4]	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter [3, 4]		–	–	0.15	UI
$T_{J5.0}$	Total jitter [3, 4]	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter [3, 4]		–	–	0.15	UI
$T_{J4.25}$	Total jitter [3, 4]	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter [3, 4]		–	–	0.15	UI
$T_{J4.0}$	Total jitter [3, 4]	4.0 Gb/s	–	–	0.32	UI
$D_{J4.0}$	Deterministic jitter [3, 4]		–	–	0.16	UI
$T_{J3.20}$	Total jitter [3, 4]	3.20 Gb/s [5]	–	–	0.20	UI
$D_{J3.20}$	Deterministic jitter [3, 4]		–	–	0.10	UI
$T_{J2.5}$	Total jitter [3, 4]	2.5 Gb/s [6]	–	–	0.20	UI
$D_{J2.5}$	Deterministic jitter [3, 4]		–	–	0.10	UI
$T_{J1.25}$	Total jitter [3, 4]	1.25 Gb/s[7]	–	–	0.15	UI
$D_{J1.25}$	Deterministic jitter [3, 4]		–	–	0.06	UI
T_{J500}	Total jitter [3, 4]	500 Mb/s [8]	–	–	0.10	UI
D_{J500}	Deterministic jitter [3, 4]		–	–	0.03	UI

Symbol	Description	Condition	Min	Typ	Max	Units

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTH Quad) at the maximum line rate.
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
8. CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Table: GTH Transceiver Receiver Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTHRX}	Serial data rate		0.500	–	F_{GTHMAX}	Gb/s
R_{XSST}	Receiver spread-spectrum tracking [1]	Modulated at 33 kHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)		–	–	256	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance [2]						
$J_{T\_SJ16.375}$	Sinusoidal jitter (QPLL) [3]	16.375 Gb/s	0.30	–	–	UI
$J_{T\_SJ15.0}$	Sinusoidal jitter (QPLL) [3]	15.0 Gb/s	0.30	–	–	UI
$J_{T\_SJ14.1}$	Sinusoidal jitter (QPLL) [3]	14.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ13.1}$	Sinusoidal jitter (QPLL) [3]	13.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ12.5}$	Sinusoidal jitter (QPLL) [3]	12.5 Gb/s	0.30	–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (QPLL) [3]	11.3 Gb/s	0.30	–	–	UI

Symbol	Description	Condition	Min	Typ	Max	Units
$J_{T\_SJ10.32\_QPLL}$	Sinusoidal jitter (QPLL) [3]	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_CPLL}$	Sinusoidal jitter (CPLL) [3]	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_QPLL}$	Sinusoidal jitter (QPLL) [3]	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_CPLL}$	Sinusoidal jitter (CPLL) [3]	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ8.0}$	Sinusoidal jitter (QPLL) [3]	8.0 Gb/s	0.42	–	–	UI
$J_{T\_SJ6.6\_CPLL}$	Sinusoidal jitter (CPLL) [3]	6.6 Gb/s	0.44	–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL) [3]	5.0 Gb/s	0.44	–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL) [3]	4.25 Gb/s	0.44	–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL) [3]	3.2 Gb/s [4]	0.45	–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL) [3]	2.5 Gb/s [5]	0.30	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL) [3]	1.25 Gb/s [6]	0.30	–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL) [3]	500 Mb/s [7]	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye [2]						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye [8]	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye [8]	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Electrical Compliance

The *UltraScale Architecture GTH Transceivers User Guide* (UG576) contains recommended use modes that ensure compliance for the protocols listed in the following table. The transceiver wizard

provides the recommended settings for those use cases and for protocol specific characteristics.

Table: GTH Transceiver Protocol List

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR [1]	IEEE 802.3-2012	10.3125	Compliant
40GBASE-KR	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
TFI-5	OIF-TFI5-0.1.0	2.488	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11G-SR	4.25–12.5	Compliant
PCIe Gen1, 2, 3, 4	PCI Express base 4.0	2.5, 5.0, 8.0, and 16.0	Compliant
SDI [2]	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI [2]	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys Bandwidth Engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
HDMI [2]	HDMI 2.0	All	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort [2]	DP 1.2B CTS	1.62–5.4	Compliant
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625–12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	up to 11.180997	Compliant

1. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
2. This protocol requires external circuitry to achieve compliance.

GTY Transceiver Specifications

The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists the Artix UltraScale+ FPGAs that include the GTY transceivers.

GTY Transceiver DC Input and Output Levels

Table 1 summarizes the DC specifications of the GTY transceivers in Artix UltraScale+ FPGAs. Consult the *UltraScale Architecture GTY Transceivers User Guide* (UG578) for further details.

Table: GTY Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled $V_{MGTAVTT}$ = 1.2V	–400	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage [1]	Transmitter output swing is set to 11111	800	–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 – D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} – D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM} [2]				mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled	Equation based	$V_{MGTAVTT} – D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance		–	100	–	Ω
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor [3]		–	100	–	nF

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceivers User Guide* (UG578) and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

Figure: Single-Ended Peak-to-Peak Voltage

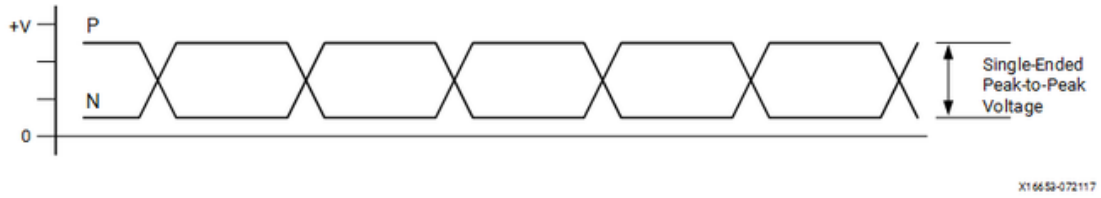
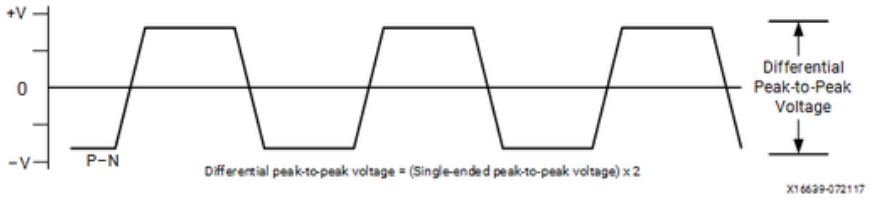


Figure: Differential Peak-to-Peak Voltage



The following tables summarize the DC specifications of the clock input/output levels of the GTY transceivers in Artix UltraScale+ FPGAs. Consult the *UltraScale Architecture GTY Transceivers User Guide* (UG578) for further details.

Table: GTY Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table: GTY Transceiver Clock Output Level Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	R_T = 100Ω across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	R_T = 100Ω across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	R_T = 100Ω across P and N signals	300	–	500	mV

GTY Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTY Transceivers User Guide* (UG578) for further information.

Table: GTY Transceiver Performance

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages						Units
			0.85V				0.72V		
			-2		-1		-1		
F_{GTYMAX}	GTY maximum line rate		16.375 [1]		16.375 [1]		12.5		Gb/s
F_{GTYMIN}	GTY minimum line rate		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	
$F_{GTYCRANGE}$	CPLL line rate range [2]	1	4.0	12.5	4.0	8.5	4.0	8.5	Gb/s
		2	2.0	6.25	2.0	4.25	2.0	4.25	Gb/s
		4	1.0	3.125	1.0	2.125	1.0	2.125	Gb/s
		8	0.5	1.5625	0.5	1.0625	0.5	1.0625	Gb/s
		16	N/A						Gb/s
		32	N/A						Gb/s
			Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE1}$	QPLL0 line rate range [3]	1	9.8	16.375	9.8	16.375	9.8	12.5	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.0938	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0469	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	Gb/s
			Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE2}$	QPLL1 line rate range [4]	1	16.0	16.375	16.0	16.375	N/A		Gb/s
		1	8.0	13.0	8.0	12.5	8.0	12.5	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages						Units
			0.85V				0.72V		
			-2		-1		-1		
$F_{CPLLRANGE}$	CPLL frequency range		2.0	6.25	2.0	4.25	2.0	4.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	GHz

1. GTY transceiver line rates are package limited: UBVA368, SBVB484, SFVB784 to 12.5 Gb/s.
2. The values listed are the rounded results of the calculated equation (2 × CPLL_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (QPLL0_Frequency × RATE)/Output_Divider where RATE is 1 when QPLL0_CLKOUT_RATE is set to HALF and 2 if QPLL0_CLKOUT_RATE is set to FULL.
4. The values listed are the rounded results of the calculated equation (QPLL1_Frequency × RATE)/Output_Divider where RATE is 1 when QPLL1_CLKOUT_RATE is set to HALF and 2 if QPLL1_CLKOUT_RATE is set to FULL.

Table: GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	All Speed Grades	Units
$F_{GTYDRPCLK}$	GTYDRPCLK maximum frequency	250	MHz

Table: GTY Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	820	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

Table: GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask

Symbol	Description [1, 2]	Offset Frequency	Min	Typ	Max	Units

Symbol	Description [1, 2]	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 625 MHz	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
$CPLL_{REFCLKMASK}$	CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

1. For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.
2. This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table: GTY Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock.		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE)	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled		–	50,000	2.3×10^6	UI

Table: GTY Transceiver User Clock Switching Characteristics

Symbol	Description [1]	Data Width Conditions (bits)		Speed Grade and V_{CCINT} Operating Voltages			Units
				0.85V		0.72V	
		Internal Logic	Interconnect Logic	-2 [2]	-1 [3, 5]	-1 [4]	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	402.891	322.266	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	402.891	322.266	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK [6] maximum frequency	16	16, 32	511.719	390.625	322.266	MHz
		32	32, 64	511.719	390.625	322.266	MHz
		64	64, 128	255.859	255.859	195.313	MHz
		20	20, 40	409.375	312.500	257.813	MHz
		40	40, 80	409.375	312.500	257.813	MHz
		80	80, 160	204.688	204.688	156.250	MHz
F_{RXIN}	RXUSRCLK [6] maximum frequency	16	16, 32	511.719	390.625	322.266	MHz
		32	32, 64	511.719	390.625	322.266	MHz

Symbol	Description [1]	Data Width Conditions		Speed Grade and V_{CCINT} Operating Voltages			Units
				0.85V		0.72V	
		Internal Logic	Interconnect Logic	-2 [2]	-1 [3, 5]	-1 [4]	
		64	64, 128	255.859	255.859	195.313	MHz
		20	20, 40	409.375	312.500	257.813	MHz
		40	40, 80	409.375	312.500	257.813	MHz
		80	80, 160	204.688	204.688	156.250	MHz
F_{TXIN2}	TXUSRCLK2 [6] maximum frequency	16	16	511.719	390.625	322.266	MHz
		16	32	255.859	195.313	161.133	MHz
		32	32	511.719	390.625	322.266	MHz
		32	64	255.859	195.313	161.133	MHz
		64	64	255.859	255.859	195.313	MHz
		64	128	127.930	127.930	97.656	MHz
		20	20	409.375	312.500	257.813	MHz
		20	40	204.688	156.250	128.906	MHz
		40	40	409.375	312.500	257.813	MHz
		40	80	204.688	156.250	128.906	MHz
		80	80	204.688	204.688	156.250	MHz
		80	160	102.344	102.344	78.125	MHz
F_{RXIN2}	RXUSRCLK2 [6] maximum frequency	16	16	511.719	390.625	322.266	MHz
		16	32	255.859	195.313	161.133	MHz
		32	32	511.719	390.625	322.266	MHz
		32	64	255.859	195.313	161.133	MHz
		64	64	255.859	255.859	195.313	MHz
		64	128	127.930	127.930	97.656	MHz
		20	20	409.375	312.500	257.813	MHz
		20	40	204.688	156.250	128.906	MHz
		40	40	409.375	312.500	257.813	MHz
		40	80	204.688	156.250	128.906	MHz

Symbol	Description [1]	Data Width Conditions (bits)		Speed Grade and V_{CCINT} Operating Voltages			Units
				0.85V		0.72V	
		Internal Logic	Interconnect Logic	-2 [2]	-1 [3, 5]	-1 [4]	
		80	80	204.688	204.688	156.250	MHz
		80	160	102.344	102.344	78.125	MHz

1. Clocking must be implemented as described in the *UltraScale Architecture GTY Transceivers User Guide* (UG578).
2. For speed grades -2E and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grades -1E, and -1I a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
4. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
5. For the speed grades -1E and -1I, only a 64- or 80-bit internal data path can be used for line rates above 12.5 Gb/s.
6. When the gearbox is used, these maximums refer to the XCLK. For more information, see the Valid Data Width Combinations for TX Asynchronous Gearbox table in the *UltraScale Architecture GTY Transceivers User Guide* (UG578).

Table: GTY Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYTX}	Serial data rate range		0.500	–	F_{GTYMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew [1]		–	–	500.00	ps
$T_{J16.375}$	Total jitter [2, 4]	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J15.0}$	Total jitter [2, 4]	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J14.1}$	Total jitter [2, 4]	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter [2, 4]		–	–	0.17	UI

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{J14.1}$	Total jitter [2, 4]	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J13.1}$	Total jitter [2, 4]	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J12.5\_QPLL}$	Total jitter [2, 4]	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter [3, 4]	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter [3, 4]		–	–	0.17	UI
$T_{J11.3\_QPLL}$	Total jitter [2, 4]	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3\_QPLL}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J10.3125\_QPLL}$	Total jitter [2, 4]	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter [3, 4]	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter [3, 4]		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter [2, 4]	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter [2, 4]		–	–	0.17	UI
$T_{J9.953\_CPLL}$	Total jitter [3, 4]	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953\_CPLL}$	Deterministic jitter [3, 4]		–	–	0.17	UI
$T_{J8.0}$	Total jitter [3, 4]	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter [3, 4]		–	–	0.17	UI
$T_{J6.6}$	Total jitter [3, 4]	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter [3, 4]		–	–	0.15	UI
$T_{J5.0}$	Total jitter [3, 4]	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter [3, 4]		–	–	0.15	UI
$T_{J4.25}$	Total jitter [3, 4]	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter [3, 4]		–	–	0.15	UI

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{J3.20}$	Total jitter [3, 4]	3.20 Gb/s [5]	–	–	0.20	UI
$D_{J3.20}$	Deterministic jitter [3, 4]		–	–	0.10	UI
$T_{J2.5}$	Total jitter [3, 4]	2.5 Gb/s [6]	–	–	0.20	UI
$D_{J2.5}$	Deterministic jitter [3, 4]		–	–	0.10	UI
$T_{J1.25}$	Total jitter [3, 4]	1.25 Gb/s [7]	–	–	0.15	UI
$D_{J1.25}$	Deterministic jitter [3, 4]		–	–	0.06	UI
T_{J500}	Total jitter [3, 4]	500 Mb/s [8]	–	–	0.10	UI
D_{J500}	Deterministic jitter [3, 4]		–	–	0.03	UI

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
8. CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Table: GTY Transceiver Receiver Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYRX}	Serial data rate		0.500	–	F_{GTYMAX}	Gb/s
R_{XSST}	Receiver spread-spectrum tracking [1]	Modulated at 33 kHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)		–	–	256	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm

Symbol	Description	Condition	Min	Typ	Max	Units
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance [2]						
$J_{T\_SJ16.375}$	Sinusoidal jitter (QPLL) [3]	16.375 Gb/s	0.30	–	–	UI
$J_{T\_SJ15.0}$	Sinusoidal jitter (QPLL) [3]	15.0 Gb/s	0.30	–	–	UI
$J_{T\_SJ14.1}$	Sinusoidal jitter (QPLL) [3]	14.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ13.1}$	Sinusoidal jitter (QPLL) [3]	13.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ12.5}$	Sinusoidal jitter (QPLL) [3]	12.5 Gb/s	0.30	–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (QPLL) [3]	11.3 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_QPLL}$	Sinusoidal jitter (QPLL) [3]	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_CPLL}$	Sinusoidal jitter (CPLL) [3]	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_QPLL}$	Sinusoidal jitter (QPLL) [3]	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_CPLL}$	Sinusoidal jitter (CPLL) [3]	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ8.0}$	Sinusoidal jitter (CPLL) [3]	8.0 Gb/s	0.42	–	–	UI
$J_{T\_SJ6.6}$	Sinusoidal jitter (CPLL) [3]	6.6 Gb/s	0.44	–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL) [3]	5.0 Gb/s	0.44	–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL) [3]	4.25 Gb/s	0.44	–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL) [3]	3.2 Gb/s [4]	0.45	–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL) [3]	2.5 Gb/s [5]	0.30	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL) [3]	1.25 Gb/s [6]	0.30	–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL) [3]	500 Mb/s [7]	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye [2]						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye [8]	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye [8]	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

Symbol	Description	Condition	Min	Typ	Max	Units

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceivers User Guide* (UG578) contains recommended use modes that ensure compliance for the protocols listed in the following table. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table: GTY Transceiver Protocol List

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
OTU4 (OTL4.4) CFP	OIF-CEI-11G-MR	11.18–13.1	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR [1]	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
QSGMII	QSGMII v1.2 (Cisco System, ENG-46158)	5	Compliant
OTU2	ITU G.8251	10.709225	Compliant

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI [2]	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI [2]	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys bandwidth engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort	DP 1.2B CTS	1.62–5.4	Compliant [2]
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

1. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
2. This protocol requires external circuitry to achieve compliance.

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express® designs can be found at PCI Express . The *UltraScale Architecture and Product Data Sheet: Overview* (DS890) lists how many

blocks are in each Artix UltraScale+ FPGA.

Table: Maximum Performance for PCIE4-based PCI Express Designs

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
$F_{PIPECLK}$	Pipe clock maximum frequency	250.00	250.00	250.00	MHz
$F_{CORECLK}$	Core clock maximum frequency	500.00	500.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	MHz
$F_{MCAPCLK}$	MCAP clock maximum frequency [1]	125.00	125.00	125.00	MHz

1. For information on tandem PCIe support, see the *UltraScale+ Devices Integrated Block for PCI Express LogiCORE IP Product Guide* (PG213).

The PCIE4C blocks in the XCAU10P and XCAU15P include support for the CCIX protocol.

Table: Maximum Performance for PCIE4C-based PCI Express and CCIX Designs

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
$F_{PIPECLK}$	Pipe clock maximum frequency	250.00	250.00	250.00	MHz
$F_{CORECLK}$	Core clock maximum frequency	500.00	500.00	250.00	MHz
$F_{CORECLKCCIX}$	CCIX TL interface clock maximum frequency	500.00	500.00	N/A	MHz
F_{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	MHz
$F_{MCAPCLK}$	MCAP clock maximum frequency [1]	125.00	125.00	125.00	MHz

1. For information on tandem PCIe support in XCAU10P and XCAU15P devices, see the *UltraScale+ Devices Integrated Block for PCI Express LogiCORE IP Product Guide* (PG213).

System Monitor Specifications

Table: System Monitor Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ±3%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy [1]						
Resolution			10	–	–	Bits
Integral nonlinearity [2]	INL		–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset error		Offset calibration enabled	–	–	±2	LSBs
Gain error			–	–	±0.4	%
Sample rate			–	–	0.2	MS/s
RMS code noise		External 1.25V reference	–	–	1	LSBs
		On-chip reference	–	1	–	LSBs
ADC Accuracy at Extended Temperatures						
Resolution		T_j = –55°C to 125°C	10	–	–	Bits
Integral nonlinearity [2]	INL	T_j = –55°C to 125°C	–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic T_j = –55°C to 125°C	–	–	±1	
Analog Inputs [2]						
ADC input ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
On-Chip Sensor Accuracy						
Temperature sensor error [1, 3]		T_j = –55°C to 125°C (with external REF)	–	–	±3	°C
		T_j = –55°C to 110°C (with internal REF)	–	–	±3.5	°C
		T_j = 110°C to 125°C (with internal REF)	–	–	±5	°C
Supply sensor error [4]		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with external REF)	–	–	±0.5	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –40°C to 100°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –55°C to 125°C (with external REF)	–	–	±2.0	%
		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with internal REF)	–	–	±1.0	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with internal REF)	–	–	±2.0	%
		All other supply voltages, T_j = –40°C to 100°C (with internal REF)	–	–	±1.5	%
		All other supply voltages, T_j = –55°C to 125°C (with internal REF)	–	–	±2.5	%
Conversion Rate [5]						
Conversion time—continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Conversion time—event	t_{CONV}	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
DCLK duty cycle			40	–	60	%
SYSMON Reference [6]						
External reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, T_j = –55°C to 125°C	1.225	1.25	1.275	V

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. See the Analog Input section in the *UltraScale Architecture System Monitor User Guide* (UG580).
3. When reading temperature values directly from the PMBus interface, the SYSMON has a +4°C offset due to the transfer function used by the PMBus application. For example, the external REF temperature sensor error's range of ±3°C becomes +1°C to +7°C when the temperature is read through the PMBus interface.
4. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
5. See the Adjusting the Acquisition Settling Time section in the *UltraScale Architecture System Monitor User Guide* (UG580).
6. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

SYSMON I2C/PMBus Interfaces

Table: SYSMON I2C Fast Mode Interface Switching Characteristics

Symbol	Description [1]	Min	Max	Units

Symbol	Description [1]	Min	Max	Units
T_{SMFCKL}	SCL Low time	1.3	–	µs
T_{SMFCKH}	SCL High time	0.6	–	µs
T_{SMFCKO}	SDAO clock-to-out delay	–	900	ns
T_{SMFDCK}	SDAI setup time	100	–	ns
F_{SMFCLK}	SCL clock frequency	–	400	kHz

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Table: SYSMON I2C Standard Mode Interface Switching Characteristics

Symbol	Description [1]	Min	Max	Units
T_{SMSCKL}	SCL Low time	4.7	–	µs
T_{SMSCKH}	SCL High time	4.0	–	µs
T_{SMSCKO}	SDAO clock-to-out delay	–	3450	ns
T_{SMSDCK}	SDAI setup time	250	–	ns
F_{SMSCLK}	SCL clock frequency	–	100	kHz

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Configuration Switching Characteristics

Table: Configuration Switching Characteristics

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
Power-up Timing Characteristics					
T_{PL}	Program latency	7.5	7.5	7.5	ms, Max
T_{POR}	Power-on reset (40 ms maximum ramp rate)	65	65	65	ms, Max

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
		0	0	0	ms, Min
	Power-on reset with POR override (2 ms maximum ramp rate)	15	15	15	ms, Max
		5	5	5	ms, Min
$T_{PROGRAM}$	Program pulse width	250	250	250	ns, Min
CCLK Output (Master Mode)					
T_{ICCK}	Master CCLK output delay from INIT_B	150	150	150	ns, Min
T_{MCCKL} [1]	Master CCLK clock Low time duty cycle	40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle	40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master SPI (x1/x2/x4) CCLK frequency	150	150	125	MHz, Max
	Master SPI (x8) or Master BPI (x8/x16) [2] CCLK frequency	150	150	125	
F_{MCCK_START}	Master CCLK frequency at start of configuration	2.70	2.70	2.70	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK	±15	±15	±15	%, Max
CCLK Input (Slave Mode)					
T_{SCCKL}	Slave CCLK clock minimum Low time	2.5	2.5	2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.5	2.5	2.5	ns, Min
F_{SCCK}	Slave serial CCLK frequency	125	125	125	MHz, Max
	Slave SelectMAP CCLK frequency	125	125	125	
EMCCLK Input (Master Mode)					
T_{EMCCKL}	External master CCLK Low time	2.5	2.5	2.5	ns, Min

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
T_{EMCCKH}	External master CCLK High time	2.5	2.5	2.5	ns, Min
F_{EMCCK}	External master CCLK frequency with Master SPI x1/x2/x4	150	150	125	MHz, Max
	External master CCLK frequency with Master SPI x8 or Master BPI x8/x16 [2]	150	150	125	
Internal Configuration Access Port					
F_{ICAPCK}	Internal configuration access port (ICAPE3)	200	200	150	MHz, Max
Slave Serial Mode Programming Switching					
T_{DCCK}/T_{CCKD}	D_{IN} setup/hold	3.0/0	3.0/0	4.0/0	ns, Min
T_{CCO}	D_{OUT} clock to out	8.0	8.0	9.0	ns, Max
SelectMAP Mode Programming Switching					
T_{SMDCCK}/T_{SMCCKD}	D[31:00] setup/hold	3.5/0	3.5/0	4.5/0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B setup/hold	4.0/0	4.0/0	5.0/0	ns, Min
T_{SMWCCK}/T_{SMCCKW}	RDWR_B setup/hold	10.0/0	10.0/0	11.0/0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330Ω pull-up resistor required)	7.0	7.0	7.0	ns, Max
T_{SMCO}	D[31:00] clock to out in readback	8.0	8.0	8.0	ns, Max
F_{RBCCK}	Readback frequency	125	125	125	MHz, Max
Boundary-Scan Port Timing Specifications					
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup/hold	3.0/2.0	3.0/2.0	3.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	7.0	7.0	7.0	ns, Max
F_{TCK}	TCK frequency	66	66	66	MHz, Max

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
BPI Master Flash Mode Programming Switching					
T_{BPICCO}	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out	10	10	10	ns, Max
T_{BPIDCC}/T_{BPICCD}	D[15:00] setup/hold	3.5/0	3.5/0	4.5/0	ns, Min
SPI Master Flash Mode Programming Switching					
T_{SPIDCC}/T_{SPICCD}	D[03:00] setup/hold	3.0/0	3.0/0	4.0/0	ns, Min
T_{SPIDCC}/T_{SPICCD}	D[07:04] setup/hold	3.5/0	3.5/0	4.5/0	ns, Min
T_{SPICCM}	MOSI clock to out	8.0	8.0	8.0	ns, Max
$T_{SPICCM2}$	D[04] clock to out	10.0	10.0	10.0	ns, Max
$T_{SPICCFC}$	FCS_B clock to out	8.0	8.0	8.0	ns, Max
$T_{SPICCFC2}$	FCS2_B clock to out	10.0	10.0	10.0	ns, Max
DNA Port Switching					
F_{DNACK}	DNA port frequency	200	200	175	MHz, Max
STARTUPE3 Ports					
$T_{USRCCLKO}$	STARTUPE3 USRCCLKO input port to CCLK pin output delay	0.25/6.50	0.25/7.50	0.25/9.00	ns, Min/Max
T_{DO}	DO[3:0] ports to D03-D00 pins output delay	0.25/7.70	0.25/8.40	0.25/10.00	ns, Min/Max
T_{DTS}	DTS[3:0] ports to D03-D00 pins 3-state delays	0.25/7.70	0.25/8.40	0.25/10.00	ns, Min/Max
T_{FCSBO}	FCSBO port to FCS_B pin output delay	0.25/7.50	0.25/8.40	0.25/9.80	ns, Min/Max
T_{FCSBTS}	FCSBTS port to FCS_B pin 3-state delay	0.25/7.50	0.25/8.40	0.25/9.80	ns, Min/Max

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages			Units
		0.85V		0.72V	
		-2	-1	-1	
$T_{USRDONEO}$	USRDONEO port to DONE pin output delay	0.25/9.40	0.25/10.50	0.25/12.10	ns, Min/Max
$T_{USRDONETS}$	USRDONETS port to DONE pin 3-state delay	0.25/9.40	0.25/10.50	0.25/12.10	ns, Min/Max
T_{DI}	D03-D00 pins to DI[3:0] ports input delay	0.5/3.1	0.5/3.5	0.5/4.0	ns, Min/Max
$F_{CFGMCLK}$	STARTUPE3 CFGMCLK output frequency	50	50	50	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE3 CFGMCLK output frequency tolerance	±15	±15	±15	%, Max
T_{DCI_MATCH}	Specifies a stall in the start-up cycle until the digitally controlled impedance (DCI) match signals are asserted	4	4	4	ms, Max

1. When the CCLK is sourced from the EMCCLK pin with a divide-by-one setting, the external EMCCLK must meet this duty-cycle requirement.
2. SPI mode is recommended for master mode configuration from flash memory because of the higher configuration rates and low configuration interface pin counts. Due to the obsolescence of synchronous read-mode flash devices, BPI mode performance is limited. For system configuration rates with SPI flash and parallel NOR flash in BPI asynchronous read mode see the *UltraScale Architecture Configuration User Guide* (UG570).

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
04/13/2022 Version 1.2	
Recommended Operating Conditions	Updated note 1 and 4.
Table 1	Added new table.
Table 4	Updated note 8.

Section	Revision Summary
AC Switching Characteristics	Updated to production release the XCAU10P and XCAU15P in Vivado Design Suite 2022.1 v1.29.
Speed Grade Designations	Updated the following devices in Vivado Design Suite 2022.1 v1.29 for the following speed/temperature grades: XCAU10P: -2E, -2I, -1E, -1I, -1LI, -1LI (V_{CCINT} = 0.72V) XCAU15P: -2E, -2I, -1E, -1I, -1LI, -1LI (V_{CCINT} = 0.72V)
Production Silicon and Software Status	Moved all speed grades of the XCAU10P and XCAU15P from advance to production.
Table 5	• In DDR4 memory standard, updated data rates for FFVB676 and SFVB784 packages, and added rates for SBVB484 and UBVA368 packages. • In DDR3 memory standard, updated data rates for FFVB676 package, and added rates for SBVB484 and UBVA368 packages. • In DDR3L memory standard, updated data rates for FFVB676 package, and added rates for SBVB484 and UBVA368 packages. • In QDR IV XP memory standard, broke out data rates by package. • In RLDRAM 3 memory standard, updated data rates for FFVB676 package, and added rates for SBVB484 and UBVA368 packages. • In LPDDR3 memory standard, added data rates for SBVB484 and UBVA368 packages. • Removed note about DDR4 DDP components.
Package Parameter Guidelines	Added package skew values for XCAU10P and XCAU15P devices in UBVA368 and SBVB484 packages.

Section	Revision Summary
Table 1	Added SBVB484 and UBVA368 packages to note 1.
Table 1	Updated to PCIe Gen1, 2, 3, 4 protocol.
Table 1	Removed line rate of 16.3 Gb/s for SFVB784 package from note 1.
10/20/2021 Version 1.1	
AC Switching Characteristics	Updated to production release the XCAU20P in Vivado Design Suite 2021.2 v1.28.
Speed Grade Designations	Updated the following devices in Vivado Design Suite 2021.2 v1.28 for the following speed/temperature grades: XCAU20P: -2E, -2I, -1E, -1I, -1LI XCAU25P: -1LI (V_{CCINT} = 0.72V)
Production Silicon and Software Status	Updated the following devices in Vivado Design Suite 2021.2 v1.28 for the following speed/temperature grades: XCAU20P: -2E, -2I, -1E, -1I, -1LI XCAU25P: -1LI (V_{CCINT} = 0.72V) moved from 2021.1.1 to 2021.2.
Quiescent Supply Current	Filled in data for XCAU10P, XCAU15P, and XCAU20P. Updated data for XCAU25P.
Device Pin-to-Pin Output Parameter Guidelines	Added XCAU20P values in the tables.
Device Pin-to-Pin Input Parameter Guidelines	Added XCAU20P values in the tables.
Package Parameter Guidelines	Added XCAU20P values in the table.
08/03/2021 Version 1.0	
Initial release.	N/A

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