D.I.C.E

Dynamic Image Compression Engine

Theory of Operation

John Hofmeyr - 04/05/2024

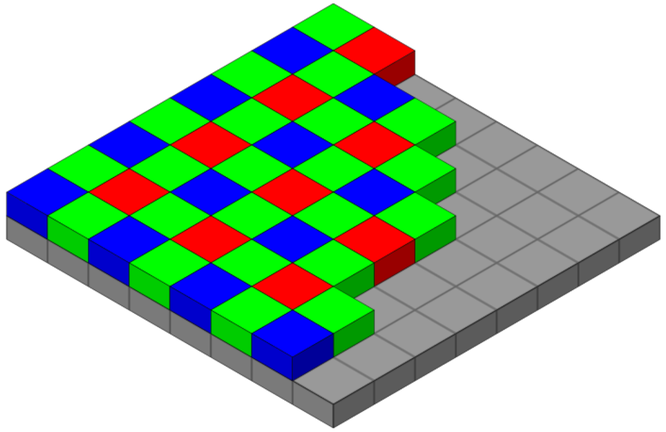
D.I.C.E| Stage 1 - Image capture

Image Sensor Output

- IMX477 sensor captures 4056x3040 10-bit RAW images
- Maximum frame rate of 60FPS
- Each frame requires ~124Mb to store
- ~7.4Gb/s of bandwidth needed for 60FPS stream
- Images are received in Bayer mosaic form

Sample Image from Sensor

Bayer Mosaic Sensor Format



D.I.C.E | Stage 2 - Image Ingest & Tiling

Image Ingest

- FPGA receives image data via 4 Lane MIPI bus @ 2.1Gb/s per lane
- Image is scanned from top left to bottom right, image frame is buffered in DRAM

Image Tiling

- Image is divided into NxN image tile grid
- Grid is user selectable, must be 2x2, 3x3 or 4x4
  - Limited by resource availability on FPGA
  - Higher tile count increases resource usage

4x4 Image tile | 1014x760px blocks

D.I.C.E | Stage 3 - Image Pre-processing

4x4 Image tile | 1014x760px blocks

Tile (2,3)

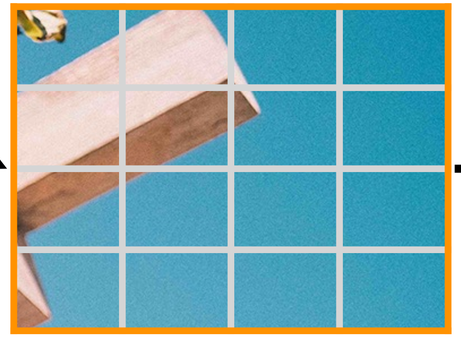
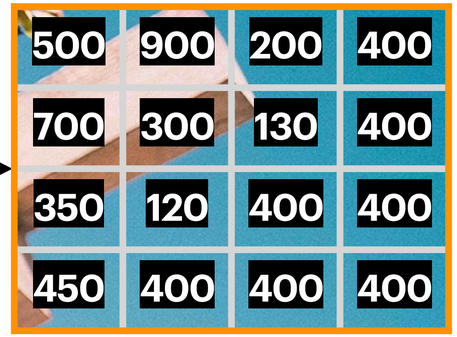


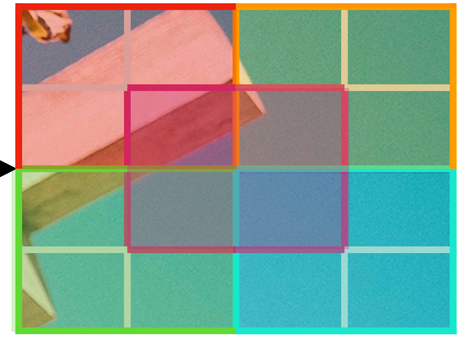
Image Tile Pixel Groups

Pixel Group Average Intensity (0-1024)

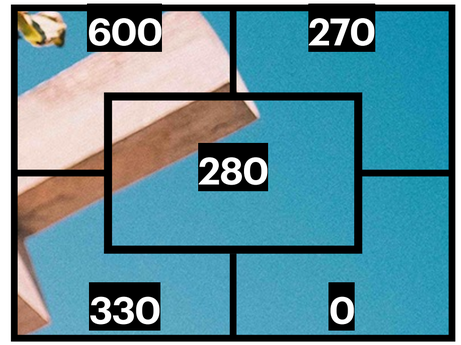


Each Sub-Tile is averaged

Image Tile Intensity Comparison



Intensity Differences



Tile Contrast Weight = 296

Image Tile Pixel Groups

- Image Tiles and subdivided into 4x4 grids (Pixel Groups)
- Image contains a total of 256 Pixel groups
- Pixel groups contain 48,165 pixels each

Pixel Group Processing

- Pixel intensities are averaged for each pixel group
- Resulting 16 average intensities are compared in blocks of 4 sub-tiles, 5 comparisons total
- Difference in intensity is calculated for each comparison
  - Two tiles with largest intensity difference are subtracted
- Intensity differences are averaged to obtain the **Contrast Wight**

*Intensity Values are for example only

D.I.C.E | Stage 4 - Image Tile Compression Weights

Image Tile Location Weights

- Tile location weights infer that primary image detail is located in center of image
- Location weight increases from center of image out
- Location Weight determines contrast weight increase

Image Tile Compression Weights

- Location Weight = 0
  - No contrast weight increase
- Location Weight = 1
  - Increases contrast weight by 50%
- Location Weight = 2
  - Increases contrast weight by 100%

Compression Ratio Calculation

- Final weight values for Image tile used as input to lookup table
- Compression ratios range from 0-3
- Compression ratio used to re-size image tiles after compression for tile restitching

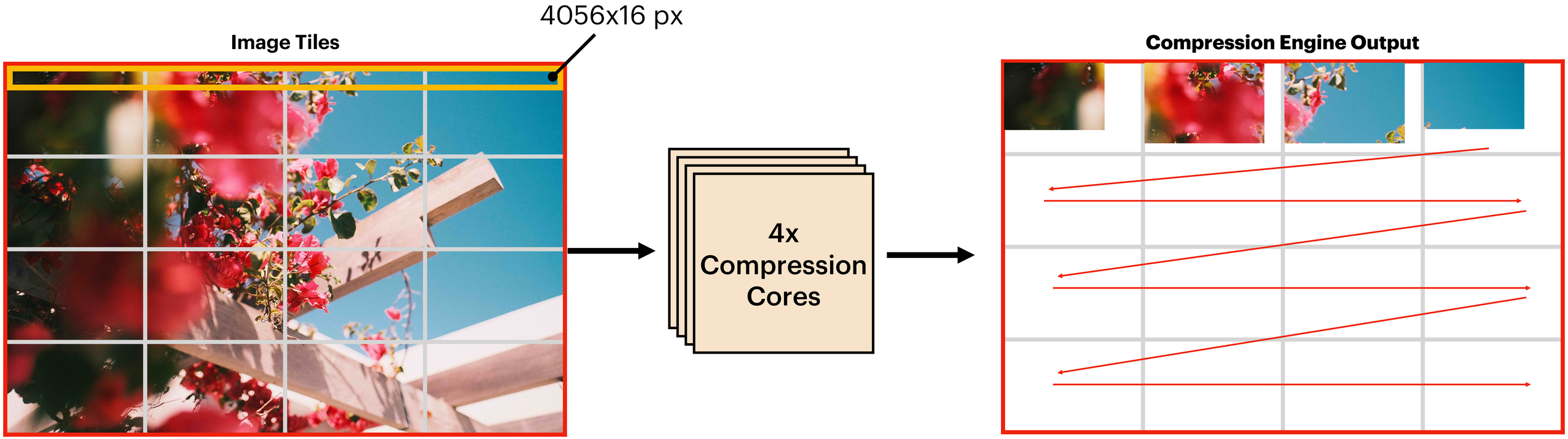
4x4 Image tile | 1014x760px blocks

LW:2	LW:1	LW:1	LW:2
LW:1	LW: 0	LW:0	LW:1
LW:1	LW:0	LW:0	LW:1
LW:2	LW:1	LW:1	LW:2

D.I.C.E | Stage 5 - Image Tile Compression

Image Compression Engine

- Tiles are loaded into FPGA BRAM in chunks of 16 Pixel Rows
  - Requires ~650Kb
- Lossy or Lossless compression is applied
- Compression engine output is buffered into 2nd 650Kb BRAM block
- Data transactions from RAM to BRAM are done in 650Kb blocks



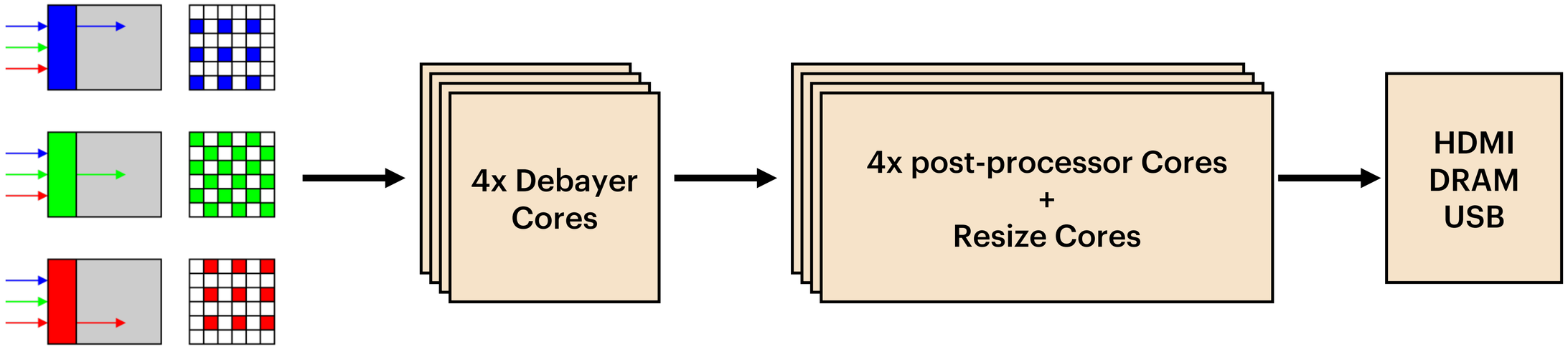
D.I.C.E | Stage 6 - Image Tile De-bayer & Re-size

Image Tile De-bayer

- After compression, image tiles pass through 4x debayer cores
  - Bilinear, nearest neighbor or edge detect

Image Tile Pre-processor

- Debayered RGB image is passed through RGB-HSV-RGB Post-processor
  - Can apply color correction to image
- Final image re-sized to match original image capture size or match user defied resolution
  - Final image stored in RAM, Displayed over HDMI or formatted as JPEG and sent to host machine via USB



D.I.C.E | System Resources

XC7A200T FPGA

- 215,360 Logic Cells
  - 33,650 Logic Slices
- 2.88Mb Distributed RAM
- 13.14Mb Block Ram
  - 36Kb Dual Port BRAMs With FIFO & ECC
- 740 DSP48E1 Cores
  - 25x18b two’s-complement Multiplier
  - 48-b Accumulator
  - Add/Sub/Accumulate SIMD
    - Dual 24b or Quad 12b Add,Sub,Accumulate
  - ALU
    - AND, OR, NOT, NAD, NOR, XOR, XNOR
  - Patern Detector
- 12W Maximum Power Dissipation
- 10A on VCCINT (1V)
- 1A on VCCIO/VCCAUX (1V8)

DDR2 DRAM

- MT47H64M16NF-25E IT:M
  - 1Gb (64M x 16)
  - 16b Data bus @ 400Mhz (800MT/s)
  - 1.6GB/s or 12.8Gb/s data rate **per chip**
- **Two Chips total**
  - 2Gb total
  - 3.2GB/s (25.6Gb/s) Uni-directional or 1.6GB/s (12.8Gb/s) bi-directional
- Separate DDR Controllers (One per chip)