

2 A Top-Level View of Computer Function and Interconnection

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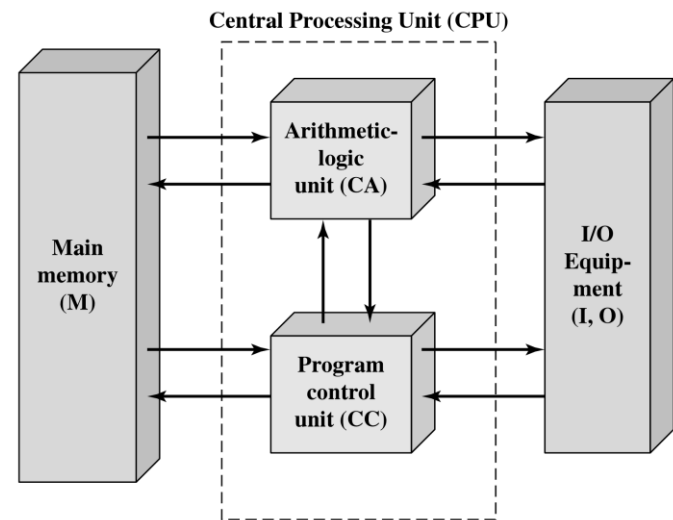
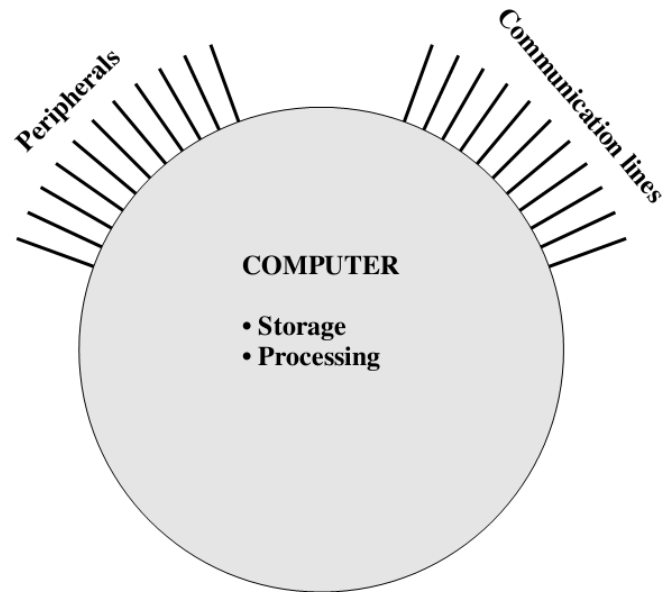
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Review

- Concepts
 - Computer, architecture, organization
- The von Neumann machine
 - Idea: main memory storing programs and data
 - Components: central arithmetical, central control, memory, input / output
- Moore's law and its consequence
- Computer performance
 - System clock, CPI, MIPS, MFLOPS, benchmarks

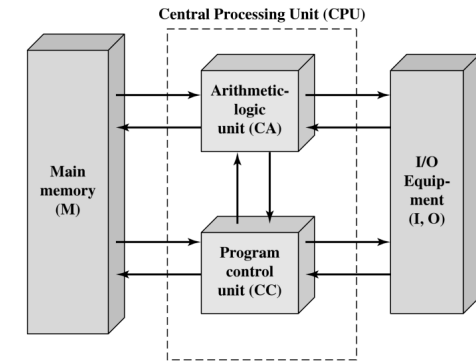


Computer

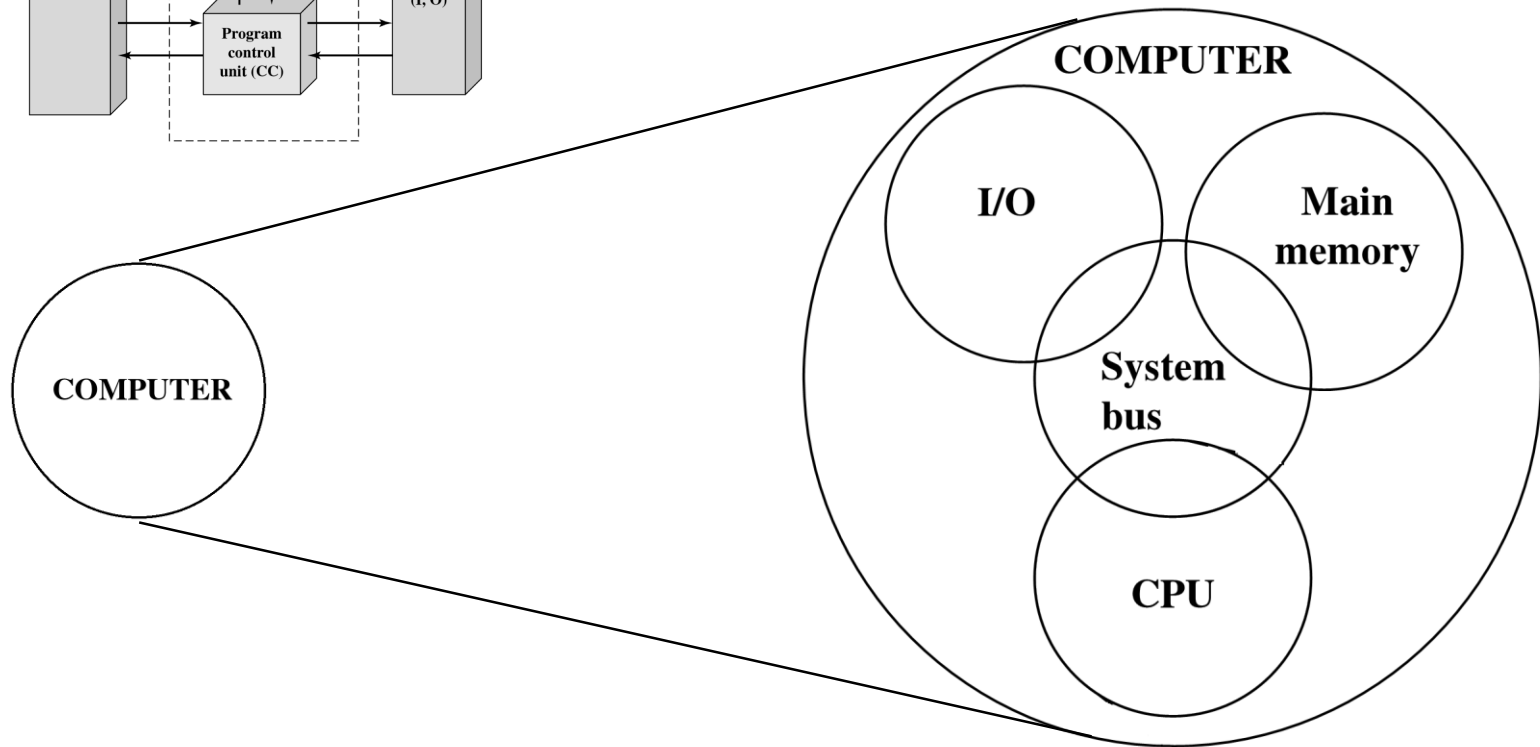


the von Neumann machine

A Top-Level Overview

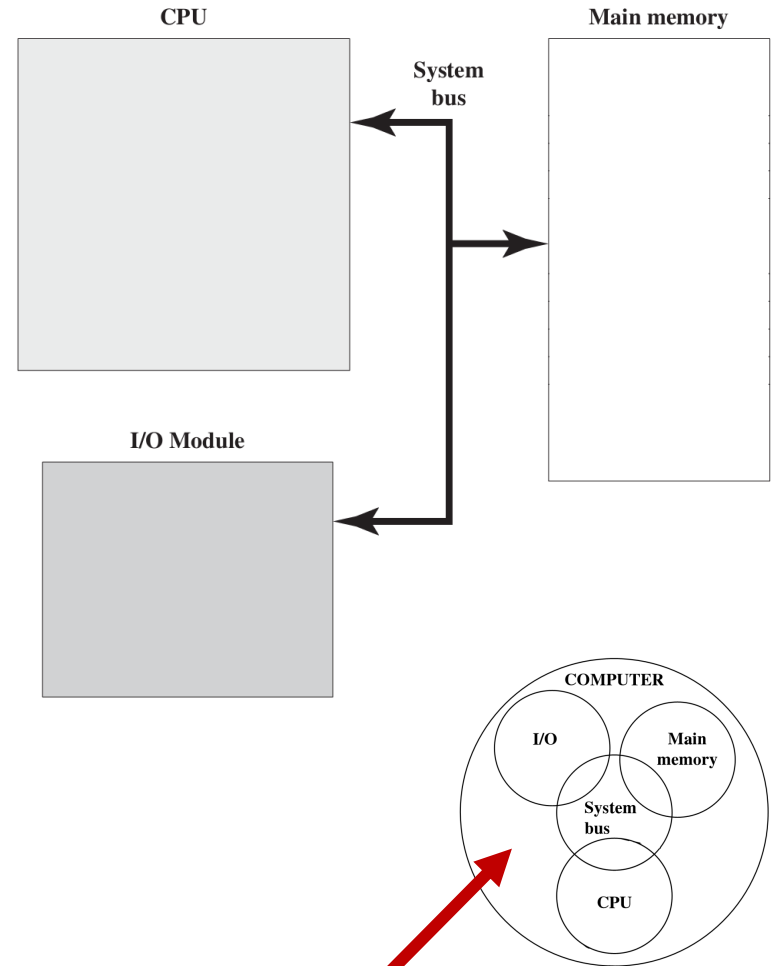


the von Neumann machine



Computer Components

- Data and instructions are stored in a single read-write memory
- The contents of this memory are addressable by location, without regard to the type of data contained there
- Execution occurs in a sequential fashion (unless explicitly modified) from one instruction to the next

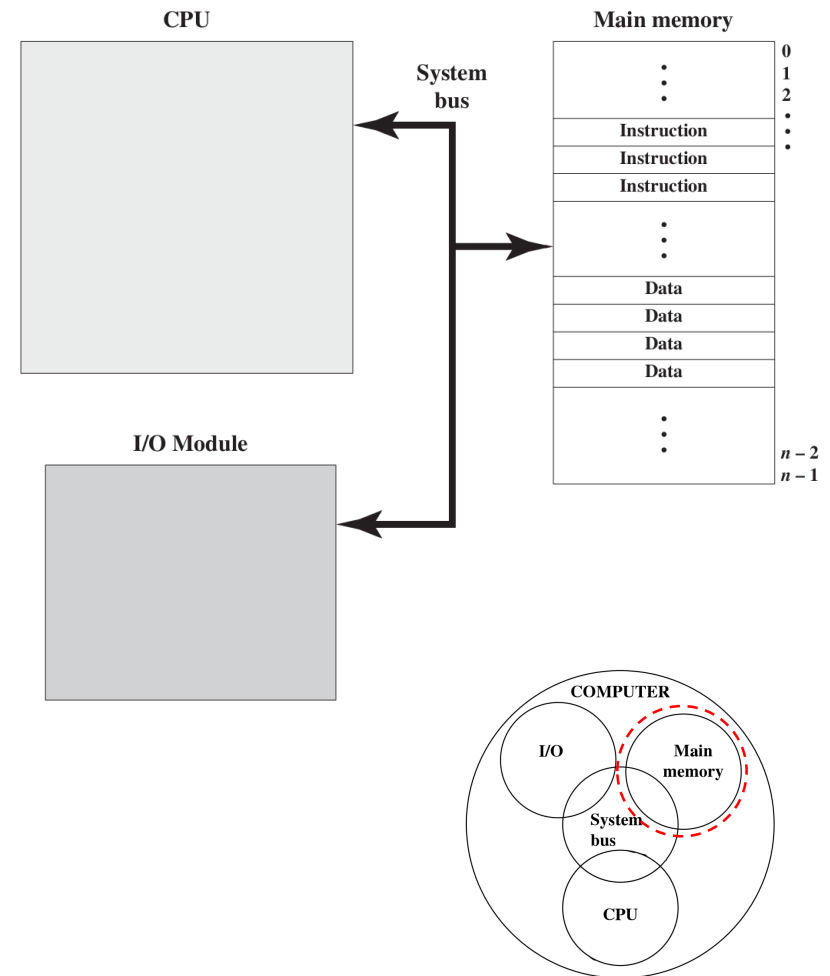


Incommensurate Scaling



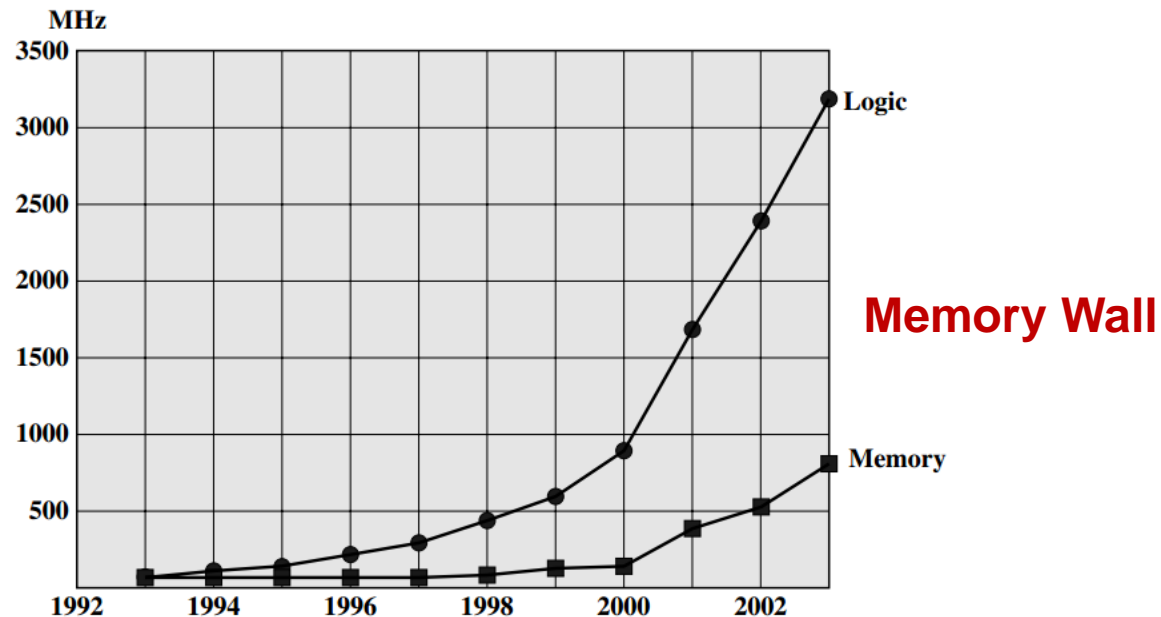
Computer Components: Memory

- Data and instructions are stored in a single read-write memory
- The contents of this memory are addressable by location, without regard to the type of data contained there



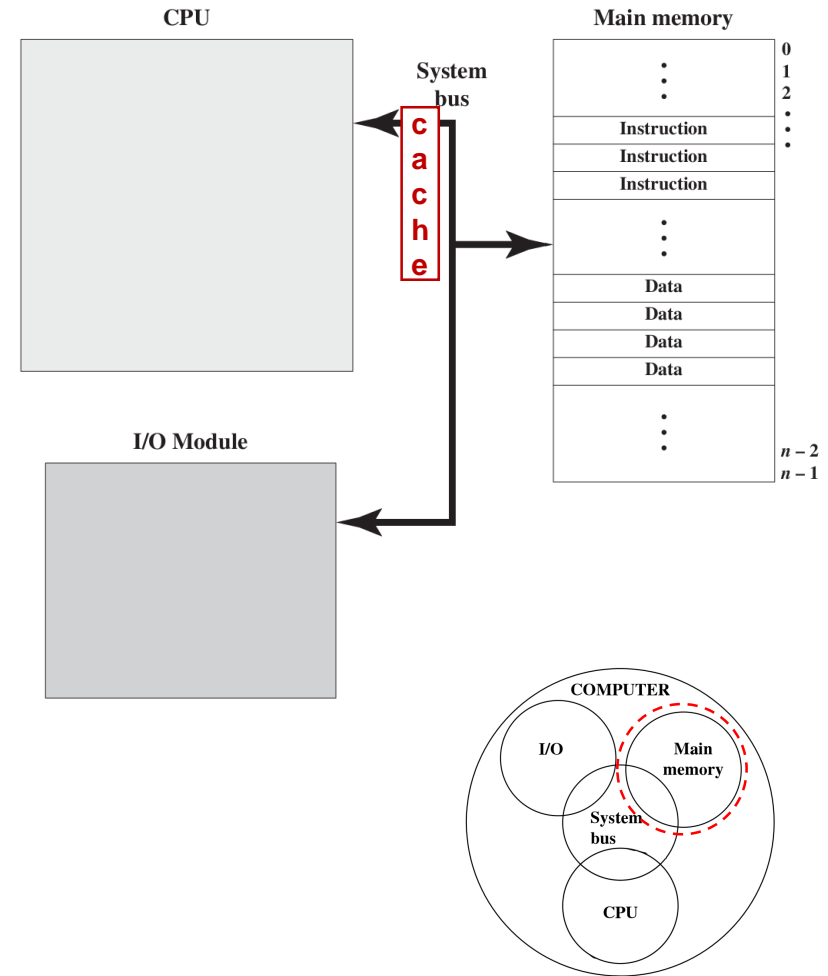
Computer Components: Memory (cont.)

- Problem
 - The speed of transferring data between main memory and CPU fails to keep up with the speed of CPU



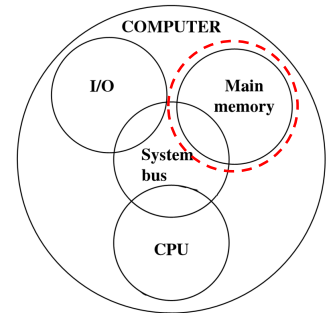
Computer Components: Memory (cont.)

- Solution
 - Add a cache or other buffering scheme to reduce the frequency of memory access and increase data transfer rate
 - Increase the number of bits retrieved one-time
 - ...



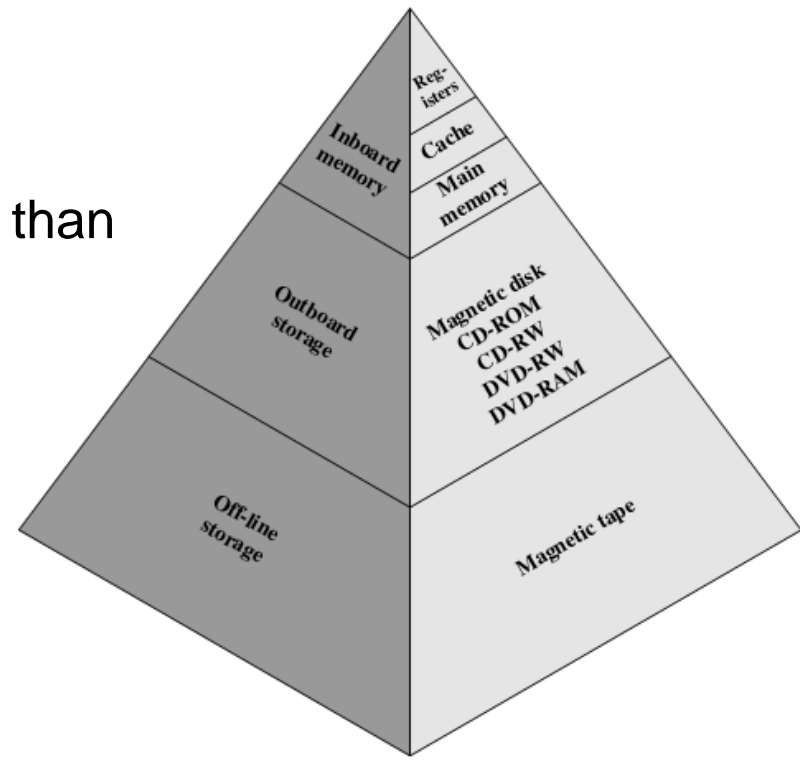
Computer Components: Memory (cont.)

- Constraints
 - Capacity: larger is better
 - Speed: keep up with the processor
 - Cost: reasonable to other components
- Relationship between constraints
 - Shorter access time, greater cost per bit



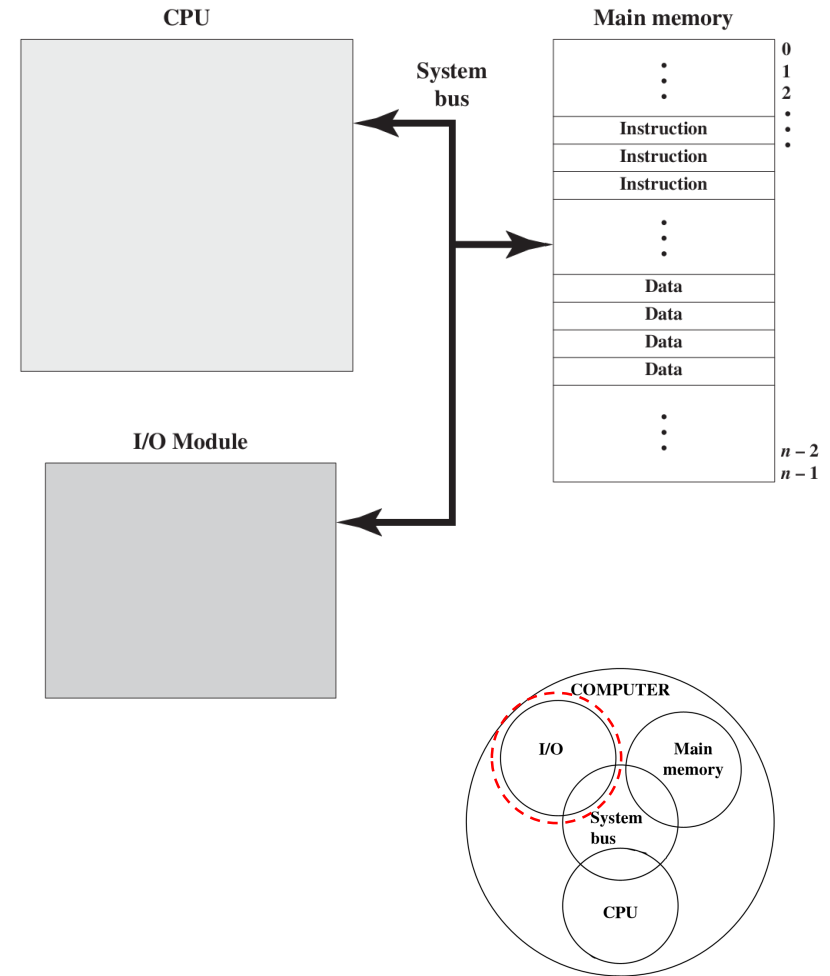
Computer Components: Memory (cont.)

- Requirement
 - Large capacity for data storage
 - High speed for performance
- Solution
 - Employ a memory hierarchy than rely on a single memory component



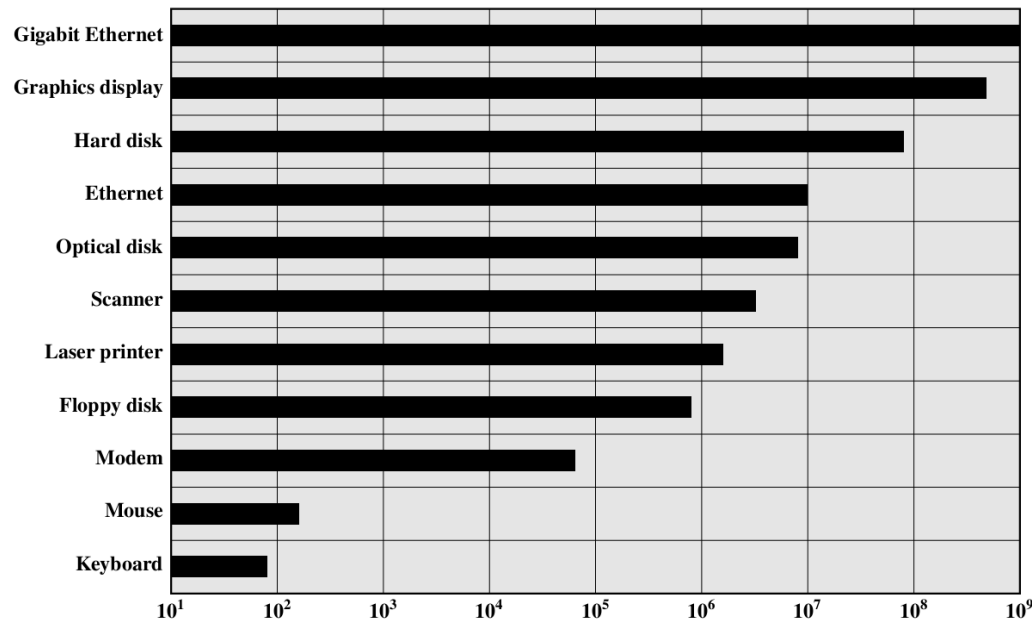
Computer Components: I/O

- Exchange data gathered from external sources with CPU and memory



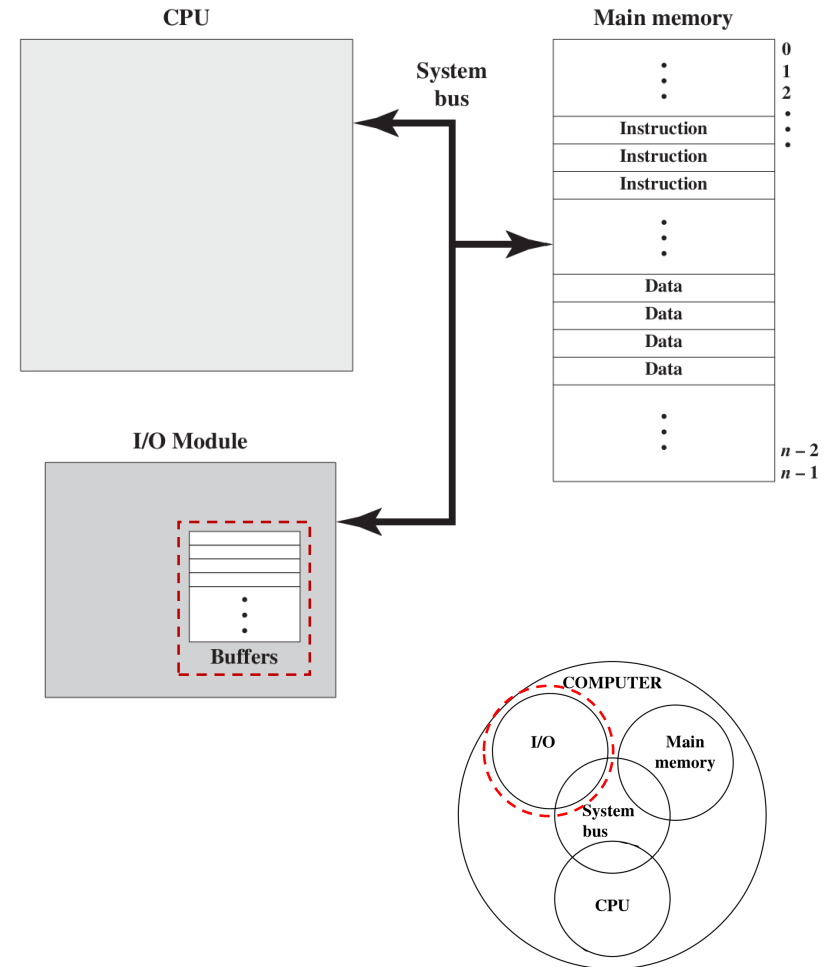
Computer Components: I/O (cont.)

- Problem
 - I/O performance cannot keep up with the increase of CPU speed



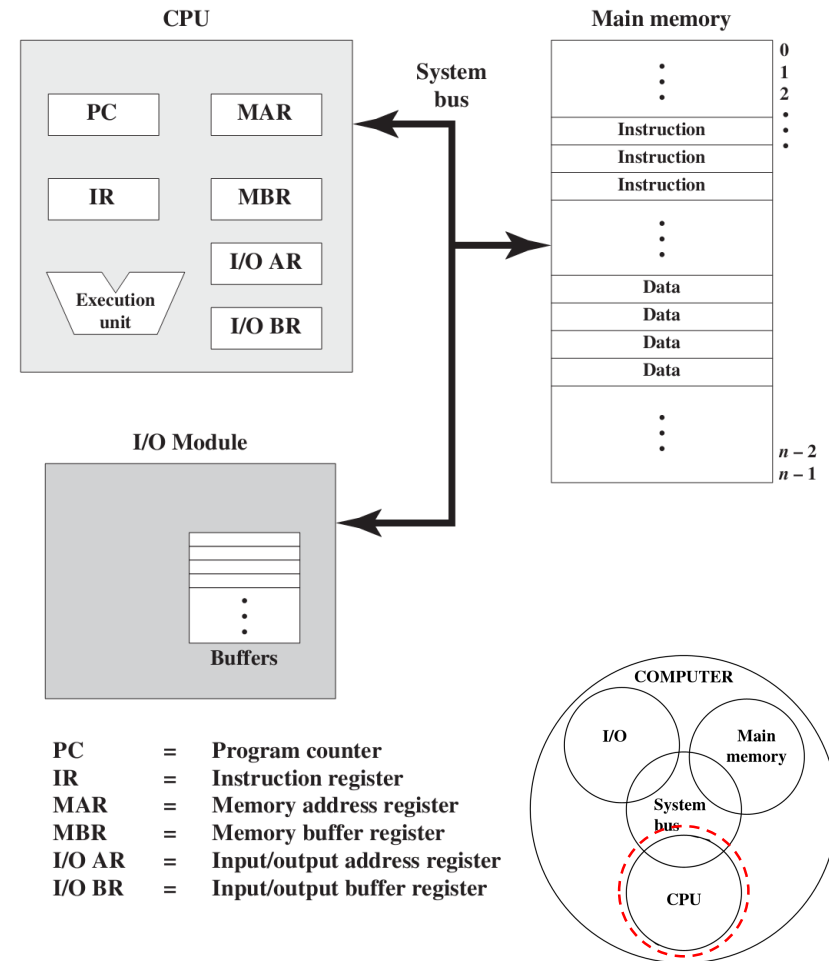
Computer Components: I/O (cont.)

- Solution
 - Buffering
 - New interface techniques
 - ...



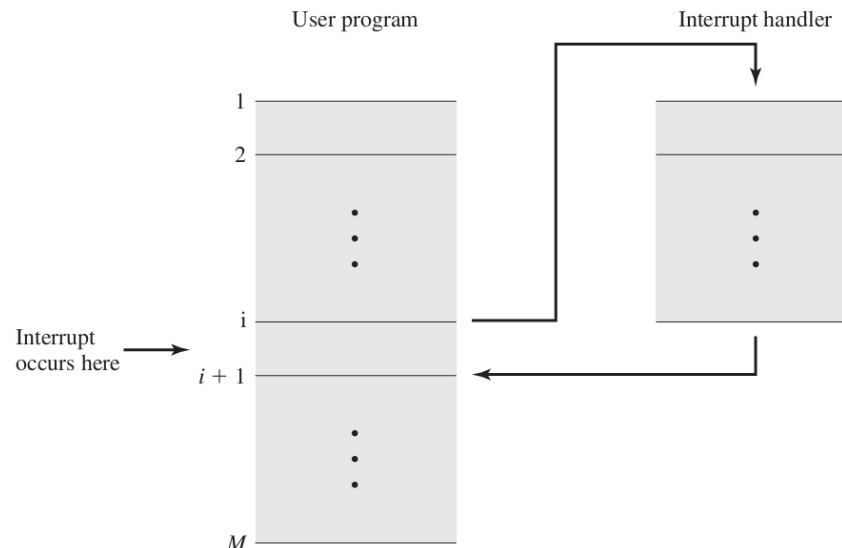
Computer Components: CPU

- Execution occurs in a sequential fashion (unless explicitly modified) from one instruction to the next
- Data and instructions are stored in a single read-write memory
- The contents of this memory are addressable by location, without regard to the type of data contained there



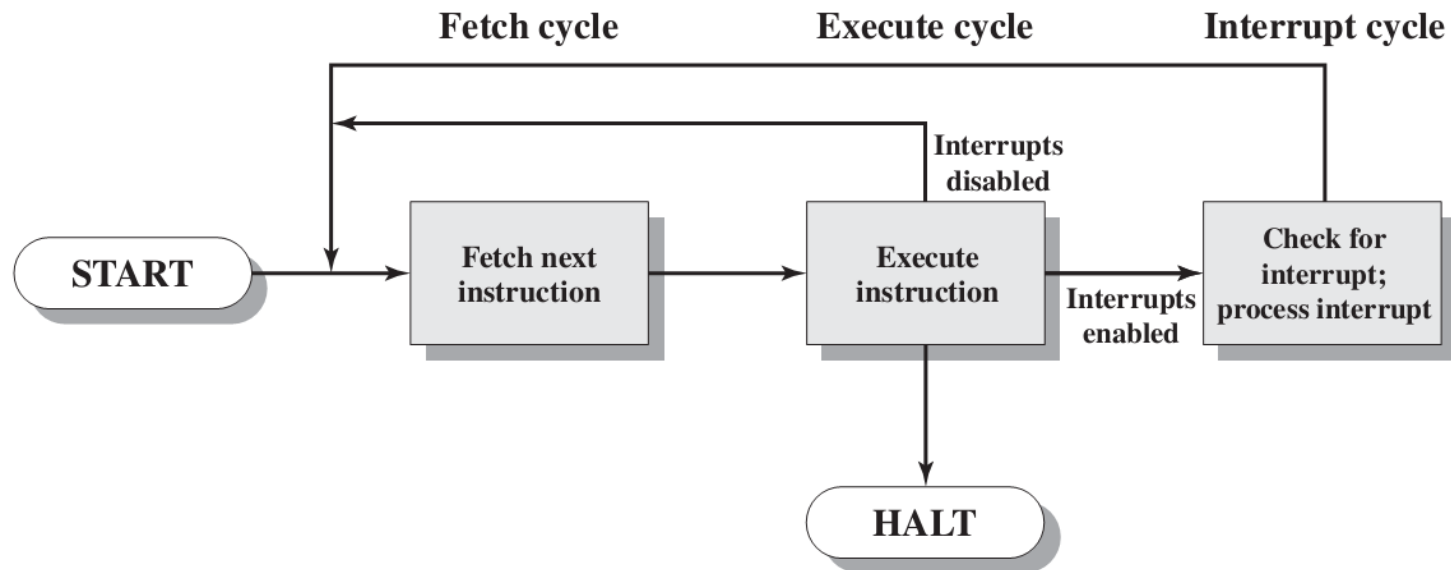
Computer Components: CPU (cont.)

- Problem
 - CPU remains idle when waiting for I/O devices
- Solution
 - Interrupt: a mechanism by which other modules (e.g. I/O) may interrupt normal sequence of processing



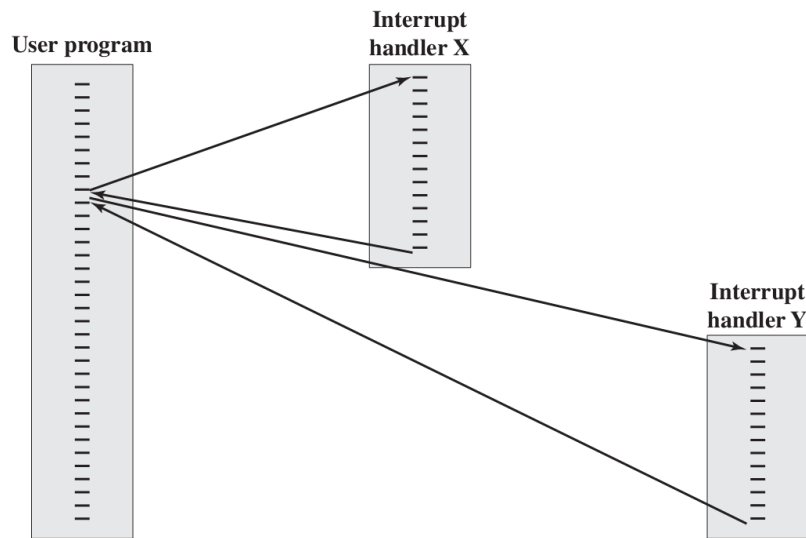
Computer Components: CPU (cont.)

- Interrupt detection
 - Add interrupt cycle into instruction cycle

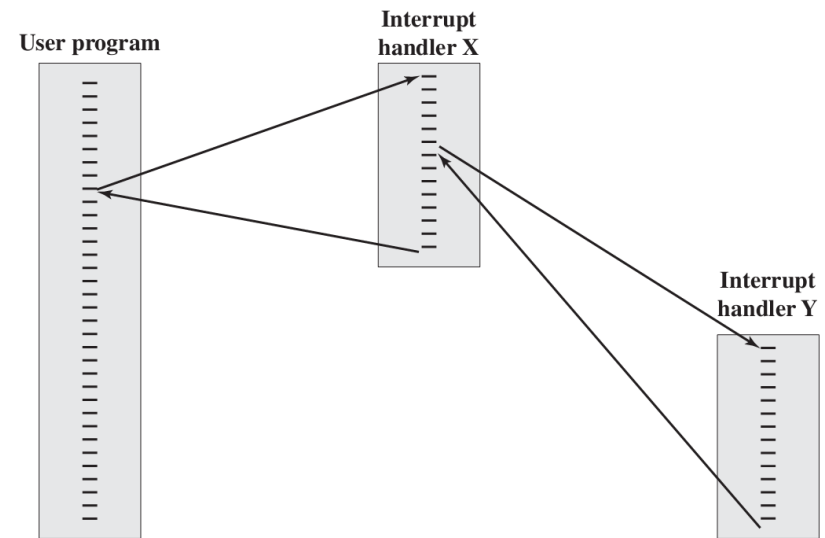


Computer Components: CPU (cont.)

- Multiple interrupts

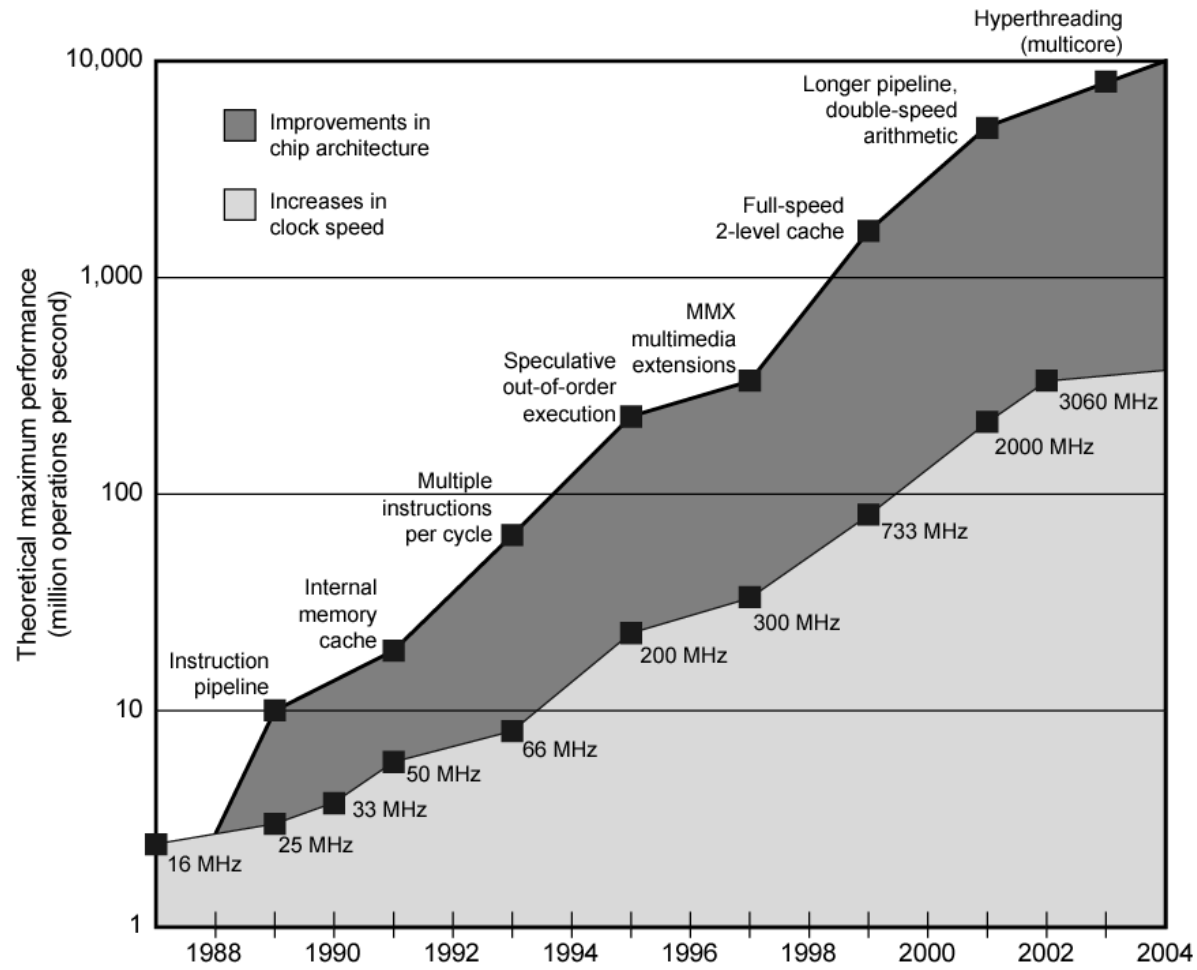


Sequential interrupt processing



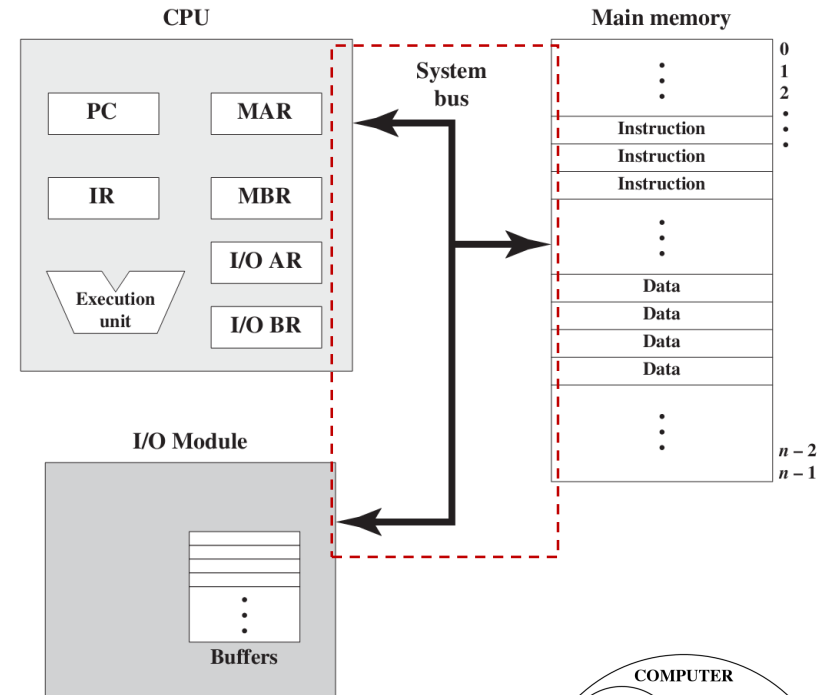
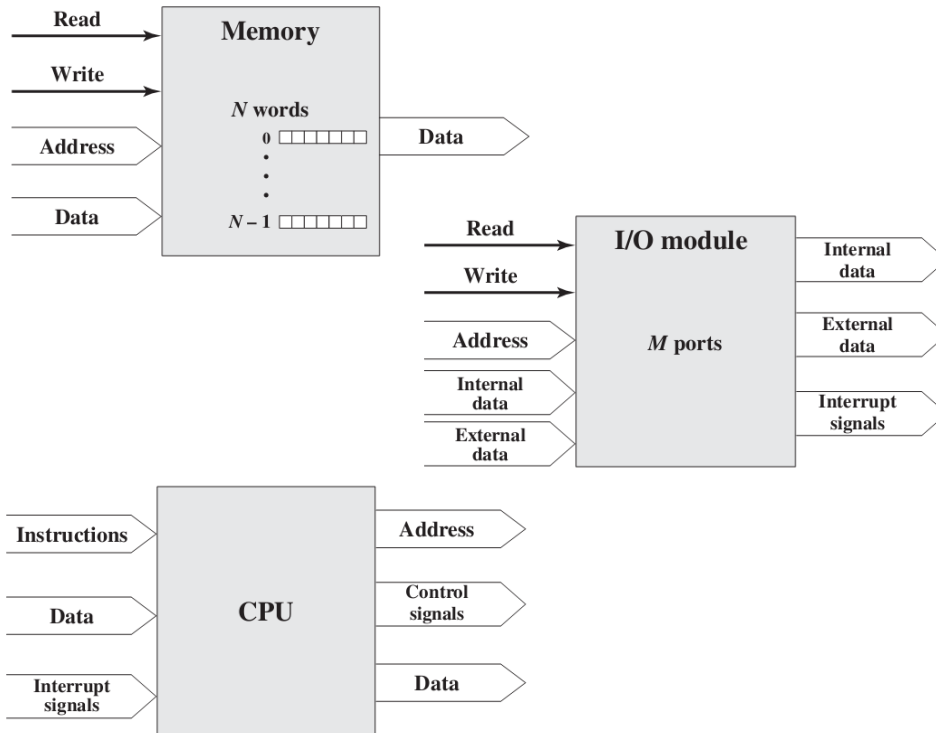
Nested interrupt processing

Computer Components: CPU (cont.)

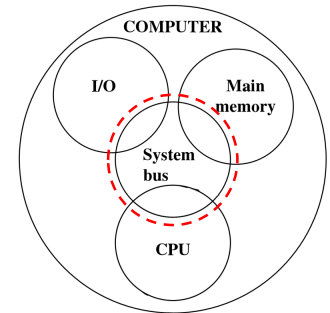


Computer Components: Bus

- Bus is a communication pathway connecting two or more devices

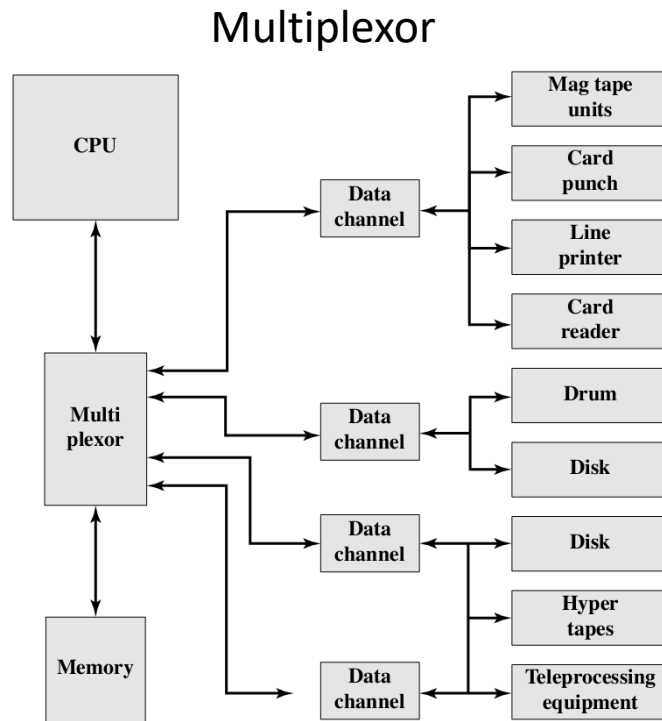


PC = Program counter
 IR = Instruction register
 MAR = Memory address register
 MBR = Memory buffer register
 I/O AR = Input/output address register
 I/O BR = Input/output buffer register



Computer Components: Bus (cont.)

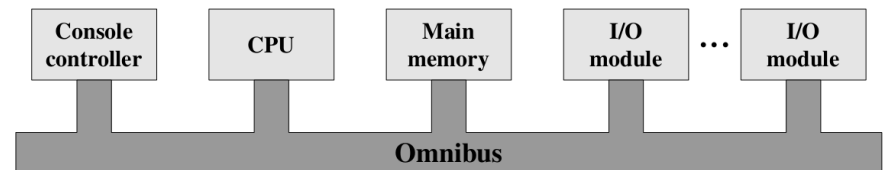
- Interconnection solution



IBM 7094

Bus

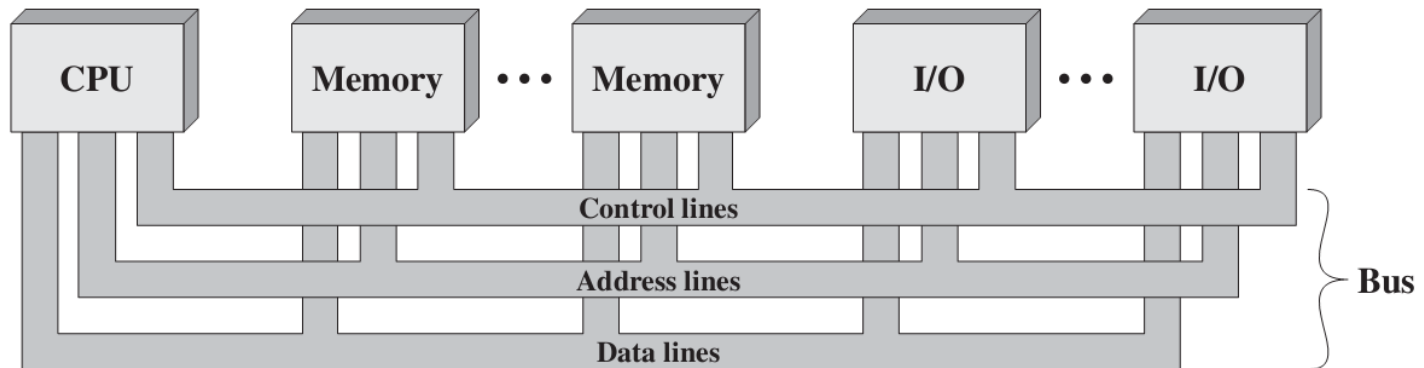
**a shared transmission medium
simplify the interconnection layout and
the control of processor**



PDP-8

Computer Components: Bus (cont.)

- Data transfer type
 - Any bus lines can be classified into three functional groups
 - Data lines: move data between system modules
 - Address lines: designate the source or destination of the data on the data bus and address I/O ports
 - Control lines: control the access to and the use of the data and address lines



Summary

- A top-level view of computer
- Computer component
 - Memory: cache, memory hierarchy
 - I/O: buffer
 - CPU: interrupt
 - Bus: type



Thank You

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