Computer Organization and Architecture

7 Internal Memory

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Review

- Floating-point arithmetic operations
  - Addition
  - Subtraction
  - Multiplication
  - Division
- Precision Consideration

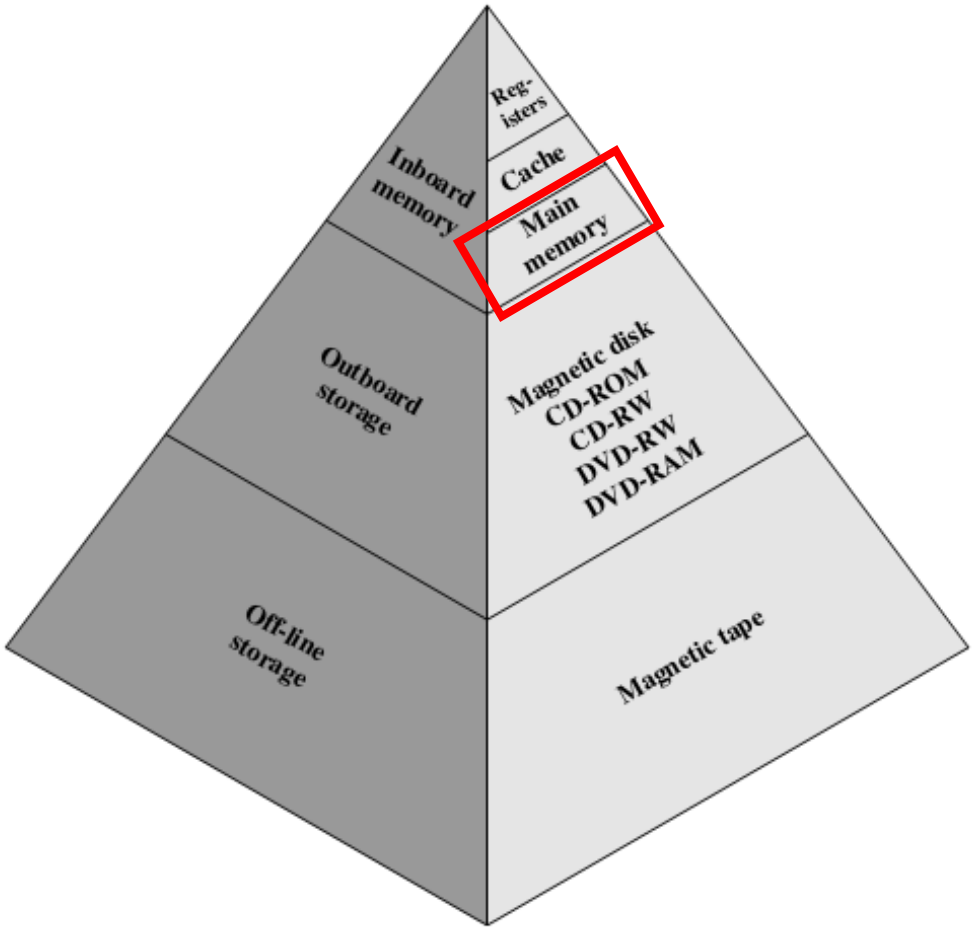
Review: Memory

Review: Memory

存储器由一定数量的单元构成，每个单元可以被唯一标识，每个单元都有存储一个数值的能力

- 地址：单元的唯一标识符（采用二进制）
- 地址空间：可唯一标识的单元总数
- 寻址能力：存储在每个单元中的信息的位数
  - 大多数存储器是字节寻址的，而执行科学计算的计算机通常是64位寻址的

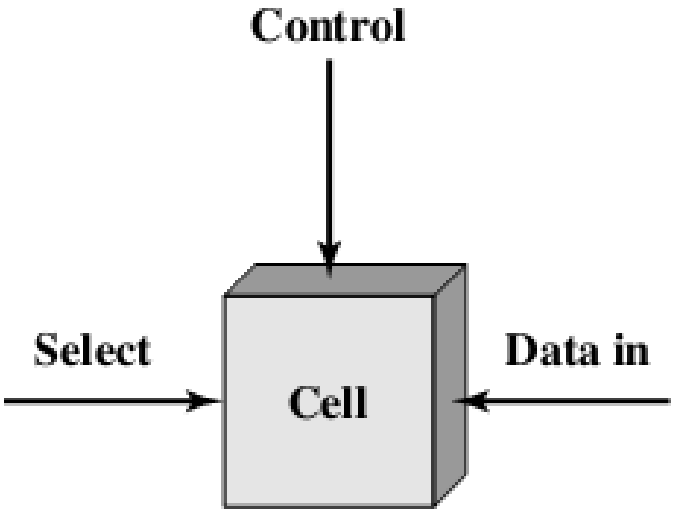
Memory Hierarchy



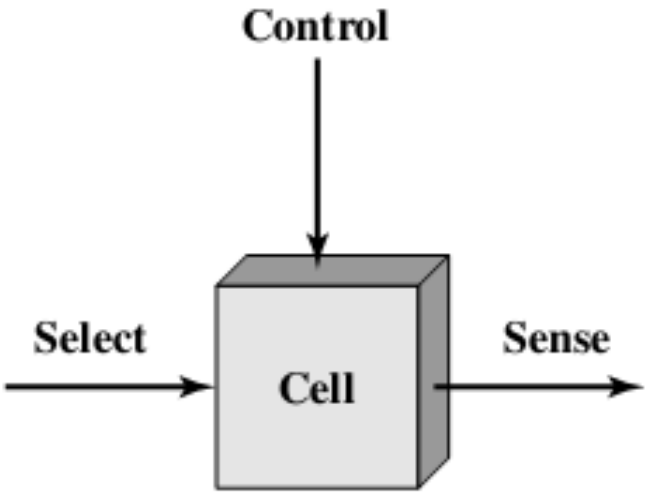
Semiconductor Main Memory

- The use of semiconductor chips for main memory is almost universal
- **Memory cell**: basic element of semiconductor memory
- Properties
  - They exhibit two stable (or semi-stable) states, which can be used to represent binaries 1 and 0
  - They are capable of being written into (at least once), to set the state
  - They are capable of being read to sense the state

Memory Cell Operation



Write



Read

Semiconductor Memory Types

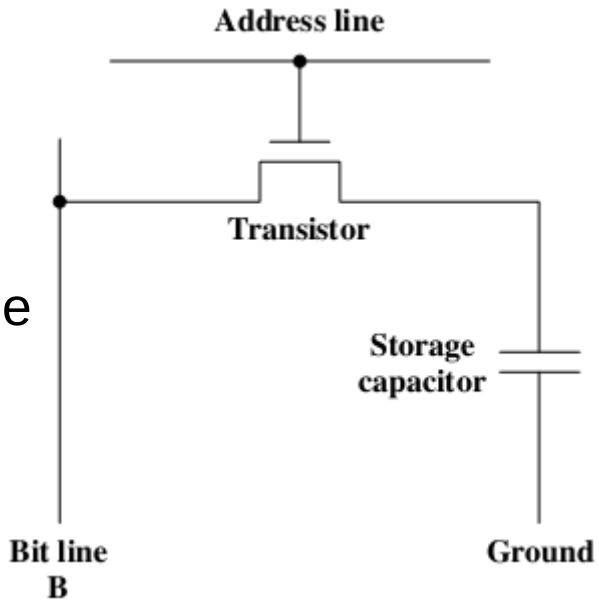
Memory Type	Category	Erasure	Write Mechanism	Volatility
Random-access memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile
Read-only memory (ROM)	Read-only memory	Not possible	Masks	Nonvolatile
Programmable ROM (PROM)			Electrically	
Erasable PROM (EPROM)	Read-mostly memory	UV light, chip-level		
Electrically Erasable PROM (EEPROM)		Electrically, byte-level		
Flash memory		Electrically, block-level		

RAM

- Random-Access Memory
- Characteristics
  - Reading/writing can be easy and rapid
  - Volatile
- Types
  - DRAM: Dynamic RAM
  - SRAM: Static RAM

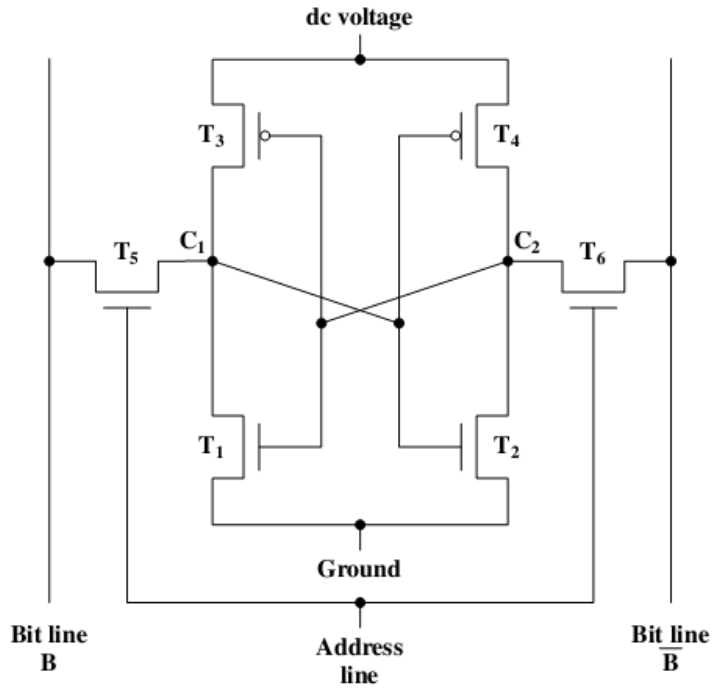
DRAM

- Store data as charge on capacitors
  - The presence or absence of charge in a capacitor is interpreted as a binary 1 or 0
- Require periodic charge refreshing to maintain data storage
  - Reason: capacitors have a natural tendency to discharge
  - A threshold value determines whether the charge is interpreted as 1 or 0
    - It is essentially an analog device



SRAM

- Store data with traditional flip-flop logic-gate configurations
  - The same logic elements used in the processor
- Hold its data as long as power is supplied to it



Comparison between DRAM and SRAM

- Similarity
  - Volatile, i.e. power must be continuously supplied to the memory to preserve the bit values
- Differences
  - DRAM has simpler and smaller cells than SRAM, but requires the supporting refresh circuitry
    - A DRAM is more dense and less expensive than a corresponding SRAM
    - DRAMs tend to be favored for large memory requirements
  - SRAM is generally faster than DRAM
  - SRAM is used for cache and DRAM is used for main memory

Advanced DRAM Organization

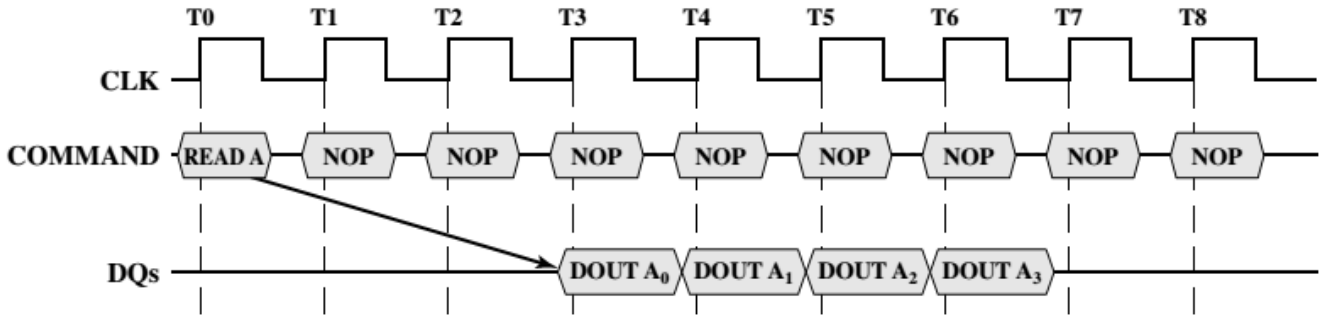
- Problem
  - The traditional DRAM chip is constrained both by its internal architecture and by its interface to the processor's memory bus
- Types
  - Synchronous DRAM (SDRAM)
  - DDR SDRAM (DDR)

Synchronous DRAM

- Traditional DRAM is asynchronous
  - The processor presents addresses and control levels to the memory, indicating that a set of data at a particular location in memory should be either read from or written into the DRAM
  - The DRAM performs various internal functions, such as activating the high capacitance of the row and column lines, sensing the data, and routing the data out through the output buffers, and the processor must simply wait through this delay
  - After a delay, the DRAM either writes or reads the data

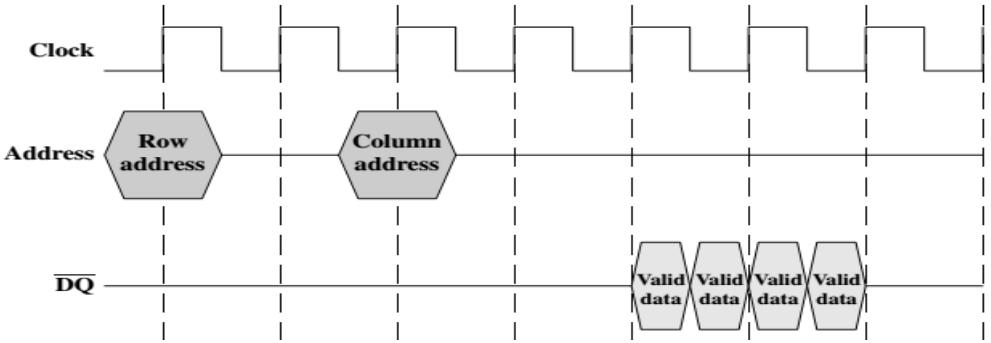
Synchronous DRAM (cont.)

- SDRAM exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states
- Since SDRAM moves data in time with system clock, CPU knows when data will be ready



DDR SDRAM

- Double-data-rate SDRAM
- Send data twice per clock cycle, once on the rising edge of the clock pulse and once on the falling edge
- Comparison of DDR, DDR2 and DDR3
  - Increase operational frequency
  - Increase the prefetch buffer



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ROM

- Read-only memory
- Characteristics
  - Nonvolatile: no power source is required to maintain the bit
  - Possible to read a ROM but not possible to write new data
- Applications
  - Microprogramming, library subroutines, system programs, function tables
- Problems
  - Data insertion incurs a relatively large fixed cost
  - No room for error: If one bit is wrong, the whole batch of ROMs must be thrown out

PROM

- Programmable ROM
- Characteristics
  - Nonvolatile
  - Can be written only once
    - Electrically
    - Special equipment is required for writing
- Compared to ROM
  - PROMs provide flexibility and convenience
  - The ROM remains attractive for high-volume production runs

[周文卿, 121250226]

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Read-Mostly Memory

- Characteristics
  - Read operations are far more frequent than write operations
  - Nonvolatile storage
- Types
  - EPROM
  - EEPROM
  - Flash memory

EPROM

- Erasable programmable read-only memory
- Characteristics
  - Read and written electrically
  - Erasure: exposure of the packaged chip to ultraviolet radiation before a write operation
    - All the storage cells will be the same initial state
    - Take as much as 20 minutes
- Compared to PROM
  - EPROM is more expensive, but it can be updated multiple times

EEPROM

- Electrically erasable programmable read-only memory
- Characteristics
  - Can be written into at any time without erasing prior contents
  - Update the byte or bytes addressed only
  - Write operation takes several hundred microseconds per byte
- Compared to EPROM
  - EEPROM is more expensive than EPROM and also is less dense

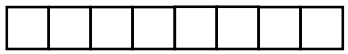
Flash Memory

- Characteristics
  - Electrically erasing
  - Erased in up to a few seconds, much faster than EPROM
  - Possible to erase on block-level but not byte-level
  - Achieve as high density as EPROM (compared with EEPROM)
- Compared to EPROM and EEPROM
  - Intermediate between EPROM and EEPROM in both cost and functionality

From Cell to Main Memory

- Addressable unit
  - Composed of the cells with the same address
  - Addressing mode
    - Byte (common)
    - Word

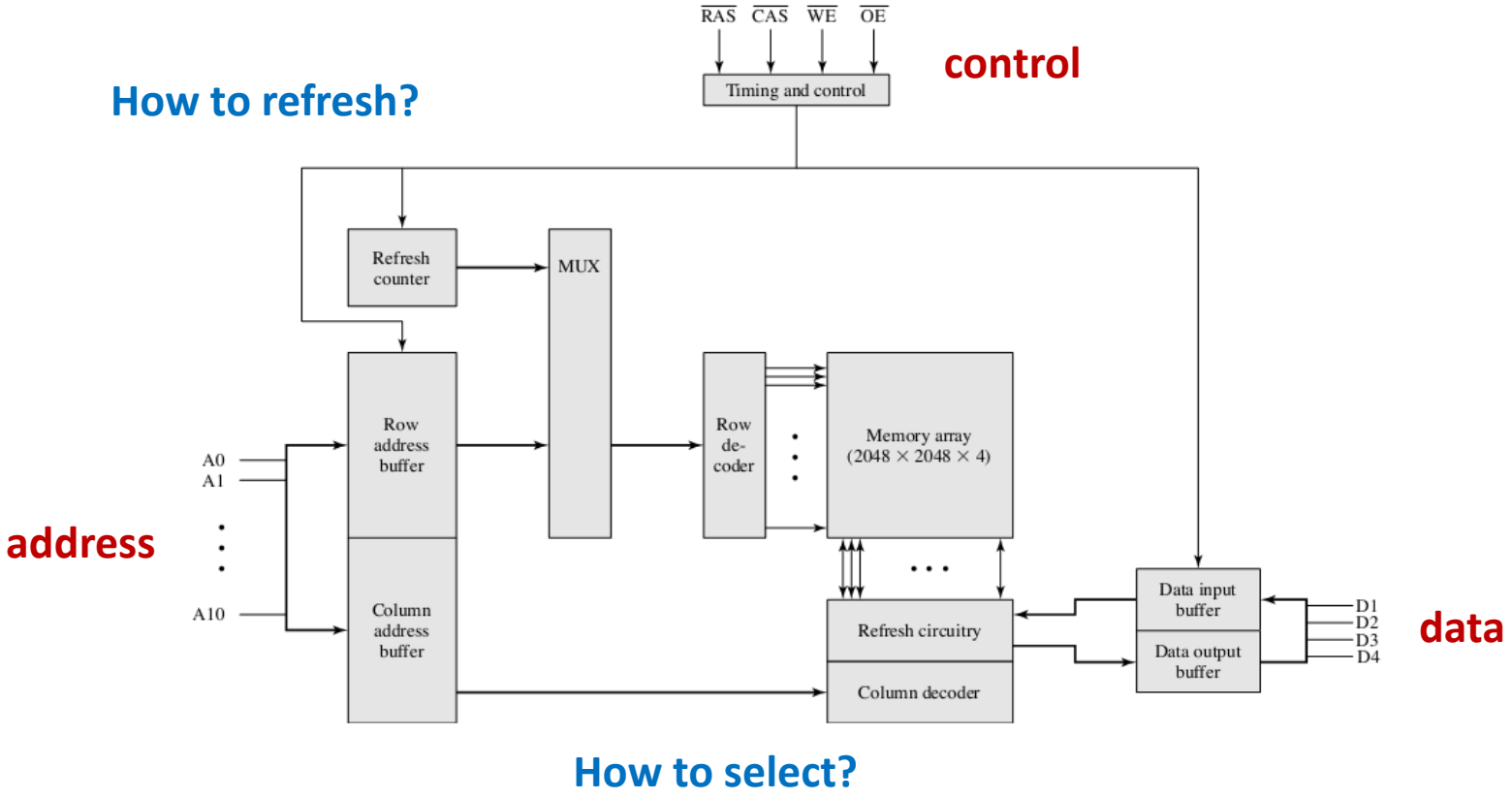
cell



addressing unit

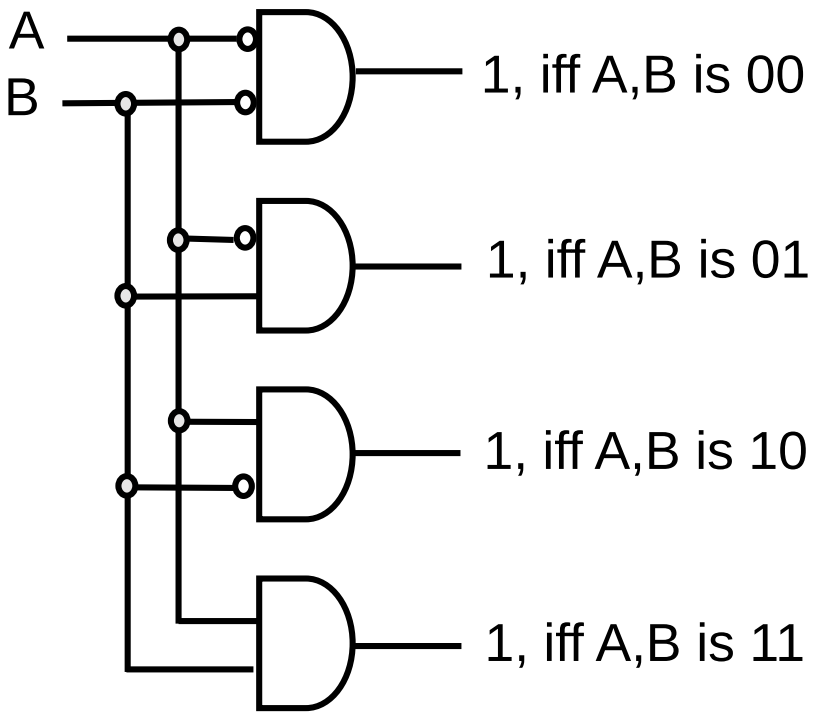
From Cell to Main Memory (cont.)

- Memory array
  - Composed of many addressing units



Address Decoder

- An n input decoder has 2^n outputs.
- Output$_i$ is 1 iff the binary value of the n-bit input is i
- At any time, exactly one output is 1, all others are 0



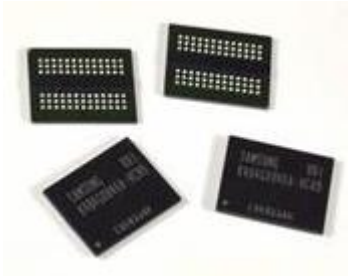
2-bit decoder

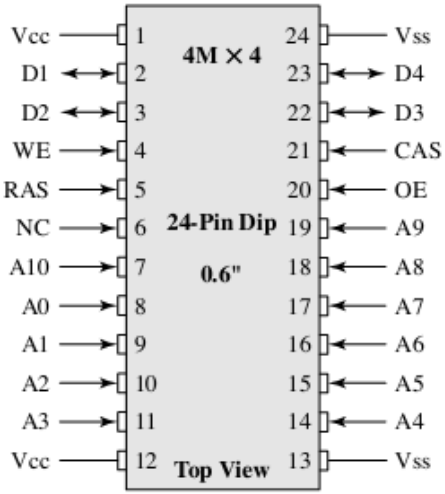
Refreshing

- Centralized refresh
  - Stop read/write operation, and refresh each line
  - The memory cannot be operated when refreshing
- Decentralized refresh
  - Refresh in each storage cycle when the read/write operation is finished
  - Increase the time of each storage cycle
- Asynchronous refresh
  - Refresh each line in 64ms
  - High efficiency (common)

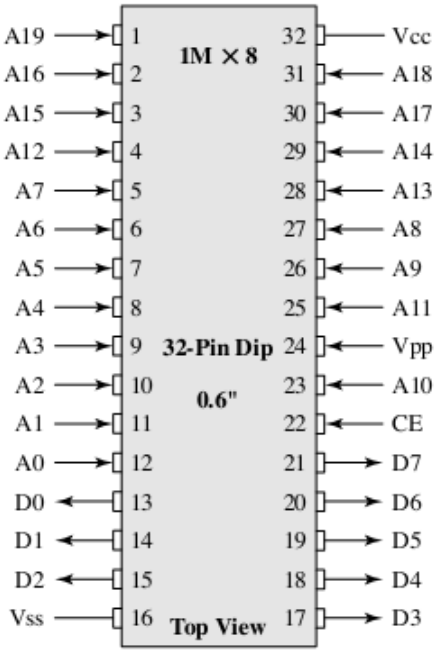
From Cell to Main Memory (cont.)

- Chip
  - Address: A0 – A19
  - Data: D0 – D7
  - Vcc: power supply
  - Vss: ground pin
  - CE: chip enable
  - Vpp: program voltage
  - WE: write enable
  - OE: output enable
  - RAS: row address select
  - CAS: column address select





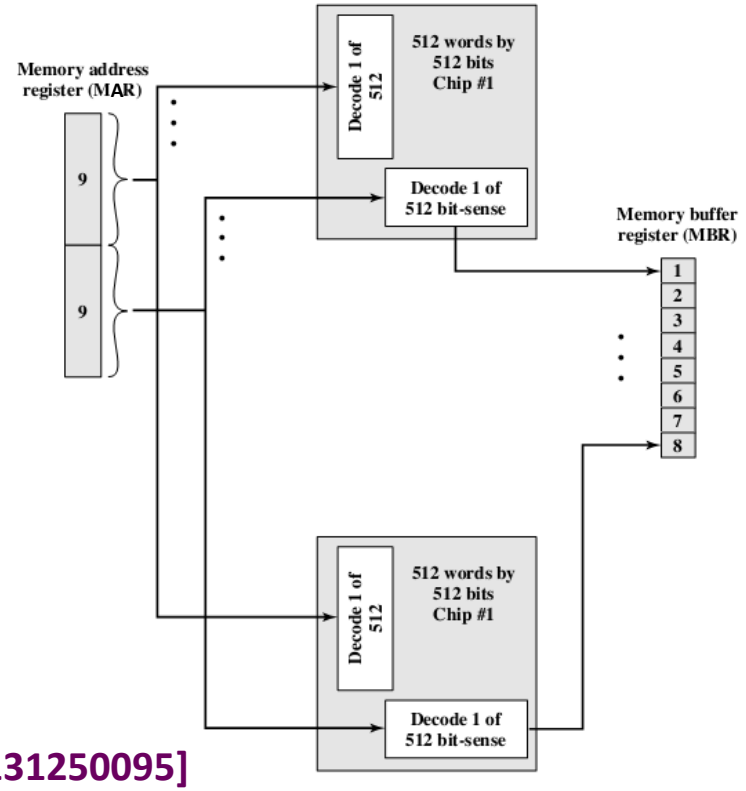
16-Mbit DRAM



8-Mbit EPROM

From Cell to Main Memory (cont.)

- Module organization
  - Number of bits extended
    - Address line: no change
    - Data line: increased
    - Use eight 4K*1 bit chips to organize 4K*8 bit memory



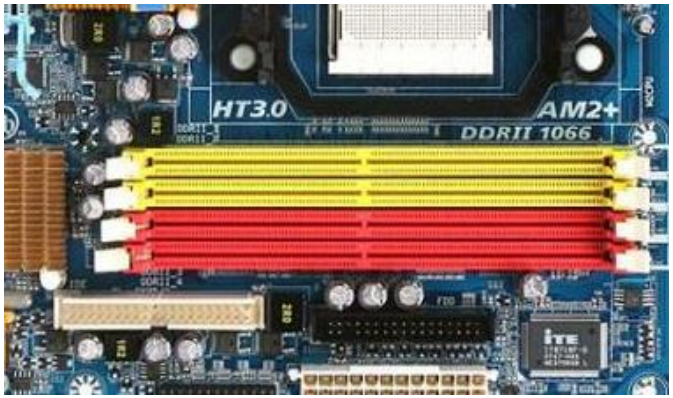
[丁峰, 131250095]

From Cell to Main Memory (cont.)

- Module organization (cont.)
  - Length of words extended
    - Address line: increased
    - Data line: no change
    - Use four 16K*8 bit chips to organize 64K*8 bit memory
  - Both extended
    - Address line: increased
    - Data line: increased
    - Use 8 16K*4 bit chips to organize 64K*8 bit memory

From Cell to Main Memory (cont.)

- Slots
  - Combine multiple memory modules



- Main Memory
  - Main memory = RAM + ROM
  - Main memory capacity = RAM capacity

Summary

- Semiconductor memory
  - RAM: DRAM, SRAM, SDRAM, DDR
  - ROM, PROM
  - EPROM, EEPROM, flash memory
- From cell to main memory
  - Addressable unit, memory array, chip, module, main memory

Thank You

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