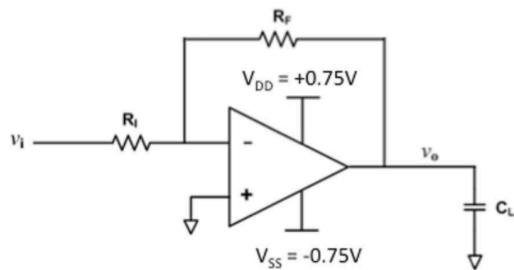


# Design of an Operational Amplifier from Matthew Choi in 18623 of Fall 24

Matthew Choi  
Carnegie Mellon University  
Pittsburg, PA  
mchoi3

## Abstract

The High Speed Operational Amplifier(OP AMP) design that was achieved had an open gain of 719.6, bandwidth of 205 MHz, Input Offset of 161.5u, Output swing of 0.5431V and -0.602V on each end, slew rate of 239.8M and -138.7M on each end, phase margin of 72.61 and power of 461.3uW. Bias current used was -110uA, and the testbench utilized transient amplitude of 600mV. Monte Carlo Analysis yield was 64.6 percent, and the total area of the design was 271.3012 um<sup>2</sup>.



## I. INTRODUCTION

The Operational amplifier(OP AMP) is an analog circuit block that initially takes in a differential voltage input, and returns a single-ended voltage output. Its main functions involve signal amplification and amplifying voltage difference

The initial design of the OP AMP was set as a two stage Operational Amplifier, with the first stage receiving the inputs with a differential pair, and the second stage raising the output swing and gain.

When it comes to the design procedure, I started by setting the  $C_c$  capacitor to a reasonable value less than  $C_L$ , and multiplied it with the minimum slew rate to get an estimate

of current through the differential pair. Using that current value, I then calculated the  $G_m/I_D$  values of the differential pairs and then calculated the W/L ratios for them as well. After setting the W/L of the pairs, I then calculated the  $G_m/I_D$ , current, and W/L of the N-MOS right below the differential pair, and the current mirror paired to it. Furthermore, to match the drain voltage of the differential PMOS pair, I calculated the W/L of the PMOS and NMOS on the second stage of the OP AMP, while making sure that the open gain voltage would exceed the specs required

## II. NOMINAL SPECIFICATIONS AND CONSTRAINTS

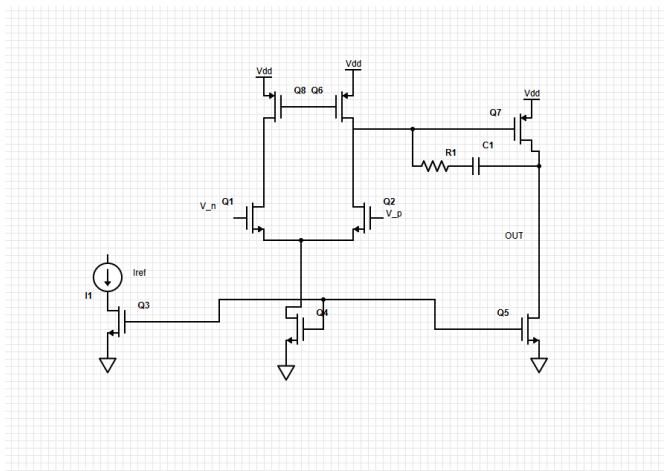
Name of the spec.	Spec. corresponding to your design	Performance from your design @ 27°C
Open Gain V/V	> 600	719.6
BW (MHz)	> 120MHz	205M
Input Offset(mV)	< 1 mV, >-1 mV	161.5u
Output Swing(positive)	> 0.5V	0.5431
Output Swing(negative)	< -0.5V	-0.6032
Slew Rate(positive)	> 100V/us	239.8M
Slew Rate(negative)	> -100 V/us	-138.7M

Phase Margin	> 70 degrees	72.61
Power(uW)	<600uW	461.3u

Design constraints:

- One ideal current source in testbench from ground to bias pin in test bench
- No ideal elements in the design
- Body Effect on N-MOSFETs not sourced to ground
- 5 nm multiples for transistor sizes
- no DC value in biasing
- All substrate terminal should be connected to ground, all PFET substrate can be connected to source
- vdd value set to 0.75V, vss value set to -0.75V
- Bias gates so that no gate oxide has more than 1V across them

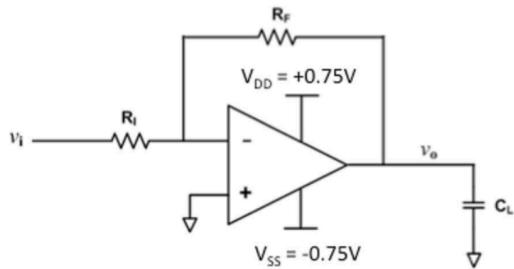
### III. CHOICE OF TOPOLOGY AND JUSTIFICATION/HAND ANALYSIS



The operational amplifier is composed of 2 stages, being the input stage and the gain boosting stage given the two-stage op-amp that I decided to use. I decided to use a two-stage op-amp set up because I realized that other setups such as a folded cascode would sacrifice too much gain in contrast to the two-stage op-amp setup. Furthermore, initial testing with the two-stage op-amp given in the lecture notes made me realize it would be far more of a hassle to deal with the lower output swing than the lower gain of the two stage op amp. Furthermore, based on the hand calculations on Lecture 12, and the lower capacitance value of  $C_L$  on the testbench, I had to calculate the minimum current given minimum slew rate with  $I_t = (C_C/C_C+C_L)*$  slew rate. Afterwards, I calculated  $Gm/Id$  of all of the mosfets using the  $Gm/Id$  standards, accounting for saturation in all MOSFETs while also ensuring that mosfets would consistently be in the same region. I set high W/Ls for the differential pair, and accordingly set W/L based on the  $I_t$  current through the MOSFETs. All MOSFET lengths were set to 0.5  $\mu m$  to ensure uniformity. Once I used the lecture 12 slides to get inspiration for the calculations, all

the MOSFET W/L values were modified to ensure all MOSFETs were actually in saturation(which involved drastically reducing the W/L of the differential pair so that they would actually be saturated). Afterwards,  $I_{ref}$  was increased to -110u to increase drain to source voltage of Q3 to ensure saturation. For input offset, I had to minimize the difference between drain voltage of the PMOSFETs above. For outswing and bandwidth, I had to tweak with the W/L values of Q5 and 7. Slew rate is directly proportional to the capacitor  $C_1$ , which I increased until it exceeded the required specs. For phase margin, I had to add a resistor to prevent it from reaching negative values, and tested the values until I met the specs required. When calculating for W/L for the mosfets, I utilized the equation  $I_D = k'/2 * (W/L) * (Vov)^2$ , given  $K' = C_{ox} * \square$ .

### IV. TESTBENCH



R <sub>L</sub> ohm	R <sub>F</sub> ohm	V <sub>DD</sub> (V)	V <sub>SS</sub> (V)	C <sub>L</sub> (pF)	Iref (uA)	Transient amplitude (mV)
10k	10k	0.75	-0.75	0.5	-110	600

### V. RESULTS

Here you will have to report the numeric values.

#### A. Performance at different temperature

Specs(Units)	-0.1(Vcm)	0(Vcm)	0.1(Vcm)
Open Gain V/V	747.7	719.6	678.5
BW (MHz)	181.1	205	210.6
Input Offset(uV)	509	161.5	7.827

Output Swing(positive)	0.5253V	0.5431	0.5196
Output Swing(negative)	-0.5615	-0.6032	-0.6188
Slew Rate(positive)	180M	239.8M	281.6M
Slew Rate(negative)	-138.3M	-138.7M	-139.8M
Phase Margin	74.82	72.61	72.16
Power	440.6uW	461.3uW	472.4uW

#### D. Power consumption calculation

Power	-0.1	0	0.1
Total(uW)	440.6uW	461.3uW	472.4uW

#### E. FoM calculation

-0.1V	0V	0.1V
4012.628844	4354.653168	4304.472031

#### B. MC yields at different Vcms

	TestBench	Results	Yield
-0.1 V			64.6%
0 V			73.4%
0.1 V			74.3%

#### C. Area Calculation

Component	Total Width (um)	Length (um)	Multiplier	Area(u m <sup>2</sup> )
M1	20	0.5	1	15.6
M2	20	0.5	1	15.6
M3	3	0.5	2	4.68
M4	3	0.5	2	4.68
M5	9	0.5	1	7.02
M6	4.7	0.5	1	3.666
M7	16	0.5	1	12.48
M8	4.7	0.5	1	3.666
C1	5	5	10	250
R1	1	5.75	2	11.5

Total area = 365.392 um<sup>2</sup>

#### VI. DISCUSSIONS

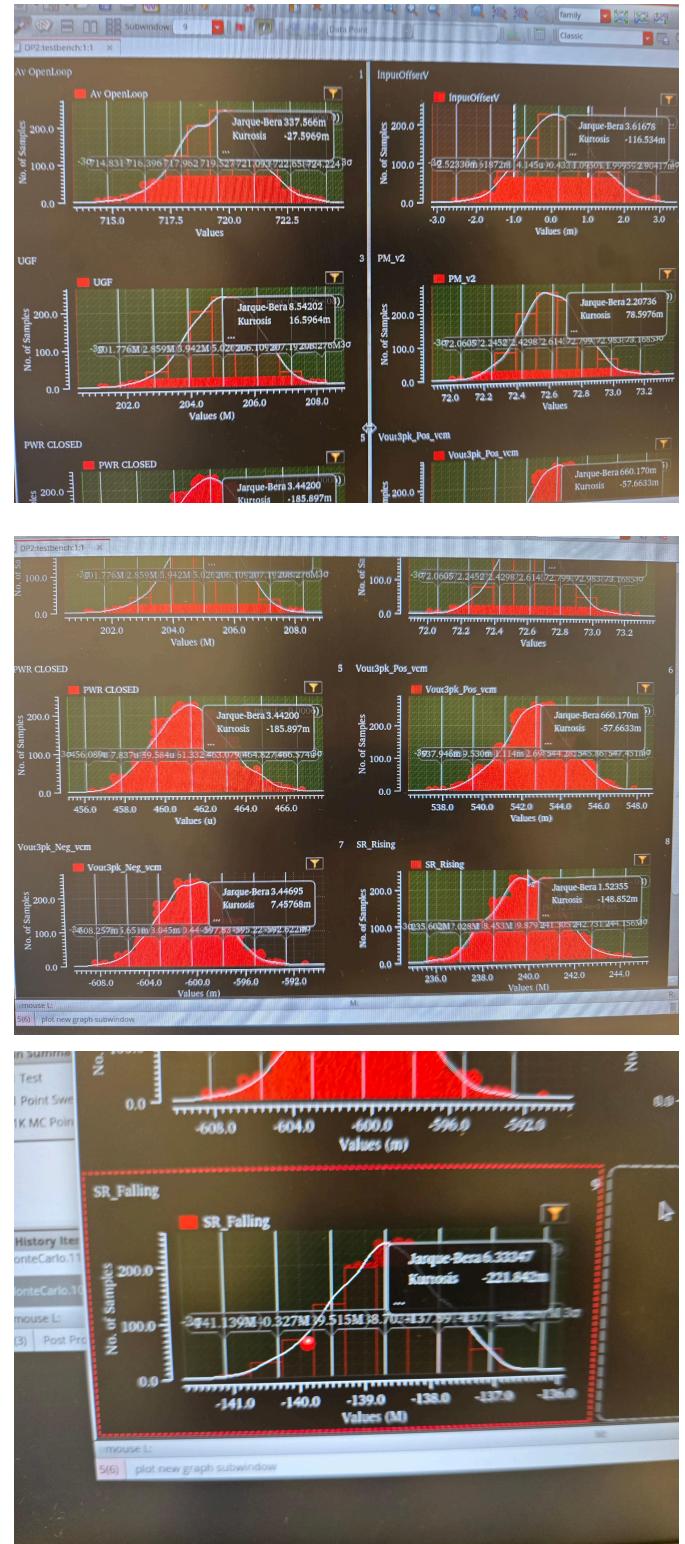
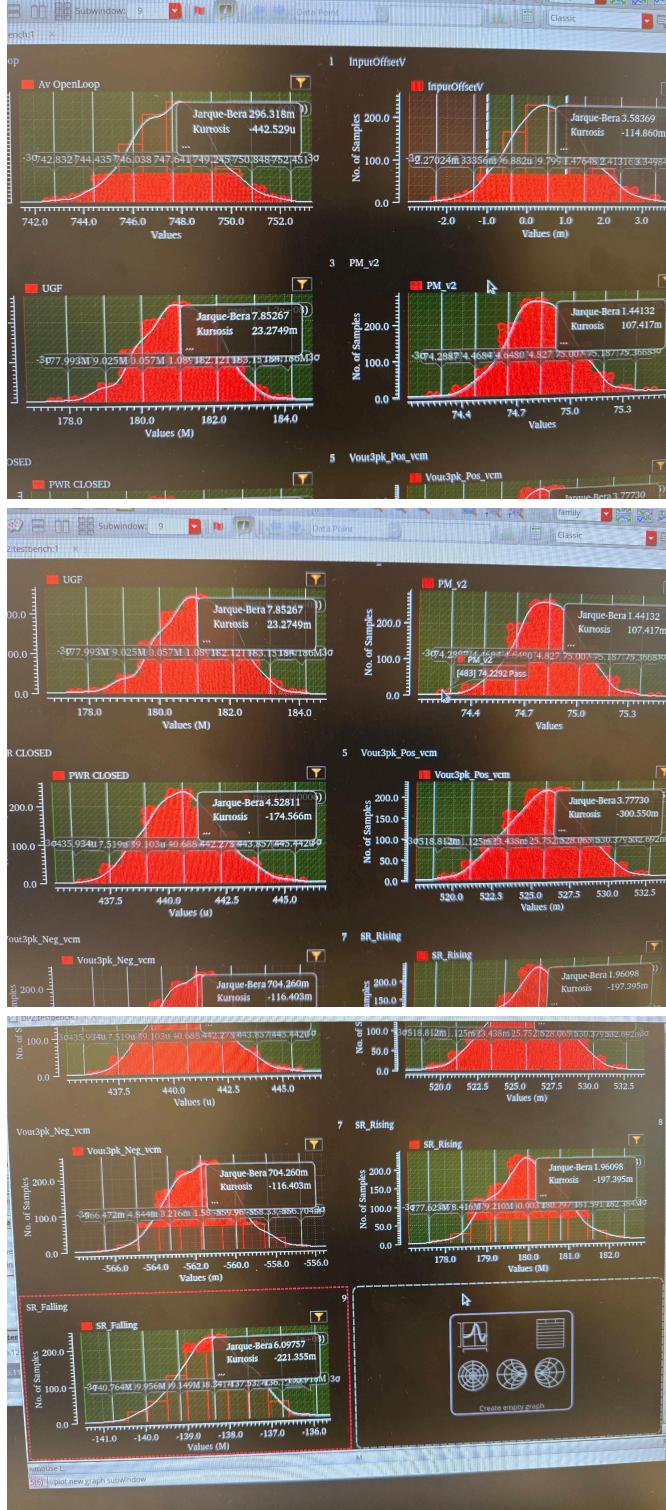
The main challenge that I faced when it came to designing the TIA was meeting the Vcm specs and the input offset specs while running monte carlo analysis. I feel like if I had a higher L, while retaining the same W/L ratios, I would have an easier time dealing with the input offset issues when I run monte carlo analysis, since increasing length would increase transconductance, but also be far more consistent for retaining a constant V<sub>GS</sub>.

#### VII. CONCLUSION

The overall design of the TIA met all of the requirements given the initial 3 Vcm values, but when Monte Carlo Analysis was involved, input offset voltage yield went down drastically(64.6% for Vcm = -0.1V, 73.4% for Vcm = 0V and 74.3% for 0.1V), whereas all other specs were met. The biggest improvement that I would make is to try to increase the length of the MOSFETs, or at very least the differential pair to reduce the input offset issues in Monte Carlo Analysis while trying to maintain the same W/L ratios, by trying to increase L for the differential pair, if not the entire circuit.

#### APPENDIX

## Monte Carlo Analysis Histograms for V = -0.1



## Monte Carlo Analysis Histograms for V = 0

## Monte Carlo Analysis Histograms for V = 0.1

