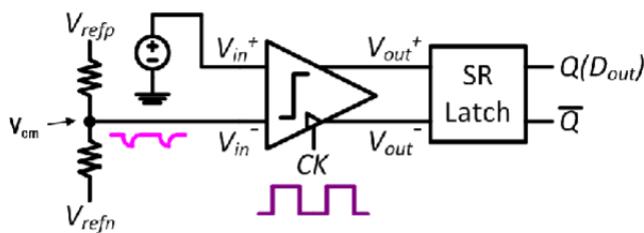


Design of an Comparator from Matthew Choi in 18623 of Fall 24

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Abstract

This particular comparator design meets all of the initial specifications for both 27°C and 100°C. Power at 27°C is 26.06uW, kickback is 6.675mV, the input capacitance is 1.544fF, and standard output deviation is 2.225mV. Common Mode voltage used was 0.6V, and the total area of the comparator was 1.125um².



I. INTRODUCTION

The comparator is an analog circuit device that takes in two different input voltages, and returns a binary output based on which of the input voltages is higher than the other. The initial design of the comparator was a strong arm latch design, since I wanted to create a comparator that would be fast, have a low input offset, and have a relatively low level of power consumption. The said comparator is then connected to a slew latch to stabilize the output of the comparator, as well as keeping speed to a certain threshold.

I initially took inspiration from the strong arm latch design from Ravazi's notes(given in the reading material folder on Canvas), and modified the values initialized so that it would match the gpdk45 process design. Afterwards, taking into consideration that I had to make a layout of the comparator, I sized the widths and fingers so that as many of the PMOS and NMOSes could be merged together with same finger width sizing.

.NOMINAL SPECIFICATIONS AND CONSTRAINTS

Name of the spec.	Spec. corresponding to your design	Performance from your design @ 27°C	Performance from your design @ 100°C
Offset Voltage standard dev (3OVos)	< 10mV	7.944mV	7.842mV
Kickback	Peak < 10mV	7.313mV	6.187mV
Input Capacitance	<20fF	787.8aF	800.7aF
Power Consumption	<150uW	23.87uW	24.92uW

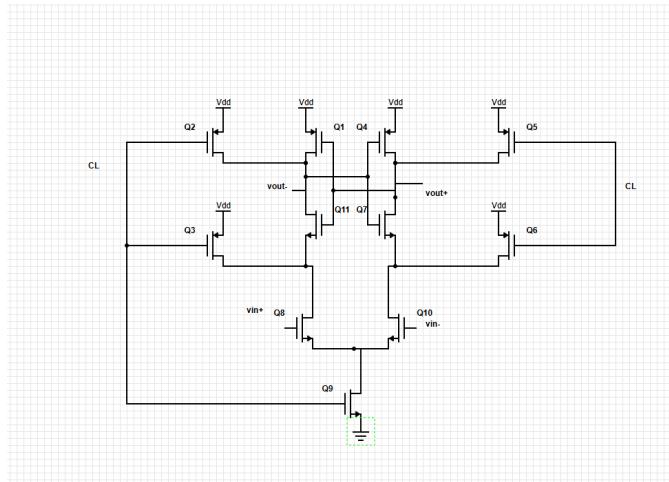
Design constraints:

- Body Effect on N-MOSFETs not sourced to ground
- 5 nm multiples for transistor sizes
- no DC value in biasing
- All substrate terminal should be connected to ground, all PFET substrate can be connected to source
- Must be within gpdk45 constraints
- Supply Voltage of 1V

- Must operate in both room temperature and SS corner(100°C)
 - Must be able to operate at clock rate of 1.2 GHz

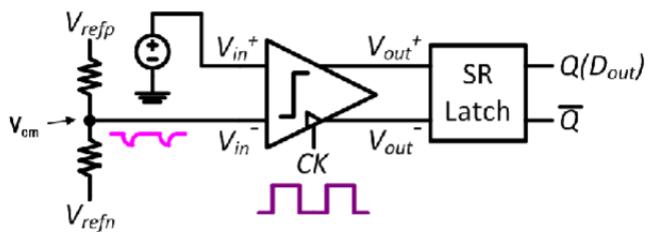
II. CHOICE OF TOPOLOGY AND JUSTIFICATION/HAND ANALYSIS

Due to the very limiting constraints on power, as well as the fast clock rate, I thought that it would be a good idea to use the Strong Arm Latch rather than other simpler configurations such as the sense amplifier. Given gpdk45, I set L to be as low as possible, being 45nm, since given that the latch delay is directly proportional to the input capacitance of the input mosfets. By minimizing the channel length, the gate and channel capacitances are decreased, since they are directly correlated to length regardless of operation region.



I wanted to standardize the MOSFETs to have the same finger width size, due to taking into account the layout portion of the project. Having the same finger width allows separate MOSFETs to be merged together while maintaining the different functions that they originally had. I chose to use 500nm as the base finger length for the PMOSs Q1,2,3,4,5 and 6. Since Q2,3,5,6 all serve as clocked transistors. They were originally set to 500nm, but I changed them to 1um with 2 fingers in width for a more compact layout. Furthermore, I wanted a decently sized differential pair for the inputs MOSFETs, since I wanted them to be large enough so that input offset would not be an issue, so I chose an arbitrary 3um. A higher width would be preferred, but 3um allowed me to have a more consistent kickback than a higher width input MOSFET. Q9 is the tail MOSFET of the comparator, so given the high speed required, we would like it to be larger, since higher Gm leads to faster response time.

III. TESTBENCH



Vcm	Vreset	vdd	vd	nominal
0.6	1	1V	5mV	1

IV. RESULTS

Here you will have to report the numeric values.

A. Performace at different temperature

	Spec. corresponding to your design	Performance from your design @ 27°C	Performance from your design @ 100°C
Offset Voltage ($30V_{OS}$)	< 10mV	7.944mV	7.842mV
Kickback	Peak < 10mV	7.313mV	6.187mV
Input Capacitance	<20fF	787.8aF	800.7aF
Power Consumption	<150uW	23.87uW	24.92uW

B. MC yields at different temperatures

	Results	Yield	Standard Deviation	3 * standard deviation
27°C		100%	2.648mV	7.944mV
100°C		100%	2.614mV	7.842mV

C. Area

Component	Finger Count	Finger Size (nm)	New Width (um)	New Length (um)	New Multiplier	New Area(um ²)
Q1	4	250	1.5	0.045	1	0.045
Q2	2	250	0.5	0.045	1	0.0225
Q3	2	250	0.5	0.045	1	0.0225
Q4	4	250	1.5	0.045	1	0.045
Q5	2	250	0.5	0.045	1	0.0225
Q6	2	250	0.5	0.045	1	0.0225
Q7	3	500	1.5	0.045	1	0.0675
Q8	8	500	4.5	0.045	2	0.36
Q9	4	500	2.5	0.045	1	0.09
Q10	8	500	4.5	0.045	2	0.36
Q11	3	500	1.5	0.045	1	0.0675

Total Area = 1.125um²

D. Power consumption

Power	27	100
Total(uW)	23.87uW	24.92uW

E. FoM calculation

$$FOM = 1/(OV_{os} * power(mW))$$

Temp	27	100
FOM	15820.84225	15351.34312

V. DISCUSSIONS

The main challenge that I faced when it came to designing the comparator was trying to get kickback and input offset working simultaneously. Initially reaching the intended values was quite doable, but I needed to adjust Vcm from 0.5 to 0.6 to have an easier time doing so. Furthermore, if I made my differential pair too large, then the kickback would increase dramatically. Along with that, getting the graphs from the testbench to be as accurate as possible was a challenge as well, since even if all the specs were met, there was still a chance that the Dout graph would be different from the example drawing shown in the schematic. Some improvements I would make is to attempt to make the W finger length a direct ratio of the L length of 45nm instead of an arbitrary number like 500nm. This would decrease the speed of the comparator, but would result in a whole number W/L ratio, making potential calculations a lot more simple for

VI. CONCLUSION

The overall design of the comparator meets all of the initial specifications for both 27°C and 100°C. Power at 27°C is 23.87uW, kickback is 6.675mV, the input capacitance is 0.7878 fF, and standard output deviation is 2.648mV. To potentially improve the circuit, I could try increasing the width of the input MOSFETs, while decreasing the width of the tail MOSFET to attempt to get a lower standard deviation for the input offset.

Layout Section:

Abstract

This layout of the comparator design meets all of the initial specifications for both 27°C and 100°C. Power at 27°C is 41.76u, kickback is 3.848mV, the input capacitance is 794.8aF, and standard output deviation is 2.225mV. Common Mode voltage used was 0.6V, and the total area used in the layout was 39.06 um².

LAYOUT METHODOLOGY:

the terms Q1, and such refer to how the mosfets are represented in the topology schematic

When designing the layout of the mosfet, I initially decided to merge all of the PMOSFETs(Q1,2,3,4,5,6) together, since all of them had the same finger sizing of 250nm, as well as length of 45nm. Furthermore, Q2,3 and Q5,6 respectively also shared gate with the clock input, so I utilized the diffusion sharing method shown in the lecture notes to merge these mosfets. Furthermore, Q1 could be merged with the combination of Q2 and Q3, as well as Q4 with Q5 and Q6, due to the mutual Vout- connection between Q1 and Q2, and the Vout+ connection between Q4 and Q5. Since Q1,2,3 and Q4,5,6 have a matching orientation, using the mutual VDD connection, they can be merged together.

Regarding the cascaded NMOSFET pair(Q7,11) above the input differential pair, they have a matching orientation, but none of the node connections allow diffusion sharing, so they were simply placed right next to each other in parallel, since a symmetric layout reduces potential input offset.

For the differential input NMOSFET pair(Q8,10), they have a matching orientation, and the source of the pair is the drain of the tail NMOSFET, so this particular pair can be used for diffusion sharing. Furthermore, this pair utilizes multipliers to compensate wide mosfet, since each MOSFET would have an effective width of 8um, and a multiplier can help reduce it to 4um, allowing us to be more space efficient. Furthermore, with the usage of multipliers, the common centroid methodology can be used to even out potential variations in the differential input. Although there is a slight drawback of potential metal 1 and 2 mismatching thanks to routing issues, since there is no size limitation, this was not a major concern.

Finally for the tail MOSFET(Q8), I directly connected the drain of the tail to the source of the differential input. Furthermore, to ensure that all NMOSFETs were grounded, I created a via grounded to the P-sub, which was directly

connected to the source of the tail MOSFET, since it was meant to be connected to ground.

Other practices I utilized in layout include utilizing metal 1 and 2 for very specific purposes. I used metal 1 only for horizontal connections, and only metal 2 for vertical connections. This came in very handy to attempt to make all the metal connections as symmetrical as possible, as well as helping debug potential LVS errors.

POTENTIAL AREAS OF VARIATION:

The parts with the highest sensitivity to layout and process variations are the metal connections and the input offset in the differential input pair. If the metal connections are not as symmetric as possible, the voltage needed inside of the differential pair may not be as accurate as intended, leading to a larger input offset. Furthermore, the narrower the metal is, the more prone it is to not completely transfer the intended voltage. Input offset is also prone to change thanks to potential asymmetric placement of the differential pair, as well as some level of uncertainty thanks to the process variations.

RESULTS:

Performance at different temperatures

	Spec. corresponding to your design	Performance from your design @ 27°C	Performance from your design @ 100°C
Offset Voltage (3OV _{OS})	< 10mV	7.269mV	7.329mV
Kickback	Peak < 10mV	3.848mV	3.224mV
Input Capacitance	<20fF	794.8aF	806.8aF
Power Consumption	<150uW	41.76uW	42.76uW

F. MC yields at different temperatures

	Results	Yield	Standard Deviation	3 * standard deviation
27°C		99.6%	2.443mV	7.329mV

100°C		99.5%	2.423mV	7.269mV
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G. Post Layout FoM calculation

$$\text{FOM} = 1/(\text{OV}_{\text{os}} * \text{power(mW)})$$

Temp	27	100
FOM	9802.030353	9651.812784

DISCUSSIONS:

The main challenge I faced when designing the comparator was trying to modify the existing design so that I could efficiently merge MOSFETs. I went through several iterations before realizing that all of the P-MOSFETs could be merged together, and how to use multipliers to create more symmetrical metal connections for the differential pairs. The usage of multipliers and symmetry allowed me to create a more consistent design with a lower input offset than my other iterations.

CONCLUSION:

The overall layout of the comparator meets all of the specifications for both 27°C and 100°C. Power at 27°C is significantly higher but still comfortably within specifications at 41.76uW. The input capacitance is relatively similar to that in the schematic at 794.8aF at 27°C. Kickback has significantly reduced from the schematic design to 3.848mV at 27°C. Finally, offset voltage remains relatively similar at 27°C, resulting in 7.269mV.

Annex:

I changed the schematic from the previous DP3 report due to significant issues with the layout in contrast to the schematic, which worked as intended. The input offset being returned was significantly higher in magnitude than expected at -13mV even without running monte carlo analysis, and it affected the waveform to the point where the Dout graph was consistently inaccurate for the layout with the initial schematic.

The primary changes I made in comparison to the previous version of the schematic are reducing the widths of the P-MOSFET, along with reducing the finger length of the P-MOSFETs from 500nm to 250nm. The number of fingers used remained the same, but overall width was reduced to half of what it was.

Along with that, I realized that the main reason why the layout input offset was high in magnitude was due to the input differential pair not being wide enough. Initially, I planned on converting the width from 3um to 8um, but realized that for efficiency purposes, using a multiplier with 4um would yield a more area efficient layout. Furthermore, it also helps increase the symmetry of the layout when using metal connections thanks to common centroid methodology.

Increasing the length of the input differential pair would lead to the kickback drastically increasing, so in order to compensate, I reduced the width of the tail MOSFET significantly, down from 11um to 2um.

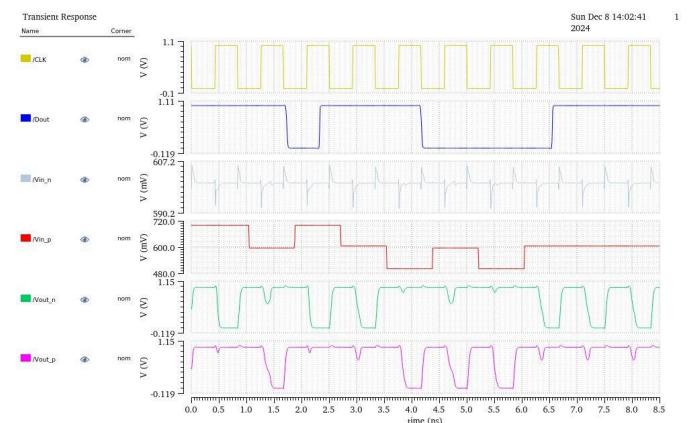
The cascaded N-MOSFETs also contributed to the kickback, so I also halved their overall width by a factor of 2 by reducing the finger length from 500 nm to 250 nm.

These overall changes resulted in a consistently accurate waveform output, as well as meeting the specifications for both 27°C and 100°C.

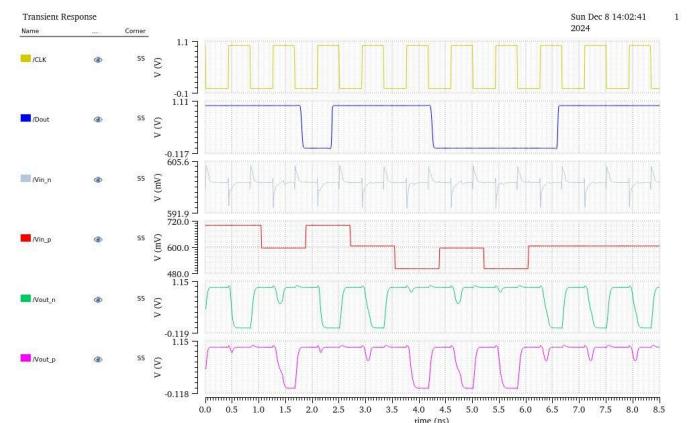
APPENDIX

Schematic Section

Waveforms(27°C)



Waveforms(100°C)

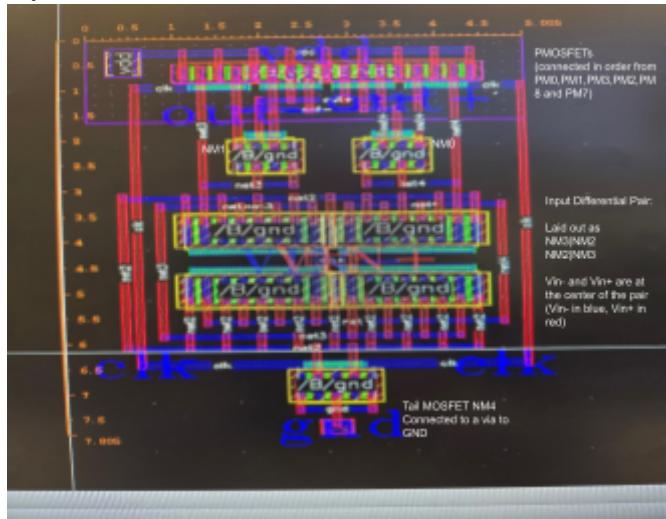


Monte Carlo Graph Results(27°C & 100°C from left to right)



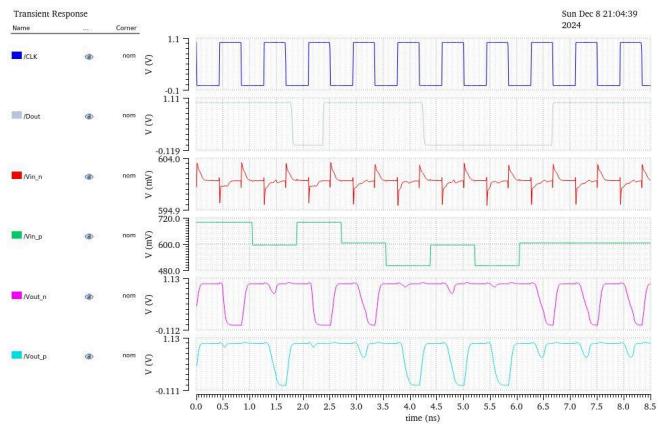
Layout Section

Layout Screenshot

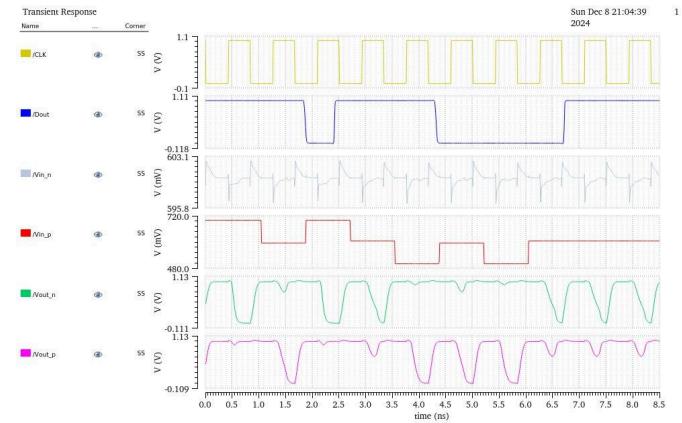


Area of 39.064 um²

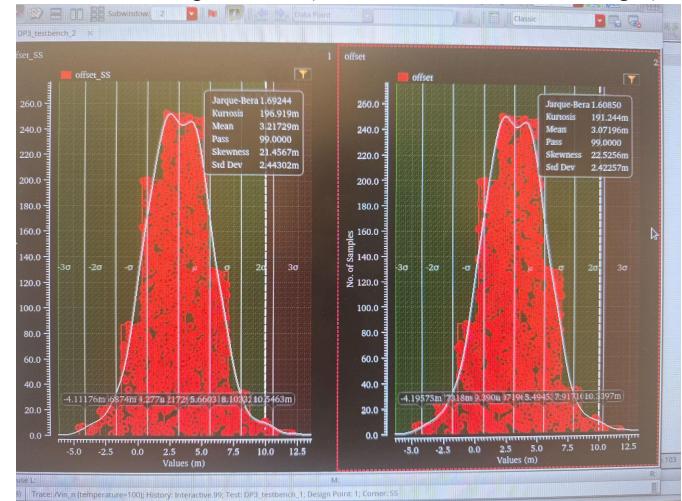
Waveforms(27°C)



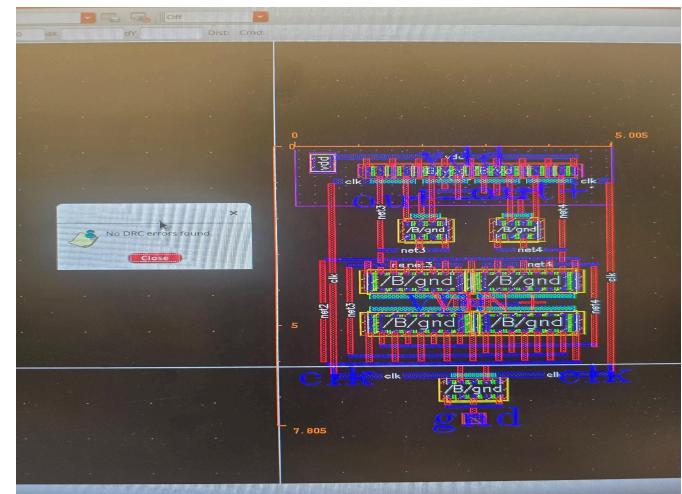
Waveforms(100°C)



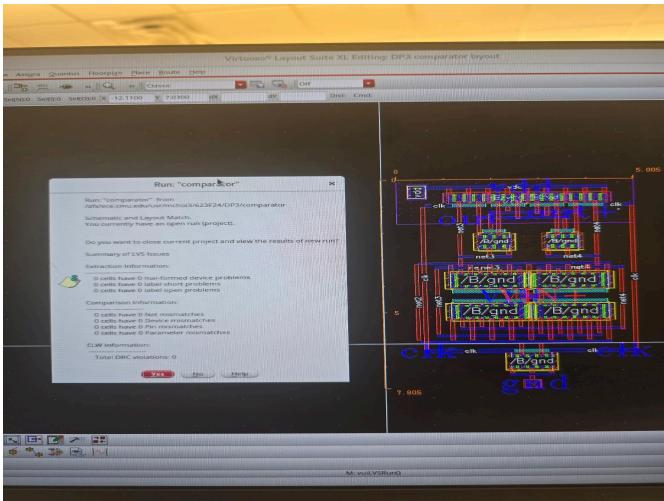
Monte Carlo Graph Results(27°C & 100°C from left to right)



DRC



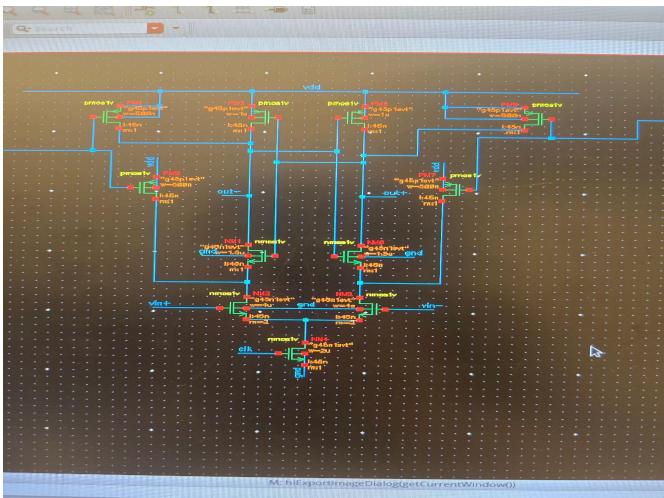
LVS



Testbench Values

Vcm	Vreset	vdd	vd	nominal
0.6	1	1V	5mV	1

Schematic



Device Dimensions

Component	Finger Count	Finger Size (nm)	New Width (um)	New Length (um)	New Multiplier	New Area(um ²)
PM0	2	250	0.5	0.045	1	0.0225
PM1	2	250	0.5	0.045	1	0.0225
PM2	4	250	1	0.045	1	0.045

PM3	4	250	1	0.045	1	0.045
PM7	2	250	0.5	0.045	1	0.0225
PM8	2	250	0.5	0.045	1	0.0225
NM0	3	500	1.5	0.045	1	0.0675
NM1	3	500	1.5	0.045	1	0.0675
NM2	8	500	4	0.045	2	0.36
NM3	8	500	4	0.045	2	0.36
NM4	4	500	2	0.045	1	0.09

This table is based on the schematic in the appendix, and all values are identical to that of the table in the schematic section of the report