

# Design of a Transimpedance Amplifier (TIA) from Matthew Choi in 18623 of Fall 24

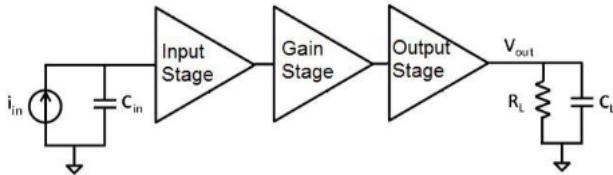
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## Abstract

The TIA design that was achieved had an input impedance of 195 ohms, a trans-impedance gain of 444.7k ohms, a bandwidth of 81 MHz, a power of 201.3 uW, and an output swing of 320 mV at room temperature of 27°C. Over different temperature ranges of 0 and 100°C, monte carlo analysis yield was 99.5 percent, and the total area of the design was 271.3012 um<sup>2</sup>. The DC bias value was 30 uA, and the AC amplitude was 700 nA.

## I. INTRODUCTION

The trans-impedance amplifier(TIA) is a current to voltage converter that is usually associated with detecting small currents in the uA region produced by photodiodes and MEMs sensors. The output of the TIA can be utilized in piezooresistive pressure sensors, probes and accelerometers.



The initial design of the TIA was designed into 3 stages, being the Input, Gain and Output stage. The Input stage would be taking in the input current and combining it with the bias current

When it comes to the design procedure, I started with the initial current mirror setup knowing that to power up all the potential mosfets, the input current wouldn't be enough in the input stage. Using the one external current source given to us, I decided that it would be for the best to use it to power up the MOSFETs and replicating it through

current mirrors and cascoding while meeting the required specs for input and output resistance. Afterwards, I began planning for the gain stage by trying to find a way to maximize bandwidth while trying to increase the gain as much as possible. Finally, I wanted enough current to flow through the drain stage while also minimizing the gain. When it came to retrieving the width and length of the mosfets, I set my mosfet default to 0.5 um, while using the Gm/Id calculator to get a satisfactory Gm/Id value with a VDS to retrieve width. If the width didn't satisfy the specs that were needed for saturation, I modified the width until it did so. If there were ever a point that I maximized width, I would then alter L to try to raise the width/length ratio.

## II. NOMINAL SPECIFICATIONS AND CONSTRAINTS

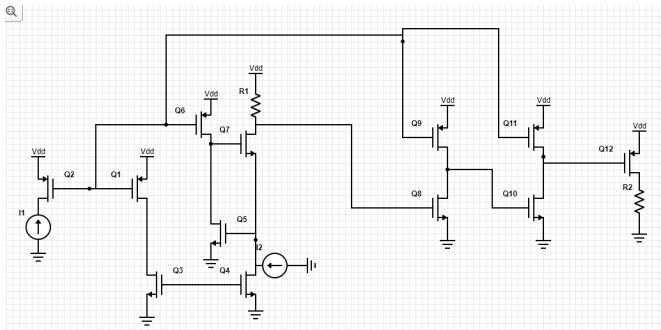
Name of the spec.	Spec. corresponding to your design	Performance from your design @ 27°C
Gain (ohm)	>100k	444k
BW (MHz)	> 65MHz	81Mhz
Input Impedance(ohm)	< 250	195
Output Swing(V)	> 300mV	320mV
Power(uW)	<500uW	201.3uW

Design constraints:

- Temperature Range

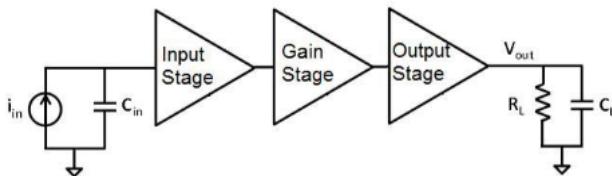
- One ideal current source in testbench from ground to bias pin in test bench
- No ideal elements in the design
- Body Effect on N-MOSFETs not sourced to ground
- 5 nm multiples for transistor sizes
- no DC value in biasing
- All substrate terminal should be connected to ground, all PFET substrate can be connected to source
- vdd value should be set to 1

### III. CHOICE OF TOPOLOGY AND JUSTIFICATION



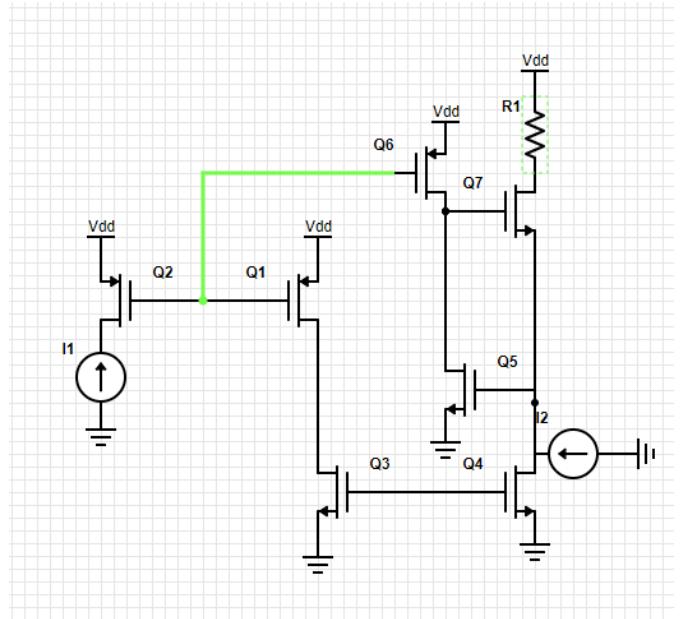
The transimpedance amplifier is composed of 3 stages, being the Input, Gain and Output stages. The initial Input stage is composed of a PMOS and NMOS current mirror to duplicate the bias current, as well as a Cascoded Common Gate Amplifier to minimize input resistance while also maximizing the resistance  $R_1$  that is used to calculate for transimpedance gain. The Gain Stage is divided into two common source active load amplifiers, which provide more gain than a resistor load while not being as temperature dependent. Since the active load is mirrored by the PMOS current mirror, the gain stage does not consume a lot of power, since the setup has a low  $30\mu A$  bias current. The output stage utilizes a common drain amplifier with a resistive load to maximize bandwidth, and to minimize gain loss while also keeping a high current flowing through the drain amplifier. a NMOS is used in the drain region, since we assume that the output of the gain stage will be high enough so that we have to use a NMOS instead of the PMOS

### IV. TEST BENCH



### V. HAND ANALYSIS CALCULATION

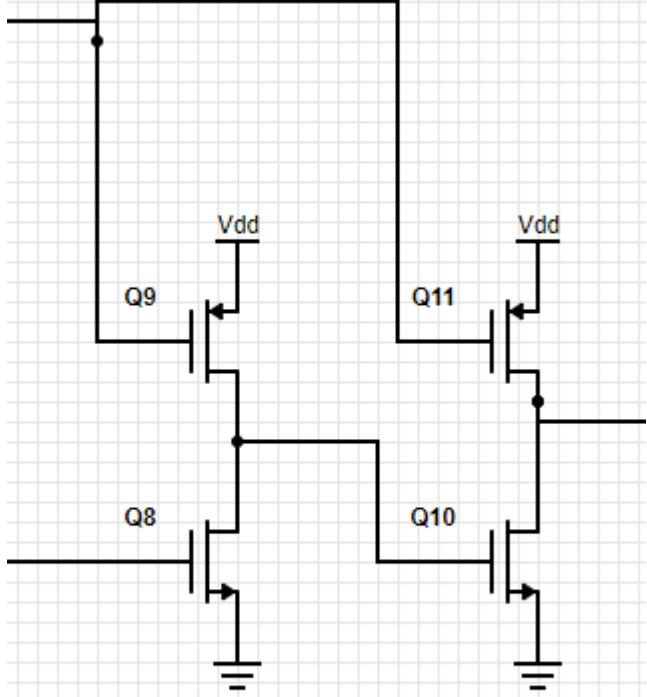
#### A. The input stage



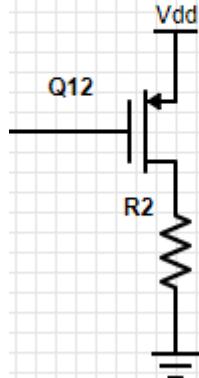
For the input stage, I used a  $G_m$  boosting Common Gate Amplifier setup to minimize the input impedance (this setup is directly referred from pages 23-24 of the lecture 5 slides). Q1 and Q2 act as a PMOS current mirror, while Q3 and Q4 are a NMOS current mirror. Considering Q6 is identical to Q1 and Q2 as a mirrored PMOS, the input impedance is given as  $1/gm(1 + A)$ , for which  $A = G_{m5}r_{o4}r_{o6}$  assuming that  $R_1 \ll r_{o5}$ . The transimpedance gain is the gain of the total circuit multiplied by  $R_1$ .

VDD	VSS	$C_{in}$	$C_L$	$R_L$	Bias	Input
1V	0V	1pF	2pF	10k $\Omega$	30uA	0.7uA

### B. The Gain stage



### C. Output buffer stage



The drain stage is a resistive load common drain, and  $V_{out}$  is  $gm_{12} * (V_{in} - V_{out}) * R_2$ , so  $V_{out}(1 + gmR_2) = gmR_2 * V_{in}$ , so  $V_{out}/V_{in}$ , or gain is equal to  $(1+gmR_2)/gmR_2$ . Furthermore,  $V_{out} < V_{DD}$ , and  $V_{out} = V_s$ , and assuming saturation status, output swing is the bound in which  $V_{ds} > V_{gs} - V_{th}$ , which has to be higher than 300mV.

## VI. RESULTS

Here you will have to report the numeric values.

### D. Performance at different temperature

Spec. (Units)	0°C	27°C	100°C
Transimpedance gain (ohm)	471.599k	444.707k	334.098k
BW (MHz)	84.5354	81.3706	72.5478
Input Impedance(ohm)	218.097	195.746	181.391
Output Swing(mV) @10MHz	347.978	341.26	305.617
Output Swing(V) @100Hz	346.87	338.38	304.27

#### E. MC yields at different temperature

	TestBench	Results	Yield
0°C			100%
27°C			100%
100°C			99.5%

#### F. Area Calculation

Component	Total Width (um)	Length (um)	Multiplier	Area(u m <sup>2</sup> )
Q1	8	0.5	1	4
Q2	8	0.5	1	4
Q3	6	0.5	1	3
Q4	6	0.5	1	3
Q5	29.8	1	1	29.8
Q6	8	0.5	1	4
Q7	47.5	1	1	47.5
Q8	0.54	0.5	1	0.27
Q9	8	0.5	1	4
Q10	4.2	0.5	1	2.1
Q11	8	0.5	1	4
Q12	20	0.5	1	10
R1	1.5	45	1	67.5
R2	1.5	30	1	45

Total area = 271.3012 um<sup>2</sup>

#### G. Power consumption calculation

I = 201.3uA, VDD = 1V, so power consumption = 201.3uW

#### H. FoM calculation

By now you should have all the values to calculate the FoM using the given formula in the handout. Pay attention to the units and the order of magnitude. FoMs for three temperatures are to be reported.

0°C	27°C	100°C
$3.37258304 \times 10^{10}$	$4.15992576 \times 10^{10}$	$3.93958772 \times 10^{10}$

Power	0°C	27°C	100°C
Gate(uW)	102.7 uW	97.545 uW	93.453 uW
Source(uW)	60 uW	60 uW	60 uW
Drain(uW)	28.06 uW	28.06 uW	27.8 uW
Total(uW)	203.55 uW	201.356uW	195.533uW

## VII. DISCUSSIONS

The main challenge that I faced when it comes to designing the TIA was the output swing, and how to set the drain stage so that I could meet the specific specs while trying to keep the input at the drain stage as high as possible. Maximizing the width of the mosfet in the drain stage would increase bandwidth, but would subsequently lower the voltage swing. Another challenge I had was increasing the gain of the common source gain stage will also trying to keep bandwidth above 65 MHz, since it was a rigorous task to reach the bandwidth specs and trans-impedance gain simultaneously.

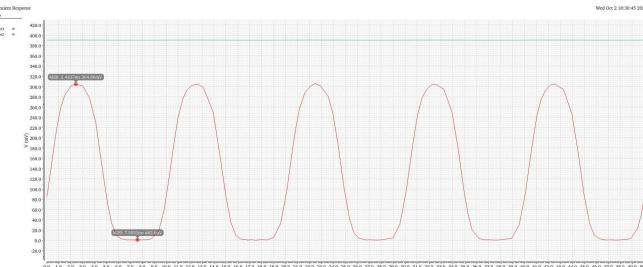
## VIII. CONCLUSION

The overall design of the TIA met all of the requirements even with the Monte Carlo analysis. Overall, this design taught me a lot about how to design an effective TIA, and the improvements I can make on it. I feel like I could have gotten a better output swing if I had forced more current through the drain stage, while also making sure that the output voltage wouldn't be as low as it was in the design. This would lead to a more consistent output swing without any dents as shown in the graphs.

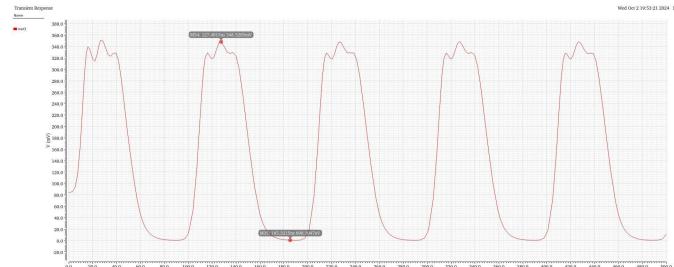
## APPENDIX



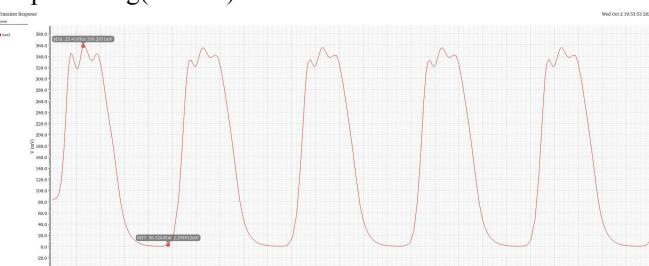
Input Impedance(lower marker) and Transconducudance gain(higher marker) at 100°C



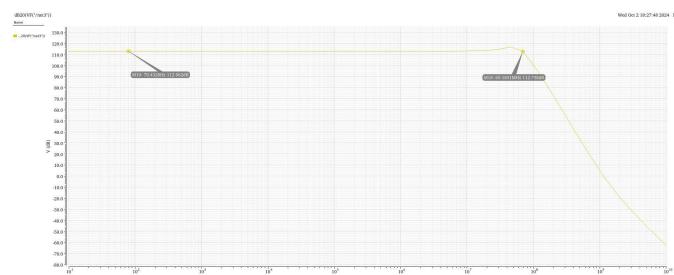
Output Swing(100 Hz) at 100°C



Output Swing(10 MHz) at 27°C



Output Swing(10 MHz) at 100°C



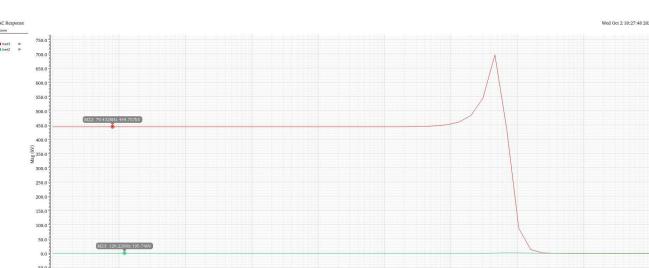
DB gain at 27°C



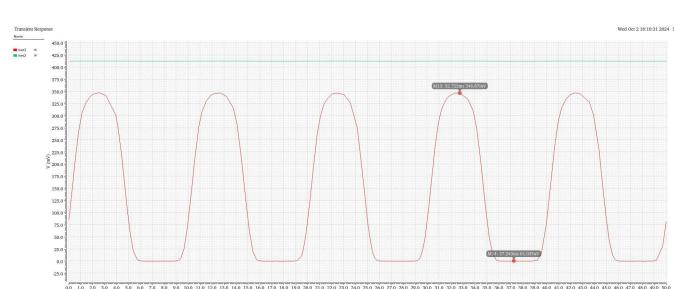
DB gain at 100°C



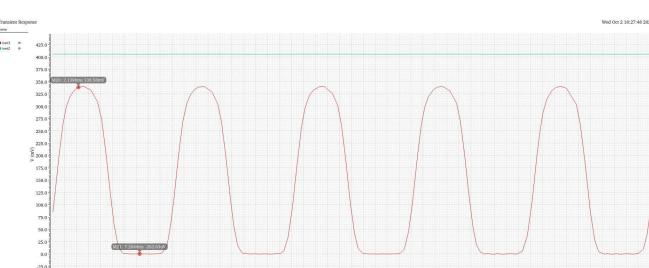
Input Impedance(lower marker) and Transconducance gain(higher marker) at 0°C



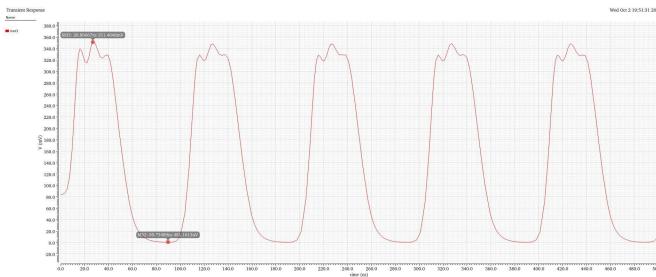
Input Impedance(lower marker) and Transconducance gain(higher marker) at 27°C



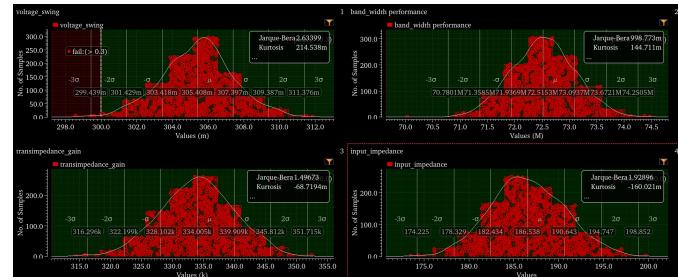
Output Swing(100 Hz) at 0°C



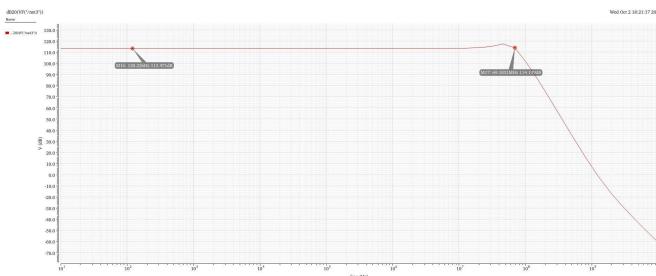
Output Swing(100 Hz) at 27°C



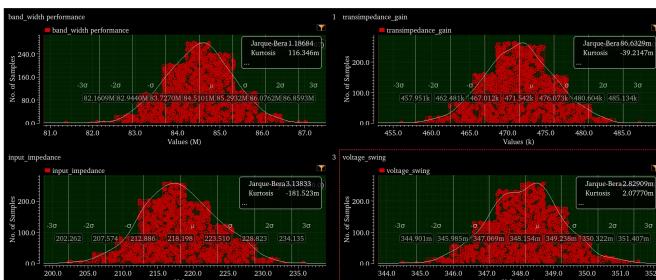
Output Swing(10MHz) at 0°C



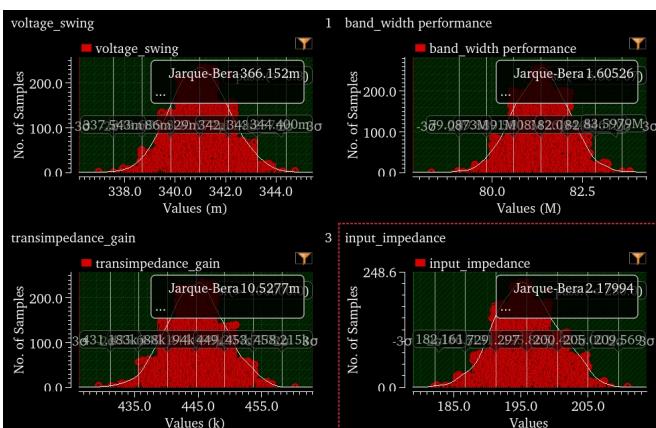
Monte Carlo Results at 100°C



DB gain at 0°C



Monte Carlo Results at 0°C



Monte Carlo Results at 27°C