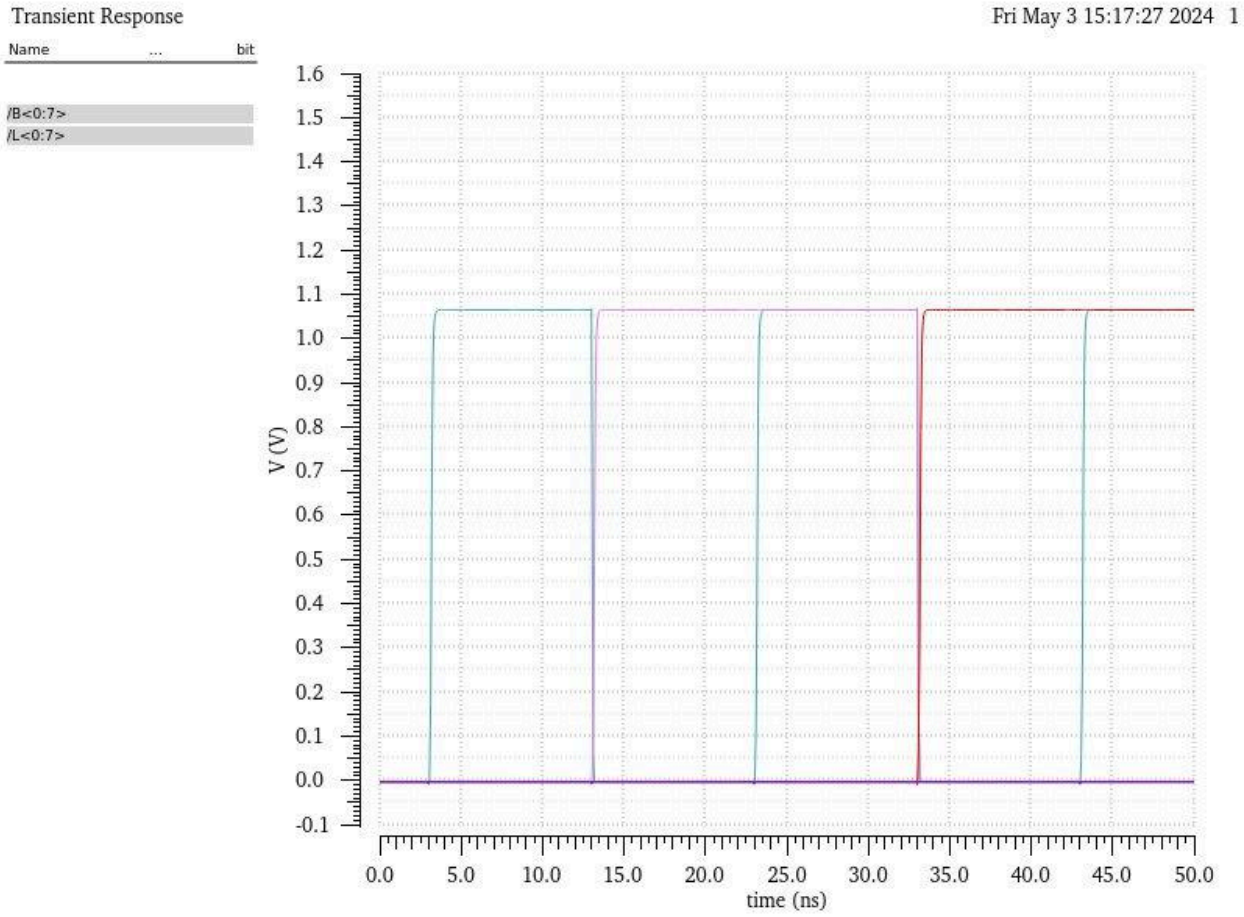
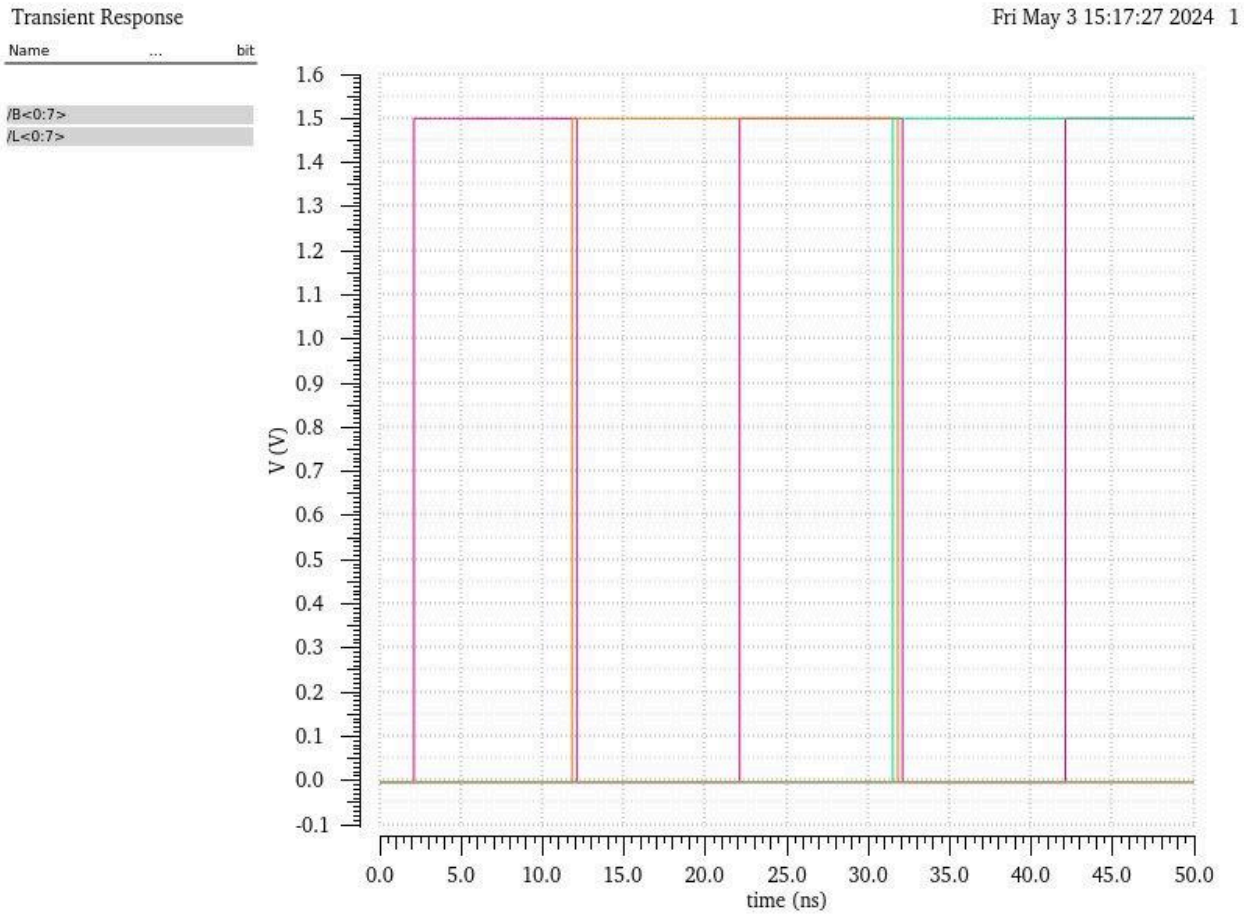
Q2.1

There are a total of 4 inverters and 2 transmission gates in this topology. This circuit is essentially 2 tri-state inverters and 2 inverters.

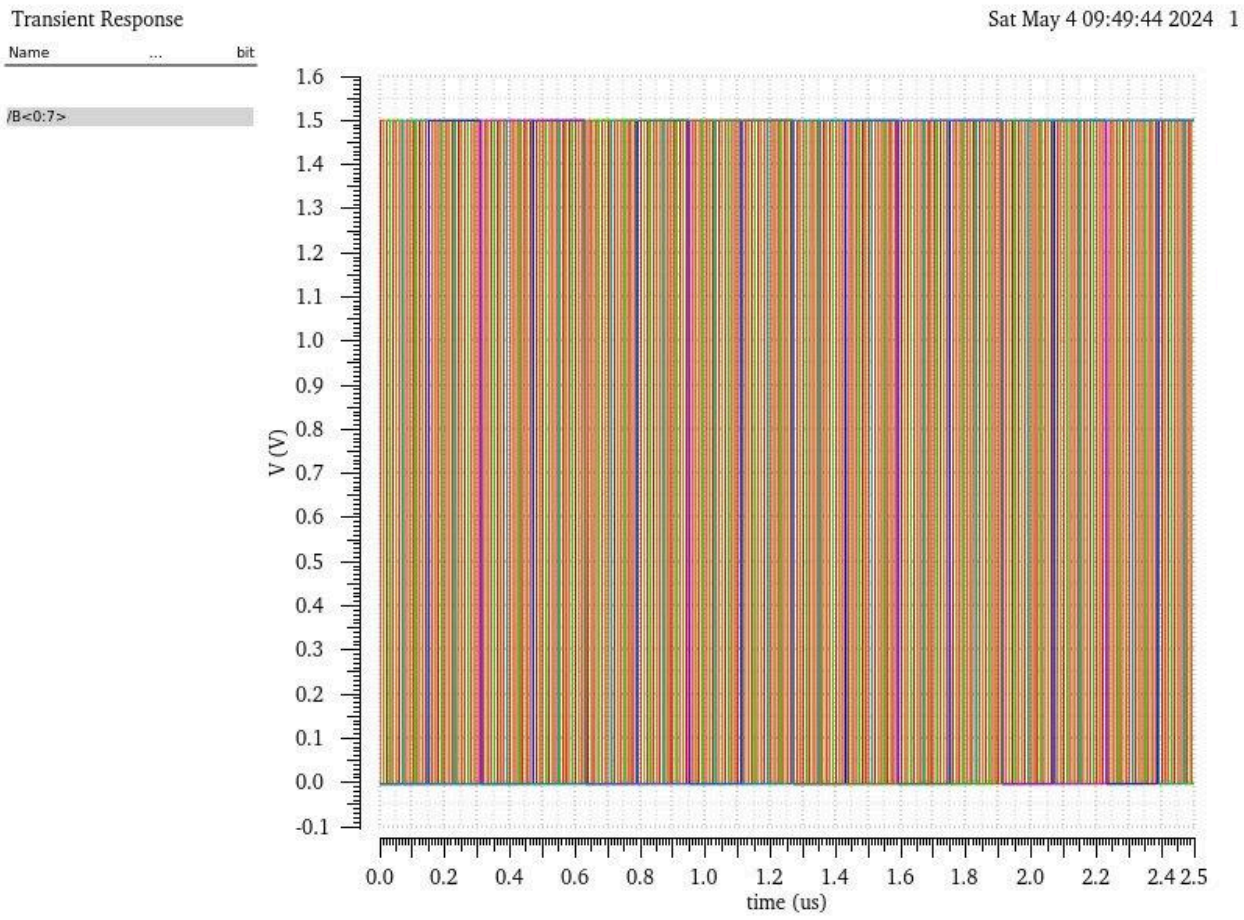
Q2.2





When EN = 0 and EN_B = 1, then Vout returns the previously stored value in the tri-state inverter with a propagation delay. When EN = 1, and EN_B = 1, then Vout returns Vin, and also stores Vin inside of the tri-state diagram for future usage with the same propagation delay.

Q2.3



The counter circuit counts the number of voltages that they receive as inputs, and they count the number of voltages that they receive as logic value ‘1’ and return the total number of logic value ‘1’s total that it has received.

The latch circuit is a circuit meant to store information to be used at a different point, and if there is high impedance in the transmission gate, the stored information

Q2.4

If EN and ENB were to be accidentally swapped, then the transmission gates would be doing the complete opposite effects within the circuit. If the transmission gates were initially supposed to be returning an inverted version of the data, then with the swap, they would now return high impedance, and return the previously stored value within the transmission gates

Q3.1

If V1 is turned on, Vo is V/24

Q3.2

If V2 is turned on, Vo is V/12

Q3.3

If V3 is turned on, Vo is V/6

Q3.4

If V4 is turned on, Vo is V/3

Q3.5

For maximum Vo, we would turn on V4, which has max Vo of V/3

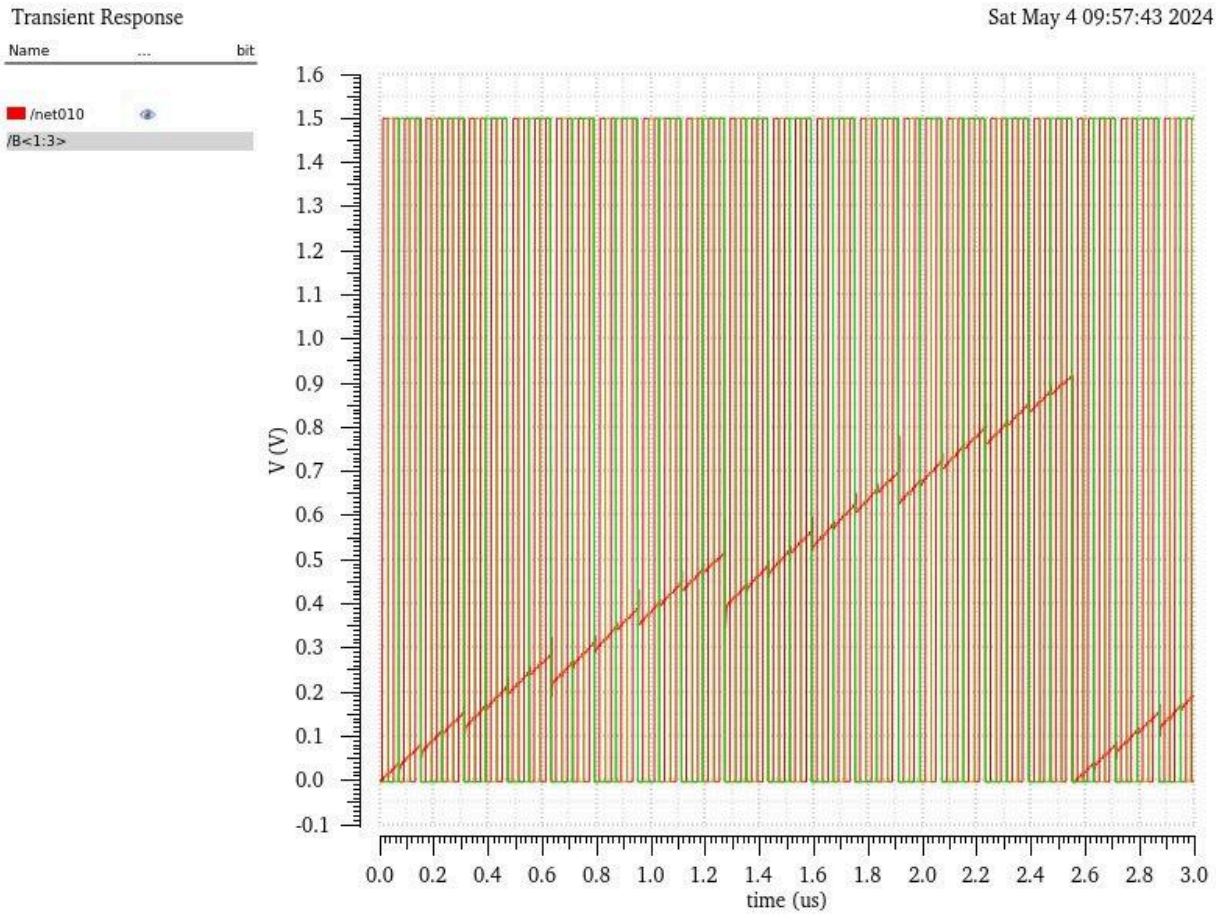
Q3.6

For minimum Vo, we would turn on V1, which has min Vo of V/24

Q3.7

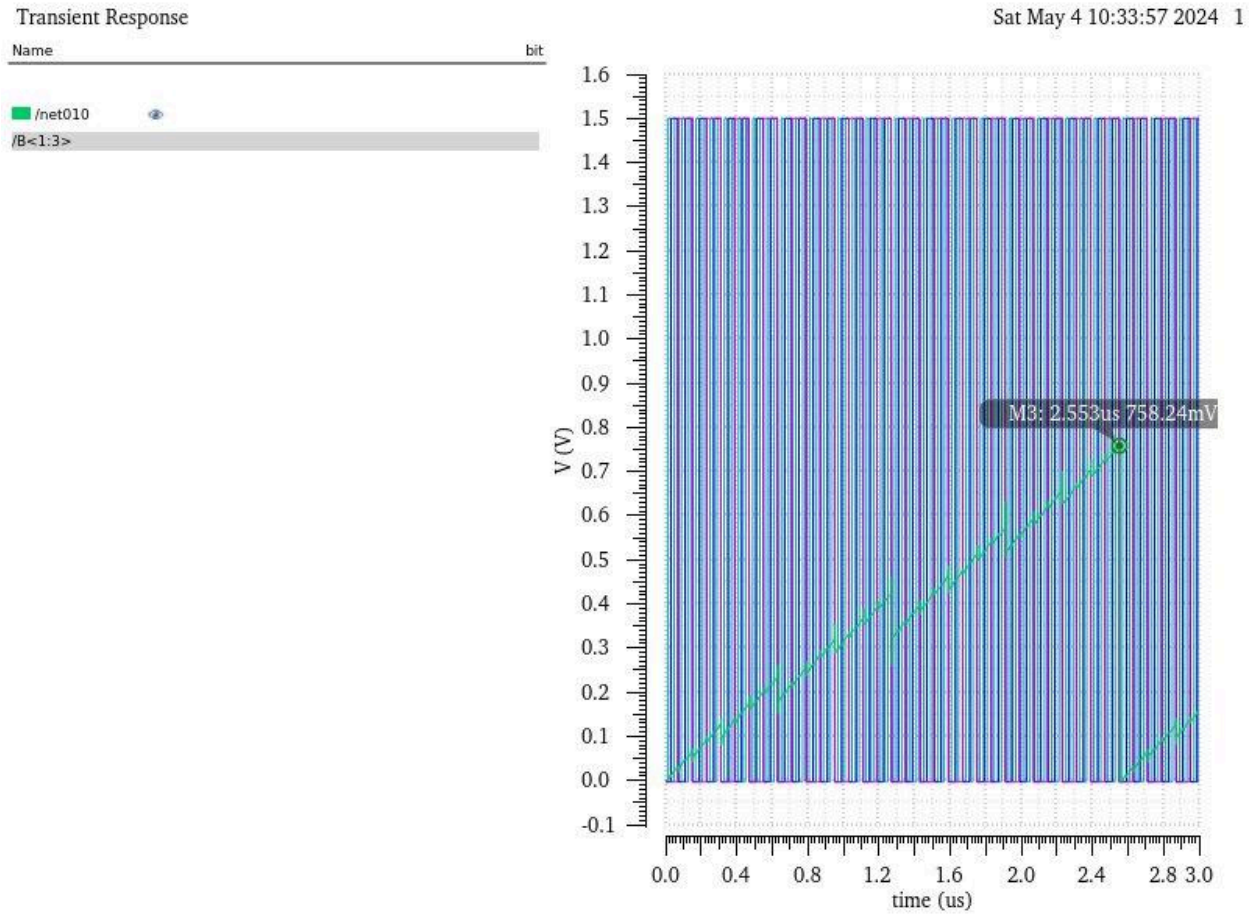
The smallest change that can be made is from V1 to V2, which has a difference of V/12 - V/24, which is equal to V/24. With 4 bits, a total of 16 different voltages can be generated with the 4 bits

Q3.8

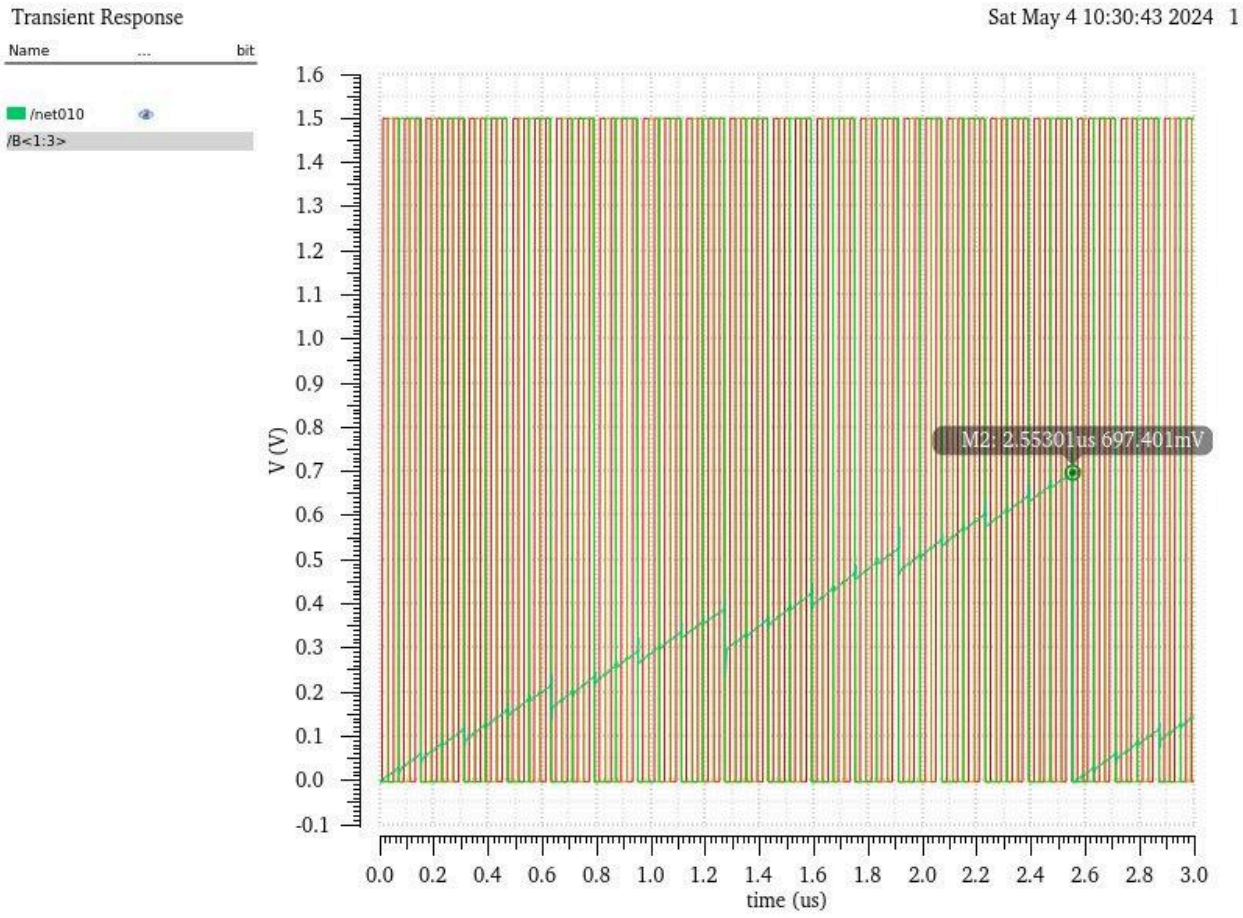

Transient Response
Sat May 4 09:57:43 2024 1
Name
...
bit
/net010
/B<1:3>
V (V)
time (us)

Q3.9

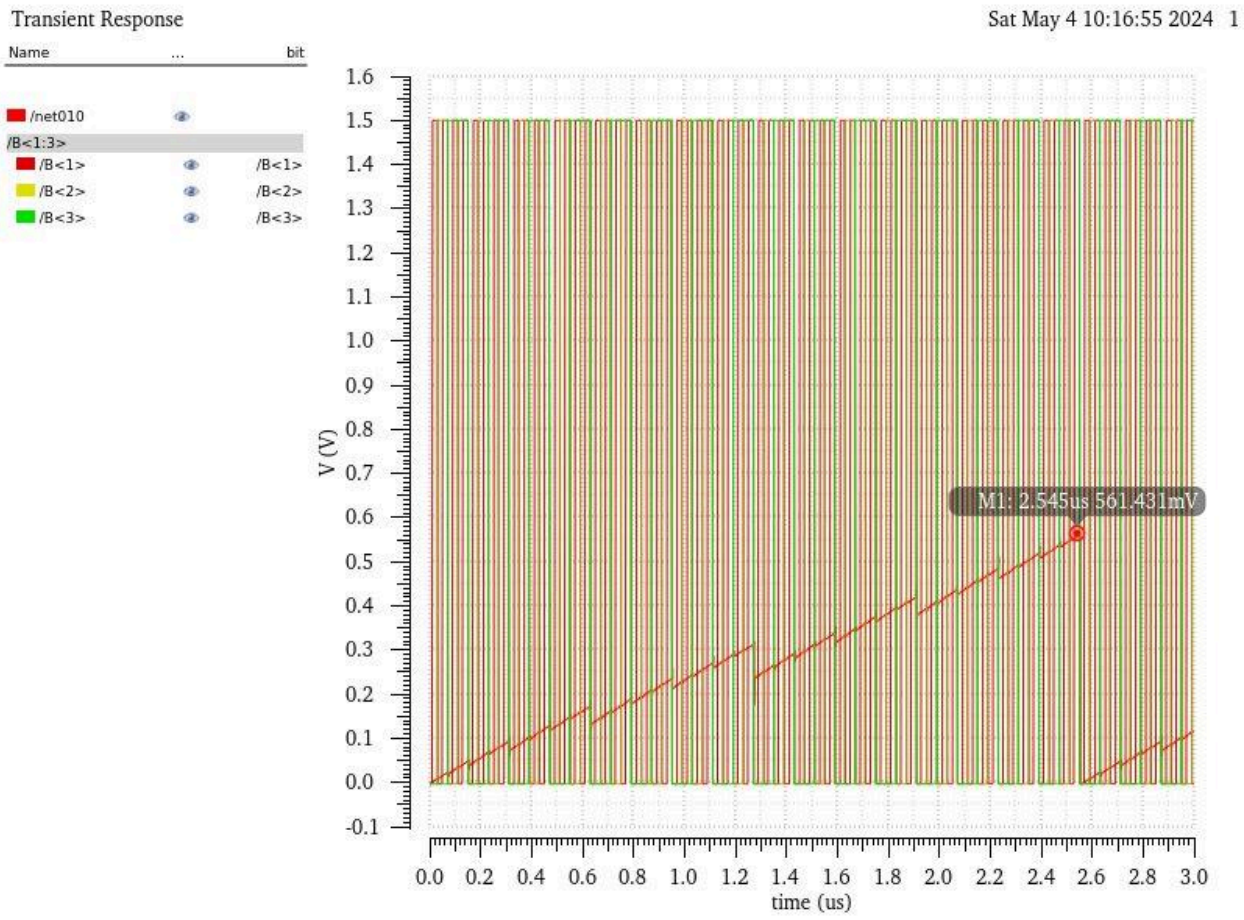
15k


Transient Response
Sat May 4 10:33:57 2024 1
Name
bit
/net010
/B<1:3>
M3: 2.553us 758.24mV
V (V)
time (us)
1.6
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
0.0
0.4
0.8
1.2
1.6
2.0
2.4
2.8
3.0

10k


Transient Response
Sat May 4 10:30:43 2024 1
Name
...
bit
/net010
/B<1:3>
M2: 2.55301us 697.401mV
V (V)
time (us)
1.6
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0 2.2 2.4 2.6 2.8 3.0

5k



Q3.10

3R after merging all resistors into 1 for the DAC 8 given R and 2R. This impacts the output range of the DAC, the overall resistance of the DAC remains consistent, which helps reduce potential noise. To bring the data closer to the no load case, we would change the impedance towards the very left of the DAC to bring it closer to the no load case.

Q3.11

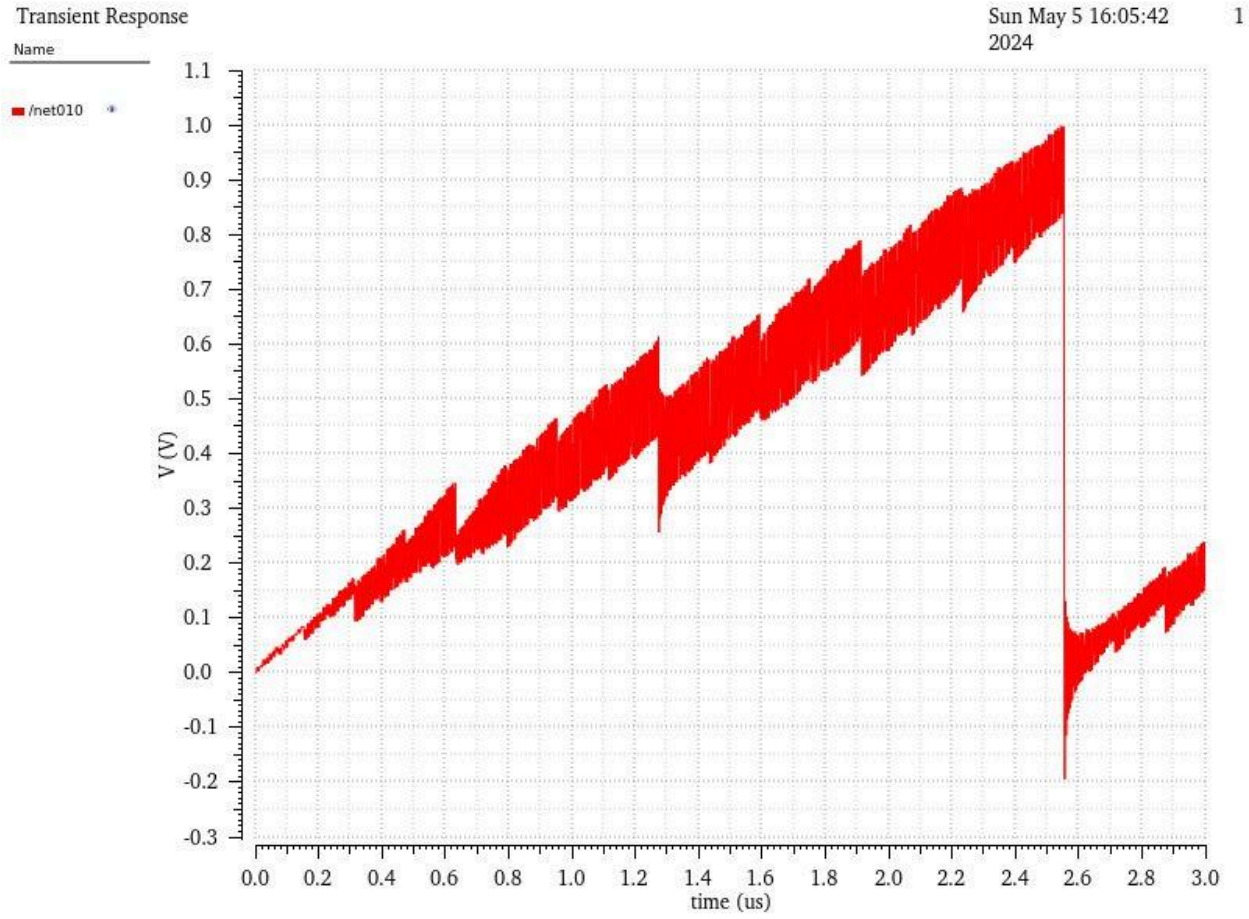
If the DAC is wired straight in instead of the latch, then the signal being sent is less stable due to the larger fluctuation in voltage, and the noise can actually end up modifying the initial data being sent, whereas having a latch would allow the data to be loaded safely by saving it. Furthermore, storing data is essential for sequential processing to ensure the safety of each piece of data in the sequence.

Q4.1

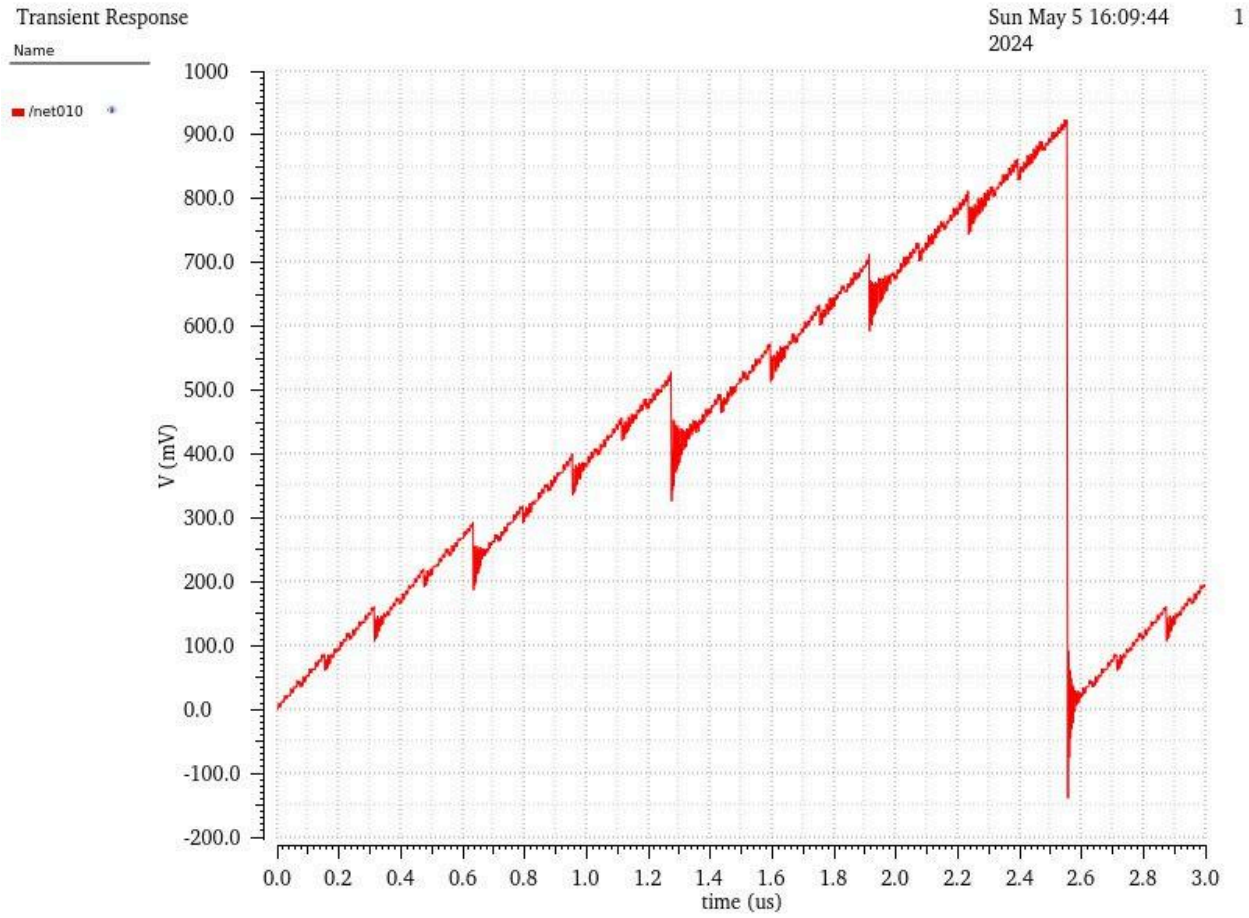
We put VSS as negative voltage since the range of output voltage starts to involve negative voltage, so a negative VSS would help keep Vout always at 0 or positive voltage.

Q4.2

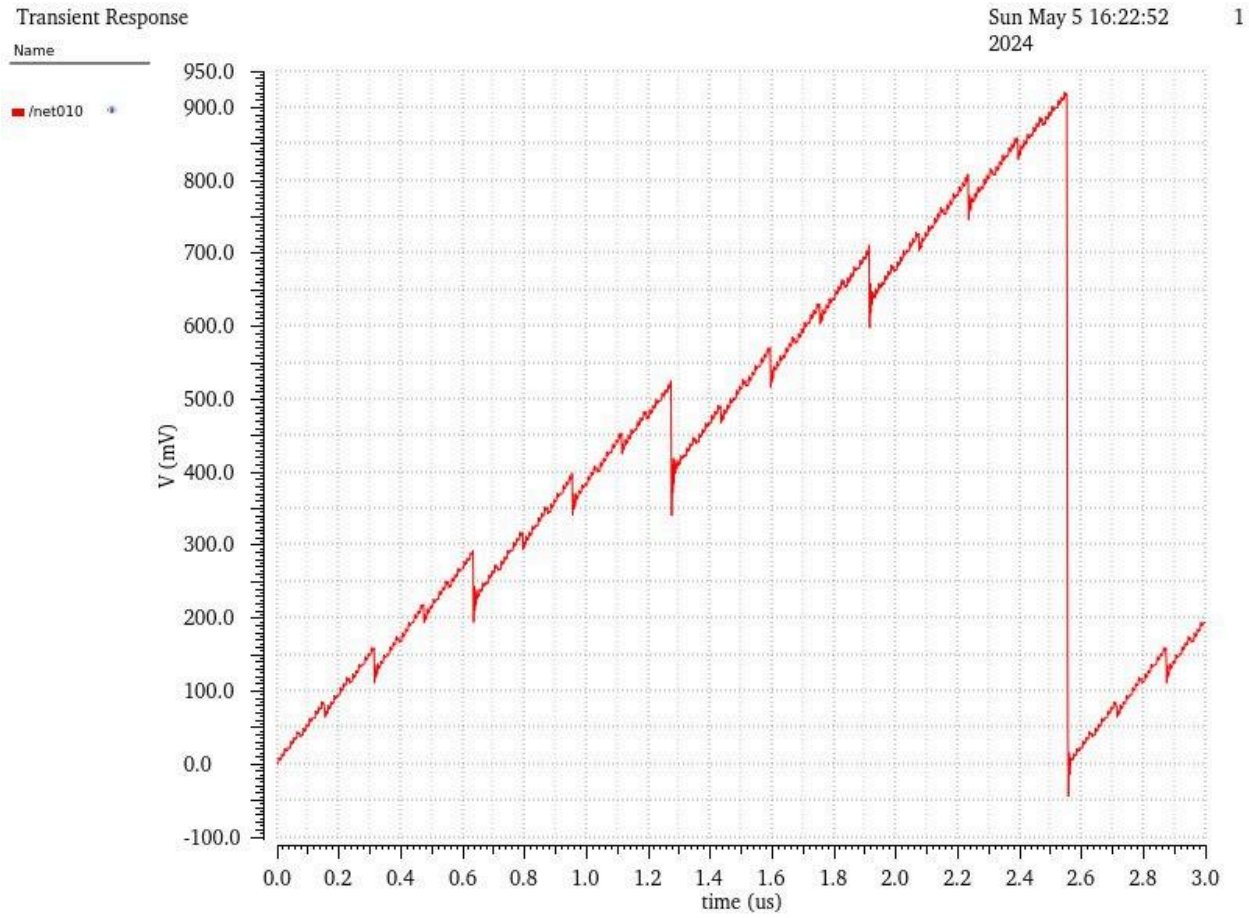
15k



10k


Transient Response
Sun May 5 16:09:44 2024
1
Name
/net010
1000
900.0
800.0
700.0
600.0
500.0
400.0
300.0
200.0
100.0
0.0
-100.0
-200.0
V (mV)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0
time (us)

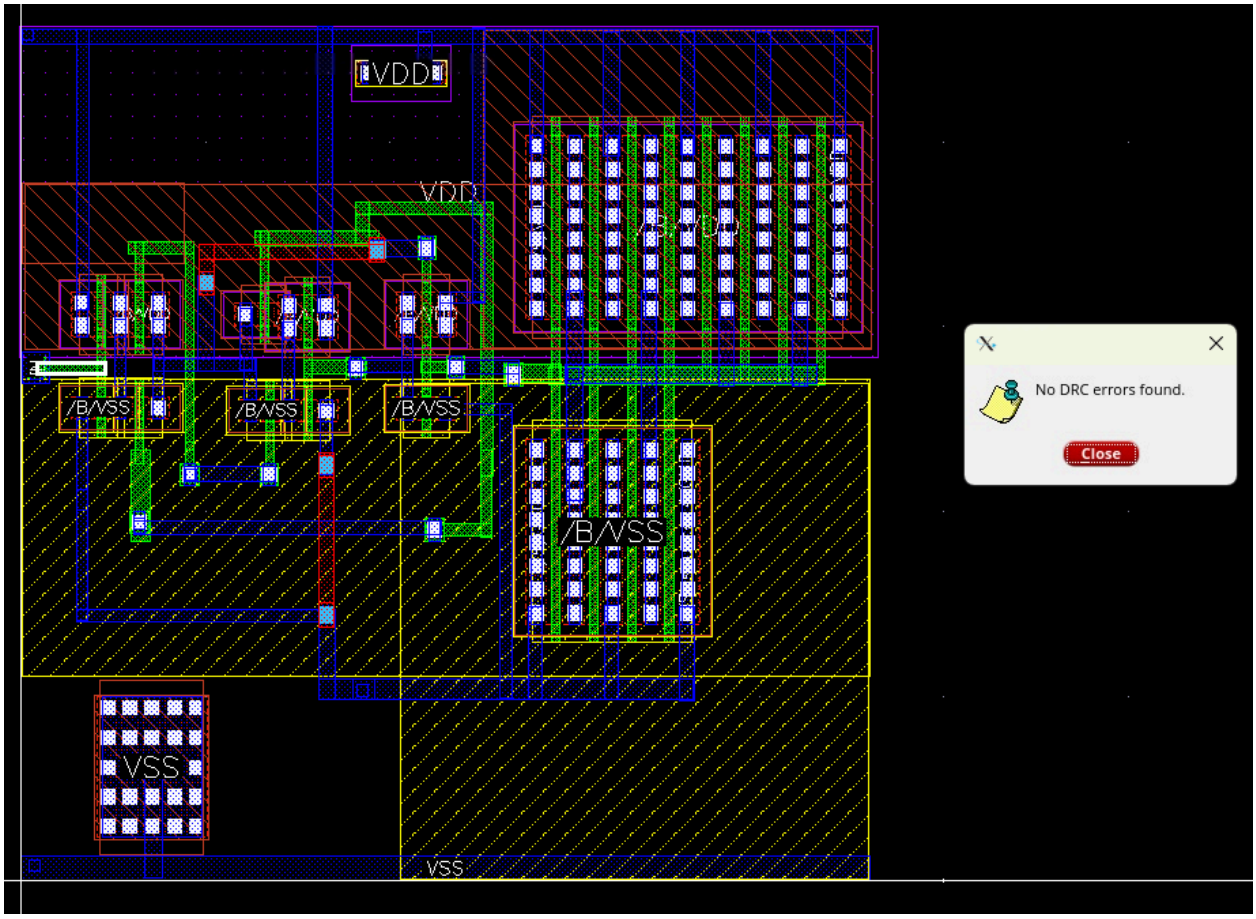
5k



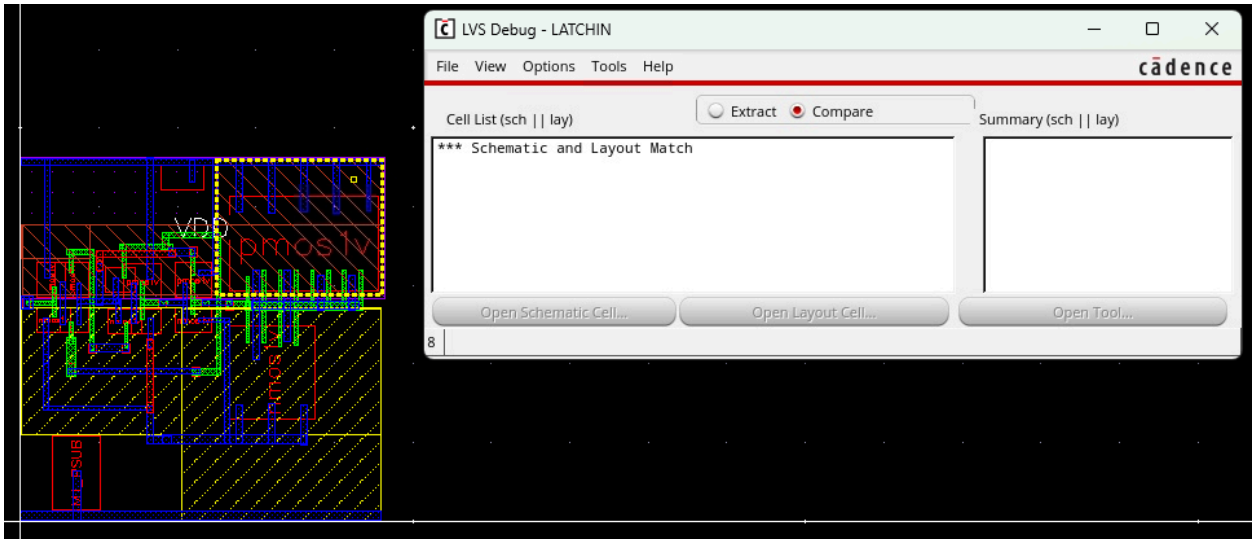
The main difference is that the voltage range of Vout conserved for this module at around 950mV, and the signal range gets more vivid, whereas for module 3, as the resistance got lower, so did the Vout voltage.

Q5

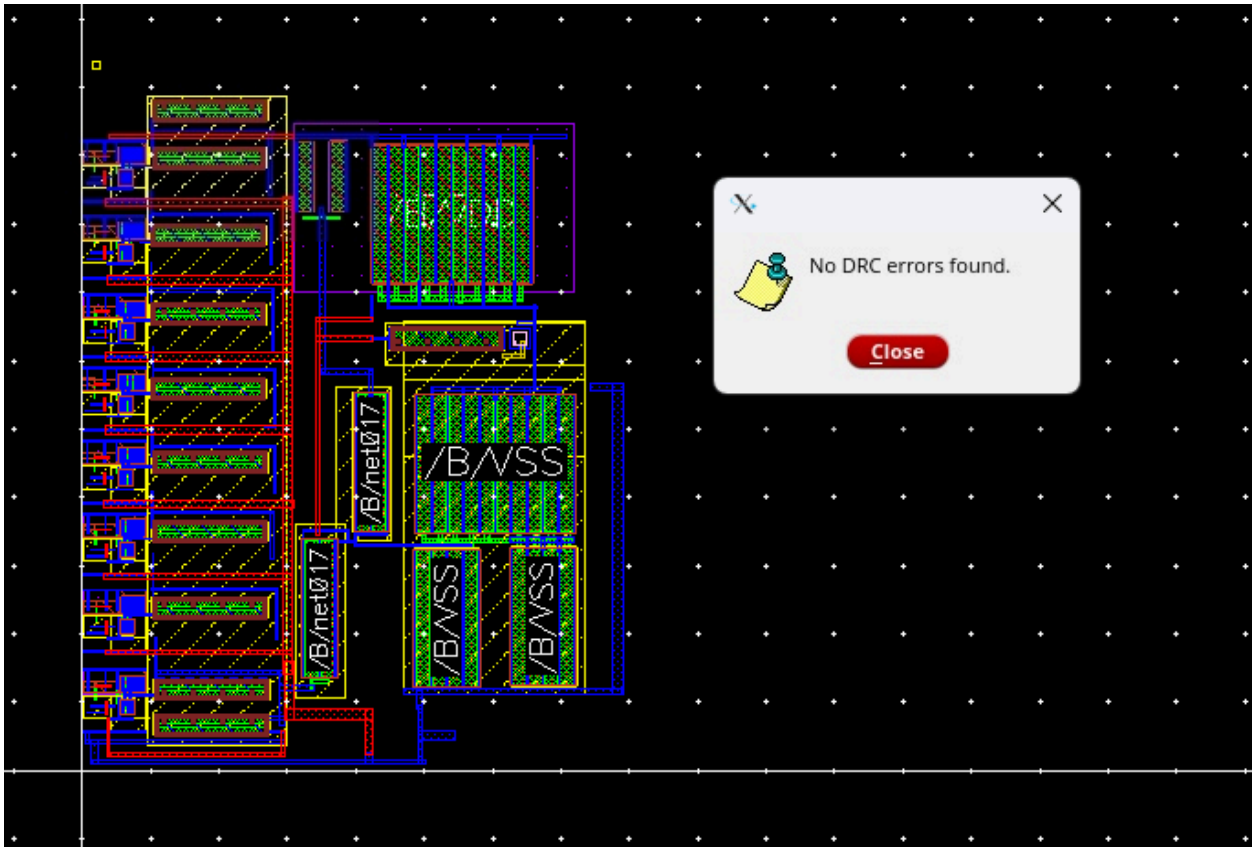
Latch DRC


VDD
VDD
/B/VSS
/B/VSS
/B/VSS
/B/VSS
VSS
VSS
No DRC errors found.
Close

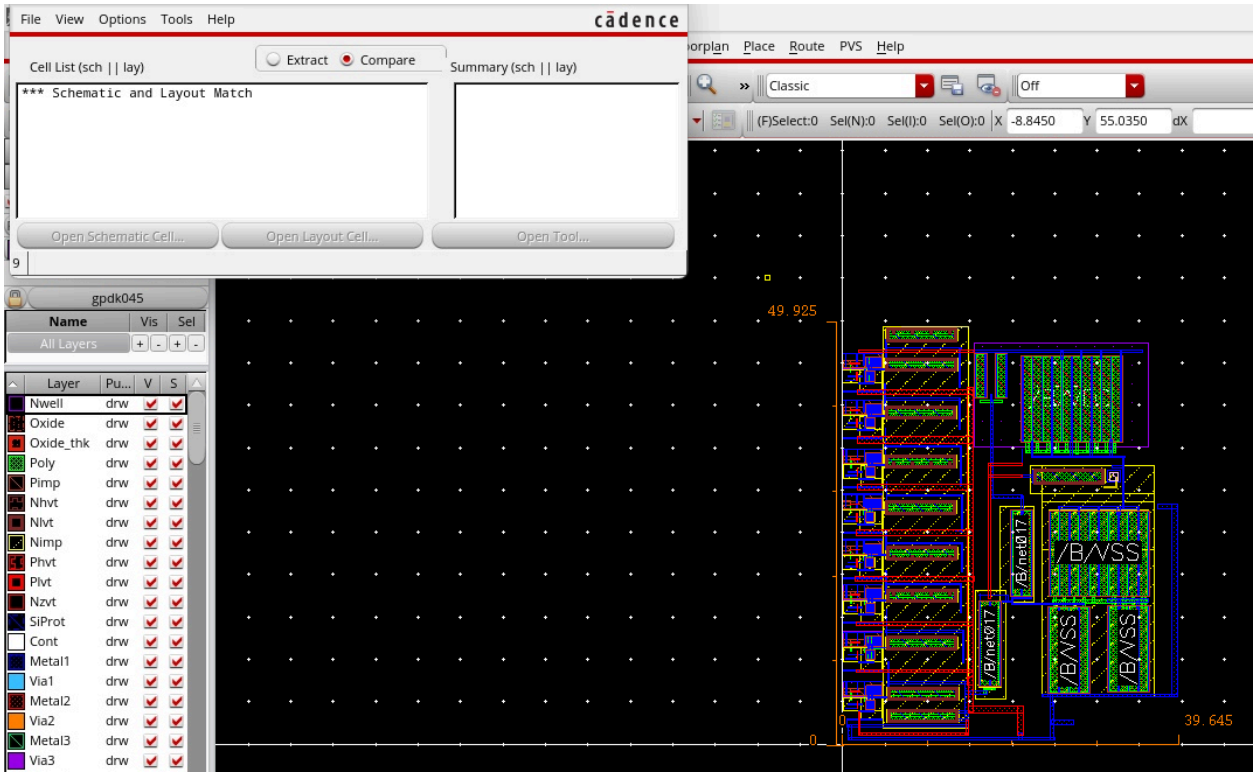
Latch LVS


LVS Debug - LATCHIN
File View Options Tools Help
cadence
Cell List (sch || lay)
Extract
Compare
Summary (sch || lay)
*** Schematic and Layout Match
Open Schematic Cell...
Open Layout Cell...
Open Tool...
8
VDD
pmos1v

DAC DRC



DAC LVS



Reflection:

Throughout the course, we went over several key concepts which laid down the foundation of microcontrollers. We initially went over the concept of NMOS/PMOS fets, and how they can form more complex circuits, as well as potential differences through triode and saturation. To dive deeper into the fundamentals of MOSFETS, we also went over small signal processing, along with more complex circuits involving MOSFETS such as inverters, the involvement of capacitance, and more. Eventually, we wrapped up the semester by going over how MOSFETs could become logic gates such as NAND and NOR, and combining our knowledge to form logic a logic DAC with a latch in the final project.

ECE 18320 1

MICROELECTC CIRCUITS

MARC DANDIN

Completed. Thank you!

Survey closes: **May 6 2024 11:59PM**