Assignment: Add a Power Optimization strategy and observe the changes in Schematic and Power

Use the HDL code mentioned in the Instruction tab and add Power Optimization strategy before placement in the Implementation to observe changes in the Synthesized Schematic and Implemented Schematic. Share the Report Power Snapshot of both Synthesize and Implemented design. Use necessary Clock XDC.

HDL Code for Assingment:

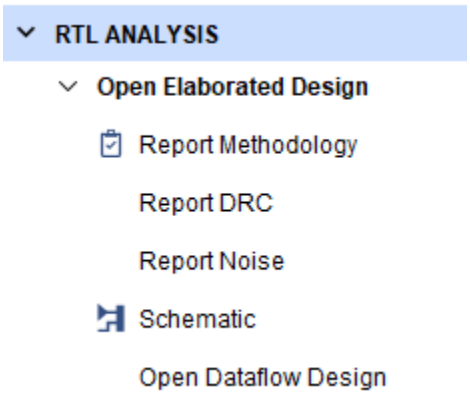
```
module single_port_sync_ram
  # (parameter ADDR_WIDTH = 4,
     parameter DATA_WIDTH = 32,
     parameter DEPTH = 16
    )

  (   input           clk,
      input [ADDR_WIDTH-1:0]  addr,
      inout [DATA_WIDTH-1:0]  data,
      input           cs,
      input           we,
      input           oe
  );

  reg [DATA_WIDTH-1:0]   tmp_data;
  reg [DATA_WIDTH-1:0]   mem [DEPTH-1:0];

  always @ (posedge clk) begin
    if (cs & we)
      mem[addr] <= data;
  end

  always @ (posedge clk) begin
    if (cs & !we)
      tmp_data <= mem[addr];
  end

  assign data = cs & oe & !we ? tmp_data : 'hz;
endmodule

```

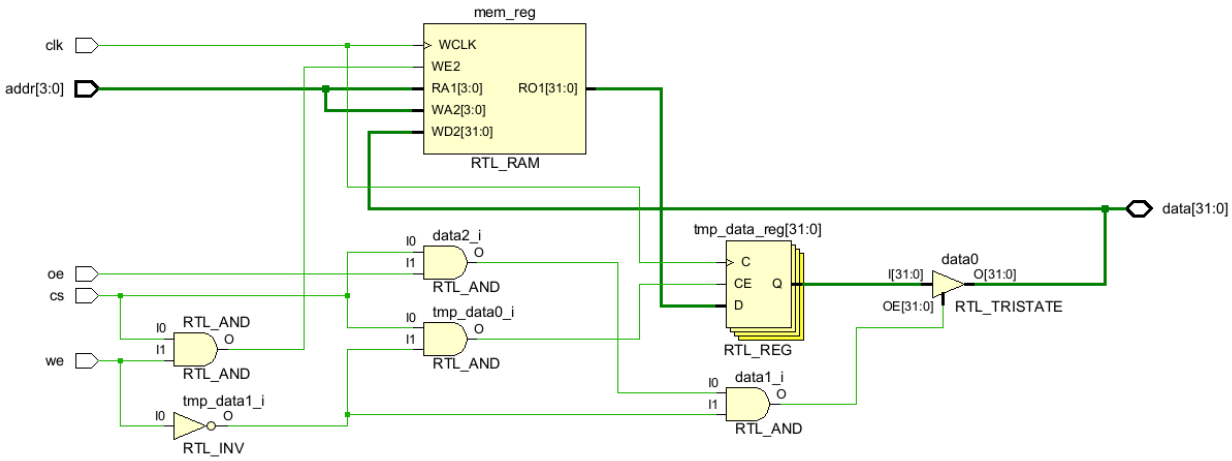
Clock Constraint:

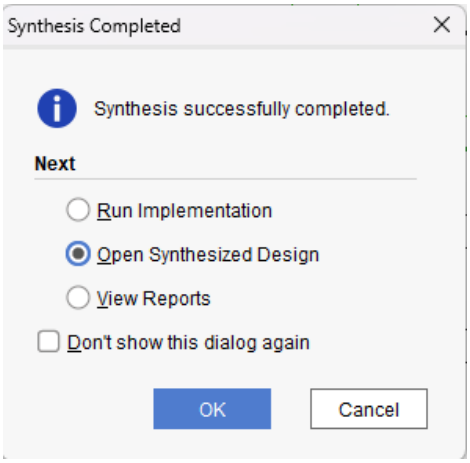
```
create_clock -period 10 -name clk [get_ports clk]
```

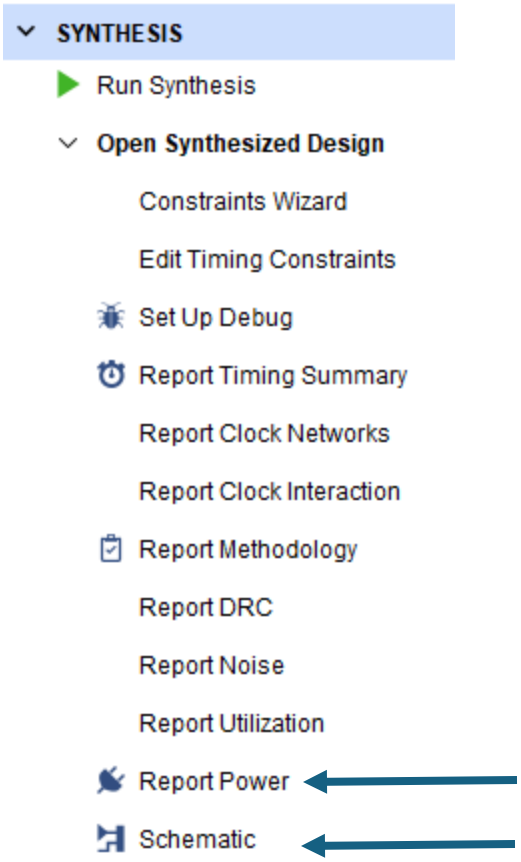
Questions for this assignment

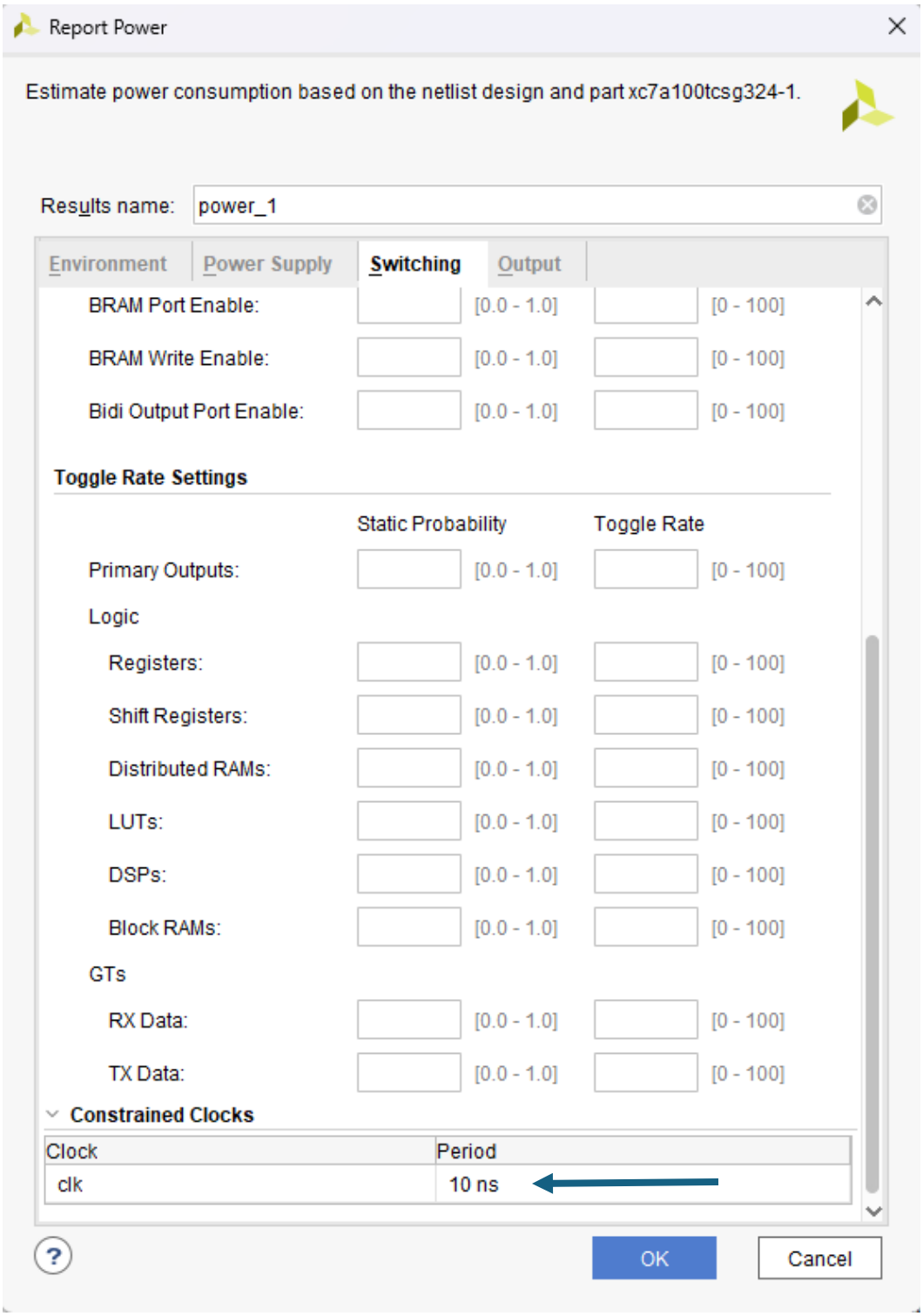
1. Understanding of the Implementation Strategies.

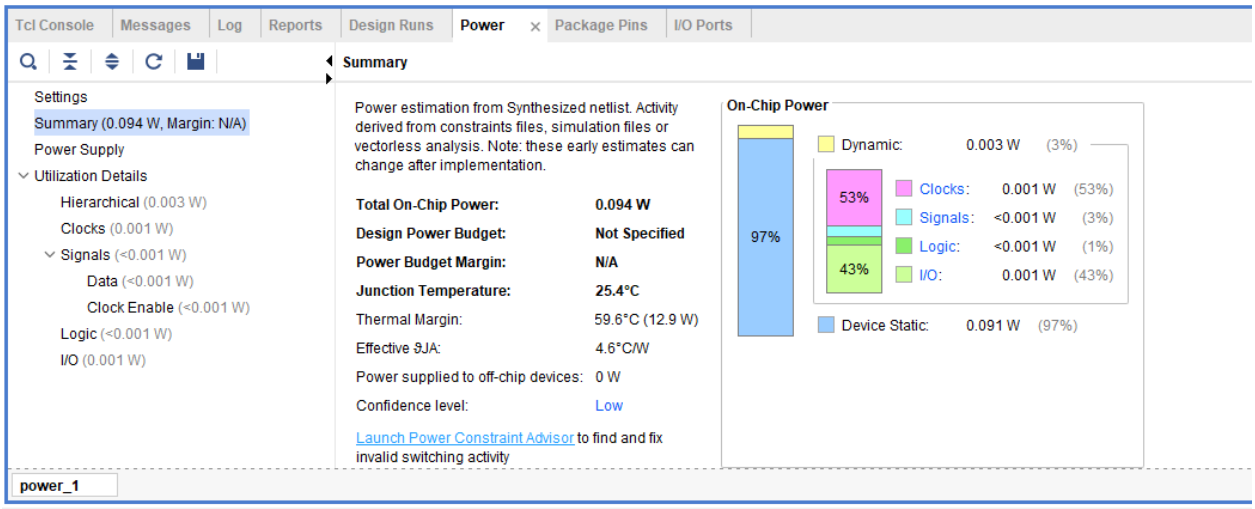




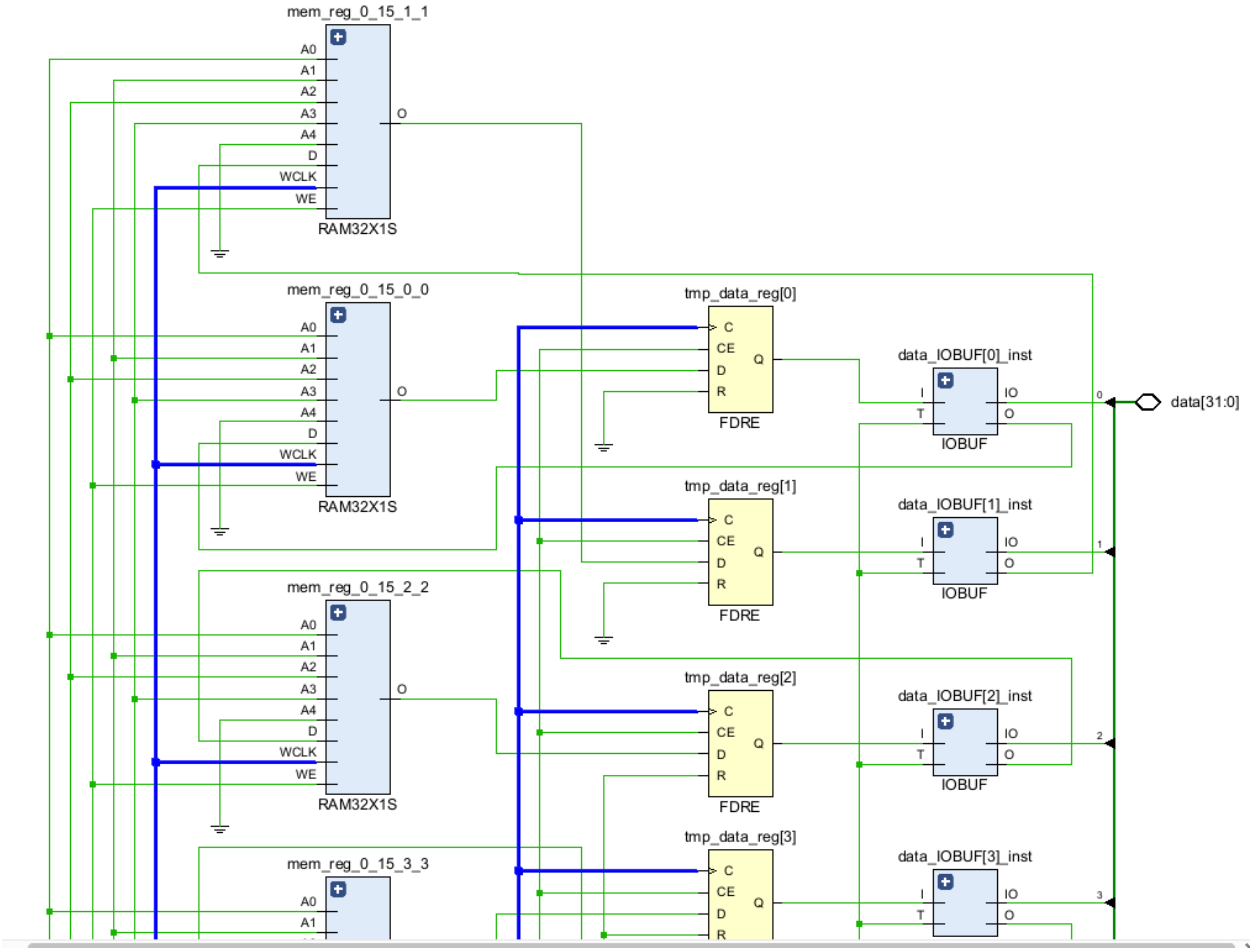


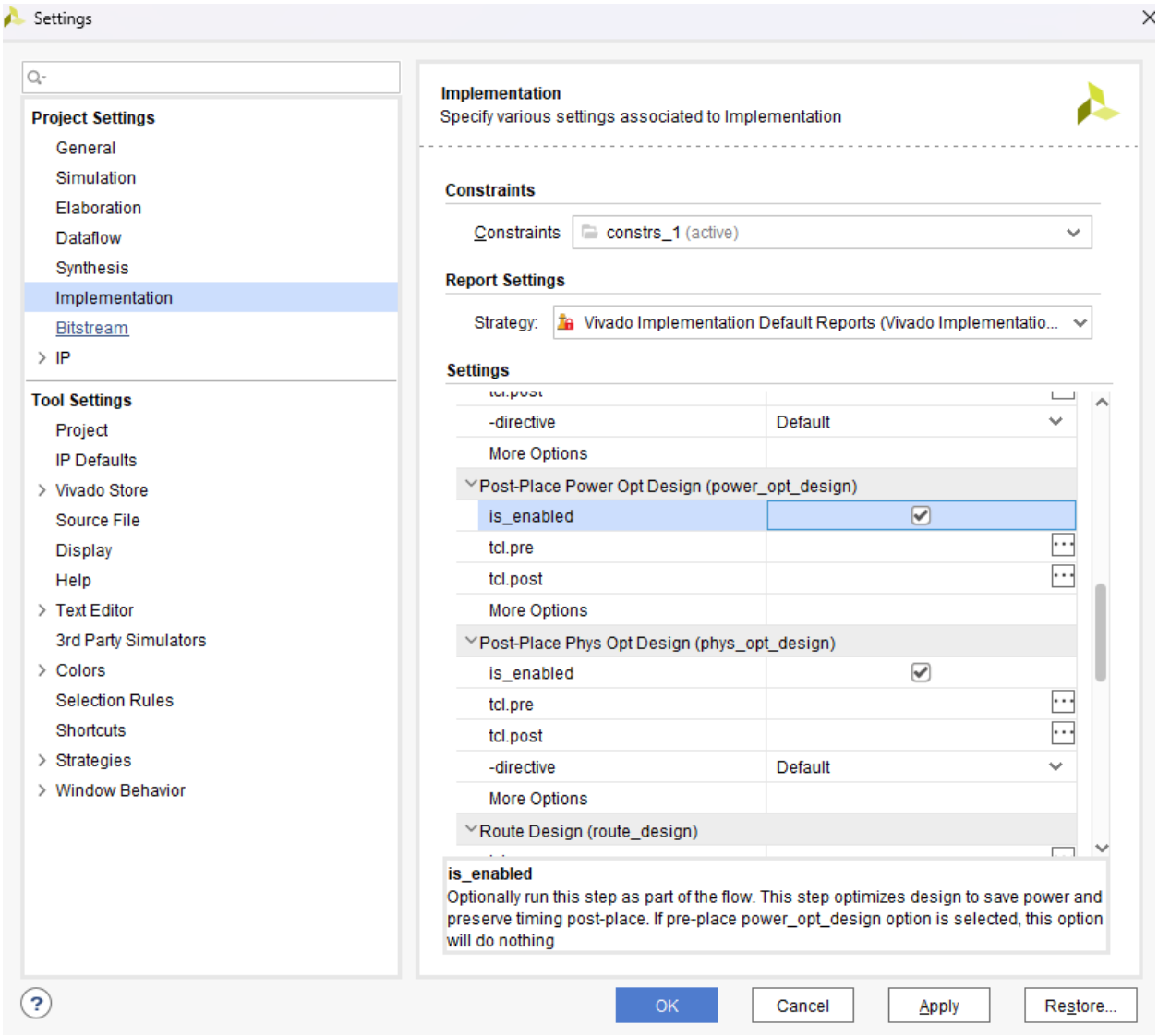

SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic

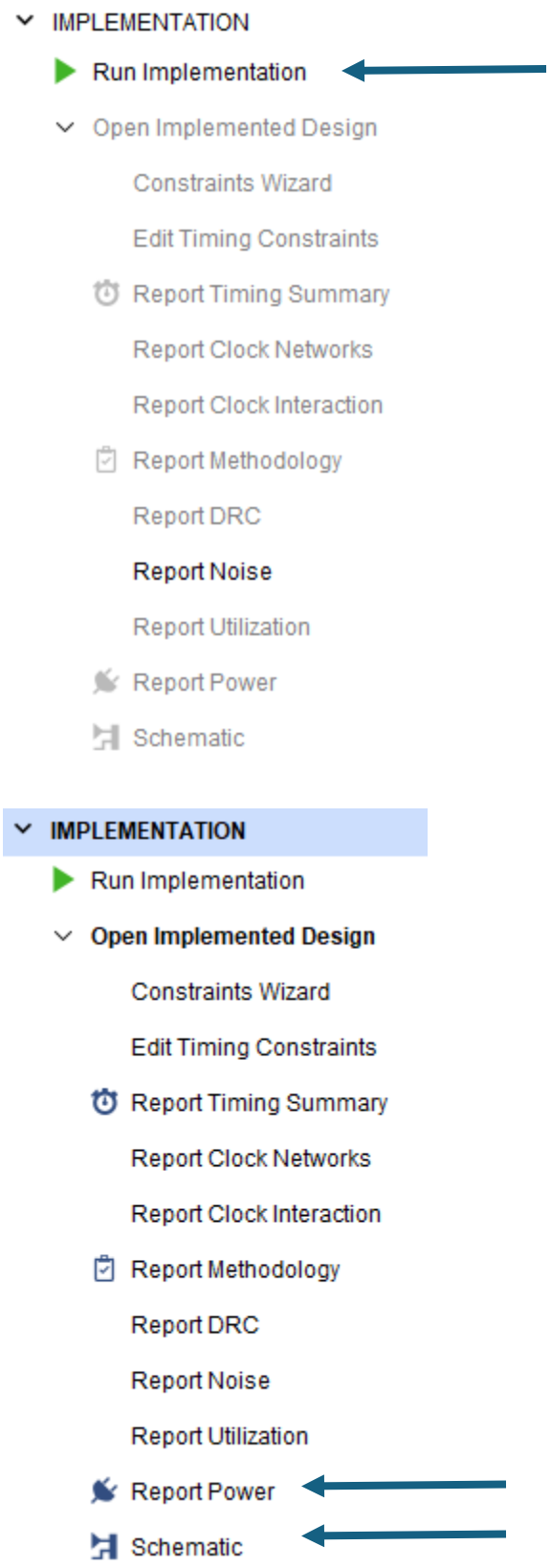

Report Power
Estimate power consumption based on the netlist design and part xc7a100tcsg324-1.
Results name:
power_1
Environment
Power Supply
Switching
Output
BRAM Port Enable:
[0.0 - 1.0]
[0 - 100]
BRAM Write Enable:
[0.0 - 1.0]
[0 - 100]
Bidi Output Port Enable:
[0.0 - 1.0]
[0 - 100]
Toggle Rate Settings
Static Probability
Toggle Rate
Primary Outputs:
[0.0 - 1.0]
[0 - 100]
Logic
Registers:
[0.0 - 1.0]
[0 - 100]
Shift Registers:
[0.0 - 1.0]
[0 - 100]
Distributed RAMs:
[0.0 - 1.0]
[0 - 100]
LUTs:
[0.0 - 1.0]
[0 - 100]
DSPs:
[0.0 - 1.0]
[0 - 100]
Block RAMs:
[0.0 - 1.0]
[0 - 100]
GTs
RX Data:
[0.0 - 1.0]
[0 - 100]
TX Data:
[0.0 - 1.0]
[0 - 100]
Constrained Clocks
Clock
Period
clk
10 ns
OK
Cancel



Most of the power draw is due to dynamic switching.




Settings
Project Settings
General
Simulation
Elaboration
Dataflow
Synthesis
Implementation
Bitstream
IP
Tool Settings
Project
IP Defaults
Vivado Store
Source File
Display
Help
Text Editor
3rd Party Simulators
Colors
Selection Rules
Shortcuts
Strategies
Window Behavior
Implementation
Specify various settings associated to Implementation
Constraints
Constraints
constrs_1 (active)
Report Settings
Strategy:
Vivado Implementation Default Reports (Vivado Implementatio...
Settings
-directive
Default
More Options
Post-Place Power Opt Design (power_opt_design)
is_enabled
tcl.pre
tcl.post
More Options
Post-Place Phys Opt Design (phys_opt_design)
is_enabled
tcl.pre
tcl.post
-directive
Default
More Options
Route Design (route_design)
is_enabled
Optionally run this step as part of the flow. This step optimizes design to save power and preserve timing post-place. If pre-place power_opt_design option is selected, this option will do nothing
OK
Cancel
Apply
Restore...


IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
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Report Clock Interaction
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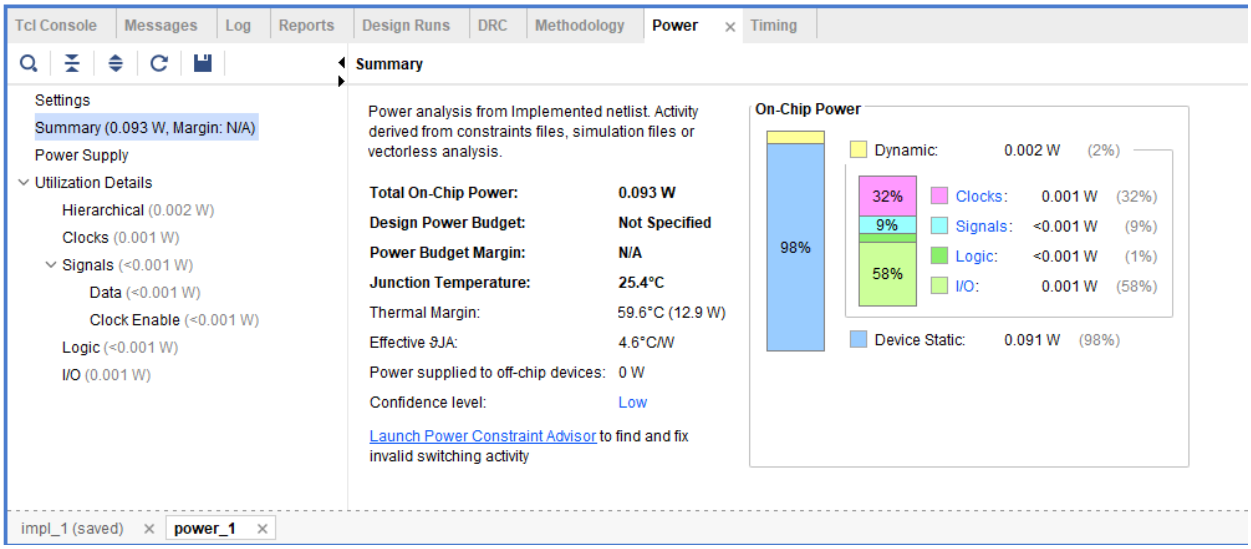
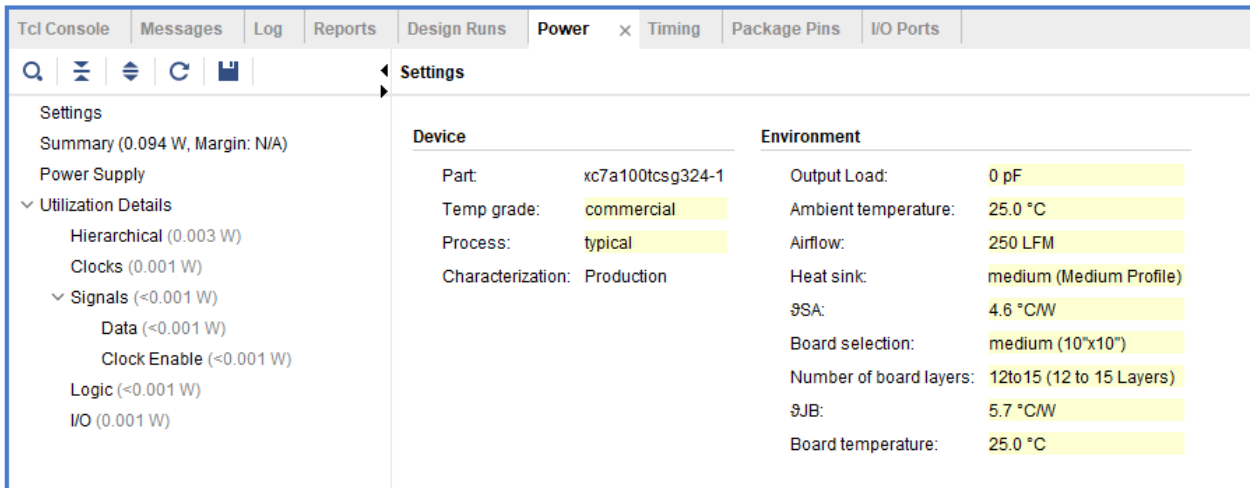


I did not observe much difference in power ~ .001W improvement. Schematic looks the same. The clock percentage did decrease a 19%. Device Static power percentage increased.

Report Power Snapshot (post-synth):



Report Power Snapshot (post-implementation) – After Optimization