

Assignment: Add a Power Optimization strategy and observe the changes in Schematic and Power

Use the HDL code mentioned in the Instruction tab and add Power Optimization strategy before placement in the Implementation to observe changes in the Synthesized Schematic and Implemented Schematic. Share the Report Power Snapshot of both Synthesize and Implemented design. Use necessary Clock XDC.

HDL Code for Assingment:

```
1  module single_port_sync_ram
2    # (parameter ADDR_WIDTH = 4,
3      parameter DATA_WIDTH = 32,
4      parameter DEPTH = 16
5    )
6
7    (  input          clk,
8      input [ADDR_WIDTH-1:0]  addr,
9      inout [DATA_WIDTH-1:0]  data,
10     input          cs,
11     input          we,
12     input          oe
13   );
14
15   reg [DATA_WIDTH-1:0]  tmp_data;
16   reg [DATA_WIDTH-1:0]  mem [DEPTH-1:0];
17
18   always @ (posedge clk) begin
19     if (cs & we)
20       mem[addr] <= data;
21   end
22
23   always @ (posedge clk) begin
24     if (cs & !we)
25       tmp_data <= mem[addr];
26   end
27
28   assign data = cs & oe & !we ? tmp_data : 'hz;
29 endmodule
30
```

Clock Constraint:

```
create_clock -period 10 -name clk [get_ports clk]
```

Questions for this assignment

1. Understanding of the Implementation Strategies.

▼ RTL ANALYSIS

▼ Open Elaborated Design

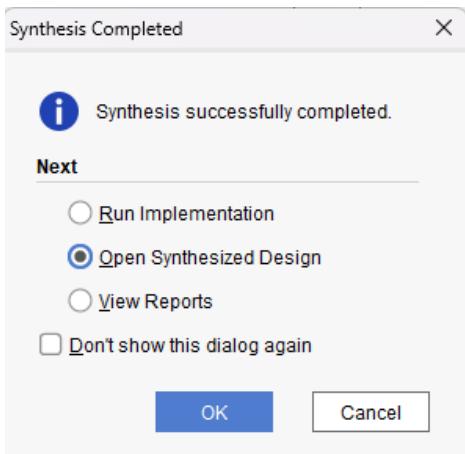
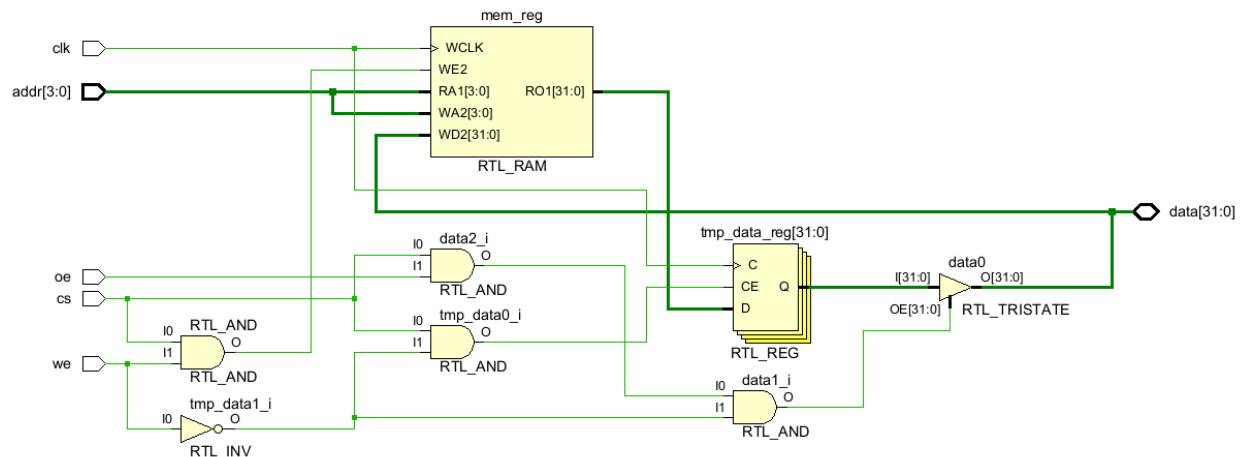
Report Methodology

Report DRC

Report Noise

 Schematic

Open Dataflow Design



▼ **SYNTHESIS**

▶ Run Synthesis

▼ Open Synthesized Design

 Constraints Wizard

 Edit Timing Constraints

 🐞 Set Up Debug

 ⌚ Report Timing Summary

 Report Clock Networks

 Report Clock Interaction

 📋 Report Methodology

 Report DRC

 Report Noise

 Report Utilization

 ⚡ Report Power 

 ↳ Schematic 

Report Power

Estimate power consumption based on the netlist design and part xc7a100tcszg324-1.

Results name: ×

Environment	Power Supply	Switching	Output
BRAM Port Enable:	<input type="text"/>	[0.0 - 1.0]	<input type="text"/> [0 - 100]
BRAM Write Enable:	<input type="text"/>	[0.0 - 1.0]	<input type="text"/> [0 - 100]
Bidi Output Port Enable:	<input type="text"/>	[0.0 - 1.0]	<input type="text"/> [0 - 100]

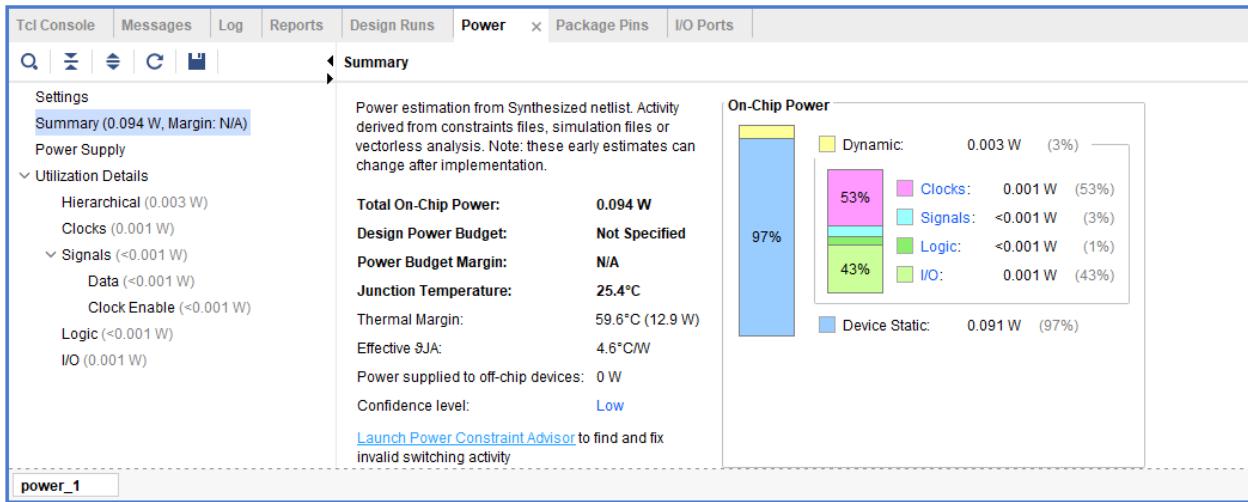
Toggle Rate Settings

	Static Probability	Toggle Rate
Primary Outputs:	<input type="text"/> [0.0 - 1.0]	<input type="text"/> [0 - 100]
Logic		
Registers:	<input type="text"/> [0.0 - 1.0]	<input type="text"/> [0 - 100]
Shift Registers:	<input type="text"/> [0.0 - 1.0]	<input type="text"/> [0 - 100]
Distributed RAMs:	<input type="text"/> [0.0 - 1.0]	<input type="text"/> [0 - 100]
LUTs:	<input type="text"/> [0.0 - 1.0]	<input type="text"/> [0 - 100]
DSPs:	<input type="text"/> [0.0 - 1.0]	<input type="text"/> [0 - 100]
Block RAMs:	<input type="text"/> [0.0 - 1.0]	<input type="text"/> [0 - 100]
GTs		
RX Data:	<input type="text"/> [0.0 - 1.0]	<input type="text"/> [0 - 100]
TX Data:	<input type="text"/> [0.0 - 1.0]	<input type="text"/> [0 - 100]

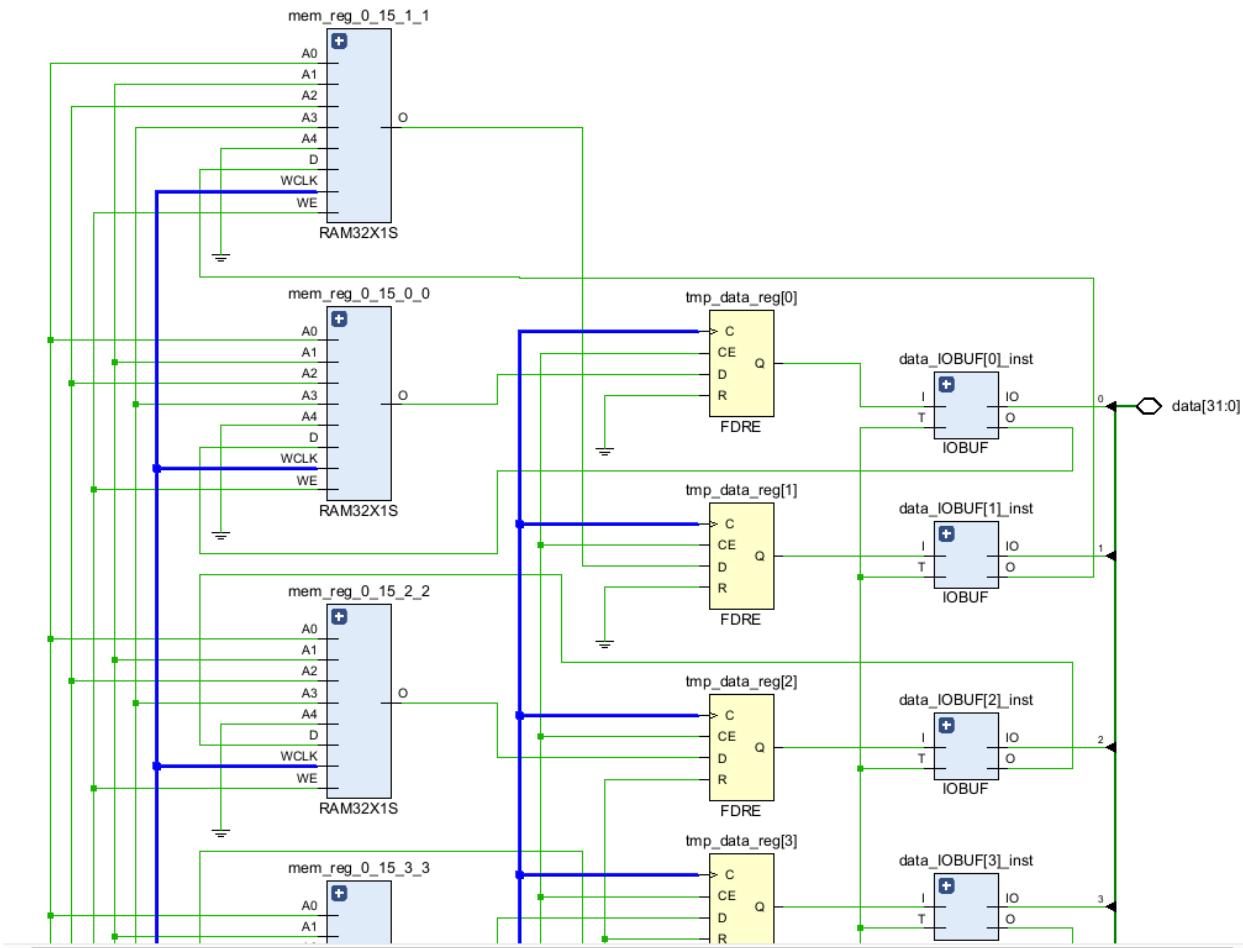
Constrained Clocks

Clock	Period
clk	10 ns ←

? OK Cancel



Most of the power draw is due to dynamic switching.



Settings

Project Settings

- General
- Simulation
- Elaboration
- Dataflow
- Synthesis
- Implementation
- Bitstream

Tool Settings

- Project
- IP Defaults
- Vivado Store
- Source File
- Display
- Help
- Text Editor
- 3rd Party Simulators
- Colors
- Selection Rules
- Shortcuts
- Strategies
- Window Behavior

Implementation

Specify various settings associated to Implementation

Constraints

Constraints: constrs_1 (active)

Report Settings

Strategy: Vivado Implementation Default Reports (Vivado Implementation Default Reports)

Settings

-directive	Default	...
More Options		
Post-Place Power Opt Design (power_opt_design)		
is_enabled	<input checked="" type="checkbox"/>	...
tcl.pre		...
tcl.post		...
More Options		
Post-Place Phys Opt Design (phys_opt_design)		
is_enabled	<input checked="" type="checkbox"/>	...
tcl.pre		...
tcl.post		...
-directive	Default	...
More Options		
Route Design (route_design)		
is_enabled		

Optional note: Optionally run this step as part of the flow. This step optimizes design to save power and preserve timing post-place. If pre-place power_opt_design option is selected, this option will do nothing.

OK Cancel Apply Restore...

▼ IMPLEMENTATION

▶ Run Implementation 

▼ Open Implemented Design

Constraints Wizard

Edit Timing Constraints

⌚ Report Timing Summary

Report Clock Networks

Report Clock Interaction

Report Methodology

Report DRC

Report Noise

Report Utilization

⚡ Report Power

↳ Schematic

▼ IMPLEMENTATION

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Constraints Wizard

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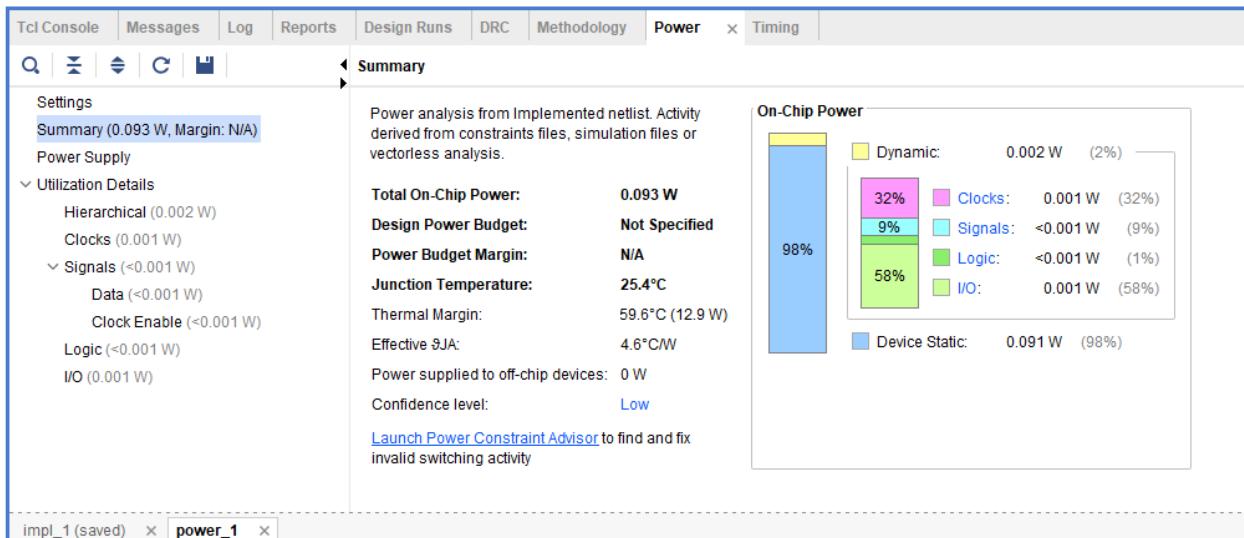
Report DRC

Report Noise

Report Utilization

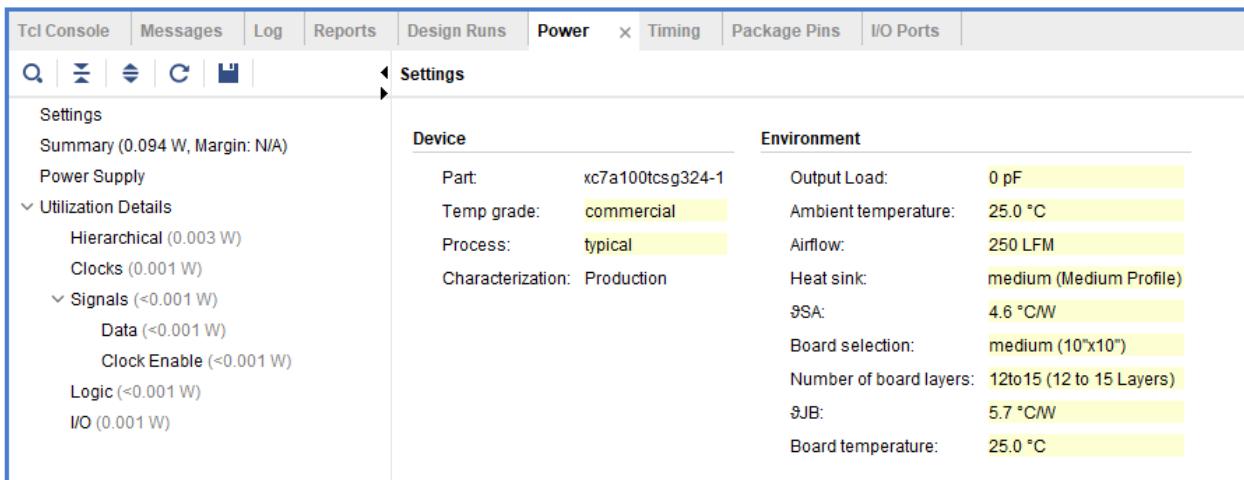
⚡ Report Power 

↳ Schematic 



I did not observe much difference in power ~.001W improvement. Schematic looks the same. The clock percentage did decrease a 19%. Device Static power percentage increased.

Report Power Snapshot (post-synth):



Report Power Snapshot (post-implementation) – After Optimization

Tcl Console | Messages | Log | Reports | Design Runs | DRC | Methodology | **Power** | × | Timing |

Q | | | | | |

◀ **Settings**

Settings

Summary (0.093 W, Margin: N/A)

Power Supply

Utilization Details

- Hierarchical (0.002 W)
- Clocks (0.001 W)
- Signals (<0.001 W)
 - Data (<0.001 W)
 - Clock Enable (<0.001 W)
- Logic (<0.001 W)
- I/O (0.001 W)

Device

Device	Environment
Part: xc7a100tcsg324-1	Output Load: 0 pF
Temp grade: commercial	Ambient temperature: 25.0 °C
Process: typical	Airflow: 250 LFM
Characterization: Production	Heat sink: medium (Medium Profile)
	θ _{SA} : 4.6 °C/W
	Board selection: medium (10"x10")
	Number of board layers: 12to15 (12 to 15 Layers)
	θ _{JB} : 5.7 °C/W
	Board temperature: 25.0 °C

impl_1 (saved) × power_1 × power_2 × |