Embedded Systems Design Laboratory

VHDL Programming Assignment: RAM128_32

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Platform: Intel Quartus + ModelSim (Starter Edition 2021.1)
Course: VHDL Design & Simulation – Week 2 Assignment
Result: Passed – 10/10 Points

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1. Objective

The goal of this laboratory exercise is to design and verify a 128×32-bit single-port RAM in VHDL. The design must implement a synchronous write and asynchronous read mechanism, with the output (q) remaining unregistered. The implementation should pass the provided testbench (AAC2M2P2_tb.vhdp) and produce the correct simulation output file (myvectorh.out).

2. Design Specifications

Signal	Direction	Width	Description
address	IN	7 bits	Memory address (0–127)
clock	IN	1 bit	Synchronous clock input
data	IN	32 bits	Input data to be written to memory
wren	IN	1 bit	Write enable control signal
q	OUT	32 bits	Asynchronous output data

3. VHDL Source Code

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity RAM128_32 is
  port (
    address : in  std_logic_vector(6 downto 0);
    clock   : in  std_logic := '1';
    data    : in  std_logic_vector(31 downto 0);
    wren    : in  std_logic;
    q       : out std_logic_vector(31 downto 0)
  );
end RAM128_32;

architecture behavior of RAM128_32 is
  type ram_type is array (0 to 127) of std_logic_vector(31 downto 0);
  signal ram : ram_type;
  signal addr_reg : natural range 0 to 127;
begin
  addr_reg <= to_integer(unsigned(address));

  process(clock)
  begin
    if rising_edge(clock) then
      if wren = '1' then
        ram(addr_reg) <= data;
      end if;
    end if;
```

```
  end process;

  q <= ram(addr_reg);
end behavior;
```

4. Simulation Procedure

The simulation was conducted using ModelSim Intel FPGA Starter Edition 2021.1. The following TCL commands were executed in the transcript window to compile and simulate the design:

```
vlib work
vmap work work
vcom AAC2M2P2.vhd
vcom AAC2M2P2_tb.vhdp
vsim work.aac2m2p2_tb
add wave sim:/aac2m2p2_tb/*
run 15us
```

Upon running the simulation, the waveform confirmed proper synchronous writes and instantaneous asynchronous reads. The auto-grader verified functional correctness and produced a perfect score.

Figure 1: ModelSim simulation waveform showing address, clock, wren, data, and q signals.

5. Verification and Results

All functional tests passed successfully. The output file (myvectorh.out) matched the reference vectorh.out exactly.

Key Results:
• Asynchronous read verified – output q updates immediately upon address change.
• Synchronous write verified – memory updates on rising edge when wren='1'.
• No output latching when wren=0 – confirmed by waveform and testbench output.
• Autograder score: 10/10 – Passed.

6. Conclusion

This lab successfully demonstrates the implementation and verification of a 128×32 single-port RAM module in VHDL. The design adheres to industry-standard synchronous write and asynchronous read principles. All tests confirmed compliance with the assignment specification, achieving full credit.