Final Evaluation

Common Emitter BJT Amplifier

A report submitted to the

Department of Electrical and Information Engineering

Faculty of Engineering

University of Ruhuna

Sri Lanka

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In completing the final report for the
module
EE4105/ECE4152 Electronics Project
By

Group 59

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ABSTRACT

This report briefly describes a few real-world applications in addition to focusing on the essential features of common emitter BJT amplifiers. The Common Emitter BJT Amplifier design method is covered in this study. The introduction, computations, implementation, and Proteus-based computer simulations are all included in this project.

PREFACE

The final assessment for the Electronic Project module (EE4105) is contained in this project report. We have designed a common emitter BJT amplifier for our assessment. While preparing this study, we got the chance to conduct extensive research on the BJT amplifier and its applications in industry. With three people in the group, we constructed a Common Emitter BJT amplifier with the given specs. We covered amplifier design, discussion, and circuit implementation in this study. The project covers the basic results of the module and entails creating a common emitter BJT amplifier. Utilizing the foundational knowledge from this module as well as that from EE2202 Introduction to Electronic Engineering and EE3301 Analog Electronics, the project was finished. To learn more, books and the Internet were examined.

We are grateful to G.C.W. Thilakarathne, Lecturer, Electrical and Information Engineering Department, Faculty of Engineering, for his guidance in getting the project completed.

01. INTRODUCTION

1.1. INTRODUCTION

One form of bipolar junction transistor (BJT) amplifier that is frequently used to amplify tiny signals is the common emitter amplifier circuit. Since both the input and output signals share the same emitter terminal, this type of amplifier is referred to as a "common emitter".

Signals in the few millivolts to few volts range are usually amplified using the common emitter amplifier circuit. Depending on the type of BJT being used and the circuit arrangement, it can yield power, voltage, and current gains.
Three components make up the common emitter amplifier circuit: a load resistor, a DC power source, and a BJT. The BJT's emitter terminal is connected to the ground, and the base terminal receives the input signal.

The collector terminal, which is attached to the load resistor, provides the output signal. High voltage gain and an excellent common-mode rejection ratio are two characteristics of the common emitter amplifier circuit (CMRR). It is a well-liked option for many applications since it is also reasonably simple to design and construct. It does, however, have several drawbacks, such as a propensity to generate appreciable harmonic distortion.

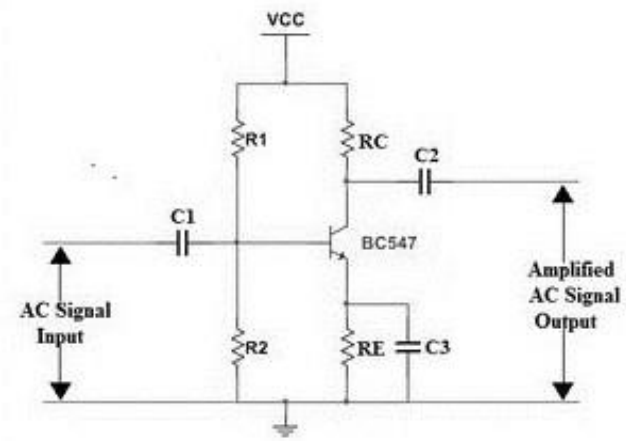

FIGURE 1: CIRCUIT DIAGRAM FOR COMMON EMITTER AMPLIFIER

The voltage divider bias and coupling capacitors C1 and C2 at the input and output, along with a bypass capacitor C3 connected from the emitter to the ground, are all part of the circuit for the common emitter amplifier. Capacitor C1 isolates the AC signals from the DC biasing voltage and permits the input signal to be fed into the amplifier.

1.2. OPERATION OF COMMON EMITTER BJT AMPLIFIER

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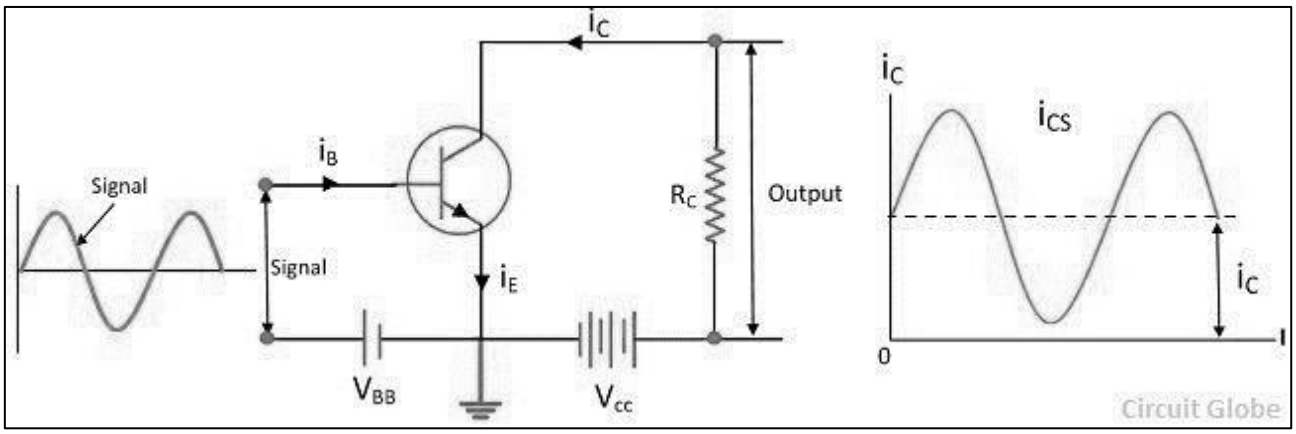


FIGURE 2: OPERATION OF COMMON EMITTER AMPLIFIER

1.3. APPLICATION OF COMMON EMITTER BJT AMPLIFIER

- Because of their strong voltage gain and decent CMRR, they are used in audio applications including speaker and headphone amplifiers.
- To magnify signals in the range of a few kilohertz to a few gigahertz in radio frequency applications, such as transmitters and receivers.
- Small signals from sensors and other sources are amplified by instrumentation amplifiers, which reject common-mode noise and interference.
- Boost weak signals with low noise figures in low-noise amplifier (LNA) circuits. To drive loads like speakers and motors and amplify strong signals.

1.4. PROBLEM STATEMENT

Our task is to design a common emitter bipolar junction transistor (BJT) amplifier that meets the specified requirements.

Voltage gain = 385

Bandwidth of low pass filter = 6MHz

1.5. OBJECTIVES

- Research BJT attributes and learn the fundamentals of CE configuration. Choose a task that has enough bandwidth to finish the assigned work.
- Determine component values with reduced error.
- Use Proteus software to simulate the circuit. o Build the circuit utilizing conventional PCB circuit design methods.
- Show off the finished circuit with the highest level of output precision.

1.6. METHODOLOGY

1. Study about CE amplifier circuits of BJT.
2. Calculate values of components according to the task
3. Provide proper assumptions.
4. Create Proteus design using calculated component values.
5. Observe the frequency response curve and get the required observations.
6. Implement the final PCB design.

02. DESIGN OF THE AMPLIFIER

1.7. REQUIRED COMPONENTS

- Transistor
  - BC547BP
  - 2N3904
- Resistors
  - 1.2 kΩ
  - 1 kΩ
  - 4.7 kΩ
  - 5.6 kΩ
  - 6.8 kΩ
  - 2.2 kΩ
  - 100 kΩ
  - 220 kΩ
- Capacitors
  - 1 µF
  - 22 µF
  - 3.3 pF
  - 2.2 pF
  - 100 µF
  - 4.7 µF
  - 4 pF

1.8. MATHEMATICAL CALCULATIONS

The circuit was first designed without buffer circuits, however even with Proteus simulation, it was difficult to get the necessary results. Therefore, in order to prevent impedance mismatches and obtain a better output, we have chosen to use two buffer circuits. (Here we used Common Collector 2N3904 Transistor with gain = 1 and bandwidth >> 6 MHz, for input)

1.1. BUFFER CIRCUITS (Input and output buffers)

Calculations are same for the both buffer circuits.

- Decided input voltage = 24V

Large possible output swing $= \frac{1}{2} V_{cc}$
$= 12V$

Gain of Transistors (β) = 100

The Q point used $V_{CE} = 10V$

$I_C = 6mA$

Assume that $I_C \approx I_E$

$$V_E = V_{cc} - V_{CE}$$

$$V_E = 24 - 10 = 14V$$

- Finding R_E,

$$R_E = \frac{V_E}{I_E}$$

$$R_E = \frac{14}{6} \approx 2.2k\Omega$$

- Finding R_1 and R_2, (Base voltage)

$$V_E = V_B - V_{BE}$$

$$V_B = 14 + 0.7 = 14.7V$$

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

$$14.7 = \frac{24 \times R_2}{R_1 + R_2}$$

$$\frac{R_1}{R_2} = \frac{31}{49}$$

Hence taking suitable values for R1 and R2

R1 = 5.6 kΩ

R2 = 6.8 kΩ

- Input impedance of the buffer

$$Z_{IN} = R_1//R_2//[\beta R_E + (1+\beta)R_E]$$

Here $r_E << R_E$

$$Z_{IN} = R_1//R_2//[\beta R_E]$$

$$Z_{IN} = 5600//6800//[100 \times 2200]$$

$$Z_{IN} = 3028.69\Omega$$

- To get a lower cutoff frequency around 10Hz,

$$C_2 = \frac{1}{2\pi \times 10 \times 3028.69}$$

$$C_2 = 5.2549\ \mu F \approx 4.7\mu F$$

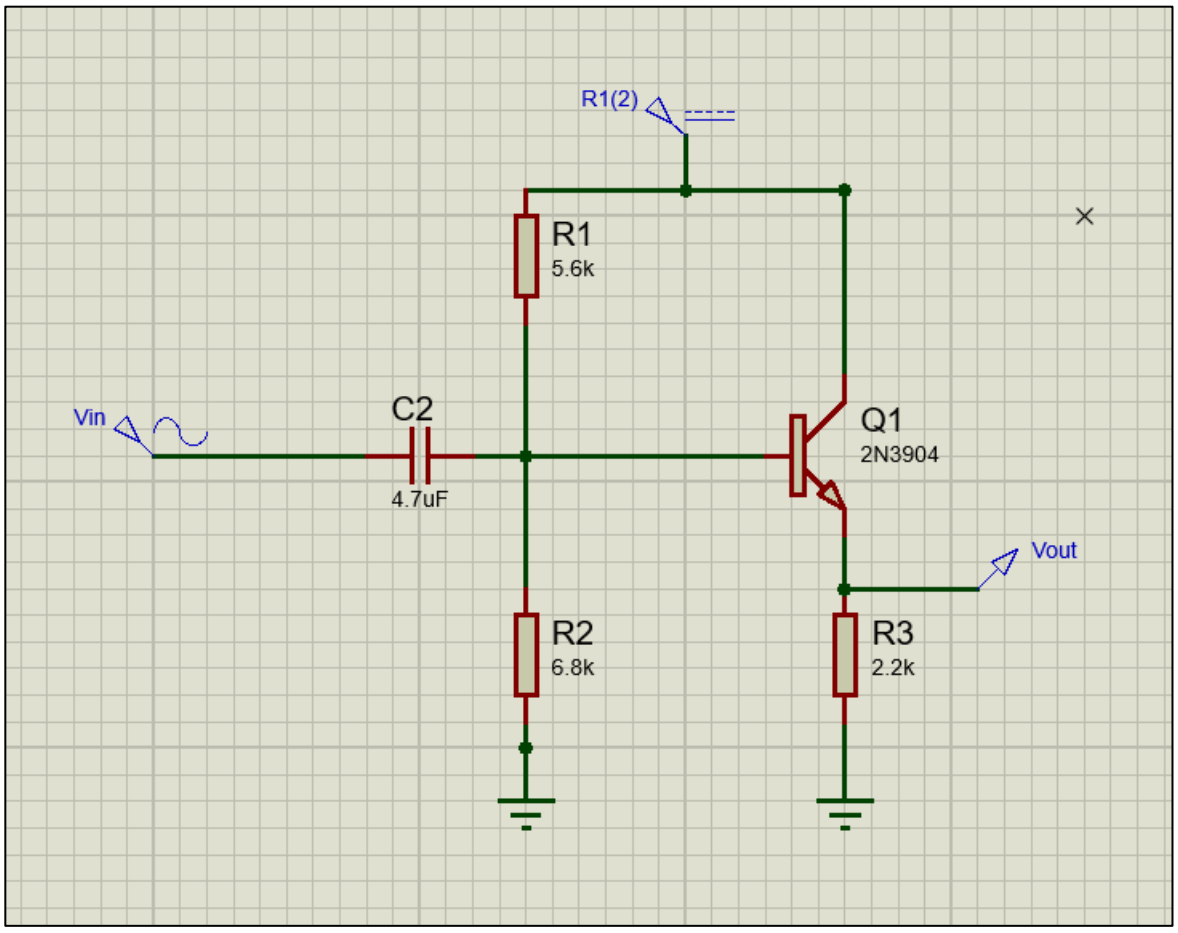


FIGURE 1 : INPUT BUFFER COMPLETE CIRCUIT

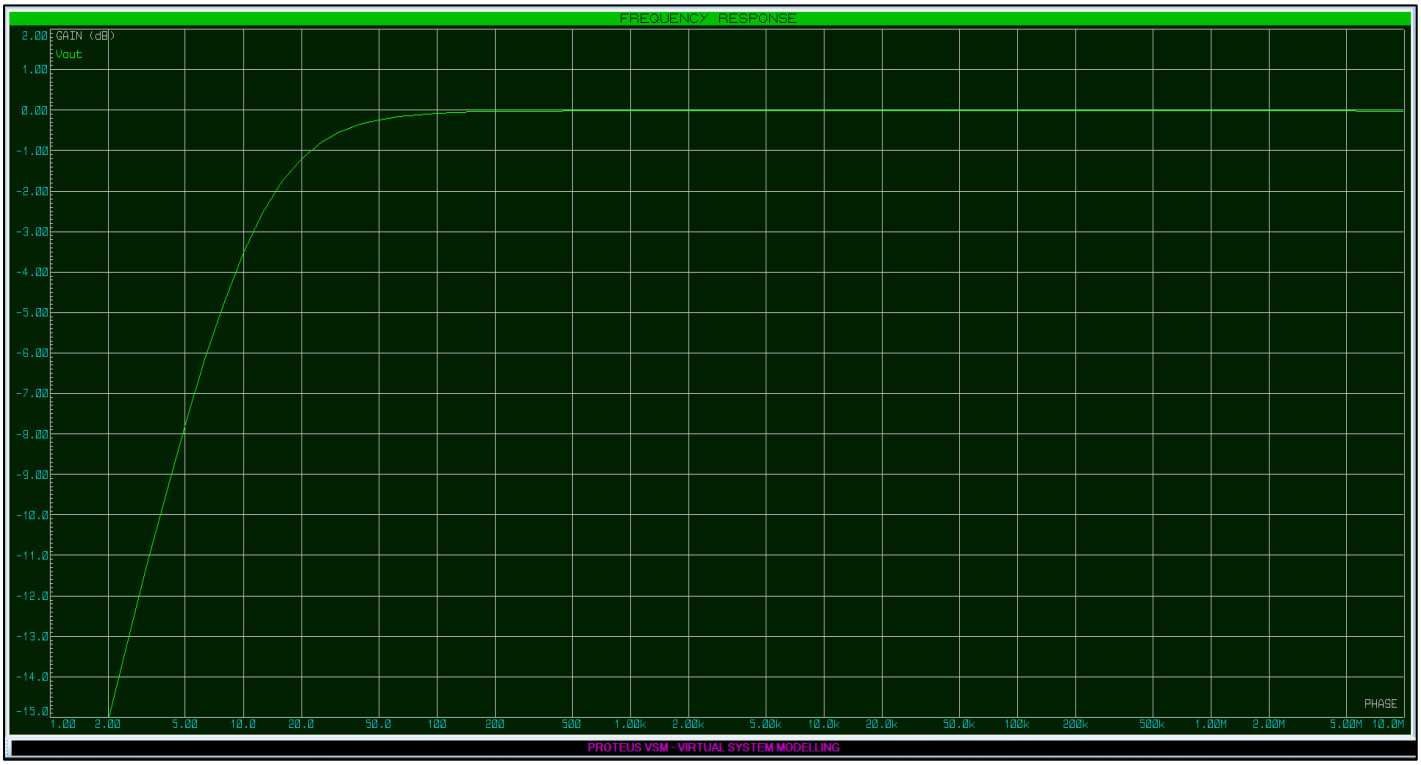


FIGURE 2 : FREQUENCY RESPONSE OF THE INPUT BUFFER

-

Observations:

Pass band gain = -0.052dB

Lower cutoff frequency = 4.72Hz

Higher cutoff frequency >> 6 MHz

Input buffer is worked as expected.

BJT Amplifier (Common Emitter) and adjusting the bandwidth

AC Analysis

$V_0 = -i_c R_{10}$

$i_c = \beta i_B$

$V_0 = -\beta i_B R_{10}$

$i_B = \frac{V_i}{r_{in}}$

$r_{in} = \beta r_e$

$r_e = \frac{0.025V}{I_E}$

Using the above equations, the Gain of the amplifier can be defined as,

$$A_v = \frac{R_C}{r_e}$$

Hence, $R_C = |A_v| \times r_e$ (1)

DC Analysis

Value of the gain is 385. Also, assume that Vcc = 24V, V_{CE} = 10V and $I_C \approx I_E$ = 2mA. Then,

$r_e = 0.025\ V / 2\ mV$

$r_e = 12.5\Omega$

Applying equation (1),

$R_C = 385 \times 12.5$

$R_C = 4812.5\Omega$

$R_C \approx 4700\ k\Omega$ (Taking)

Applying K'Choff law,

$$V_{cc} = I_C R_C + V_{CE} + I_E R_E$$

$24 = 2 \times 10^{-3}(R_C + R_E) + 10$, where $I_C \approx I_E$

$R_E = 2300\ \Omega$

$R_C \approx 2400\ \Omega$ (Taking)

Base Voltage,

$V_B = V_E + 0.7$

$V_B = I_E R_E + 0.7$

$V_B = (2\times 10^{-3} \times 2400) + 0.7$

$V_B = 5.5V$

R_8 and R_9 Ratio can be calculated using voltage divider rule.

$$V_B = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

$$\frac{R_1}{R_2} = \frac{37}{11}$$

Taking R1 = 2400 Ω and R2 = 1000 Ω

Resistor values were selected as R_1 = 2.4kΩ and R_2 =1kΩ. Now let's find the value of C_1 capacitor.

$$R_{in(eq)} = R_1//R_2//\beta r_e$$

$$R_{in(eq)} = 2400//1000//200 \times 12.5$$

$$R_{in\,(eq)} = 550.46\ \Omega$$

For 10Hz lower cutoff frequency,

$$C_1 = \frac{1}{2\pi \times 550.46 \times 10}$$

$$C_1 = 28.91\mu F$$

Taking C1 = $22\mu F$

No let's calculate the C_2 capacitor,

$$R_{in(eq)} = R_1//R_2//\beta r_e$$

$$R_{in(eq)} = 2400//1000//12.5$$

$$R_{in\,(eq)} = 12.28\ \Omega$$

For 10Hz lower cutoff frequency,

$$C_2 = \frac{1}{2\pi \times 12.28 \times 10}$$

$$C_2 = 1296\ \mu F$$

Taking C2 = $1000\mu F$ = 1mF

To get C3 value,

$$C_3 = \frac{1}{2\pi \times R_C \times 10}$$

$$C_3 = \frac{1}{2\pi \times 4700 \times 10}$$

$$C_3 = 3.38\ \mu F$$

Taking C3 = 3.3 μF

To adjust the bandwidth, we use a capacitor C5 with the common emitter transistor

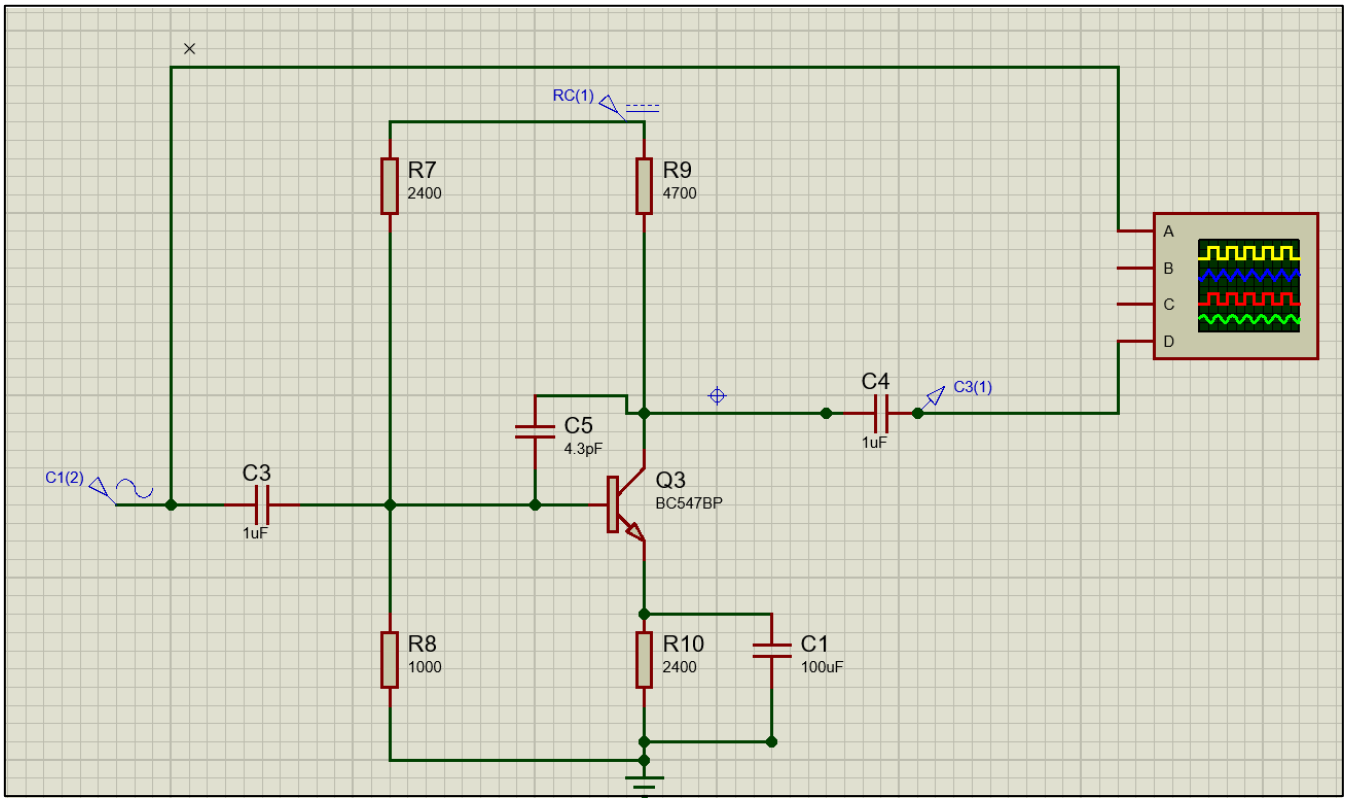


FIGURE 4 : AMPLIFIER CIRCUIT AFTER ADJUSTING THE BANDWIDTH

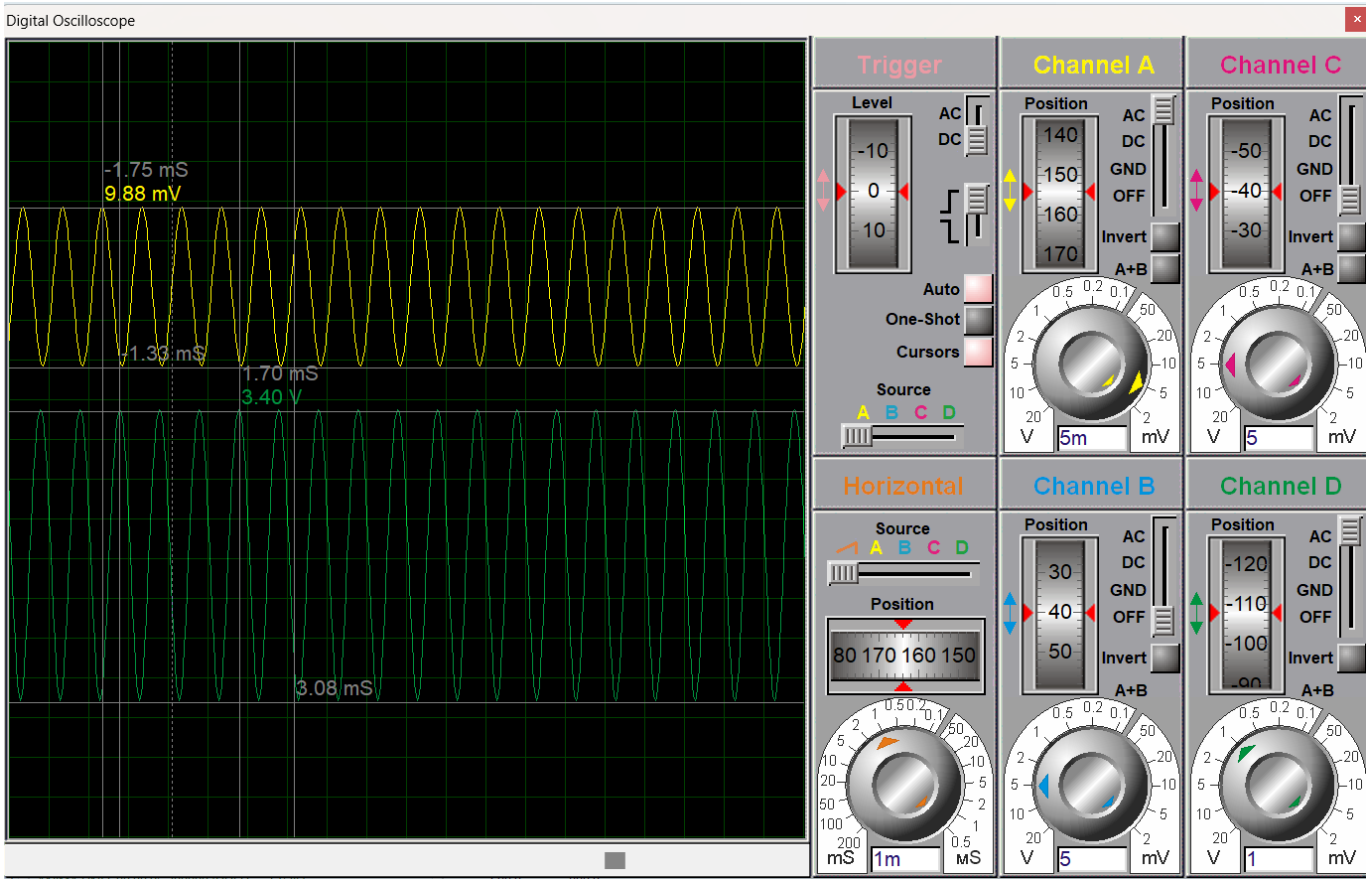


FIGURE 3 : OSCILLOSCOPE OUTPUT OF THE AMPLIFIER CIRCUIT

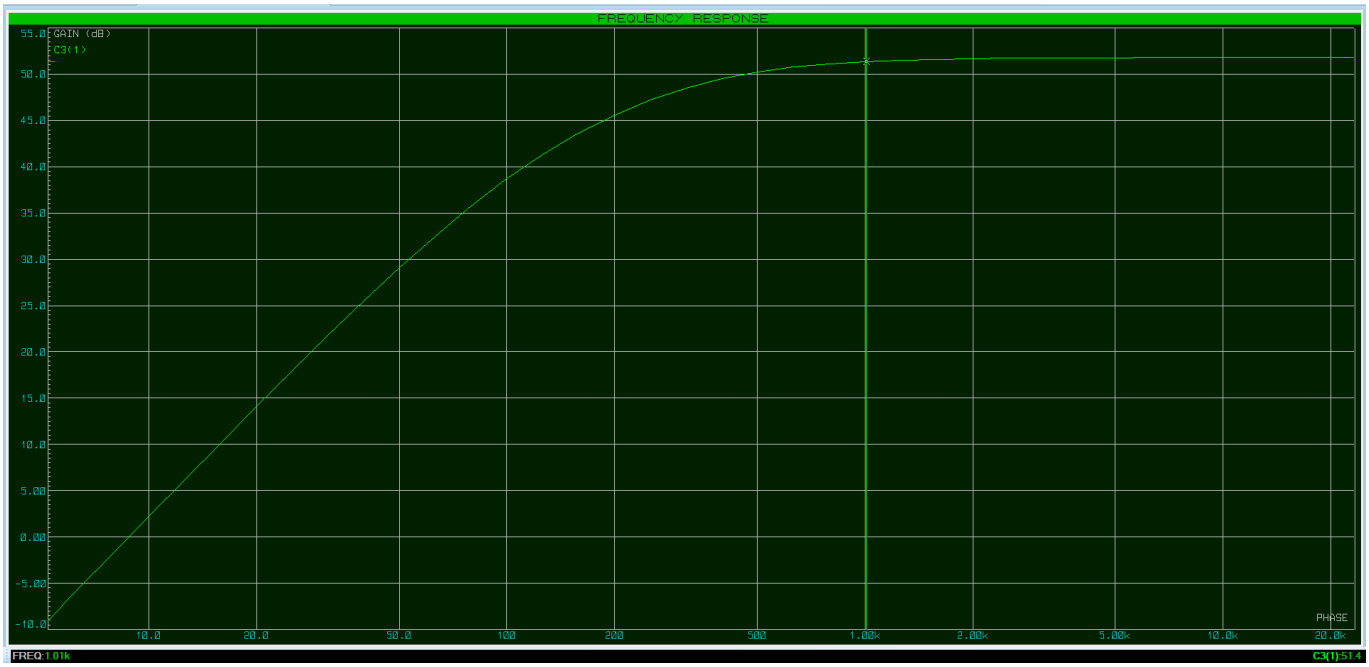


FIGURE 5 : FREQUENCY RESPONSE CURVE OF THE AMPLIFYING CIRCUIT

Observations:

Pass band gain = 51.8dB (gain ≈ 385)

Lower cutoff frequency = 336 Hz

Higher cutoff frequency = 6.15 MHz

Hence the bandwidth = 6.15MHz ≈ 6 MHz

After connecting all circuit together (Input buffer, output buffer and amplifier circuit with having 6MHz bandwidth)

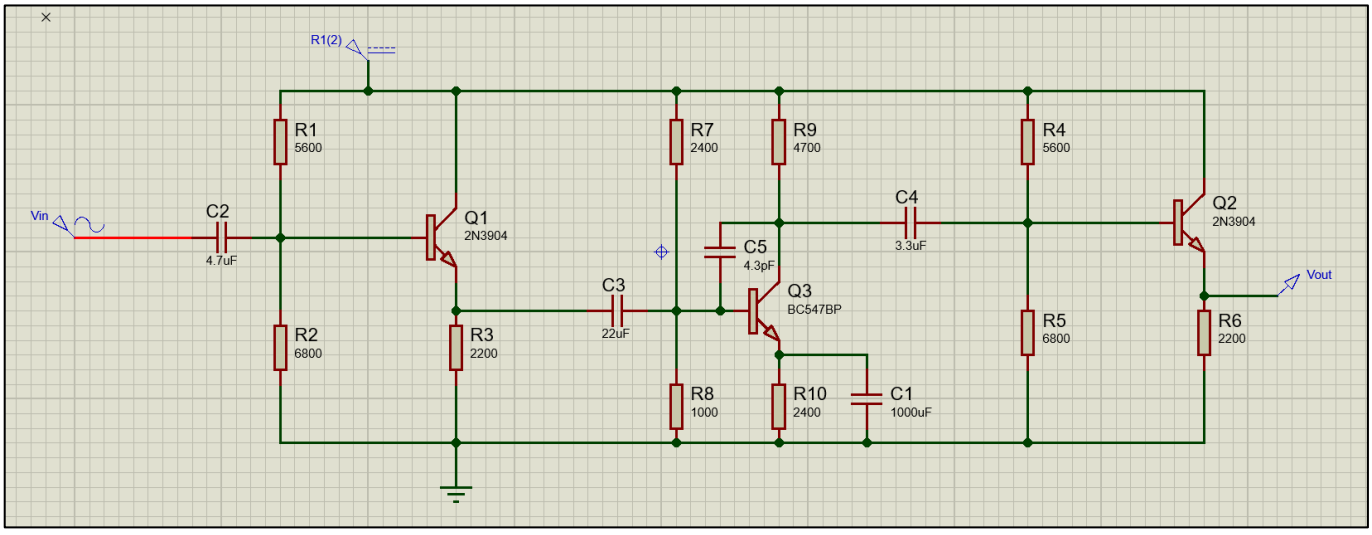


FIGURE 6 : AFTER CONNECTING ALL CIRCUIT TOGETHER

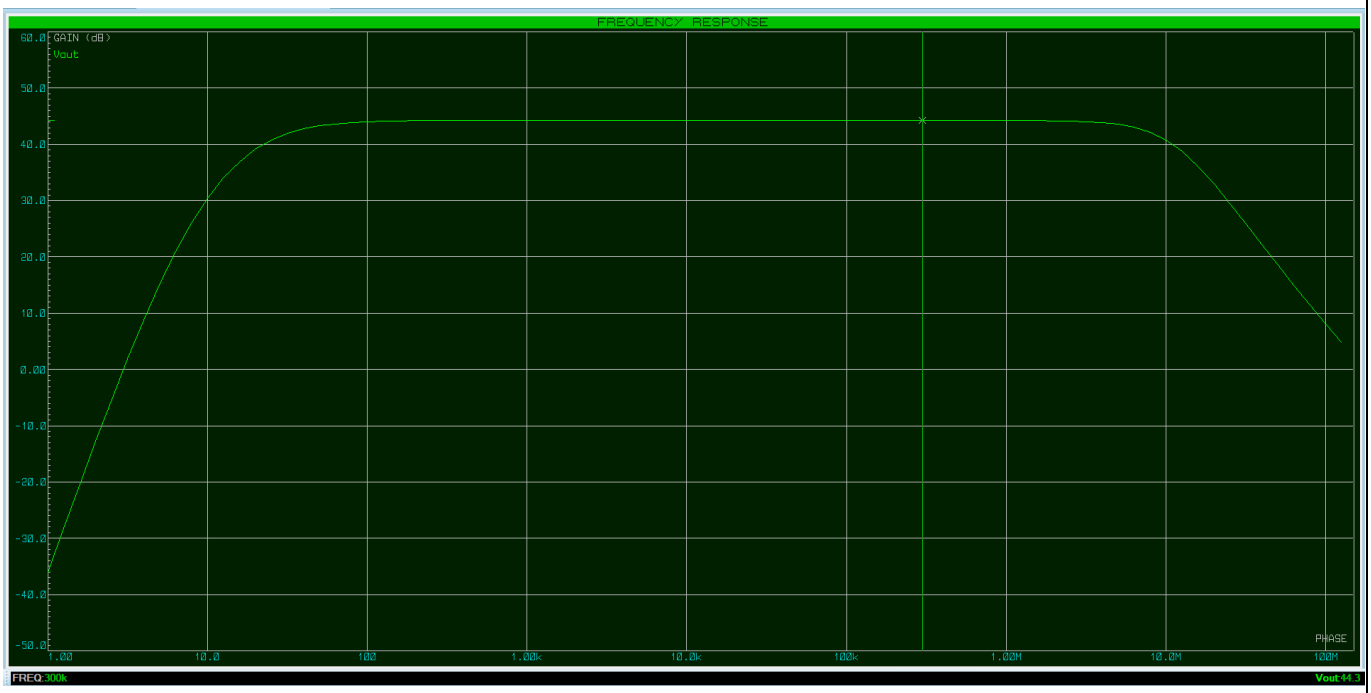


FIGURE 7 : FREQUENCY RESPONSE OF AFTER CONNECTING ALL CIRCUIT TOGETHER

Observations:

Pass band gain = 44.3dB (gain ≠ 385)

Lower cutoff frequency = 27.9 Hz

Higher cutoff frequency = 9.30 MHz

Hence the bandwidth almost = 9.30MHz

We can observe that the expected gain and bandwidth are changed when connecting all circuits. To get the expected output we have to adjust some resistor values and capacitor values.

Here,

- Used two 2.2pF capacitors (C5, C6 – Both are series)
- R10 changed 2400 Ω to 2200 Ω
- R4 changed 5600 Ω to 100kΩ
- R5 changed 6800 Ω to 220k Ω

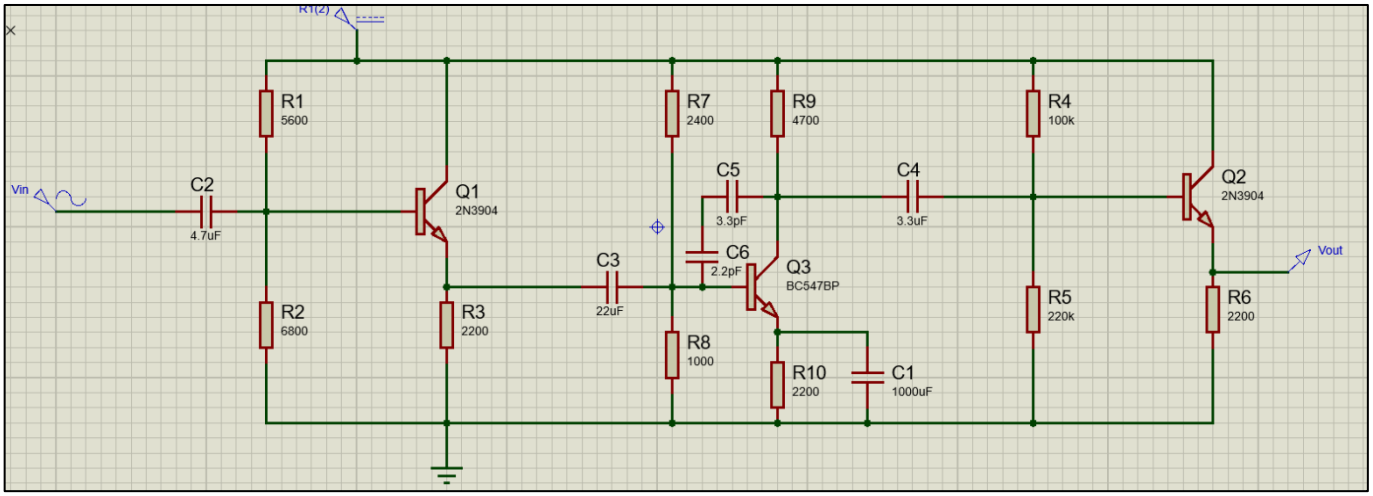


FIGURE 8 : FINAL IMPLEMENTED CORRECT PROTEUS CIRCUIT

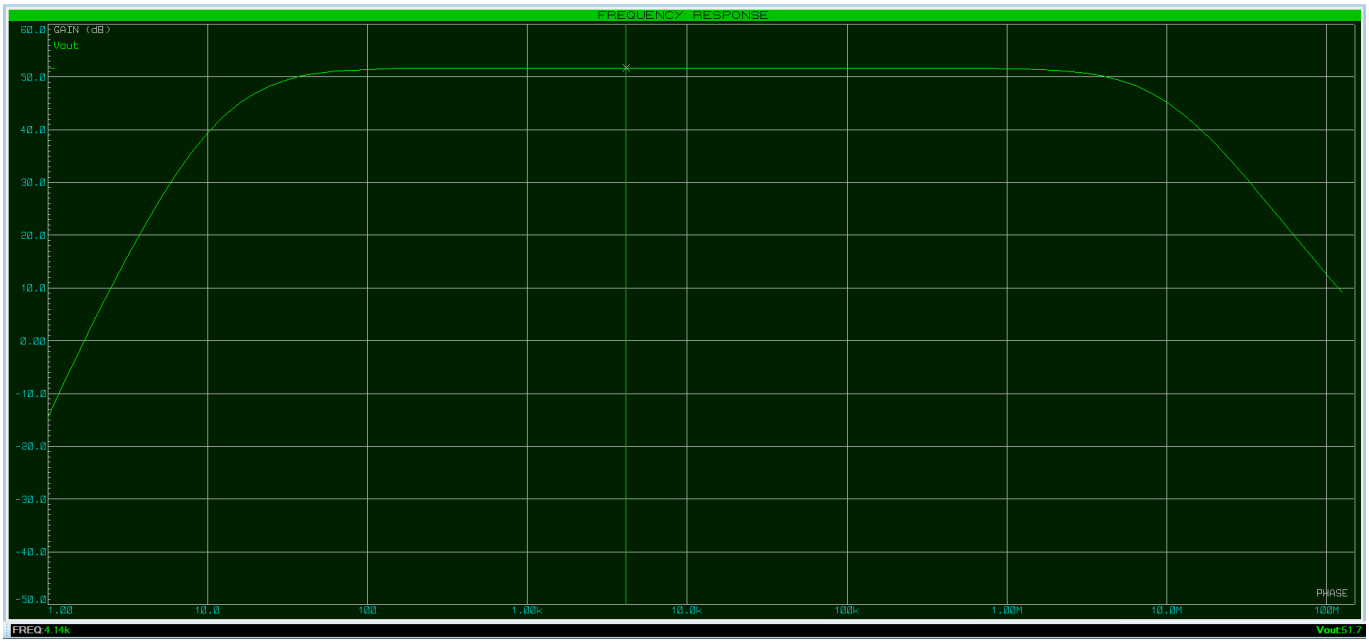


FIGURE 9 : FREQUENCY RESPONSE OF THE FINAL CIRCUIT

Observations:

Pass band gain = 51.7dB (gain = 385)

Lower cutoff frequency = 26.7 Hz

Higher cutoff frequency = 5.94 MHz

Hence the bandwidth almost = 6 MHz

03. IMPLEMENTATION OF THE CIRCUIT

3.1 Proteus Implementation

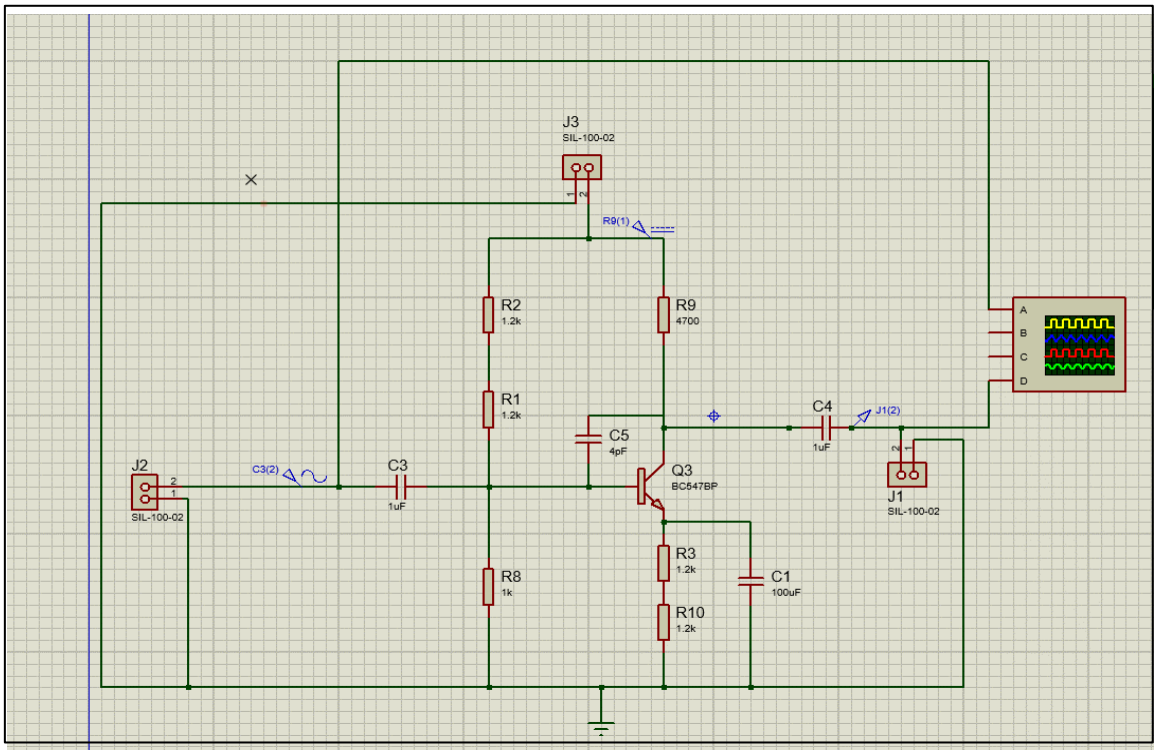


FIGURE 11 : FINAL IMPLEMENTED CIRCUIT ON PROTEUS

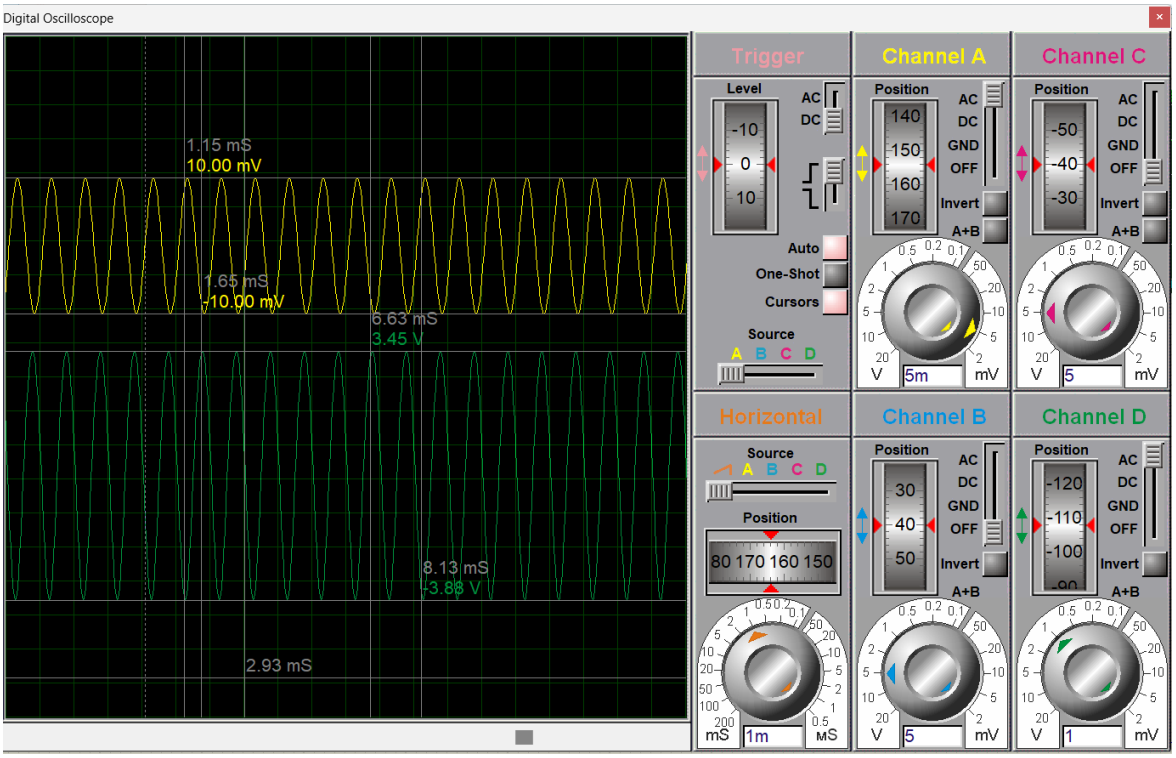


FIGURE 10 : OSCILLOSCOPE OUTPUT IF THE CURCUIT

FREQUENCY RESPONSE

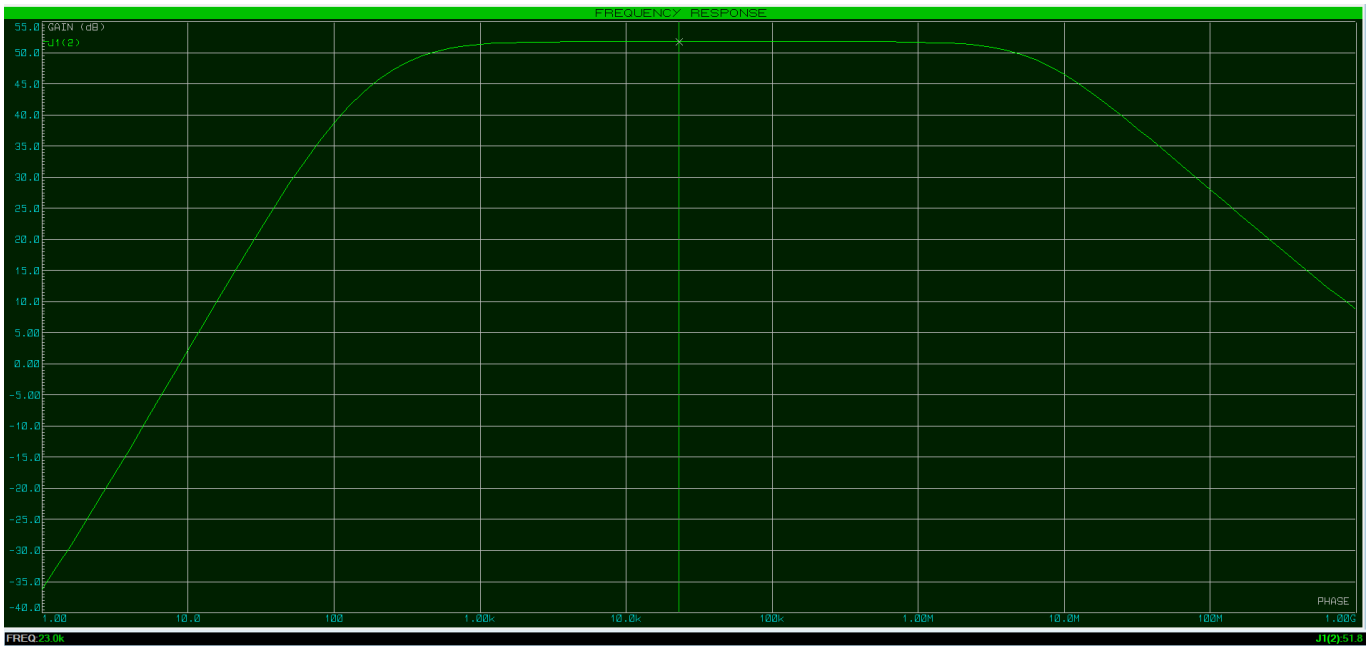


FIGURE 12 : GAIN OF THE AMPLIFIERIN FREQUENCY RESPONSE CURVE

Upper Cut-off Frequency – 6.53 MHz

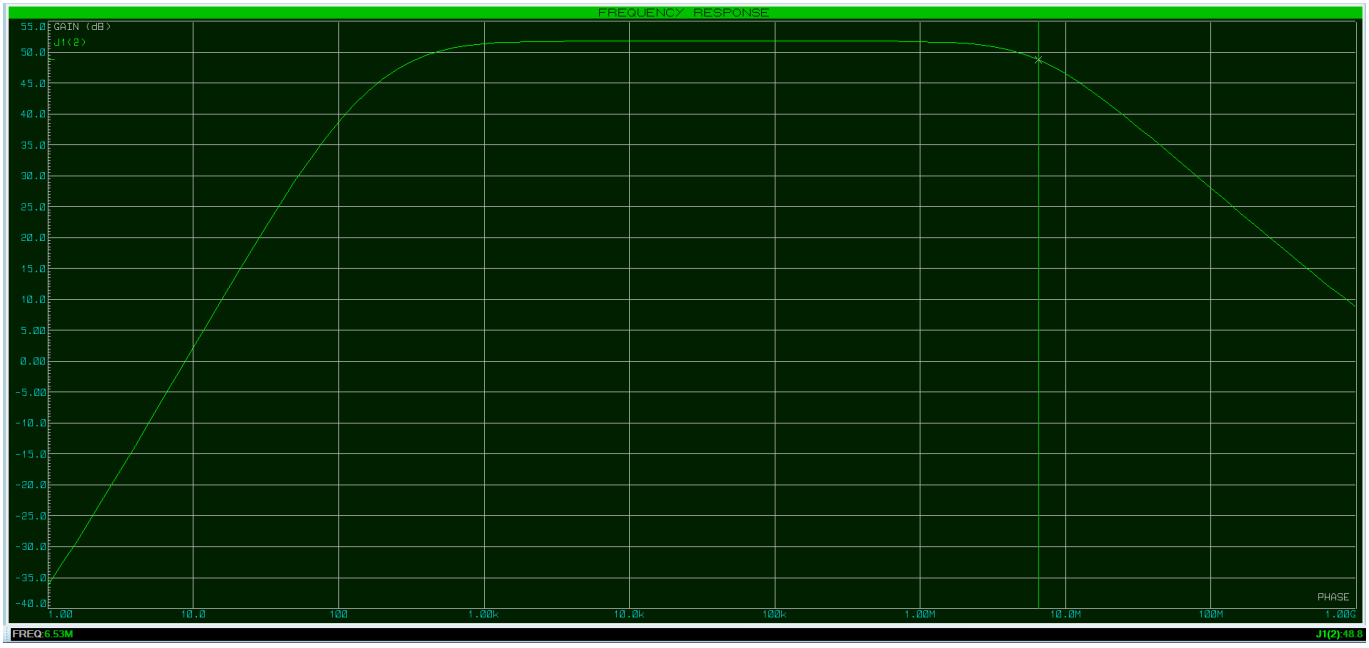


FIGURE 13 : UPPER CUT OFF FREQUENCY OF THE FREQUENCY RESPONSE CURVE

Lower Cut-off Frequency – 338 Hz

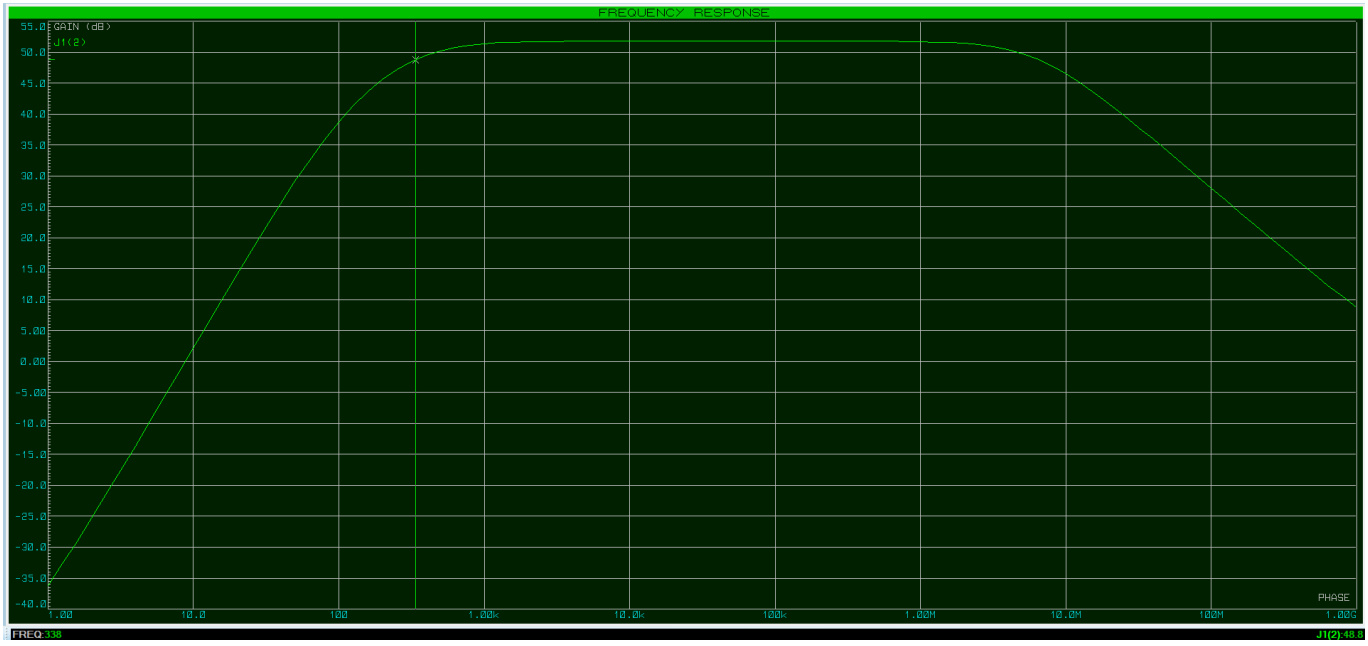


FIGURE 14 : LOWER CUT OFF FREQUENCY OF THE FREQUENCY RESPONSE CURVE

Now the Bandwidth can be calculated as,

$$\text{Bandwidth} = f(upper\ cut - off\ frequency) - f(lower\ cut - off\ frequency)$$

= 6.53 MHz – 338 Hz

= 6.529 MHz

This is closer to 6 MHz. Hence the required bandwidth is being obtained accurately.

Observations Summary:

- Pass band gain = 51.8dB (gain ≈ 385)
- Lower cutoff frequency = 338 Hz
- Higher cutoff frequency = 6.53 MHz
- Bandwidth = 6.52 MHz

3.2 PCB on proteus

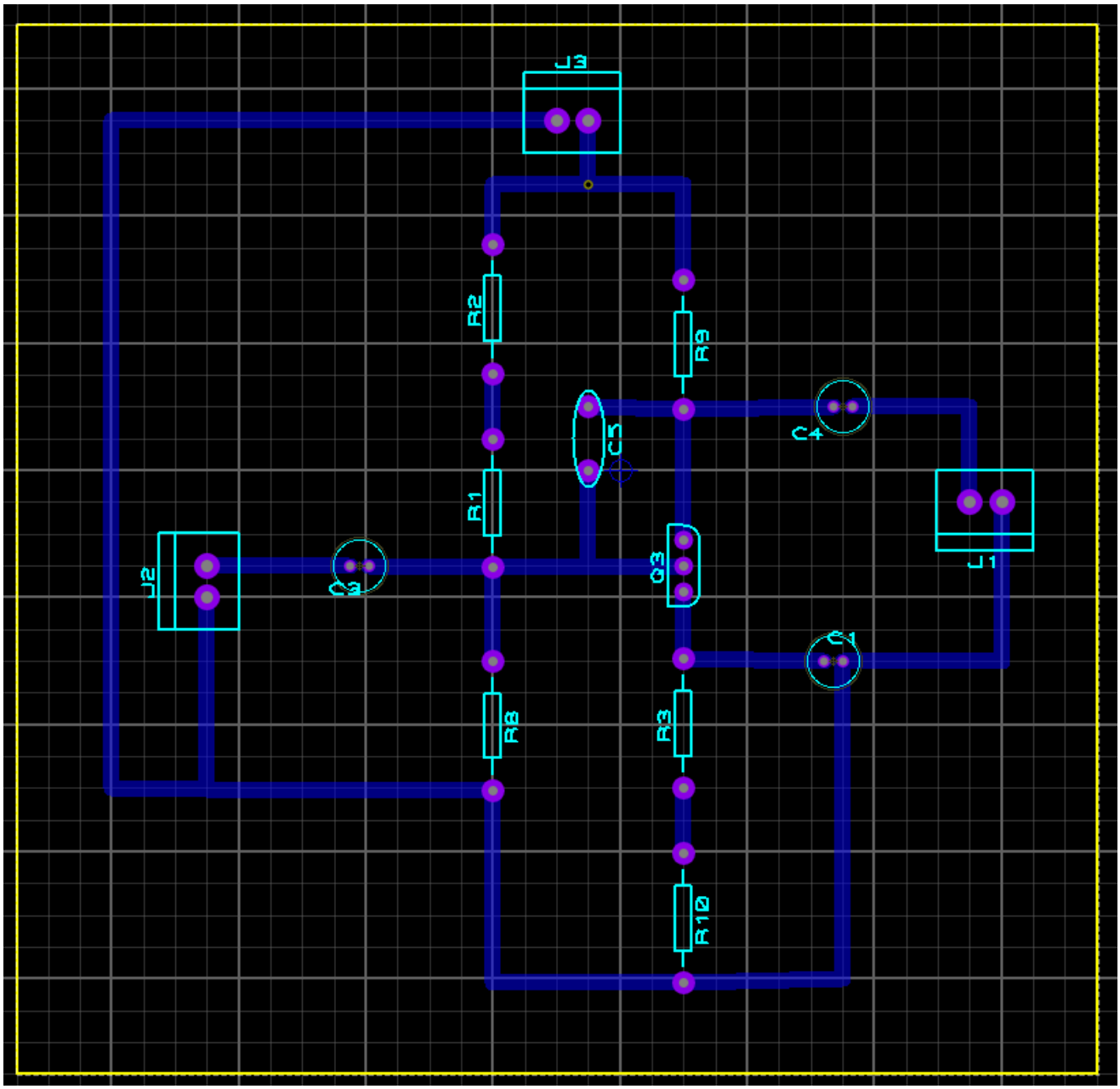
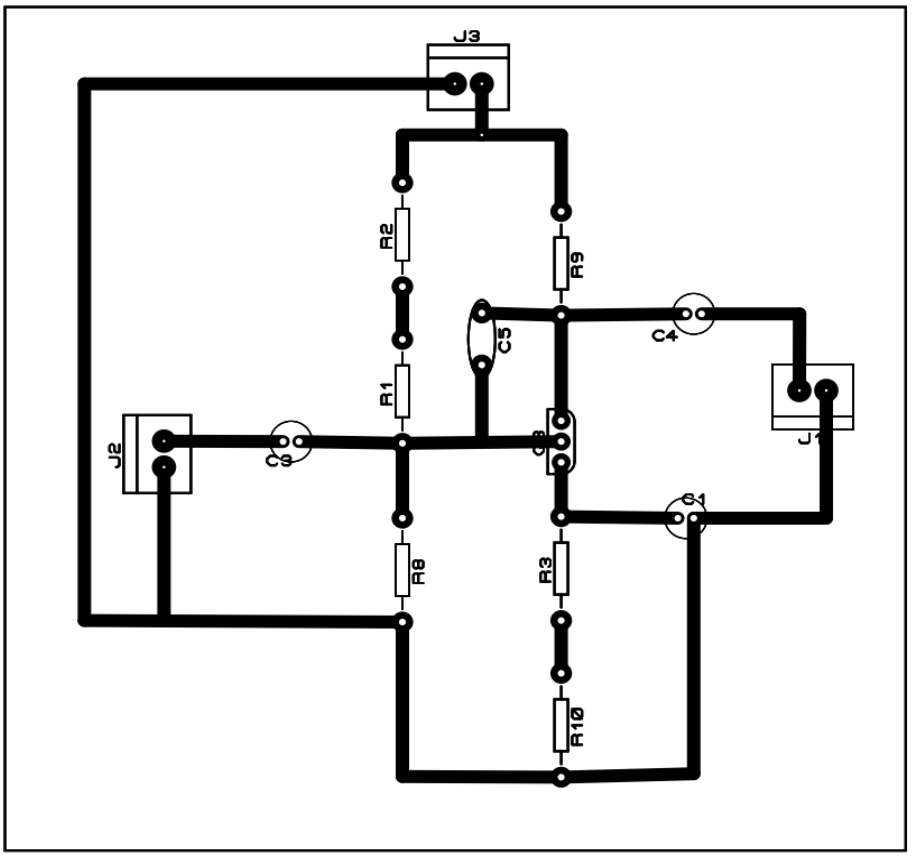


FIGURE 15 : FINAL PCB DESIGN



3.3. 3D Visualization

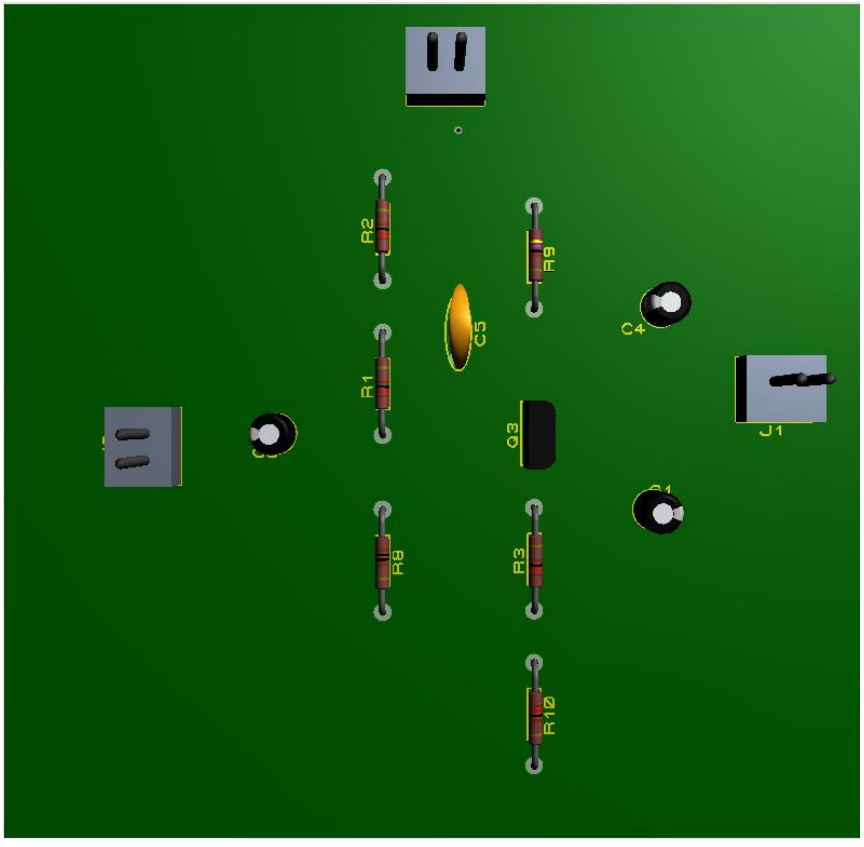


FIGURE 16 : 3D VISUALIZATION OF THE PCB

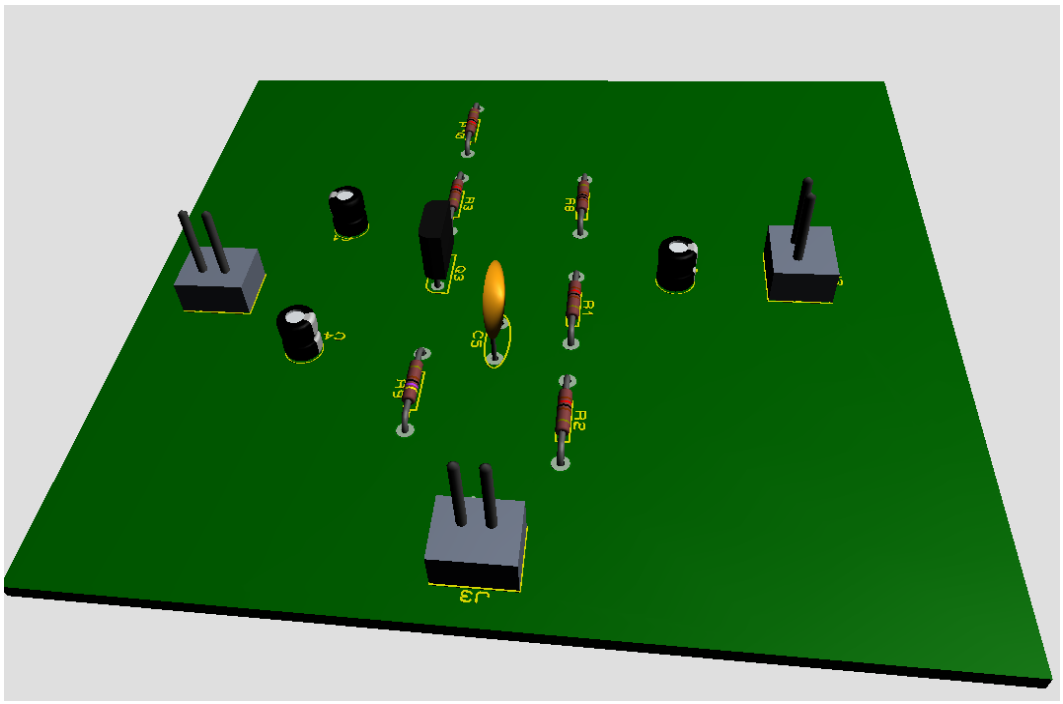


FIGURE 17 : TOP VIEW OF 3D VISULAIZATION

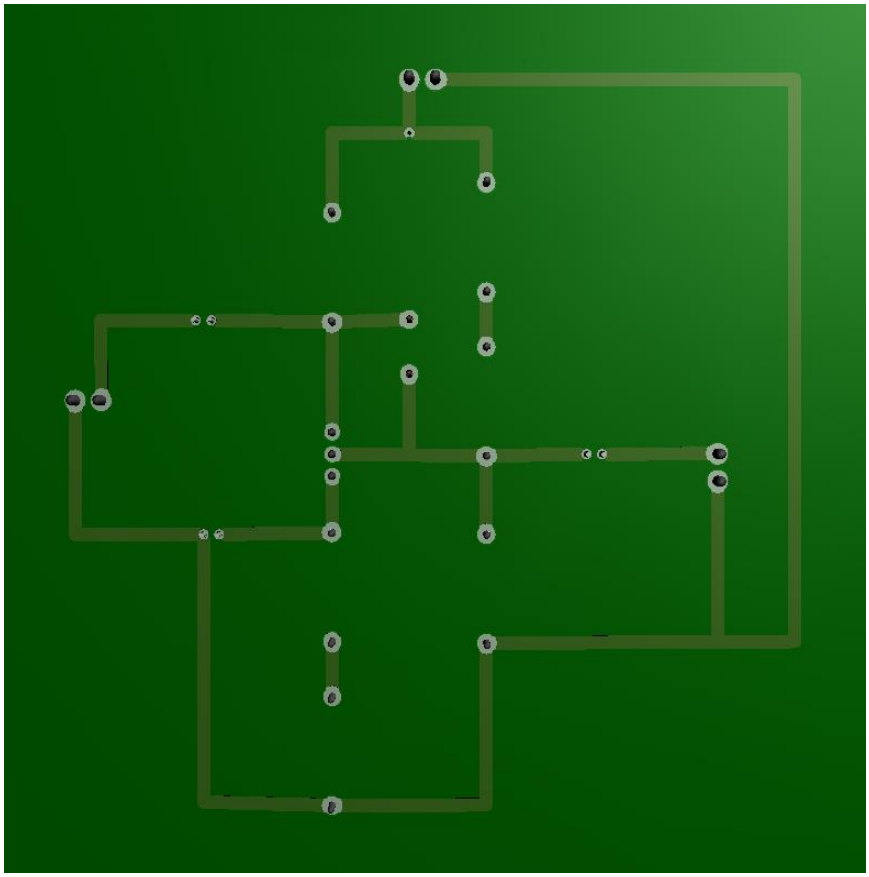


FIGURE 18 : BOTTOM VIEW OF 3D VISULAIZATION

3.2 Breadboard Implementation

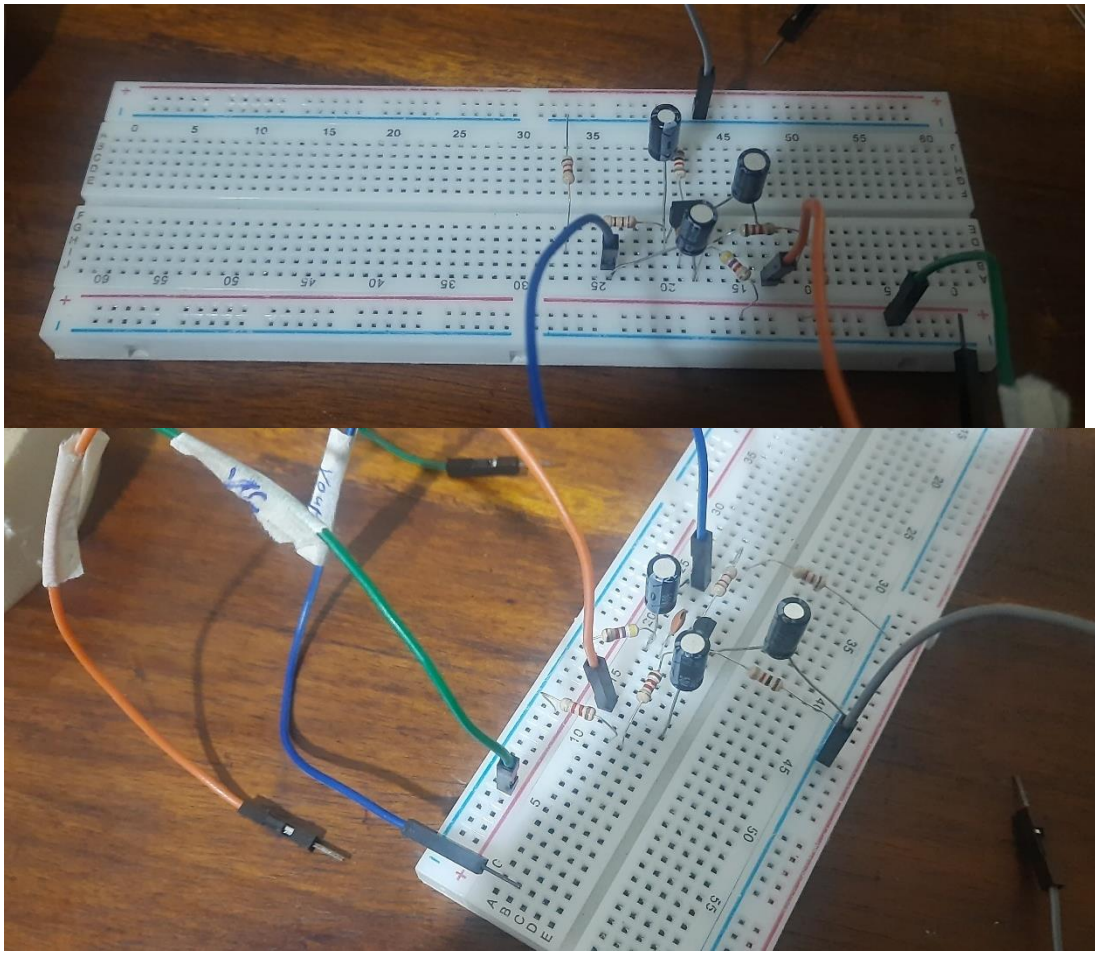


FIGURE 19 : CIRCUIT IMPLMENTED ON THE BREADBOARD

04. DISCUSSION

The Common Emitter BJT amplifier was designed to have a bandwidth of 6 MHz and a gain of 385.

At first we tried many circuits to amplify the amplify the signal. But finally, the circuit present in the report was used because we thought that circuit is simpler to implement physically. Accordingly, the theoretical calculations and the proteus simulation were done according to that. So, we obtained a gain of 51.8 dB (389.07) as shown in the FIGURE *12* and bandwidth of 6.52 MHz. So, there is only a small deviation in the gain obtained in proteus and actual gain required.

The reasons behind the small deviations of the gain can be analyzed as below.

- An oscilloscope is being used to measure the output signal. The input impedance of the oscilloscope will act as a load impedance to the circuit. This load impedance was not considered when the simulations in the proteous were done. An output buffer was used to minimize this issue.
- The exactly calculated resistor and capacitor components were not being able to use since some of the components were not available in the Sri Lanka market. Therefore, approximated components were used.
- Oscilloscope calibration errors, the capacitances in the probes are another practical issues that contribute to the deviations in the gain.

We implemented our circuit on a breadboard as shown in the FIGURE *19*. But the required output was not observed. Within that limited time, we were only able to connect the components and supply the signal generator input to the circuit.