**Title**

HW-SW SystemC Co-Simulation SoC Validation Platform

**Analysis Capability Report**

Contract No. 4200022968

by

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**Table of Contents**

1 introduction 3

1.1 Purpose and Scope 3

1.2 Reference Documents 3

1.3 Revisions 3

2 Configuration Analysis 4

2.1 AHBCTRL 4

2.2 APBCTRL 5

2.3 MCTRL 5

2.4 Generic Memory 6

2.5 MMU\_CACHE 6

2.5.1 Cache 6

2.5.2 Localram 7

2.5.3 MMU 7

2.6 GPTimer 7

2.7 IRQMP 8

2.8 SoCWire 8

3 Performance Analysis & Communication analysis 8

3.1 AHBCTRL 8

3.2 APBCTRL 8

3.3 MCTRL 8

3.4 Generic Memory 8

3.5 MMU\_CACHE 8

3.5.1 Cache 8

3.5.2 Localram 8

3.5.3 MMU 8

3.6 GPTimer 8

3.7 IRQMP 9

3.8 SoCWire 9

**Table of Tables**

Table 1 - Referenced Documents 4

Table 2 - Revisions of this document 4

# introduction

## Purpose and Scope

This document is the Analysis Capability Report of the SystemC Co-Simulation SoC Validation Platform (SoCRocket) and ist contained simulation models. It describes all analysis features provided for the user concerning configuration

## Reference Documents

|  |  |  |
| --- | --- | --- |
| **Reference** | **Document Number** | **Document Title, Author** |
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|  |  |  |

Table 1 - Referenced Documents

## Revisions

The following table will be updated during the course of the project.

|  |  |  |
| --- | --- | --- |
| **Version** | **Date** | **Description** |
| 0.1 | 02/01/11 | Initial draft version |
| 0.2 | 23/01/11 | Configuration analysis |
|  |  |  |
|  |  |  |

Table 2 - Revisions of this document

# Configuration Analysis

The VPI produces reports for the configuration of each simulation model in the system. The reports are generated in the constructor of the separate IPs. They are written to std::out, if the system is configured for verbosity-level 4 (info) or above.

## AHBCTRL

The configuration report is generated in the constructor of class ahbctrl. It displays all constructor parameters of the device. The example below shows the report for an AHBCTRL with priority arbitration (rrobin = 0), power monitoring enabled (pow\_mon = 1) and AT abstractions.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

@0 s /0 (ahbctrl): Info: \* Created AHBCTRL with following parameters:

@0 s /0 (ahbctrl): Info: \* ioaddr/iomask: fff/fff

@0 s /0 (ahbctrl): Info: \* cfgaddr/cfmask: ff0/ff0

@0 s /0 (ahbctrl): Info: \* rrobin: 0

@0 s /0 (ahbctrl): Info: \* split: 0

@0 s /0 (ahbctrl): Info: \* defmast: 0

@0 s /0 (ahbctrl): Info: \* ioen: 0

@0 s /0 (ahbctrl): Info: \* fixbrst: 0

@0 s /0 (ahbctrl): Info: \* fpnpen: 1

@0 s /0 (ahbctrl): Info: \* mcheck: 1

@0 s /0 (ahbctrl): Info: \* pow\_mon: 1

@0 s /0 (ahbctrl): Info: \* abstractionLayer (LT = 8 / AT = 4): 4

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The AHBCTRL additionally generates a report describing the decoder initialization. This report is produced in the start\_of\_simulation function of class ahbctrl (for verbosity >= 4).

The report lists the up to 16 slaves and up to 16 masters, which are bound to the AHBCTRL. Each of them may contain up to four sub-devices. Sub-devices are identified by a base register entry (BAR0-4) comprising the 12bit MSB address of the component (haddr) and the 12bit AHB address mask (hmask).

The example below shows a report for an AHBCTRL with one master (Testbench) and two slaves: APBCTRL, MCTRL. The MCTRL contains three sub-devices.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

@0 s /0 (top.ahbctrl): Info: \* DECODER INITIALIZATION

@0 s /0 (top.ahbctrl): Info: \* ----------------------

@0 s /0 (top.ahbctrl): Info: \* SLAVE name: top.apbctrl

@0 s /0 (top.ahbctrl): Info: \* BAR0 with MSB addr: 0x800 and mask: 0xfff

@0 s /0 (top.ahbctrl): Info: \* BAR1 not used.

@0 s /0 (top.ahbctrl): Info: \* BAR2 not used.

@0 s /0 (top.ahbctrl): Info: \* BAR3 not used.

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@0 s /0 (top.ahbctrl): Info: \* SLAVE name: top.mctrl

@0 s /0 (top.ahbctrl): Info: \* BAR0 with MSB addr: 0x0 and mask: 0xe00

@0 s /0 (top.ahbctrl): Info: \* BAR1 with MSB addr: 0x200 and mask: 0xe00

@0 s /0 (top.ahbctrl): Info: \* BAR2 with MSB addr: 0x400 and mask: 0xc00

@0 s /0 (top.ahbctrl): Info: \* BAR3 not used.

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@0 s /0 (top.ahbctrl): Info: \* Master name: top.testbench

@0 s /0 (top.ahbctrl): Info: \* BAR0 not used.

@0 s /0 (top.ahbctrl): Info: \* BAR1 not used.

@0 s /0 (top.ahbctrl): Info: \* BAR2 not used.

@0 s /0 (top.ahbctrl): Info: \* BAR3 not used.

@0 s /0 (top.ahbctrl): Info: \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

## APBCTRL

The configuration report for the APBCTRL is generated in the constructor of class apbctrl. It displays all constructor parameters of the device. The example below shows an APBCTRL at LT abstraction.

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@0 s /0 (top.apbctrl): Info: \* Created APBCTRL with following parameters:

@0 s /0 (top.apbctrl): Info: \* haddr/hmask: 800/fff

@0 s /0 (top.apbctrl): Info: \* mcheck: 1

@0 s /0 (top.apbctrl): Info: \* hindex: 1

@0 s /0 (top.apbctrl): Info: \* pow\_mon: 0

@0 s /0 (top.apbctrl): Info: \* ambaLayer (LT = 8/AT = 4): 8

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The APBCTRL additionally generates a report describing its decoder initialization. This report is produced in the start\_of\_simulation function of class apbctrl (for verbosity >= 4).

The report lists the up to 16 slaves, which are bound to the APBCTRL. Each of them is identified by a 12 bit segment address (paddr) and a 12 bit AMBA address mask (pmask). The example shows a report for an APBCTRL with one slave. The APB interface of the MCTRL is located at address/mask: 0x000/0xfff.

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@0 s /0 (top.apbctrl): Info: \* APB DECODER INITIALIZATION

@0 s /0 (top.apbctrl): Info: \* --------------------------

@0 s /0 (top.apbctrl): Info: \* Slave name: top.mctrl

@0 s /0 (top.apbctrl): Info: \* BAR with MSB addr: 0 and mask: fff

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## MCTRL

The configuration report for the memory controller unit (MCTRL) is generated in the constructor of class mctrl. It displays all constructor parameters of the device. The example below shows a MCTRL with AT abstraction and SDRAM enabled (sden = 1). The SD bus is 32 bits wide (sdbits). The special features of mobile RAM are disabled (mobile = 0).

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@0 s /0 (top.mctrl): Info: \* Created MCTRL with following parameters:

@0 s /0 (top.mctrl): Info: \* romasel: 28

@0 s /0 (top.mctrl): Info: \* sdrasel: 29

@0 s /0 (top.mctrl): Info: \* romaddr/rommask: 0/e00

@0 s /0 (top.mctrl): Info: \* ioaddr/iomask: 200/e00

@0 s /0 (top.mctrl): Info: \* ramaddr/rammask: 400/c00

@0 s /0 (top.mctrl): Info: \* paddr/pmask: 0/fff

@0 s /0 (top.mctrl): Info: \* wprot: 0

@0 s /0 (top.mctrl): Info: \* srbanks: 5

@0 s /0 (top.mctrl): Info: \* ram8: 1

@0 s /0 (top.mctrl): Info: \* ram16: 1

@0 s /0 (top.mctrl): Info: \* sepbus: 0

@0 s /0 (top.mctrl): Info: \* sdbits: 32

@0 s /0 (top.mctrl): Info: \* mobile: 0

@0 s /0 (top.mctrl): Info: \* sden: 1

@0 s /0 (top.mctrl): Info: \* hindex: 0

@0 s /0 (top.mctrl): Info: \* pindex: 0

@0 s /0 (top.mctrl): Info: \* pow\_mon: 0

@0 s /0 (top.mctrl): Info: \* abstractionLayer (LT = 8 / AT = 4): 4

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## Generic Memory

The configuration memory for the generic memory is generated in the constructor of class GenericMemory. The generic memory can be configured to represent ROM, IO, SRAM and SDRAM storage. The example below shows the configuration report for a 512 MB SDRAM consisting of one memory bank with 16 columns.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

@0 s /0 (top.sdram): Info: \* Created GenericMemory with following parameters:

@0 s /0 (top.sdram): Info: \* device\_type (0-ROM, 1-IO, 2-SRAM, 3-SDRAM): 3

@0 s /0 (top.sdram): Info: \* banks: 1

@0 s /0 (top.sdram): Info: \* bsize: 20000000

@0 s /0 (top.sdram): Info: \* bit width: 32

@0 s /0 (top.sdram): Info: \* cols (SD only): 16

@0 s /0 (top.sdram): Info: \* pow\_mon: 0

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## MMU\_CACHE

Depending on the configuration the MMU\_CACHE IP consists of multiple sub-components. Each of them independently generates a configuration report.

### Cache

The configuration reports for the instruction cache and the data cache are generated by the constructor of class vectorcache. The report contains all relevant constructor parameters. Additionally, information is given concerning the size of the cache in kb, the number of bytes per cache line, the number of cache lines per set and the width of the cache tag in bits. The example below shows the configuration report for a data cache with 4 sets of 1kb:

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@0 s /0 (mmu\_cache.dcache): Info: \* Created cache memory with following parameters:

@0 s /0 (mmu\_cache.dcache): Info: \* ------------------------------------------

@0 s /0 (mmu\_cache.dcache): Info: \* mmu\_en: 0

@0 s /0 (mmu\_cache.dcache): Info: \* burst\_en: 0

@0 s /0 (mmu\_cache.dcache): Info: \* sets: 4

@0 s /0 (mmu\_cache.dcache): Info: \* setsize: 1

@0 s /0 (mmu\_cache.dcache): Info: \* setlock: 0

@0 s /0 (mmu\_cache.dcache): Info: \* linesize: 4

@0 s /0 (mmu\_cache.dcache): Info: \* repl (0-Direct Mapped, 1-LRU,   
 2-LRR, 3-RANDOM): 3

@0 s /0 (mmu\_cache.dcache): Info: \* ------------------------------------

@0 s /0 (mmu\_cache.dcache): Info: \* Size of each cache set 1 kb

@0 s /0 (mmu\_cache.dcache): Info: \* Bytes per line 16 (offset bits: 4)

@0 s /0 (mmu\_cache.dcache): Info: \* Number of cache lines per set 64   
 (index bits: 6)

@0 s /0 (mmu\_cache.dcache): Info: \* Width of cache tag in bits 22

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### Localram

The configuration report for the localram is generated in the constructor of class localram. Because the localram is a very simple storage device, the report only contains two parameters, associated with starting address and capacity. The example shows the reports for an instruction scratchpad and a data scratchpad in default configuration.

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@0 s /0 (mmu\_cache.ilocalram): Info: \* Created localram with following parameters:

@0 s /0 (mmu\_cache.ilocalram): Info: \* ---------------------------------------

@0 s /0 (mmu\_cache.ilocalram): Info: \* lrstart (start address): 8e000000

@0 s /0 (mmu\_cache.ilocalram): Info: \* lrsize: 80000 bytes

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@0 s /0 (mmu\_cache.dlocalram): Info: \* Created localram with following parameters:

@0 s /0 (mmu\_cache.dlocalram): Info: \* ---------------------------------------

@0 s /0 (mmu\_cache.dlocalram): Info: \* lrstart (start address): 8f000000

@0 s /0 (mmu\_cache.dlocalram): Info: \* lrsize: 80000 bytes

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### MMU

The MMU configuration report is generated in the constructor of class mmu. The report contains all the configuration parameters of the mmu. The example below shows the report for a MMU with split TLBs (8x instructions, 8x data).

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

@0 s /0 (mmu\_cache.mmu): Info: \* Created mmu with following parameters:

@0 s /0 (mmu\_cache.mmu): Info: \* --------------------------------------

@0 s /0 (mmu\_cache.mmu): Info: \* itlbnum: 8

@0 s /0 (mmu\_cache.mmu): Info: \* dtlbnum: 8

@0 s /0 (mmu\_cache.mmu): Info: \* tlb\_type (0 - split, 1 - shared): 0

@0 s /0 (mmu\_cache.mmu): Info: \* tlb\_rep: 1

@0 s /0 (mmu\_cache.mmu): Info: \* mmupgsz (0, 2-4kb, 3-8kb, 4-16kb, 5-32kb): 0

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## GPTimer

The configuration report for the GPTimer is generated in the constructor of class gptimer. The report contains all the configuration parameters of the GPTimer. The example below shows the report for a GPTimer with 7 parallel counters and watchdog disabled.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

@0 s /0 (top.timer): Info: \* Created gptimer with following parameters:

@0 s /0 (top.timer): Info: \* ------------------------------------------

@0 s /0 (top.timer): Info: \* ntimers: 7

@0 s /0 (top.timer): Info: \* pindex: 0

@0 s /0 (top.timer): Info: \* paddr/pmask: 0/fff

@0 s /0 (top.timer): Info: \* pirq: 0

@0 s /0 (top.timer): Info: \* sepirq: 0

@0 s /0 (top.timer): Info: \* sbits: 18

@0 s /0 (top.timer): Info: \* nbits: 22

@0 s /0 (top.timer): Info: \* wdog: 0

@0 s /0 (top.timer): Info: \* pow\_mon: 0

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## IRQMP

The configuration report for the IRQMP is generated in the constructor of class irqmp. The report shows all the constructor parameters of the module. The example refers to an instance configured for two master CPUs. The extended interrupt (eirq) is mapped to IRQ line 4.

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@0 s /0 (top.irqmp): Info: \* Created configuration report with following parameters:

@0 s /0 (top.irqmp): Info: \* --------------------------------------------

@0 s /0 (top.irqmp): Info: \* paddr/pmask: 0/fff

@0 s /0 (top.irqmp): Info: \* ncpu: 2

@0 s /0 (top.irqmp): Info: \* eirq: 4

@0 s /0 (top.irqmp): Info: \* pindex: 0

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## SoCWire

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@0 s /0 (DUT): Info: \* Created AHB2SoCWire with following parameters:

@0 s /0 (DUT): Info: \* ----------------------------------------------

@0 s /0 (DUT): Info: \* paddr/pmask: fff/fff

@0 s /0 (DUT): Info: \* pindex: 0

@0 s /0 (DUT): Info: \* apb\_irq\_id: 0

@0 s /0 (DUT): Info: \* hindex: 0

@0 s /0 (DUT): Info: \* abstractionLayer (LT = 8 / AT = 4): 8

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# Performance Analysis & Communication analysis

## AHBCTRL

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@25360001 ps (ahbctrl): Report: \* AHBCtrl Statistic:

@25360001 ps (ahbctrl): Report: \* ------------------

@25360001 ps (ahbctrl): Report: \* Successful Transactions: 2500

@25360001 ps (ahbctrl): Report: \* Total Transactions: 2500

@25360001 ps (ahbctrl): Report: \* Simulation cycles: 2536

@25360001 ps (ahbctrl): Report: \* Idle cycles: 36

@25360001 ps (ahbctrl): Report: \* Bus utilization: 0.985804

@25360001 ps (ahbctrl): Report: \* Maximum arbiter waiting time: 10 ns

@25360001 ps (ahbctrl): Report: \* Master with maximum waiting time: 0

@25360001 ps (ahbctrl): Report: \* Average arbitr. time / transaction: 9996 ps

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## APBCTRL

## MCTRL

## Generic Memory

## MMU\_CACHE

### Cache

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@246700 ns (mmu\_cache.dcache): Report: \* Cacheing statistic:

@246700 ns (mmu\_cache.dcache): Report: \* -------------------

@246700 ns (mmu\_cache.dcache): Report: \* Read hits set0: 256

@246700 ns (mmu\_cache.dcache): Report: \* Read hits set1: 256

@246700 ns (mmu\_cache.dcache): Report: \* Read hits set2: 256

@246700 ns (mmu\_cache.dcache): Report: \* Read hits set3: 256

@246700 ns (mmu\_cache.dcache): Report: \* Total Read Hits: 1024

@246700 ns (mmu\_cache.dcache): Report: \* Read Misses: 1024

@246700 ns (mmu\_cache.dcache): Report: \* Read Hit Rate: 0.5

@246700 ns (mmu\_cache.dcache): Report: \* Write hits set0: 0

@246700 ns (mmu\_cache.dcache): Report: \* Write hits set1: 0

@246700 ns (mmu\_cache.dcache): Report: \* Write hits set2: 0

@246700 ns (mmu\_cache.dcache): Report: \* Write hits set3: 0

@246700 ns (mmu\_cache.dcache): Report: \* Total Write Hits: 0

@246700 ns (mmu\_cache.dcache): Report: \* Write Misses: 0

@246700 ns (mmu\_cache.dcache): Report: \* Bypass ops: 4096

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### Localram

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@34390002 ps (mmu\_cache.dlocalram): Report: \* Scratchpad statisitics:

@34390002 ps (mmu\_cache.dlocalram): Report: \* -----------------------

@34390002 ps (mmu\_cache.dlocalram): Report: \* Read accesses: 134 (Bytes: 520)

@34390002 ps (mmu\_cache.dlocalram): Report: \* Write accesses: 133 (Bytes: 516) \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

### MMU

## GPTimer

## IRQMP

## SoCWire