

STUDENTS' SPACE ASSOCIATION

THE FACULTY OF POWER AND AERONAUTICAL ENGINEERING

WARSAW UNIVERSITY OF TECHNOLOGY





## INTERFACE CONTROL DOCUMENT

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# Electrical Power System

November 2016

Issue no. 1

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## Changes

Date	Changes	Pages/Section	Responsible
2016-11-30	First issue of the document	Whole document	Piotr Kuligowski
		Mechanical drawings	Mateusz Sobiecki
		Communication protocol	Grzegorz Gajoch
			Dominik Roszkowski

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Published by

Students' Space Association

Warsaw University of Technology, 2016



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Project logo by Krzysztof Karaś

Artist's impressions by Marcin Świetlik



Quote as: PW-Sat2 Team, Phase C Documentation – Critical Design Review – Electrical Power System Interface Control Document, Students' Space Association, Warsaw University of Technology, pw-sat.pl 2016

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	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## Table of contents



1	Introduction	9
1.1	Scope.....	9
1.2	Reference Documents .....	9
1.3	Applicable Project Documents.....	9
2	System overview	10
2.1	MPPT regulators .....	10
2.1.1	ORing diodes for solar panels.....	11
2.1.2	Input EMI filters.....	11
2.1.3	I and V measurements .....	11
2.1.4	Controlled DCDC converter .....	11
2.1.5	ORing diodes to MPB.....	11
2.2	Battery controller .....	12
2.3	Kill-switch circuit .....	12
2.4	Remove before launch circuit .....	12
2.5	DCDC converters for 3V3 and 5V .....	12
2.6	Internal supply .....	12
2.7	Controllers.....	12
2.7.1	Controller A .....	12
2.7.2	Controller B .....	12
2.8	Distribution .....	13
3	Electrical interfaces	15
3.1	Connectors for solar panels.....	15
3.2	Battery pack connector.....	16
3.3	Kill-switch connectors .....	17
3.4	Remove before launch connector.....	18
3.5	PC-104 header.....	19
3.6	ANTenna module connector .....	21
4	Electrical characteristics	23
4.1	MPPT regulators .....	23

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

4.2	Battery controller .....	23
4.3	Distribution RLCLs and LCLs.....	23
4.3.1	Permanent lines.....	24
4.3.2	Subsystem lines.....	24
5	EPS internal modes .....	25
5.1	EPS overheat sub-mode .....	25
6	Communication interfaces .....	26
6.1	I <sup>2</sup> C electrical characteristics.....	26
6.2	Communication protocol.....	27
6.3	Commands .....	27
6.3.1	Perform full power cycle .....	27
6.3.2	Enable LCL .....	28
6.3.3	Disable LCL .....	28
6.3.4	Enable BURN switch.....	28
6.3.5	Disable overheat sub-mode .....	29
6.4	HouseKeeping readout.....	30
6.5	Housekeeping tables .....	31
7	Safety mechanisms .....	36
7.1	EPS redundancy .....	36
7.2	EPS as a watchdog for OBC .....	37
7.3	Battery pack damage .....	37
7.4	Safety mechanisms in low-battery mode .....	37
8	Mechanical interfaces .....	38
8.1	Physical dimensions.....	38
8.2	Mechanical characteristics .....	39
9	Thermal interfaces .....	40
9.1	Power dissipation .....	41
9.2	Temperature sensors .....	41
10	Harness .....	43
11	Storage and Handling .....	44

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

11.1	EPS board.....	44
11.2	EPS as a whole system.....	44
12	Testing	45
12.1	External supply and battery charging.....	45
12.2	Battery pack simulator .....	45

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## List of figures

Figure 1-1 Functional block diagram of the system .....	9
Figure 2-1 Simplified block diagram.....	10
Figure 2-2 MPPT regulators.....	11
Figure 2-3 Distribution for 3V3 lines .....	13
Figure 2-4 Distribution for 5V lines.....	13
Figure 2-5 Distribution for VBAT lines .....	14
Figure 3-1 Connectors placement.....	15
Figure 3-2 Harwin M80-8670805 CAD model .....	16
Figure 3-3 Kill-switch wiring diagram.....	17
Figure 3-4 Harwin M80-8770222 CAD model .....	17
Figure 3-5 RBL switch wiring.....	18
Figure 3-6 Samtec ESQ-126-39-G-D CAD model.....	19
Figure 3-7 Harwin M80-8671005 CAD model .....	22
Figure 5-1 Transitions between EPS internal modes.....	25
Figure 6-1 I <sup>2</sup> C buses on the EPS board .....	26
Figure 7-1 Redundancy diagram for thermal knives .....	36
Figure 8-1 PCB top view.....	38
Figure 8-2 PCB side view .....	38
Figure 9-1 Power dissipation areas on the EPS board .....	40
Figure 12-1 Solar panels simulator for EXT X.....	45
Figure 12-2 Solar panels simulator for EXT Y+ and Y- .....	45
Figure 12-3 Battery pack simulator .....	46

## List of tables

Table 3-1 Solar panels connector specification .....	16
Table 3-2 Connector for X+ and Y- solar panels.....	16
Table 3-3 Connector for X- and Y+ solar panels.....	16
Table 3-4 RBL connector type .....	17
Table 3-5 RBL connector pin-out.....	18
Table 3-6 RBL connector type .....	18
Table 3-7 RBL connector pin-out.....	18
Table 3-8 PC-104 H1/H2 connectors specification .....	19
Table 3-9 PC-104 pins table – H1 .....	20
Table 3-10 PC-104 pins table – H2 .....	21
Table 3-11 ANTenna module connector specification .....	21
Table 3-12 ANTenna module connector pin-out.....	22
Table 4-1 Absolute maximum ratings for MPPT regulators.....	23
Table 4-2 Absolute maximum ratings for battery controller .....	23
Table 4-3 Permanent lines – RLCL protection levels.....	24
Table 4-4 Subsystem lines - LCL protection levels.....	24
Table 6-1 I <sup>2</sup> C electrical characteristics .....	27





	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		



Table 6-2 IDs for LCLs .....	28
Table 6-3 IDs for BURN switches .....	29
Table 6-4 HK values for controller A.....	34
Table 6-5 HK values for controller B.....	35
Table 8-1 Mechanical characteristics .....	39
Table 9-1 Power dissipation depends on input/output power .....	41
Table 9-2 Temperature sensors list.....	42

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

#### Abbreviated terms

ADCS	Attitude Determination and Control System
COMM	Communication subsystem
DT	Deployment Team
EM	Engineering Model
EPS	Electrical Power System
ESA	European Space Agency
FM	Flight Model
GS	Ground Station
LEO	Low Earth Orbit
MA	Mission Analysis
MDR	Mission Definition Review
PDR	Preliminary Design Review
RLCL	Retriggerable Latching Current Limiter.
SC	Spacecraft
SKA	Studenckie Koło Astronautyczne (Students' Space Association)
SSO	Sun-Synchronous Orbit
SW	Software
TBC	To Be Continued
TBD	To Be Defined
WUT	Warsaw University of Technology



	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

# 1 INTRODUCTION

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The PW-Sat2's Electrical Power System (EPS) is responsible for power conversion from solar panels, energy storage in battery and power distribution to subsystems.

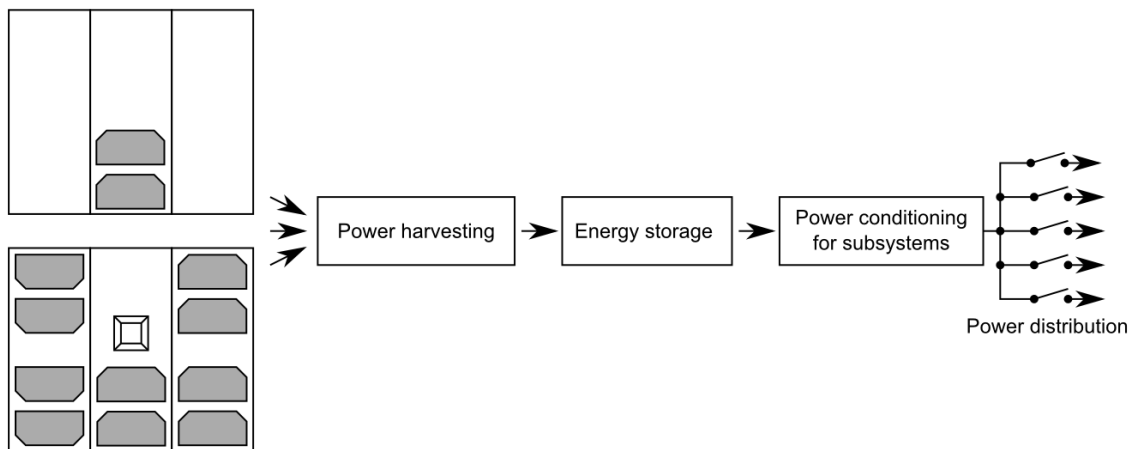


Figure 1-1 Functional block diagram of the system

EPS is designed and it will be built by the EPS team of the PW-Sat2 project.

## 1.1 SCOPE



The aim of this document is to describe all electrical and software interfaces between EPS and rest of the PW-Sat2.

## 1.2 REFERENCE DOCUMENTS

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## 1.3 APPLICABLE PROJECT DOCUMENTS

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	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 2 SYSTEM OVERVIEW

A simplified block diagram shows the main idea of the electrical power system:

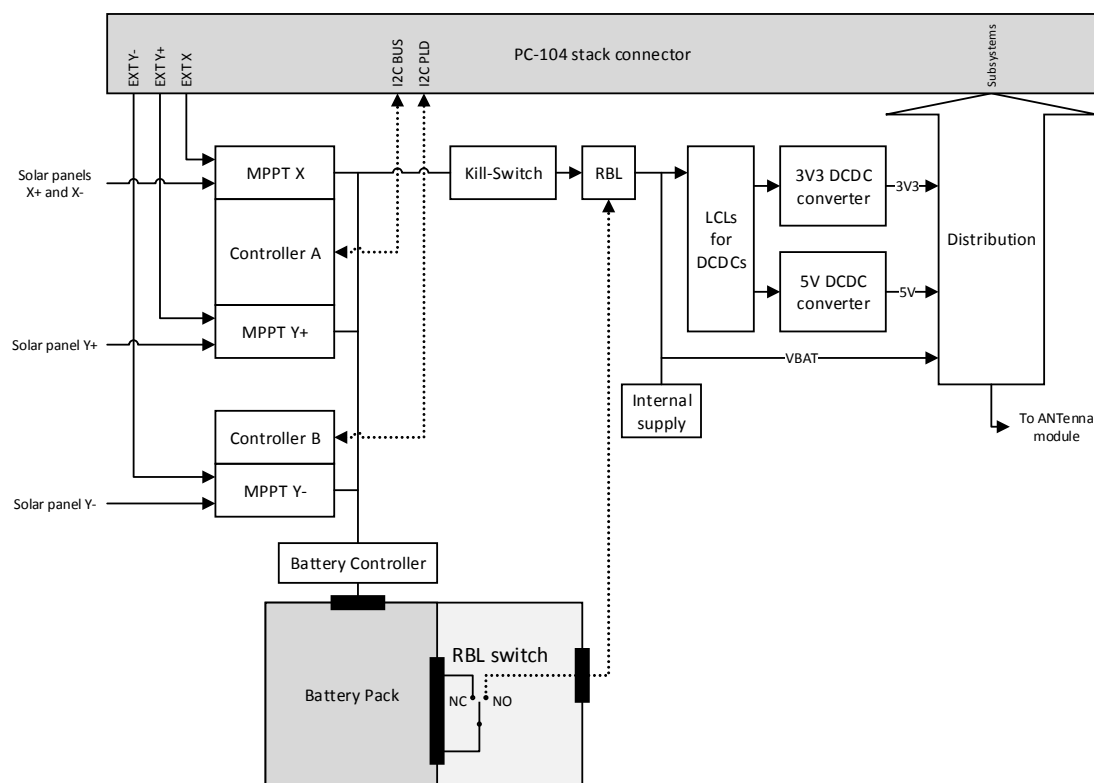




Figure 2-1 Simplified block diagram

### 2.1 MPPT REGULATORS

MPPT regulators are responsible for converting electrical power which is harvested by solar panels. A single MPPT regulator consists of controlled DCDC converter, current and voltage measurement circuits, ADC and DAC converters which are controlled with controller A or B (depends on channel). Solar panels are connected to X+, X-, Y+ and Y- inputs.

In addition, the MPPT regulators may convert electrical power which is provided from EGSE through EXT X, EXT Y+ and EXT Y- inputs. This feature allows to charge the batteries and test the EPS before launch.

Detailed diagram of the MPPT regulators:

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

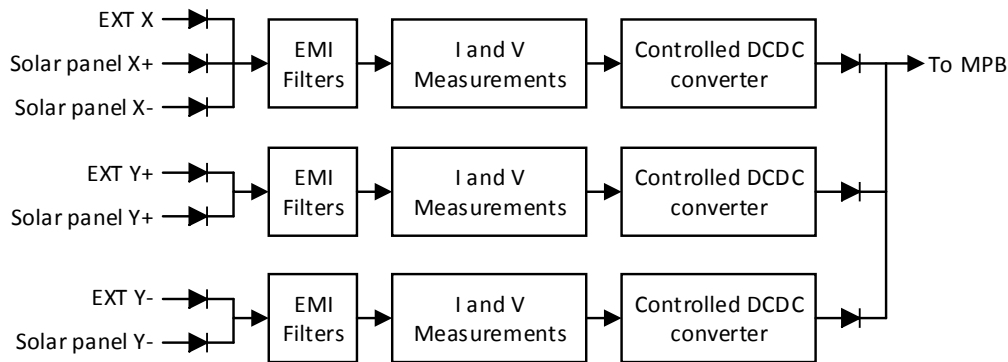


Figure 2-2 MPPT regulators

The controller A is responsible for controlling the MPPT X and MPPT Y+ regulators. The controller B controls the MPPT Y- regulator.

### 2.1.1 ORING DIODES FOR SOLAR PANELS

Four solar panels are connected to three MPPT regulators. Because of X+ and X- solar panels are on the opposite sides they are ORed to a single MPPT regulator. The Y+ and Y- solar panels have two independent MPPT regulators.

### 2.1.2 INPUT EMI FILTERS

To decrease EMI susceptibility of the system, the additional input EMI filters were applied. Both differential mode and common mode filters for solar panels were applied. For EXT supply lines just differential mode filters were applied (in EGSE additional common mode filters should be applied).

### 2.1.3 I AND V MEASUREMENTS



To perform MPPT regulation, the MPPT regulator measures input voltage and current. These values are available in telemetry.

### 2.1.4 CONTROLLED DCDC CONVERTER

This unit contains: a controlled DCDC converter with input and output filters.

### 2.1.5 ORING DIODES TO MPB

There are three ORing diodes, a single diode for a single MPPT regulator. These diodes are responsible for summing MPPT regulators to MPB bus.

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 2.2 BATTERY CONTROLLER

This is a power stage for the battery controller feature. Both Controller A and B are responsible for controlling the power stage. Appropriate algorithms maintain the batteries in the suitable conditions.

## 2.3 KILL-SWITCH CIRCUIT

The kill-switch circuit ensures that the whole system is not active during launch. This circuit consists of two external electro-mechanical switches which are responsible to cut-off subsystems from both battery pack and solar panels.

## 2.4 REMOVE BEFORE LAUNCH CIRCUIT

The RBL circuit ensures that the whole system is not active during transportation and storage. This circuit consists of internal cut-off circuits and external electromechanical switch. The electromechanical switch locks the internal cut-off circuits.

## 2.5 DCDC CONVERTERS FOR 3V3 AND 5V

DCDC converters are responsible for converting VBAT raw voltage to 3.3V and 5V. These voltages are supplied for subsystems to the PC-104 stack connector.

To protect both Main Power Bus (MPB) and DCDC converters, corresponding input LCL are applied.

## 2.6 INTERNAL SUPPLY

This part provides supply voltages to internal EPS' circuits.

## 2.7 CONTROLLERS



There are two independent controllers in the EPS. To increase reliability of the system, they are completely separated from point of view of electrical connections.

### 2.7.1 CONTROLLER A

The controller A is responsible for controlling most of the features of the EPS.

### 2.7.2 CONTROLLER B

Controller B controls redundant thermal knife for Sail and it is responsible for voting with Controller A for critical features.

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 2.8 DISTRIBUTION

Distribution contains current measurements, voltage measurements and RLCLs/LCLs for subsystems. RLCL are permanently turned-on, but LCLs are controlled with controller A. Controller B only controls redundant thermal knife for Sail.

The 3V3 line is supplying the permanent 3V3 bus, SunS, CamWing and CamNadir. LCLs for SunS. The CamWing and CamNadir are turned on/off on demand (on a command from OBC).

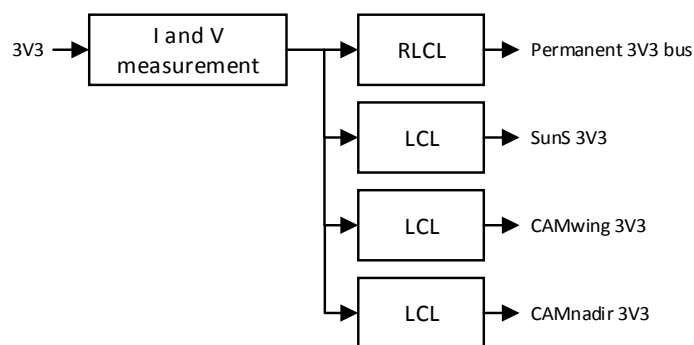


Figure 2-3 Distribution for 3V3 lines

The 5V line is supplying the permanent 5V bus, ANTenna module and SENS line (which supplies all sensors on PLD board). Both ANTenna module and SENS line are turned on/off on demand (on a command from OBC).

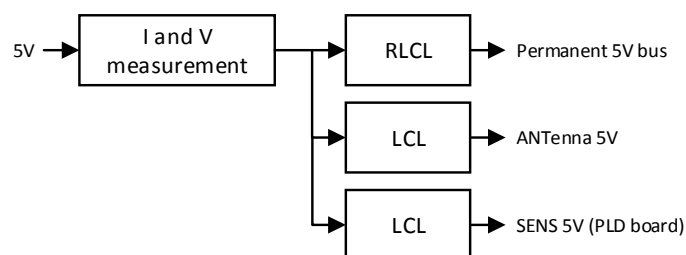




Figure 2-4 Distribution for 5V lines

The VBAT line is connected through a RLCL to the PC-104 stack connector as the permanent VBAT bus. The VBAT bus provides supply voltages to deployment LCLs and switches also.

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

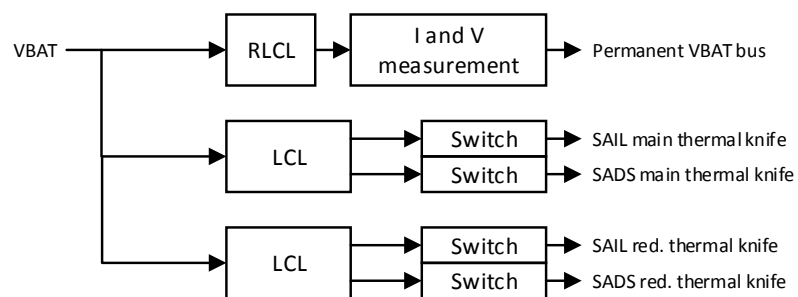


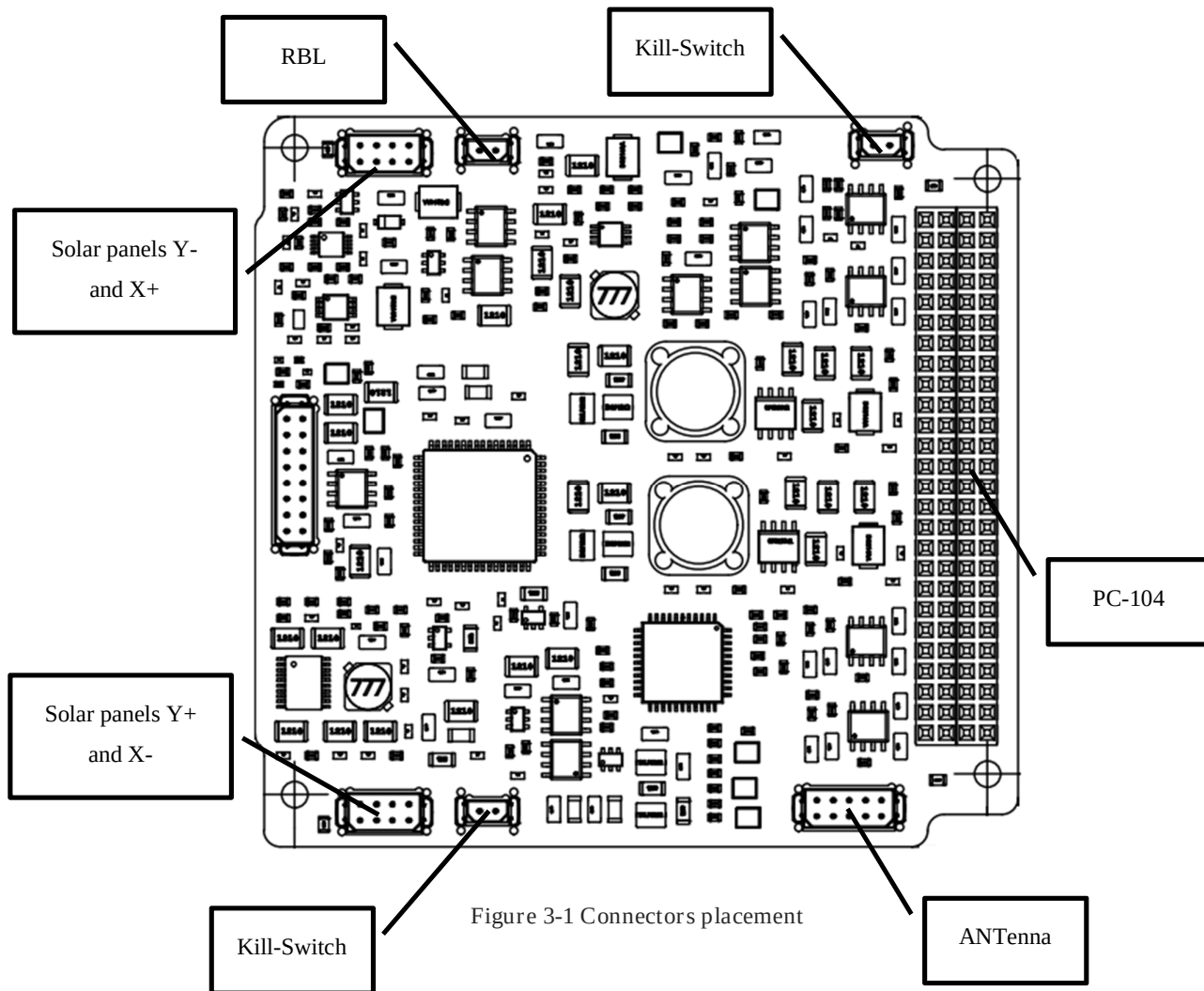


Figure 2-5 Distribution for VBAT lines

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		



### 3 ELECTRICAL INTERFACES



#### 3.1 CONNECTORS FOR SOLAR PANELS

There are four solar panels which have to be connected to the EPS. These solar panels were grouped up to two connectors. These two connectors are the same its Harwin L-Tek M80-8670805. Full specification for a single connector:

Parameter	Value
Manufacturer	Harwin
Manufacturer part number	M80-8670805
Pins count	4 pins per row, double row = 8 pins

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

Pitch 2mm

Mounting Style Through Hole

Table 3-1 Solar panels connector specification

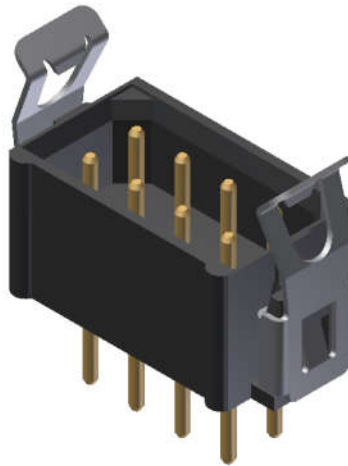


Figure 3-2 Harwin M80-8670805 CAD model

Pin-out definition for a connector for X+ and Y- solar panels:

Pin	Name	Type	Voltage level	Description
1, 5	SolarPanelY-_IN	Power	0 – 12 V	Solar panel power
2, 6	SolarPanelY-_RTN	Power return	0 V	Solar panel power return
3, 7	SolarPanelX+_IN	Power	0 – 6 V	Solar panel power
4, 8	SolarPanelX+_RTN	Power return	0 V	Solar panel power return

Table 3-2 Connector for X+ and Y- solar panels

Pin-out definition for a connector for X- and Y+ solar panels:



Pin	Name	Type	Voltage level	Description
1, 5	SolarPanelY+_IN	Power	0 – 12 V	
2, 6	SolarPanelY+_RTN	Power return	0 V	
3, 7	SolarPanelX-_IN	Power	0 – 6 V	
4, 8	SolarPanelX-_RTN	Power return	0 V	

Table 3-3 Connector for X- and Y+ solar panels

## 3.2 BATTERY PACK CONNECTOR

[TBD]



	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

### 3.3 KILL-SWITCH CONNECTORS

Two SPDT switches are connected through two connectors to the EPS. A wiring diagram:

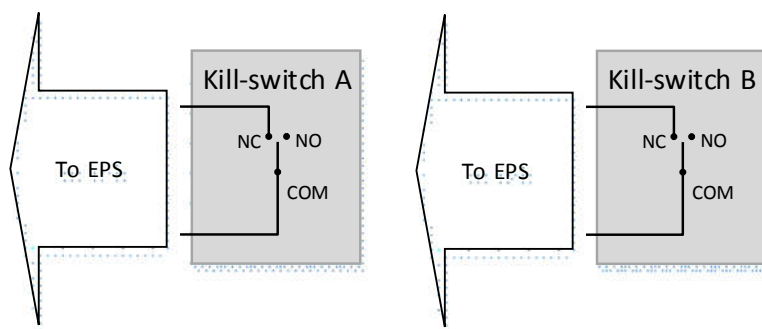


Figure 3-3 Kill-switch wiring diagram

These connectors are the same. Specification data for a single connector:



Parameter	Value
Manufacturer	Harwin
Manufacturer part number	M80-8770222
Pins count	2 pins
Pitch	2mm
Mounting Style	Through Hole

Table 3-4 RBL connector type



Figure 3-4 Harwin M80-8770222 CAD model

Pin-out for a single connector:

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

Pin	Name	Type	Voltage level	Description
1	KILL_COM	Power	0 – 8 V	Ki
2	KILL_NC	Power	0 – 8 V	

Table 3-5 RBL connector pin-out

### 3.4 REMOVE BEFORE LAUNCH CONNECTOR

An SPDT switch is connected to the RBL connector. A wiring diagram:

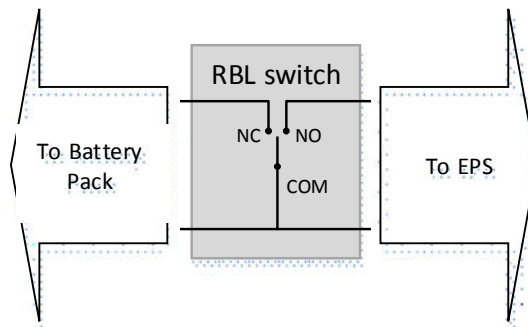


Figure 3-5 RBL switch wiring

RBL connector type on the EPS side:



Parameter	Value
Manufacturer	Harwin
Manufacturer part number	M80-8770222
Pins count	2 pins
Pitch	2mm
Mounting Style	Through Hole

Table 3-6 RBL connector type

RBL connector pin-out on the EPS side:

Pin	Name	Type	Voltage level	Description
1	RBL_COM	Signal GND	0 V	RBL signal GND
2	RBL_NO	Signal	0 – 8 V	RBL signal

Table 3-7 RBL connector pin-out

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

### 3.5 PC-104 HEADER

The PC-104 header consists of two 52-pin connectors: H1 and H2. Full specification for a single connector is shown below:

Parameter	Value
Manufacturer	Samtec
Manufacturer part number	ESQ-126-39-G-D
Pins count	26 pins per row, double row = 52 pins
Pitch	2.54mm
Mounting Style	Through Hole

Table 3-8 PC-104 H1/H2 connectors specification

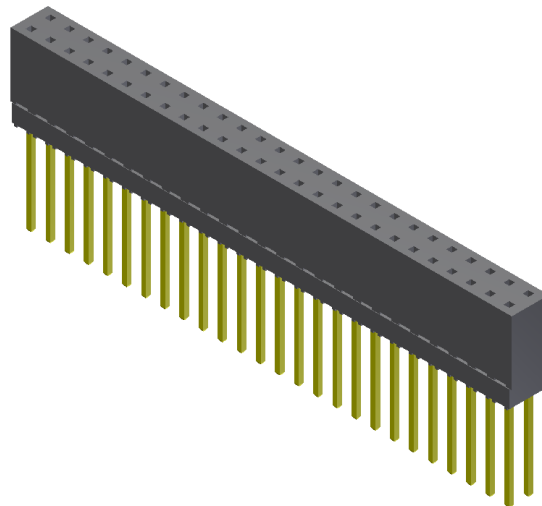




Figure 3-6 Samtec ESQ-126-39-G-D CAD model



Pin-out definition for PC-104/H1:

Pin	Name	Type	Voltage level	Description
H1-13	EXT_X	External supply	0 – 6 V	External power supply for MPPTX.
H1-15	EXT_Y+	External supply	0 – 12 V	External power supply for MPPTY+.
H1-17	EXT_Y-	External supply	0 – 12 V	External power supply for MPPTY-.

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

Pin	Name	Type	Voltage level	Description
H1-21	I2C-PLD_SCL	Digital I/O, bidirectional	0 – 3.3 V	I2C PLD bus, SCL line. 3.3 V voltage level with [TBD] pull-up resistors.
H1-23	I2C-PLD_SDA	Digital I/O, bidirectional	0 – 3.3V	I2C PLD bus, SDA line. 3.3 V voltage level with [TBD] pull-up resistors.
H1-33, H1-34	PGND	Power GND	0 V	Power return line.
H1-35	SENS	5V supply	0 – 5 V	5V supply delivered to SENSors on PLD board. LCL protected.
H1-36	Reserved	Reserved	Reserved	Reserved
H1-37	SAILmain	VBAT supply	0 – 8 V	Main VBAT supply to thermal knife which is placed within SAIL (the SRM mechanism).
H1-38	SAILred	VBAT supply	0 – 8 V	Redundant VBAT supply to thermal knife which is placed within SAIL (the SRM mechanism).
H1-39	SADSmain	VBAT supply	0 – 8 V	Main VBAT supply to thermal knife which is placed within SADS (the SARM mechanism).
H1-40	SADSred	VBAT supply	0 – 8 V	Redundant VBAT supply to thermal knife which is placed within SADS (the SARM mechanism).
H1-41	I2C-BUS_SDA	Digital I/O, bidirectional	0 – 3.3 V	I2C BUS bus, SDA line. 3.3 V voltage level with [TBD] pull-up resistors.
H1-43	I2C-BUS_SCL	Digital I/O, bidirectional	0 – 3.3 V	I2C BUS bus, SCL line. 3.3 V voltage level with [TBD] pull-up resistors.

Table 3-9 PC-104 pins table – H1

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

Pin-out definition for PC-104/H2:

Pin	Name	Type	Voltage level	Description
H2-25, H2-26	5V	Permanent 5V supply	5 V	Permanent 5 V supply line which delivers power supply to bus subsystems. RLCL protected.
H2-27, H2-28	3V3	Permanent 3V3 supply	3.3 V	Permanent 3.3 V supply line which delivers power supply to bus subsystems. RLCL protected.
H2-29, H2-30, H2-32	PGND	Power GND	0 V	Power return line.
H2-31	AGND	Analogue GND	0 V	Analogue return line.
H2-35	CamWing	3.3V supply	0 – 3.3 V	3.3 V supply delivered to CamWing. LCL protected.
H2-37	CamNadir	3.3V supply	0 – 3.3 V	3.3 V supply delivered to CamNadir. LCL protected.
H2-39	SunS	3.3V supply	0 – 3.3 V	3.3 V supply delivered to SunS. LCL protected.
H2-45, H2-46	VBAT	Permanent VBAT supply	6 – 8 V	Permanent VBAT supply line which delivers power supply to bus subsystems. RLCL protected.



Table 3-10 PC-104 pins table – H2

## 3.6 ANTENNA MODULE CONNECTOR

The antenna module is connected directly to EPS. Connector specification for the EPS side:

Parameter	Value
Manufacturer	Harwin
Manufacturer part number	M80-8671005
Pins count	5 pins per row, double row = 10 pins
Pitch	2mm
Mounting Style	Through Hole

Table 3-11 ANTenna module connector specification

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

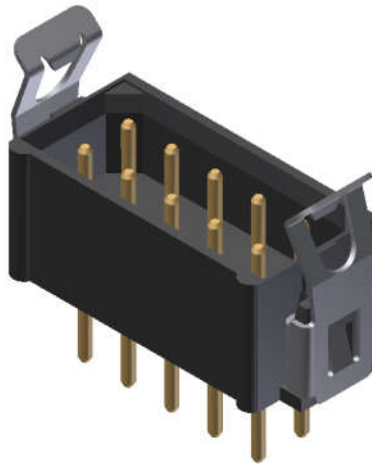




Figure 3-7 Harwin M80-8671005 CAD model

Pin-out definition for a connector on the EPS side:

Pin	Name	Type	Voltage level	Description
1	Vcc	Supply voltage	5V	Black wire
2	SDA_A	Digital I/O, bidirectional	0 – 3.3 V	Brown wire
3	GND	Power GND	0 V	Red wire
4	SDA_B	Digital I/O, bidirectional	0 – 3.3 V	Orange wire
5	GND	Power GND	0 V	Yellow wire
6	Vcc	Supply voltage	5V	Green wire
7	SCL_A	Digital I/O, bidirectional	0 – 3.3 V	Blue wire
8	SCL_B	Digital I/O, bidirectional	0 – 3.3 V	Violet wire
9	GND	Power GND	0 V	Gray wire
10	Not connected	Power GND	0 V	Not connected

Table 3-12 ANTenna module connector pi-out

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 4 ELECTRICAL CHARACTERISTICS

[TODO]

### 4.1 MPPT REGULATORS

There are three MPPT regulators which are responsible for converting electrical power harvested by solar panels. Absolute maximum ratings for the MPPT regulators are listed below. Stresses above these limits can cause permanent damage or it can decrease reliability to the EPS.

Regulator	Parameter	Min	Max	Unit
MPPT X	Input voltage	0	6.5	V
	Input current	0	600	mA
MPPT Y+	Input voltage	0	13	V
	Input current	0	700	mA
MPPT Y-	Input voltage	0	13	V
	Input current	0	700	mA

Table 4-1 Absolute maximum ratings for MPPT regulators

All MPPT regulators are reverse voltage protected. However, it is not recommended to examine this protection.

### 4.2 BATTERY CONTROLLER



Battery controller is responsible for maintaining a battery pack in the suitable conditions. Absolute maximum ratings for the battery controller are listed below.

Parameter	Min	Max	Unit
TBD			

Table 4-2 Absolute maximum ratings for battery controller

### 4.3 DISTRIBUTION RLCLs AND LCLs

Distribution RLCLs and LCLs are responsible for protecting subsystems (and EPS) against short circuits and/or excessive (unpredicted) current consumption. RLCLs are able to perform power cycles. It can help to remove a short circuit (for example due to SEL). LCLs, after a short circuit, switch-off subsystem and exposed a flag to controller. Then OBC may decide what to do.

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

RLCLs are applicable for bus (OBC, ADCS, COMM, etc.), LCLs are applicable for payload (SunS, cameras, PLD board, etc.).

#### 4.3.1 PERMANENT LINES

Permanent lines provide electrical power to subsystems, which belong to the bus group. These lines are always turned-on, unless the battery voltage is below a critical level. Permanent lines are protected with RLCLs with corresponding threshold levels. All threshold levels are listed below:

Supply line	Protection type	IC	Auto-restart time	Settable current limit range	Actual current limit
3V3	RLCL	FPF2700MX	127.5ms	0.4-2A	0.5A +/- 20%
5V	RLCL	FPF2700MX	127.5ms	0.4-2A	1A +/- 20%
VBAT	RLCL	FPF2700MX	127.5ms	0.4-2A	1.54A +/- 20%

Table 4-3 Permanent lines – RLCL protection levels



#### 4.3.2 SUBSYSTEM LINES

Other lines are protected with regular LCLs. Any LCL can be turned on/off on demand (a command from OBC to controller A). All distribution LCL are listed below:

Subsystem	Voltage	Protection type	IC	Settable current limit range	Actual current limit
ANTenna	5V	LCL	FPF2701MX	0.4-2A	1.54A +/- 20%
SunS	3V3	LCL	FPF2701MX	0.4-2A	0.5A +/- 20%
CamNadir	3V3	LCL	FPF2701MX	0.4-2A	0.5A +/- 20%
CamWing	3V3	LCL	FPF2701MX	0.4-2A	0.5A +/- 20%
SENS	5V	LCL	FPF2701MX	0.4-2A	0.5A +/- 20%
TKmain (SAIL and SADS)	VBAT	LCL	FPF2701MX	0.4-2A	1.54A +/- 20%
TKred (SAIL and SADS)	VBAT	LCL	FPF2701MX	0.4-2A	1.54A +/- 20%

Table 4-4 Subsystem lines - LCL protection levels



	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 5 EPS INTERNAL MODES

Just two EPS internal modes were implemented: nominal mode and low-battery mode. Transitions between these modes are completely autonomous. A state diagram for these modes:

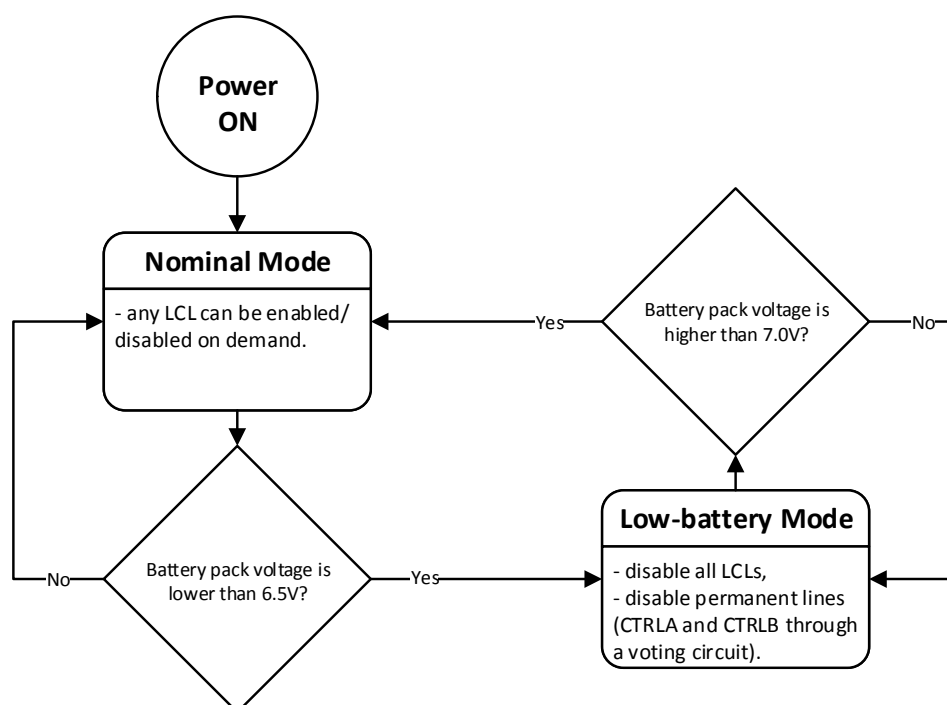




Figure 5-1 Transitions between EPS internal modes

### 5.1 EPS OVERHEAT SUB-MODE

There is a specified EPS sub-mode: overheat sub-mode. This sub-mode is applied when any temperature exceeds a pre-programmed threshold level. This sub-mode works just in nominal mode and all transitions are completely autonomous. There is also a possibility to disable this sub-mode on demand.

After entering into the overheat sub-mode, EPS disables all LCLs and next it goes to nominal mode. After this it waits for next commands. Note that all permanent lines are still active.

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 6 COMMUNICATION INTERFACES

To communicate with OBC, the EPS board has two I<sup>2</sup>C communication interfaces: I2C-BUS (slave) and I2C-PLD (slave). These buses are completely separated. The I2C-BUS bus is connected to the controller A, but the I2C-PLD bus is connected to the controller B on the EPS board.

A block diagram of the I<sup>2</sup>C buses on the EPS board is shown below:

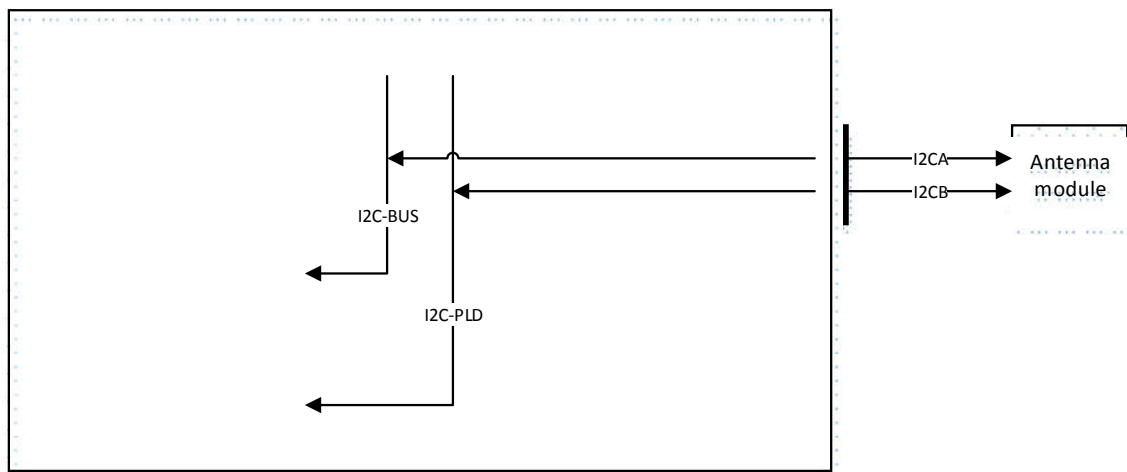


Figure 6-1 I<sup>2</sup>C buses on the EPS board



The Antenna module has built-in, same as EPS, I<sup>2</sup>C repeaters its PCA9517A.

The I2C-BUS bus is taken as a main communication bus between OBC and EPS. At nominal conditions, the I2C-PLD is taken as a secondary bus, used in order to get extra telemetry values. For critical features, simultaneous communication through two buses is needed. The I2C-PLD bus may be used as a main bus just in case of failure (note that not all functions are fully redundant).

### 6.1 I<sup>2</sup>C ELECTRICAL CHARACTERISTICS

There are four pull-up resistors at I<sup>2</sup>C buses on the EPS board. For safety reasons, two I<sup>2</sup>C repeaters were applied.

Parameter	Value
I2C-BUS node	slave
I2C-PLD node	slave
I2C-BUS pull-up resistors (SCL and SDA)	3.3 kΩ
I2C-PLD pull-up resistors (SCL and SDA)	3.3 kΩ

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

I2C-BUS logic level	3.3 V
I2C-PLD logic level	3.3 V
I2C-BUS series resistance (SCL and SDA)	100 $\Omega$
I2C-PLD series resistance (SCL and SDA)	100 $\Omega$
I2C-BUS repeater	PCA9517A
I2C-PLD repeater	PCA9517A

Table 6-1 I<sup>2</sup>C electrical characteristics

## 6.2 COMMUNICATION PROTOCOL

EPS has two on-board controllers: Ctrl A and Ctrl B. They act as slaves on I<sup>2</sup>C buses (Ctrl A on BUS I<sup>2</sup>C bus, Ctrl on PLD I<sup>2</sup>C bus).

Communication is split into two parts – commands & housekeeping readout.

EPS address on I<sup>2</sup>C is 0xAF.

## 6.3 COMMANDS

Controller A is responsible for all LCLs, controller B is only in case A is broken – for Sail deployment. Therefore Controller A have a lot more commands then Controller B.

Basic communication scheme:

START + W	COMMAND OPCODE	[optional parameters]	STOP
-----------	----------------	-----------------------	------

TBD



### 6.3.1 PERFORM FULL POWER CYCLE

Opcode	Parameters	Controllers
0xE0	none	A & B

This command should be received by two controllers within 1 second [TBC], otherwise it will be rejected.

If the command has been received by two controllers, an internal commands sequence will be performed:

- Disable LCLs for: thermal knives (SADS and SAIL), SunS, CamNadir, CamWing, SENS and ANT's.
- Simultaneously two controllers send signals to a voting circuit which performs full power cycle.
- Next, two controllers perform power cycle for themselves by watchdog timers overflow.

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

- EPS starts in nominal mode and it waits for next commands.

This commands sequence takes about 3 seconds [TBC].

[TBD]

### 6.3.2 ENABLE LCL

Opcode	Parameters	Controllers
0xE1	1 byte – LCL ID	A & B for “main thermal knives” A for rest

This command enables selected LCL. There are 7 LCLs on the EPS board:

LCL name	Responsible controller	LCL ID	Description
TKmain	A	0x01	LCL for main thermal knives
SunS	A	0x02	LCL for SunS
CamNadir	A	0x03	LCL for CamNadir
CamWing	A	0x04	LCL for CamWing
SENS	A	0x05	LCL for SENSors (on PLD board)
ANTenna	A	0x06	LCL for ANTenna module
TKred	B	0x01	LCL for redundant thermal knives

Table 6-2 IDs for LCLs



### 6.3.3 DISABLE LCL

Opcode	Parameters	Controllers
0xE2	1 byte – LCL ID	A & B for “main thermal knives” A for rest

This command disables selected LCL.

### 6.3.4 ENABLE BURN SWITCH

Opcode	Parameters	Controllers

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

0xE3	1 byte – switch ID	A & B
------	--------------------	-------

It enables selected BURN switch for 5 minutes [TBC].



BURN switch name	Responsible controller	BURN switch ID
SAILmain	A	0x01
SAILred	B	0x01
SADSmain	A	0x02
SADSred	B	0x02

Table 6-3 IDs for BURN switches

### 6.3.5 DISABLE OVERHEAT SUB-MODE

Opcode	Parameters	Controllers
0xE4	none	A

It disables pre-programmed overheat sub-mode. This sub-mode disables all LCLs when any temperature exceeds pre-programmed threshold level. Just a power cycle restores this sub-mode.

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 6.4 HOUSEKEEPING READOUT

HouseKeeping is refreshed internally by EPS and needs to be read out by OBC.

OBC requests for particular register in EPS memory (with auto-increment after each byte), the only exception is first returned byte – it contains error flag register. Second byte is requested one, and next are being read from auto-incremented address counter.

Multi-byte data are send little endian (lowest byte first).



Example data readout (MPPTX\_SOL from Ctrl A):

START (Addr+W)	0x00	REP-START (Addr + R)	Error flag	MPPTX_SOL_SUM (lower byte)	MPPTX_SOL_SUM (upper byte)	STOP
-------------------	------	-------------------------	---------------	-------------------------------	-------------------------------	------

To read multiple channels:

START (Addr+W)	0x00	REP-START (Addr + R)	Error flag	MPPTX_SO L_SUM (lower byte)	MPPTX_SO L_SUM (upper byte)	MPPTX_SO L_VOLT (lower byte)	MPPTX_SO L_VOLT (upper byte)	STOP
-------------------	------	-------------------------	---------------	-----------------------------------	-----------------------------------	------------------------------------	------------------------------------	------



Housekeeping tables are different for both controllers, both of them are written below.

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 6.5 HOUSEKEEPING TABLES



HK table for controller A:

ID	Designator	Sensor type	Data type	Length [bits]	Conversion formula	Unit (after conversion)	Accuracy	Priority
MPPT X								
0x00	MPPTX_SOL_SUM	2x STAT lines @ 2xLTC4412	2 flags	2	[TBD]	NA	NA	Medium
0x02	MPPTX_SOL_VOLT	12 bit ADC + resistor divider	uint 16-bit	12	[TBD]	V	[TBD]	High
0x04	MPPTX_SOL_CURR	12 bit ADC + shunt resistor + MAX4372F	uint 16-bit	12	[TBD]	mA	[TBD]	High
0x06	MPPTX_OUT_VOLT	12 bit ADC + resistor divider	uint 16-bit	12	[TBD]	V	[TBD]	Medium
0x08	MPPTX_TEMP	12 bit ADC + LMT87	uint 16-bit	12	[TBD]	°C	[TBD]	High
0x0A	MPPTX_STATE	MPPT algorithms state	6 flags	6	[TBD]	NA	NA	High
MPPT Y+								
0x0C	MPPTY+_SOL_SUM	STAT line @ LTC4412	1 flag	1	[TBD]	NA	NA	Medium
0x0E	MPPTY+_SOL_CURR	12 bit ADC + shunt resistor + MAX4372F	uint 16-bit	12	[TBD]	mA	[TBD]	High
0x10	MPPTY+_SOL_VOLT	12 bit ADC + resistor divider	uint 16-bit	12	[TBD]	V	[TBD]	High
0x12	MPPTY+_OUT_VOLT	12 bit ADC + resistor divider	uint 16-bit	12	[TBD]	V	[TBD]	Medium
0x14	MPPTY+_TEMP	12 bit ADC + LMT87	uint 16-bit	12	[TBD]	°C	[TBD]	High
0x16	MPPTY+_STATE	MPPT algorithms state	6 flags	6	[TBD]	NA	NA	High



	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

ID	Designator	Sensor type	Data type	Length [bits]	Conversion formula	Unit (after conversion)	Accuracy	Priority
MPB								
0x18	MPB_VOLT	10 bit ADC + resistor divider	uint 16-bit	10	[TBD]	V	[TBD]	High
Distribution								
0x1A	DISTR_TEMP	10 bit ADC + LMT87	uint 16-bit	12	[TBD]	°C	[TBD]	High
0x1A	DISTR_3V3_VOLT	10 bit ADC + resistor divider	uint 16-bit	10	[TBD]	V	[TBD]	High
0x1C	DISTR_3V3_CURR	10 bit ADC + shunt resistor + MAX4372F	uint 16-bit	10	[TBD]	mA	[TBD]	High
0x1E	DISTR_5V_VOLT	10 bit ADC + resistor divider	uint 16-bit	10	[TBD]	V	[TBD]	High
0x20	DISTR_5V_CURR	10 bit ADC + shunt resistor + MAX4372F	uint 16-bit	10	[TBD]	mA	[TBD]	High
0x22	DISTR_VBAT_VOLT	10 bit ADC + resistor divider	uint 16-bit	10	[TBD]	V	[TBD]	High
0x24	DISTR_VBAT_CURR	10 bit ADC + shunt resistor + MAX4372F	uint 16-bit	10	[TBD]	mA	[TBD]	High
0x26	DISTR_LCL_STATE	LCL's states (ON state @ FPF2701MX)	8 flags	8	[TBD]	NA	NA	High
0x28	DISTR_LCL_FLAGB	FLAGB for LCLs (FlagB state @ FPF2701MX)	8 flags	8	[TBD]	NA	NA	High
Battery controller								
0x2A	BATC_VOLT-0	10 bit ADC + resistor divider	uint 16-bit	10	[TBD]	V	[TBD]	High



	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

ID	Designator	Sensor type	Data type	Length [bits]	Conversion formula	Unit (after conversion)	Accuracy	Priority
0x2C	BATC_CHRG_CURR	10 bit ADC + shunt resistor + MAX4372F	uint 16-bit	10	[TBD]	mA	[TBD]	High
0x2E	BATC_DCHRG_CURR	10 bit ADC + shunt resistor + MAX4372F	uint 16-bit	10	[TBD]	mA	[TBD]	High
0x30	BATC_TEMP-0	10 bit ADC + LMT87	uint 16-bit	12	[TBD]	°C	[TBD]	High
0x32	BATC_STATE	Internal states	8 flags	8	[TBD]	NA	NA	Medium
Battery pack								
0x34	BP_TEMP-0	SPI temperature sensor: TMP121	uint 16-bit	12	[TBD]	°C	[TBD]	High
0x36	BP_TEMP-1	SPI temperature sensor: TMP121	uint 16-bit	12	[TBD]	°C	[TBD]	High
Controller B								
0x38	CTRLB_3V3a_VOLT	10 bit ADC + resistor divider	uint 16-bit	10	[TBD]	V	[TBD]	High
0x3A	CTRLB_3V3d_VOLT	10 bit ADC + resistor divider	uint 16-bit	10	[TBD]	V	[TBD]	High
Controller A								
0x3C	CTRLA_ERR	8 bit error code	uint 8-bit	8	[TBD]	NA	NA	High
0x3E	CTRLA_PWR-CYCLES	Number of power cycles for controller A	uint 16-bit	16	[TBD]	NA	NA	High
0x40	CTRLA_UPTIME	Controller A internal timer	uint 32-bit	32	[TBD]	seconds	[TBD]	High
0x44	CTRLA_TEMP	10 bit ADC + LMT87	uint 16-bit	12	[TBD]	°C	[TBD]	High



	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

ID	Designator	Sensor type	Data type	Length [bits]	Conversion formula	Unit (after conversion)	Accuracy	Priority
3.3 V DCDC converter								
0x46	3V3_TEMP	10 bit ADC + LMT87	uint 16-bit	12	[TBD]	°C	[TBD]	High
5 V DCDC regulator								
0x48	5V_TEMP	10 bit ADC + LMT87	uint 16-bit	12	[TBD]	°C	[TBD]	High

Table 6-4 HK values for controller A



HK table for controller B:

ID	Designator	Sensor type	Data type	Length [bits]	Conversion formula	Unit (after conversion)	Accuracy	Priority
MPPT Y-								
0x00	MPPTY-_SOL_SUM	STAT line @ LTC4412	1 flag	1	[TBD]	NA	NA	Medium
0x02	MPPTY-_SOL_CURR	12 bit ADC + shunt resistor + MAX4372F	uint 16-bit	12	[TBD]	mA	[TBD]	High
0x04	MPPTY-_SOL_VOLT	12 bit ADC + resistor divider	uint 16-bit	12	[TBD]	V	[TBD]	High
0x06	MPPTY-_OUT_VOLT	12 bit ADC + resistor divider	uint 16-bit	12	[TBD]	V	[TBD]	Medium
0x08	MPPTY-_TEMP	12 bit ADC + LMT87	uint 16-bit	12	[TBD]	°C	[TBD]	High
0x0A	MPPTY-_STATE	MPPT algorithms state	6 flags	6	[TBD]	NA	NA	Medium
MPB								
0x0C	MPB_VOLT	10 bit ADC + resistor divider	uint 16-bit	10	[TBD]	V	[TBD]	High

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

ID	Designator	Sensor type	Data type	Length [bits]	Conversion formula	Unit (after conversion)	Accuracy	Priority
Battery controller								
0x0E	BATC_VOLT-1	10 bit ADC + resistor divider	uint 16-bit	10	[TBD]	V	[TBD]	High
0x10	BATC_TEMP-1	[TBD]	[TBD]	[TBD]	[TBD]	[TBD]	[TBD]	High
Controller A								
0x12	CTRLA_3V3a_VOLT	10 bit ADC + resistor divider	uint 16-bit	10	[TBD]	V	[TBD]	High
0x14	CTRLA_3V3d_VOLT	10 bit ADC + resistor divider	uint 16-bit	10	[TBD]	V	[TBD]	High
Controller B								
0x16	CTRLB_ERR	8 bit error code	uint 8-bit	8	[TBD]	NA	NA	High
0x18	CTRLB_PWR-CYCLES	Number of power cycles for controller B	uint 16-bit	16	[TBD]	NA	NA	High
0x1C	CTRLB_UPTIME	Controller B internal timer	uint 32-bit	32	[TBD]	seconds	[TBD]	High
0x20	CTRLB_TEMP	10 bit ADC + LMT87	uint 16-bit	12	[TBD]	°C	[TBD]	High

Table 6-5 HK values for controller B

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 7 SAFETY MECHANISMS

EPS system should protect the main purpose of the PW-Sat2 mission: to open SAIL. We implemented few simple safety mechanisms built-in EPS system. In case of failure of OBC or in case of permanent damage of supply lines, the EPS performs emergency SAIL deployment sequence.

### 7.1 EPS REDUNDANCY

Due to lack of space on the EPS board, there is no possibility to implement full redundancy for all EPS circuits. We implemented simple redundancy. In case of failure, this redundancy is enough to perform emergency SAIL deployment sequence.

Both SAIL and SADS release mechanisms contain redundant thermal knives. We implemented redundant power electronics within EPS system also. As mentioned before, there are two controllers (A and B). These controllers control two LCLs and four BURN switches independently:

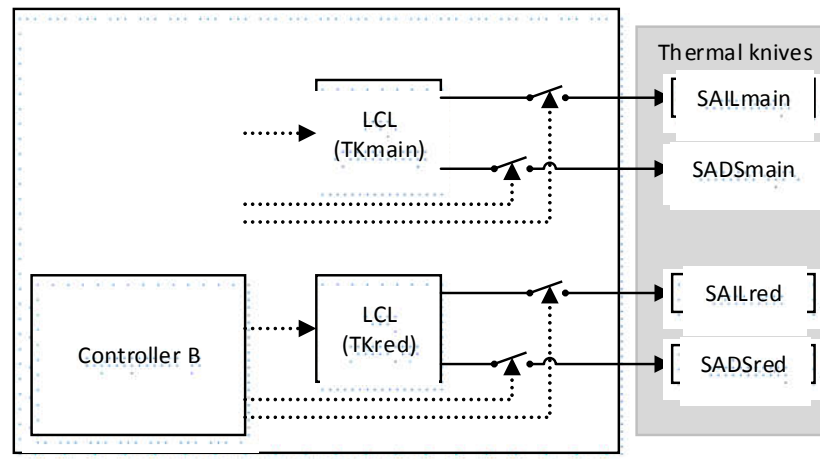




Figure 7-1 Redundancy diagram for thermal knives

To open SAIL, a specified commands sequence is needed. These commands can be triggered autonomously (EPS safety mechanisms) or on demand. To open SAIL by OBC, these commands have to be send to EPS (to controller A or B):

- Enable selected LCL for thermal knives.
- Enable selected BURN switch for SAIL (or SADS).

The second command should be send within 5 minutes [TBC].

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 7.2 EPS AS A WATCHDOG FOR OBC

EPS should be queried for HK values at least once per 5 minutes [TBC]. If OBC does not ask for HK values within 5 minutes [TBC], this means that there is something wrong. Then EPS should perform full power cycles. If it does not give any effect (many power cycles were performed), after 16 hours [TBC] EPS should perform emergency SAIL deployment sequence.

Full power cycle command, in every 5 minutes [TBC], can be executed by at least two controllers (through a voting circuit). Emergency SAIL deployment sequence, after 16 hours [TBC], can be performed by any controller.

## 7.3 BATTERY PACK DAMAGE

In case of battery pack damage, EPS performs emergency SAIL deployment sequence.



If battery voltage drops below 4.5 V [TBC] this means that its damaged. Then controllers are waiting for 5 minutes [TBC] and then they are cutting-off damaged battery pack. After this, EPS performs emergency SAIL deployment sequence.

Of course, if there is no sunlight during this sequence, it turns on and off itself in every 5 minutes [TBC]. After entering in sunlight, it performs emergency SAIL deployment sequence.

Any controller can detect this accident and perform emergency SAIL deployment sequence. To cut-off battery pack from MPB, two controllers have to detect this accident.

## 7.4 SAFETY MECHANISMS IN LOW-BATTERY MODE

All safety mechanisms are working properly in the low-battery mode. Of course, a power cycle command does not any effect, because all LCLs and all permanent lines are disabled. During this mode EPS counts 16 hours [TBC] to perform emergency SAIL deployment sequence. This means that the maximum time in low-battery mode should be lower than 16 hours [TBC].

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 8 MECHANICAL INTERFACES

### 8.1 PHYSICAL DIMENSIONS

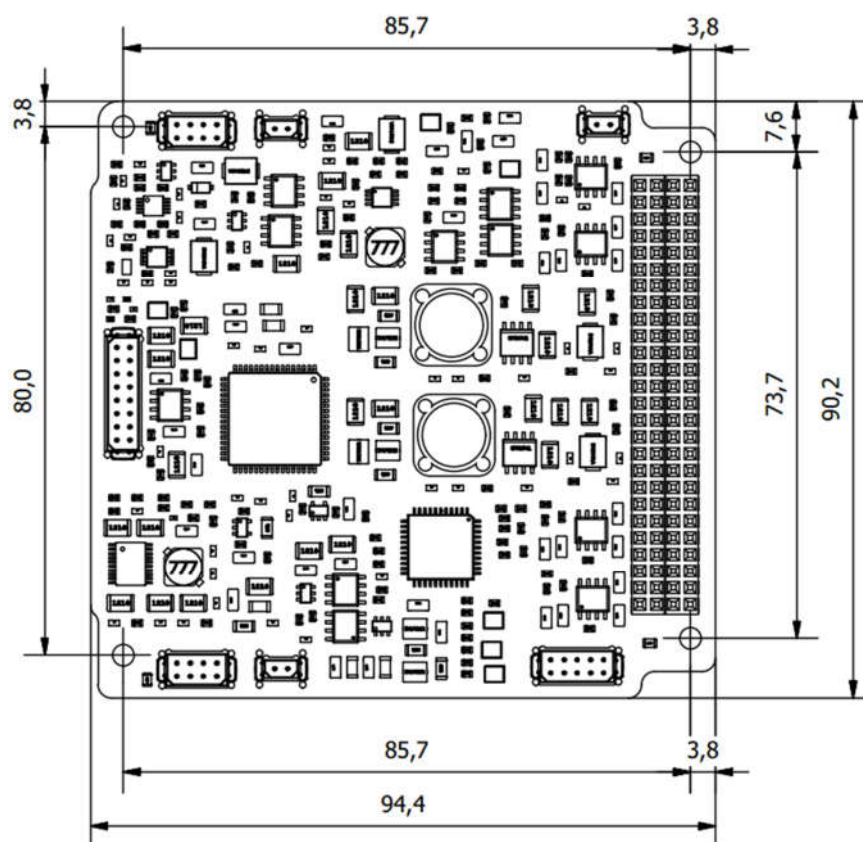


Figure 8-1 PCB top view

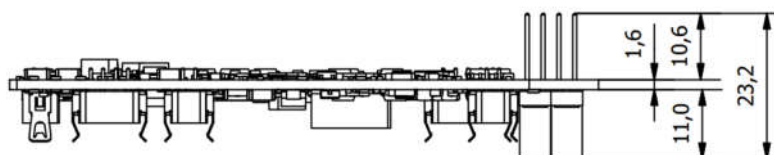






Figure 8-2 PCB side view

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 8.2 MECHANICAL CHARACTERISTICS

Parameter	Unit	Value
Max weight	g	110
PCB thickness	mm	1.55 +/- 10%

Table 8-1 Mechanical characteristics

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 9 THERMAL INTERFACES

The EPS board has been divided to 9 areas. These areas are different from point of view of power dissipations.

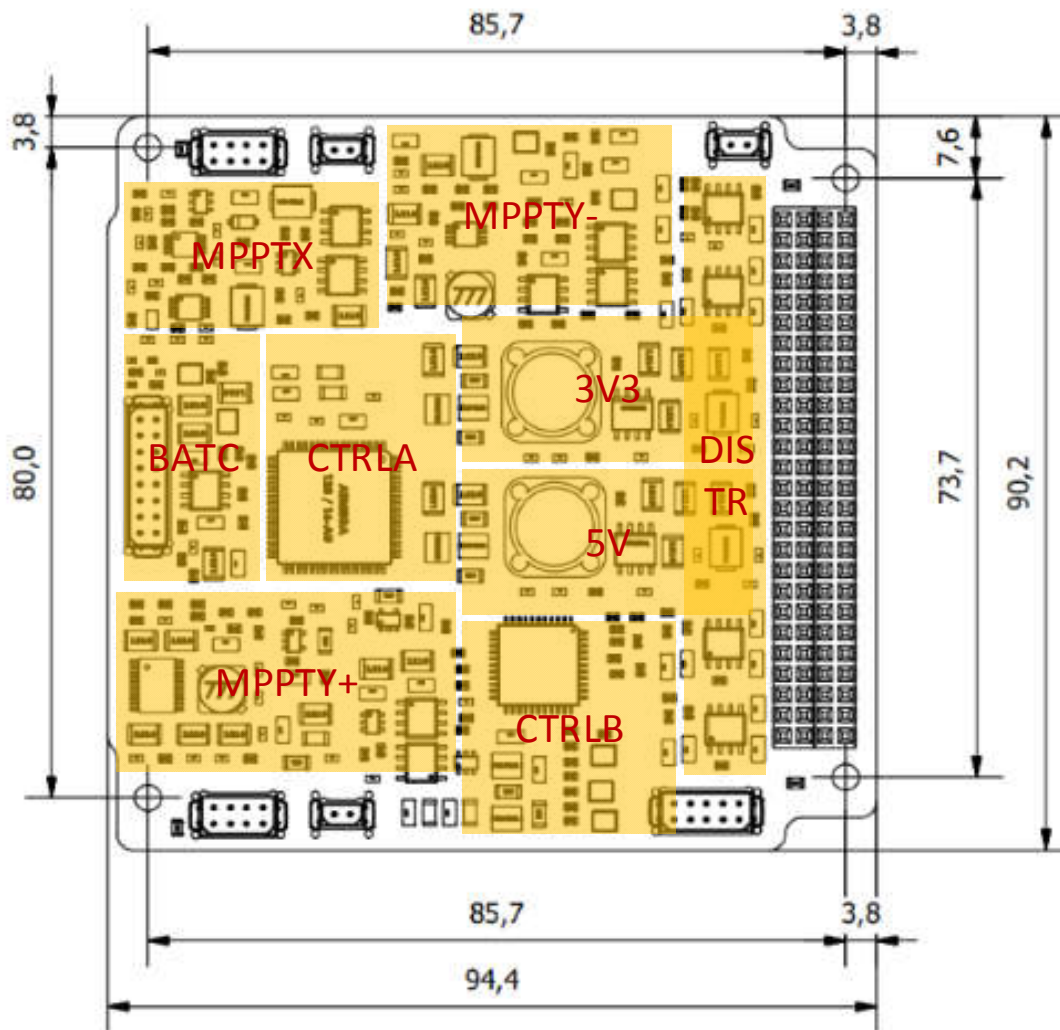




Figure 9-1 Power dissipation areas on the EPS board



	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 9.1 POWER DISSIPATION



EPS part	Power dissipation [W] @ 10W input power to MPPTs (SunPointing) and 1W load.	Power dissipation [W] @ no input power (eclipse). 1W load.	Power dissipation [W] @ 10W input power (SunPointing) and 10W load
MPPTX	0.4	0	0.4
MPPTY+	0.8	0	0.8
MPPTY-	0.8	0	0.8
BATC	0.1	0.1	0.2
3V3	0.1	0.1	1
5V	0.1	0.1	1
DISTR	0.1	0.1	0.1
CTRLA	0.01	0.01	0.01
CTRLB	0.01	0.01	0.01

Table 9-1 Power dissipation depends on input/output power

## 9.2 TEMPERATURE SENSORS

All temperatures are collected as a reply for a full HK values request. Temperature sensors list is shown below:

HK designator	Location	Accuracy
MPPTX_TEMP	MPPT X regulator	
MPPTY+_TEMP	MPPT Y+ regulator	
MPPTY-_TEMP	MPPT Y- regulator	
DISTR_TEMP	Distribution	
BATC_TEMP-0	Battery controller	+/- 3°C
BATC_TEMP-1		
CTRLA_TEMP	Controller A	
CTRLB_TEMP	Controller B	
3V3_TEMP	3.3 V DCDC converter	
5V_TEMP	5 V DCDC converter	

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

BP\_TEMP-0



Battery pack

+/- 2°C

BP\_TEMP-1

---

Table 9-2 Temperature sensors list



	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 10 HARNESS

---

Harness will be designed after the STM model integration.

[TBD]

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 11 STORAGE AND HANDLING

---

### 11.1 EPS BOARD



The EPS FM board (with no battery pack) should be stored in a cleanroom conditions (i.e. ISO 8) or in a sealed container. It does not require special handling.

### 11.2 EPS AS A WHOLE SYSTEM

The EPS as a whole system, this means:

- solar panels,
- battery pack,
- EPS board,

should be stored in special conditions and it requires special handling. Solar panels are very fragile and they require a special MGSE for storage. To maintain the battery pack capacity it needs periodic recharging. Intervals between recharging depend on both RBLs and Kill-Switches. Battery pack can survive up to 6 months when RBLs or Kill-Switches deactivate the EPS. Recharging intervals should be lower than 3 months.

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

## 12 TESTING

### 12.1 EXTERNAL SUPPLY AND BATTERY CHARGING

To battery charging during testing, at least one external supply voltage should be connected to EXT X, EXT Y+ or EXT Y- lines. These lines are available on the PC-104 header. For return the PGND line should be used.

These lines are directly connected to MPPT regulators. This means that an external power supply should be able to simulate solar panels. You can use a standard power supply in constant current source mode with external rectifier (i.e. 1N4007) diodes.

Solar panels simulator for the EXT X input:

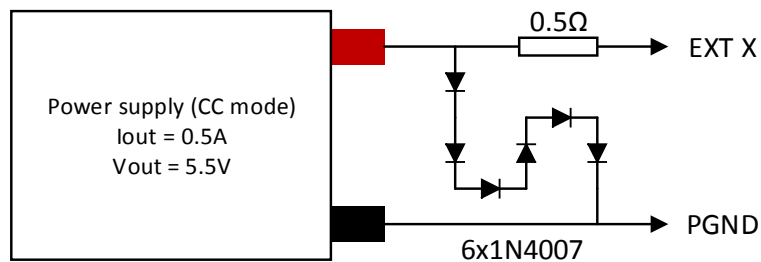


Figure 12-1 Solar panels simulator for EXT X

Solar panels simulator for both EXT Y+ and EXT Y- inputs:

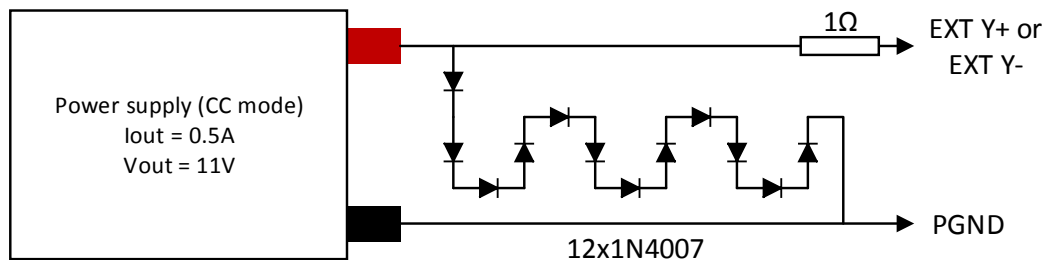




Figure 12-2 Solar panels simulator for EXT Y+ and Y-

The power supply can be controlled with a PC through an opto-isolated RS232 interface. To simulate sunlight intensity changing, the constant current should be regulated in range between 0 to 500mA.

### 12.2 BATTERY PACK SIMULATOR

To simulate battery pack a power supply and a power resistor can be used. This feature may be useful during a test campaign.

	PW-Sat2	Interface Control Document	
	2016-11-30	Electrical Power System	
	Phase C		

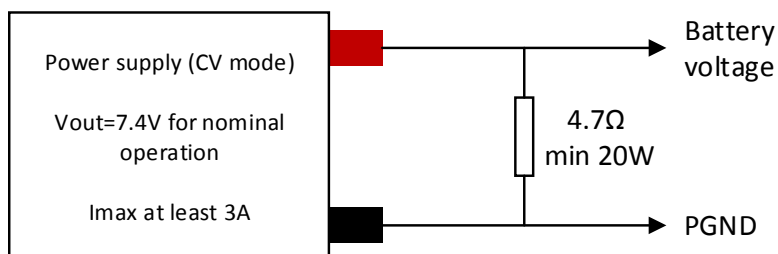


Figure 12-3 Battery pack simulator

There is possibility to simulate battery charging/discharging and all protections using this circuit. To simulate charging/discharging, the power supply voltage should be changed in range between 6.5 and 8 V. Lower or higher voltages can activate other protections.