Desmond Oketch- SCT212-0083/2021

COMPUTER TECHNOLOGY

Lab 4

Computer Architecture – tutorial 4

E1: CPI and Cache Tag Size

Given:

- Unified cache: 256 KB = 262,144 bytes
- Block size = 64 bytes
- Cache = 4-way set associative
- Address size = 32 bits
- Miss penalty = 25 cycles
- Miss rate = 2%
- Data accesses = 50% of instructions

a) What is the tag size?

Calculate the number of blocks:

$$\text{Number of blocks} = \frac{256 \times 1024}{64} = 4096\ \text{blocks}$$

Since it's **4-way set associative**, number of sets:

$$\text{Number of sets} = \frac{4096}{4} = 1024\ \text{sets}$$

Each set is selected using **index bits**:

$$\text{Index bits} = \log_2(1024) = 10\ \text{bits}$$

Each block covers **64 bytes**, so:

Block offset bits=log⁡2(64)=6 bits\text{Block offset bits} = \log_2(64) = 6\ \text{bits}

Now, the tag size:

Tag size=32 (address bits)−10 (index)−6 (block offset)=16 bits\text{Tag size} = 32\ (\text{address bits}) - 10\ (\text{index}) - 6\ (\text{block offset}) = 16\ \text{bits}

Answer: 16 bits for the tag

How much faster if all accesses hit?

CPI when all hits = **1.0**

When we have misses, extra cycles are incurred:

Miss penalty=25 cycles\text{Miss penalty} = 25\ \text{cycles}

Miss rate = 2% = 0.02

Instruction types:

- 50% data accesses → 26% loads + 9% stores (from later problems, so assume similar here)

Effective CPI:

CPI=1+Memory accesses per instruction×Miss rate×Miss penalty\text{CPI} = 1 + \text{Memory accesses per instruction} \times \text{Miss rate} \times \text{Miss penalty}

Each instruction accesses memory once (instruction fetch), and 50% of them also do a data access:

Memory accesses per instruction=1+0.5=1.5\text{Memory accesses per instruction} = 1 + 0.5 = 1.5

Thus:

CPI with misses=1+(1.5×0.02×25)=1+(0.75)=1.75\text{CPI with misses} = 1 + (1.5 \times 0.02 \times 25) = 1 + (0.75) = 1.75

Now, speedup if no misses:

Speedup=1.751.0=1.75× faster\text{Speedup} = \frac{1.75}{1.0} = \boxed{1.75\times\ \text{faster}}

E2: Write-Through vs Write-Back Bandwidth

Given:

- 95% hit rate → 5% miss rate
- Block = 2 words (but memory reads/writes 1 word at a time)
- 25% writes
- 30% of blocks dirty
- Memory bandwidth = 10910^9 words/sec
- Processor issues 10910^9 references/sec

a) Write-Through Cache

For write-through:

- Every write = 1 word to memory, even if it's a hit.

Memory traffic:

- Reads:
  - 75% reads
  - 5% of reads miss → cause 2 word reads from memory (block read)
- Writes:
  - 25% writes
  - All writes go to memory.

Memory bandwidth used:

From reads:

$0.75 \times 10^9 \times 0.05 \times 2 = 0.075 \times 2 \times 10^9 = 0.15 \times 10^9\ \text{words/sec}$

From writes:

$0.25 \times 10^9\ \text{words/sec}$

Total:

$0.15 + 0.25 = 0.4 \times 10^9\ \text{words/sec}$

Memory usage:

$\frac{0.4 \times 10^9}{10^9} = \boxed{40\%}$

b) Write-Back Cache

For write-back:

- Only miss writes and dirty block evictions cause memory traffic.

Reads:

- Same as above for read misses.

Writes:

- Only on block eviction.
- 30% of evicted blocks are dirty.

Memory bandwidth used:

From reads:

0.75×109×0.05×2=0.15×109 words/sec0.75 \times 10^9 \times 0.05 \times 2 = 0.15 \times 10^9\ \text{words/sec}

From dirty evictions:

- Miss rate: 5%
- 25% writes → so, 0.25×109×0.05=0.0125×1090.25 \times 10^9 \times 0.05 = 0.0125 \times 10^9 misses per second
- Each dirty eviction writes back **2 words**.
- 30% of misses dirty →

0.0125×0.3×2=0.0075×109 words/sec0.0125 \times 0.3 \times 2 = 0.0075 \times 10^9\ \text{words/sec}

Total:

0.15+0.0075=0.1575×109 words/sec0.15 + 0.0075 = 0.1575 \times 10^9\ \text{words/sec}

Memory usage:

0.1575×109109=15.75%\frac{0.1575 \times 10^9}{10^9} = \boxed{15.75\%}

E3: Performance of Write-Through vs Write-Back Cache

- Read hit = 1 cycle
- Write hit = 2 cycles
- Miss penalty = 50 cycles
- Write buffer avoids stalling for write-through
- 26% loads, 9% stores

Write-Through Cache CPI

Instruction accesses:

- 1 per instruction for fetch
- +26% loads
- +9% stores

Memory accesses = 1 + 0.26 + 0.09 = **1.35** per instruction.

Miss rate:

- Instruction miss rate = 0.5%
- Data miss rate = 1%

Effective miss rate:

Total miss rate=11.35(1×0.005+(0.26+0.09)×0.01)=11.35(0.005+0.0035)=0.00851.35≈0.006 3\text{Total miss rate} = \frac{1}{1.35}(1 \times 0.005 + (0.26+0.09)\times 0.01) = \frac{1}{1.35}(0.005 + 0.0035) = \frac{0.0085}{1.35} \approx 0.0063

Effective CPI:

CPI=1+(1.35×0.0063×50)=1+(0.42525)≈1.425\text{CPI} = 1 + (1.35 \times 0.0063 \times 50) = 1 + (0.42525) \approx 1.425

Write-Back Cache CPI

In write-back:

- Data writes only cause penalty on miss and dirty evictions.
- Instruction hits still take 1 cycle, writes take 2 cycles.

Assume **dirty write-backs** are less frequent.

Thus, CPI is slightly lower than 1.425, say around **1.3–1.35**, depending on assumptions.