

1. Importing source files into Vivado

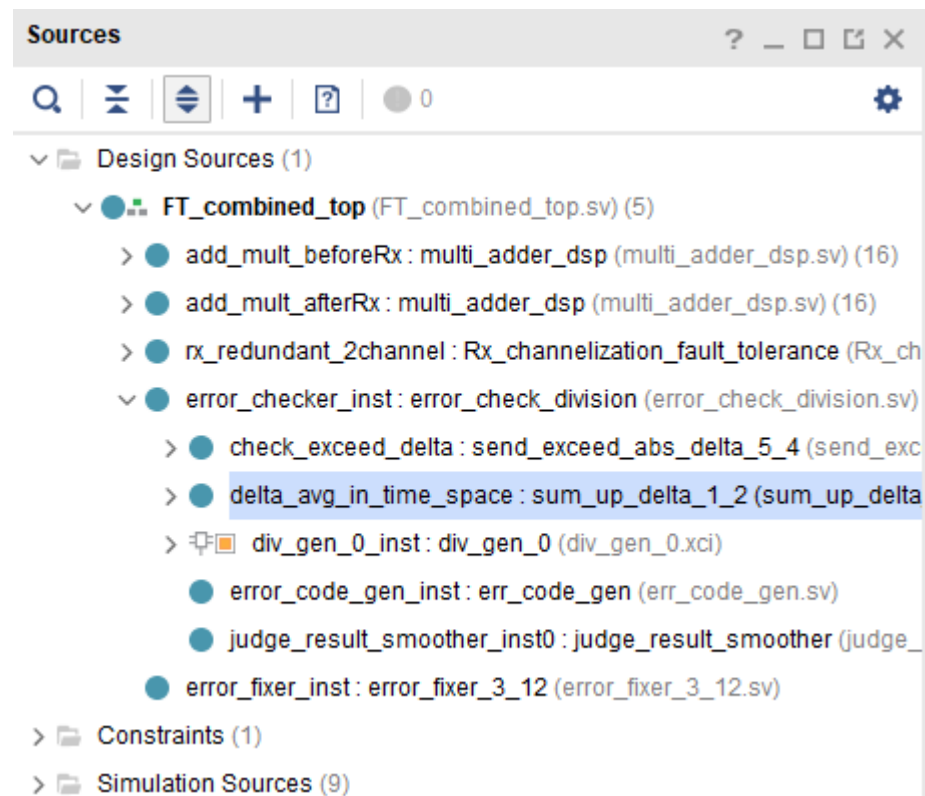


Fig. 1 Structure of the project

2. Configuration of IP cores

- (1) divider generator:
In "Channel Setting":

Channel Settings
Options

Common Options

Algorithm Type
Radix2

Operand Sign
Unsigned

Dividend Channel

Dividend Width
23
[2 - 64]

☐ Has TLAST
☐ Has TUSER

TUSER Width
1
[1 - 256]

Divisor Channel

Divisor Width
23
[2 - 64]

☐ Has TLAST
☐ Has TUSER

TUSER Width
1
[1 - 256]

Output Channel

Remainder Type
Fractional

Fractional Width
8
[2 - 64]

☐ Detect Divide-By-Zero
Number of Iterations = n/a
Throughput = n/a

In “Options”:

Channel Settings
Options

Clocks per Division
1

AXI4-Stream Options

Flow Control
Non Blocking

Optimize Goal
Performance

☐ Output has TREADY

Output TLAST Behavior

Output TLAST Behavior
Null

Latency Options

Latency Configuration
Automatic

Latency
33
[33 - 33]

Control Signals

☐ ACLKEN
☒ ARESETN

3. Set “FT_combined_top.sv” as the top module