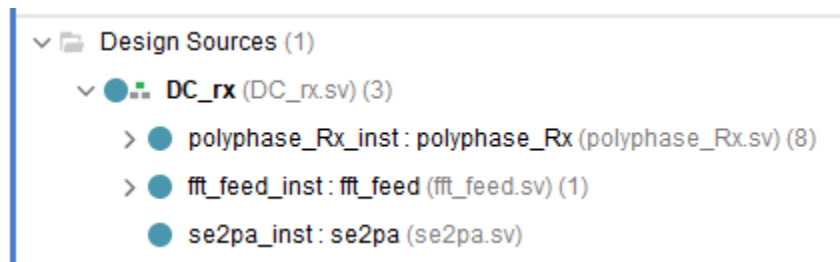


1. Importing source files into Vivado



2. Configuration of IP cores

(1) Filter IP core

“Filter Options”:

The screenshot shows the 'Filter Options' configuration window for the 'fir_Rx_0' component. The window has a tabbed interface with 'Filter Options' selected. The 'Filter Coefficients' section includes a 'Select Source' dropdown set to 'Vector', a 'Coefficient Vector' text field containing a long list of integers, a 'Coefficient File' text field with a file icon, and a 'Number of Coefficient Sets' spinner set to 1. The 'Filter Specification' section includes a 'Filter Type' dropdown set to 'Single Rate', an 'Inferred Coefficient Structure(s)' label set to 'Non Symmetric', a 'Rate Change Type' dropdown set to 'Integer', and three numeric input fields for 'Interpolation Rate Value', 'Decimation Rate Value', and 'Zero Pack Factor', all set to 1.

- Set corresponding coefficient vector

For fir_Rx_0:

-4,-46,7,125,-21,-318,46,698,-101,-1539,248,5467,8191,4804,-232,-1458,95,666,-45,-302,18,117,-7,-44

For fir_Rx_1:

-11,-47,23,128,-64,-322,145,704,-314,-1564,793,6087,8082,4115,-642,-1329,270,610,-126,-275,53,106,-20,-40

For fir_Rx_2:

-18,-46,40,126,-109,-313,248,680,-535,-1525,1393,6650,7866,3414,-977,-
1163,419,536,-195,-240,81,91,-29,-36

For fir_Rx_3:

-24,-42,57,117,-155,-289,350,625,-756,-1418,2039,7141,7550,2717,-1236,-
969,537,448,-249,-200,102,75,-37,-30

For fir_Rx_4:

-30,-37,75,102,-200,-249,448,537,-969,-1236,2717,7550,7141,2039,-1418,-
756,625,350,-289,-155,117,57,-42,-24

For fir_Rx_5:

-36,-29,91,81,-240,-195,536,419,-1163,-977,3414,7866,6650,1393,-1525,-
535,680,248,-313,-109,126,40,-46,-18

For fir_Rx_6:

-40,-20,106,53,-275,-126,610,270,-1329,-642,4115,8082,6087,793,-1564,-
314,704,145,-322,-64,128,23,-47,-11

For fir_Rx_7:

-44,-7,117,18,-302,-45,666,95,-1458,-232,4804,8191,5467,248,-1539,-
101,698,46,-318,-21,125,7,-46,-4

“Channel Specification”:

Filter Options	Channel Specification	Implementation	Detailed Implementation	Interface	Summary
Interleaved Channel Specification					
Channel Sequence		Basic			
Number of Channels		1 [1 - 1024]			
Select Sequence					
Select Sequence		All			
Sequence ID List		P4-0,P4-1,P4-2,P4-3,P4-4			
Parallel Channel Specification					
Number of Paths		2 [1 - 16]			
Hardware Oversampling Specification					
Select Format		Frequency Specification			
Sample Period (Clock Cycles)		1 [1.0 - 1.0E7]			
Input Sampling Frequency (MHz)		0.001 [1.0E-6 - 189952.0]			
Clock Frequency (MHz)		300.0 [4.0E-6 - 742.0]			
Clock cycles per input:		300000			
Clock cycles per output:		300000			
Number of parallel inputs:		1			
Number of parallel outputs:		1			

- Set “Number of Paths” as 2

“Implementation”:

Filter Options | Channel Specification | **Implementation** | Detailed Implementation | Interface | Summary

Coefficient Options

Coefficient Type: Signed

Quantization: Integer Coefficients

Coefficient Width: 16 [14 - 49]

☐ Best Precision Fraction Length

Coefficient Fractional Bits: 0 [0 - 0]

Coefficient Structure

☒ Inferred

☐ Non Symmetric

Data Path Options

Input Data Type: Signed

Input Data Width: 16 [2 - 49]

Input Data Fractional Bits: 0 [0 - 16]

Output Rounding Mode: Non Symmetric Rounding Down

Output Width: 16 [1 - 30]

Output Fractional Bits : 0

- Set “Coefficient Width” as 16
- Set “Output Rounding Mode” as non symmetric rounding down
- Set “Output Width” as 16

“Interface”:

Data Channel Options

TLAST: Not Required

☐ Output TREADY ☒ Input FIFO

TUSER

Input: Not Required Output: Not Required

User Field Width: 1 [1 - 256]

Configuration Channel Options

Synchronization Mode: On Vector

Configuration Method: Single

Reload Channel Options

Reload Slots: 1 [1 - 256]

Control Signals

☒ ARESETn (active low) ☐ ACLKEN

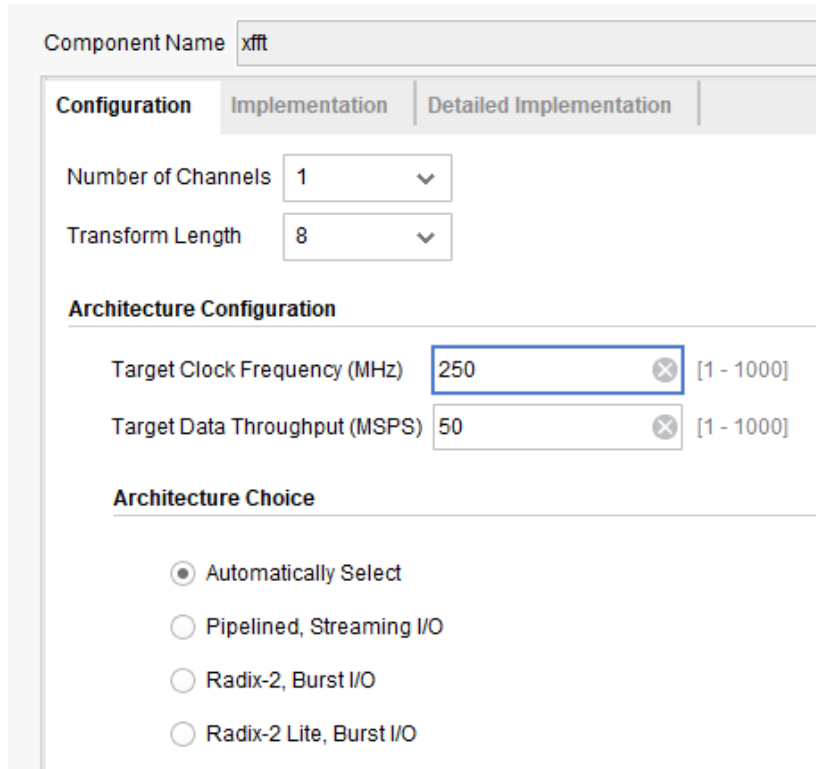
ARESETn must be asserted for a minimum of 2 cycles

☒ Reset Data Vector ☐ Blank Output

- check “ARESETn (active low)” box

(2) FFT IP Core

“Configuration”:



The screenshot shows the 'Configuration' tab of the FFT IP Core configuration window. The 'Component Name' is 'xfft'. Under 'Architecture Configuration', 'Target Clock Frequency (MHz)' is set to 250 and 'Target Data Throughput (MSPS)' is set to 50. Under 'Architecture Choice', 'Automatically Select' is selected.

Component Name: xfft

Configuration | Implementation | Detailed Implementation

Number of Channels: 1

Transform Length: 8

Architecture Configuration

Target Clock Frequency (MHz): 250 [1 - 1000]

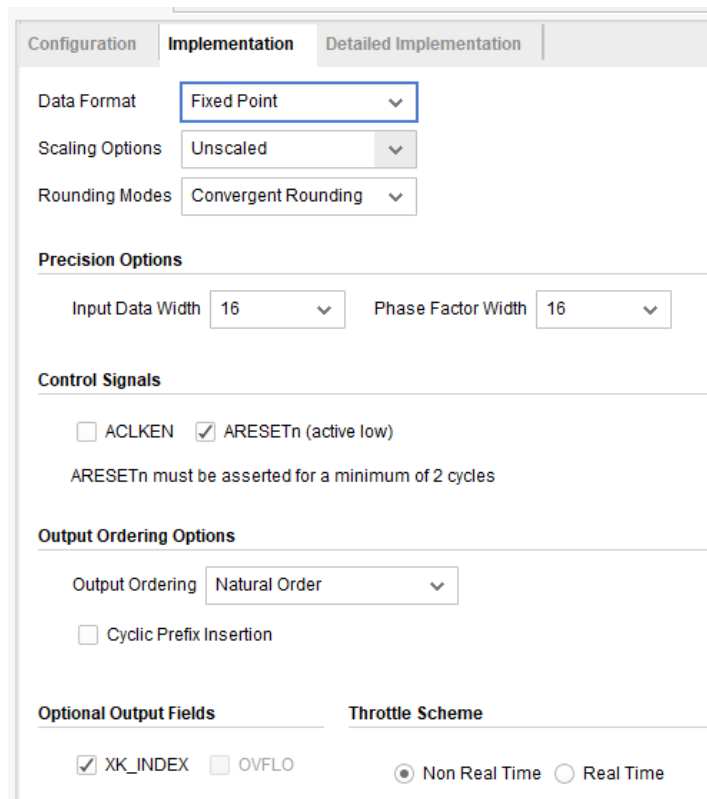
Target Data Throughput (MSPS): 50 [1 - 1000]

Architecture Choice

- ☒ Automatically Select
- ☐ Pipelined, Streaming I/O
- ☐ Radix-2, Burst I/O
- ☐ Radix-2 Lite, Burst I/O

- Set “Transform Length” as 8

“Implementation”:



The screenshot shows the 'Implementation' tab of the FFT IP Core configuration window. 'Data Format' is 'Fixed Point', 'Scaling Options' is 'Unscaled', and 'Rounding Modes' is 'Convergent Rounding'. Under 'Precision Options', 'Input Data Width' and 'Phase Factor Width' are both 16. Under 'Control Signals', 'ARESETn (active low)' is checked. Under 'Output Ordering Options', 'Output Ordering' is 'Natural Order'. Under 'Optional Output Fields', 'XK_INDEX' is checked. Under 'Throttle Scheme', 'Non Real Time' is selected.

Configuration | **Implementation** | Detailed Implementation

Data Format: Fixed Point

Scaling Options: Unscaled

Rounding Modes: Convergent Rounding

Precision Options

Input Data Width: 16 Phase Factor Width: 16

Control Signals

☐ ACLKEN ☒ ARESETn (active low)

ARESETn must be asserted for a minimum of 2 cycles

Output Ordering Options

Output Ordering: Natural Order

☐ Cyclic Prefix Insertion

Optional Output Fields | **Throttle Scheme**

☒ XK_INDEX ☐ OVFO

☒ Non Real Time ☐ Real Time

- Set each parameter as above

3. Set "DC_rx.sv" as the top module