1. **Importing source files into Vivado**

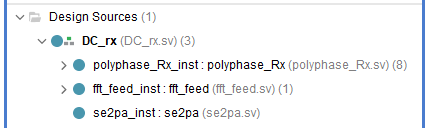
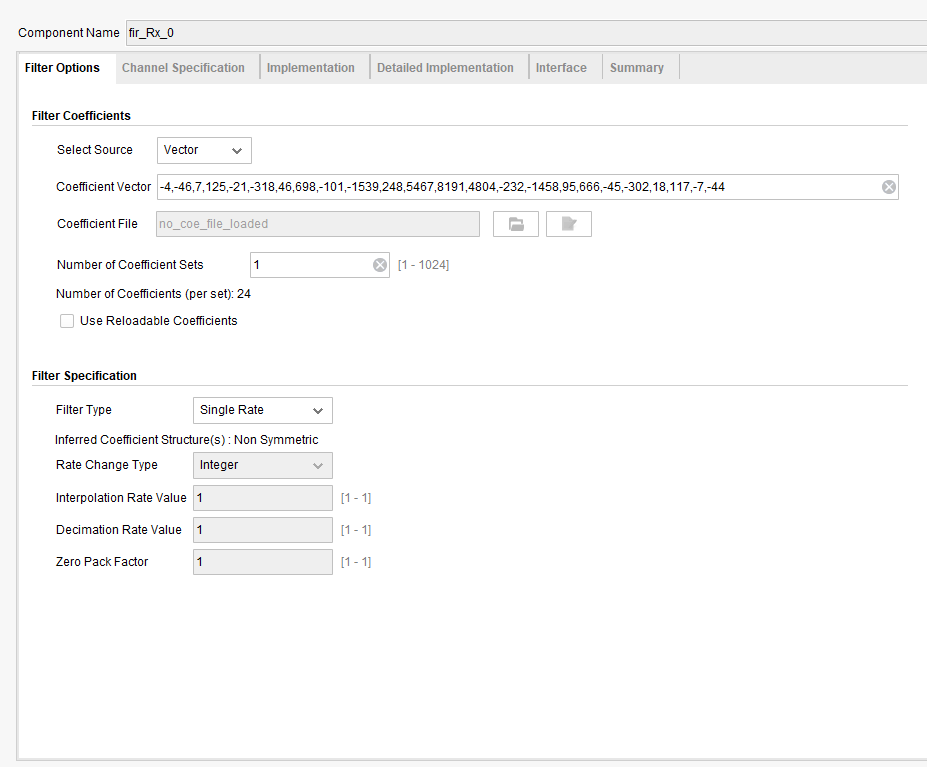


Fig. 1 Structure of the project

1. **Configuration of IP cores**
2. **Filter IP core**

In “Filter Options”:



* Set corresponding coefficient vector

For fir\_Rx\_0:

-4,-46,7,125,-21,-318,46,698,-101,-1539,248,5467,8191,4804,-232,-1458,95,666,-45,-302,18,117,-7,-44

For fir\_Rx\_1:

-11,-47,23,128,-64,-322,145,704,-314,-1564,793,6087,8082,4115,-642,-1329,270,610,-126,-275,53,106,-20,-40

For fir\_Rx\_2:

-18,-46,40,126,-109,-313,248,680,-535,-1525,1393,6650,7866,3414,-977,-1163,419,536,-195,-240,81,91,-29,-36

For fir\_Rx\_3:

-24,-42,57,117,-155,-289,350,625,-756,-1418,2039,7141,7550,2717,-1236,-969,537,448,-249,-200,102,75,-37,-30

For fir\_Rx\_4:

-30,-37,75,102,-200,-249,448,537,-969,-1236,2717,7550,7141,2039,-1418,-756,625,350,-289,-155,117,57,-42,-24

For fir\_Rx\_5:

-36,-29,91,81,-240,-195,536,419,-1163,-977,3414,7866,6650,1393,-1525,-535,680,248,-313,-109,126,40,-46,-18

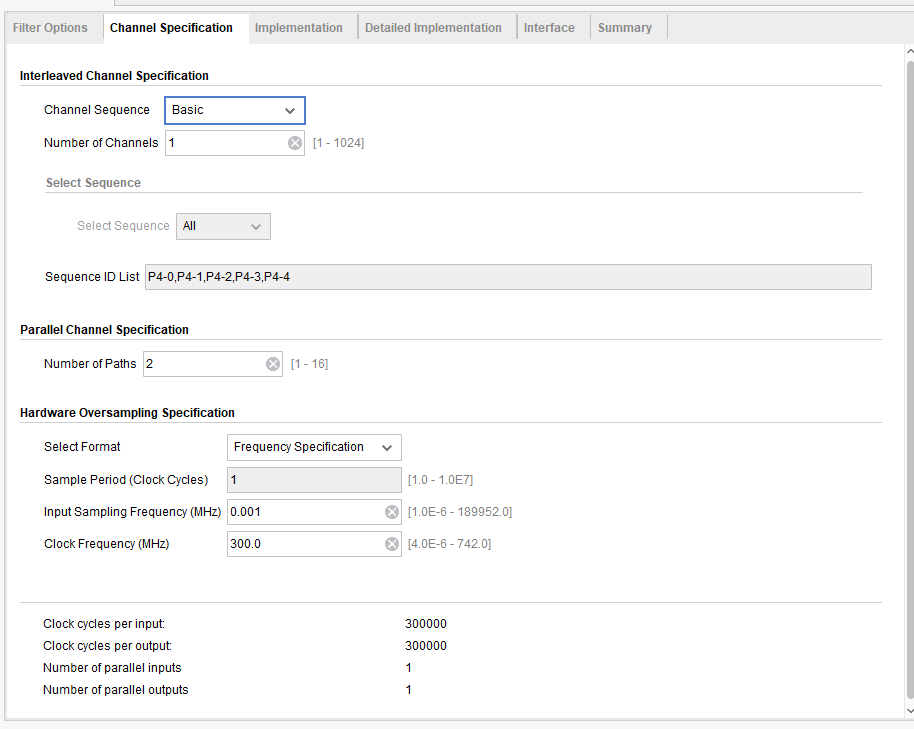
For fir\_Rx\_6:

-40,-20,106,53,-275,-126,610,270,-1329,-642,4115,8082,6087,793,-1564,-314,704,145,-322,-64,128,23,-47,-11

For fir\_Rx\_7:

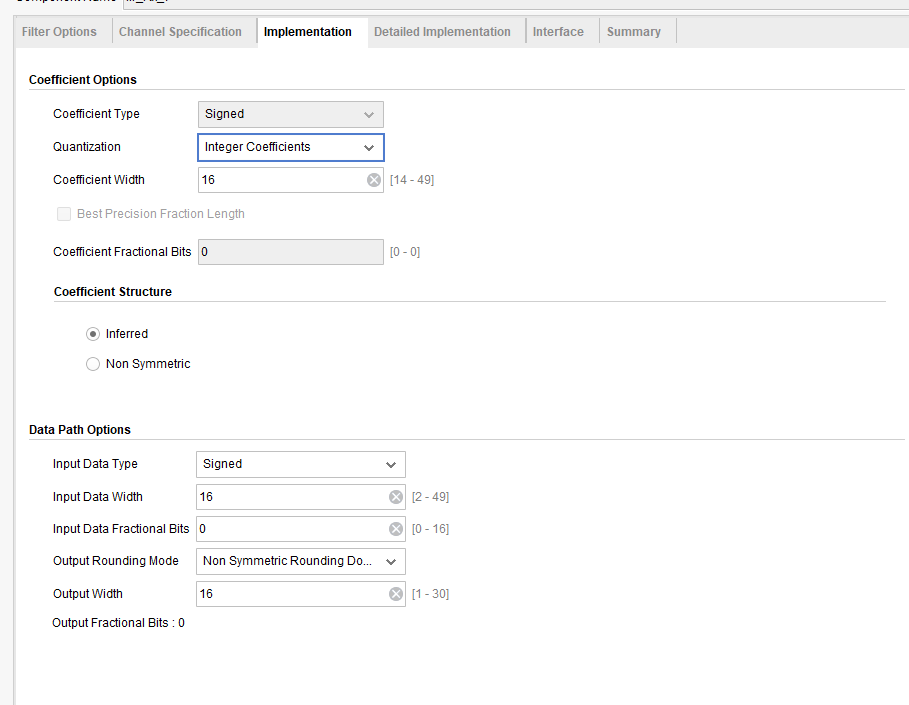
-44,-7,117,18,-302,-45,666,95,-1458,-232,4804,8191,5467,248,-1539,-101,698,46,-318,-21,125,7,-46,-4

In “Channel Specification”:



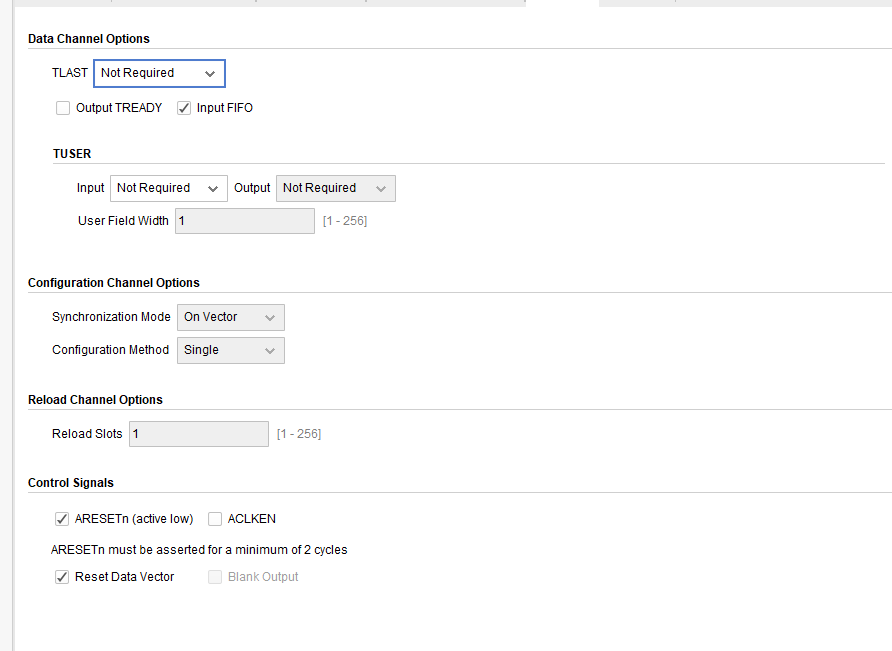
* Set “Number of Paths” as 2

In “Implementation”:



* Set “Coefficient Width” as 16
* Set “Output Rounding Mode” as non symmetric rounding down
* Set “Output Width” as 16

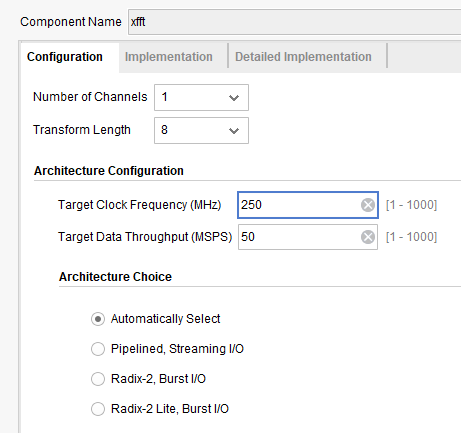
In “Interface”:



* check “ARESETn (active low)” box

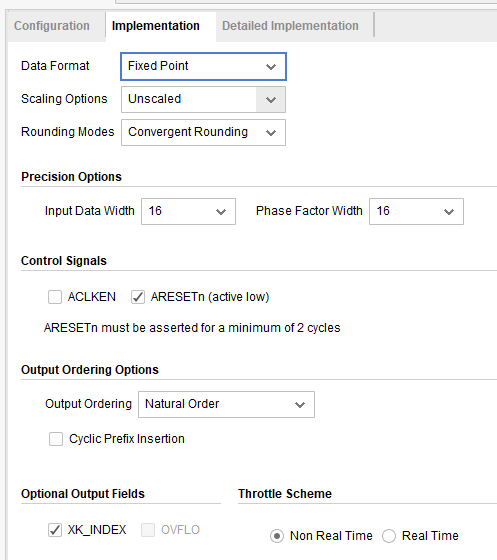
1. **FFT IP Core**

In “Configuration”:



* Set “Transform Length” as 8

In “Implementation”:



* Set each parameter as above

1. **Set “DC\_rx.sv” as the top module**