ECSE 323 - Digital System Design
After Action Report - The Dealer Finite State Machine

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Part I

A Pleasant Preamble

Sometimes in life one may be presented with situations that make him rethink his beliefs and question who, in fact, he really is. It is moments like these that actually define an individual *ad postremum*. Of course, it is up to the individual in question to *realize* that he shall be withdrawing cathexis from the myriad objects of empirical reality around him if enlightenment should be obtained. People that occasionally experience this enlightenment are called patricians. Those who continuously experience this enlightenment are called Engineers.

Consider the infamous game of Blackjack. Some may enjoy this game as a nice way to pass the time, others may be violently obsessed with it. Regardless of who is playing, the game can only be played reliably when players understand and follow the rules and when a credible dealer is present. Naturally, the players are needed for the game to be played, and of course the game is only really *being played* when the rules are followed. The presence of the dealer, however, is far more interesting than what the uninformed reader may believe.

Some say the dealer's job is to deal the cards, but that is a vast and decadent oversimplification. Sure, the dealer *should* deal the cards (at the appropriate times, that is), but the dealer is also responsible for establishing structure and ensuring that the game does not get out of hand. In fact, the rules of the game themselves have their strings pulled by the dealer.
But some dealers do not follow the rules.

It is no longer news that the goal of these laboratory sessions is to build a *crazy eights* game, and not a Blackjack game. Although the rules of the two games are different, both take on the rules-dealer paradigm of gameplay. The layman, and even the patrician, may focus on the rules of the game principally. However, as Engineers, the main focus of this laboratory was to create not just a functional dealer, but a reliable, ethical, and ultimately compliant dealer. As shown later in this report, this was successfully accomplished due to the design of a clever *finite state machine*, a construct that has also been used in the design of underwhelming robots.

In the interest of moral behavior, it would be unethical to display the accomplishments of this laboratory session without giving due credit to the Altera Quartus II and Modelsim software, whose magical functionalities allow such complex designs to be mapped onto an FPGA. Given Altera's great text editing accomodations and incredible timing simulation tools, the development of this system was dream-like.

At this stage, the reader is invited to explore the remainder of this report, which will go through in a (hopefully) simple and organized manner the discoveries made during this laboratory session. Beyond that, this report will discuss *how* these discoveries were made, and how they were reinforced, so the reader may gain intuition on developing state of the art digital systems.

Please enjoy the discoveries and details that follow, and try to learn something from them. Much is to be gained by grasping the concepts of the rules-dealer paradigm, as they apply to more in life than simply digital systems and card games. To conclude this pleasant preamble, the reader is encouraged to, above all, *have fun* with this report, and better yet, to have fun with life. Finally, it is important to remember that while by law a man is guilty for violating the rules, in ethics a man is guilty merely by *considering* such violation. Be careful, be wise, and Baba Booey to all.

Part II

The Dealer Circuit

Introduction

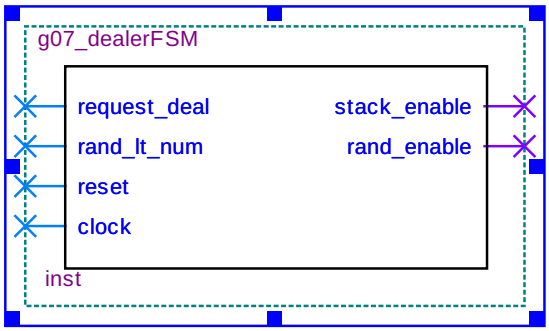
As foreshadowed in the pleasant preamble above, having a loyal, dependable dealer will be crucial to the reliable functionality of the crazy eights system. Without such a dealer, the *rules* of the game *may not* be followed, causing complete and utter pandemonium, ultimately resulting in a rather atrocious crazy eights game.

Therefore, it would benefit the system to create a robust *finite state machine*, a machine of a finite number of states. The system was reduced to a machine of 4 states (where $4 < \infty$ holds), of which include the state that waits for the previous request to end (denoted by A), the state that waits for the next request to *be* sent (denoted by B), the state that generates random numbers, so as to deal the cards (denoted by C), and finally, the state that activates a stack (or more accurately, a bi-directional Jenga tower) circuit (denoted by D).

All of the cleverness and power that has been teased above was encompassed by a circuit that has since been named the `g07_dealerFSM`. A more detailed insight to the design of the finite state machine and the `g07_dealerFSM` follows below, and is complemented by thoughtful pictorial support for easier understanding.

Circuit Description

Figure 1: Pin-out diagram of the `g07_dealerFSM` circuit



Above is a pin-out diagram of the miraculous `g07_dealerFSM` circuit, showcasing its input and output ports. A more detailed description of these ports will be given below.

Description of ports

request_deal

The `request_deal` input bit is activated when the system requests that the dealer should deal a card.

rand_lt_num

The `rand_lt_num` input bit is controlled by an external circuit that is high when a random number has a value that is less than the BJT's `NUM` output that the dealer is associated with. This allows the dealer to tell whether it should keep generating random numbers (in state C), or move on.

reset

The `reset` input bit causes the finite state machine to be reset to its initial state when `reset` is high. It is asynchronous.

stack_enable

The `stack_enable` output bit is active when a valid random number has been generated in the proper state. It is used to enable the BJT associated with the dealer to pop a card.

rand_enable

The rand_enable output bit is active after request_deal has been asserted anew, and enables a random number generator to generate random numbers until rand_lt_num is high.

A complete VHDL description of the g07_dealerFSM circuit is provided in the following section.

VHDL portrayal of the g07_dealerFSM circuit

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.numeric_std.all;
4
5  entity g07_dealerFSM is
6          port (
7                  request_deal: in std_logic;
8                  rand_lt_num: in std_logic;
9                  reset: in std_logic;
10                 clock: in std_logic;
11                 stack_enable: out std_logic;
12                 rand_enable: out std_logic
13         );
14 end g07_dealerFSM;
15
16 architecture machineOfState of g07_dealerFSM is
17         SIGNAL initial_seed: std_logic_vector(31 downto 0) := std_logic_vector(
               to_unsigned(1337,32));
18         SIGNAL random: std_logic_vector(31 downto 0);
19         SIGNAL reg_out: std_logic_vector(5 downto 0);
20         SIGNAL comp_lt: std_logic;
21         SIGNAL stack_num: std_logic_vector(5 downto 0);
22
23         TYPE State_type is (A,B,C,D);
24         SIGNAL state: State_Type;
25 begin
26         rand_enable <= '1' when state = C else '0';
27         stack_enable <= '1' when state = D else '0';
28         machine: process (clock, reset)
29         begin
30                 if(reset = '1') then state <= A;
31                 elsif (clock'event and clock = '1') then
32                         case state is
33                                 WHEN A =>
34                                         if(request_deal = '0') then state <= B;
35                                         else state <= A;
36                                         end if;
37                                 WHEN B =>
38                                         if(request_deal = '0') then state <= B;
39                                         else state <= C;
40                                         end if;
41                                 WHEN C =>
42                                         if(rand_lt_num = '0') then state <= C;
```

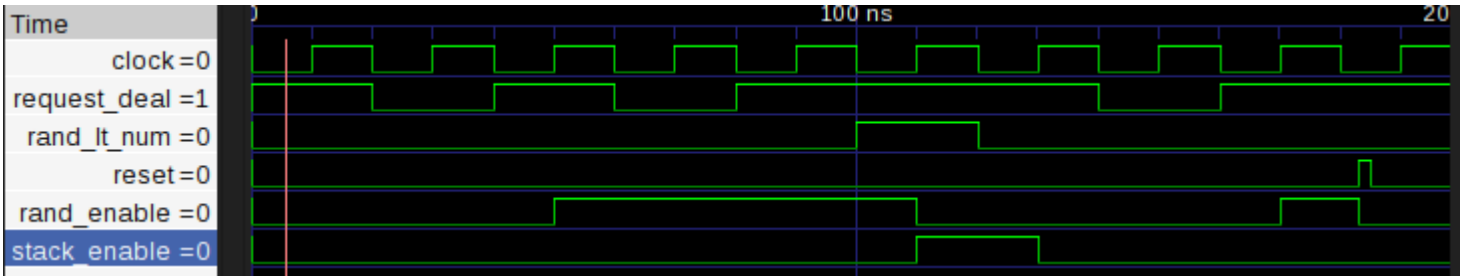
```
43                                          else state <= D;
44                                          end if;
45                                  WHEN D =>
46                                          state <= A;
47                          end CASE;
48                  end if;
49          end process machine;
50  end machineOfState;
```

On the Testing of the Dealer Circuit

It was an important and difficult challenge to resist being seduced by the beauty of the VHDL code that describes the `g07_dealerFSM` circuit. Despite it's beauty, a dealer cannot be trusted without being tested. Think about this following section as an analog to an interview process, if you will. Before putting the `g07_dealerFSM` in commission, it was important to make sure it satisfied all dealing requirements (and boy, did it ever), and to make sure it functioned correctly on the hardware. The demonstrations that follow will prove that the `g07_dealerFSM` is in fact an excellent candidate.

The software circuit simulation: A poor man's analysis

The first order of business in judging the effectiveness of the `g07_dealerFSM` was to test it with the magical Modelsim simulator. Unfortunately, said software was not functioning to the tester's standards. As a consequence, the miraculous GtkWave VCD viewer came to the rescue, and the `g07_dealerFSM` was examined thoroughly according to a carefully-written testbench.
For the less-enthused, the testbench starts the state machine in its default state, and examines each state transition in the trivial order. Then, the machine is brought to state C (where `rand_enable` is high) and reset is activated to ensure that it causes the machine to return to its initial state.
The resulting waveforms can be viewed below.



Of course, the results shown above cannot conclusively confirm the excellence of the `g07_dealerFSM` circuit on their own, because they give no evidence of the dealer functioning on real hardware. Hence, this test was called a *poor man's analysis*. Fortunately, the testers *are not* poor men. In fact, they have access to an Altera DE1 FPGA development board equipped with an Altera Cyclone II FPGA. The tests in the following section will describe how *full confidence* of the `g07_dealerFSM` was obtained.

The hardware circuit simulation: an Engineer's victory

Some tests are easy, leaving the participants in a relaxing state of mind. Yet, some tests are hard, leaving participants in a state of panic. However, occasionally a test may reach a transcendental level of difficulty, such that it may be said that the test *separates the boys from the men*. That, dear reader, is what you will witness in the remainder of this section. Anyone from laymen to patricians can make a software circuit simulation, neglecting the possiblity that something may go wrong on the hardware. While seemingly reasonable to the un-seasoned tester, this train of thought is highly dangerous and irresponsible. It is up to the Engineer to realize that this, in fact, will not suffice. This realization was exhibited, more than anything else, in the results below.

The first order of business was to create a *test bed*, or circuit that bridges the gap between human input and dealer communication. This was done using the not-short-of-incredible Altera Quartus II schematic designer, and may be perused here.

For the less-motivated reader, a brief description of the testbed will be given. Firstly, The `stack_enable` output of the dealer circuit is passed as the `enable` input of the BJT. The `rand_enable` output was passed to the `enable` input of a `g07_register6` circuit, which is a masterfully-simple 6-bit register designed by the same designers of the `g07_dealerFSM`. The design of the `g07_register6` is unfortunately beyond the scope of this report. The register serves the purpose of latching a random number generated by the random number generator module. Then, the value stored by the register is passed through a comparator, which sends a 1 to the `g07_dealerFSM` when the random value is less than the `NUM` output of the BJT. The `request_deal` input comes from the output of the infamous `g07_debounder` debouncer circuit (discussed in a previous laboratory report), so as to remove the all-feared bouncing of the DE1's hardware buttons. The random number generator module consists of a `g07_RANDU` (discussed in a previous laboratory report) which takes as input the multiplexation of a constant seed, and the last generated random output of itself. When the BJT is full, the constant seed is passed to the RANDU, and otherwise it uses its own seed to enliven itself.

Finally, the `NUM` output of the BJT as well as the `VALUE` output corresponding to the address described by the value stored in the `g07_register6` are passed through `mod13` circuits (discussed in previous laboratory reports) to be conveniently displayed on the 7 segment decoders on the DE1 board.

Some say a picture is worth a thousand words, however only an infinite amount of words can be used to describe the joy of the testers upon witnessing the massive success of the `g07_dealerFSM` circuit on the testbed. It would be infeasible to include so many pictures in this report. Instead, a brief overview of what was accomplished will be offered.

There were just two more criteria that needed to be confirmed to ensure the proper functioning of the dealer. Firstly, it needed to be confirmed that the `NUM` output of the BJT decreases by only 1 after each deal (thus implying that the dealer deals one card at a time). This test passed immediately with flying carpets. Furthermore, it had to be ensured that the cards being dealt were random! Although this part did provide some inconsistencies early one (due to a mistake with the comparator connections, mostly), eventually it was seen that random numbers in the range of 0 to `NUM` were seen being popped from the BJT. Victory was gracefully achieved.

Computer Analysis of the Dealer Circuit

If you thought the validation of the g07_dealerFSM circuit was complete, you have successfully been tricked. What blasphemy! Surely, the g07_dealerFSM must be shown to not inhibit the circuitry that it will integrated with. To verify that this will not be an issue, Altera's magical Quartus II Flow Summary and TimeQuest Timing Analyzer will be used extensively. Please continue reading the final sections of this report to determine whether or not the g07_dealerFSM is a *feasible* circuit, given all its unwieldly power.

The Flow Summary

According to Quartus II's Flow Summary, the g07_dealerFSM allegedly uses only 3 combinational logic functions, and 3 dedicated logic registers. Given that there are 18752 logic registers and combinational logic functions available in the FPGA, these numbers make for less than 1% of the resources available. Then, it can be safely concluded that the g07_dealerFSM does not require too much hardware, and is in fact *very* feasible in that regard. Furthermore, the g07_dealerFSM allegedly requires absolutely no memory bits, further convincing the feasibility of the dealer.

The Timing Analysis

Lastly (and you are not being fooled this time), the dealer must not require particularly low clock frequencies for its operation to be successful. It also would be beneficial for it to not impose any restrictions on the envelope of the clock pulse, as that would be rather inconvenient. According to the Timing Analyzer of Quartus II, the g07_dealerFSM allegedly imposes a minimum pulse width of -1.631 (units not given). Regardless of the units, negative pulse widths are not a problem in the measuring systems in use today. In fact, most may say negative pulse widths do not exist (but it's better not to generalize in a report like this). However, due to the negative minimum pulse width, it can be safely concluded that no testable pulse width should cause a problem for the g07_dealerFSM circuit.

Finally, the Quartus II Timing Analyzer reported a restricted maximum frequency of 380.08MHz. This is extremely impressive, given that the maximum clock frequency that will be supplied to the g07_dealerFSM is the DE1's clock of 50MHz. Therefore, there shall be no timing violations caused by the g07_dealerFSM given its clock. This maximum frequency corresponds to a maximum propagation delay within the circuit of $1/38008000 = 2.63$ns, which is exceedingly small.

Given these results, it is clear that the g07_dealer circuit uses very little hardware and imposes no considerable timing issues. Finally, the Engineer may leave his mark.

Appendix A

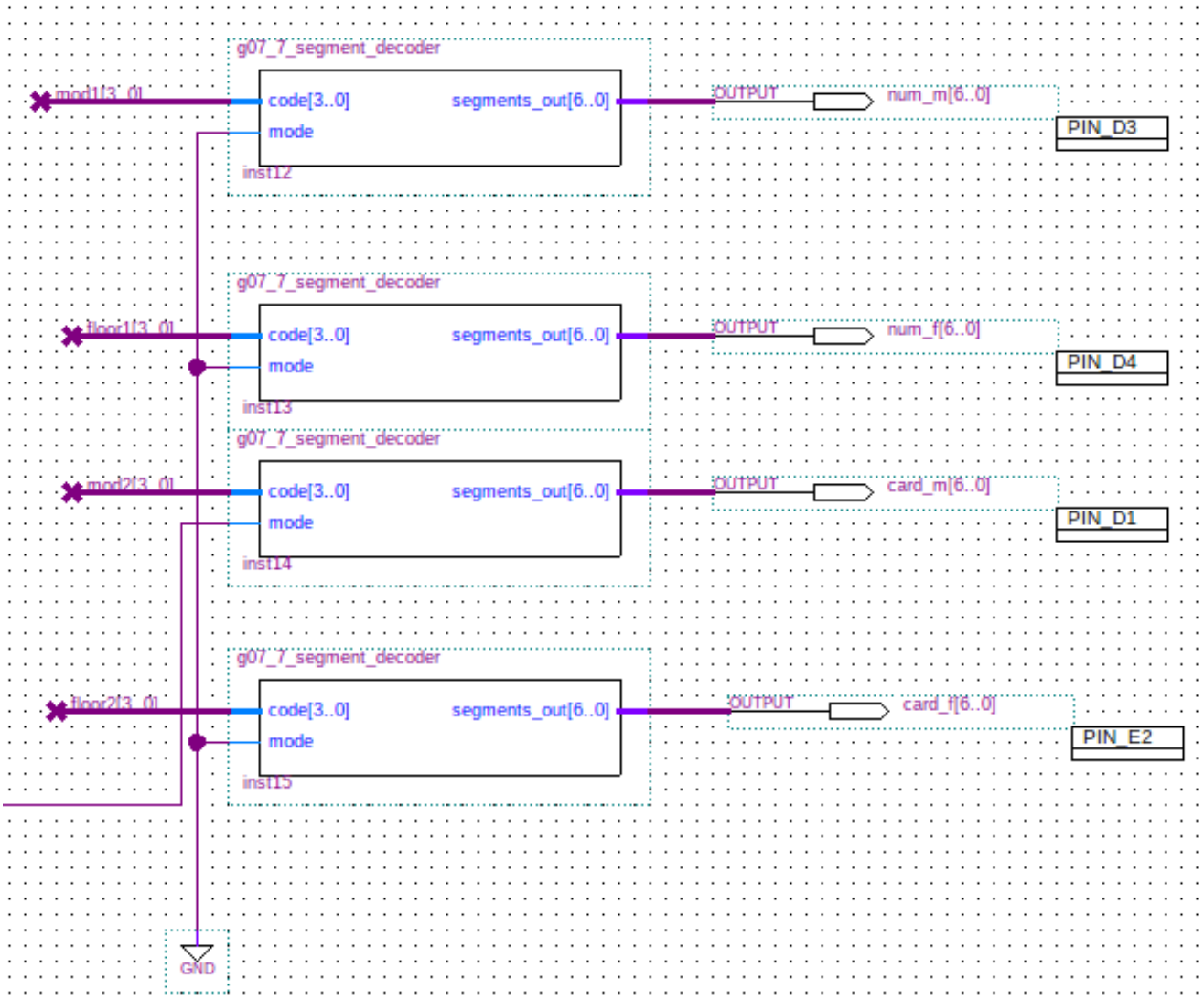
VHDL Testbench for the g07_dealerFSM

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.numeric_std.all;
4
5  entity dealerFSM_tst is
6  end;
7
8  architecture test of dealerFSM_tst is
9          component g07_dealerFSM
10                 port (
11                         request_deal: in std_logic;
12                         rand_lt_num: in std_logic;
13                         reset: in std_logic;
14                         clock: in std_logic;
15                         stack_enable: out std_logic;
16                         rand_enable: out std_logic
17                 );
18         end component;
19         SIGNAL request_deal, rand_lt_num, reset, stack_enable, rand_enable:
               std_logic;
20         SIGNAL clock: std_logic := '0';
21         SIGNAL finished: std_logic := '0';
22
23 begin
24         machine: g07_dealerFSM
25         port map (
26                 request_deal => request_deal,
27                 rand_lt_num => rand_lt_num,
28                 reset => reset,
29                 clock => clock,
30                 stack_enable => stack_enable,
31                 rand_enable => rand_enable
32         );
33
34         clock <= '0' when finished = '1' else not clock after 10 ns;
35
36         always: process
37         begin
38                 request_deal <= '1';
39                 rand_lt_num <= '0';
40                 reset <= '0';
```

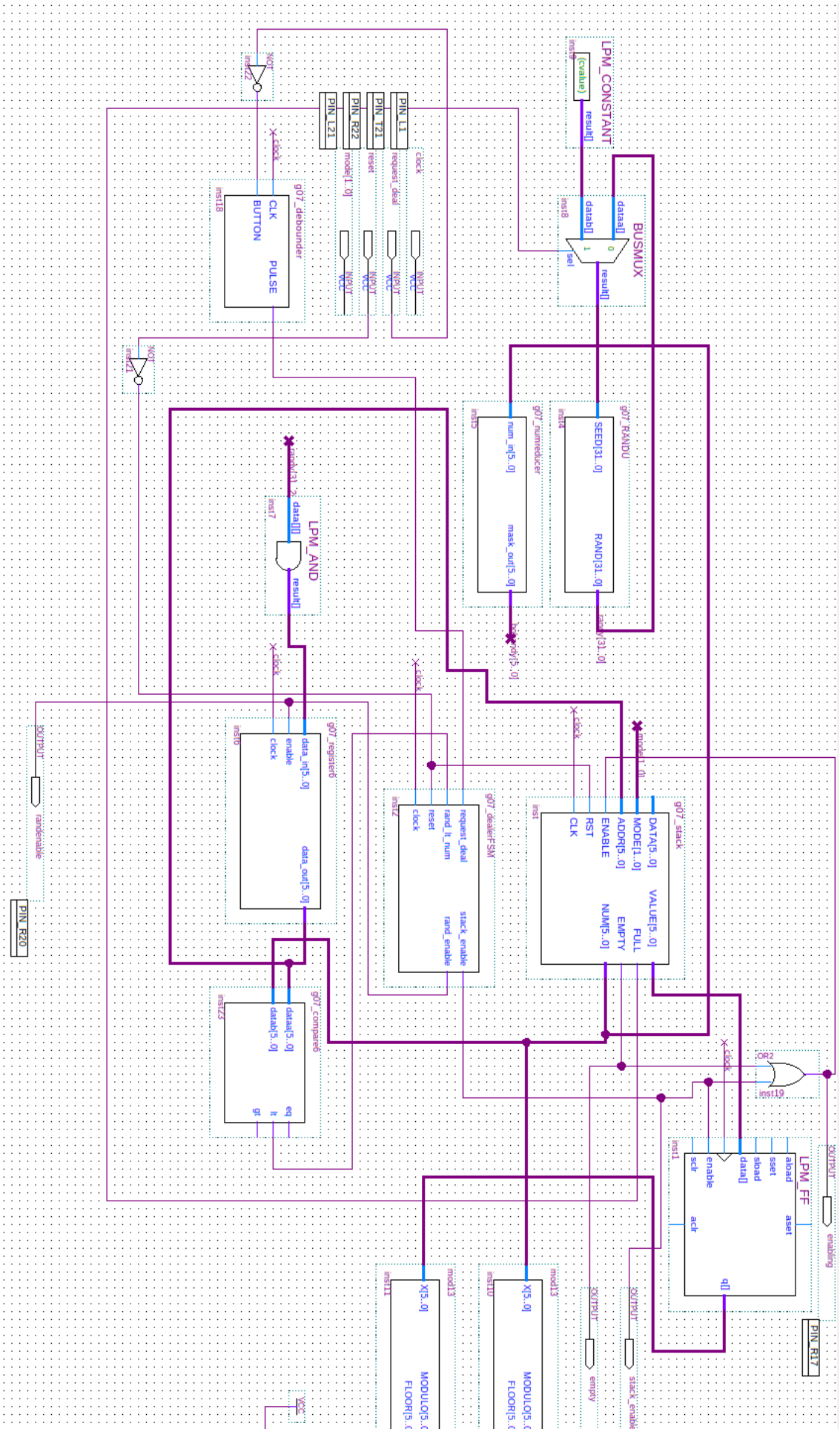
```
41                  WAIT FOR 20 ns;
42                  request_deal <= '0';
43                  WAIT FOR 20 ns;
44                  request_deal <= '1';
45                  WAIT FOR 20 ns;
46                  request_deal <= '0';
47                  WAIT FOR 20 ns;
48                  request_deal <= '1';
49                  WAIT FOR 20 ns;
50                  rand_lt_num <= '1';
51                  WAIT FOR 20 ns;
52                  rand_lt_num <= '0';
53                  WAIT FOR 20 ns;
54                  request_deal <= '0';
55                  WAIT FOR 20 ns;
56                  request_deal <= '1';
57                  WAIT FOR 23 ns;
58                  reset <= '1';
59                  WAIT FOR 2 ns;
60                  reset <= '0';
61                  WAIT FOR 15 ns;
62                  finished <= '1';
63                  WAIT;
64          end process always;
65  end test;
```

Appendix B

Testbed for the `g07_dealerFSM`



Above is the section of the testbed that showws how data is output to the 7 segment displays on the DE1. On the following page, the main body of the testbed may be observed.


LPM_CONSTANT
BUSMUX
LPM_AND
LPM_FF
g07_debounder
g07_numreducer
g07_RANDU
g07_register6
g07_deasertFSM
g07_stack
g07_compare6
PIN_L21
PIN_R22
PIN_T21
PIN_L1
PIN_R20
PIN_R17
CLK
BUTTON
PULSE
num_in[5..0]
mask_out[5..0]
SEED[31..0]
RAND[31..0]
data[][]
resu[]
datab[]
dataa[]
sel
clock
enable
data_in[5..0]
data_out[5..0]
reset
rand_lt_num
request_deal
stack_enable
rand_enable
RST
ADDR[5..0]
MODE[1..0]
DATA[5..0]
VALUE[5..0]
FULL
EMPTY
NUM[5..0]
datab[5..0]
dataa[5..0]
gt
lt
eq
OR2
inst19
scir
aclr
sload
sset
aload
aset
q[]
MODULO[5..0]
FLOOR[5..0]
empty
enabling
randenable
OUTPUT
VCC