

# Thorpe-2 TBT Logic Schematics

THP2 D-0  
VER 0.01  
Oct/26/2016

BASE LOGIC :  
thp2\_sitr\_lcfc\_20161014

- 1.TITLE PAGE
- 2.EC HISTORY
- 3.CPU(1/16) : DDI/EDP
- 4.CPU(2/16) : DDR CHANNEL-A
- 5.CPU(3/16) : DDR CHANNEL-B
- 6.CPU(4/16) : MISC/JTAG
- 7.CPU(5/16) : LPC/SPI/SMBUS/C-LINK
- 8.CPU(6/16) : LPSS/ISH
- 9.CPU(7/16) : AUDIO/SDXC
- 10.CPU(8/16) : PCIE/USB/SATA
- 11.CPU(9/16) : CSI-2/EMMC
- 12.CPU(10/16) : CLOCK SIGNALS
- 13.CPU(11/16) : SYSTEM PM
- 14.CPU(12/16) : CPU POWER (1/2)
- 15.CPU(13/16) : CPU POWER (2/2)
- 16.CPU(14/16) : PCH POWER
- 17.CPU(15/16) : GND
- 18.CPU(16/16) : CFG/RESERVED
- 19.XDP CONNECTOR
- 20.RTC BATTERY
- 21.SPI FLASH
- 22.DDR4 BASE MEMORY CH-A (1/2)
- 23.DDR4 BASE MEMORY CH-A (2/2)
- 24.DDR4 SO DIMM CHANNEL-B (1/2)
- 25.DDR4 SO DIMM CHANNEL-B (2/2)
- 26.LCD/USB/LID/MIC/CAMERA/PWR SW
- 27.BLANK
- 28.BLANK
- 29.DDI DEMUX/HDMI LEVEL SHIFTER
- 30.HDMI CONNECTOR
- 31.M.2 SATA/PCIE SSD CARD SLOT
- 32.USB POWER/CONN
- 33.BLANK
- 34.GBE JACKSONVILLE
- 35.GBE LAN SWITCH
- 36.GBE MAGNETICS
- 37.RJ45 CONNECTOR
- 38.BLANK
- 39.BLANK
- 40.BLANK
- 41.BLANK
- 42.BLANK
- 43.BLANK
- 44.BLANK
- 45.BLANK
- 46.PCIE M.2 (NGFF) CARD SLOT
- 47.SD/AUDIO CONNECTOR I/F
- 48.BLANK
- 49.BLANK
- 50.AUDIO ALC3268
- 51.AUDIO HP JACK DETECT
- 52.AUDIO JACK SENSE
- 53.BLANK
- 54.AUDIO SPEAKER
- 55.AUDIO BEEP
- 56.BLANK
- 57.DOCKING CONNECTOR
- 58.MEC1653(1/3)
- 59.MEC1653(2/3)
- 60.MEC1653(3/3)
- 61.KEYBOARD/TRACK POINT
- 62.TOUCH PAD/FPR/SCR
- 63.FAN CONNECTOR
- 64.APS G-SENSOR
- 65.DISCRETE TPM 2.0
- 66.SMBUS SWITCH/LPC DEBUG PORT
- 67.THINK ENGINE-2(1/2)
- 68.THINK ENGINE-2(2/2)
- 69.DC-IN
- 70.BATTERY INPUT
- 71.BATTERY CHARGER(BQ25700)

- 72.CHARGER SELECTOR
- 73.BLANK
- 74.DC/DC VCC5M/VCC3M (TPS51285B-1)
- 75.DC/DC IMVP8 CONTROLLER(NCP81218)
- 76.DC/DC VCCCPUCORE(NCP81382)
- 77.DC/DC VCCGFXCORE\_I(NCP81382)
- 78.DC/DC VCCSA(NCP81380)
- 79.BLANK
- 80.DC/DC VCCCPUIO(NB682)
- 81.DC/DC VCC1R0\_SUS(BD91364BMUU)
- 82.LOAD SW VCCST & VCCSTG
- 83.DC/DC VCC1R2A(TPS51716RUKR)
- 84.BLANK
- 85.DC/DC VCC2R5A(TLV62080)
- 86.DC/DC VCC1R8\_SUS(BU90104GWZ)
- 87.DC/DC VCCPCHCORE(NB695)
- 88.BLANK
- 89.BLANK
- 90.BLANK
- 91.BLANK
- 92.BLANK
- 93.LOAD SW PCH SUS/TRACK POINT
- 94.LOAD SW LAN
- 95.BLANK
- 96.LOAD SW B
- 97.LOAD SW WWAN & WLAN
- 98.BLANK
- 99.PTH FOR SCREW HOLES
100. ALPINE RIDGE LP(1/2)
101. ALPINE RIDGE LP(2/2)
102. TBT PORT
103. USB TYPE-C PROTOCTOR

<https://dr-bits.com>

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	TITLE PAGE	
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EC HISTORY

CS15 THP2 D-0  
(BASE LOGIC : thp2\_sitr\_lcfc\_20161014)

VER.0.01 10/26/2016 APPLIED Power ECR10192016 / EC10242016

TABLE: Chip Capacitor Thermal Characteristics

		Code
-55 to 150degC	+/-30ppm/degC	NPO
-55 to 125degC	+/-30ppm/degC	C0G
-55 to 125degC	+/-15%	X7R
-55 to 105degC	+/-22%	X6S
-55 to 85degC	+/-15%	X5R

TABLE: Chip Capacitor Tolerance

Tolerance	Code
+/-0.25pF	C
+/-0.5pF	D
+/-5%	J
+/-10%	K
+/-20%	M
+80/-20%	Z

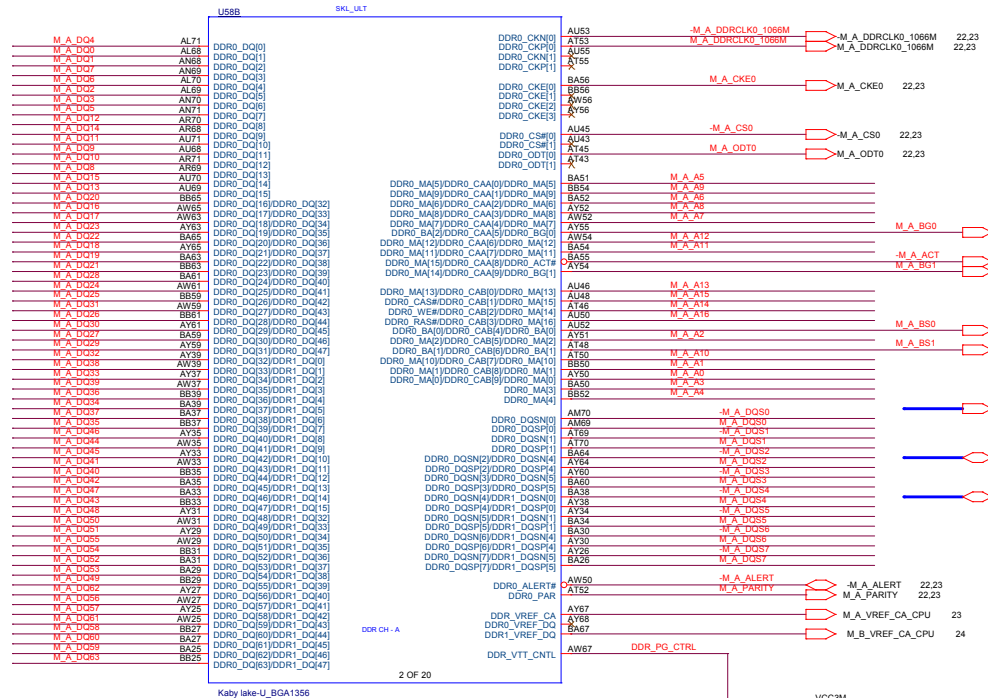
TABLE: Chip Part Dimension

Size [mm]	mm Size Code	Inch Size Code
0.40 x 0.20	0402	01005
0.60 x 0.30	0603	0201
1.00 x 0.50	1005	0402
1.60 x 0.80	1608	0603
2.00 x 1.25	2125	0805
2.00 x 1.60	2016	0806
2.50 x 2.00	2520	1008
3.20 x 1.60	3216	1206
3.20 x 2.50	3225	1210
4.50 x 1.60	4516	1806
4.50 x 2.50	4525	1810
4.50 x 3.20	4532	1812
5.00 x 2.50	5025	2010
6.40 x 3.20	6432	2512

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LOGIC



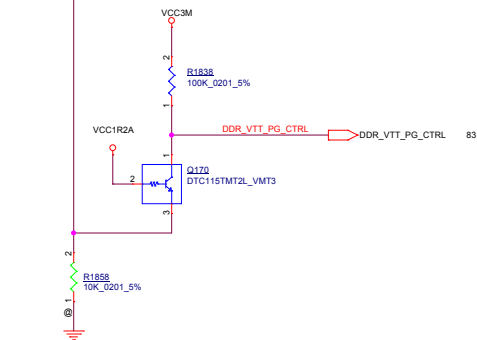
	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
AU70	DDR0_DQ[14]	DDR0_DQ[14]	
AU69	DDR0_DQ[15]	DDR0_DQ[15]	
Block 2	BB65	DDR0_DQ[16]	DDR0_DQ[32]
	AW65	DDR0_DQ[17]	DDR0_DQ[33]
	AW63	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[35]
	BA65	DDR0_DQ[20]	DDR0_DQ[36]
	AY65	DDR0_DQ[21]	DDR0_DQ[37]
	BA63	DDR0_DQ[22]	DDR0_DQ[38]
	BB63	DDR0_DQ[23]	DDR0_DQ[39]
	BA61	DDR0_DQ[24]	DDR0_DQ[40]
	AW61	DDR0_DQ[25]	DDR0_DQ[41]
	BB59	DDR0_DQ[26]	DDR0_DQ[42]
	AW59	DDR0_DQ[27]	DDR0_DQ[43]
	BB61	DDR0_DQ[28]	DDR0_DQ[44]
	AY61	DDR0_DQ[29]	DDR0_DQ[45]
BA59	DDR0_DQ[30]	DDR0_DQ[46]	
AY59	DDR0_DQ[31]	DDR0_DQ[47]	
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
BA33	DDR0_DQ[46]	DDR1_DQ[14]	
BB33	DDR0_DQ[47]	DDR1_DQ[15]	
Block 6	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	BB27	DDR0_DQ[59]	DDR1_DQ[43]
	BA27	DDR0_DQ[60]	DDR1_DQ[44]
	BA25	DDR0_DQ[61]	DDR1_DQ[45]
BB25	DDR0_DQ[62]	DDR1_DQ[46]	
	DDR0_DQ[63]	DDR1_DQ[47]	



Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

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**LOGIC**

	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]




Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	CPU(2/16) : DDR CHANNEL-A	
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Size	Document Number	Date		Rev	
Cusum	Thorp-2 UMA	Wednesday, October 26, 2016		0.01	
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TABLE	Pin	Interleave	Non-Interleave
Block 1	AF65	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK65	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF66	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK66	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH69	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[48]
	AU66	DDR1_DQ[17]	DDR0_DQ[49]
	AP65	DDR1_DQ[18]	DDR0_DQ[50]
	AN65	DDR1_DQ[19]	DDR0_DQ[51]
	AN66	DDR1_DQ[20]	DDR0_DQ[52]
	AP66	DDR1_DQ[21]	DDR0_DQ[53]
	AT65	DDR1_DQ[22]	DDR0_DQ[54]
	AU65	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AP60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AP61	DDR1_DQ[29]	DDR0_DQ[61]
	AT60	DDR1_DQ[30]	DDR0_DQ[62]
	AU60	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AP40	DDR1_DQ[36]	DDR1_DQ[20]
	AP37	DDR1_DQ[37]	DDR1_DQ[21]
	AR37	DDR1_DQ[38]	DDR1_DQ[22]
	AT33	DDR1_DQ[39]	DDR1_DQ[23]
	AU33	DDR1_DQ[40]	DDR1_DQ[24]
	AU30	DDR1_DQ[41]	DDR1_DQ[25]
	AT30	DDR1_DQ[42]	DDR1_DQ[26]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]
	AR30	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

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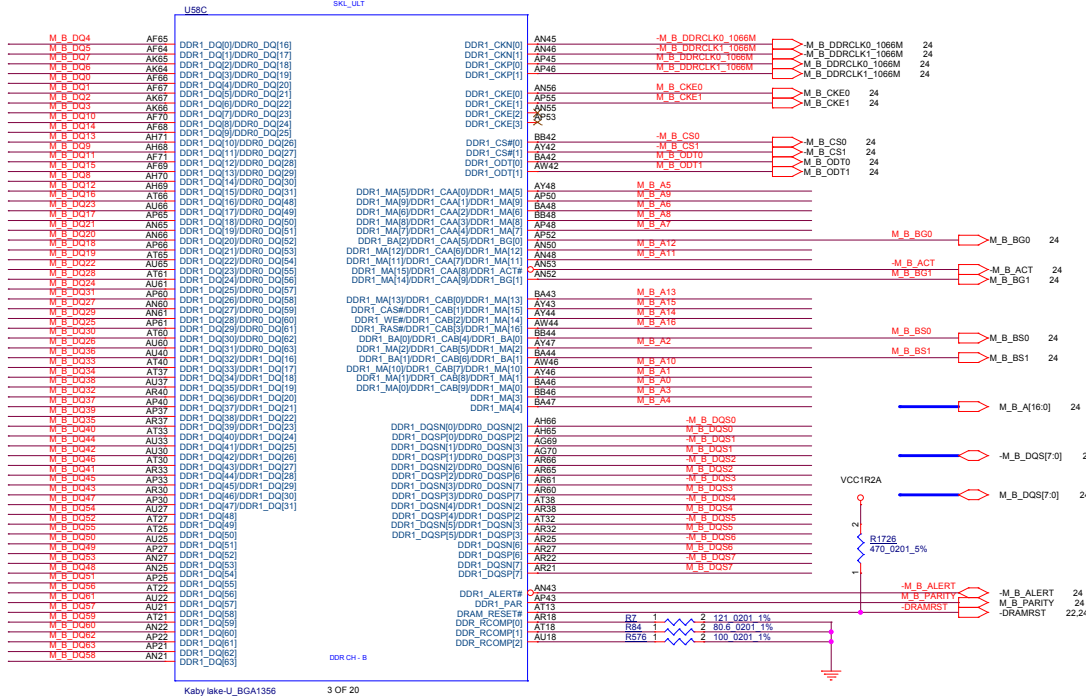


TABLE	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AG65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR64	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

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TABLE	Pin	DDR3L	LPDDR3	DDR4
Block 1	AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
	AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
	BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
	BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
	AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
	AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
	AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
	AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
	AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
	AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
Block 3	BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
	AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
	AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
	AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
	BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
	AY47	DDR1_BA[2]	DDR1_CAB[5]	DDR1_MA[2]
	BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
	AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
	AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
	BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
	BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
	BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]
Block 5	AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
	AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
	BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
	BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
	AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
	AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
	AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
	AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
	AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
	AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
Block 3	BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
	AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
	AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
	AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
	BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
	AY47	DDR1_BA[2]	DDR1_CAB[5]	DDR1_MA[2]
	BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
	AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
	AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
	BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
	BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
	BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]	DDR1_DQ[19]
	AP40	DDR1_DQ[36]	DDR1_DQ[20]	DDR1_DQ[20]
	AP37	DDR1_DQ[37]	DDR1_DQ[21]	DDR1_DQ[21]
	AR37	DDR1_DQ[38]	DDR1_DQ[22]	DDR1_DQ[22]
	AT33	DDR1_DQ[39]	DDR1_DQ[23]	DDR1_DQ[23]
	AU33	DDR1_DQ[40]	DDR1_DQ[24]	DDR1_DQ[24]
	AU30	DDR1_DQ[41]	DDR1_DQ[25]	DDR1_DQ[25]
	AT30	DDR1_DQ[42]	DDR1_DQ[26]	DDR1_DQ[26]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]	DDR1_DQ[29]
	AR30	DDR1_DQ[46]	DDR1_DQ[30]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]	DDR1_DQ[31]

↑  
LOGIC

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<b>SPI0_MOSI (Boot Halt)</b>	
<b>HIGH</b>	<b>Disabled (Default)</b>
<b>LOW</b>	<b>Enabled</b>

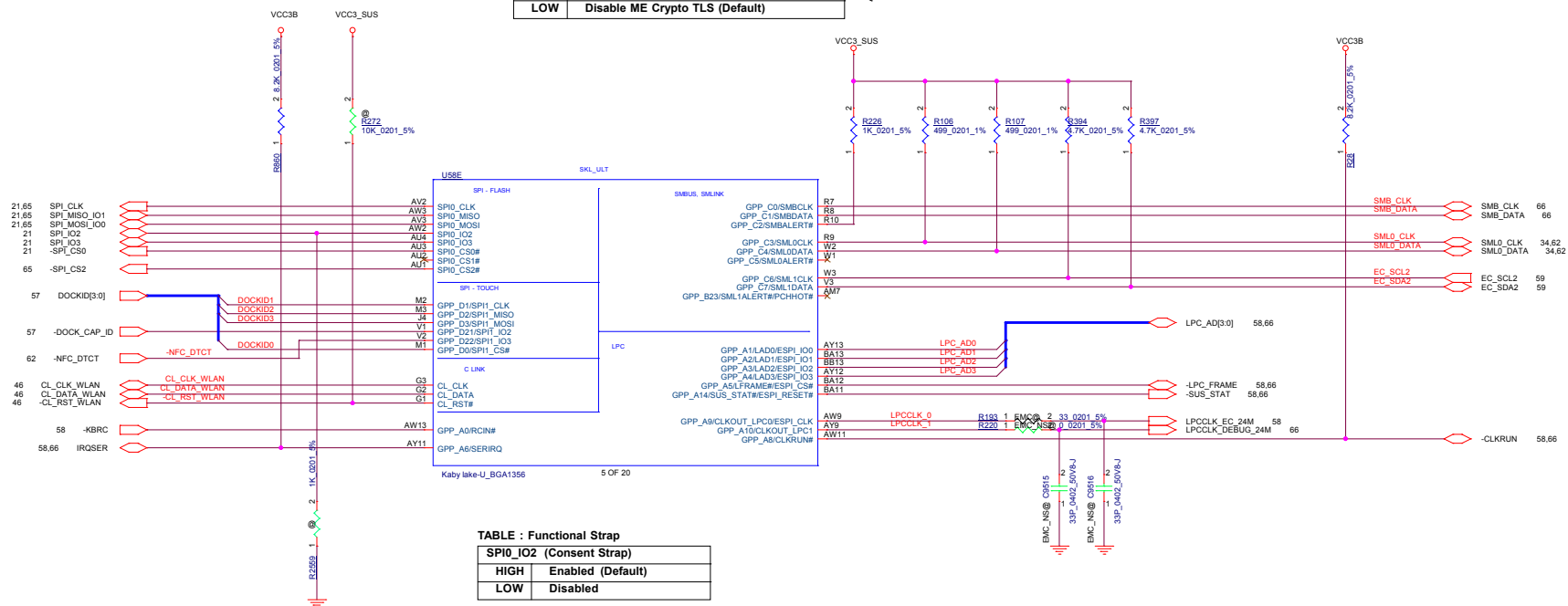
SPI0_MISO (JTAG ODT Disable)	
HIGH	Enabled (Default)
LOW	Disabled

GPP_C5/SML0ALERT # (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

## LOGIC

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

## LOGIC



SPI0_IO2 (Consent Strap)	
HIGH	Enabled (Default)
LOW	Disabled

SPI0_IO3 (A0 Personality Strap)	
HIGH	Disabled (Default)
LOW	Enabled





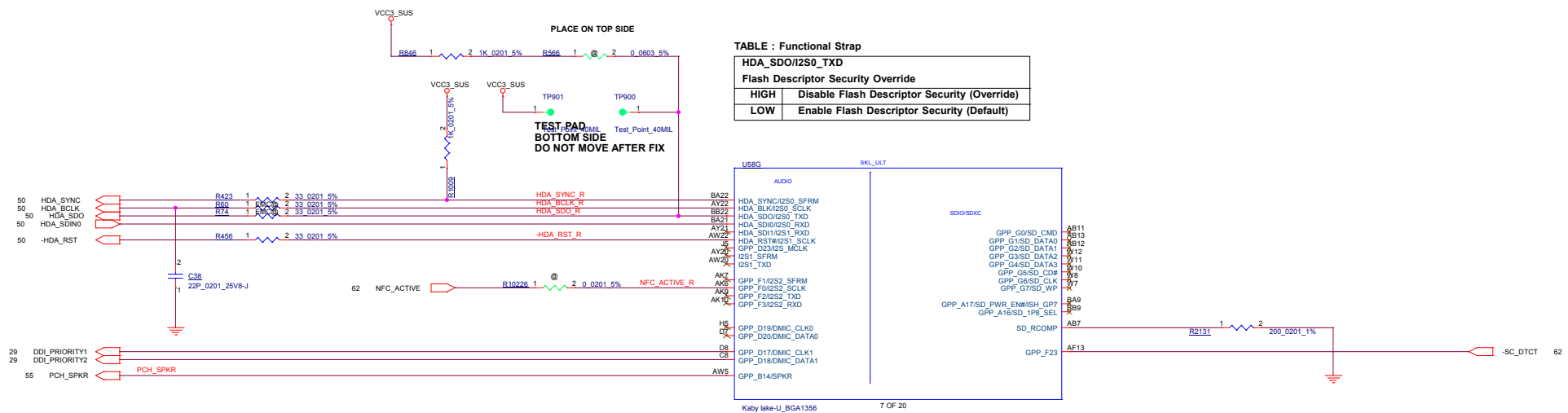


TABLE : Functional Strap

HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

TABLE : Functional Strap

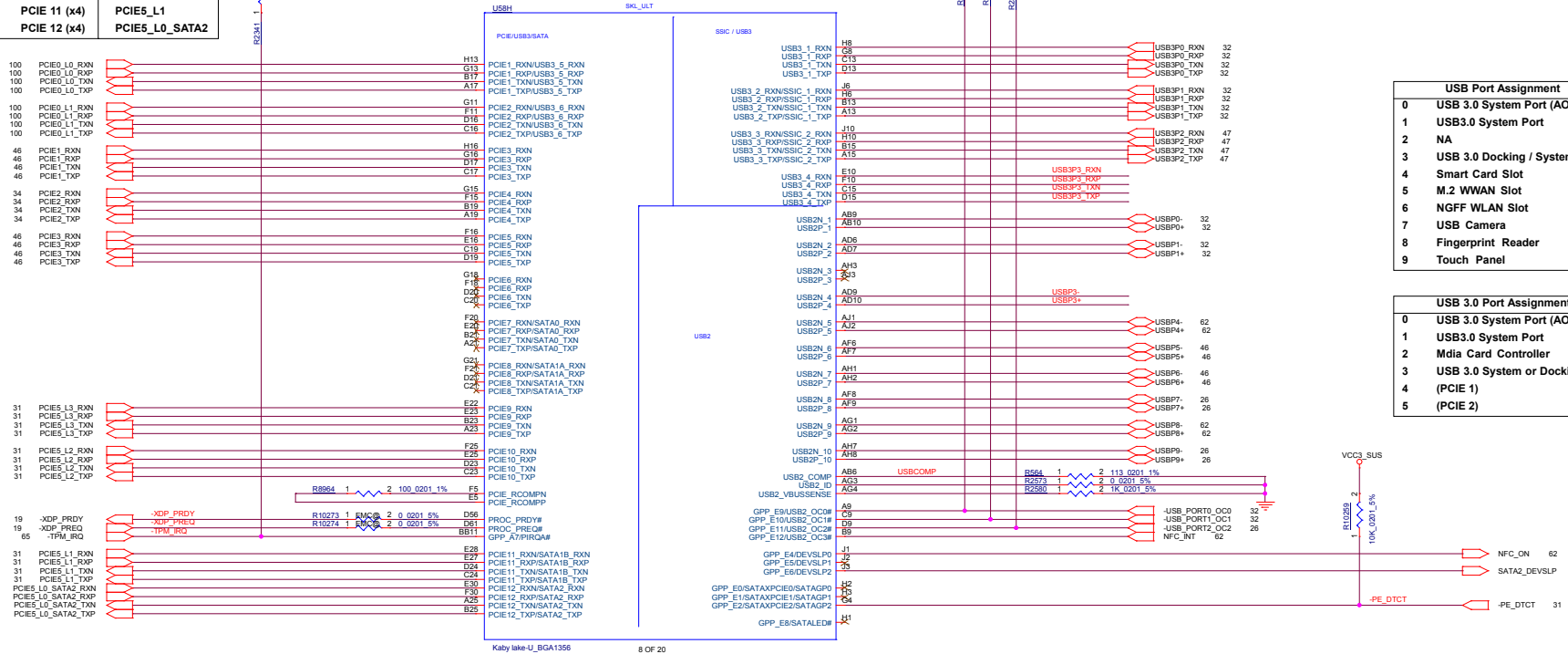
GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" Mode
LOW	Disable "Top Swap" Mode (Default)

← LOGIC

Flexible I/O Configuration			
I/O	High Speed Signals	Configuration	Net Name
Port 1	USB3 1	USB3 1	USB3P0
Port 2	USB3 2/SSIC	USB3 2 (MCC)	USB3P1
Port 3	USB3 3	USB3 3	USB3P2
Port 4	USB3 4	USB3 4	USB3P3
Port 5	USB3 5/PCIE 1	PCIE 1 (x2)	PCIE0_L0
Port 6	USB3 6/PCIE 2	PCIE 2 (x2)	PCIE0_L1
Port 7	PCIE 3 (GbE)	PCIE 3	PCIE1
Port 8	PCIE 4 (GbE)	PCIE 4	PCIE2
Port 9	PCIE 5 (GbE)	PCIE 5	PCIE3
Port 10	PCIE 6	NA	X
Port 11	PCIE 7/SATA 0	NA	X
Port 12	PCIE 8/SATA 1A	NA	X
Port 13	PCIE 9 (GbE)	PCIE 9 (x4)	PCIE5_L3
Port 14	PCIE 10 (GbE)	PCIE 10 (x4)	PCIE5_L2
Port 15	PCIE 11/SATA 1B	PCIE 11 (x4)	PCIE5_L1
Port 16	PCIE 12/SATA 2	PCIE 12 (x4)	PCIE5_L0_SATA2

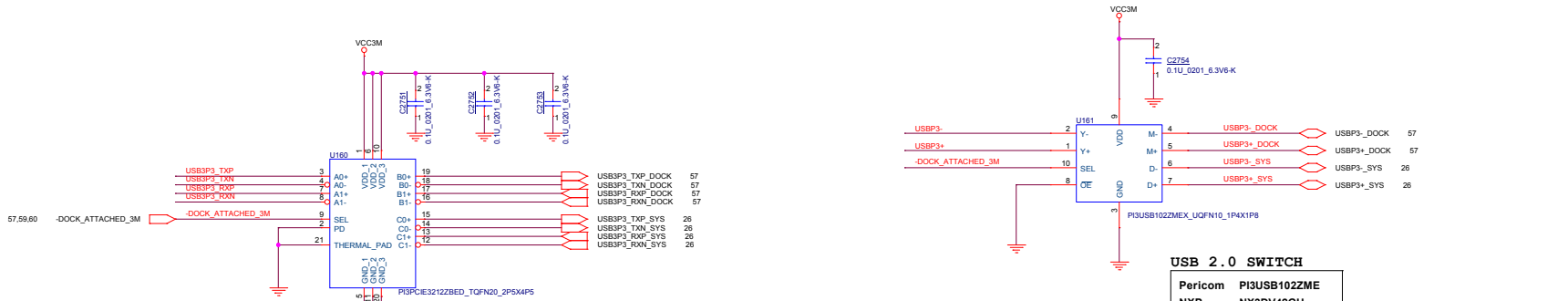
PCIe Port Assignment	
0 (x2)	Thunderbolt
1	M.2 WLAN Slot Port 0
2	GbE PHY
3	M.2 WLAN Slot Port 1
4 (x2)	NA
5 (x4)	PCIe SSD

SATA Port Assignment	
0 (PCIE 7)	
1A SATA SSD	
1B (PCIE 11)	
2 SATA SSD	



USB Port Assignment	
0	USB 3.0 System Port (AOU)
1	USB3.0 System Port
2	NA
3	USB 3.0 Docking / System Port (3rd Port)
4	Smart Card Slot
5	M.2 WWAN Slot
6	NGFF WLAN Slot
7	USB Camera
8	Fingerprint Reader
9	Touch Panel

USB 3.0 Port Assignment	
0	USB 3.0 System Port (AOU)
1	USB3.0 System Port
2	Media Card Controller
3	USB 3.0 System or DockingPort
4	(PCIE 1)
5	(PCIE 2)



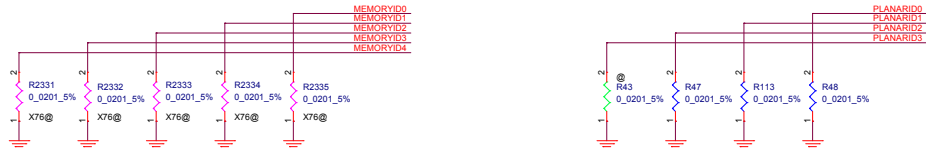
USB 3.0 MUX	
Pericom	P13PCIE3212ZBE
NXP	CBTL02043ABQ
NXP	CBTL02042ABQ

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Title		Revision	
CPU(8/16) : PCIE/USB/SATA		Rev 0.01	
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TABLE

MEMORYID[4..0]	U125, U126, U127, U128			
00000b	Micron	MT40A512M16HA-083E:A	8Gbit SDP	4GB (2133)
00001b	Micron	MT40A1G16HBA-083E:A	16Gbit DDP	8GB (2133)
00010b	Samsung	K4A8G165WB-BCPB	8Gbit SDP	4GB (2133)
00011b	SK Hynix	T.B.D.		
00100b	SK Hynix	T.B.D.		
01000b	Micron	MT40A512M16JY-083E:B	8Gbit SDP	4GB (2400)
01001b	Micron	MT40A1G16WBU-083E:B	16Gbit DDP	8GB (2400)
01010b	Samsung	K4A8G165WB-BCRC	8Gbit SDP	4GB (2400)
01011b	Samsung	K4AAG165WB-MCRC	16Gbit DDP	8GB (2400)
01100b	SK Hynix	H5AN8G6NAFR-UHC	8Gbit SDP	4GB (2400)
11111b	NO_ASM		No Soldered Memory	



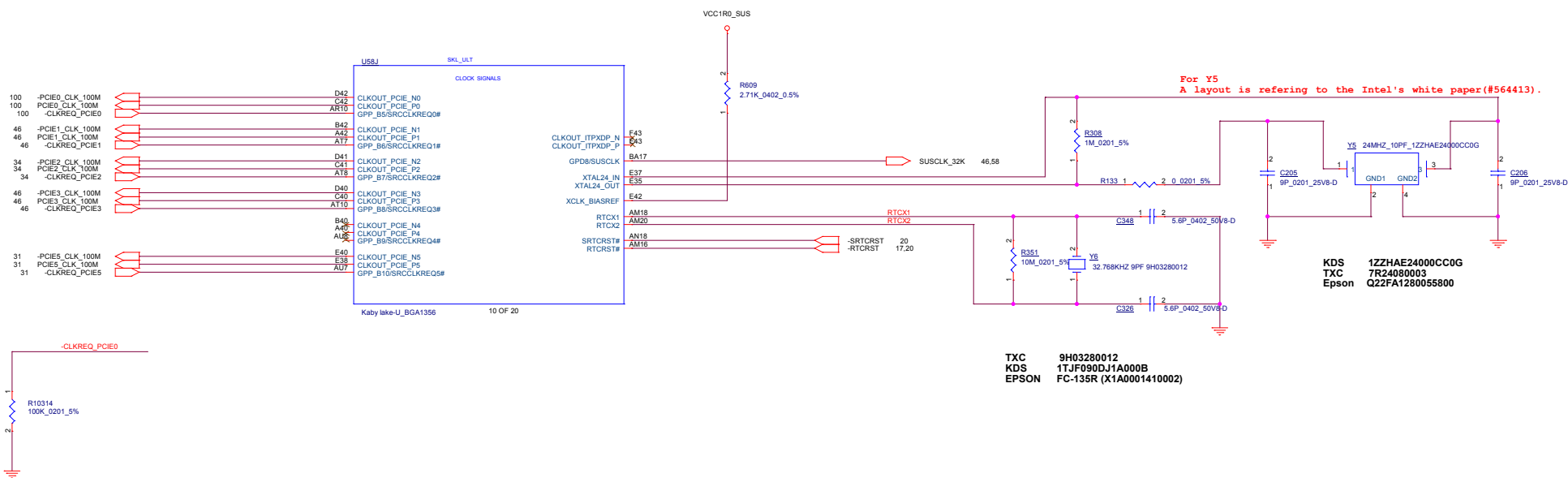
TABLE

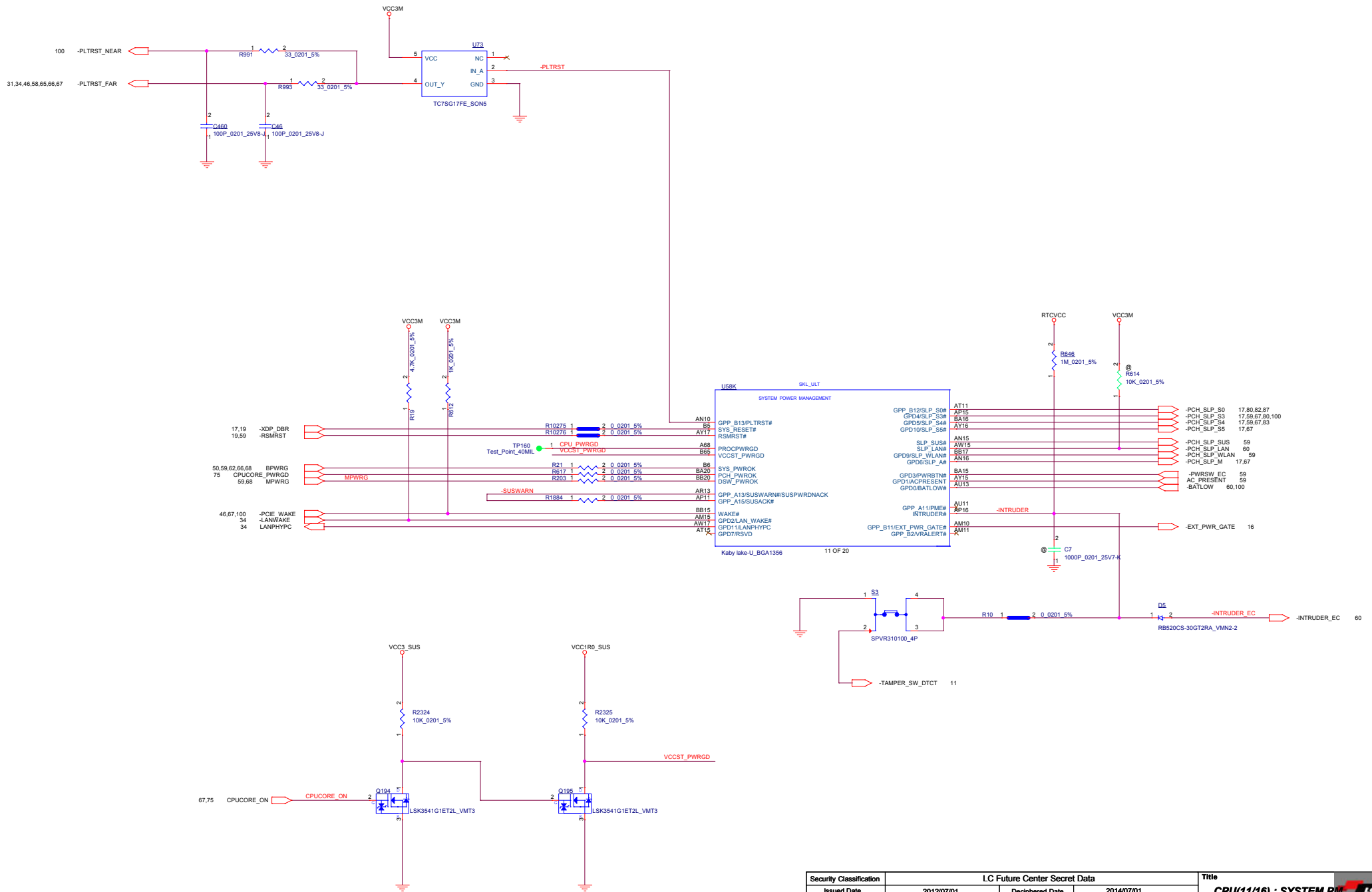
LEVEL	PLANAR ID			
	3	2	1	0
	R43	R47	R113	R48
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM


TABLE

LEVEL	PLANARID[3..0]
PDV	0000B
SDV	0001B
FVT	0010B
ME SIT	0011B
SIT	0100B / 0101B
SIT-R	0110B / 0111B
SVT	1000B
SVT-R	
SOVP	

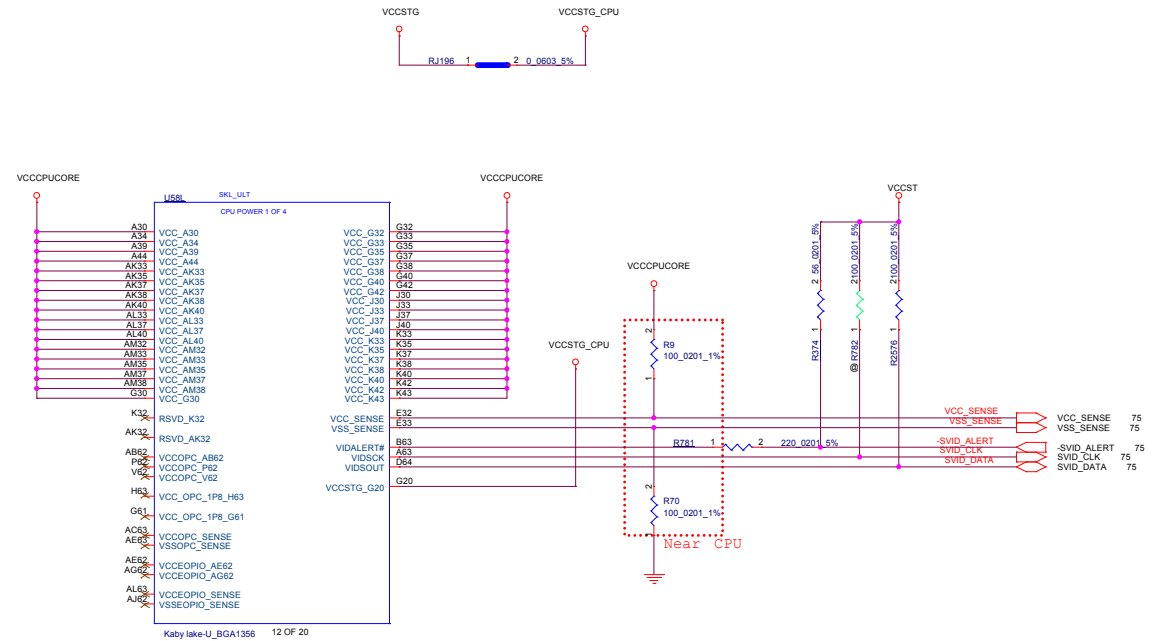
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		2014/07/01		CPU(9/16) : CSI-2/EMMC			
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				Rev		0.01	






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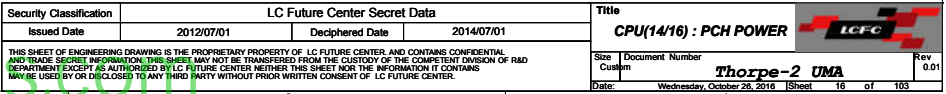
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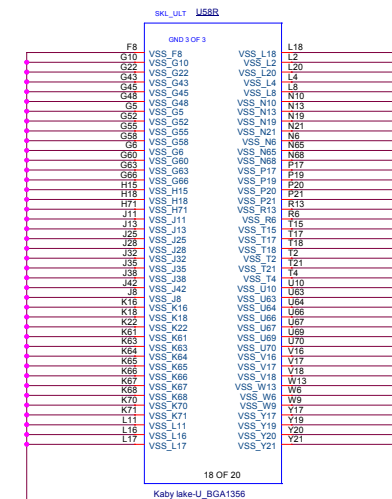
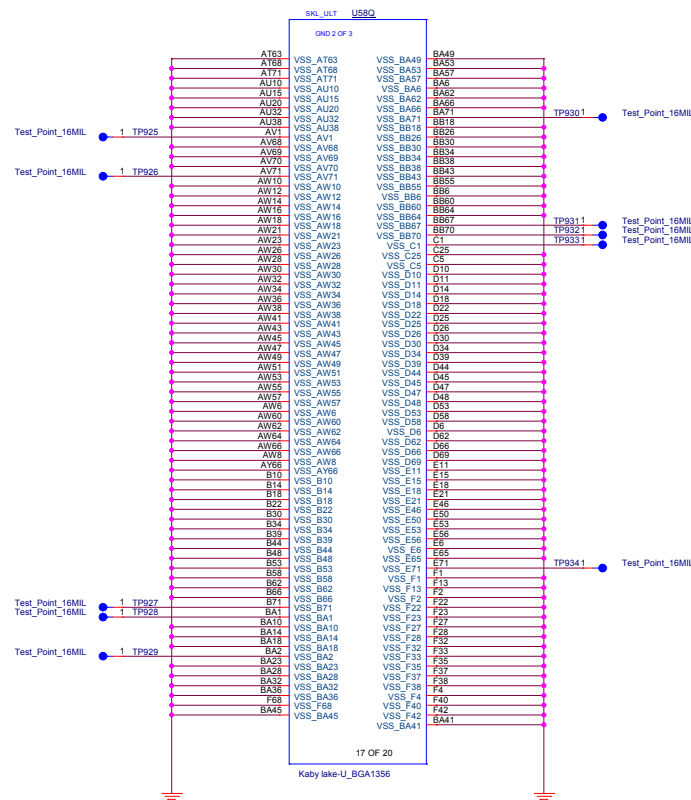
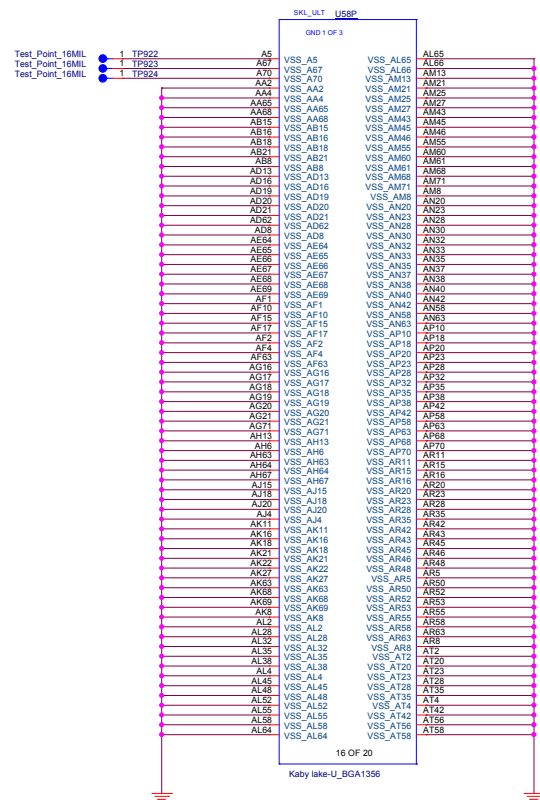
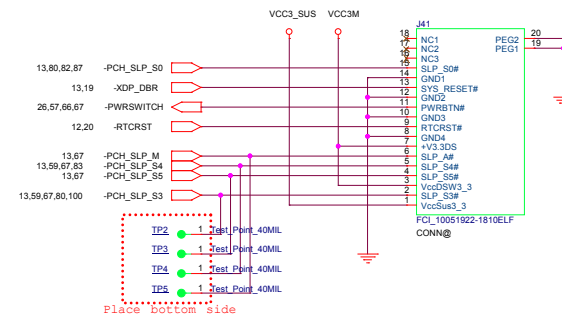
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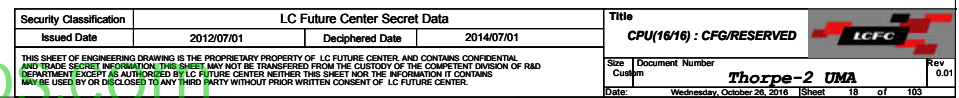


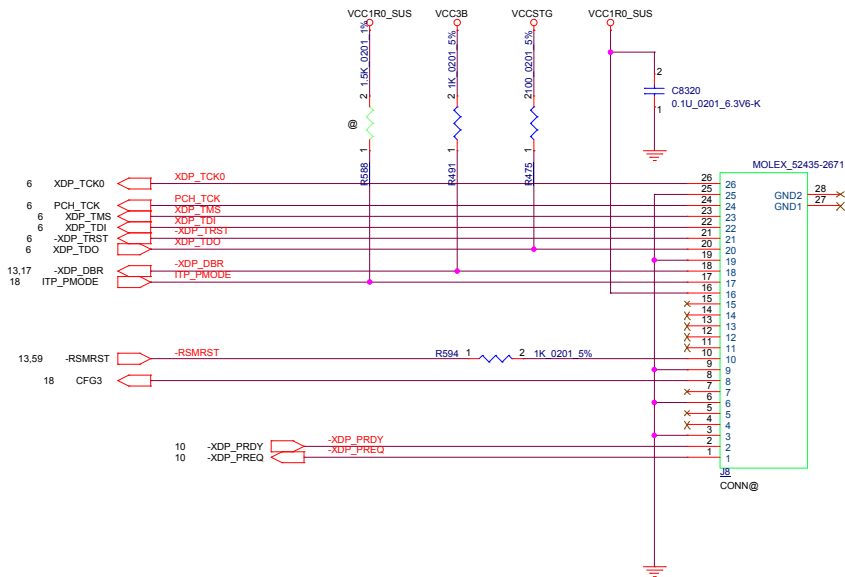
## APS/PETS Interface



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CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted 1: No Stall 0: Stall
CFG3 : MSR Privacy Bit Feature 1: MSR (C80h) bit[0] setting 0: MSR (C80h) bit[0] overridden
CFG4 : eDP Enable 1: Disabled 0: Enabled
CFG9 : SVID Bus Communication 1: Enabled 0: Disabled






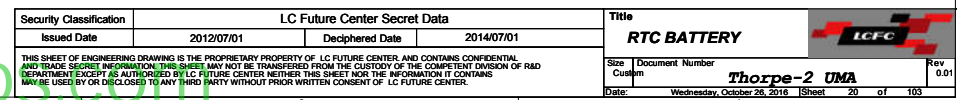
TABLE

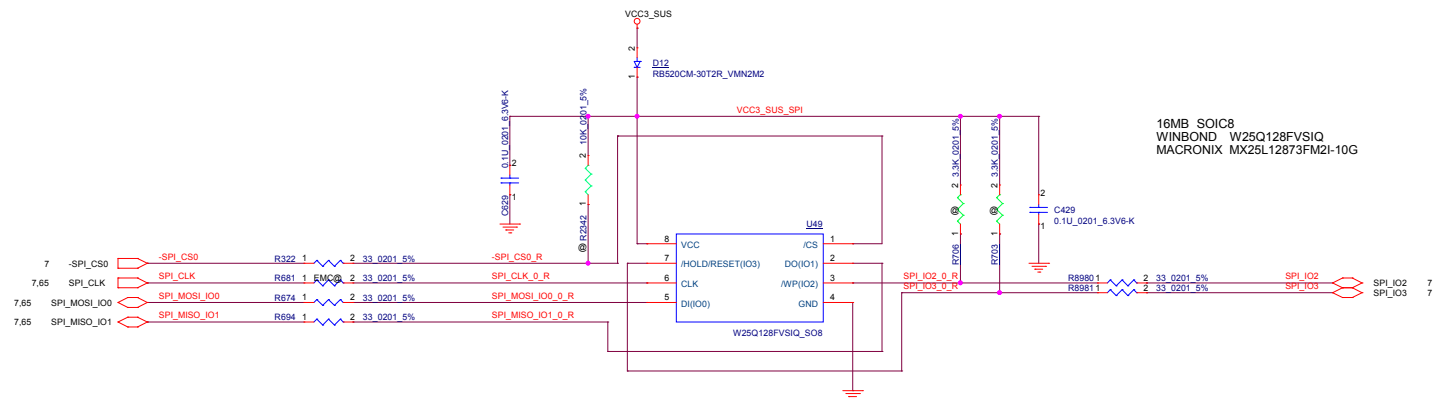
Logic	Ref Des	Merged	DCI 2.0
Page 6	R2	ASM	ASM
Page 7	R2559	ASM	NO_ASM
Page 18	R1892	ASM	NO_ASM
Page 19	J8	ASM	NO_ASM
	C8320	ASM	NO_ASM
	R475	ASM	ASM
	R491	ASM	ASM
	R588	ASM	NO_ASM
	R594	ASM	NO_ASM
	R2494	ASM	NO_ASM

↑  
LOGIC

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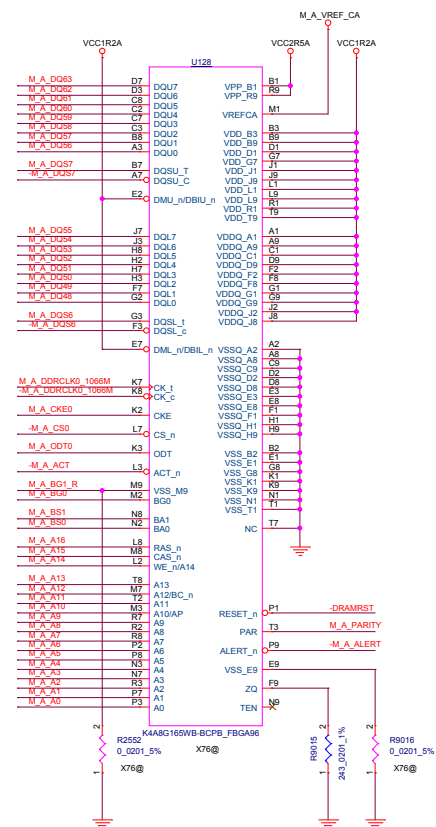
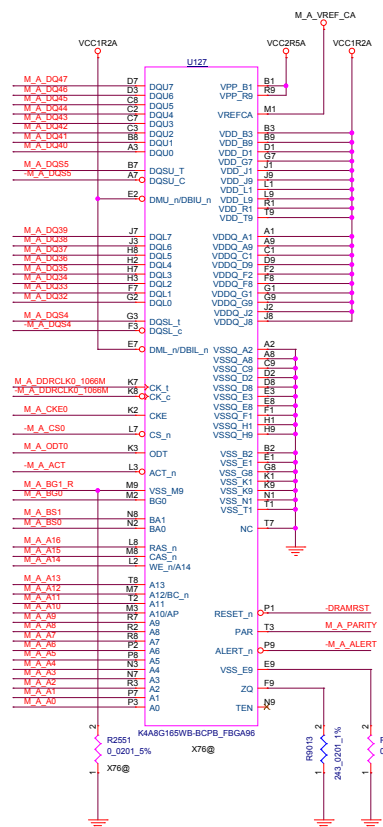
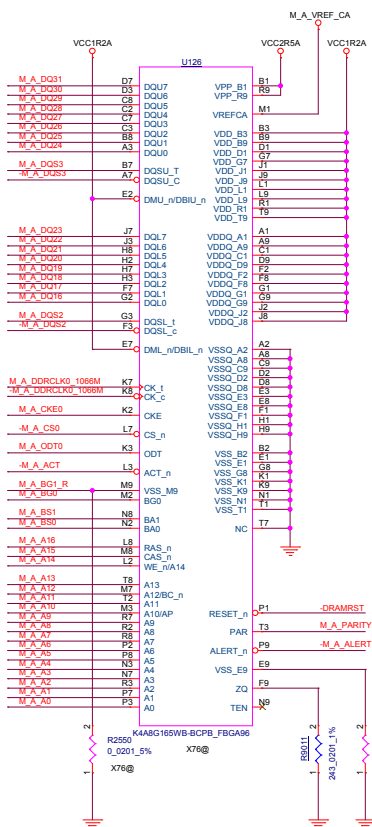
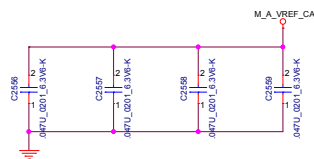




TABLE

SF100 PIN HEADER INTERFACE (TOP VIEW)							
1	VCC	D12.1	GND	GND	2		
3	CS#	R322.2	GND	R681.2	CLK	4	
5	MISO	R684.2	N/A	R674.2	MOSI	6	
7	(KEY)	N/A	N/A		(RESET)	8	

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3 M\_A\_DORCLK0\_1066M

3 -M\_A\_DORCLK0\_1066M

4 M\_A\_BG1

4 -M\_A\_BG1

5.24 -DRAMRST

4.23 M\_A\_PARITY

4.23 -M\_A\_ALERT

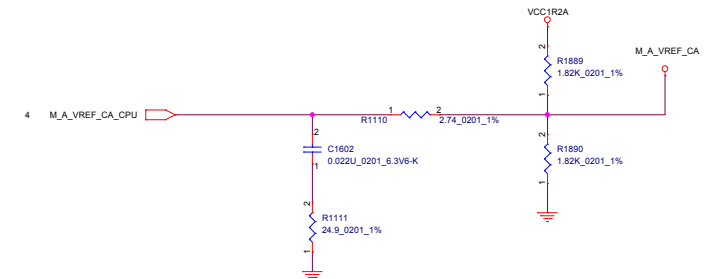
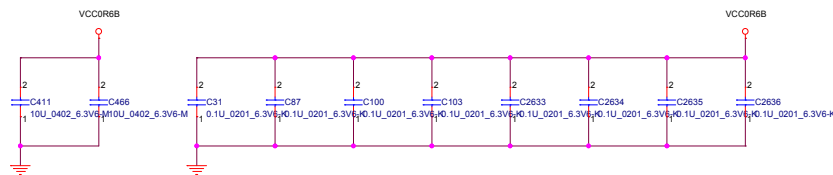
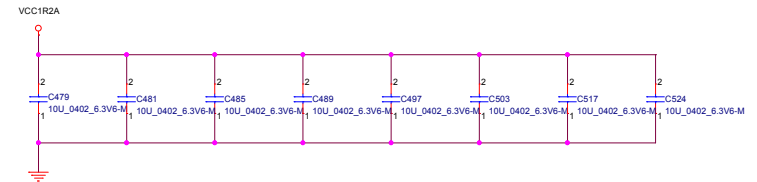
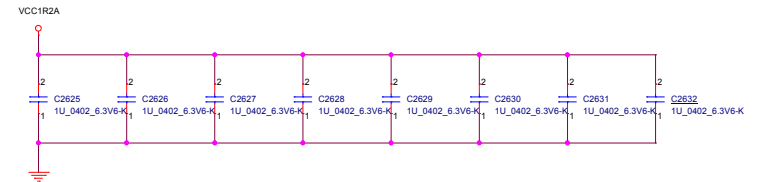
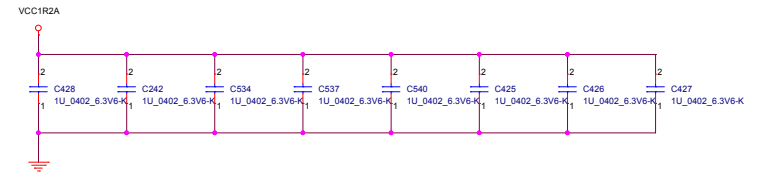
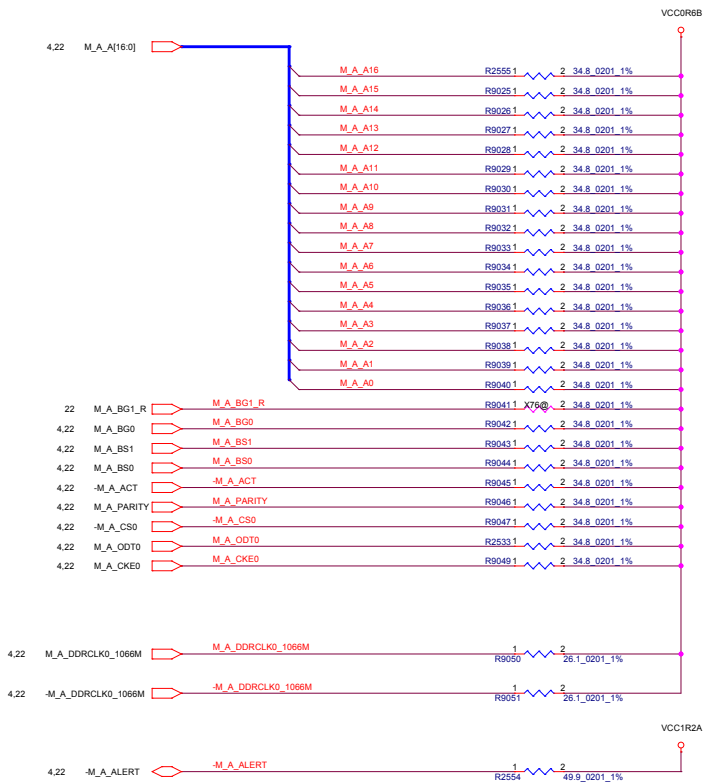
2553 X76 0.0201\_5%


2 M\_A\_BG1\_R

2 C1063 0.1u\_0201\_6.3V6-K

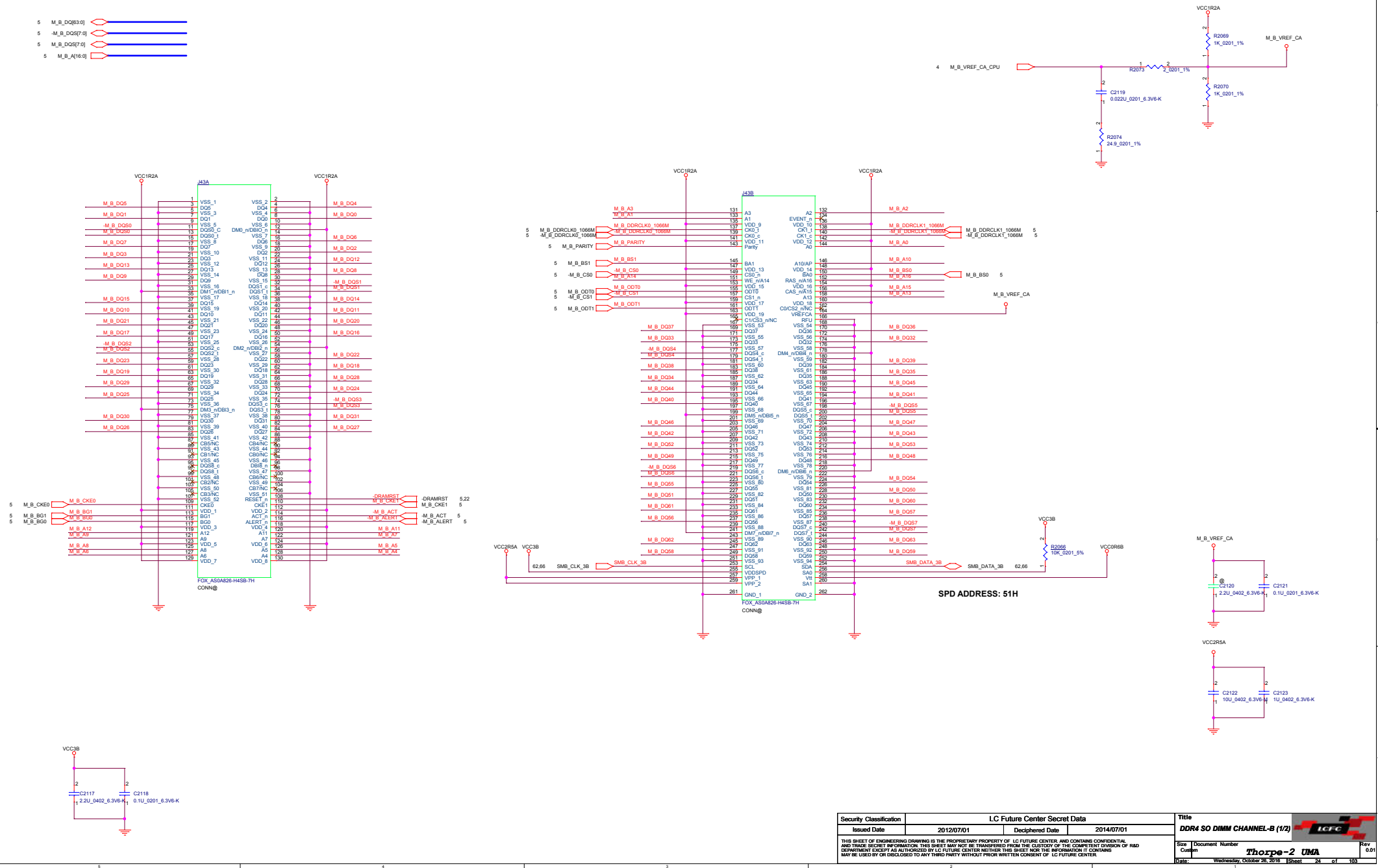
1 10k

1.0V

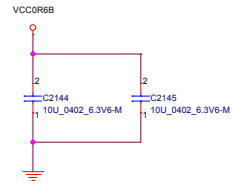
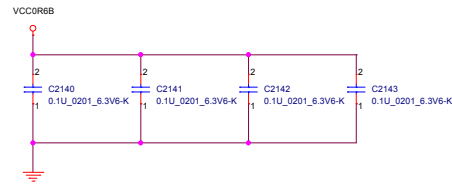
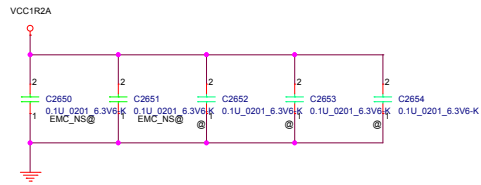
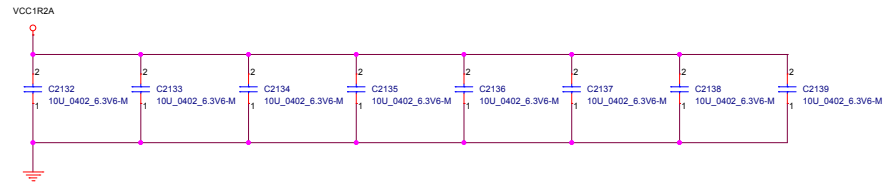
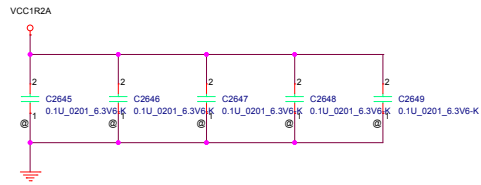
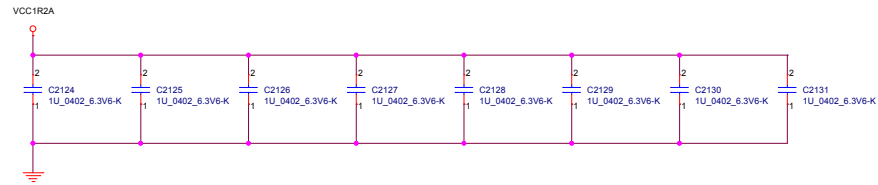
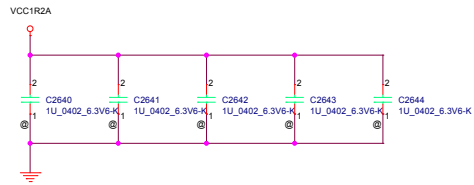


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DDR4 BASE MEMORY CH-A (2/2)							
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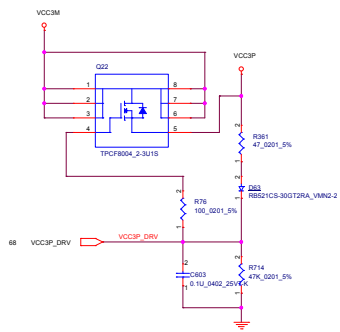




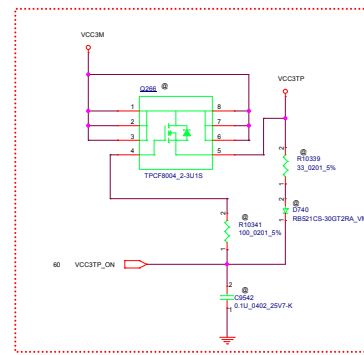


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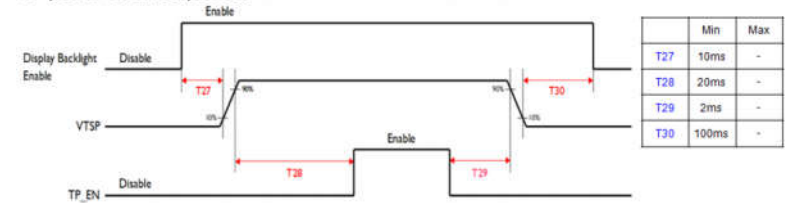
Security Classification				LC Future Center Secret Data				Title	
Issued Date				2012/07/01		Deciphered Date		2014/07/01	
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				Cust		Thorpe-2 UMA		0.01	
				Date:		Wednesday, October 26, 2018		Sheet 25 of 103	



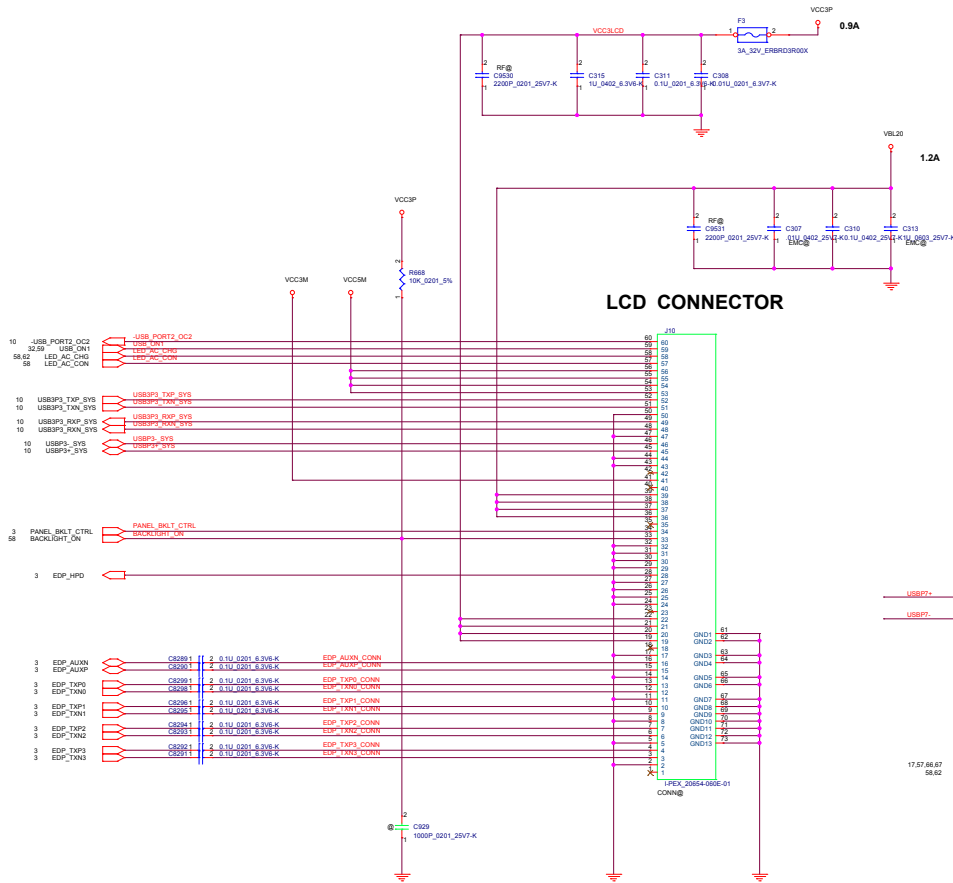
	Touch Panel		Sequence
	Support	Non-Support	
X10386	ASN	No ASN	
F42	ASN	No ASN	
D739	ASN	No ASN	
C0641	ASN	No ASN	
Q266	ASN	No ASN	
X10941	ASN	No ASN	
C0642	ASN	No ASN	
X10950	ASN	No ASN	
D740	ASN	No ASN	
X10957	ASN	No ASN	
X10958	ASN	No ASN	
X26	No ASN	ASN	
F54	No ASN	ASN	
X10959	No ASN	ASN	
X2412	No ASN	ASN	



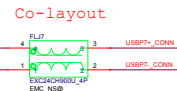
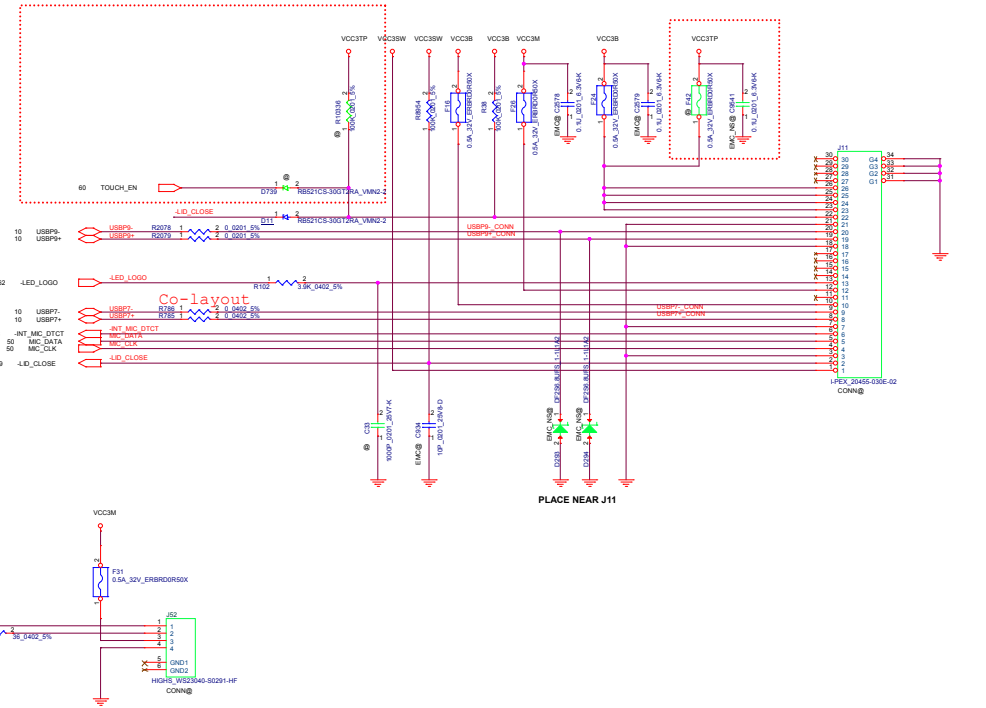
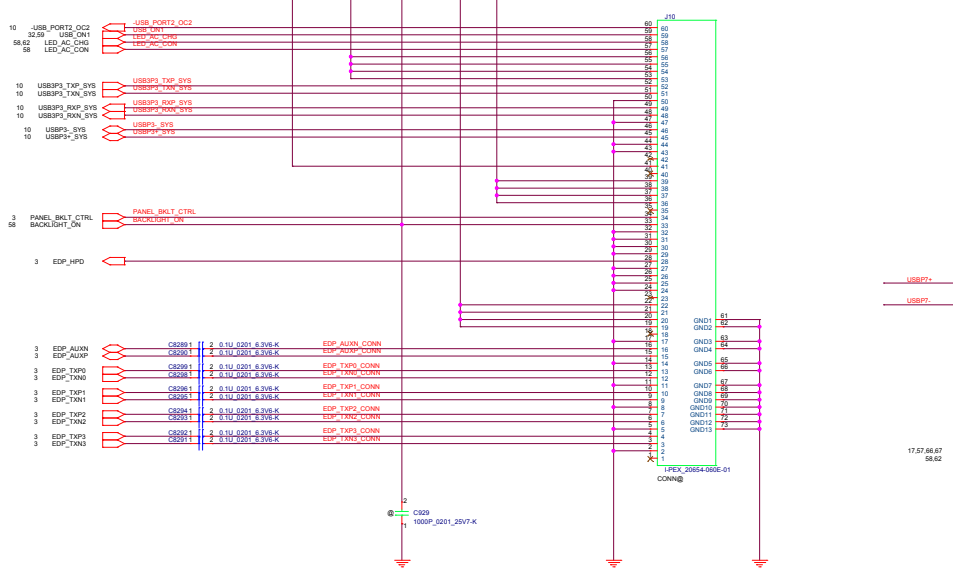
## TP power on/off Sequence:



	Min	Max
T27	10ms	-
T28	20ms	-
T29	2ms	-
T30	100ms	-



## LCD CONNECTOR



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Doc/USB/LD/MIC/CAMERA/PWR SW	Document Number	Doc/USB/LD/MIC/CAMERA/PWR SW	Document Number	Doc/USB/LD/MIC/CAMERA/PWR SW	Document Number
Doc/USB/LD/MIC/CAMERA/PWR SW	Doc/USB/LD/MIC/CAMERA/PWR SW	Doc/USB/LD/MIC/CAMERA/PWR SW	Doc/USB/LD/MIC/CAMERA/PWR SW	Doc/USB/LD/MIC/CAMERA/PWR SW	Doc/USB/LD/MIC/CAMERA/PWR SW

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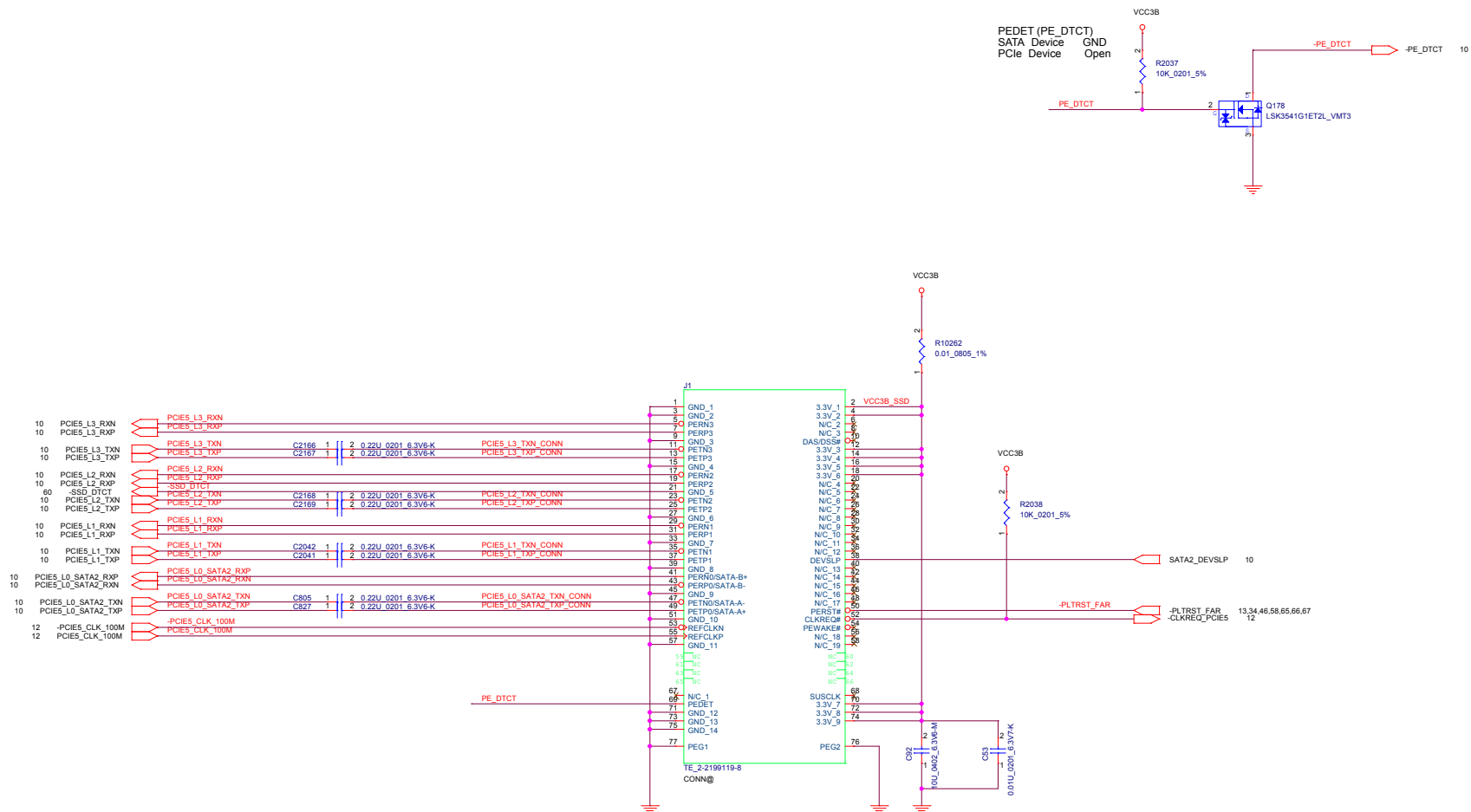
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					<small>Scale</small> <small>Thorpe-2 UMA</small>
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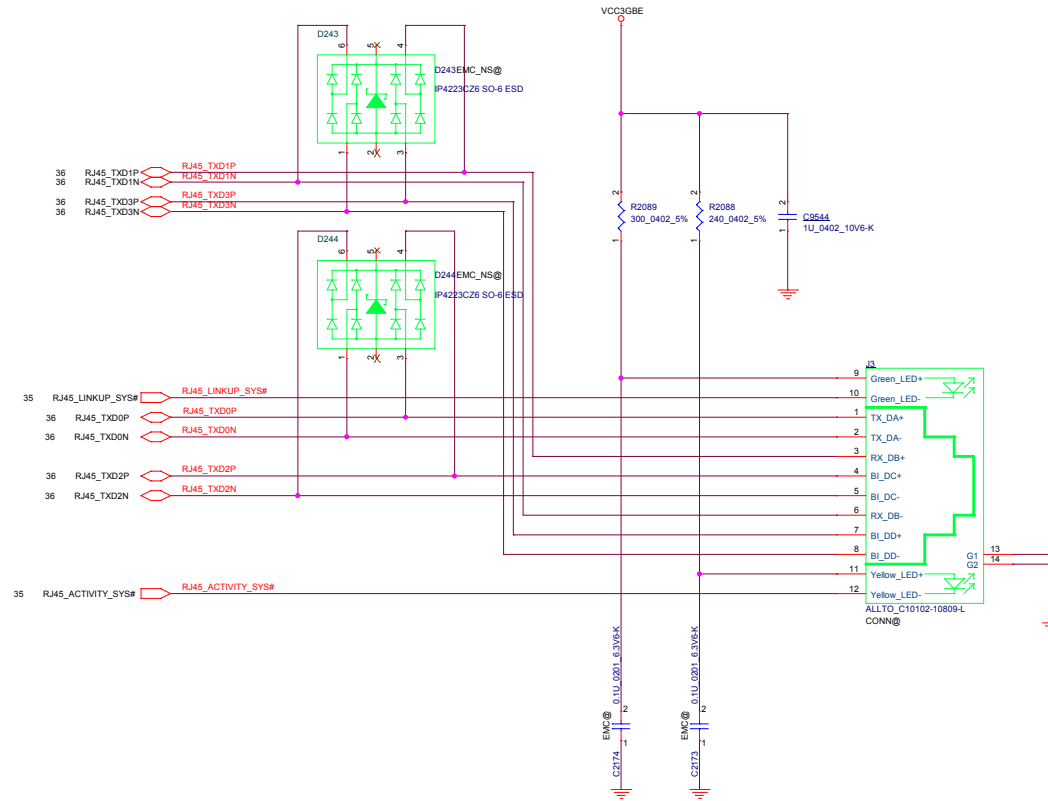
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Cus	Thorpe-2 UMA				0.01
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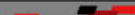










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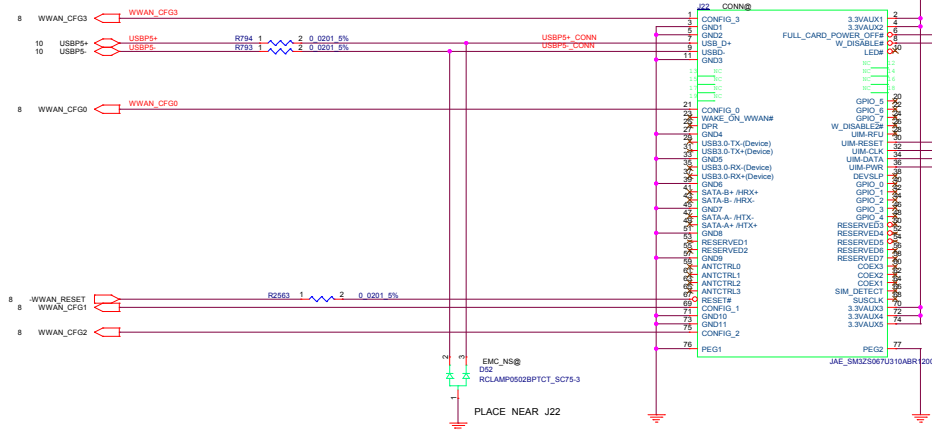
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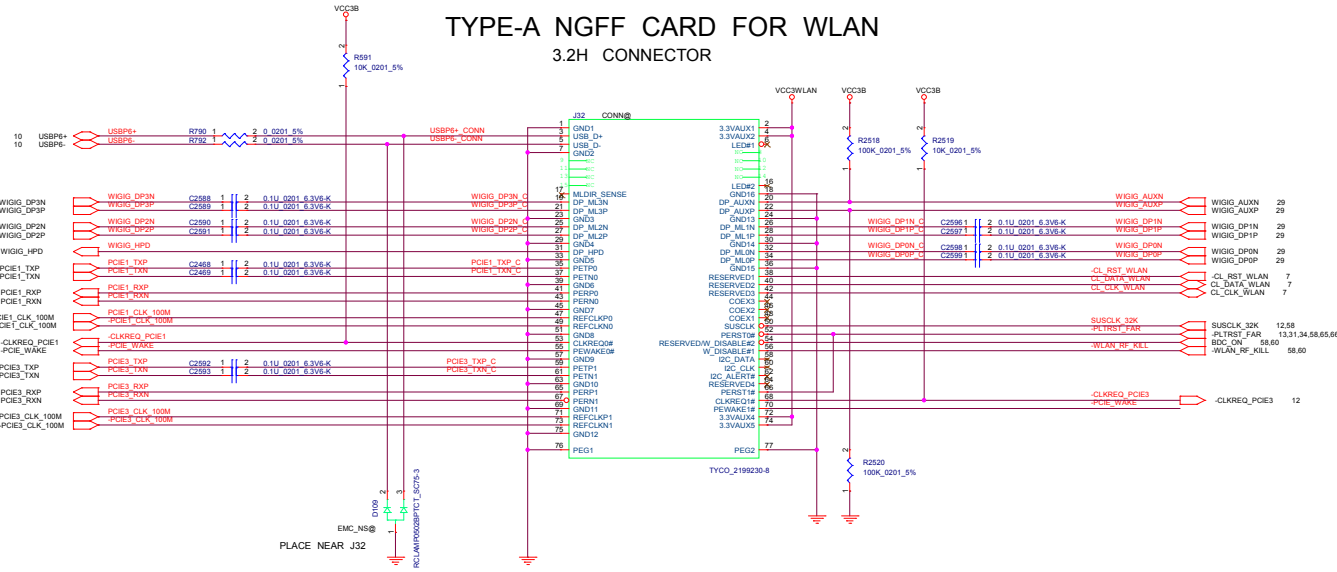
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					<small>Scale</small> <b>Thorpe-2 UMA</b> <small>Rev</small> 0.01
					<small>Date:</small> Wednesday, October 26, 2016 <small>Sheet</small> 45 <small>of</small> 103




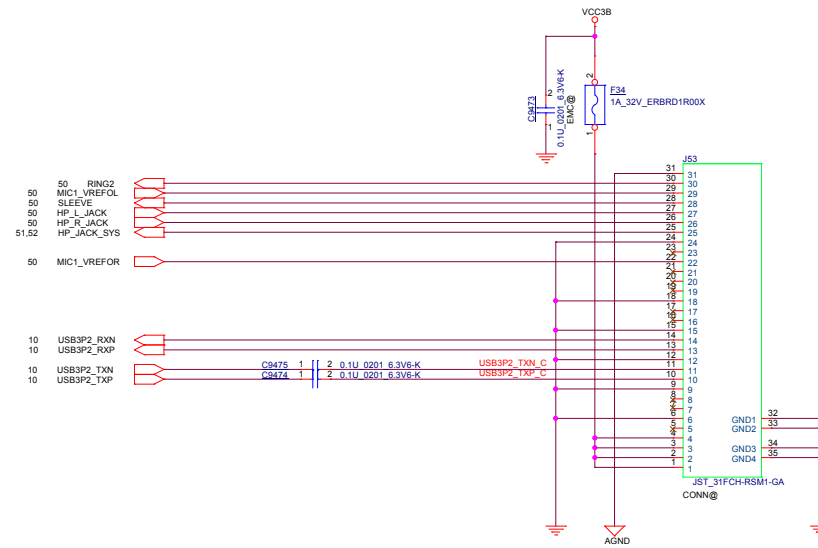
[illegible]

Three circuit diagrams are shown, each representing a different capacitor connected to the VCC3\_WAN pin. Each diagram includes a 100k resistor connected to ground and a capacitor connected to the pin. The capacitors are labeled C2062, C2063, and C2068. The values and specifications for each capacitor are as follows:

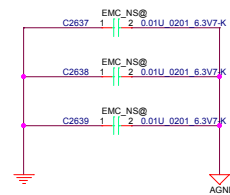
- C2062:** 0.1uF, 50V, 5%, EAC
- C2063:** 0.1uF, 50V, 5%, EAC
- C2068:** 4.7uF, 50V, 5%, EAC




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Reserved for EMC/RF solution



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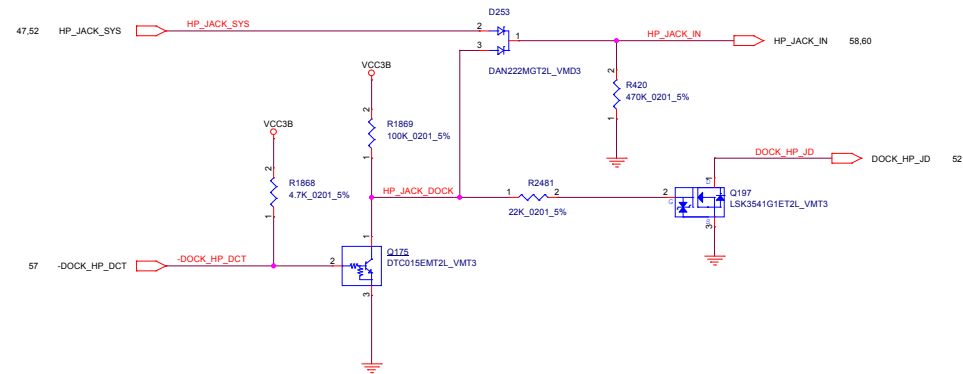


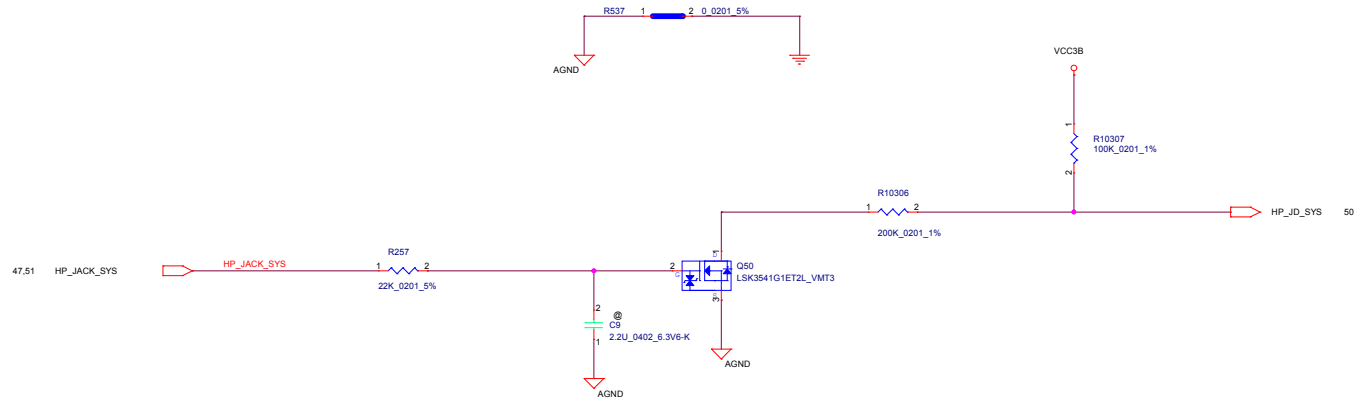


TABLE

DOCKING	SUPPORT	NON-SUPPORT
R1869	ASM	NO_ASM
Q175	ASM	NO_ASM
R2481	ASM	NO_ASM
Q197	ASM	NO_ASM

↑  
LOGIC

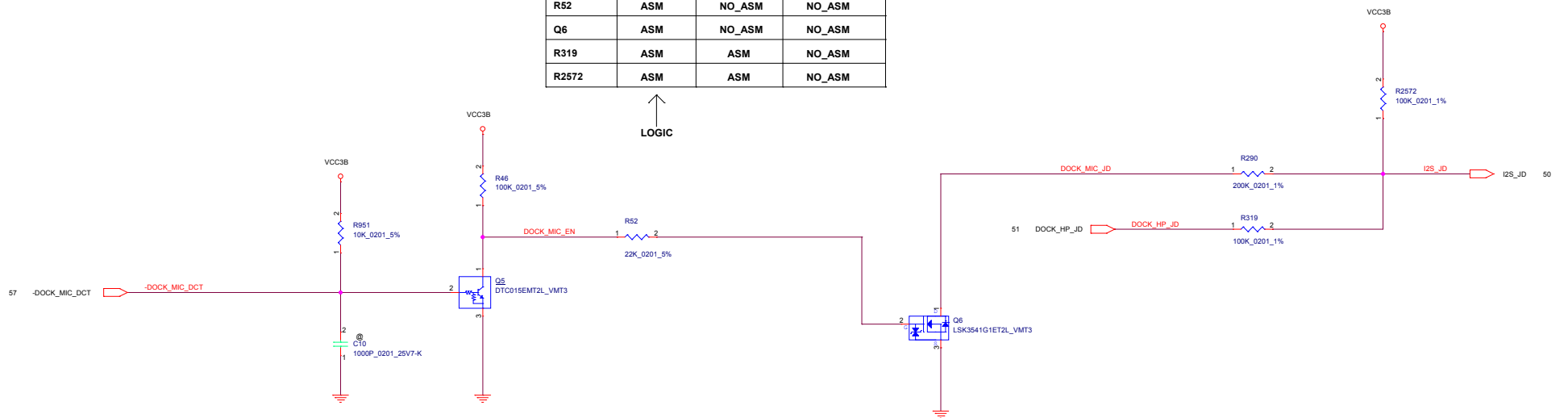




TABLE

DOCKING	SUPPORT		NON-SUPPORT
	ENABLE	DISABLE	
R951	ASM	NO_ASM	NO_ASM
R290	ASM	NO_ASM	NO_ASM
R46	ASM	NO_ASM	NO_ASM
Q5	ASM	NO_ASM	NO_ASM
R52	ASM	NO_ASM	NO_ASM
Q6	ASM	NO_ASM	NO_ASM
R319	ASM	ASM	NO_ASM
R2572	ASM	ASM	NO_ASM

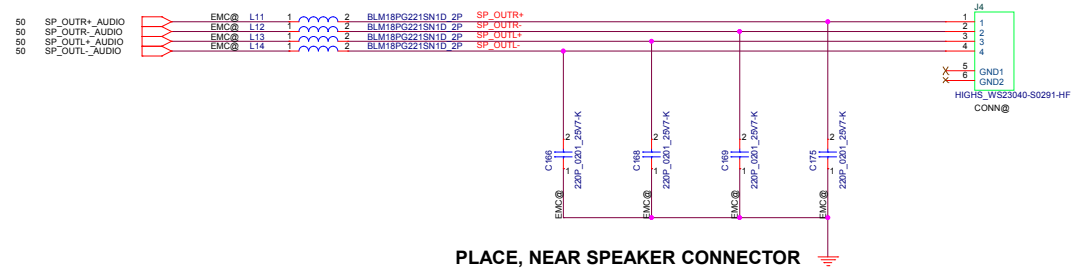
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LOGIC



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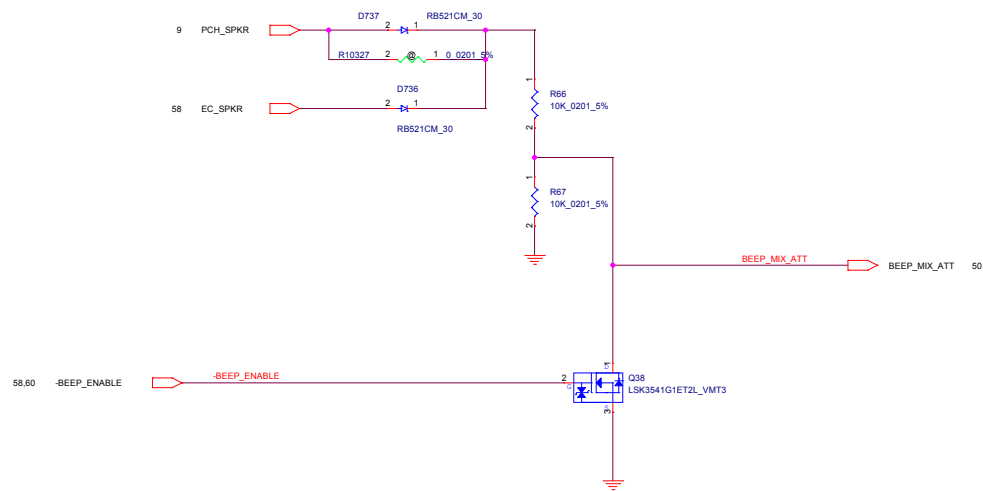
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				Sheet		55 of 103	

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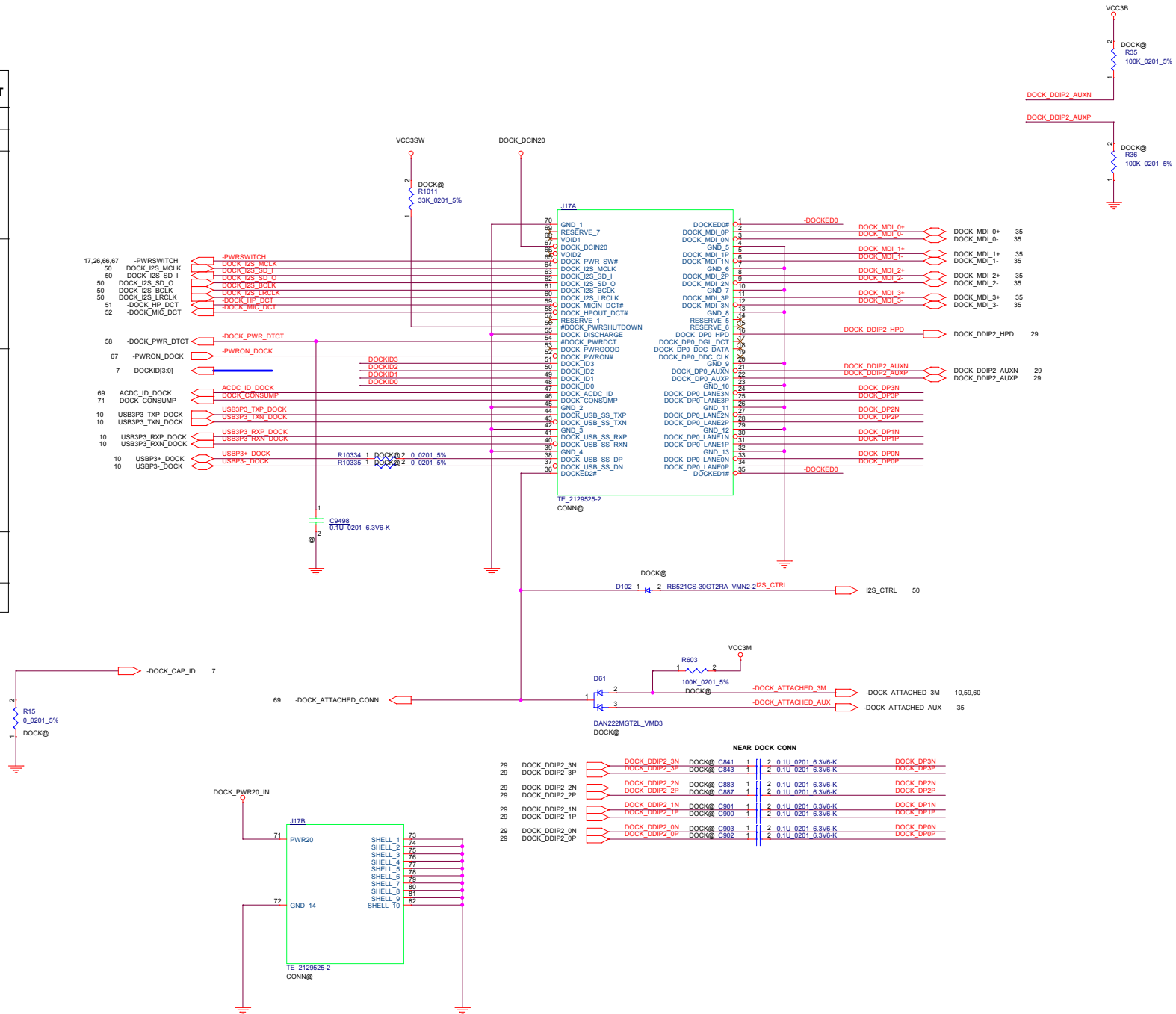
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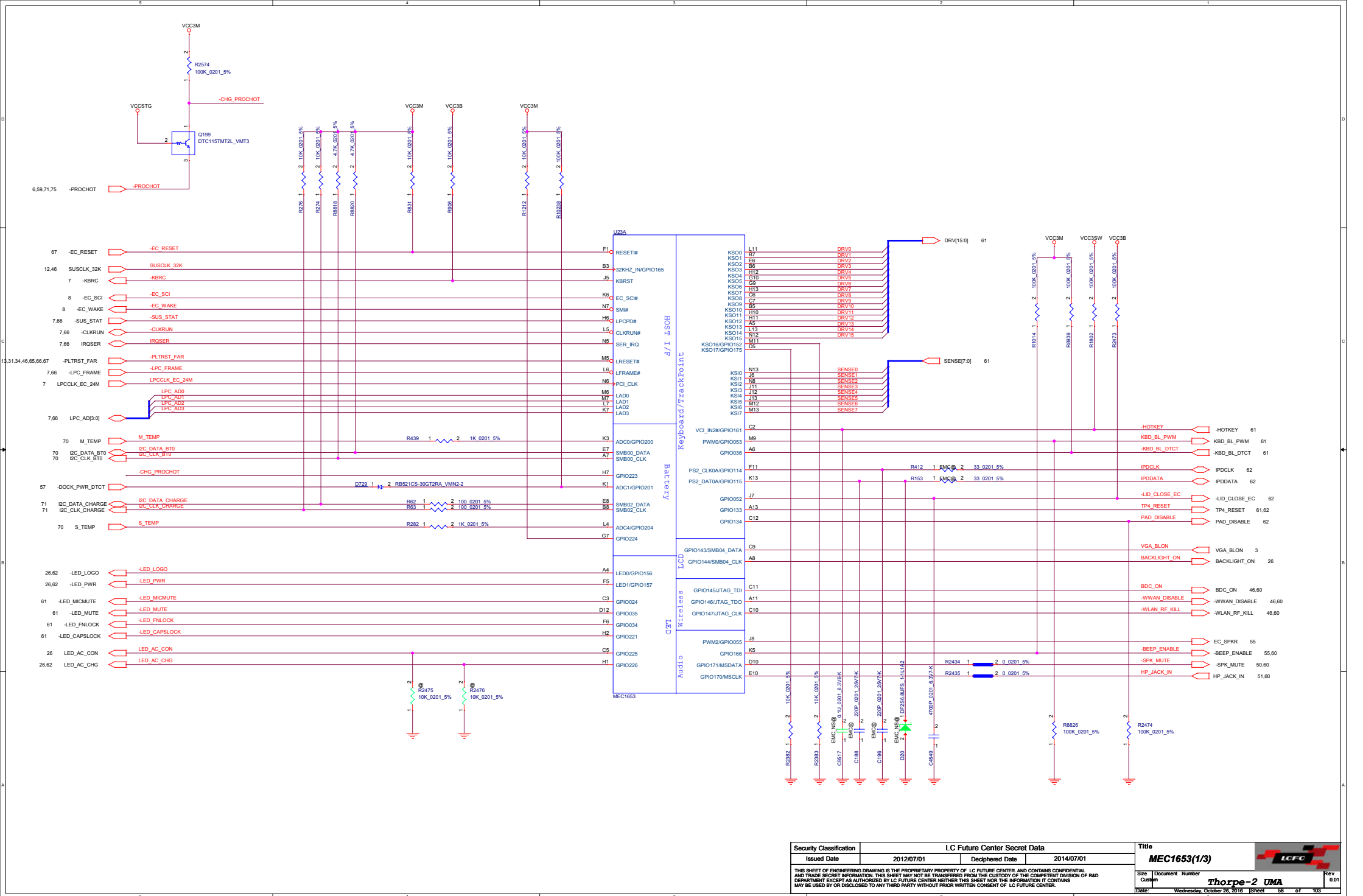
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Date:	Wednesday, October 26, 2016				Sheet 56 of 103






LOGIC		
TABLE	DOCKING SUPPORT	NON-SUPPORT
J17	ASM	NO ASM
R1011	ASM	NO ASM
D2	ASM	NO ASM
R603	ASM	ASM
D61	ASM	NO ASM
D102	ASM	NO ASM
C24	ASM	NO ASM
Q85	ASM	NO ASM
R95	ASM	NO ASM
R731	ASM	NO ASM
R657	ASM	NO ASM
C841	ASM	NO ASM
C843	ASM	NO ASM
C883	ASM	NO ASM
C887	ASM	NO ASM
C901	ASM	NO ASM
C900	ASM	NO ASM
C903	ASM	NO ASM
C902	ASM	NO ASM
R35	ASM	NO ASM
R36	ASM	NO ASM
R15	ASM	NO_ASM





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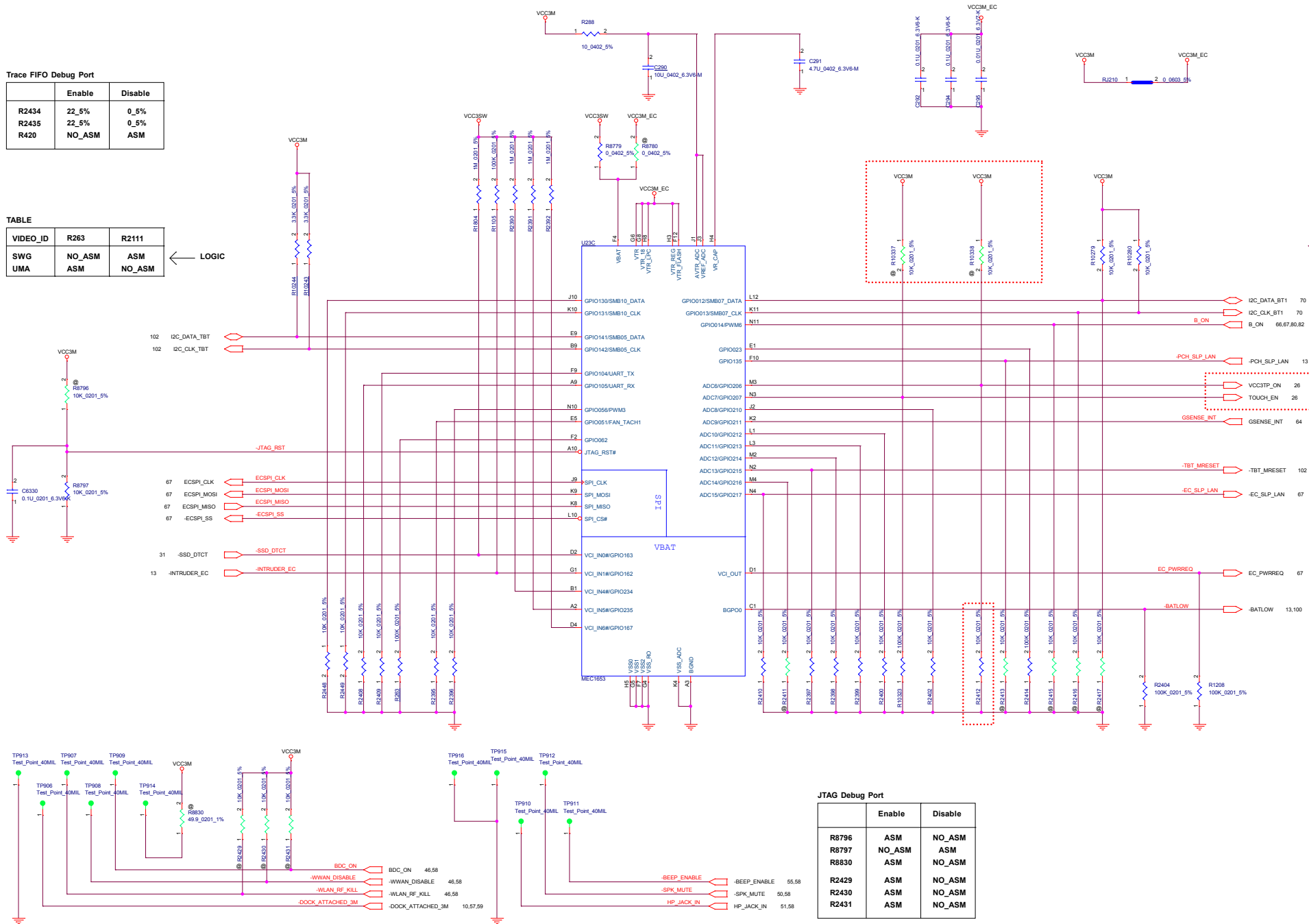
## Trace FIFO Debug Port

	Enable	Disable
R2434	22_5%	0_5%
R2435	22_5%	0_5%
R420	NO_ASM	ASM

## TABLE

VIDEO_ID	R263	R2111
SWG	NO_ASM	ASM
UMA	ASM	NO_ASM

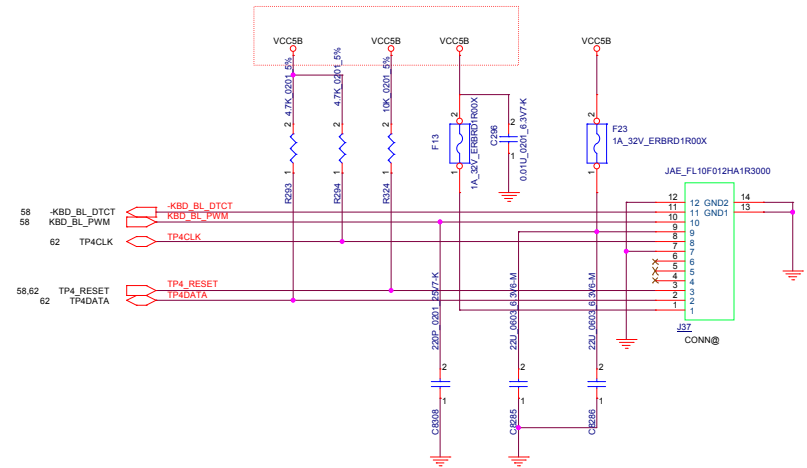
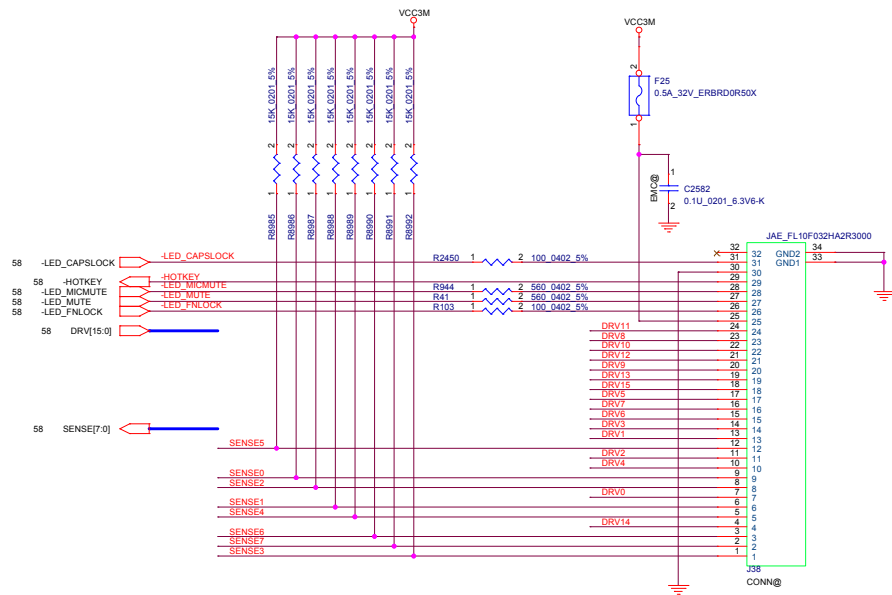
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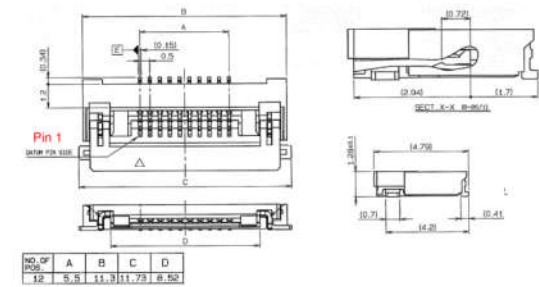
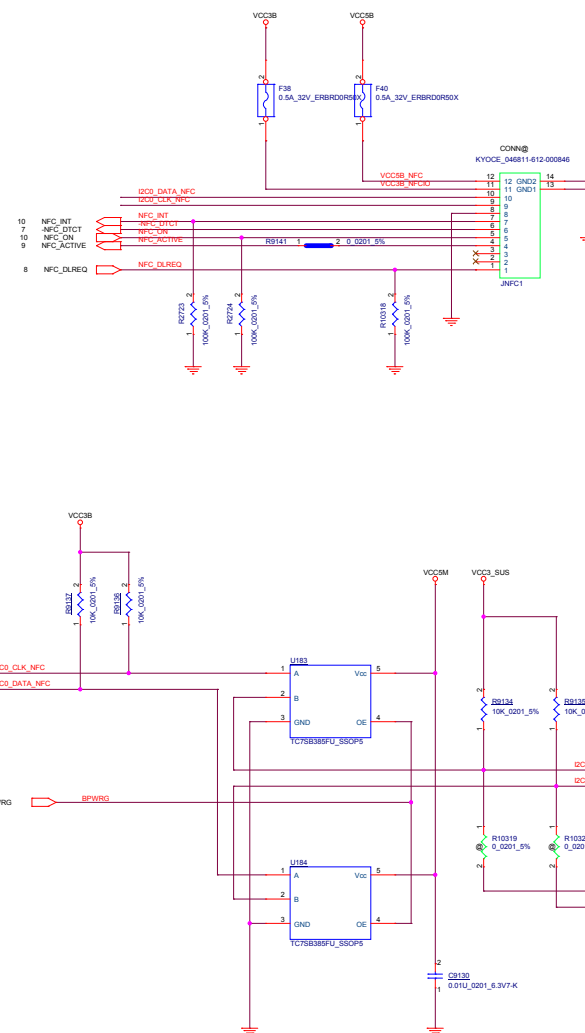
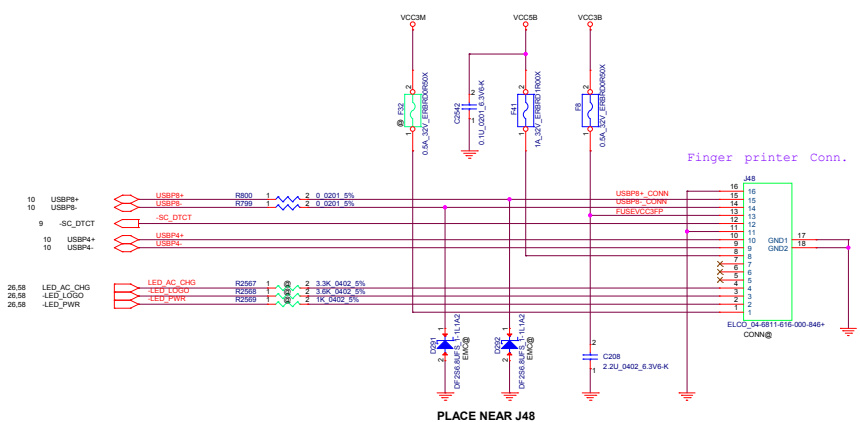
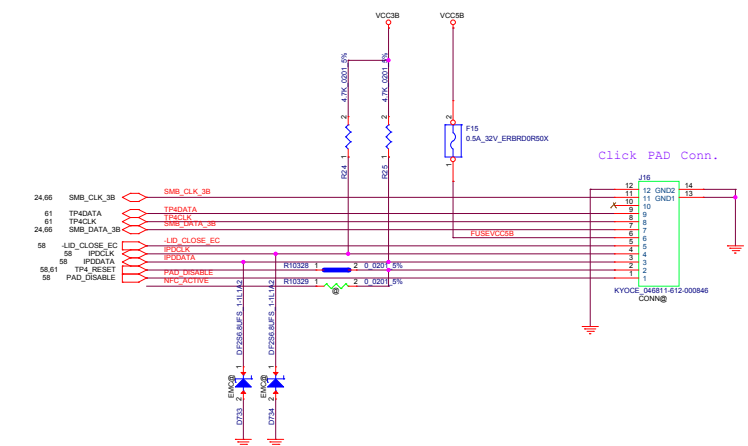
## JTAG Debug Port

	Enable	Disable
R8796	ASM	NO_ASM
R8797	NO_ASM	ASM
R8830	ASM	NO_ASM
R2429	ASM	NO_ASM
R2430	ASM	NO_ASM
R2431	ASM	NO_ASM

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Date:		Wednesday, October 26, 2016		Sheet 61 of 103	

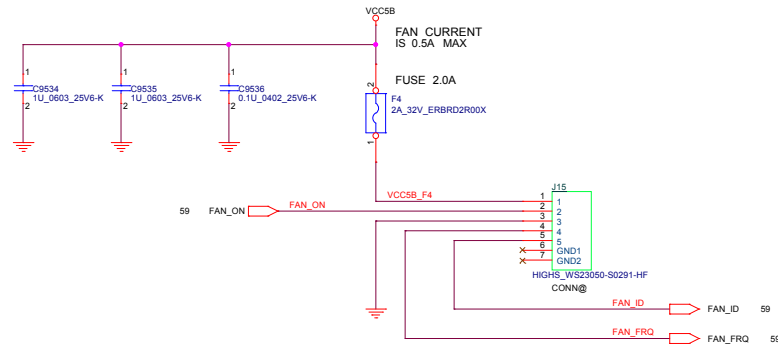



Remark: The connector is bottom conduct with golden plating of FPC cable

Pin	Symbol	Pin Type	Refer	Description
1	VBAT	Input Power	N/A	Power supply from system (4.5V - 5.5V)
2	PVDD	Input Power	N/A	Power supply to I/O (3.0V - 3.6V)
3	I2C_SDA	I/O	PVDD	I2C data
4	I2C_SCL	I	PVDD	I2C clock
5	GND	G	N/A	Ground
6	IRQ	O	PVDD	Interrupt from NFC module to the host (Host_Wake)
7	NFC_Presence	G	N/A	Connect to ground for NFC module presence bit (Low active)
8	VEN	I	VBAT	Reset pin. Set the device in Hard Power Down
9	TX_PWR_REQ	O	VDD	(External TX power supply request) (Active high 1.8V level output) Indicates NFC busy state during NFC communication to touchpad
10	PMUVCC	Input Power	N/A	Power supply to UIICC(1.78V~3.3V)
11	SWIO_UICC	I/O	VDD(SIM)	SWP data connection to SIM
12	DWL_REQ	I	PVDD	Firmware download control pin
S1	GND	G	N/A	Ground
S2	GND	G	N/A	Ground

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Wednesday, October 26, 2016		10/26/16		10/26/16	

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Date:		Wednesday, October 26, 2016		Sheet		63 of 103	

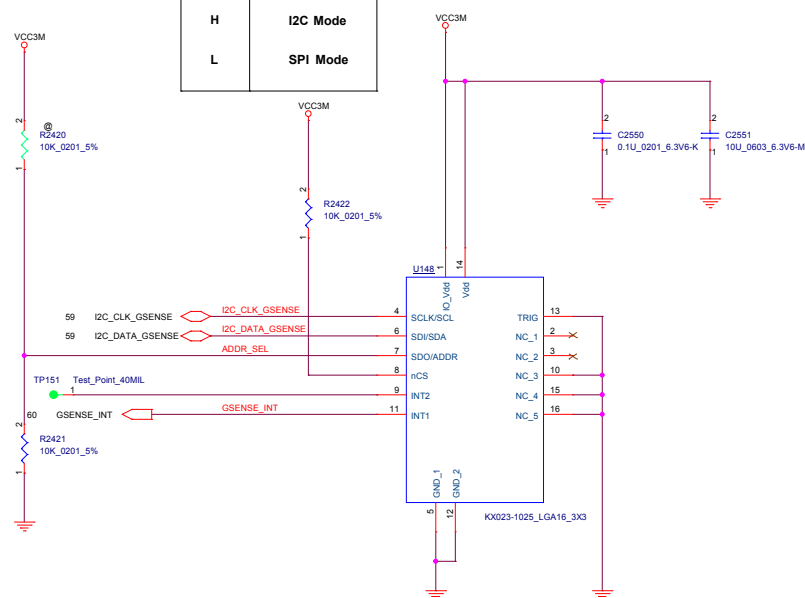
<https://dr-bios.com/>

TABLE

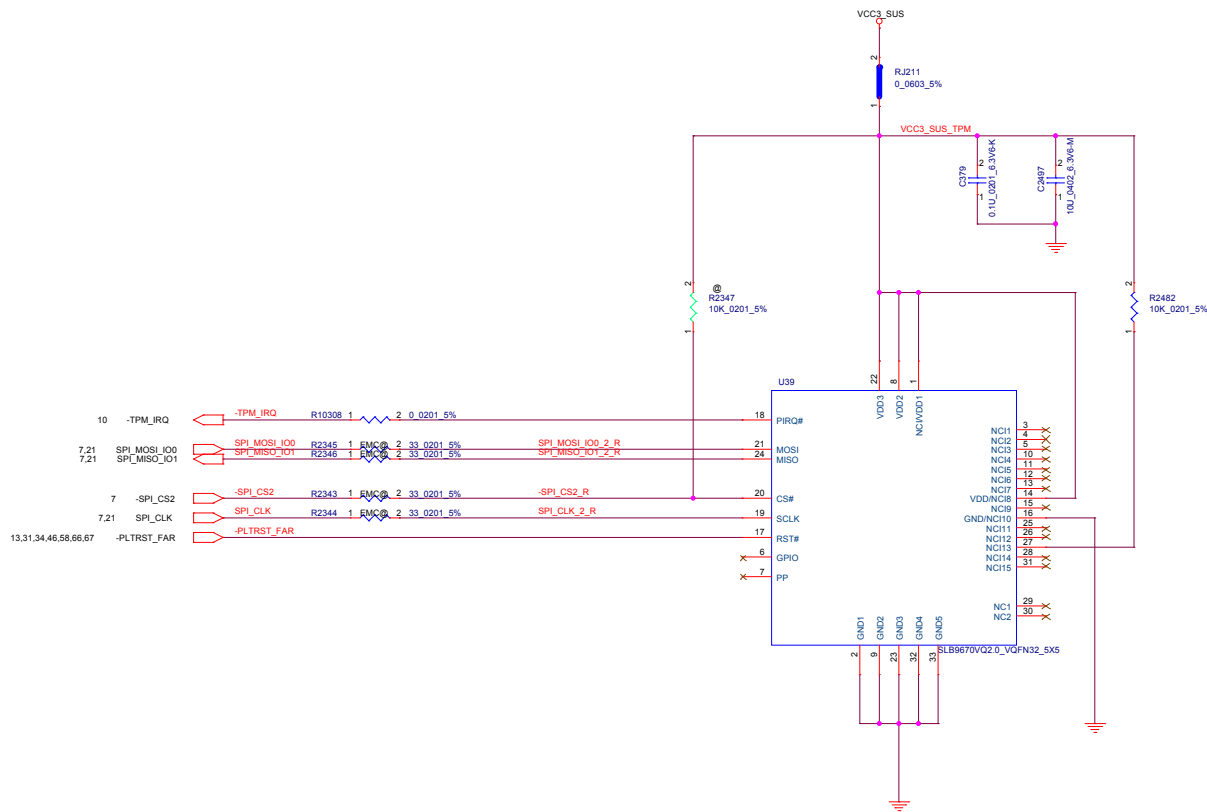
P/N	ADDR_SEL	Address
KX023-1025	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)

TABLE

P/N	Mode Selection
H	I2C Mode
L	SPI Mode







TABLE

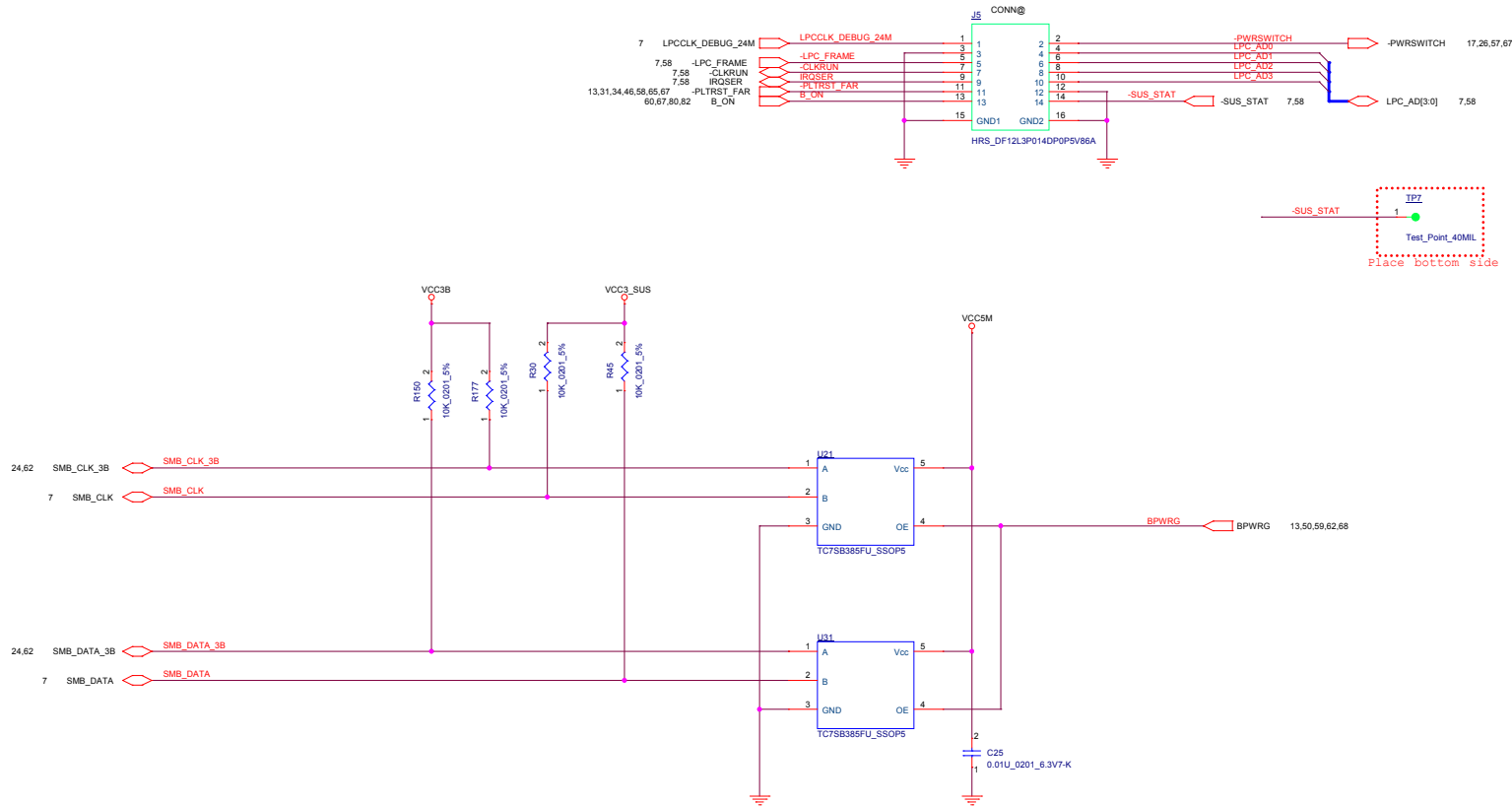
Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ2.0 FW 7.60	ST Micro ST33HTPH2E32AHA6
1	VDD	VDD	NC
2	GND	GND	GND
3	GPIO	NC	NC
4	GPIO	NC	PP
5	NC	NC	NC
6	VNC/GPIO	GPIO	NC
7	GPIO/VDD	PP	GPIO
8	VDD	VDD	NC
9	GND	GND	NC
10	VNC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	VNC/GPIO	NC	NC
14	VDD	NC	NC
15	NC	NC	NC
16	GND	NC	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	CS#	SPI_CS#
21	MOSI	MOSI	MOSI
22	VDD	VDD	VPS
23	GND	GND	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	VNC/GPIO	NC	NC
30	VNC/GPIO	NC	NC
31	VNC	NC	NC
32	GND	GND	NC

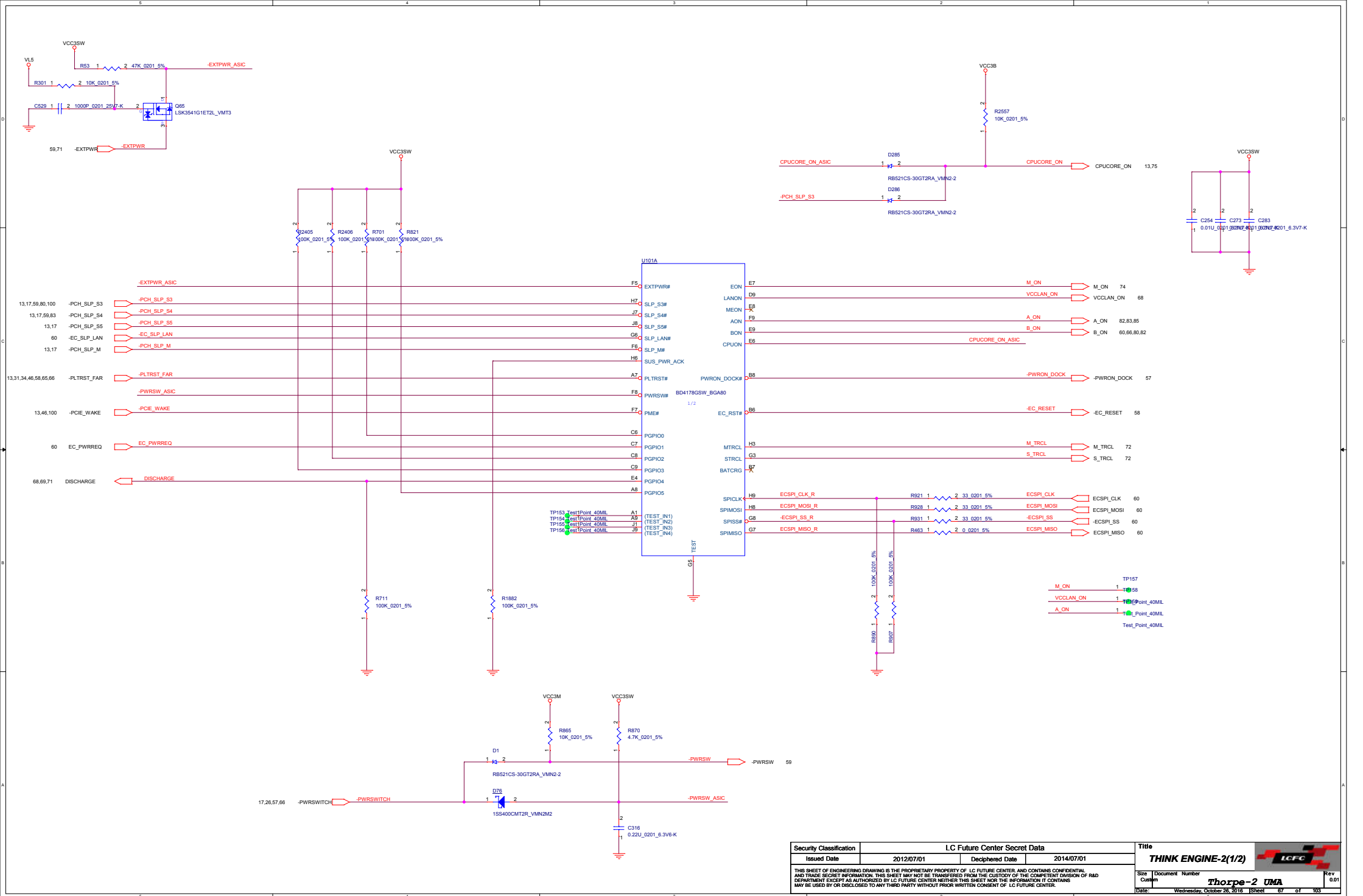
TABLE

REF DES	ENABLE	DISABLE
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R220	ASM	NO_ASM

LOGIC

SDV staff

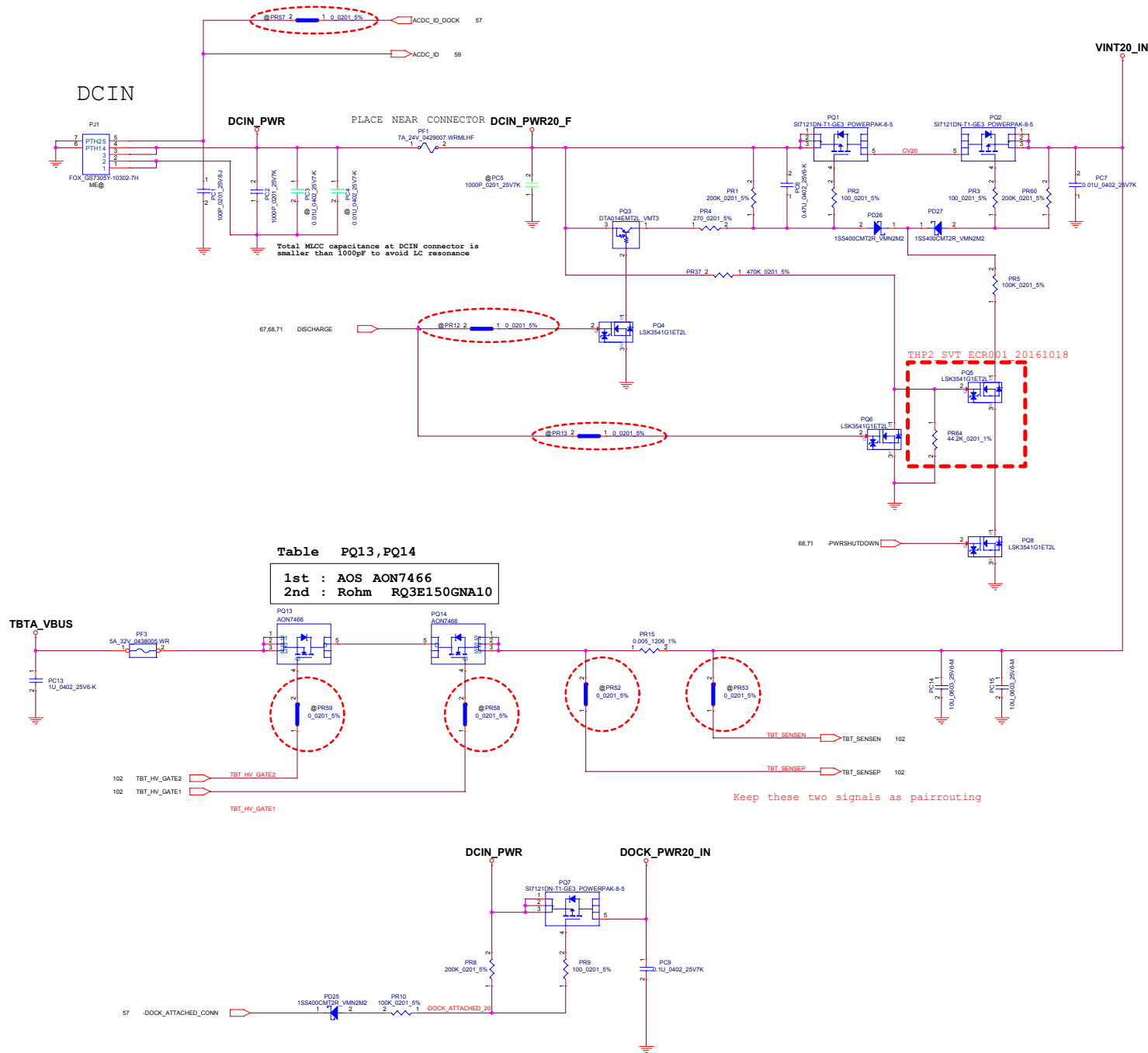




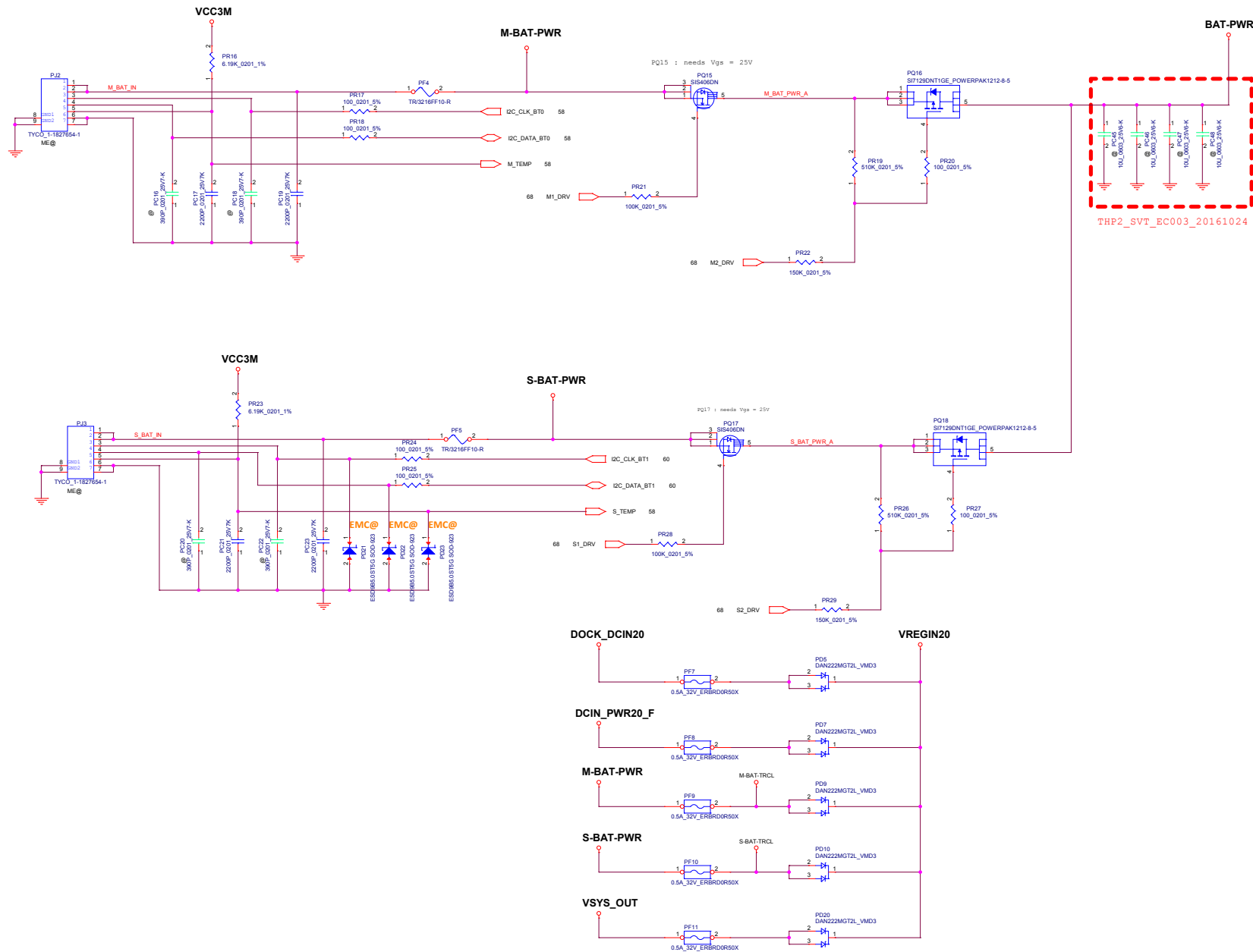
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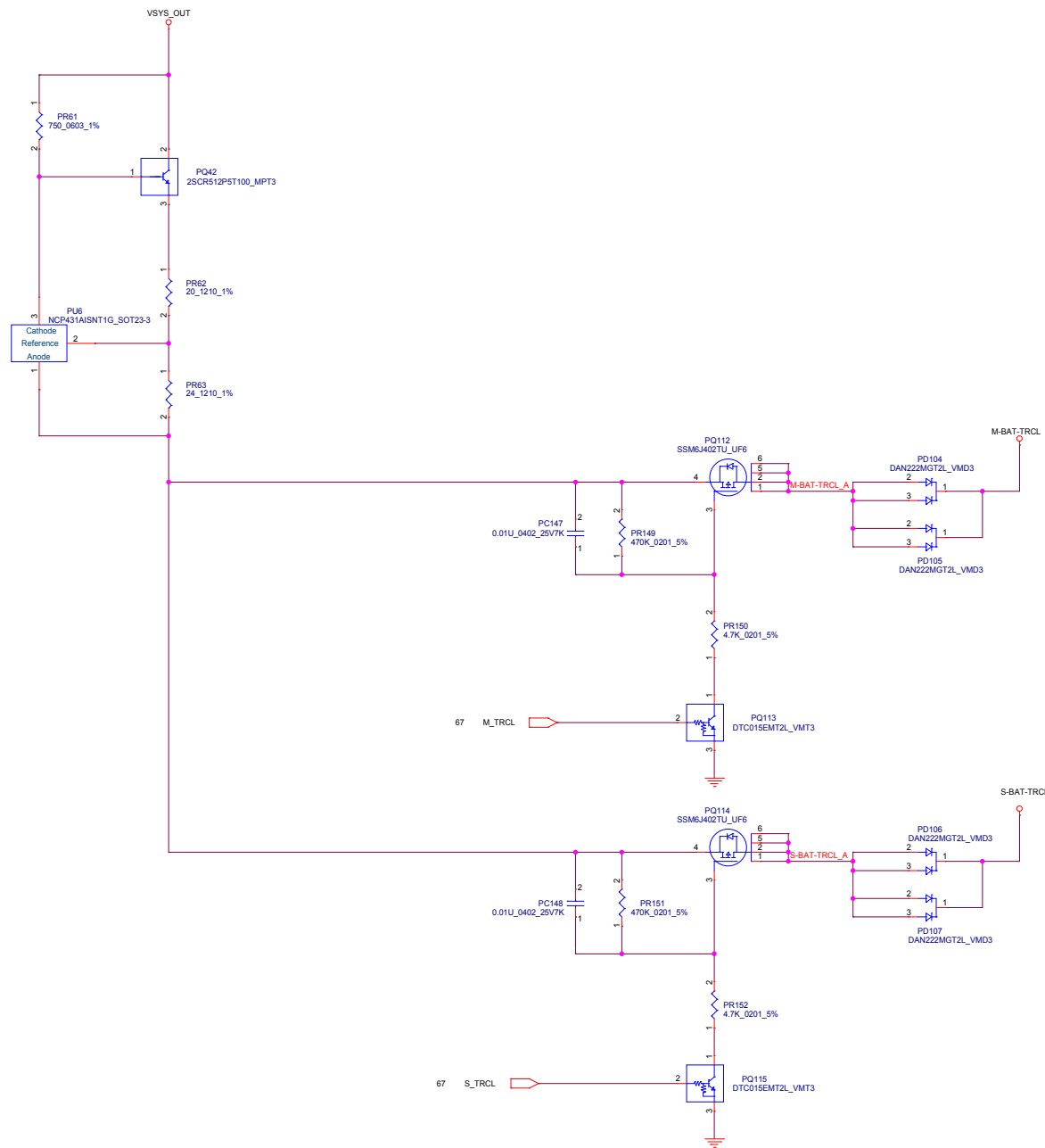
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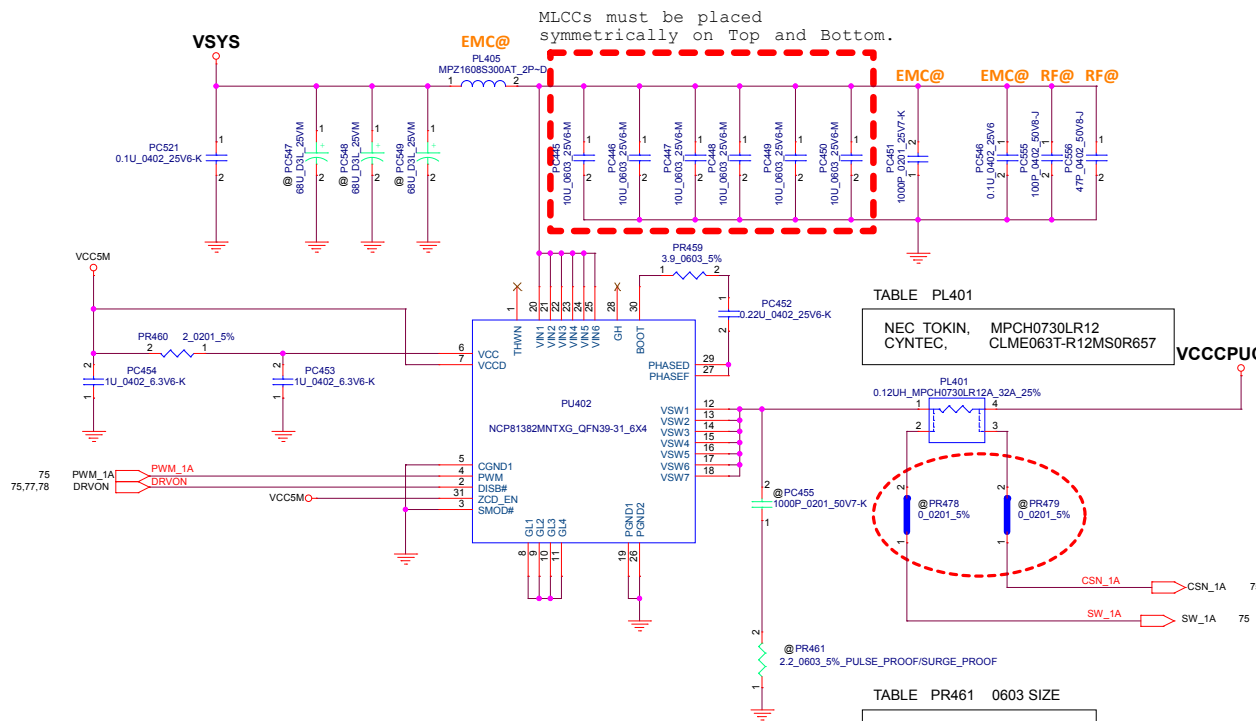
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				Custom	Thorpe-2 UMA	0.01	
Date:				Wednesday, October 26, 2016   Sheet 73 of 102			

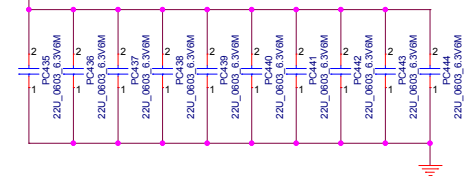






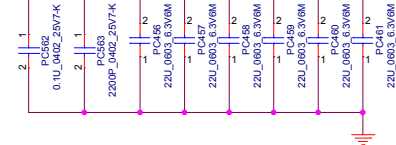
### VCCPUCORE

20pcs 22uF for VCCPUCORE



### VCCPUCORE

EMC@ EMC@



### VCCPUCORE

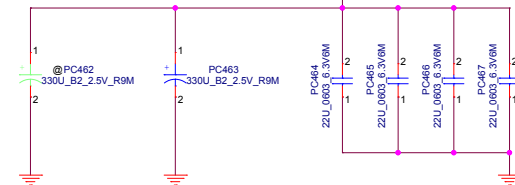


Table for PC462,PC463

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NEC TOKIN	PSGB20E337M9
KEMET	T520B337M2R5ATE009


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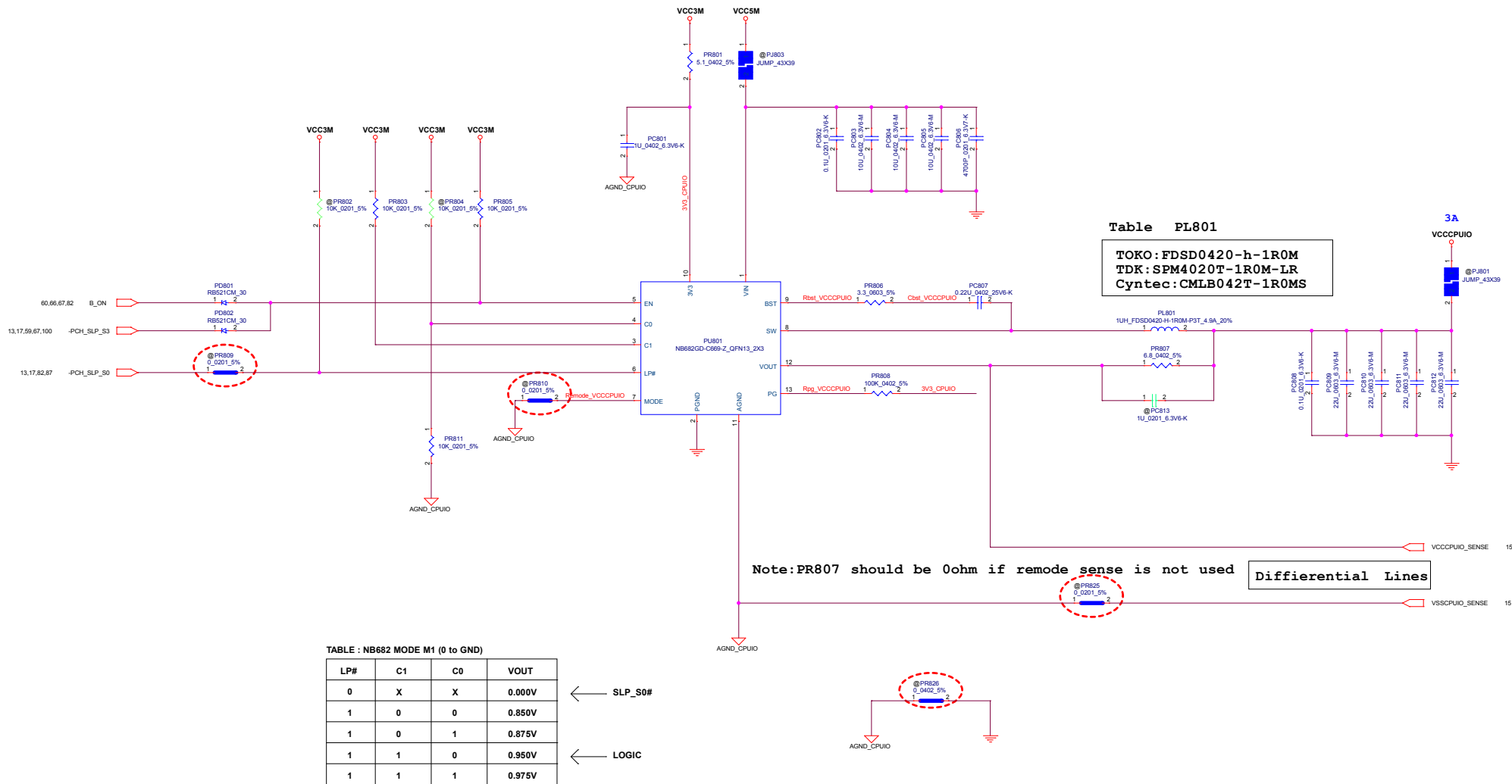




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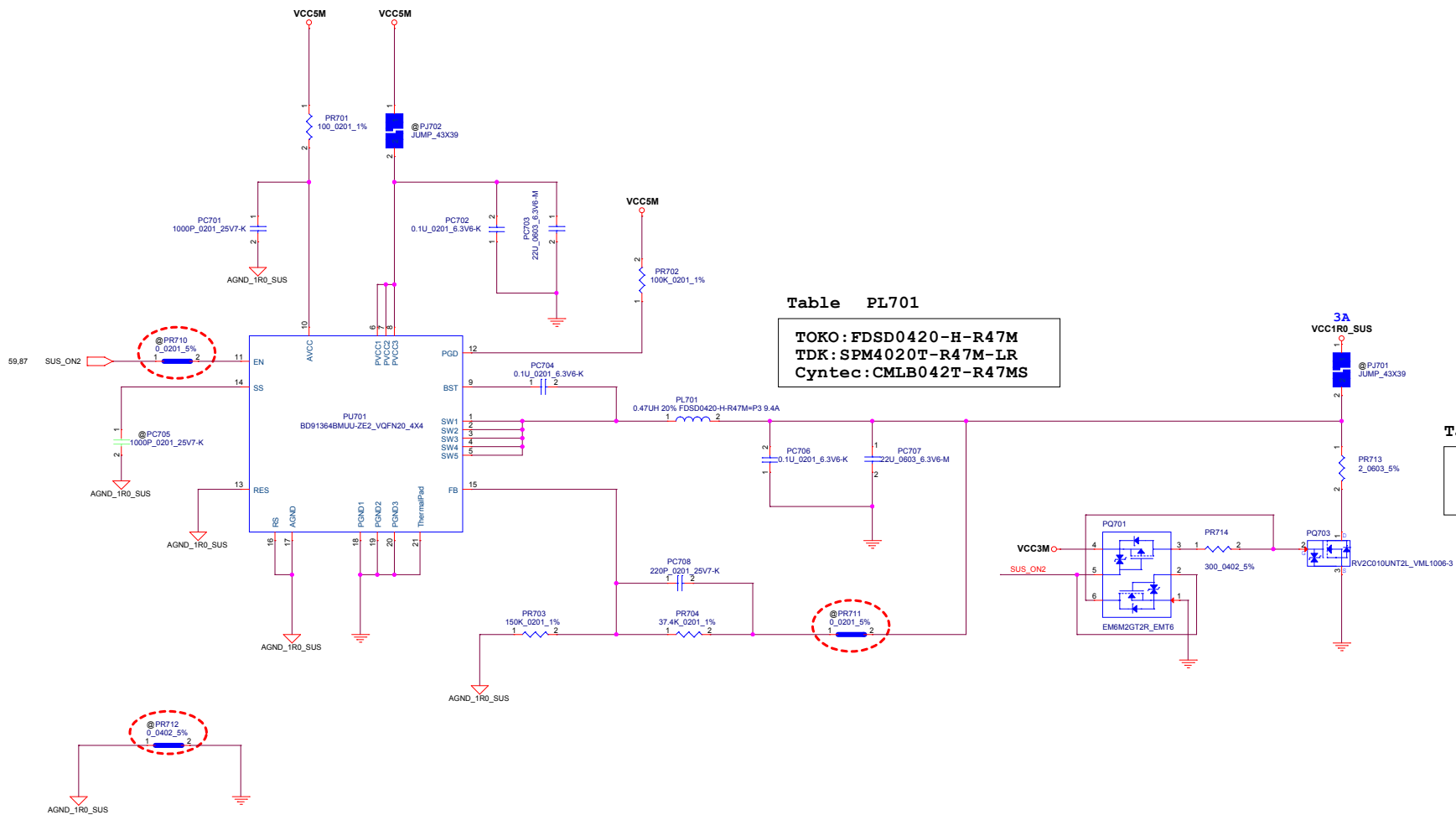


Table PL701

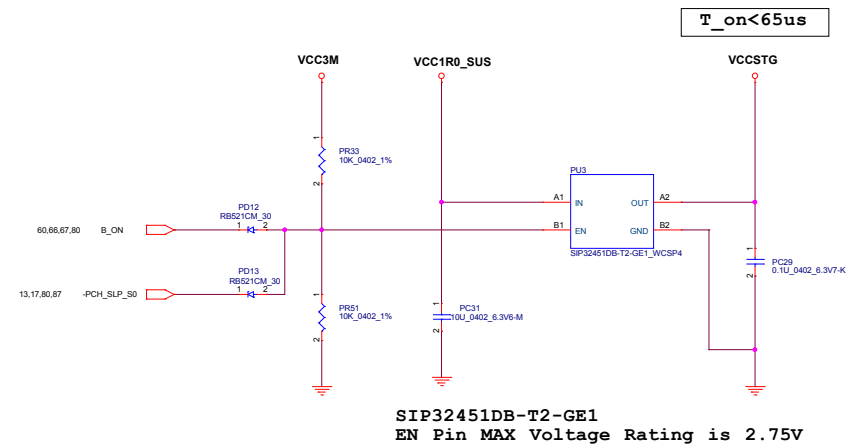
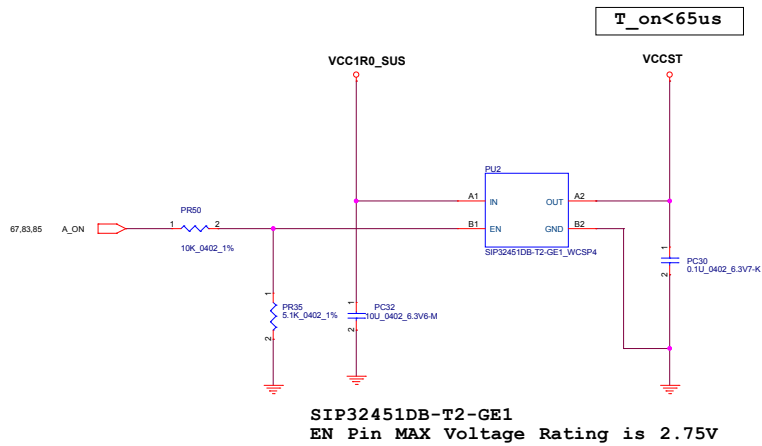
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 TDK:SPM4020T-R47M-LR  
 Cyntec:CMLB042T-R47MS


Table PR713 0603 SIZE

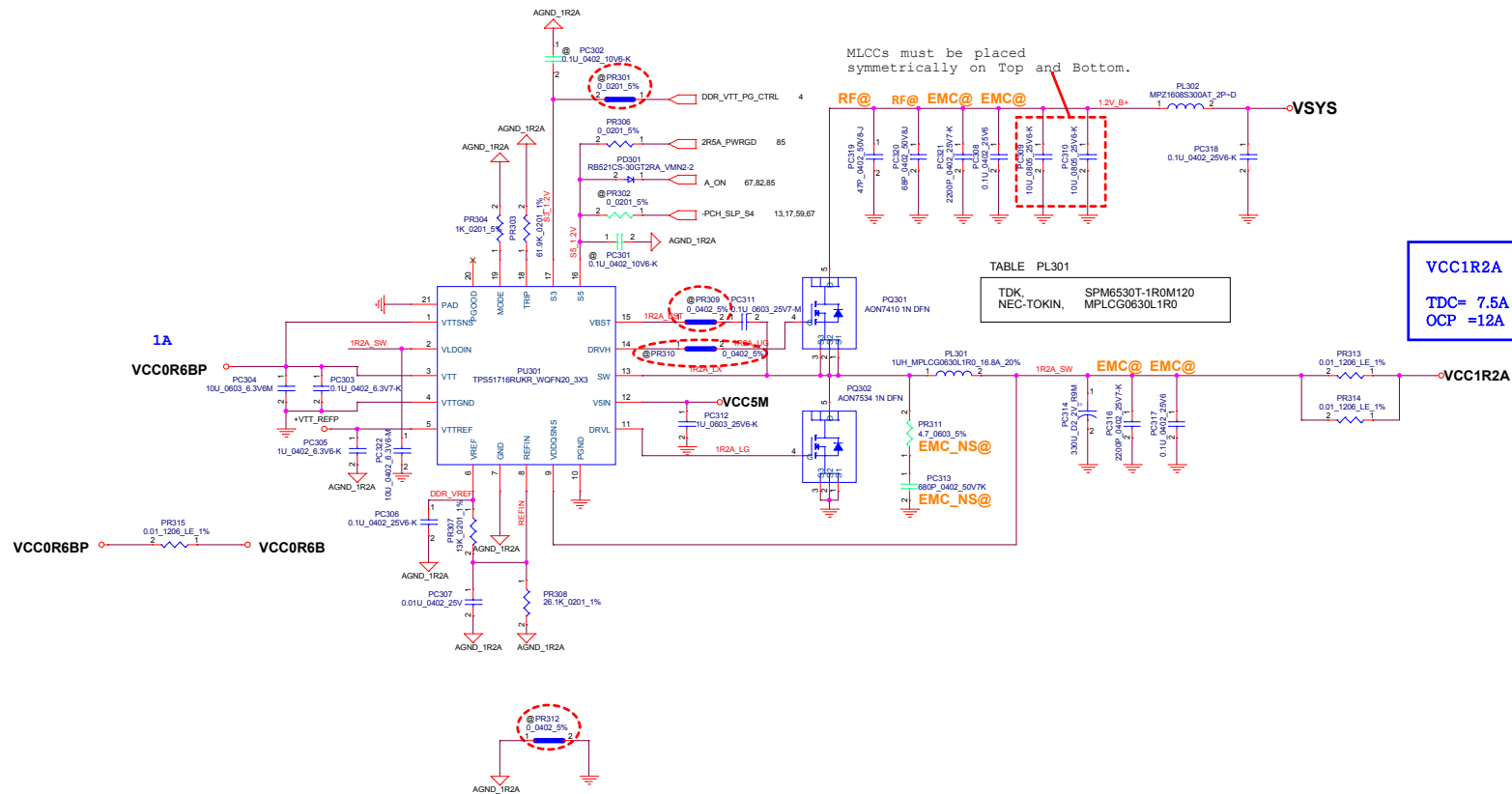
Rohm:ESR03EZPJ2R0  
 Pana:ERJPA3J2R0V  
 YDS:RN73S2CL-2R00-F


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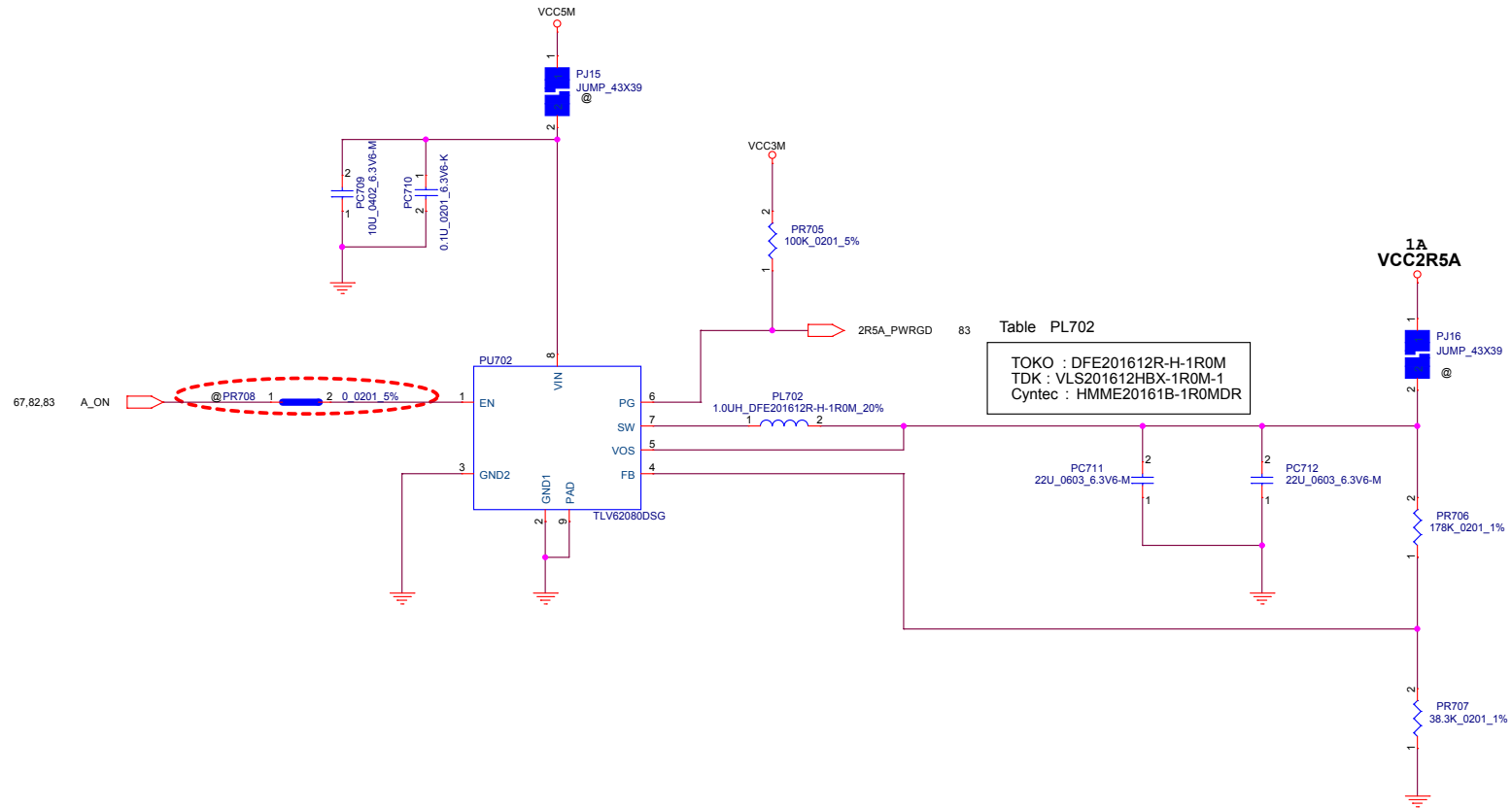

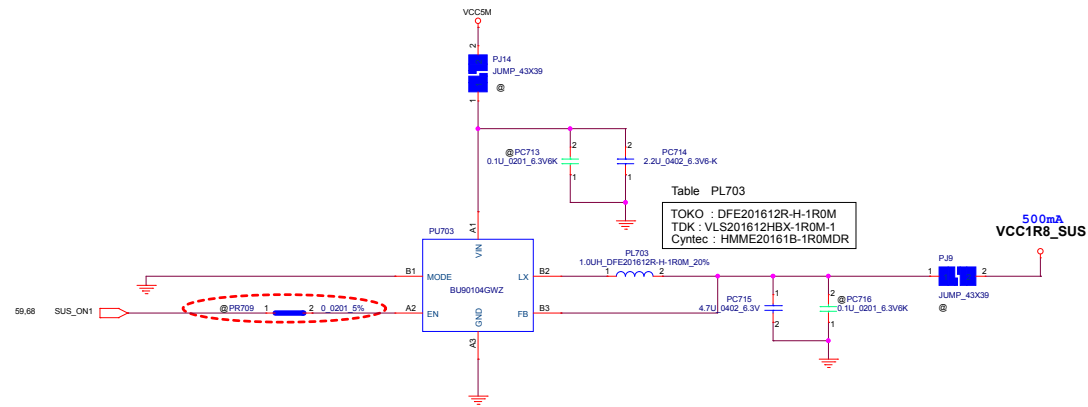



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 TDK : VLS201612HXB-1R0M-1  
 Cyntec : HMME20161B-1R0MDR

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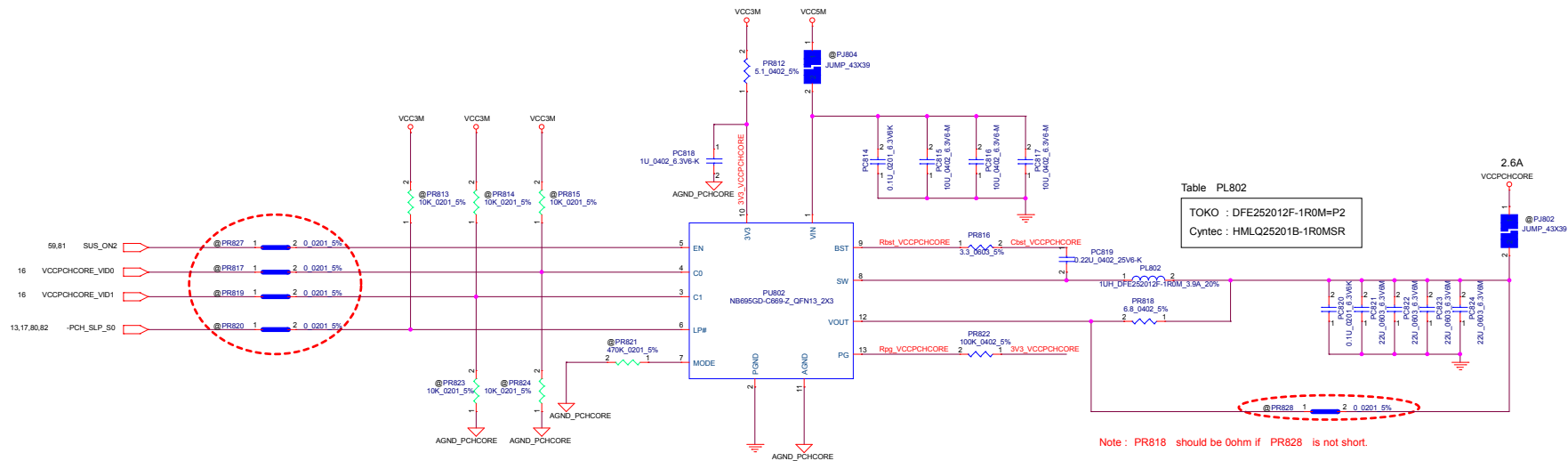


TABLE : NB695 MODE M2 (Float)

LP#	C1	C0	VOUT
0	X	X	0.700V
1	0	0	0.850V
1	0	1	0.900V
1	1	0	0.950V
1	1	1	1.000V


← SLP\_S0#

← DEFAULT



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				Date:	Wednesday, October 26, 2016		Sheet 90 of 111


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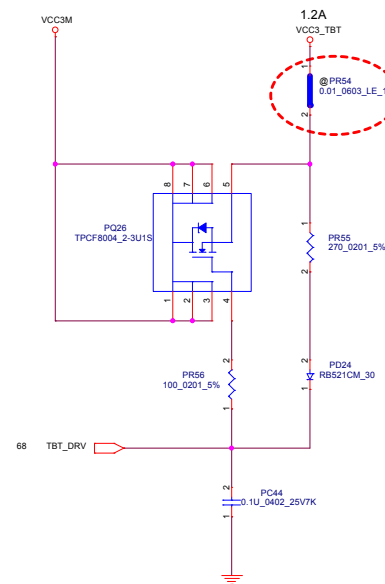
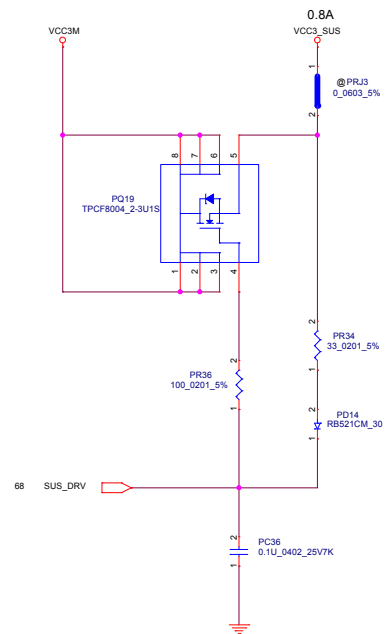
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Date:				Wednesday, October 26, 2016 Sheet 91 of 111			

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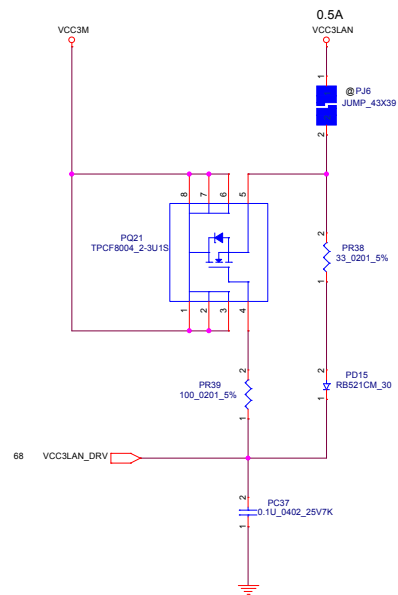
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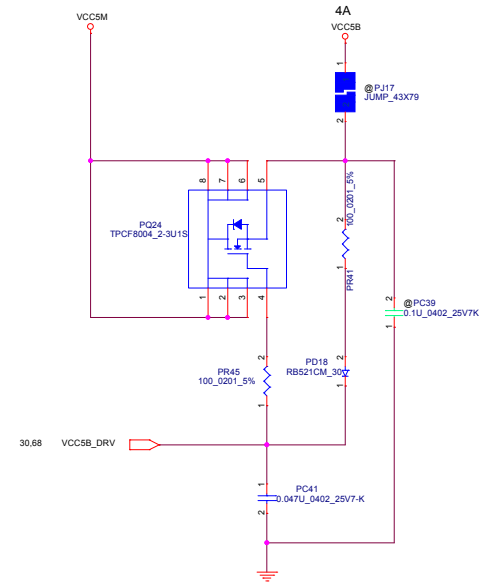
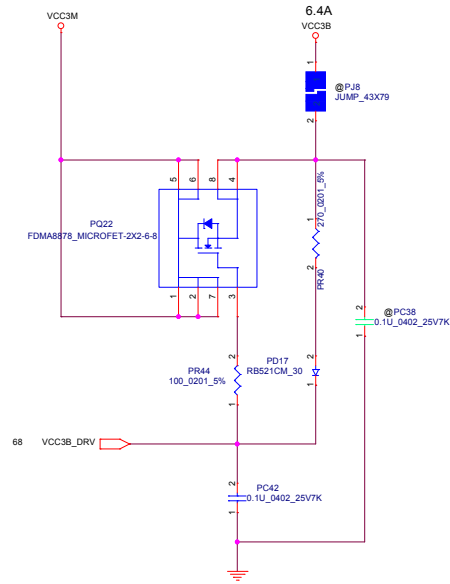



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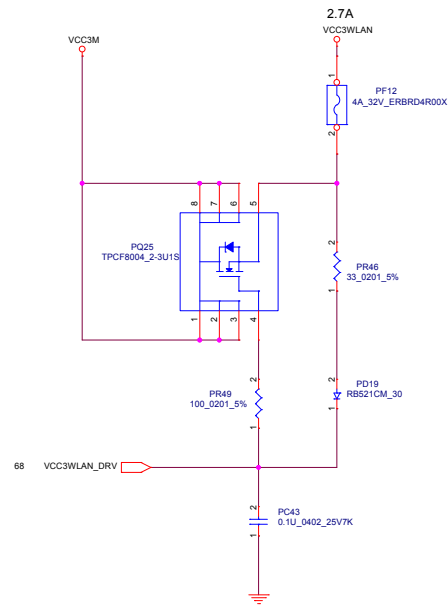
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AOAC	YES	NO
PR1055	NO-ASM	ASM
PQ94	ASM	NO-ASM
PR8924	ASM	NO-ASM
PR91	ASM	NO-ASM
PC8283	ASM	NO-ASM
PD238	ASM	NO-ASM

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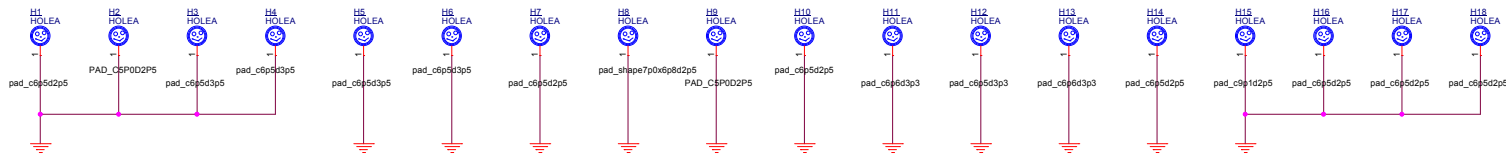
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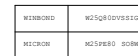
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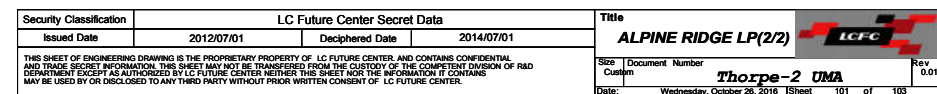
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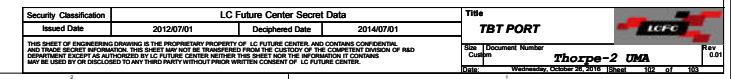


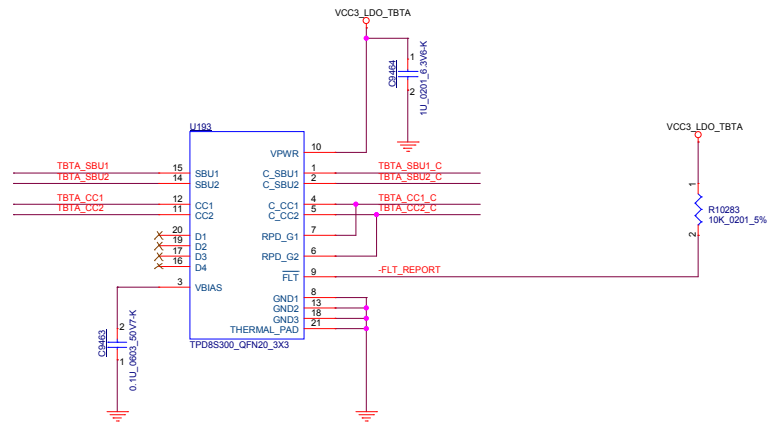
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