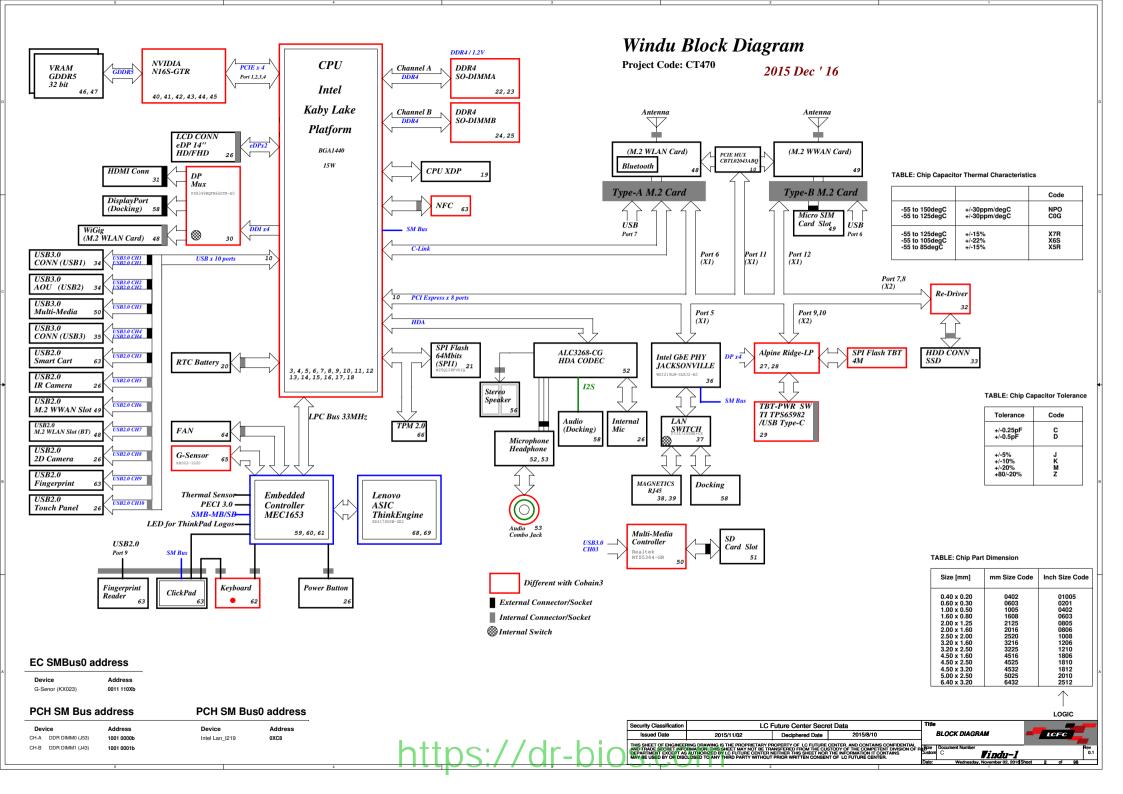
CS16 T14 Logic Schematics

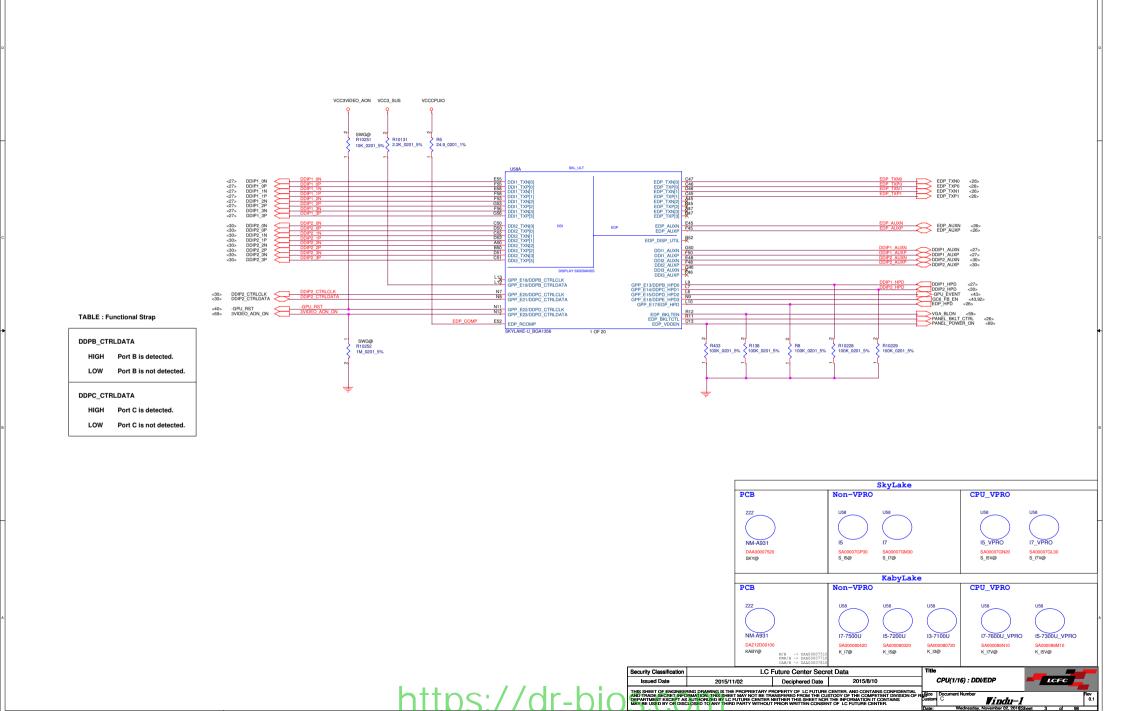
1.TITLE PAGE 2.EC HISTORY 3.CPU(1/16): DDI/EDP 4.CPU(2/16): DDR CHANNEL-A 5.CPU(3/16): DDR CHANNEL-B 6.CPU(4/16): MISC/JTAG 7.CPU(5/16): LPC/SPI/SMBUS/C-LINK 8.CPU(6/16): LPSS/ISH 9.CPU(7/16): AUDIO/SDXC 10.CPU(8/16): PCIE/USB/SATA 11.CPU(9/16): CSI-2/EMMC 12.CPU(10/16): CLOCK SIGNALS 13.CPU(11/16): SYSTEM PM 14.CPU(12/16): CPU POWER (1/2) 15.CPU(13/16): CPU POWER (2/2) 16.CPU(14/16): PCH POWER 17.CPU(15/16): GND 18.CPU(16/16): CFG/RESERVED 19.XDP CONNECTOR 20.RTC BATTERY 21.SPI FLASH 22.DDR4 SO DIMM CHANNEL-A (1/2) 23.DDR4 SO DIMM CHANNEL-A (2/2) 24.DDR4 SO DIMM CHANNEL-B (1/2) 25.DDR4 SO DIMM CHANNEL-B (2/2) 26.LCD/LID/MIC/CAMERA/PWR SW **27.ALPINE RIDGE (1/2) 28.ALPINE RIDGE (2/2)** 29.USB-C/CONN **30.DDI DEMULTIPLEXER** 31.HDMI CONNECTOR 32.STORAGE I/F REDRIVER 33.SATA EXPRESS CONNECTOR 34.USB POWER/CONN(1/2) 35.USB POWER/CONN(2/2)

36.GBE JACKSONVILLE 37.GBE LAN SWITCH 38.GBE MAGNETICS 39.RJ45 CONNECTOR 40.N16S-GTR (1/6): PEG I/F 41.N16S-GTR (2/6): DIGITAL OUT I/F 42.N16S-GTR (3/6): VRAM I/F 43.N16S-GTR (4/6): GPIO 44.N16S-GTR (5/6): POWER 45.N16S-GTR (6/6): GND **46.VRAM CHANNEL-A 47.MEMORY TERMINATION** 48.M.2 SOCKET 1 MODULE I/F 49.M.2 SOCKET 2 MODULE I/F **50.MEDIA CARD CONTROLLER** 51.MEDIA CARD INTERFACE **52.AUDIO ALC3268-CG 53.AUDIO CONNECTOR 54.AUDIO JACK SENSE** 55.AUDIO EXT MIC I/F **56.AUDIO SPEAKER 57.AUDIO BEEP 58.DOCKING CONNECTOR** 59.MEC1653(1/3) 60.MEC1653(2/3) 61.MEC1653(3/3) 62.KEYBOARD/TRACK POINT 63.TOUCH PAD/NFC/FPR/SCR **64.FAN CONNECTOR 65.APS G-SENSOR** 66.DISCRETE TPM 2.0 67.SMBUS SWITCH/LPC DEBUG PORT **68.THINK ENGINE-2(1/2) 69.THINK ENGINE-2(2/2) 70.DC-IN**

71.BLANK **72.BATTERY INPUT** 73.BATTERY CHARGER(BQ24780S) 74.CHARGER SELECTOR 75.DC/DC VCC5M/VCC3M (TPS51285B) 76.DC/DC IMVP8 CONTROLLER(NCP81208) 77.DC/DC VCCCPUCORE(NCP81382) 78.DC/DC VCCGFXCORE I(NCP81382) 79.DC/DC VCCSA(NCP81382) 80.BLANK 81.BLANK 82.DC/DC VCC1R0 SUS(BD91364BMUU) 83.LOAD SW VCCST & VCCSTG 84.DC/DC VCC1R2A(SN1409027) 85.DC/DC VCC0R6B(TPS51206) 86.DC/DC VCC2R5A(TLV62080) 87.DC/DC VCC1R8 SUS(BU90104GWZ) 88.DC/DC VCCPCHCORE(NB682) 89.BLANK 90.BLANK 91.DC/DC VCCGFXCORE D (NCP81172) 92.DC/DC VCC1R35VIDEO (SN1409027) 93.LOAD SW PCH SUS 94.LOAD SW LAN 95.LOAD SW VIDEO 96.LOAD SW B 97.LOAD SW WWAN & WLAN 98.PTH FOR SCREW HOLES

LCFC

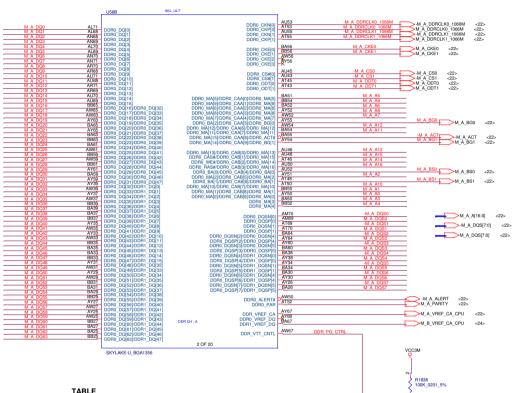




<22> M_A_DQ[63:0]

	Pin	Interleave	Non-Interleave		
Block 0	AL71 AL68 AN68 AN69 AL70 AL69 AN70 AR70 AR68 AU71 AU68 AR71 AR69 AU70 AU69	DDR0_DQ[0] DDR0_DQ[1] DDR0_DQ[2] DDR0_DQ[2] DDR0_DQ[3] DDR0_DQ[4] DDR0_DQ[6] DDR0_DQ[6] DDR0_DQ[7] DDR0_DQ[9] DDR0_DQ[10] DDR0_DQ[11] DDR0_DQ[11] DDR0_DQ[12] DDR0_DQ[13] DDR0_DQ[15]	DDR0_DQ[0] DDR0_DQ[1] DDR0_DQ[2] DDR0_DQ[3] DDR0_DQ[5] DDR0_DQ[6] DDR0_DQ[6] DDR0_DQ[6] DDR0_DQ[8] DDR0_DQ[9] DDR0_DQ[10] DDR0_DQ[10] DDR0_DQ[11] DDR0_DQ[12] DDR0_DQ[13] DDR0_DQ[13] DDR0_DQ[15]		
Block 2	BB65 AW65 AW63 AY63 BA65 AY65 BA63 BB63 BB61 AW61 BB59 AW59 BB61 AY59 AY59	DDR0_DQ[16] DDR0_DQ[17] DDR0_DQ[18] DDR0_DQ[19] DDR0_DQ[21] DDR0_DQ[21] DDR0_DQ[22] DDR0_DQ[23] DDR0_DQ[23] DDR0_DQ[25]	DDR0 DQ[32] DDR0 DQ[33] DDR0 DQ[34] DDR0 DQ[35] DDR0 DQ[35] DDR0 DQ[37] DDR0 DQ[37] DDR0 DQ[37] DDR0 DQ[49] DDR0 DQ[40] DDR0 DQ[41] DDR0 DQ[41] DDR0 DQ[42] DDR0 DQ[43] DDR0 DQ[44] DDR0 DQ[44] DDR0 DQ[44] DDR0 DQ[44] DDR0 DQ[44] DDR0 DQ[44] DDR0 DQ[45] DDR0 DQ[46] DDR0 DQ[47]		
Block 4	AY39 AW39 AY37 AW37 BB39 BA37 BB37 AW35 AW35 AW33 BB35 BB35 BB33 BB33	DDR0 DQ[32] DDR0 DQ[33] DDR0 DQ[34] DDR0 DQ[34] DDR0 DQ[35] DDR0 DQ[37] DDR0 DQ[37] DDR0 DQ[38] DDR0 DQ[38] DDR0 DQ[40] DDR0 DQ[44] DDR0 DQ[44] DDR0 DQ[44] DDR0 DQ[44] DDR0 DQ[44] DDR0 DQ[44] DDR0 DQ[45] DDR0 DQ[46] DDR0 DQ[46] DDR0 DQ[47]	DDR1 DQ[0] DDR1 DQ[1] DDR1 DQ[2] DDR1 DQ[3] DDR1 DQ[3] DDR1 DQ[5] DDR1 DQ[6] DDR1 DQ[7] DDR1 DQ[7] DDR1 DQ[9] DDR1 DQ[10] DDR1 DQ[10] DDR1 DQ[11] DDR1 DQ[12] DDR1 DQ[12] DDR1 DQ[13] DDR1 DQ[14] DDR1 DQ[15]		
Block 6	AY31 AW31 AY29 AW29 BB31 BA31 BA29 BB29 AY27 AW25 AW25 BB27 BA27 BA25 BB25	DDR0 DQ(48) DDR0 DQ(49) DDR0 DQ(50) DDR0 DQ(51) DDR0 DQ(51) DDR0 DQ(52) DDR0 DQ(53) DDR0 DQ(54) DDR0 DQ(56) DDR0 DQ(60) DDR0 DQ(61) DDR0 DQ(62) DDR0 DQ(63)	DR1 DQ[32] DR1 DQ[32] DR1 DQ[34] DR1 DQ[35] DR1 DQ[35] DR1 DQ[37] DR1 DQ[37] DR1 DQ[37] DR1 DQ[37] DR1 DQ[39] DR1 DQ[49] DR1 DQ[41] DR1 DQ[41] DR1 DQ[42] DR1 DQ[43] DR1 DQ[44] DR1 DQ[45] DR1 DQ[45] DR1 DQ[45] DR1 DQ[47]		

LOGIC



	DDIIGE	LEDDING	DUIT
BA51 BB54 BA52 AY52 AW52 AW55 AW54 BA54 BA55 AY54	DDR0 MA[5] DDR0 MA[9] DDR0 MA[6] DDR0 MA[6] DDR0 MA[7] DDR0 BA[2] DDR0 MA[12] DDR0 MA[14] DDR0 MA[15] DDR0 MA[14]	DDR0 CAA[0] DDR0-CAA[1] DDR0 CAA[2] DDR0 CAA[3] DDR0 CAA[3] DDR0 CAA[6] DDR0 CAA[6] DDR0 CAA[6] DDR0 CAA[6] DDR0 CAA[9]	DDR0 MA[5] DDR0 MA[9] DDR0 MA[6] DDR0 MA[6] DDR0 MA[7] DDR0 BG[0] DDR0 MA[11] DDR0 MA[11] DDR0 ACT# DDR0_BG[1]
AU46 AU48 AT46 AU50 AU52 AY51 AT48 AT48 AT50 BB50 AY50	DDR0 MA[13] DDR0 CAS# DDR0 WE# DDR0 RAS# DDR0 BA[0] DDR0 BA[1] DDR0 BA[1] DDR0 MA[10] DDR0 MA[1] DDR0 MA[1]	DDR0_CAB[0] DDR0_CAB[1] DDR0_CAB[2] DDR0_CAB[3] DDR0_CAB[4] DDR0_CAB[5] DDR0_CAB[6] DDR0_CAB[7] DDR0_CAB[7] DDR0_CAB[8] DDR0_CAB[8]	DDR0 MA[13] DDR0 MA[15] DDR0 MA[15] DDR0 MA[16] DDR0 BA[0] DDR0 BA[0] DDR0 BA[1] DDR0 MA[10] DDR0 MA[11] DDR0 MA[1] DDR0 MA[1] DDR0 MA[1]

Not Used

Not Used

I PDDR3

TABLE

BA50

BB52

Pin

DDB3I

DDR0 MAI31

DDR0 MA[4]

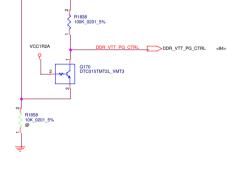
LOGIC

DDR0 MAI31

DDR0 MA[4]

DDD4

	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]



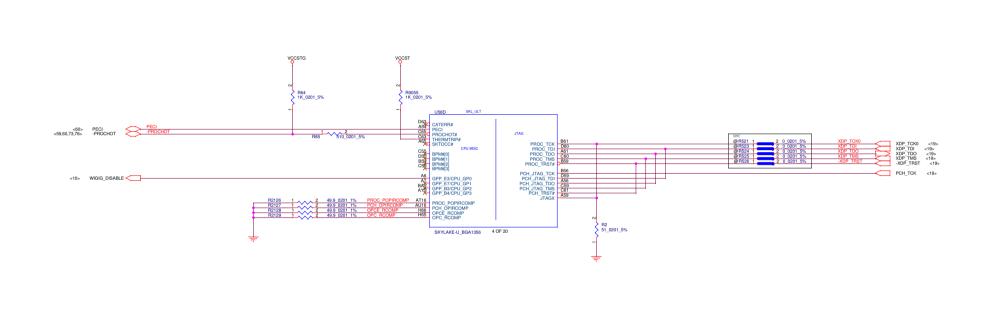
LOGIC

Security Classification	LC Future Center Secret Data			Title
Issued Date	2015/11/02	Deciphered Date	2015/8/10	CPU(
THIS SHEET OF ENGINEER	RING DRAWING IS THE PROPRIETARY PI	ROPERTY OF LC FUTURE ANSFERED FROM THE CU	CENTER. AND CONTAINS CONFIDENTIAL STODY OF THE COMPETENT DIVISION OF R	Size D

J(2/16) : DDR CHANNEL-A LCFC = Vindu-1
Wednesday, November 02, 2016 Sheet

THIS SMEET OF ENCINEERING DRAWING IS THE PROPRIETARY PROPERTY OF I.C. FUTURE CENTER, AND CUNITARIS OF MAD TRADE SECRET IN COMMITTION. THIS SMEET MAY NOT HE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT MAY RE USED BY OF DISCLOSED TO ANY MIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF I.C. FUTURE CENTER.

TABLE Pin Interleave Non-Interleave <24> M_B_DQ[63:0] Λ **E** 65 DDR1 DQI0 DDR0 DQ[16] DDR0_DQ[17] ΔF64 DDR1 DQ[1 AK65 DDR1_DQ[2 DDR1_DQ[3 SKL ULT AK64 DDR0 DQ[19 U58C AF66 DDR1 DQ[4 DDR0 DQ[20] AF67 DDR1 DQI5 DDR0 DQI21 -M_B_DDRCLK0_1066M -M_B_DDRCLK1_1066M -M_B_DDRCLK0_1066M -M_B_DDRCLK1_1066M AN46 AP45 AP46 AK67 DDR1 DQ[6 DDR0 DQ[22 AK66 AF70 DDR1_DQ[7 DDR0 DQ[23 TABLE DDR1 DQ[8 DDR0 DQI24 DRH DG | DRH DDR1_CKE[0] DDR1_CKE[1] DDR1_CKE[2] DDR1_CKE[3] Block 1 AF68 DDR1_DQ[9]
DDR1_DQ[10]
DDR1_DQ[11] DDR0_DQ[25] Pin DDB3I LPDDR3 DDR4 AH71 AH68 DDR0 DQ[27 AY48 DDR1 MA[5] DDR1 CAA[0] DDR1 MA[5] <24> <24> <24> <24> AF71 DDR1 DQ[12] DDR0 DQ[28 DDR1_MA[9] DDR1_MA[6] DDR1_MA[8] AP50 DDR1_MA[9 DDR1 CAA AF69 DDR1_DQ[13] DDR1_DQ[14] DDR0 DQ[29] DDR1_MA[6] DDR1_MA[8] DDR1_MA[7] **BA48** DDR1_CAA[AH70 AH69 DDR0_DQ[30 DDR1 MA(5)DDR1 CAN(9)DDR1 MA(5) DDR1 MA(9)DDR1 CAN(1)DDR1 MA(9) DDR1 MA(9)DDR1 CAN(3)DDR1 MA(9) DDR1 MA(9)DDR1 CAN(3)DDR1 MA(9) DDR1 MA(2)DDR1 CAN(3)DDR1 MA(10) DDR1 MA(12)DDR1 CAN(9)DDR1 MA(11) DDR1 MA(12)DDR1 CAN(9)DDR1 MA(11) DDR1 MA(13)DDR1 CAN(9)DDR1 MA(11) DDR1 MA(14)DDR1 CAN(9)DDR1 MA(11) **BB48** DDR1_CAA[3 DDR1_DQ[15] DDR0_DQ[31] AP48 DDR1 MAI7 AP52 DDR1 BAI21 DDR1 CAAL DDR1 BG[0] AN50 DDR1 MA[12] DDR1 CAA[6 DDR1 MA[12] M_B_BG0 <24: AN48 DDR1 MA[11] DDR1 CAA[7 DDR1 MA[11] AT66 DDR1 DQ[16] DDR0 DQ[48] AN53 DDR1_MA[15 DDR1_CAA[8 DDR1_ACT# AU66 DDR1 DQ[17] DDR0 DQ[49] -M_B_ACT M_B_BG1 AN52 DDR1 MA[14] DDR1_CAA[9] DDR1_BG[1] AP65 DDR1 DQ[18 DDR0 DQ[50] DORI MA(19)DORI CARIJIODRI MA(19)
DDRI MA(19)DORI CARIJIODRI MA(19)
DDRI MENDORI CARIJIODRI MA(19)
DDRI MENDORI CARIJIODRI MA(14)
DDRI RASWDDRI CARIJIODRI MA(14)
DDRI MA(19)DDRI CARIJIODRI MA(16)
DDRI MA(1)DDRI CARIJIODRI MA(16)
DDRI MA(1)DDRI CARIJIODRI MA(10)
DDRI MA(10)DRI CARIJIODRI MA(10)
DDRI MA(10)DRI CARIJIODRI MA(10)
DDRI MA(10)DRI MA(10)DRI MA(10)
DDRI MA(10)DRI MA(10)DRI MA(10)DRI MA(10)
DDRI MA(10)DRI AN65 DDR1_DQ[19 DDR0_DQ[51 AN66 AP66 AT65 DDR1_DQ[20] DDR1_DQ[21] DDR1_DQ[22] DDR0_DQ[52] DDR0_DQ[53] DDR0_DQ[54] **BA43** DDR1 MA[13] DDR1 CAB[0] DDR1 MA[13] M B BS0 <24: DDR1_MA[13] DDR1_MA[15] DDR1_MA[14] DDR1_MA[16] DDR1_BA[0] DDR1_MA[2] AY43 DDR1_CAS# DDR1_CAB[1 M_B_BS1 DDR1 DQ[23] AU65 DDR0 DQ[55] AY44 DDR1_WE# DDR1_CAB[2 DDR1 DQ[24 DDR0 DQ[56] AT61 DDR1_CAB[3] DDR1_CAB[4] DDR1_RAS# Block 3 M_B_A[16:0] <24> ΔW44 AU61 DDR1_DQ[25] DDR0_DQ[57] DDR1_BA[0] **RR44** -M_B_DQS[7:0] <24> AP60 DDR1_DQ[26 DDR0_DQ[58] AY47 DDR1 CABIS DDRI DOSNOJDDRO DOSNOJ-DDRI DOSNOJDDRO DOSNOJ-DDRI DOSNOJDDRO DOSPOJ-DDRI DOSNOJDDRO DOSNOJ-DDRI DOSNOJDDRO DOSNOJ-DDRI DOSNOJDDRO DOSNOJ-DDRI DOSNOJDDRO DOSNOJ-DDRI DOSNOJDDRO DOSNOJ-DDRI DOSNOJDDRO DOSNOJ-DDRI DOSNOJDDRI DOSNOJ-DDRI DOSNOJDDRI DOSNOJ-DDRI DOSNOJDRO DOSNOJ-DDRI DOSNOJDRO DOSNOJ-DDRI DOSNOJDRO DOSNOJ-DDRI DOSNOJ-DDRI DOSNOJ-DDRI DOSNOJ-DDRI DOSNOJ-DDRI DOSNOJ-DDRI DOSNOJ-DDRI DOSNOJ-DDRI DOSNOJ-AN60 DDR1_DQ[27 DDR0 DQ[59 M_B_DQS[7:0] <24> BA44 DDR1 BA[1] DDR1 CABI6 DDR1 BA[1] AN61 DDR1_DQ[28] DDR0_DQ[60] AW46 DDR1 MA[10] DDR1 CAB DDR1 MA[10] DDR1_MA[1] DDR1_MA[1] DDR1_CAB[8 AT60 DDR1 DQ[30 DDR1_MA[1] DDR1_MA[3] DDR1_MA[4] DDR0 DQI62 **BA46** DDR1 MAIO DDR1 CABI91 AU60 DDR1 DQ[31] DDR0 DQ[63] DDR1_MA[3] DDR1_MA[4] BB46 BA47 Not Used Not Used R1726 470_0201_5% DDR1_DQ[16] AU40 DDR1_DQ[32] DDR1_DQ[33] DDR1_DQ[34] DDR1_DQ[35] DDR1_DQ[36] AT40 AT37 DDR1_DQ[17] DDR1_ALERT# OAP43 DDR1_PAR AU37 DDR1_DQ[19] AR40 LOGIC AP40 DDR1 DQ[37 DDR1 DQ[21 AP37 DDR1 DQ[38 DDR1 DQ[22 DDR1_DQ[39] DDR1_DQ[40] DDR1_DQ[41] DDR1_DQ[42] AR37 DDR1_DQ[23 AT33 AU33 DDR1_DQ[24] Block 5 DDR1_DQ[25] 3 OF 20 SKYLAKE-U BGA1356 AU30 AT30 DDR1 DQ[43] DDR1 DQ[27 TABLE AR33 DDR1 DQ[44] DDR1 DQ[28] AP33 DDR1 DQ[45] DDR1 DQ[29 Pin Interleave Non-Interleave DDR1_DQ[46] DDR1_DQ[47] AR30 DDR1_DQ[30 AH66 DDR1 DOSNIO DDR0 DQSNI2 **AP30** DDR1 DQ[31] DDR0 DQSP[2 **AH65** DDR1 DQSPI Block 1 AG69 DDR1 DQSNI1 DDR0 DQSNI3 DDR1 DQSP[1 DDR0 DQSP[3] AG70 AU27 DDR1 DQ[48] DDR1 DQ[48] AT27 DDR1 DQ[49] DDR1 DQ[49] AR66 DDR1 DQSN[2] DDR0 DQSN[6] AT25 DDR1_DQ[50 DDR1_DQ[50 AR65 DDR1 DQSP[2 DDR0 DQSP[6] AU25 DDR1_DQ[51] DDR1_DQ[51] Block 3 AR61 DDR1_DQSN[3 DDR0_DQSN[7 DDR1_DQ[52] DDR1_DQ[53] AP27 DDR1_DQ[52] AR60 DDR1 DQSP[3] DDR0 DQSP[7] AN27 AN25 DDR1_DQ[53] DDR1_DQ[54] DDR1_DQ[54] AP25 DDR1_DQSN[4] DDR1_DQSN[2] AT22 DDR1 DQ[56 DDR1 DQ[56] DDR1_DQSP[4] AR38 DDR1_DQSP[2] Block 7 AU22 DDR1_DQ[57 DDR1_DQ[57 Block 5 AT32 DDR1_DQSN[3 DDR1_DQ[58] DDR1_DQ[59] AU21 DDR1 DQ[58 AR32 DDR1 DQSP[5] DDR1 DQSP[3] AT21 DDR1_DQ[59 DDR1_DQ[60] DDR1_DQ[61] DDR1_DQ[62] AN22 DDR1_DQ[60 AR25 AP22 AP21 DDR1 DQSN[6] DDR1 DOSNI6 DDR1_DQ[61] AR27 DDR1 DQSP[6 DDR1 DQSP[6] AN21 DDR1 DQ[63] DDR1 DQ[63] Block 7 AR22 DDR1_DQSN[7] DDR1_DQSN[7] DDR1 DQSP[7] DDR1 DQSP[7] LOGIC LOGIC Security Classification LC Future Center Secret Data CPU(3/16) : DDR CHANNEL-B Issued Date 2015/11/02 Deciphered Date 2015/8/10 LCFC THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIET ANY PROPERTY OF L. D. DITURE CENTER. AND CONTAINS COMPIDENTIAL AND FRAME STORE AND CONTAINS COMPIDENTIAL AND FRAME STORE AND GRANT HIS SHEET ANY OTHER THAN SHEET HOW THE THAN SHEET HOW THE SHOW OF THE CONTAINS CONTRIBUTION OF THE CONTAINS OF THE SHOW OF THE CONTAINS OF THE SHOW O Windu-1



Security Classification LC Future Center Secret Data CPU(4/16): MISC/JTAG 2015/11/02 Deciphered Date 2015/8/10 THIS SHEET OF ENQINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERDE FROM THE CUSTODY OF THE COMPETENT DIVISION OF A

LCFC =

Vednesday, November 02, 2016 Sheet

TABLE : Functional Strap

SPI0_MOSI (Boot Halt)		
HIGH Disabled (Default)		
LOW	Enabled	

TABLE : Functional Strap

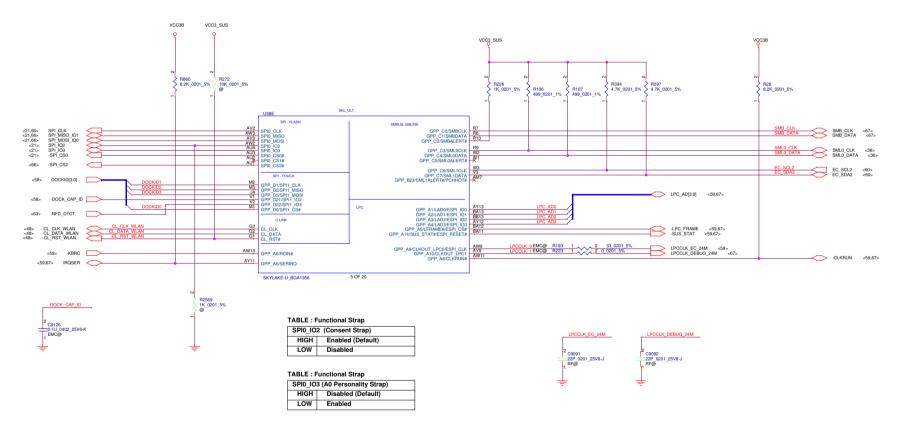
SPI0_MISO (JTAG ODT Disable)				
HIGH	Enabled (Default)			
LOW	Disabled			

TABLE : Functional Strap

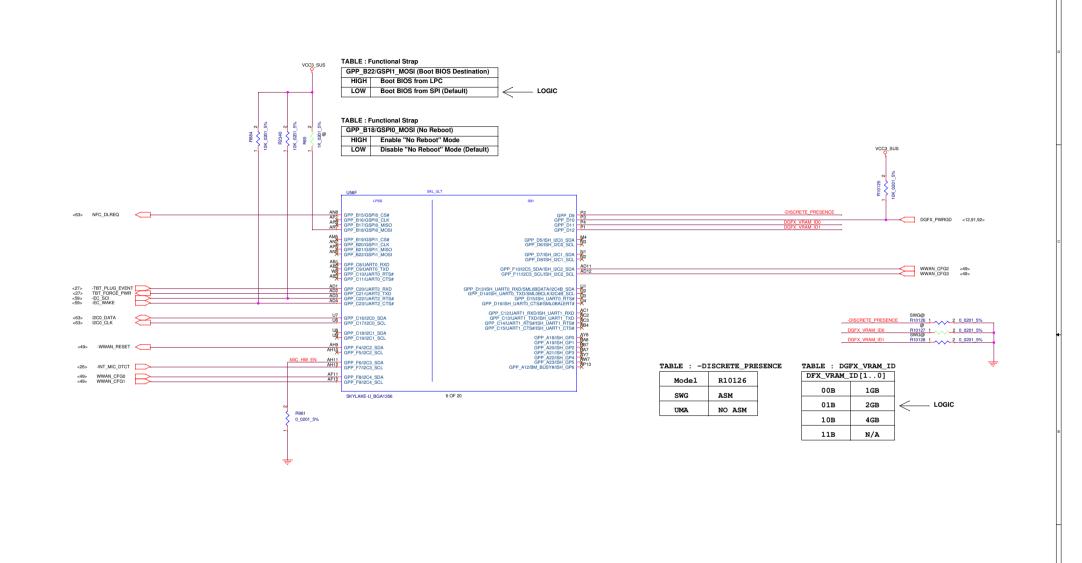
	GPP_C5	/SML0ALERT # (LPC or eSPI)	
Ī	HIGH	eSPI is selected	
	LOW	LPC is selected (Default)	

TABLE : Functional Strap

GPP_C2	/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality	← LOGIC
LOW	Disable ME Crypto TLS (Default)	•



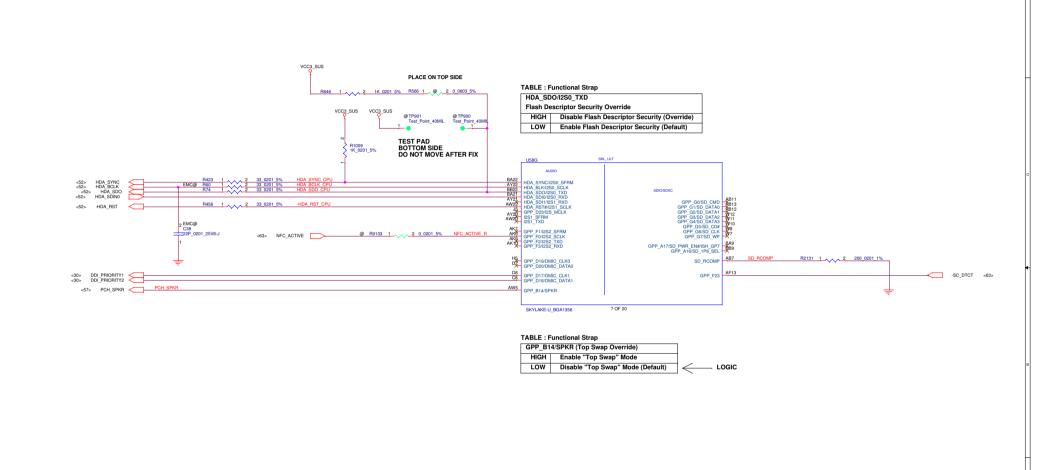
https://dr-bio

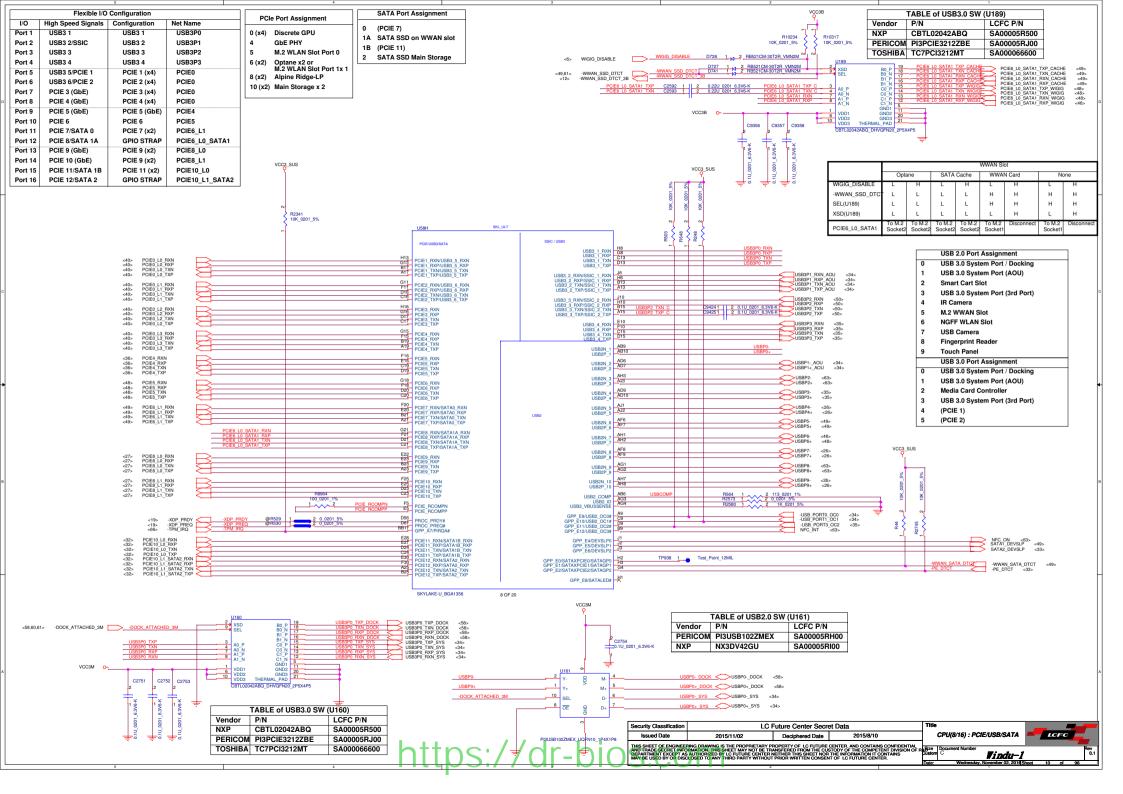


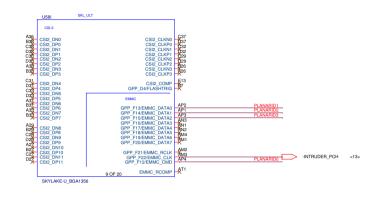
716): LPSS/ISH

It Number

| Pindu-1 | Pindu-1

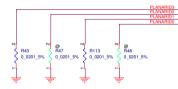






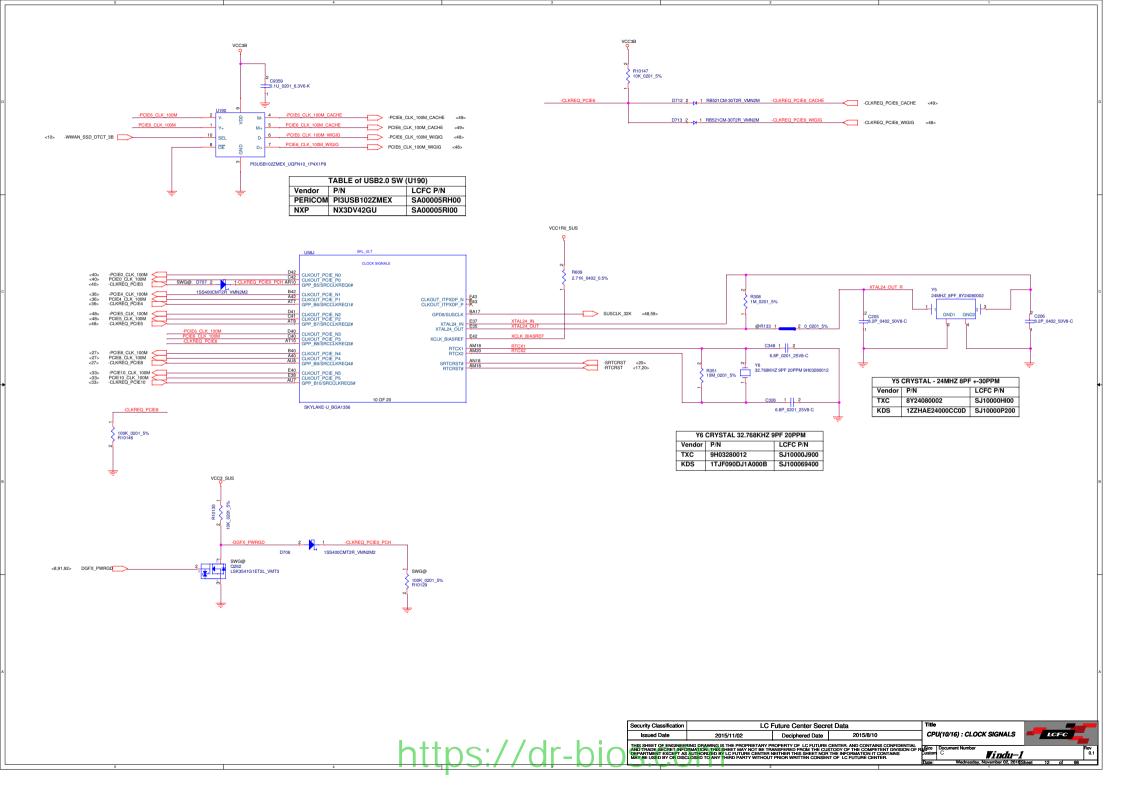
TABLE

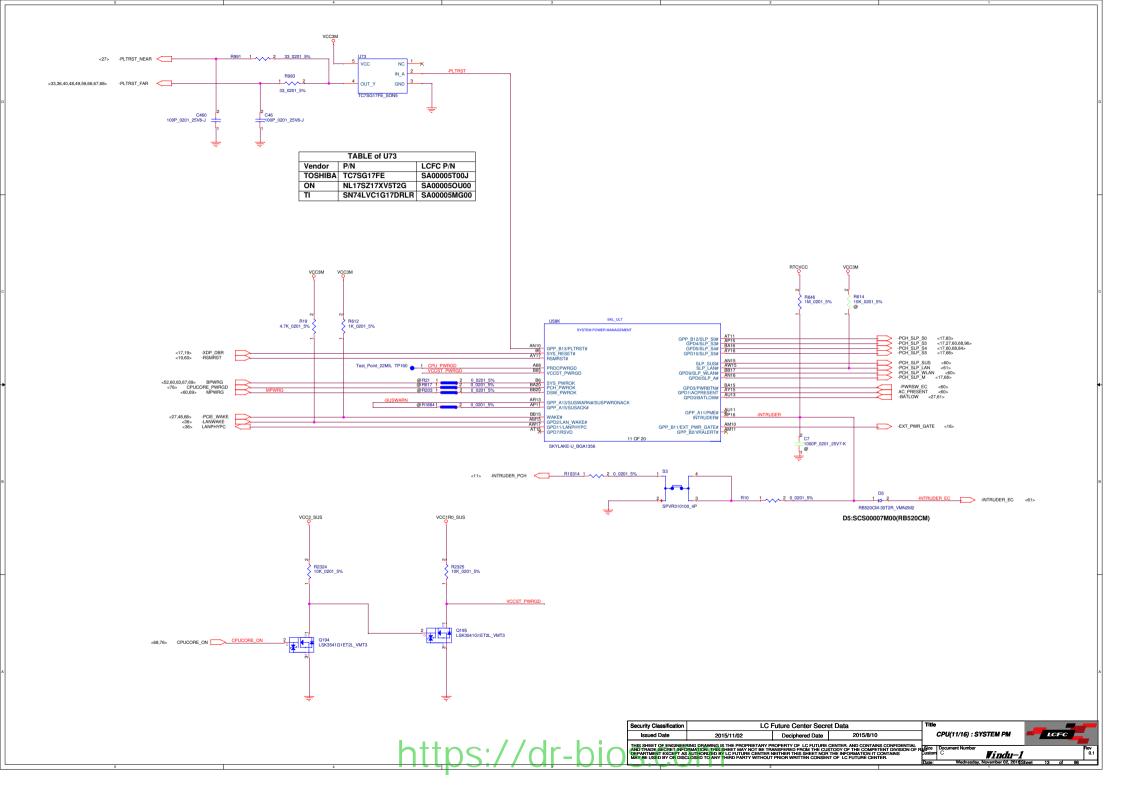
LEVEL	PLANAR ID			
	3	2	1	0
	R43	R47	R113	R48
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM



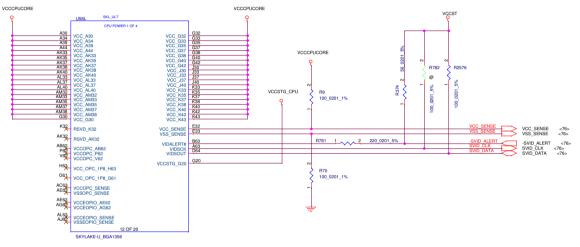
TABLE

LEVEL	PLANARID[30]
SDV	0000B
FVT	0001B
FVT-2	0010B
SIT	0011B
SIT-R	0100B
SVT	0101B





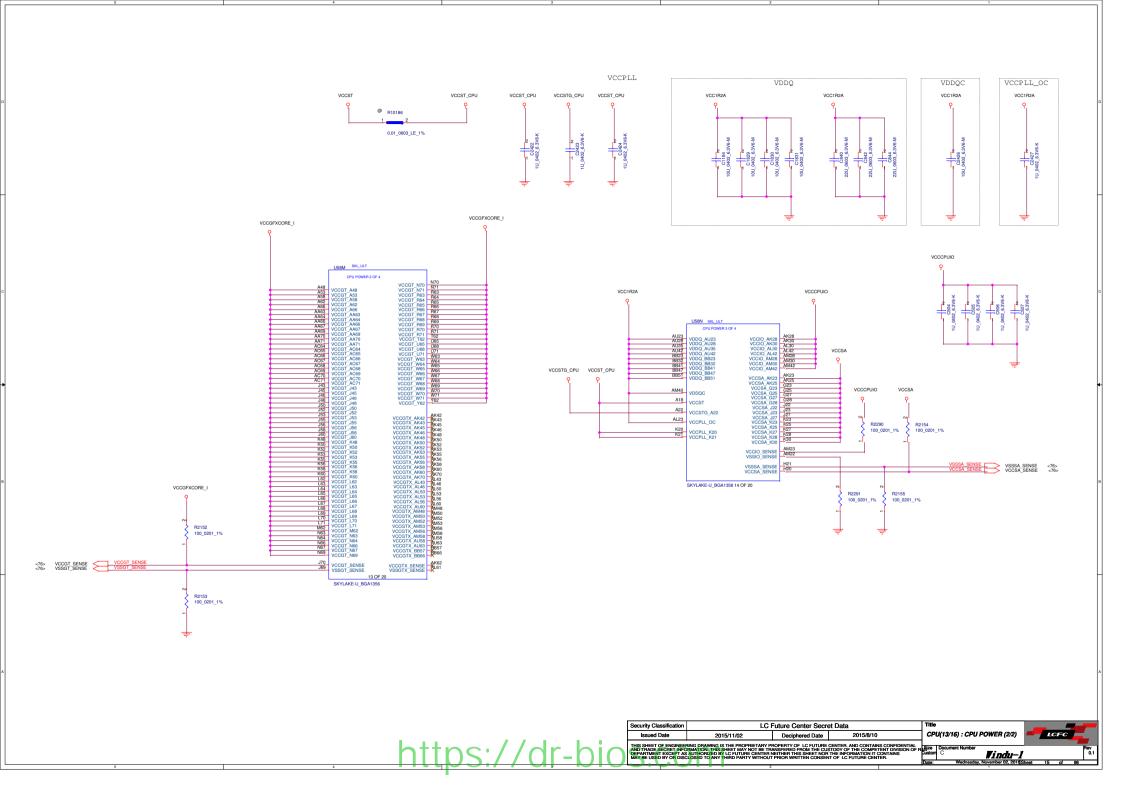


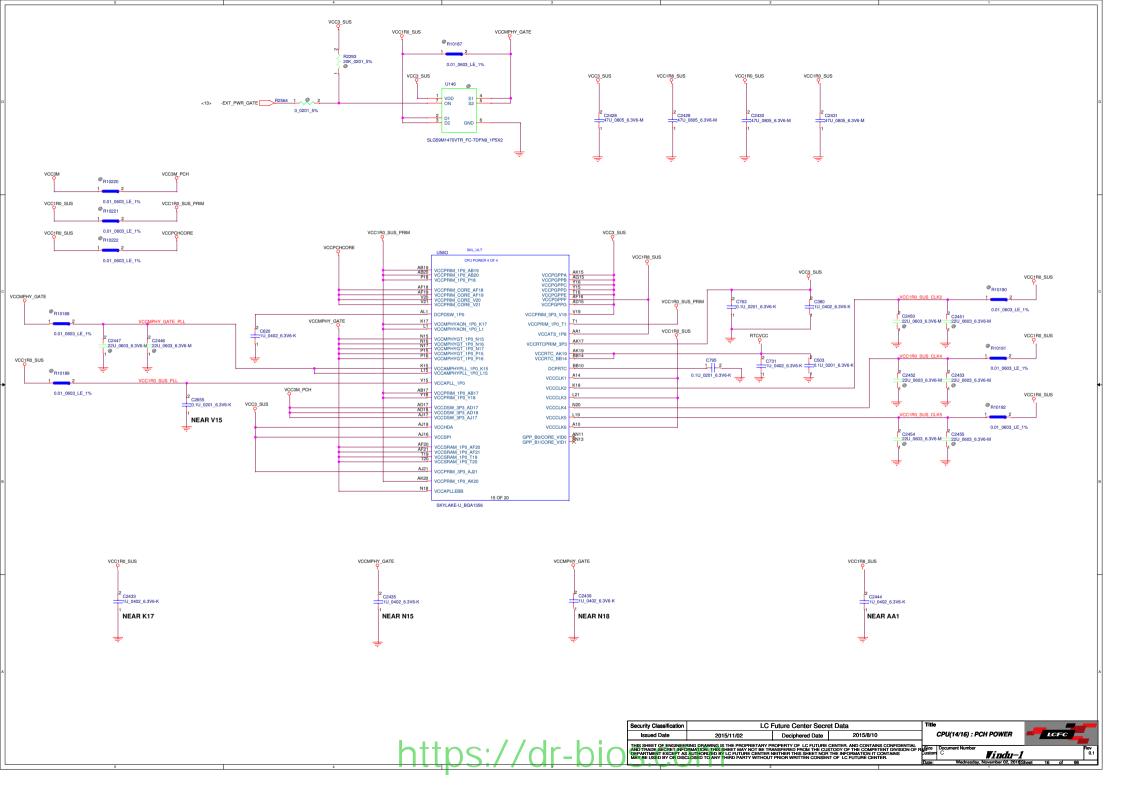


Security Classification LC Future Center Secret Data

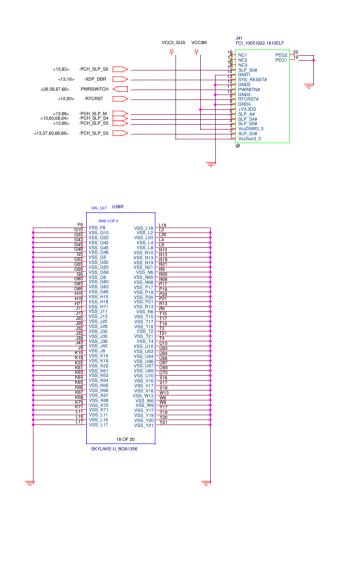
Issued Date 2015/11/02 Deciphered Date 2015/8/10

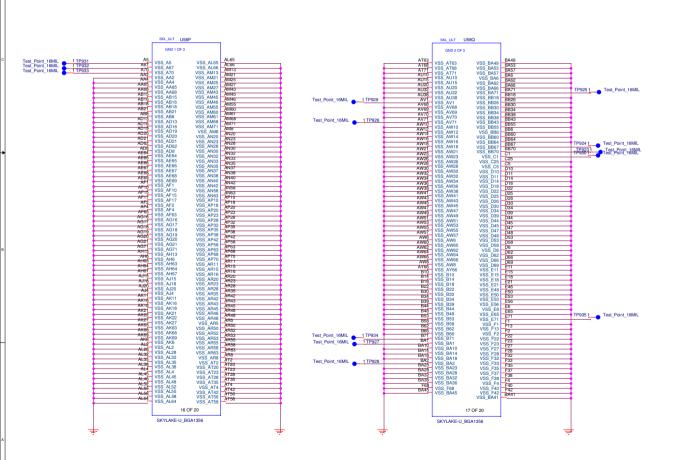
The secret of endoatesmon powers in the properties of the properties o





APS/PETS Interface





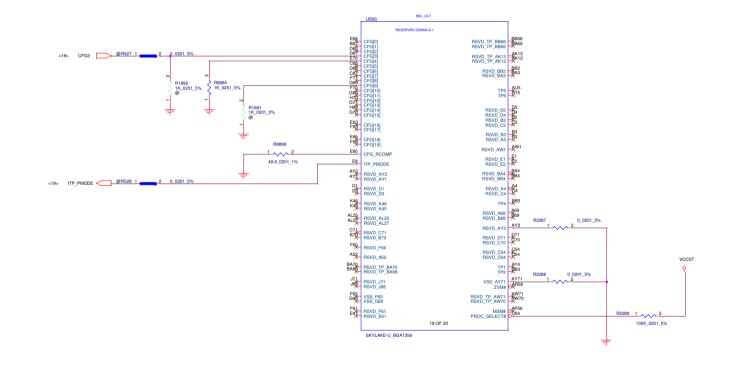
TABLE

CFG0 : Stall Reset Sequence
after PCU PLL Lock until de-asserted
1 : No Stall
0 : Stall

CFG3 : MSR Privacy Bit Feature
1 : MSR (C80h) bit[0] setting
0 : MSR (C80h) bit[0] overridden

CFG4 : eDP Enable
1 : Disabled
0 : Enabled

CFG9 : SVID Bus Communication
1 : Enabled
0 : Disabled
0 : Disabled

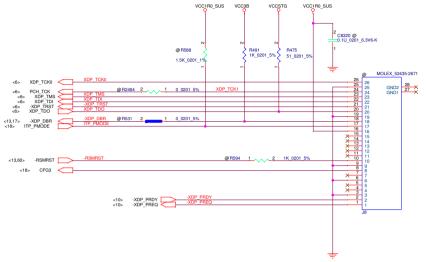




Security Classification LC Future Center Secret Data

Issued Date 2015/11/02 Deciphered Date 2015/8/10

THIS SHEET OF ENGINEERING DRAWNIN IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTANS COMPRESSION OF RESPONSIVE CONTANS CONTANS CONTANS COMPRESSION OF RESPONSIVE CONTANS CONTANT CON



TABLE

Logic	Ref Des	Merged	DCI 2.0
Page 6	R2	ASM	ASM
Page 7	R2559	ASM	NO_ASM
Page 18	R1892	ASM	NO_ASM
	J8	ASM	NO_ASM
	C8320	ASM	NO_ASM
	R475	ASM	ASM
	R491	ASM	ASM
D 40	R588	ASM	NO_ASM
Page 19	R594	ASM	NO_ASM
	R2494	ASM	NO_ASM

Security Classification

LC Future Center Secret Data

Title

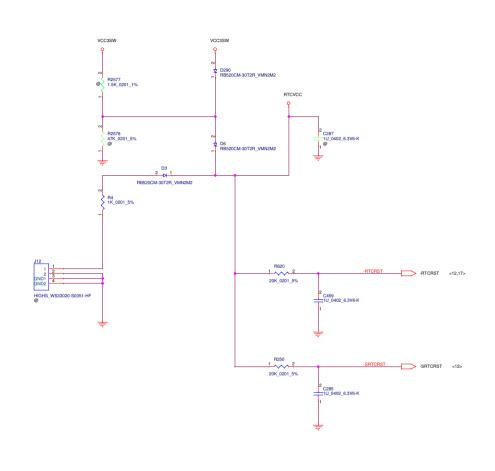
Issued Date

2015/11/02

Deciphered Date

2015/8/10

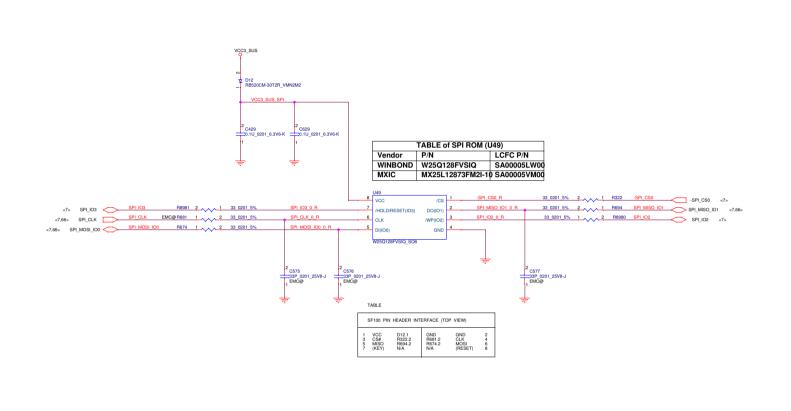
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL, WIND TRADE SECRET INFORMATION THIS SHEET MAY OF TRANSFERED FROM THE CUSTOMY OF THE CONFIDENTIAL SHEET AND THE PROPRIETARY DIVISION OF THE PROPERTY OF THE PROPRIETARY DIVISION OF THE PROPRIETARY DIV



Security Classification LC Future Center Secret Data

Issued Date 2015/1/02 Deciphered Date 2015/0/1/02 2015/0/1/02

These secret or enconscience powers to the properties of the properties of



Security Classification L.C. Future Center Secret Data

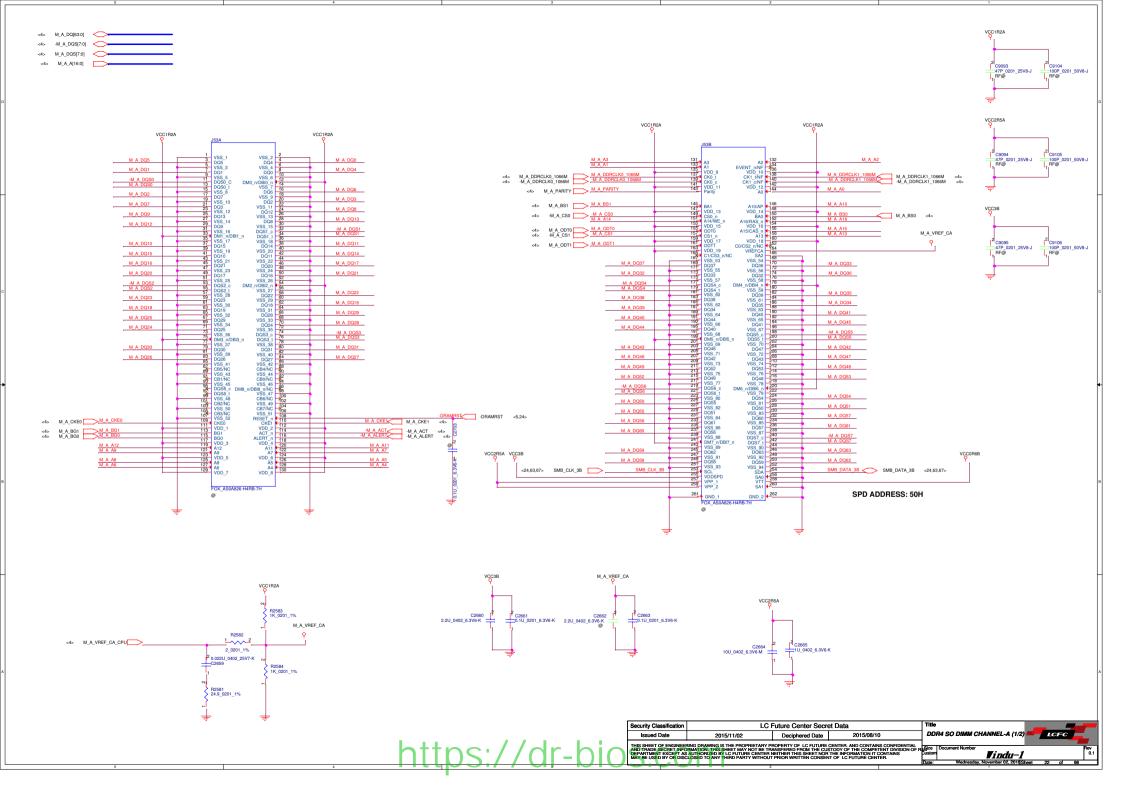
Title

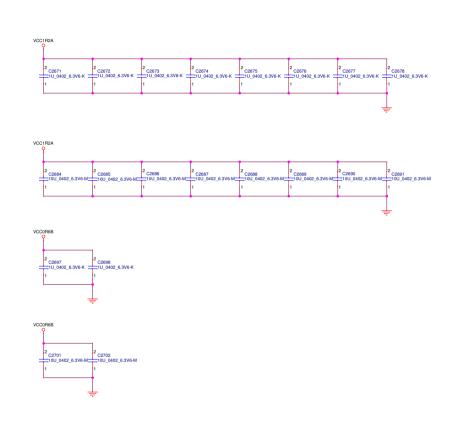
SPIFLASH

SPIFLASH

Title

S

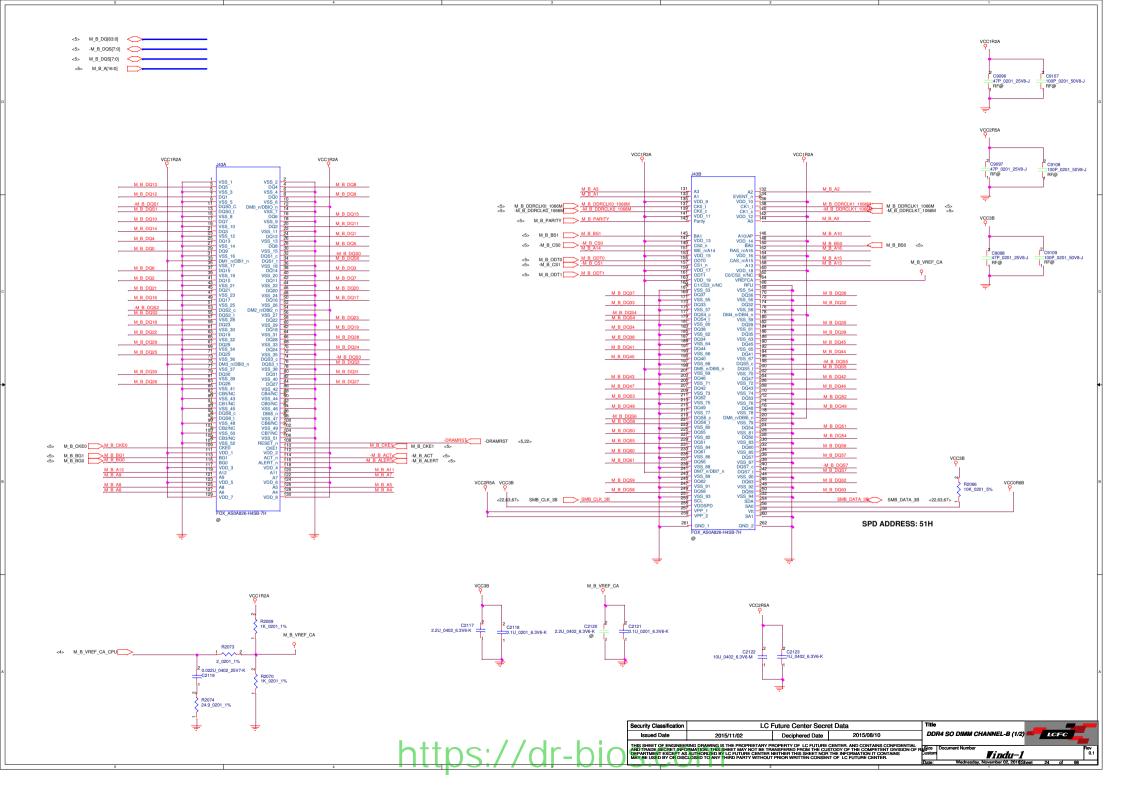




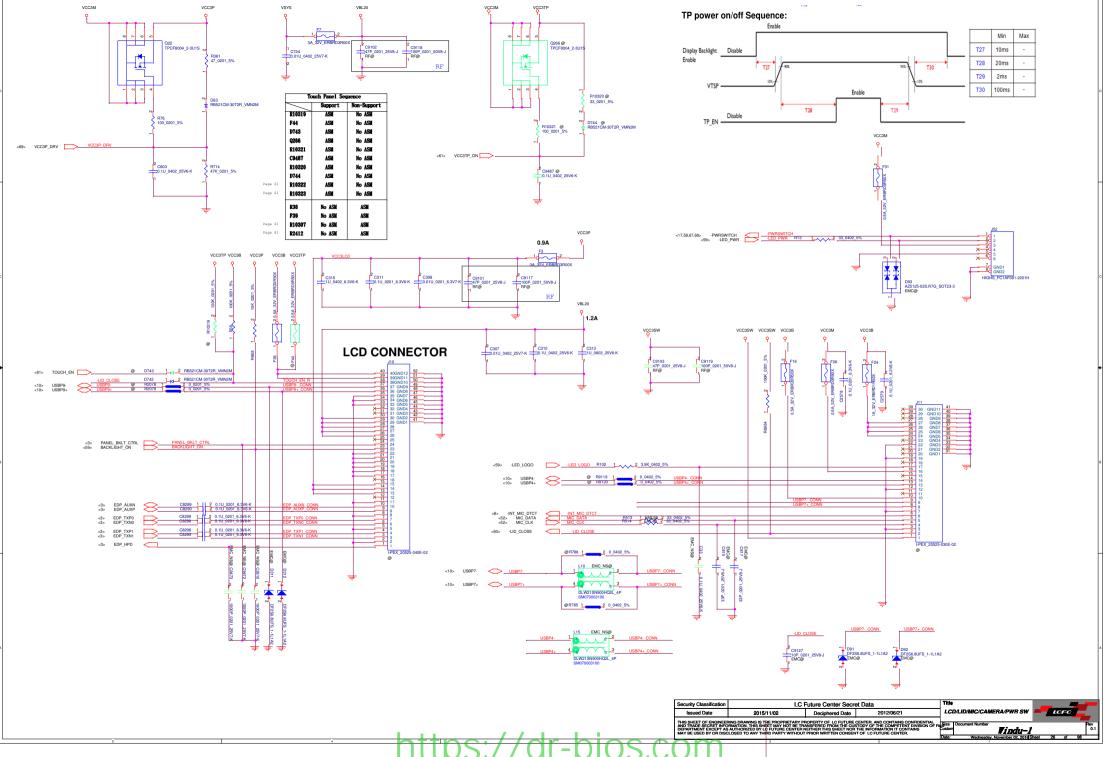
Security Classification LC Future Center Secret Data

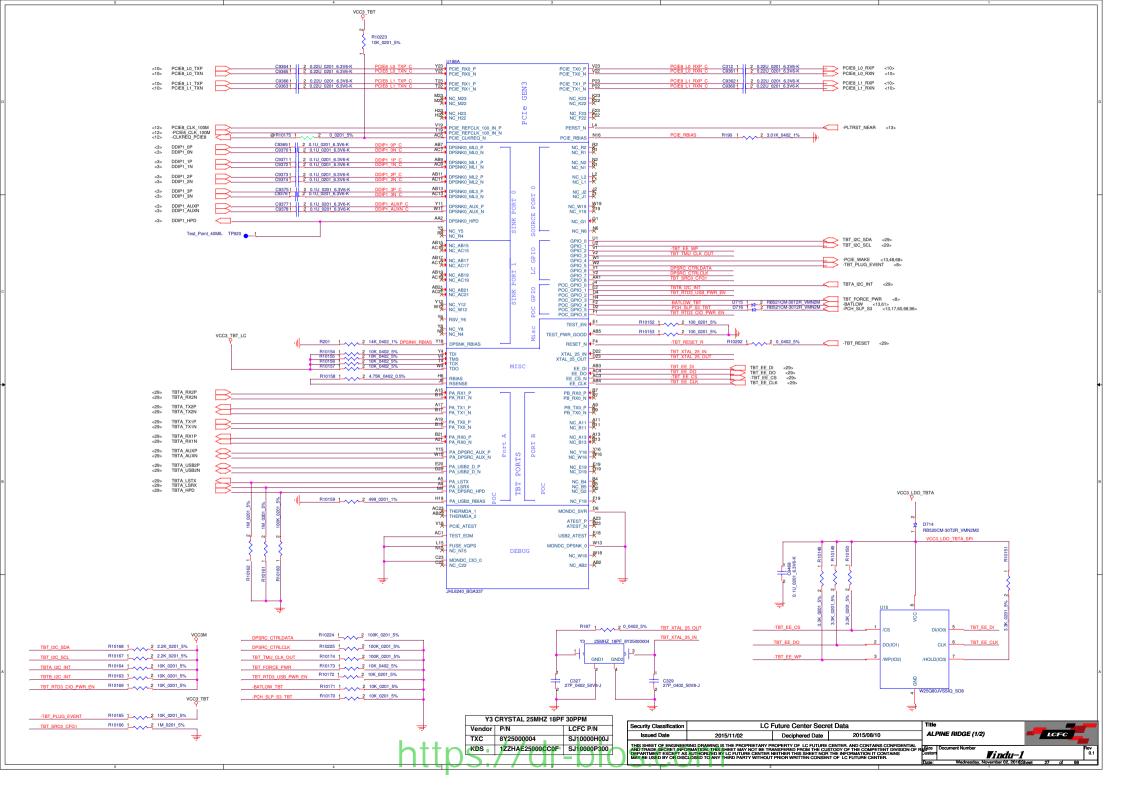
Issued Date 2015/11/02 Deciphered Date 2015/08/10

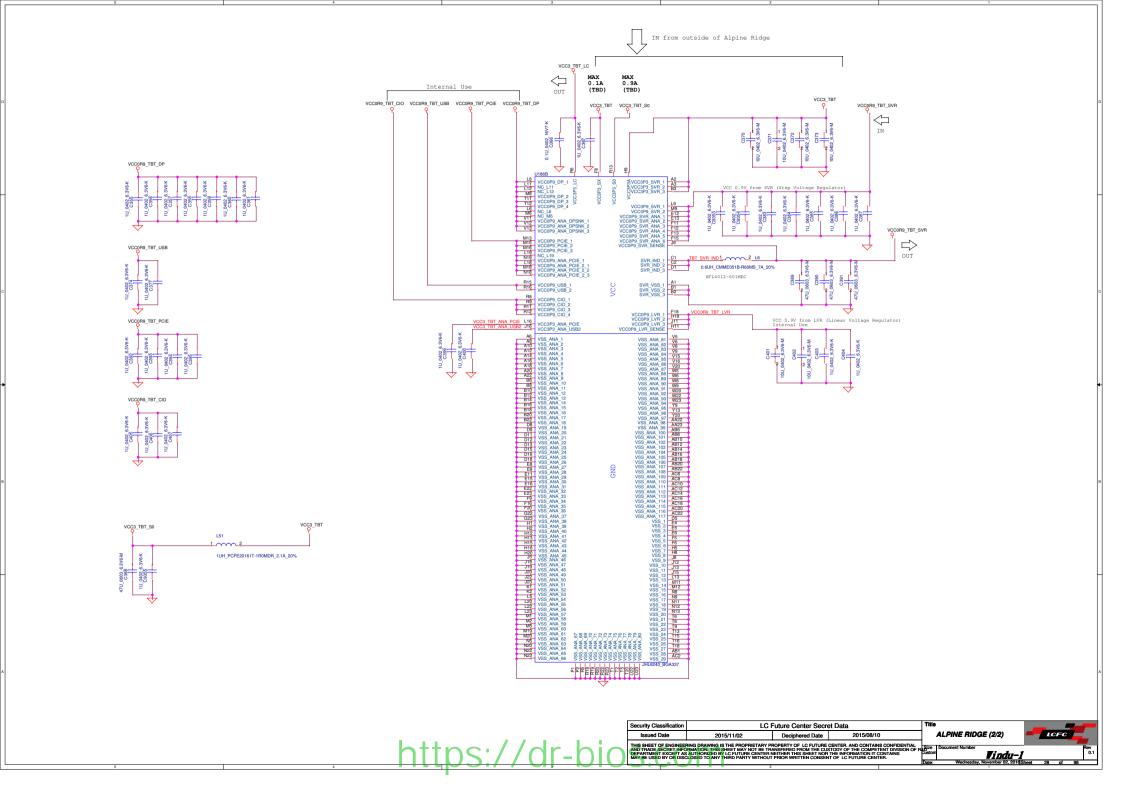
THIS SHEET OF ENGINEERING DRAWNIN IS THE PROPRIETARY PROPERTY OF LC TUTINE CENTER. AND CONTAINS COMPENSATION OF THE CAMPETER OF THE OWNER OWNER

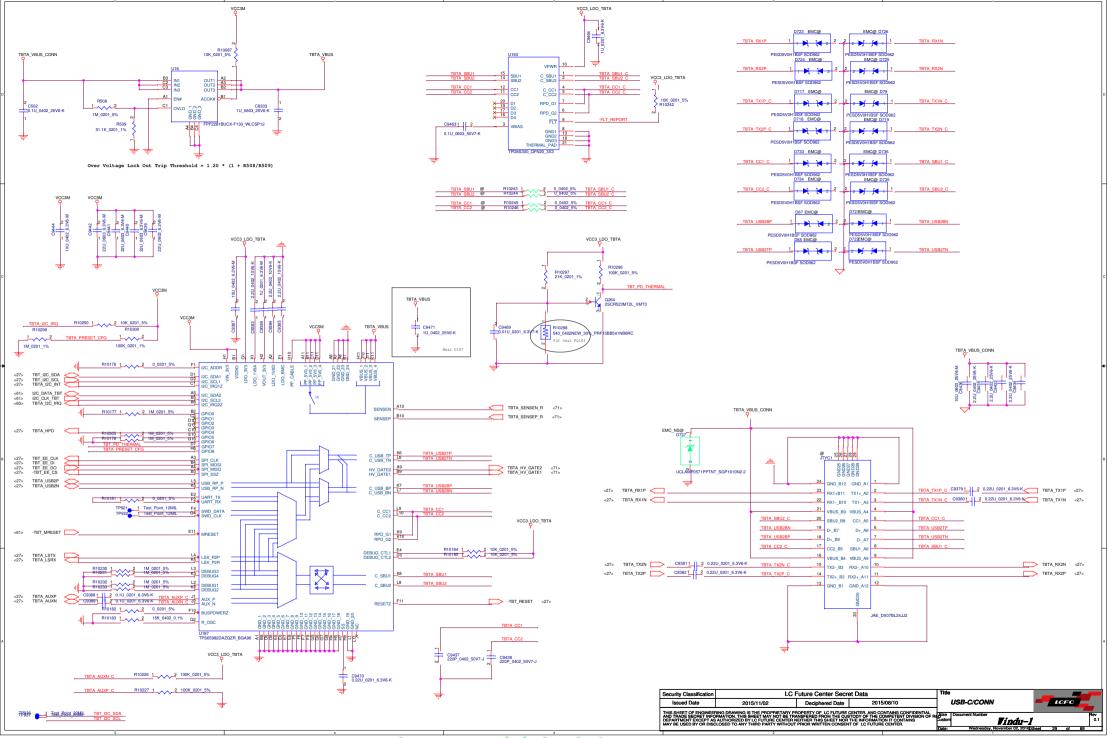




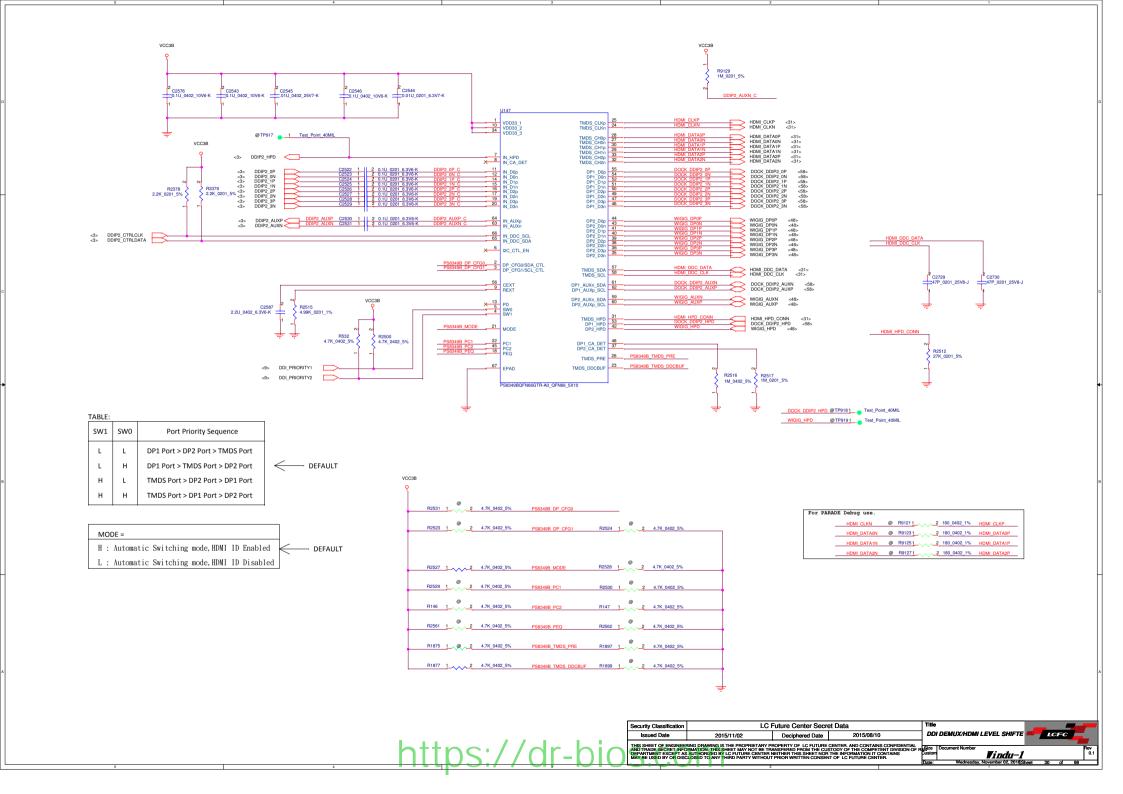


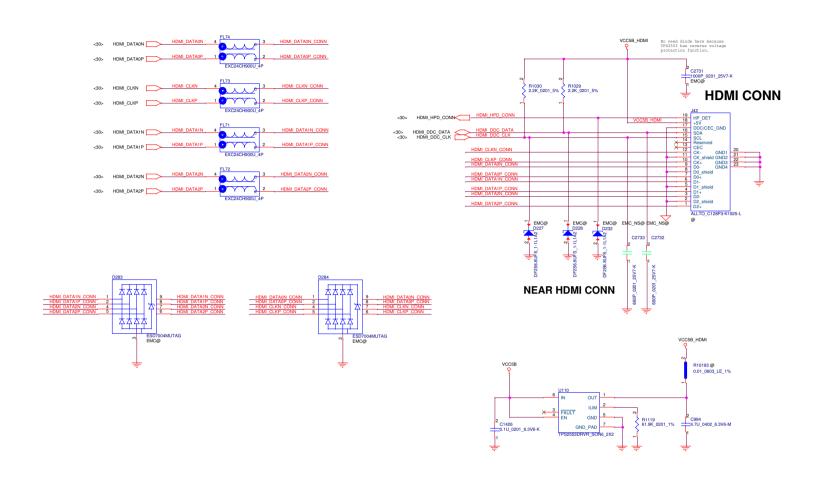




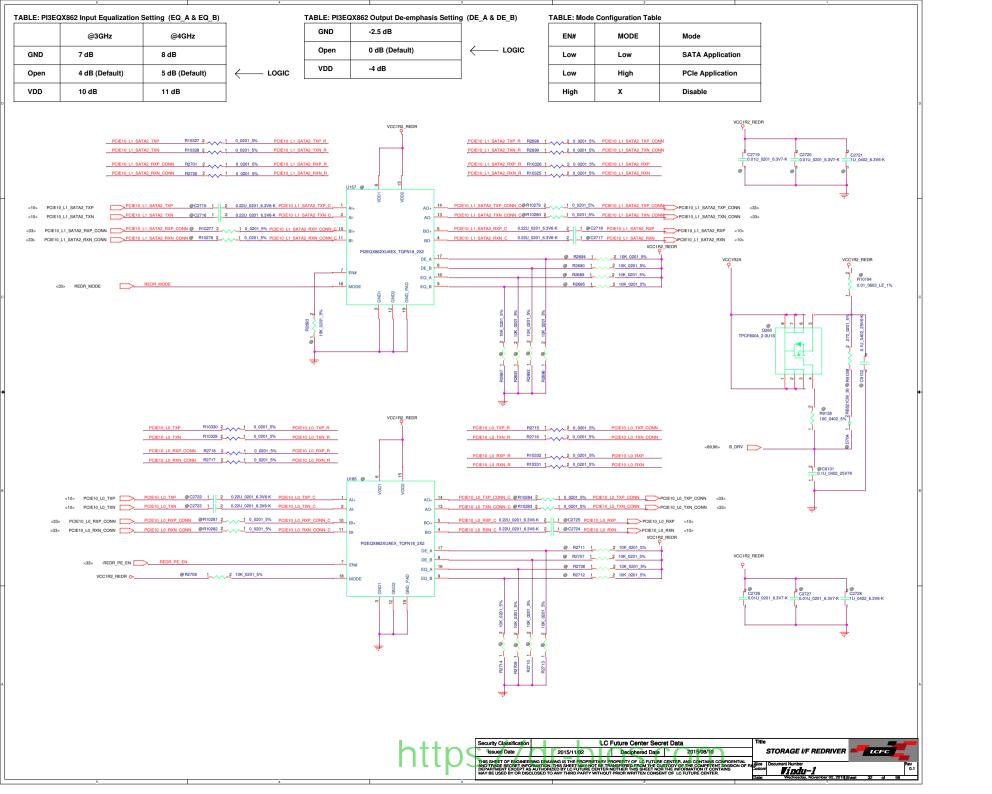


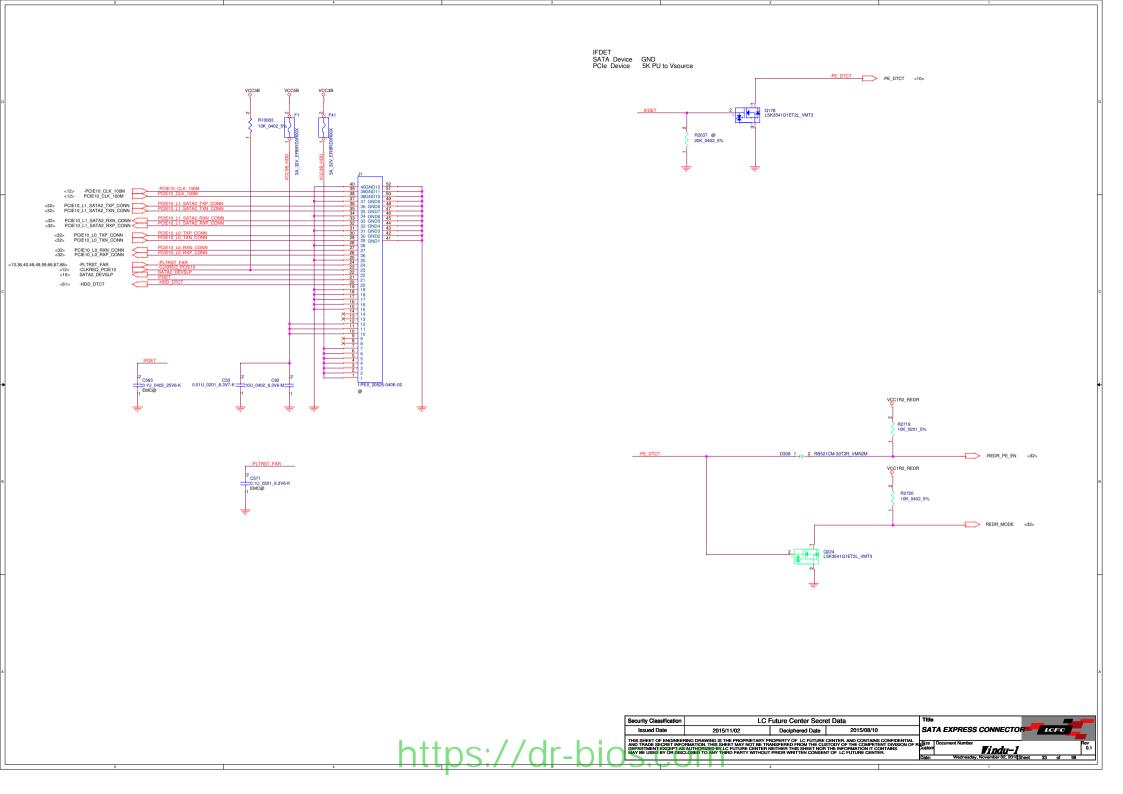
https://dr-bios.com

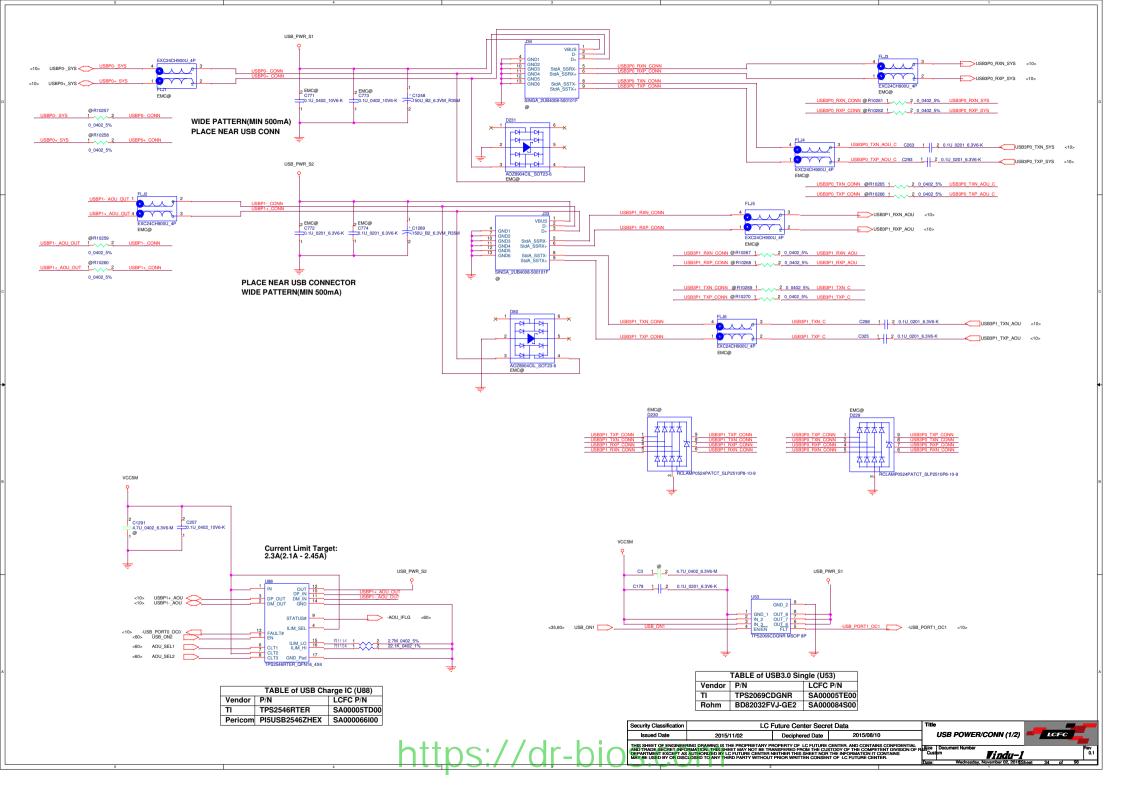


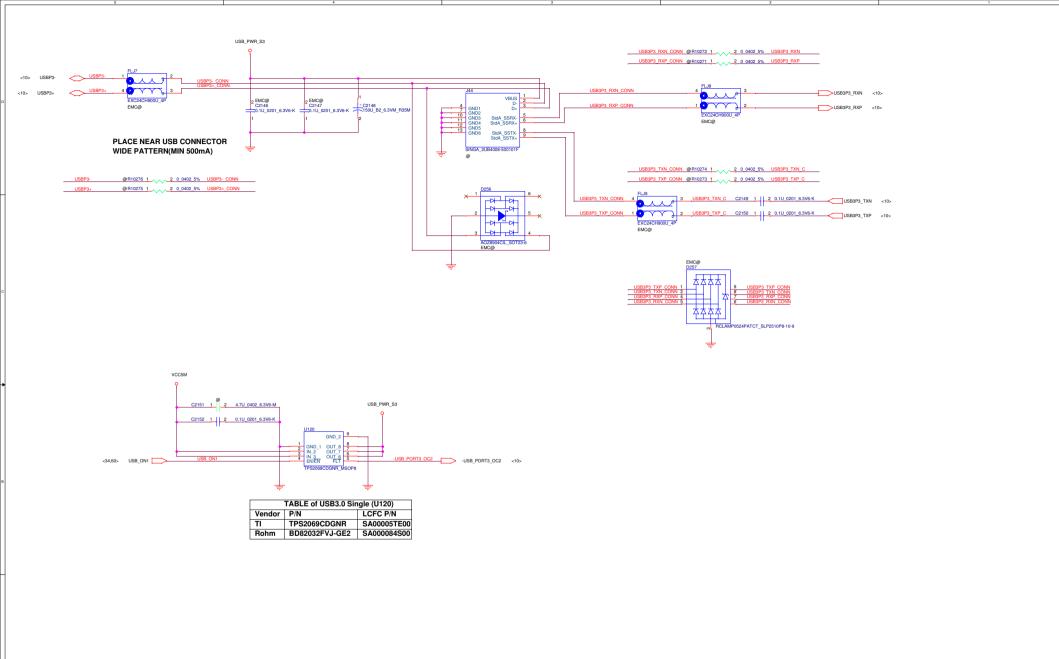


Security Classification LC Future Center Secret Data **HDMI CONNECTOR** LCFC 2015/11/02 Deciphered Date 2013/08/05 THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC ENTURE CENTER. AND CONTAINS COMFIDENTIAL AND TRADES SCIENT INFORMATION. THIS SHEET HAN OT SET TRANSFERD FROM THE LCISTODY OF THE COMPRETENT DINISION OF DEPARTMENT EXCEPT AS JUTHORIZED BY LC FUTURE CENTER NETHER THIS SHEET NOTH THE NORMATION IT CONTAINS WAY SEE USED BY OUR DISCUSSED TO ANY HINDO PRINTY WITHOUT PRION WRITTEN CONSTRUCT OF LC FUTURE CENTER. Findu-1
Nednesday, November 02, 2016 Sheet

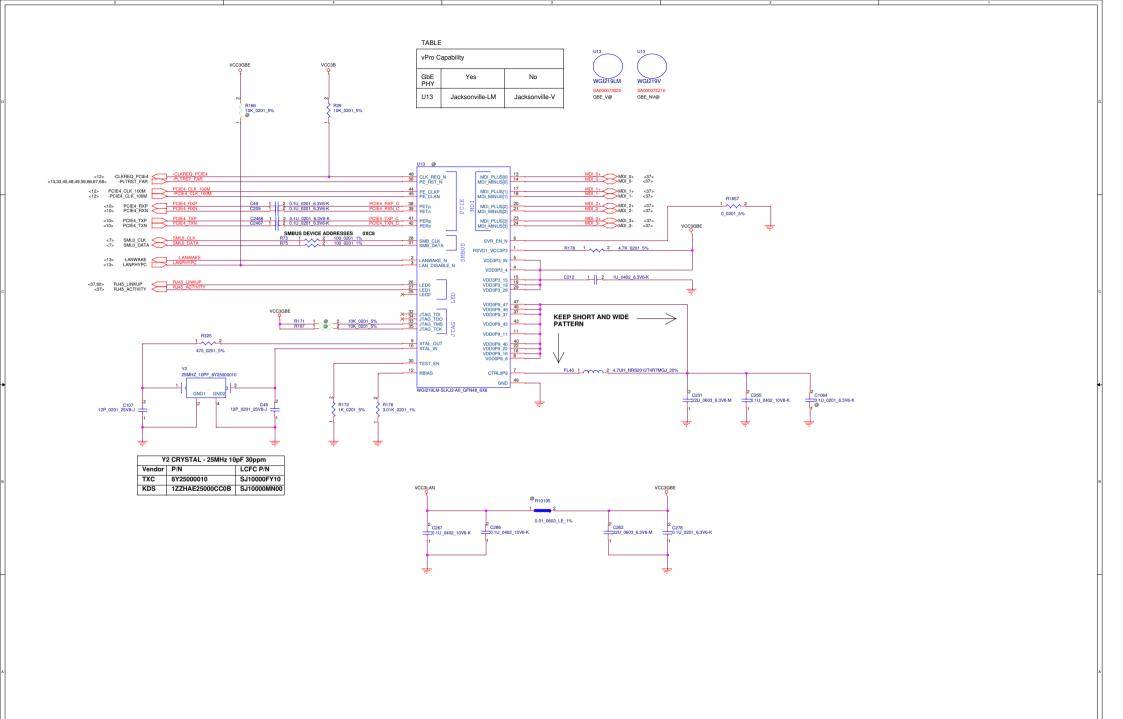








Security Classification LC Future Center Secret Data USB POWER/CONN (2/2) LCFC Issued Date 2015/11/02 Deciphered Date 2015/08/10 THE SHEET OF PROMISEND CHANNES IS THE PROPRETARY PROPERTY OF LIC PUTURE CLATTER, AND CONTAND COMPOSITION OF MINISTRANCE SCHOOL PROPERTY OF THE CONTAND CHANNES CHANNES FOR THE PROPERTY OF THE CHANNES FOR THE PROPERTY OF THE WIGHTH CHANNES FOR THE WIGHT CHANNES FOR THE WIGHTH CHANNES FOR THE WIGHT CHANNES FOR THE WIGHTH CHANNES FOR THE WIGHT CHANNES Findu-1 Nednesday, November 02, 2016 Sheet



https://dr-bio

Security Classification

LC Future Center Secret Data

Title

Issued Date

2015/11/02

Deciphered Date

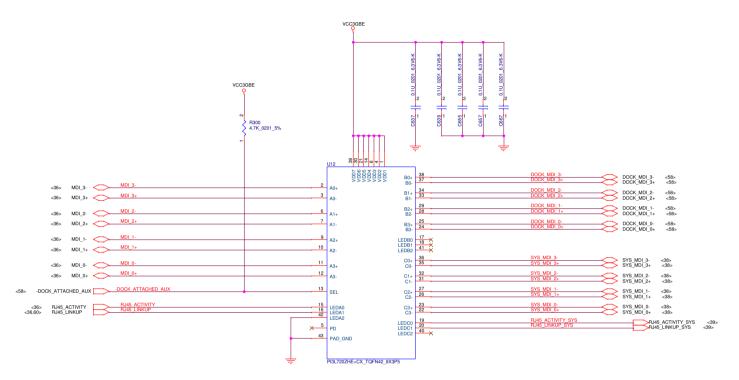
2015/08/10

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND OTHAGE SECRET INFORMATION IT ONLY THE SHEET MAY ONE ET MANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER HER THE SHEET HOST THE INFORMATION IT CONTAINS OF MAY SHEET AND THE THE SHEET HAVE THE SHEET MAY METHED AND THE THE SHEET HAVE THE SHEET AND THE SHEET MAY METHED AND THE SHEET MAY METHED CENTER HER HER HER HER SHEET HOST THE INFORMATION IT CONTAINS OF MAY HERD PARTY WHITCH PROPER WHAT HE CONSESS FOR CENTER.

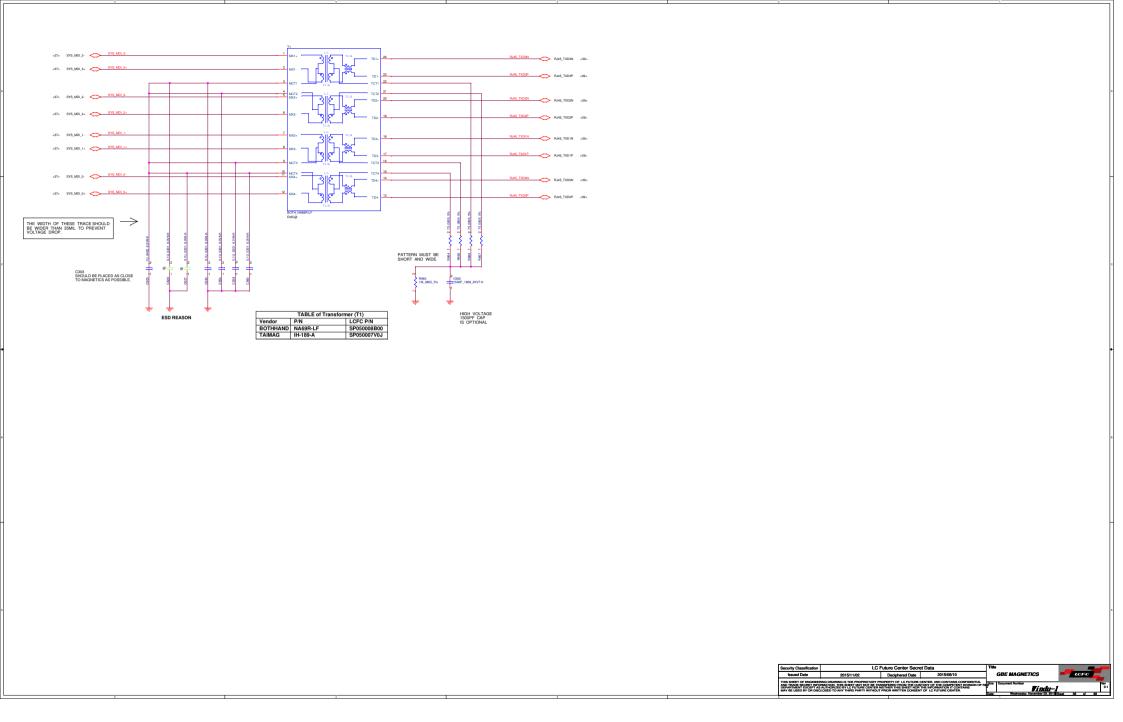
DEVICE THE SHEET OF THE SHEET MAY WHITCH PROPER WHITCH EXCEPT OF LC PUTURE CENTER.

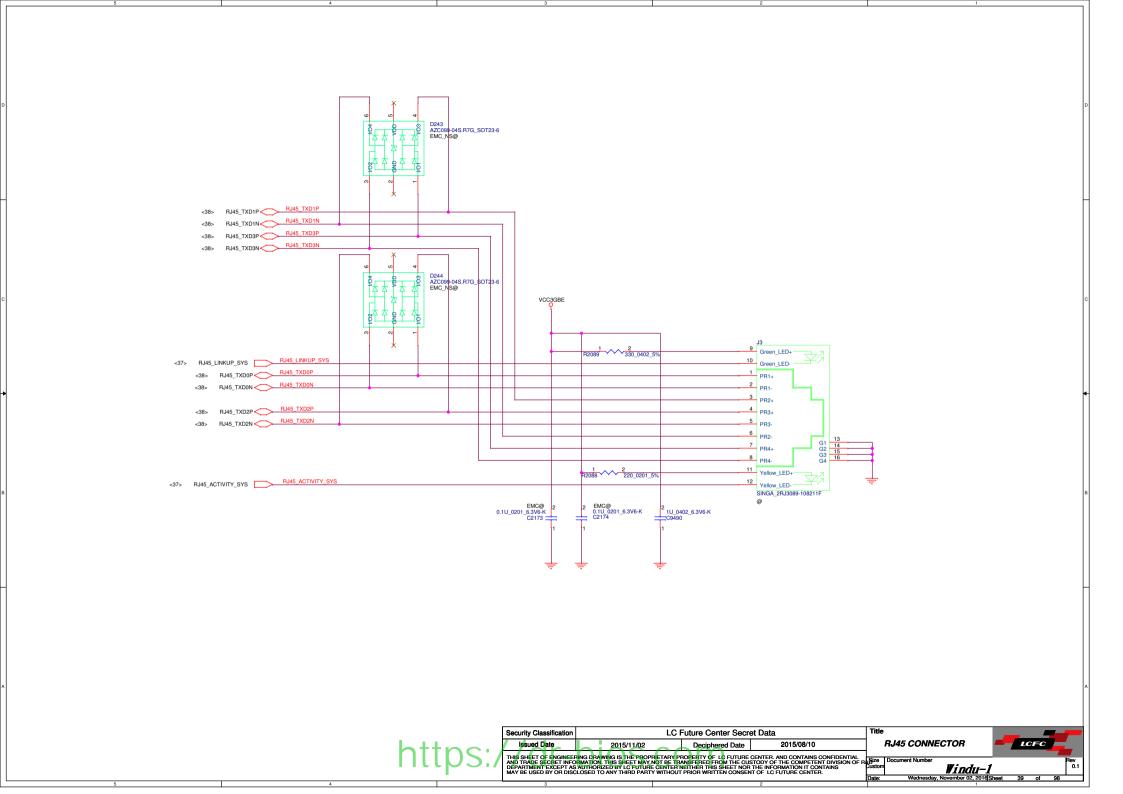
The GBE JACKSONVILLE

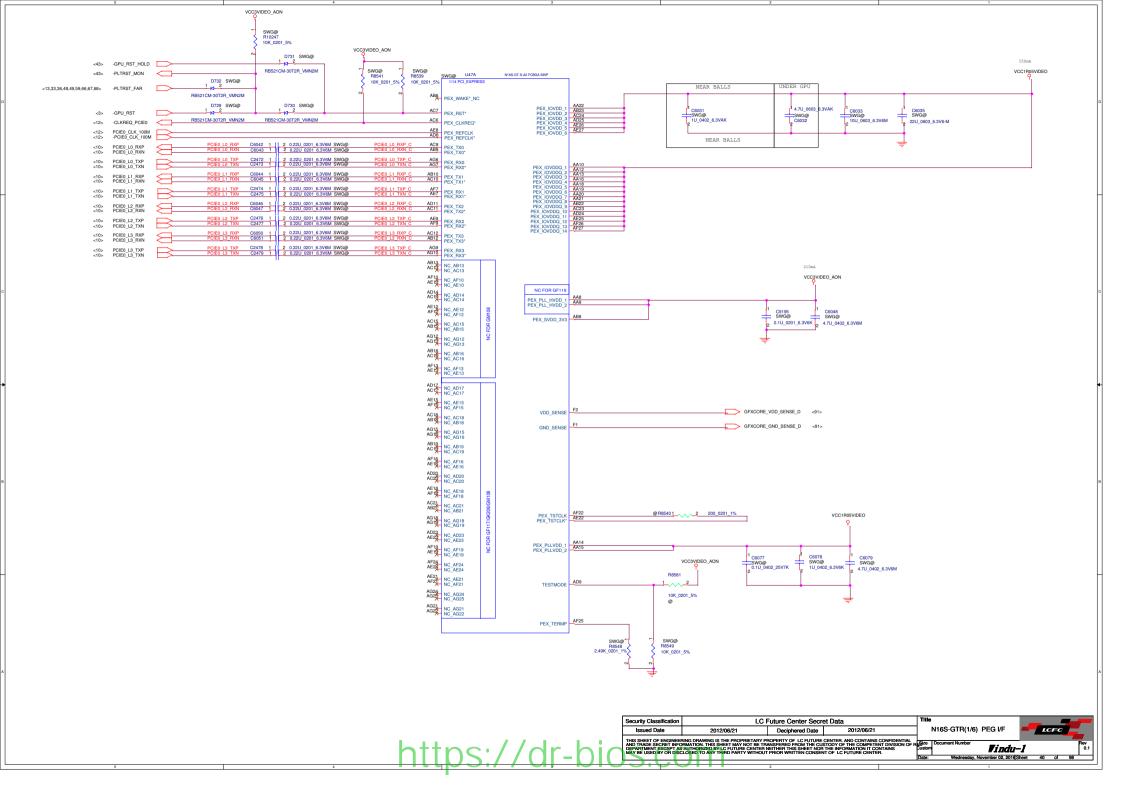
| Document Number | Docume

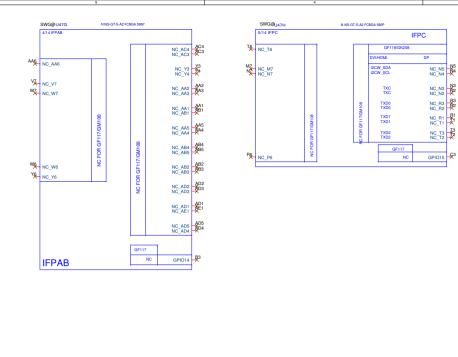


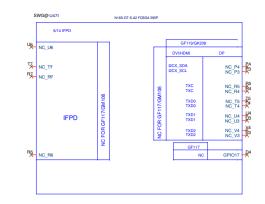
Т	TABLE of LAN Switch (U12)				
Vendor	P/N	LCFC P/N			
PERICOM	PI3L720ZHE+CX	SA00007E900			
TI	TS3L501ERUAR	SA000072400			

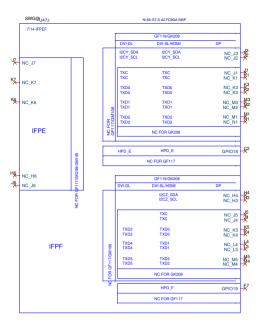












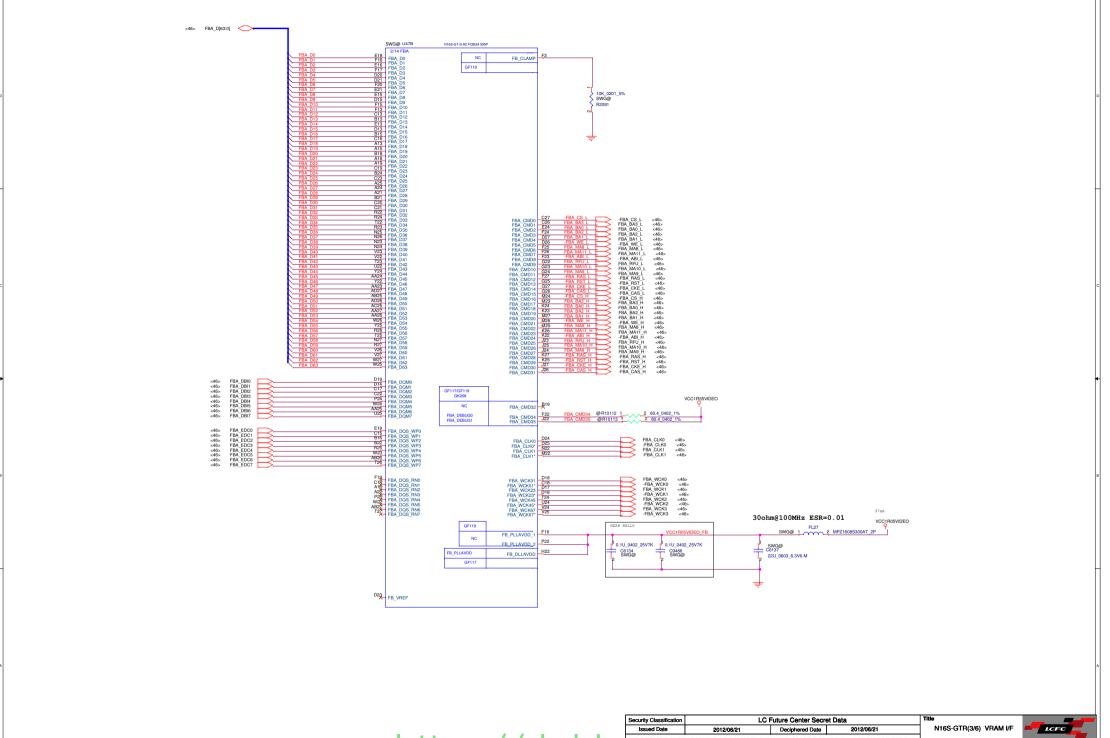
https://dr-bio

Security Classification LC Future Center Secret Data Title
Issued Date 2012/05/02 Deciphered Date 2012/05/02

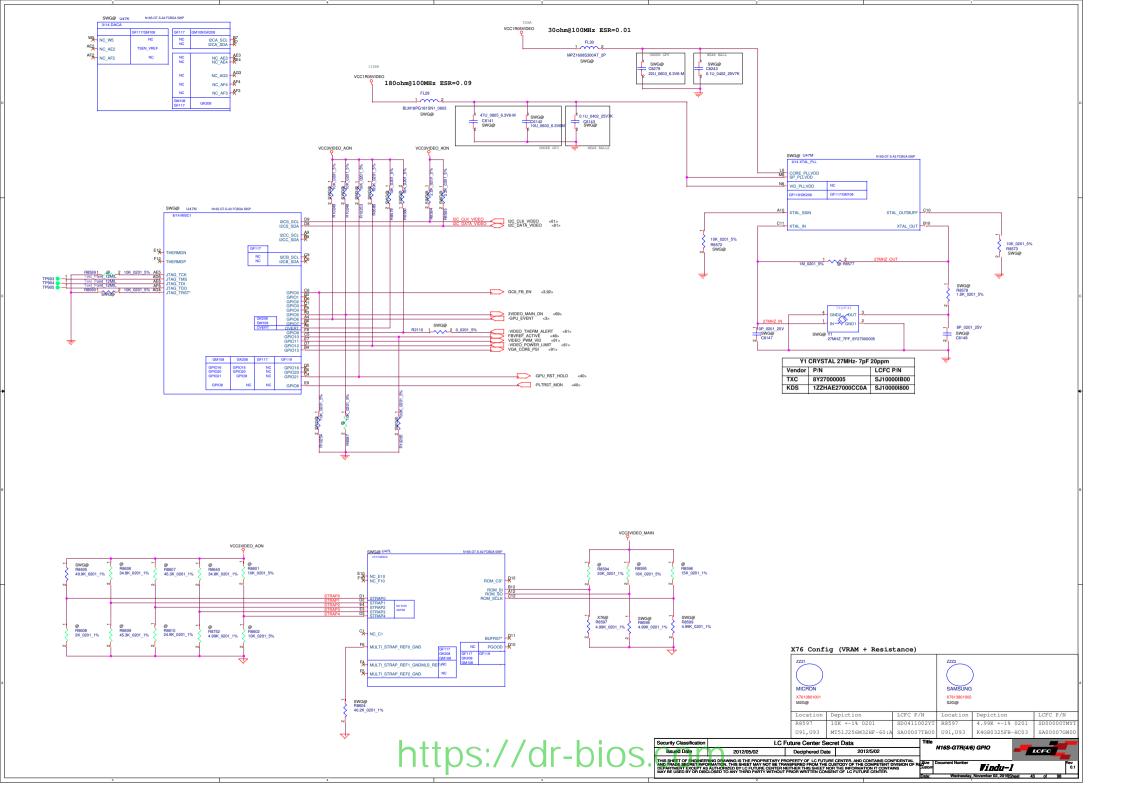
This SHEET OF ENGINEERING DRAWING IS THE PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL PROPERTY OF LC FUTURE CENTER.

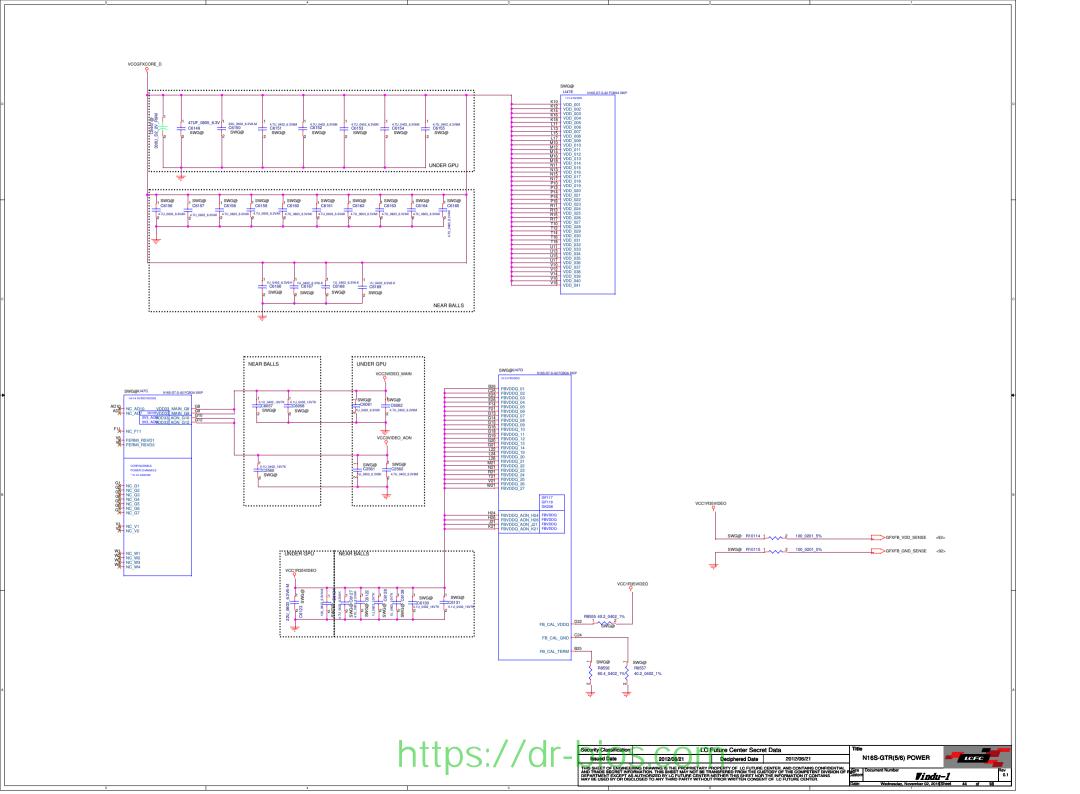
MAY BE USED BY OF DESCRIPTION OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL PROPERTY OF LC FUTURE CENTER.

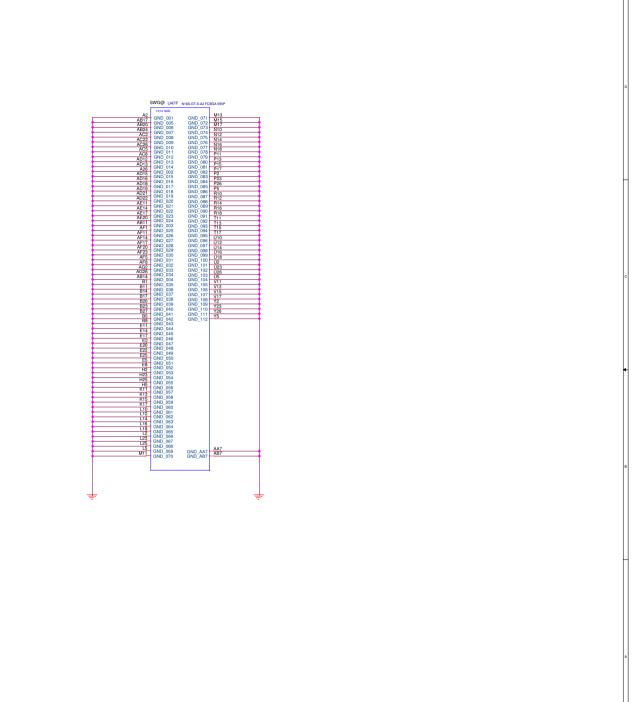
RESIDENTIAL PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL PROPERTY



THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CHITER, AND CONTAINS CONSIDERING, AND HITADAS SCIENCE WOO MIGHTON, HIS SHEET MAY ON HE THANKESPEED FIGH THE CUSTOON OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS UNFORCED BY LC FUTURE CENTER HIS SHEET AND THE INFORMATION IT CONTAINS MAY BE USED BY OF IDECUCED FOR ANY THIS PRAFFY WITHOUT PROFE WHITE CONDITION OF LC FUTURE CHITER. Vindu-1 Vednesday, November 02, 2016 Sheet







https://dr-bio

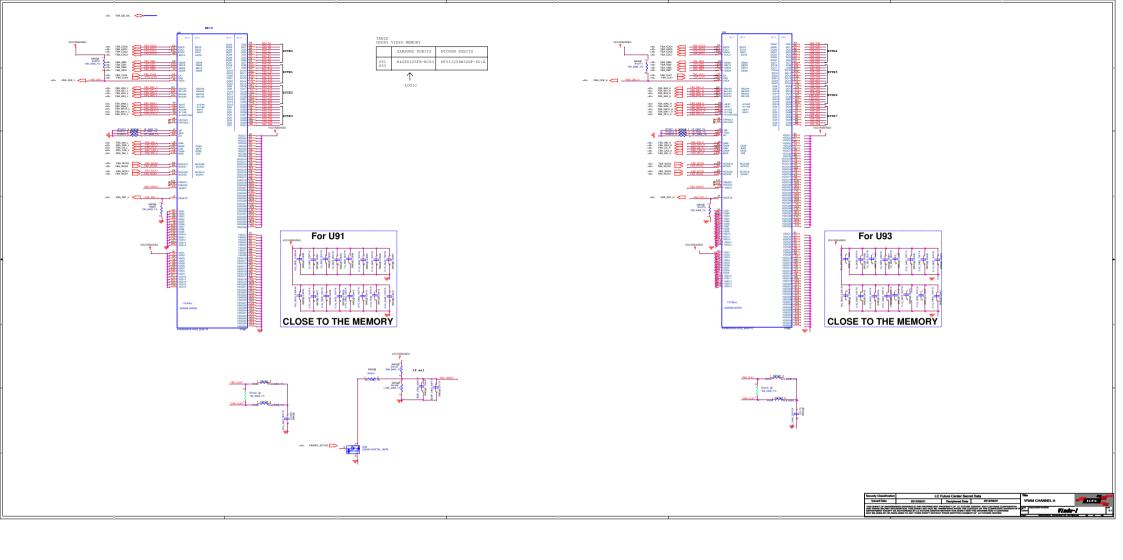
Security Classification

LC Future Center Secret Data
Title

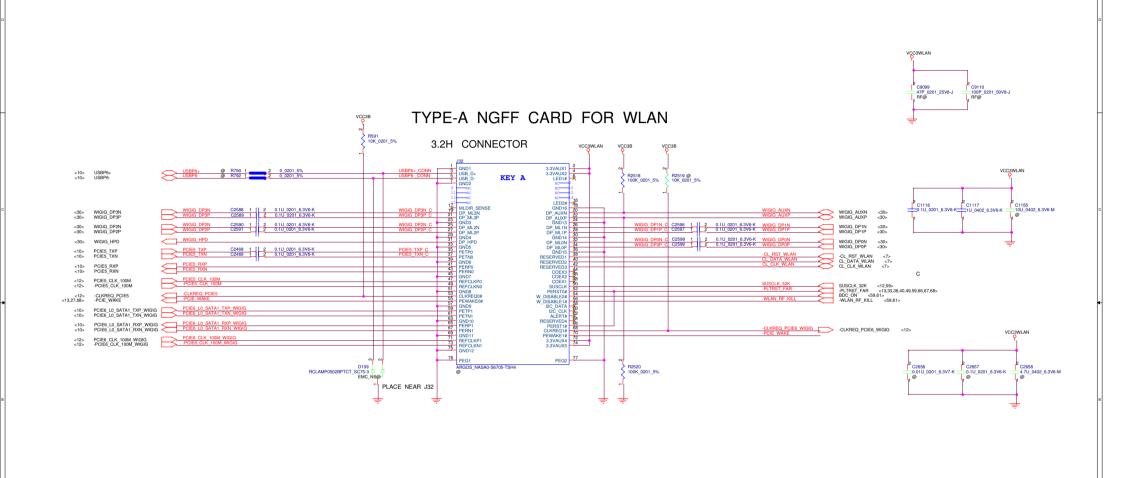
Susual Date
2012/06/21

THIS SHEET OF ENCRETENIS DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL
DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NETHER THIS SHEET TWO R THE INFORMATION IT CONTAINS
DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NETHER THIS SHEET TWO R THE INFORMATION IT CONTAINS
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Date:
Wednesday, November 02, 2019 Sheet



	•
	^
5	Security Classification LC Future Center Secret Data Title issued Date 2012/05/02 Deciphered Date 2012/5/02 MMM Security Classification Property or Lc Future Center And Contrains Conference Transcriptor Property or Lc Future Center And Contrains Conference Transcriptor Property Center Conference Transcriptor Property Center Cent



Security Classification LC Future Center Secret Data

Issued Date 2015/1/102 Deciphered Date 2015/08/10

Title M2 SOCKET 1 MODULE UF

This sheet of Engineering prawning is the Propriet Any Property of LC Future center, AND CONTAINS CONFIDENTIAL

This sheet of Engineering Drawning is the Propriet Any Property of LC Future center, AND CONTAINS CONFIDENTIAL

The M2 SOCKET 1 MODULE UF

But 2 SOCKET 1 MODULE UF

But 3 SOCKET 1 MODULE UF

But 3 SOCKET 1 MODULE UF

But 4 SOCKET 1 MODULE UF

But 4 SOCKET 1 MODULE UF

But 5 SOCKET 1 MODULE UF

But 5 SOCKET 1 MODULE UF

But 6 SOCKET 1 MODULE UF

But 7 SOCKET 1 MODULE UF

But 7 SOCKET 1 MODULE UF

But 8 SOCKET 1 MODULE UF

But 7 SOCKET 1 MODULE UF

But 8 SOCKET 1 MODULE UF

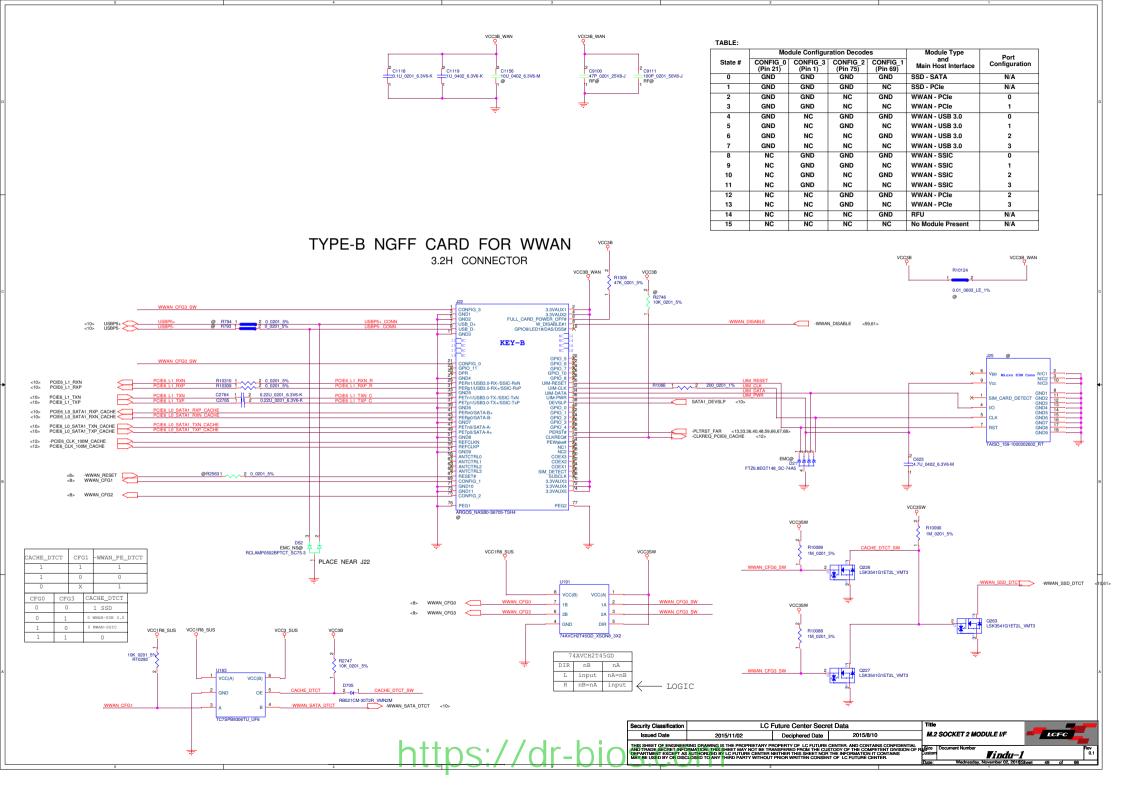
But 7 SOCKET 1 MODULE UF

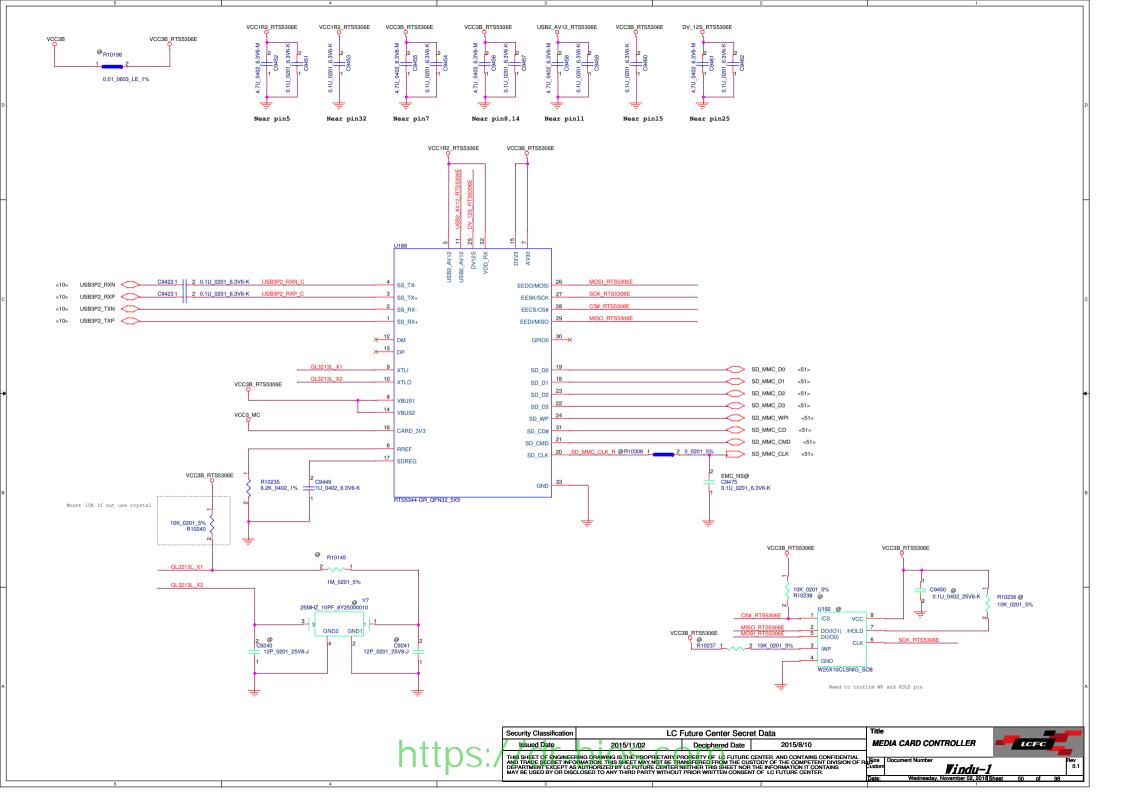
But 8 SOCKET 1 MODULE UF

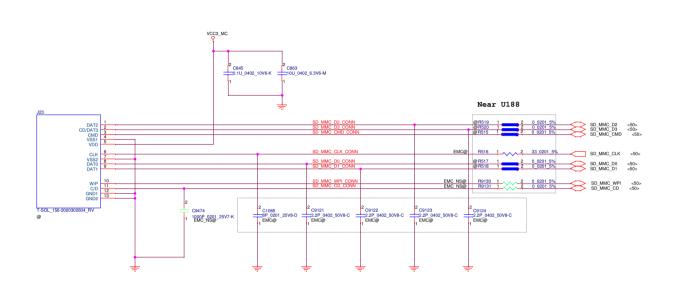
But 8 SOCKET 1 MODULE UF

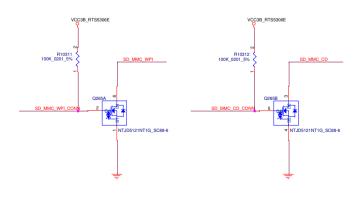
But 8 SOCKET 1 MODULE UF

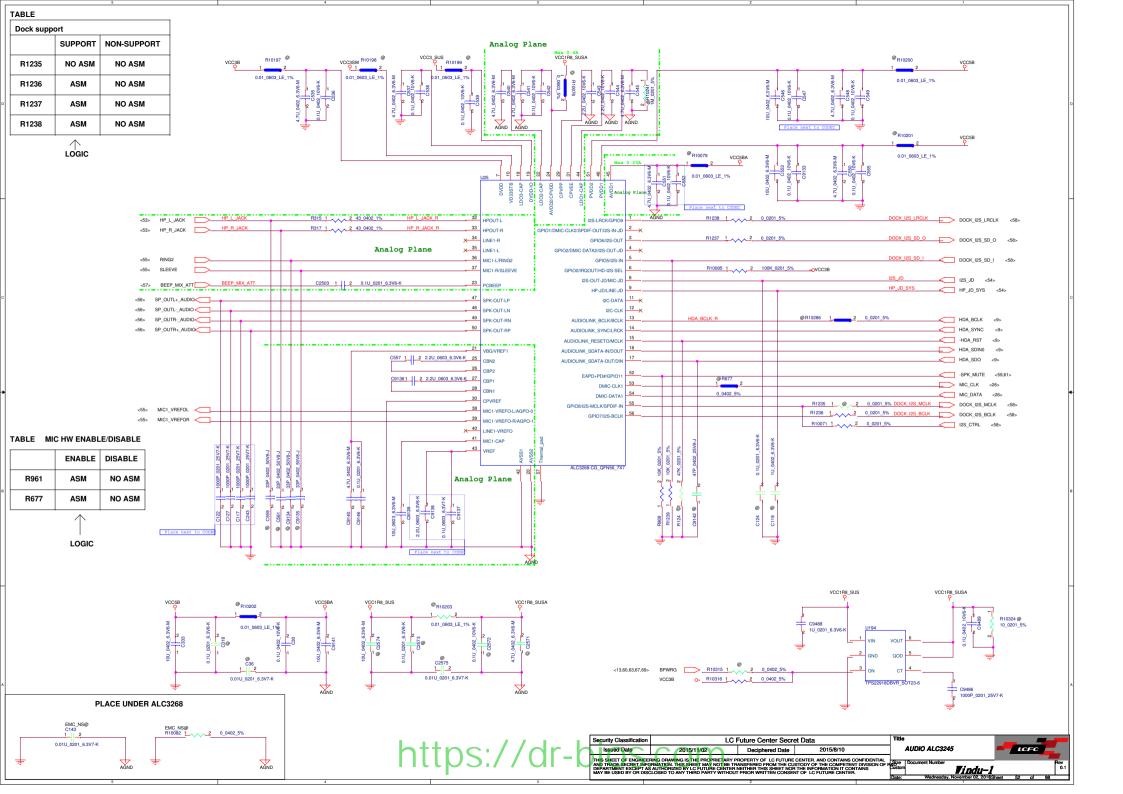
But 9 SOCKET 1 MODULE U

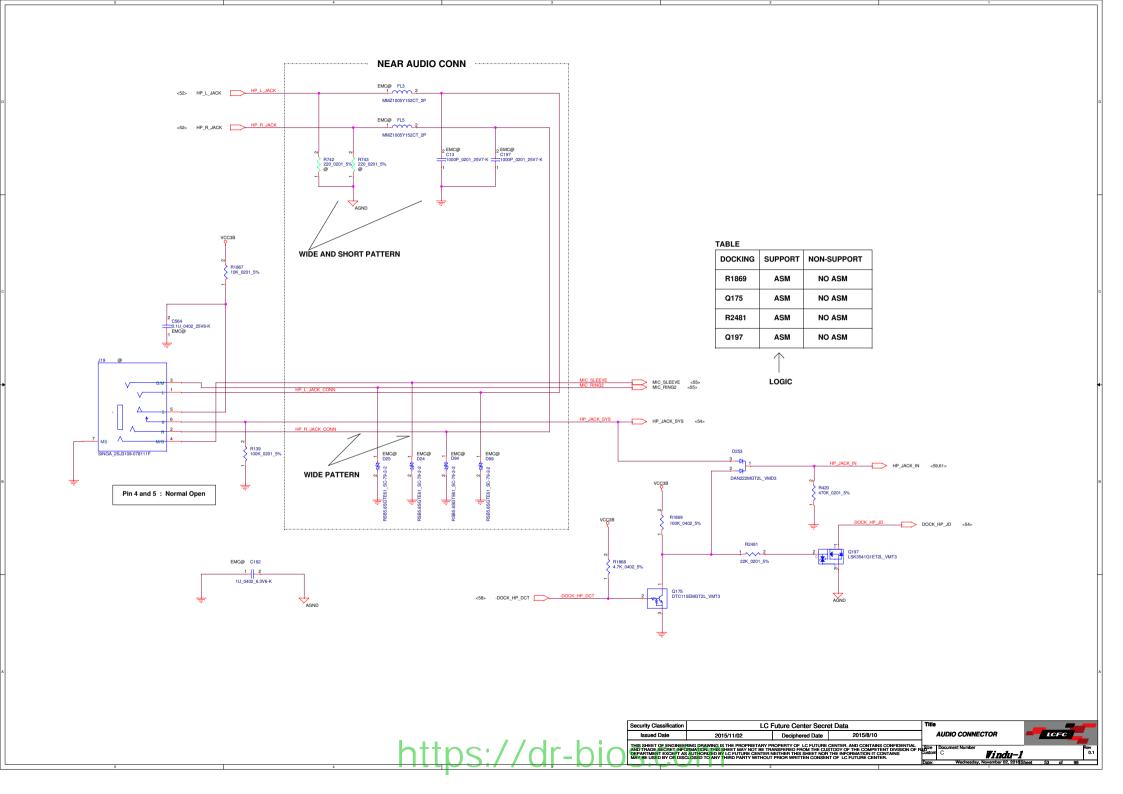


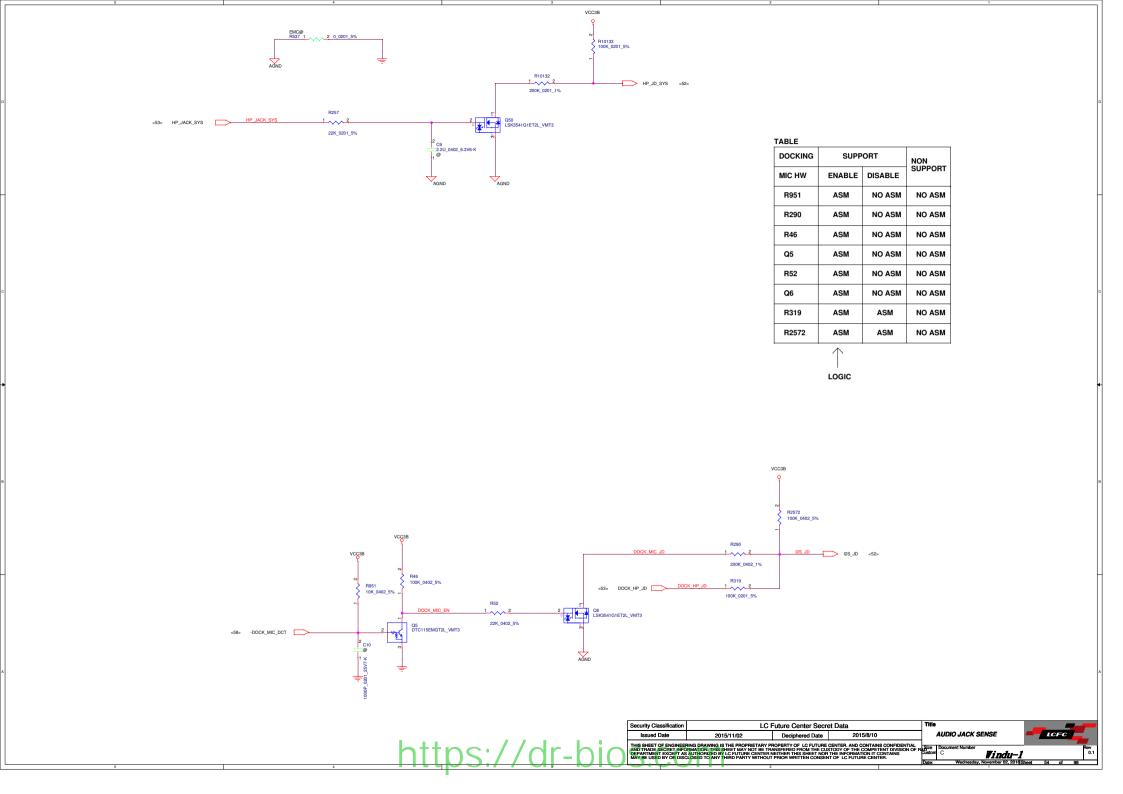


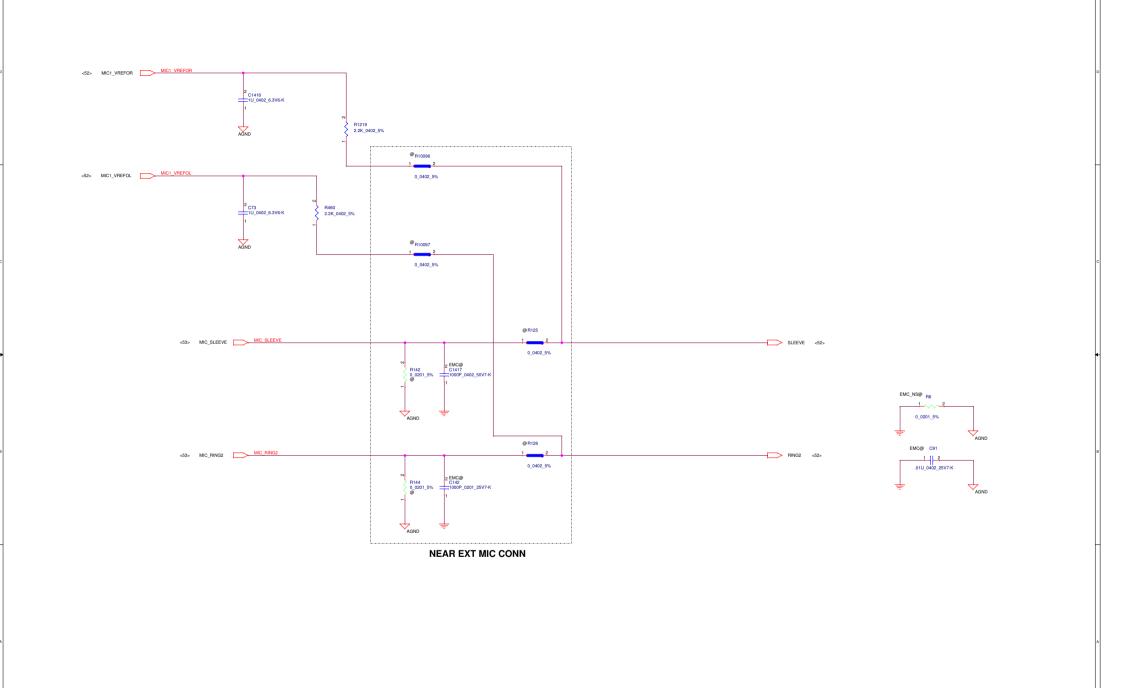








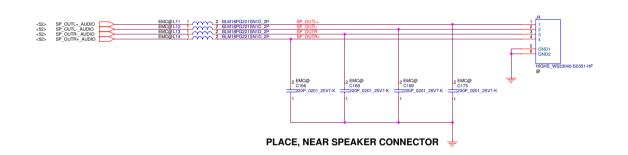




Security Classification LC Future Center Secret Data Title AUDIO EXT MIC UF

Issued Date 2015/11/02 Deciphered Date 2015/13/10

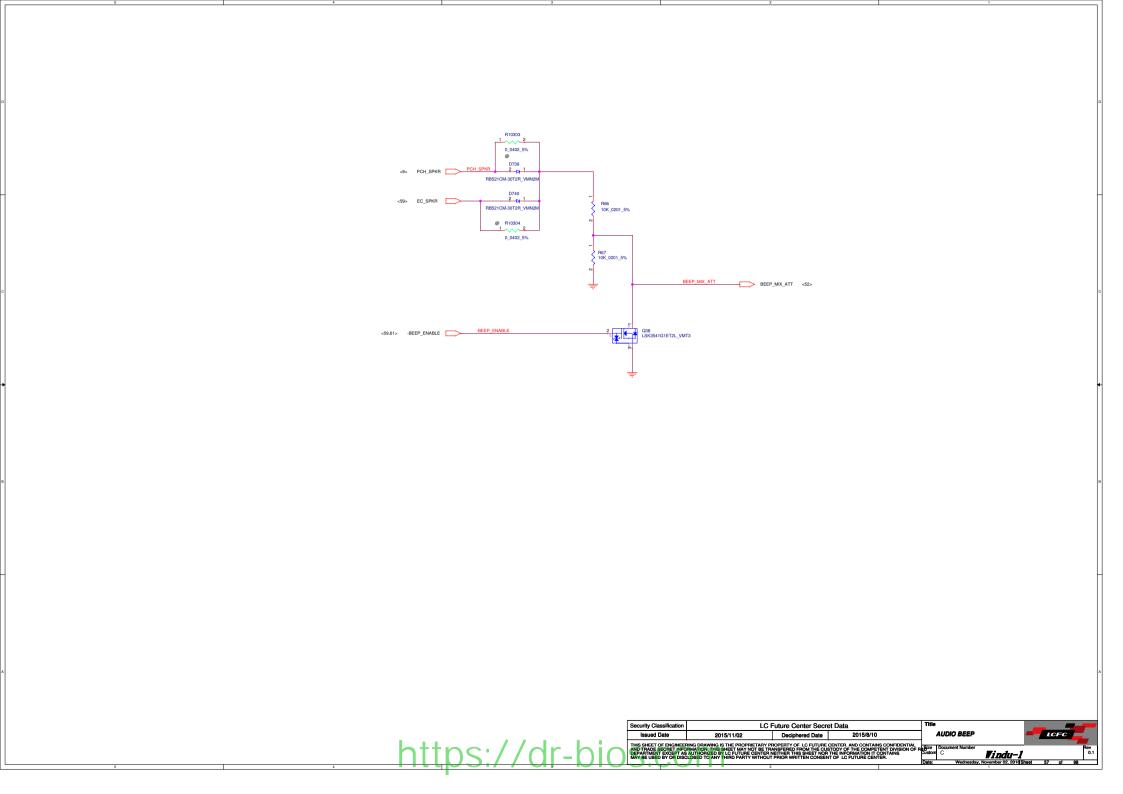
The sweet of environment opportunity property rep to Junius convenient in the sweet of environment opportunity property rep to Junius convenient in the sweet of the opportunity property representation of the sweet post of the convenient in the sweet of the sweet post of the sweet work the increase of the sweet post of the sweet work the increase of the sweet post of the sweet work the increase of the sweet post of the sweet work the increase of the sweet post of the sweet work the increase of the sweet post of the sweet work the increase of the sweet post of the sweet work the increase of the sweet post of the sweet work the increase of the sweet post of the sweet work the increase of the sweet post of the sweet work the increase of the sweet post of the sweet work th

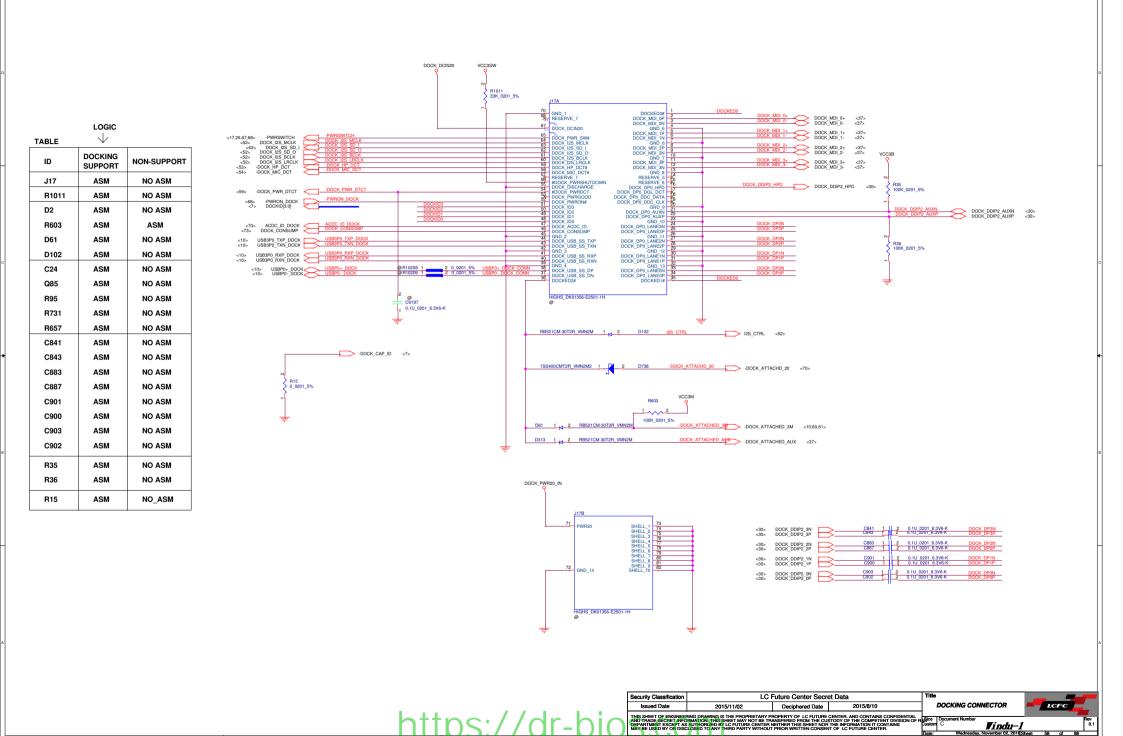


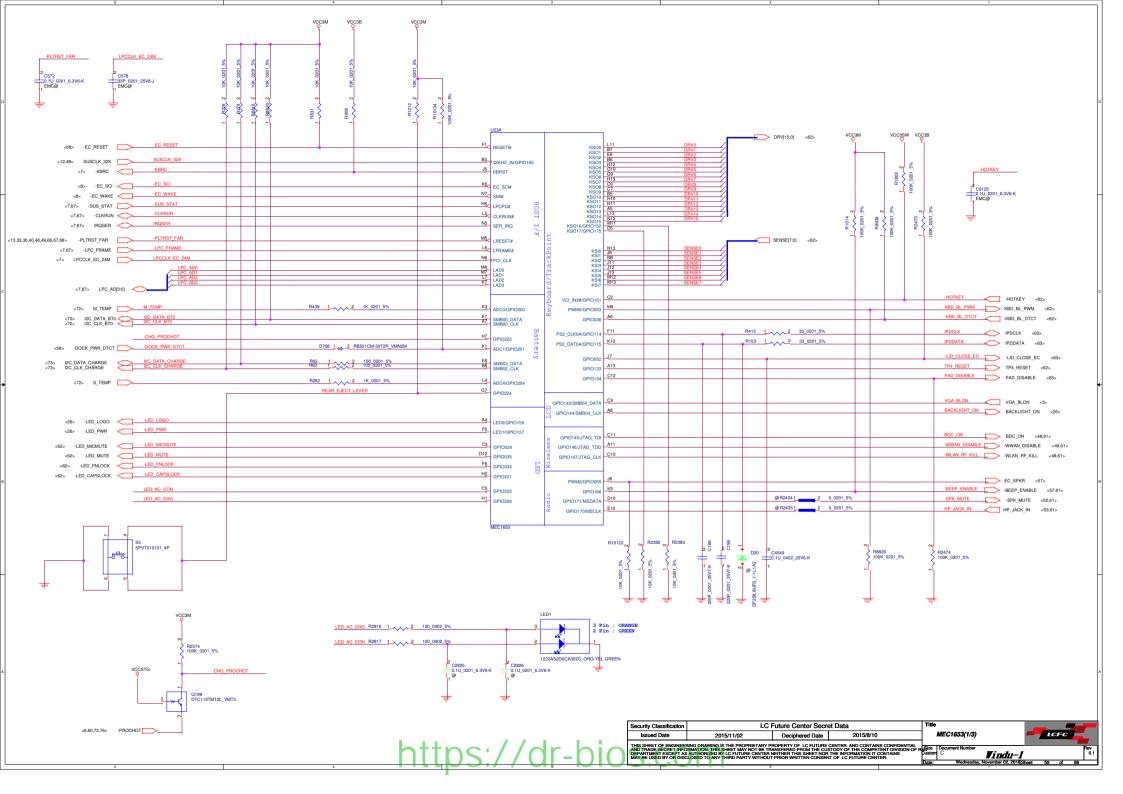
Security Classification LC Future Center Secret Data Title

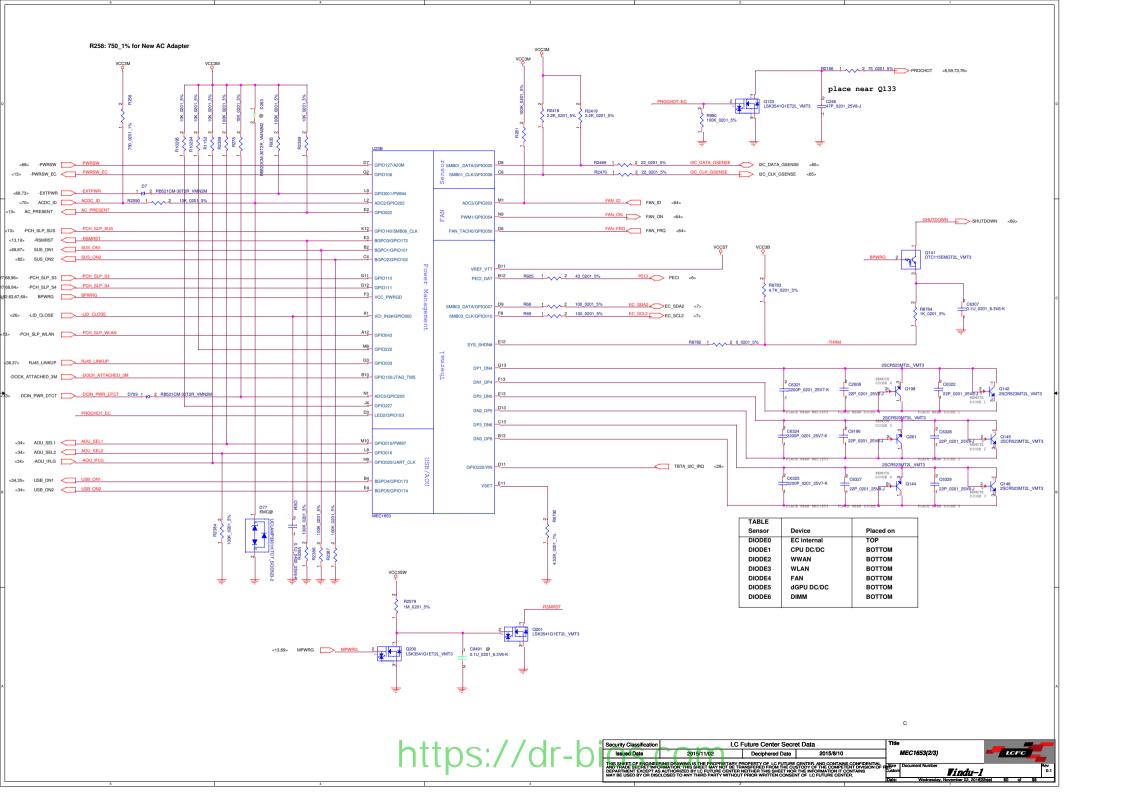
Issued Date 2015/11/02 Deciphered Date 2015/8/10 AUDIO SPEAKER

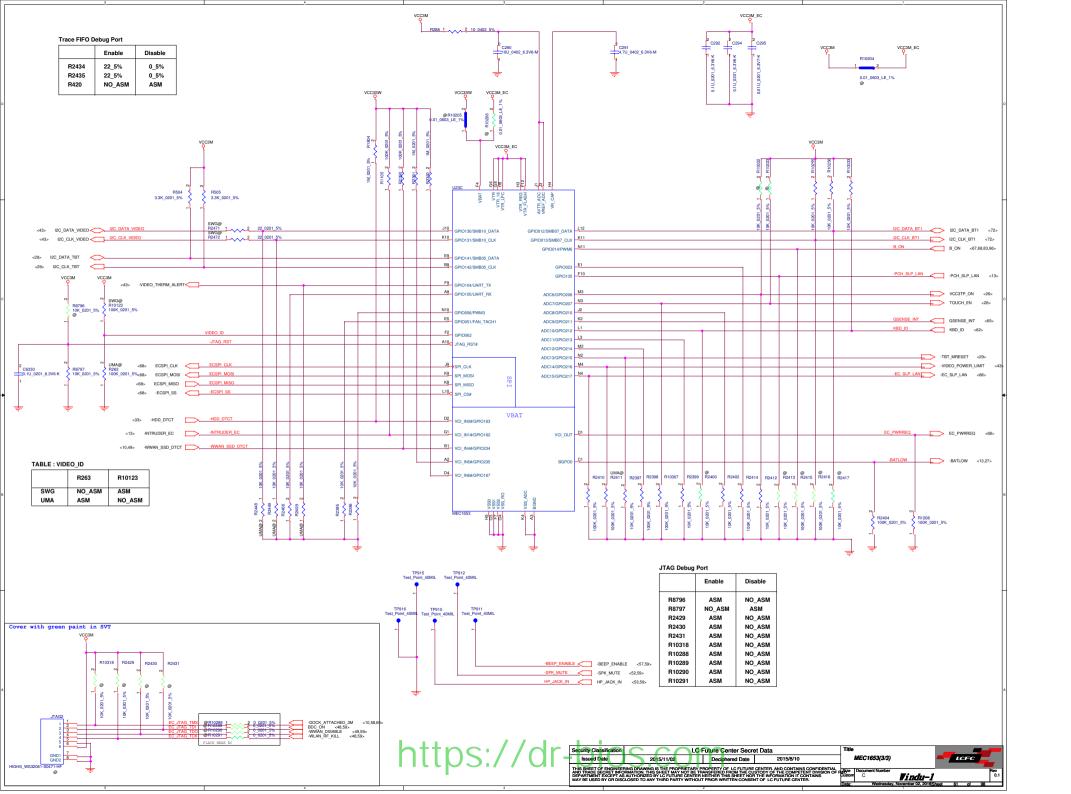
THIS SHEET OF ENGINEERING DRAWING, IS THE PROPRETARY PROPRETARY

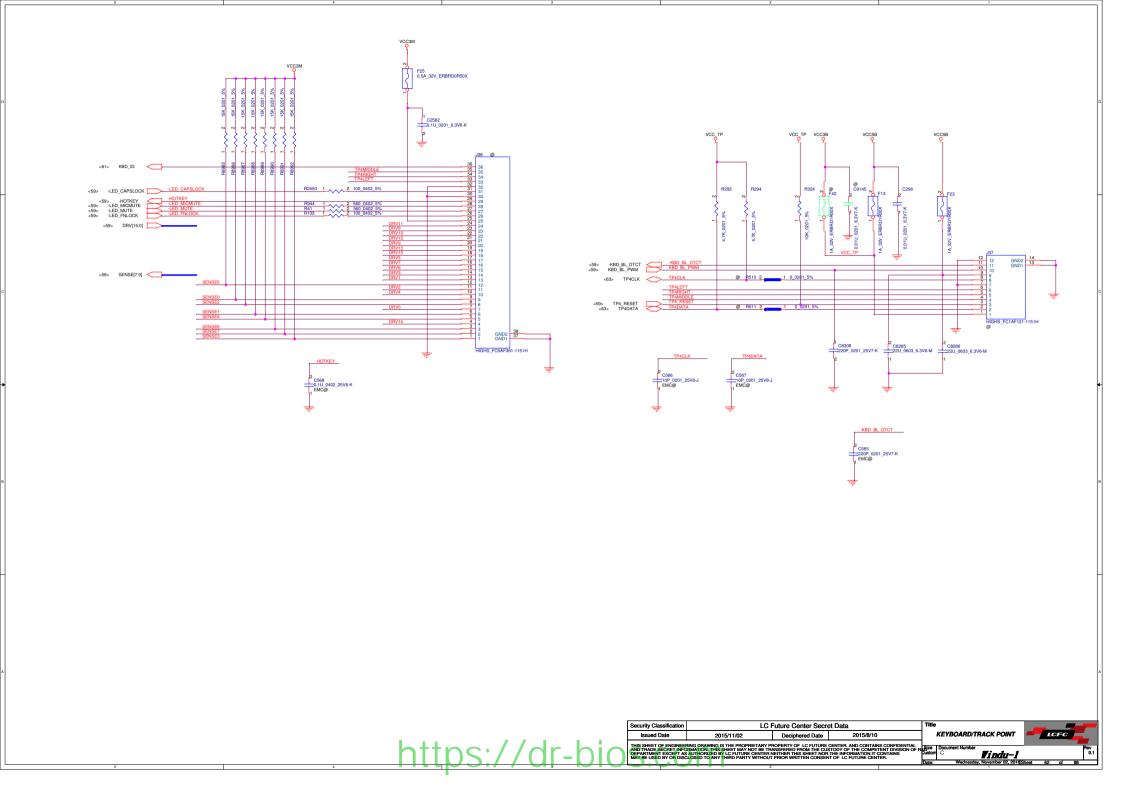


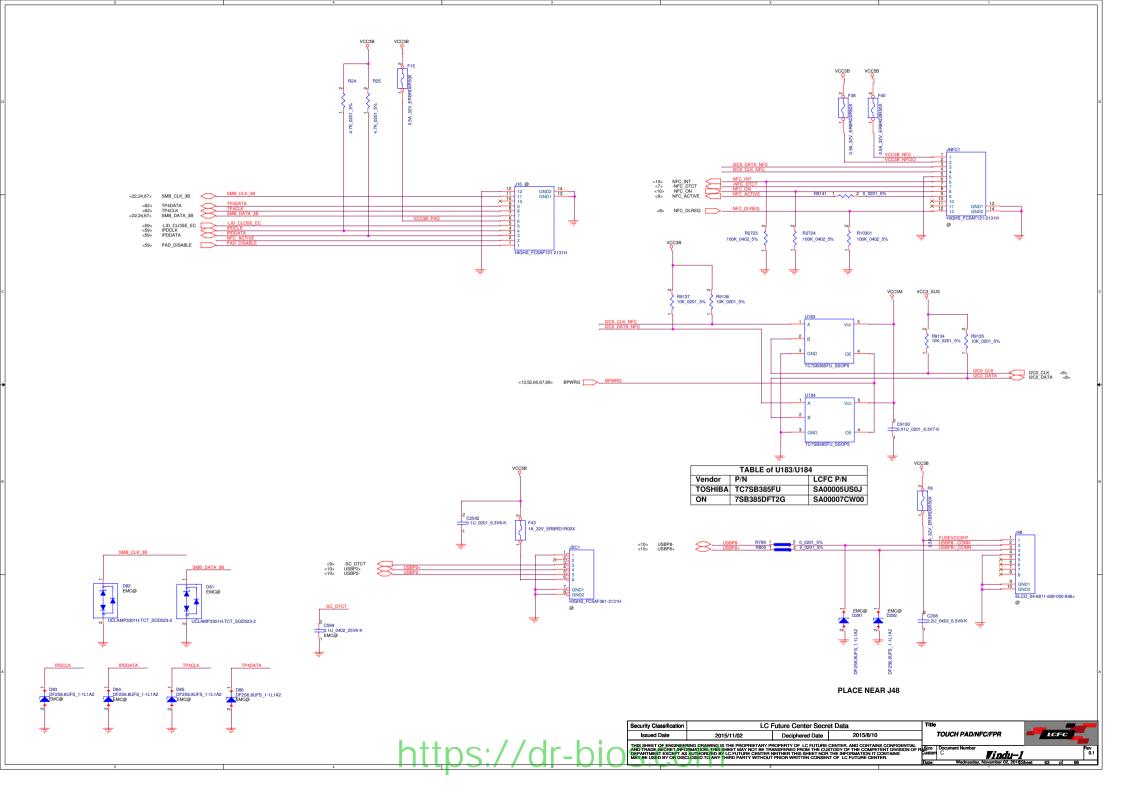


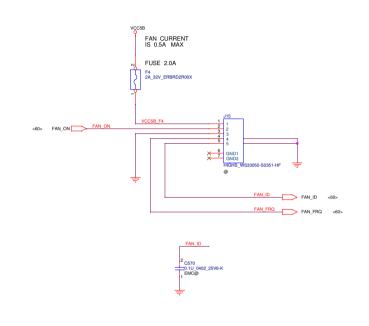








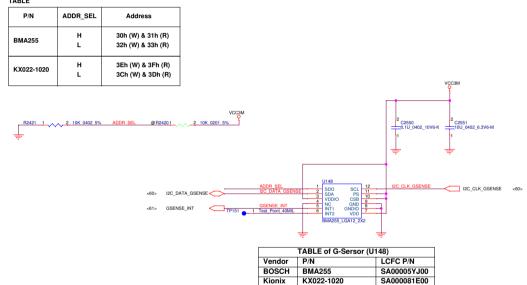


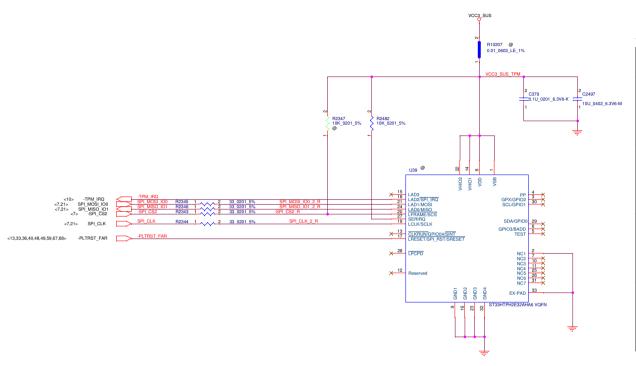


Security Classification LC Future Center Secret Data Title FAN CONNECTOR ISsued Date 2015/11/02 Deciphered Date 2015/11/02 2015/01/10

These secret or enconcernous provinces to the proprietable reproductive control and control of the proprietable reproductive control of the





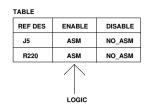


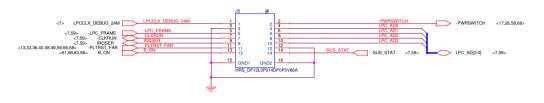
TARLE

ABLE			
	TCG	Infineon	ST Micro
Pin No	PTP Spec (v38)	SLB9670VQ2.0 FW 7.60	ST33HTPH2E32AHA6
		SA000075L20	SA000081F00
1	VDD	VDD	NC
2	GND GPIO	GND NC	GND NC
3 4 5 6	GPIO	NC NC	PP
5	NC	NC	NC
6	VNC/GPIO GPIO/VDD	GPIO PP	NC GPIO
8	VDD	VDD	NC
		155	
9	GND	GND	NC
10	VNC	NC	NC
11 12	NC NC	NC NC	NC NC
13	VNC/GPIO	NC	NC
14	VDD	NC	NC
15 16	NC GND	NC NC	NC NC
.,	GND	NO.	No
17	SPI_RST#	RST#	SPI_RST#
18 19	SPI_PIRQ# SPI_CLK	PIRQ# SCLK	SPI_PIRQ# SPI_CLK
20	SPI_CLK SPI_CS#	CS#	SPI_CLK SPI_CS#
21	MŌSI	MOSI	MŌSI
22	VDD	VDD	VPS
23 24	GND MISO	GND MISO	NC MISO
	mioo	IIII00	
25	NC	NC	NC
26 27	NC NC	NC NC	NC NC
28	NC NC	NC NC	NC NC
29	VNC/GPIO	NC	NC
30	VNC/GPIO	NC	NC
31 32	VNC GND	NC GND	NC NC
			1









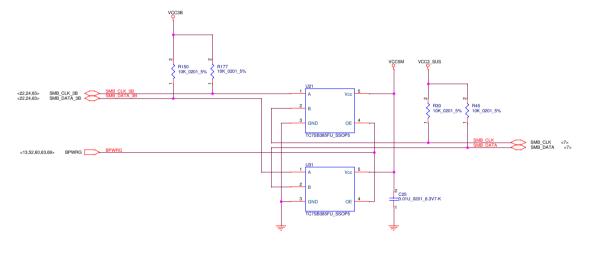


	TABLE of U21/U31				
Vendor	P/N	LCFC P/N			
TOSHIBA	TC7SB385FU	SA00005US0J			
ON	7SB385DFT2G	SA00007CW00			

https://dr-bio

Security Classification

LC Future Center Secret Data

Issued Date

2015/11/02

Deciphered Date

2015/8/10

THIS SHEET OF ENDINEEDING DRAWING IS THE PROPRIETARY PROPRETY OF LC FUTURE CENTER, AND CONTRANS CONFIDENTIAL AND TRANS CENTER AND CONTRANS CONFIDENTIAL AND TRANS CENTER AND TRANS AND TRANSCE AND

Title

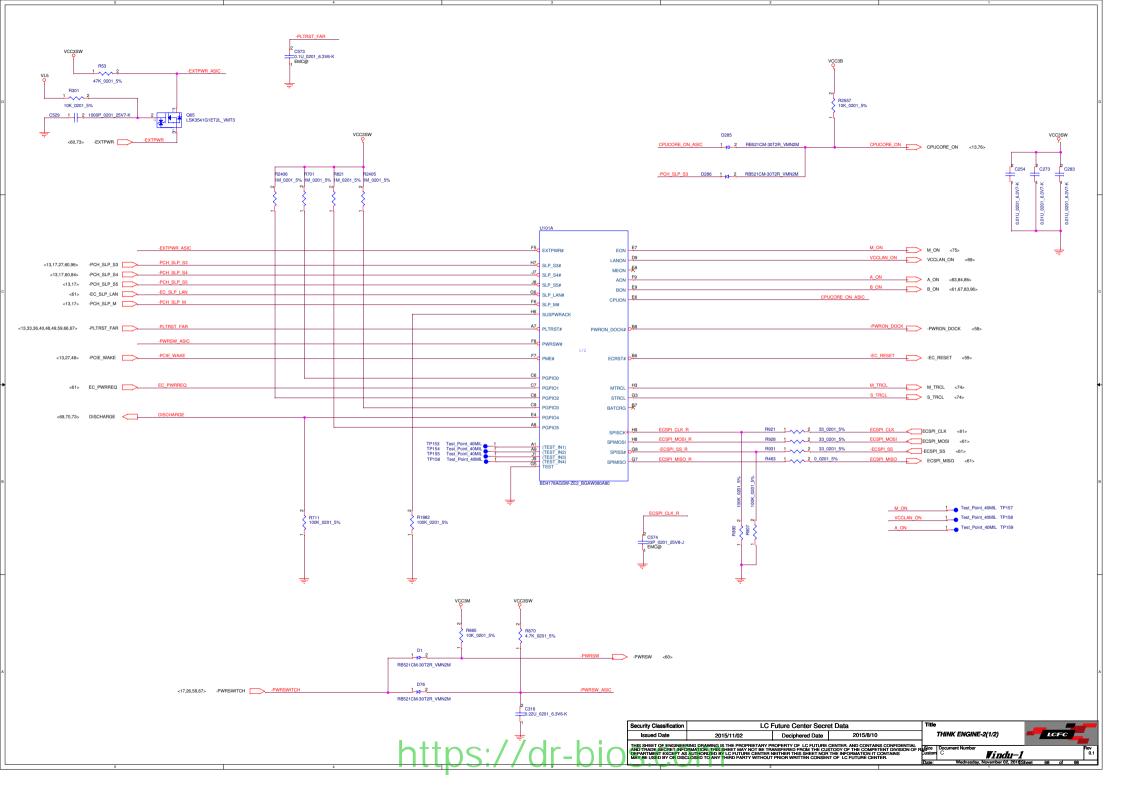
SMBUS SWITCH/LPC DEBUG PORTE

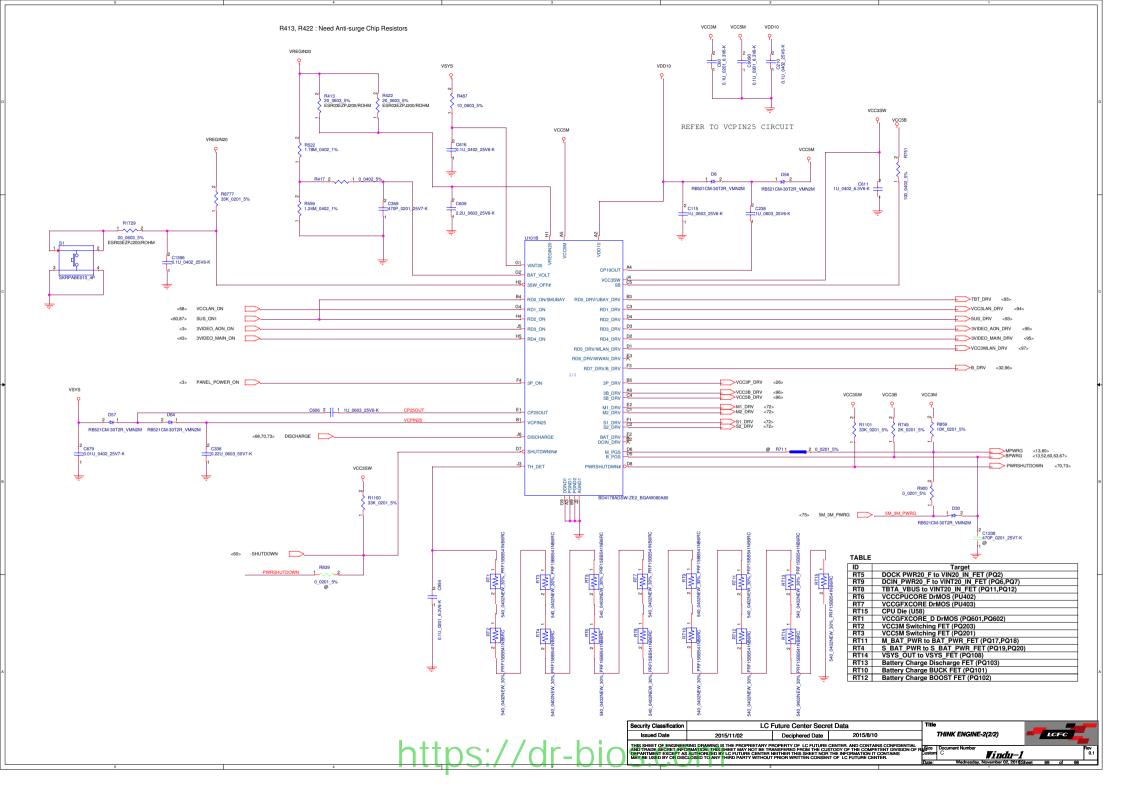
Desire

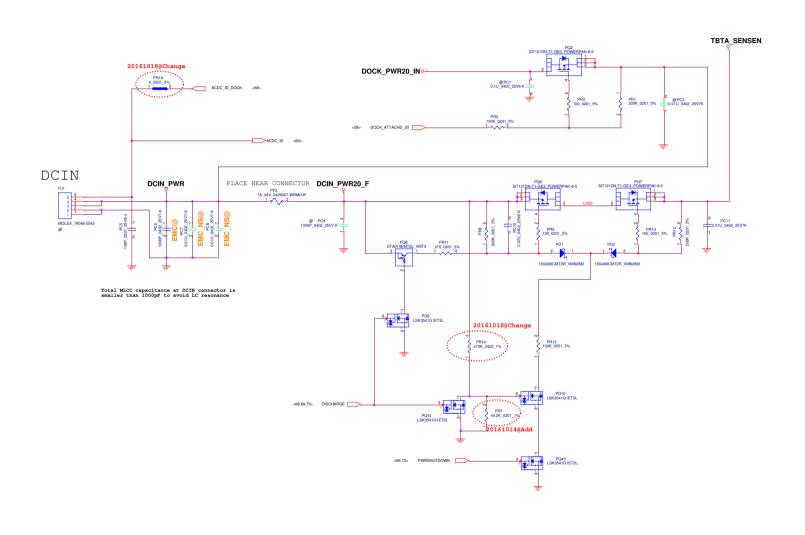
C

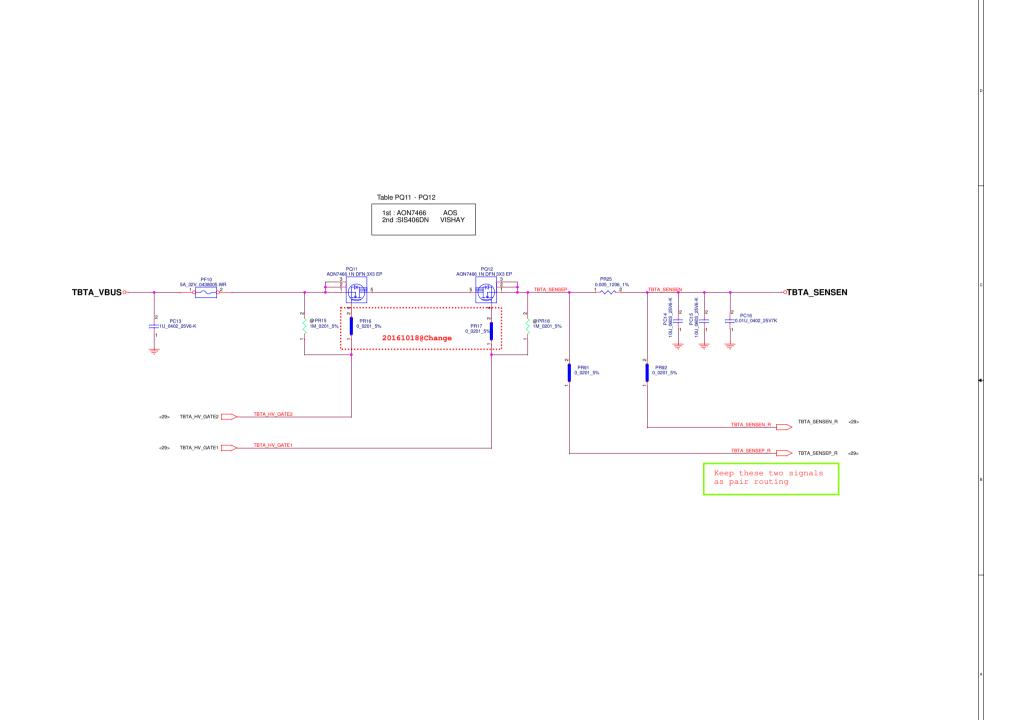
Direct

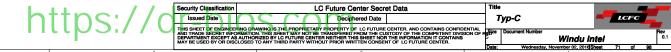
Wednesday, November 02, 2018 Speet 67 of 58

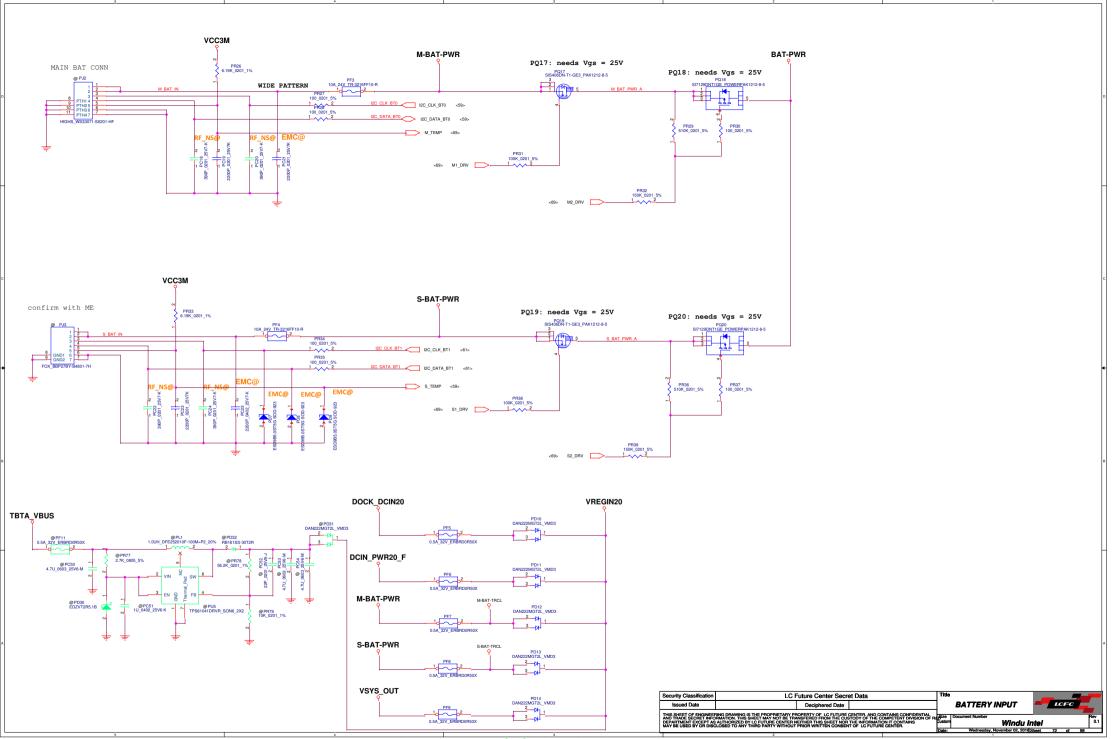




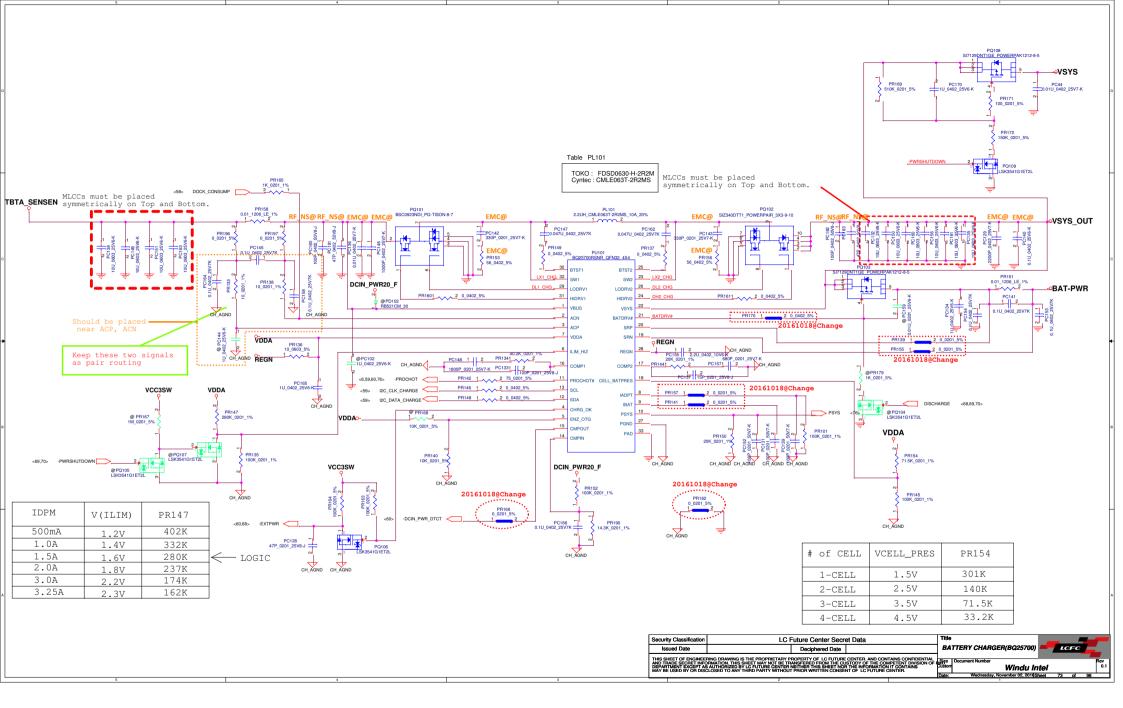




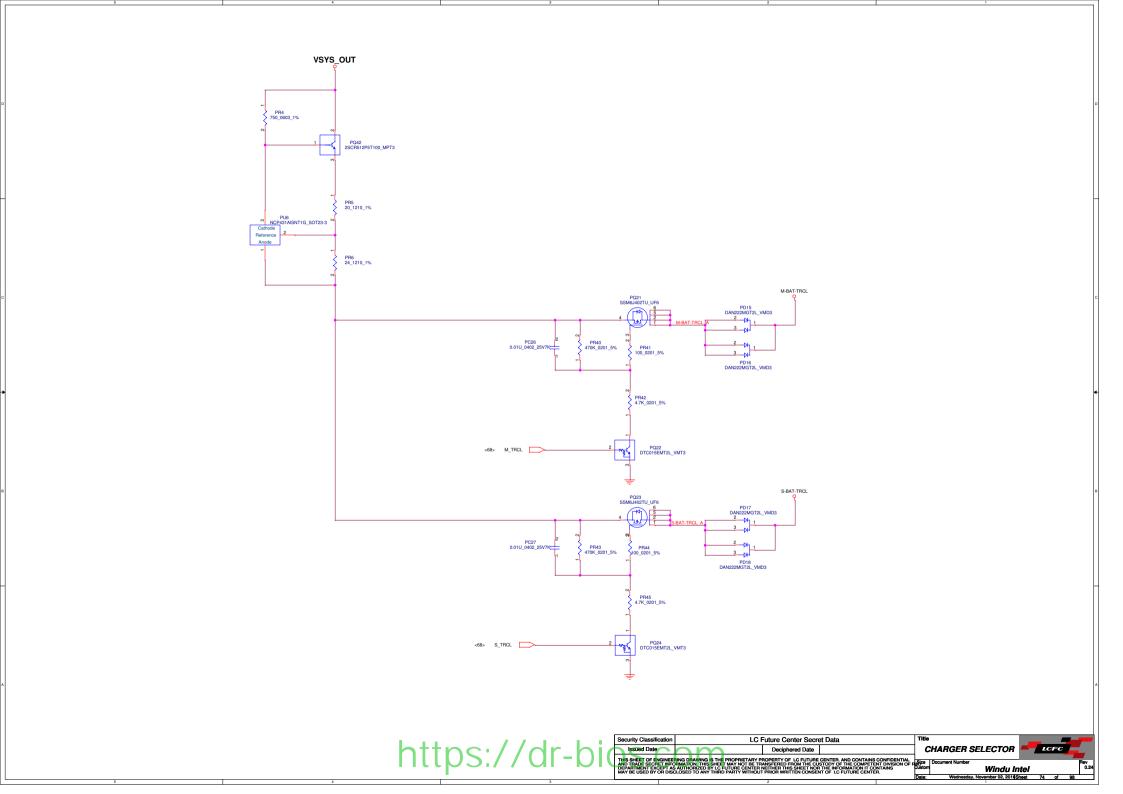


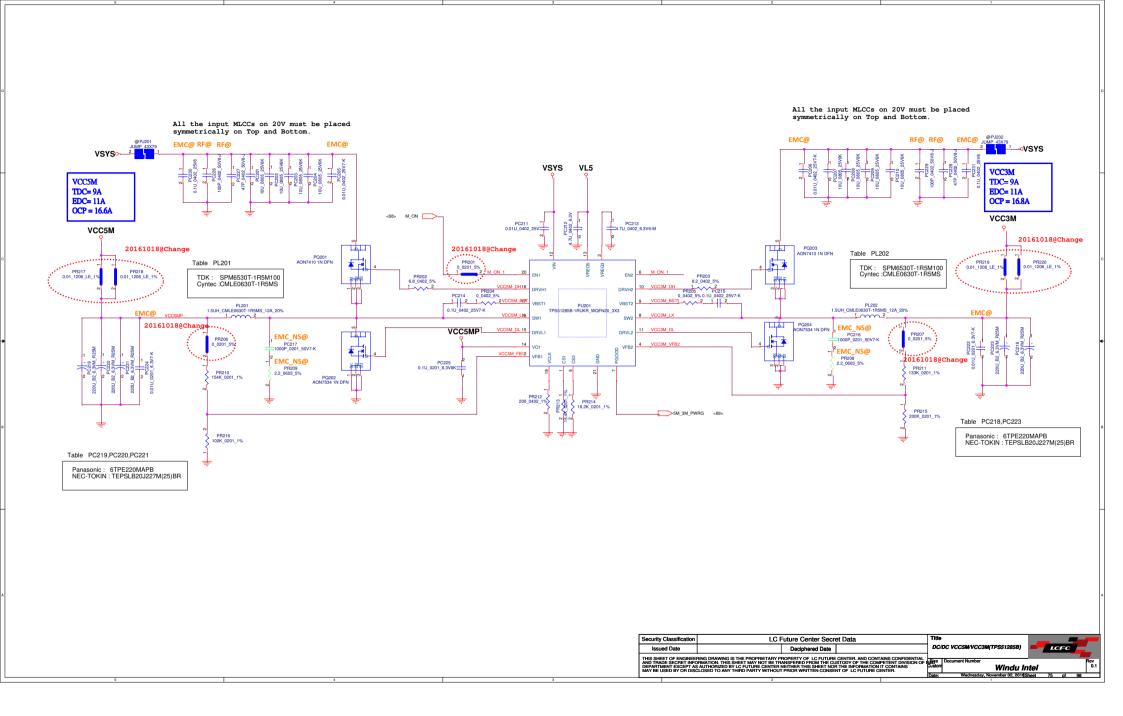


https://dr-bios.com

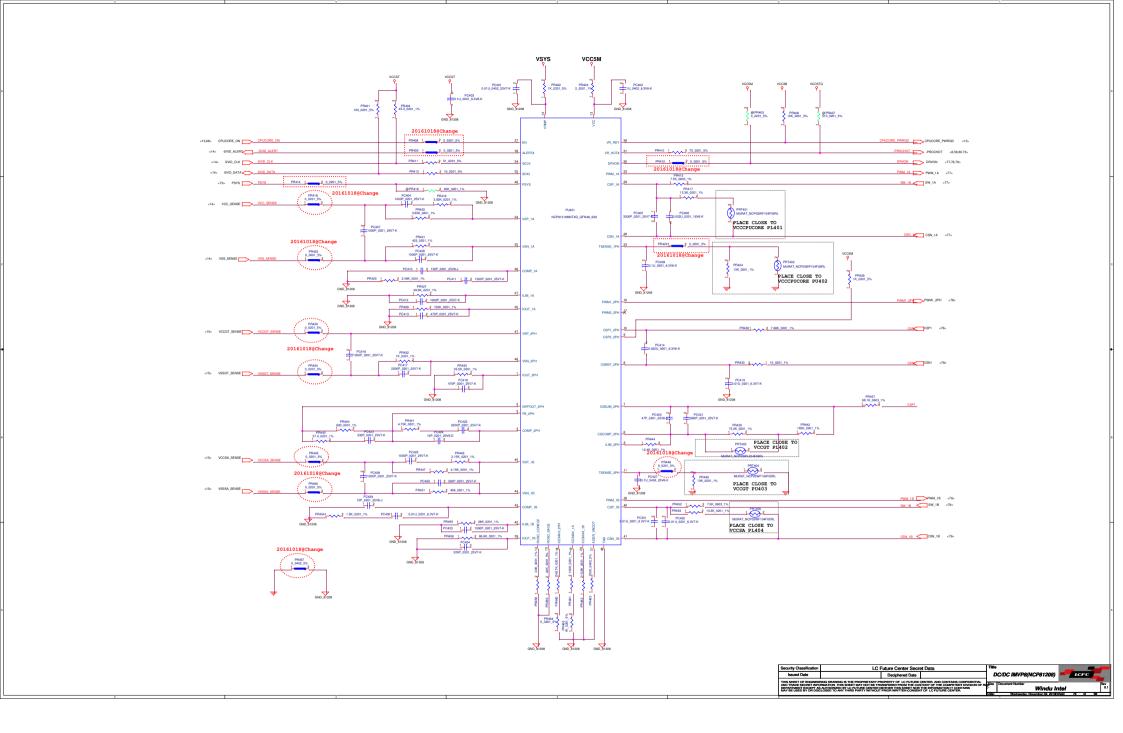


https://dr-bios.com

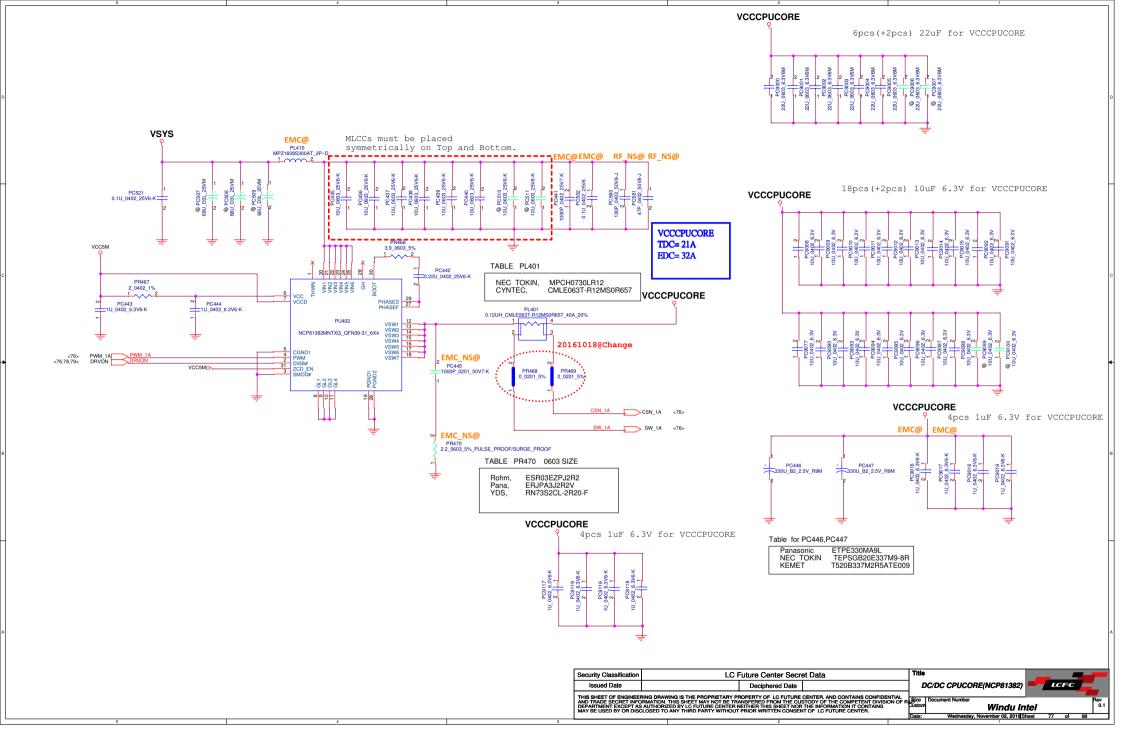




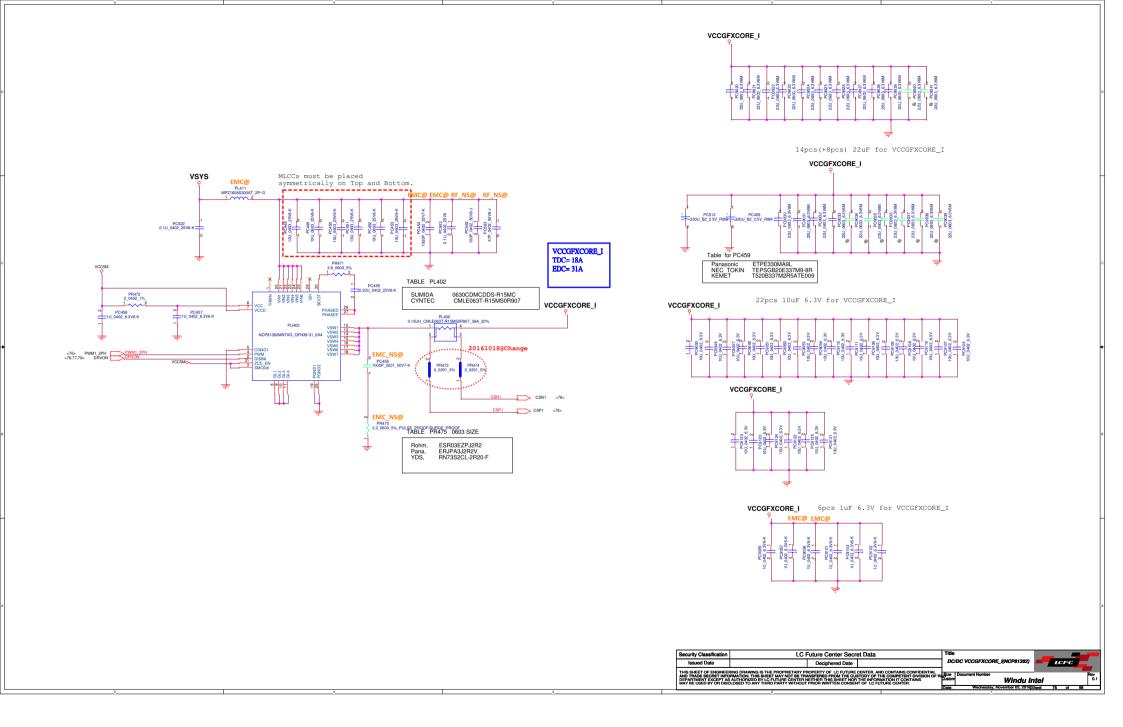
https://dr-bios.com

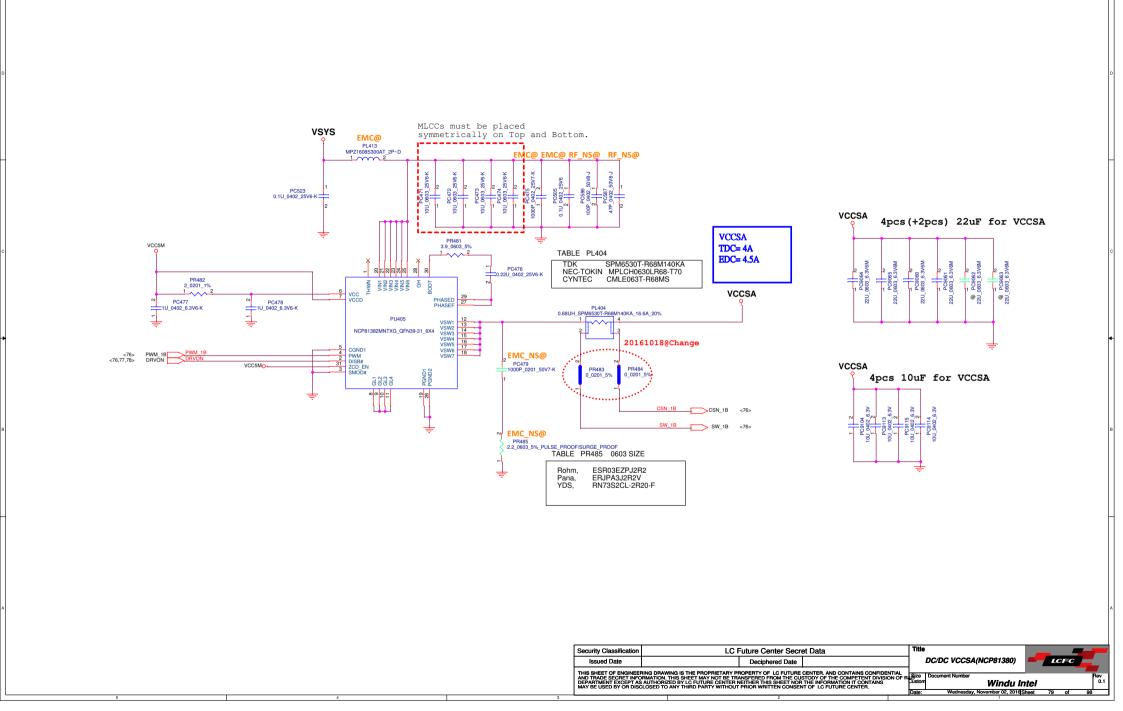


https://dr-bios.com



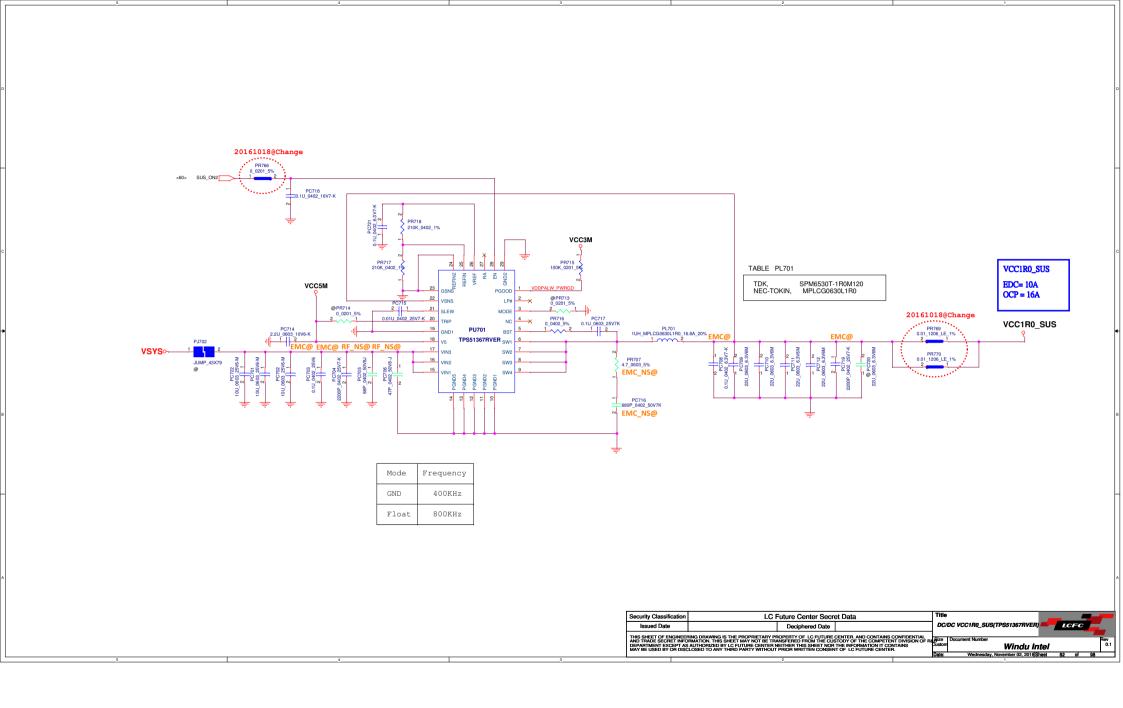
https://dr-bios.com

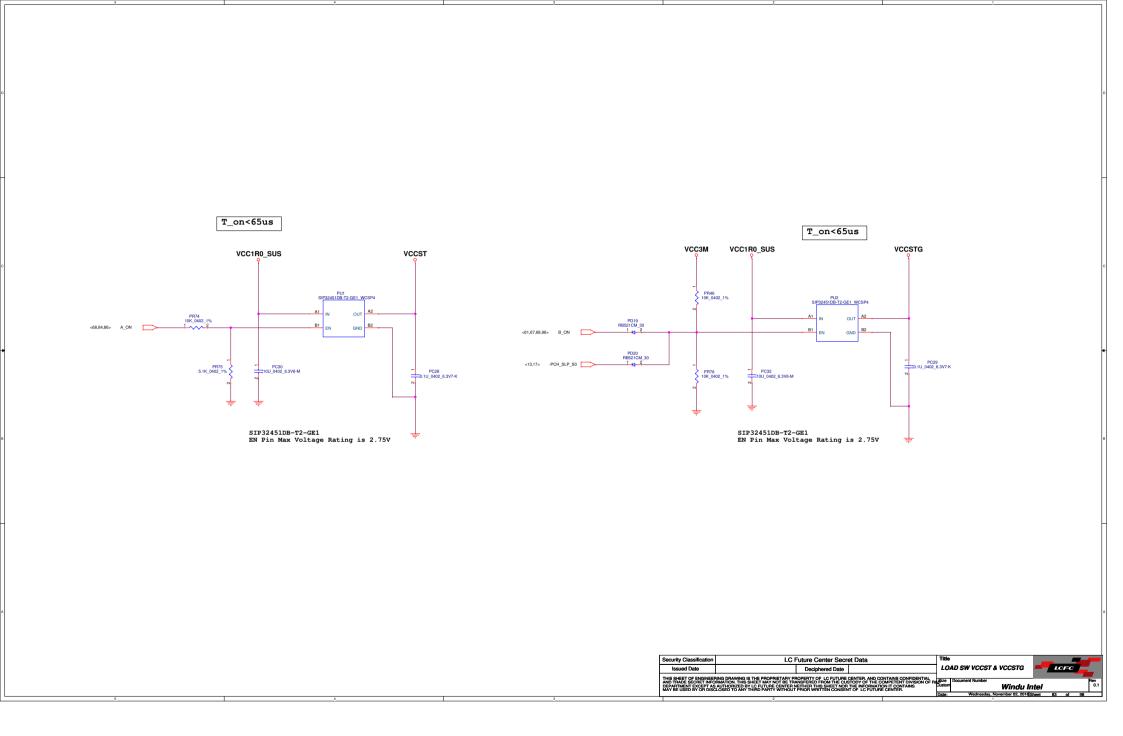


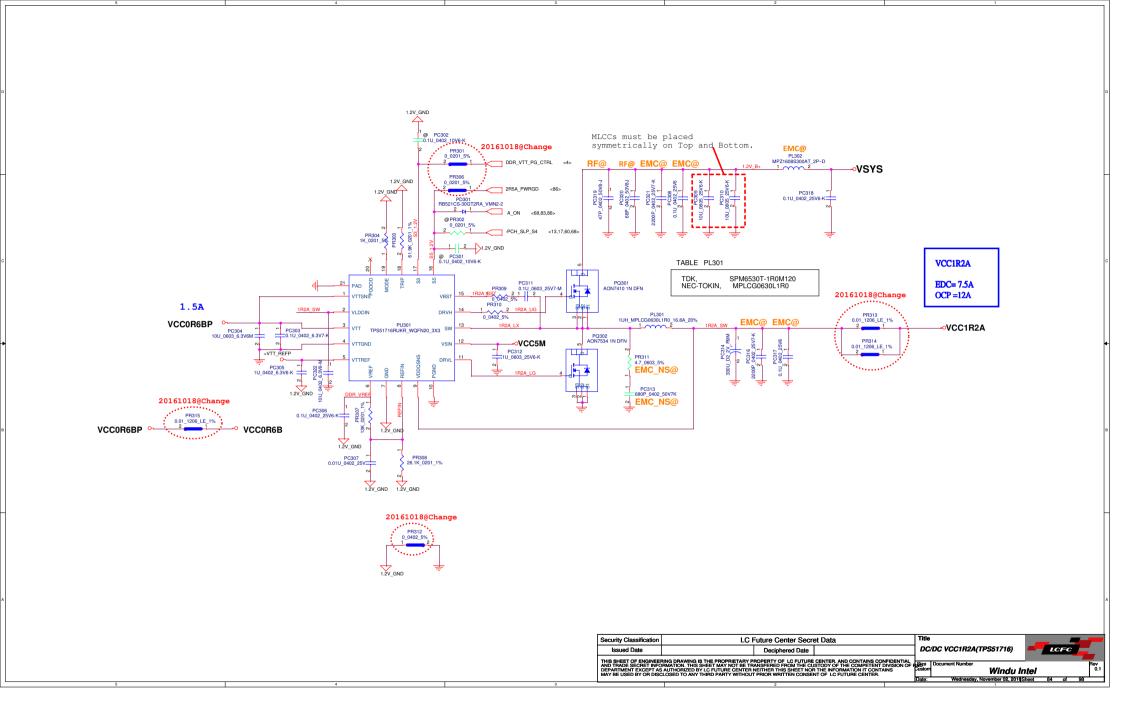


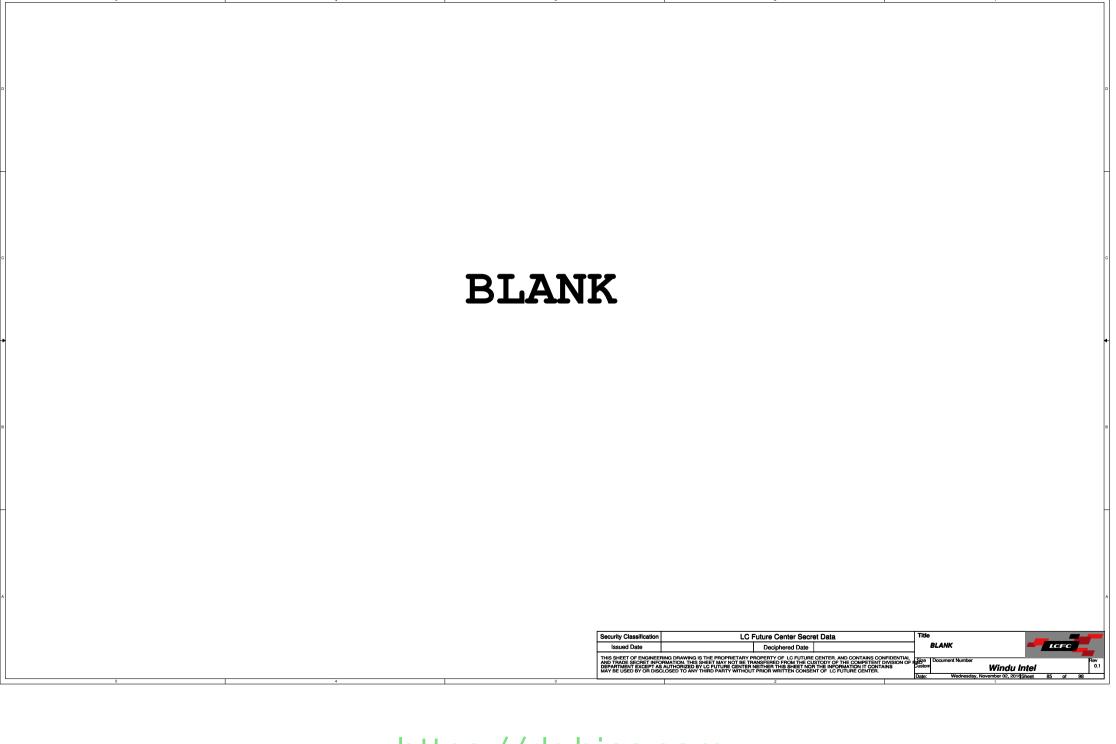


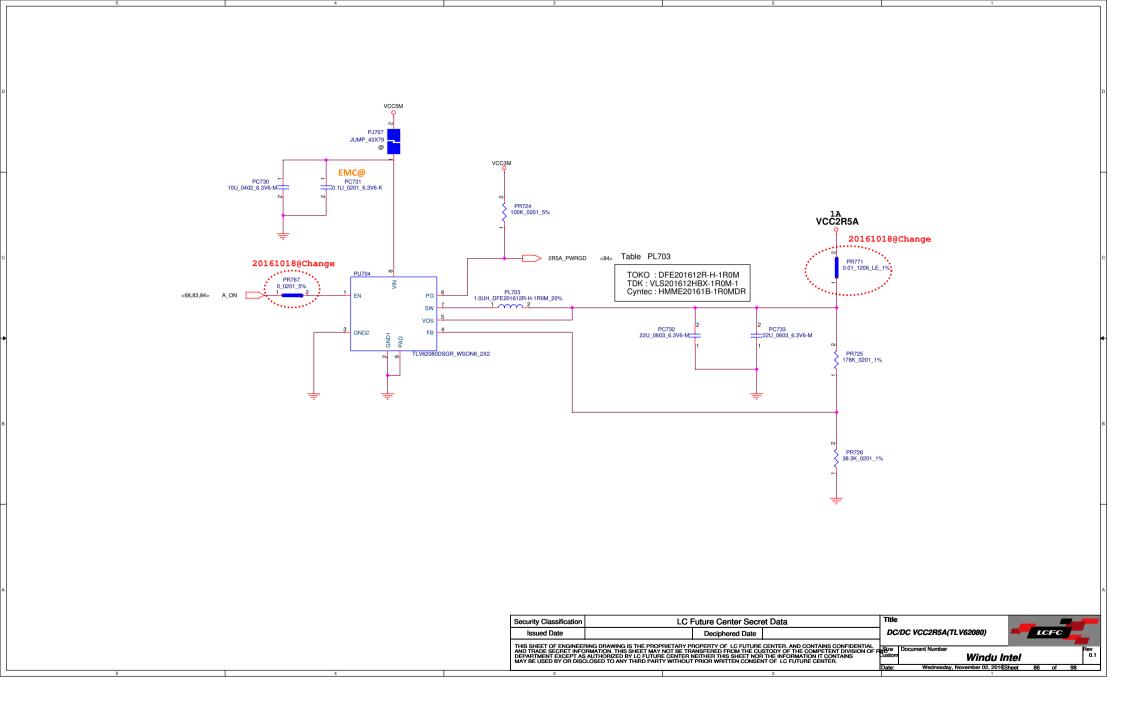


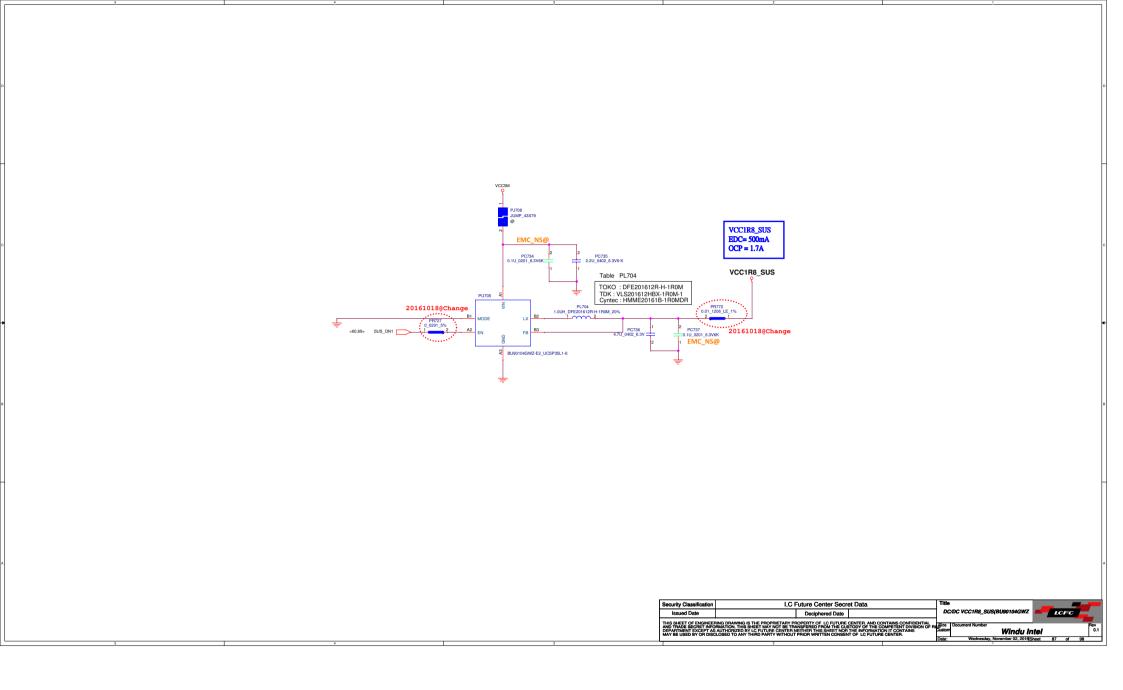












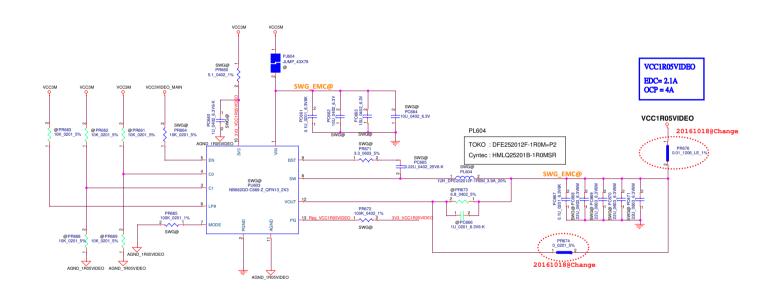


TABLE: NB682 MODE M3 (100K)

LP#	C1	C0	VOUT	
0	х	х	ov	
1	0	0	0.8V	
1	0	1	0.95V	
1	1	0	1V	
1	1	1	1.05V	



https://dr-bio

			LC Future Center Secret Data				
Issued Date	\overline{r}			Deciphered Date		[E	
THIS SHEET OF ENGINEERIN	NG DRAWING IS T	HE PRO	PRIETARY PR	ROPERTY OF LC FUTURE	CENTER, AND CONTAINS CONFIDENTIAL STODY OF THE COMPETENT DIVISION OF RE	Size	

Itle
DC/DC VCC1R05VIDEO(NB682)

TO Document Number

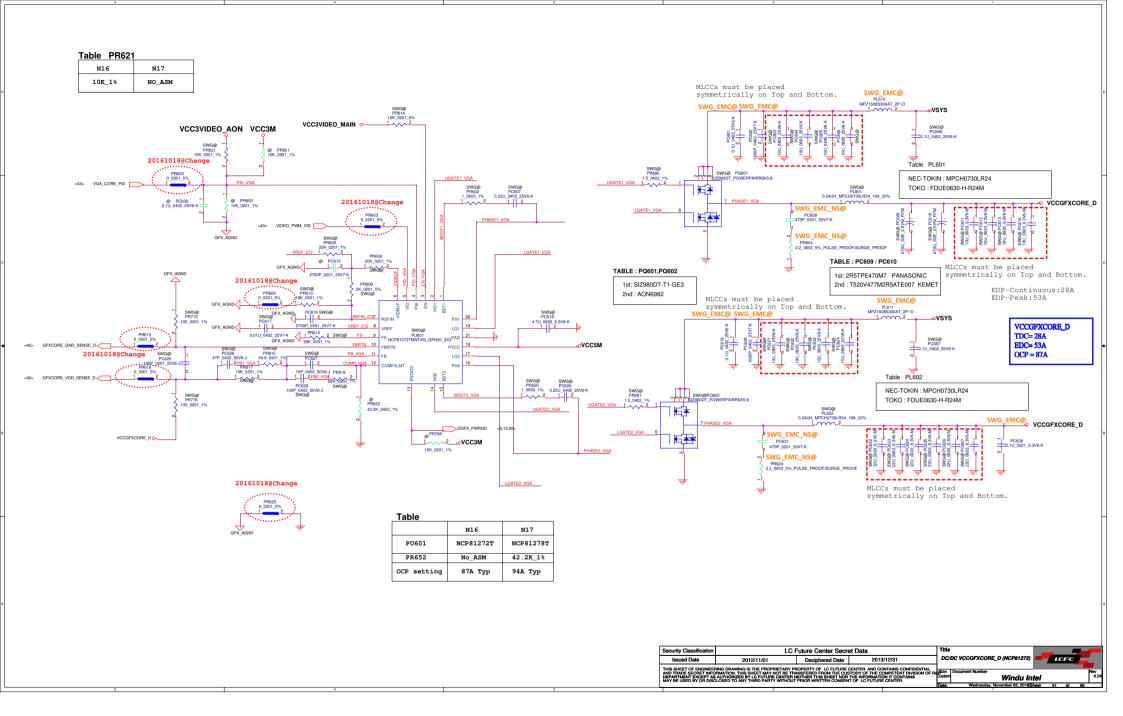
Windu Intel

Wednesday, Numerior 02, 2014 Shoet 88 of 88

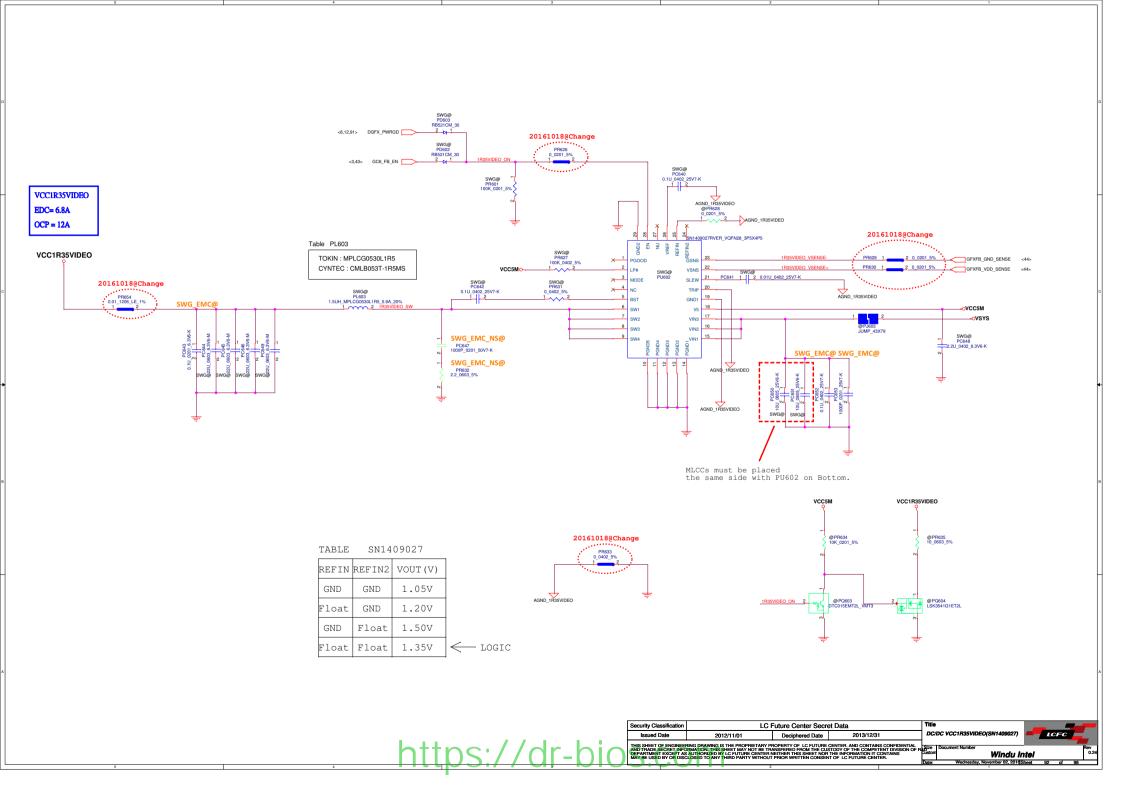
BLANK

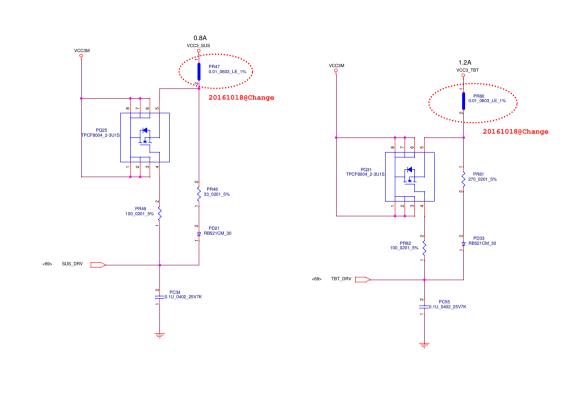
BLANK

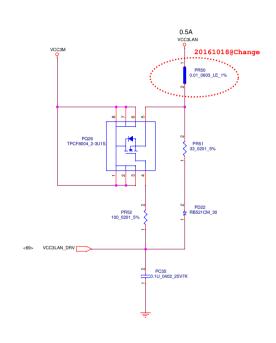
Security Classification LC Future Center Secret Data Title
| Issued Date | 2012/11/01 | Deciphered Date | 2013/12/31 |
| This SHEET OF ENINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFEDENTIAL PROPERTY OF LC FUTURE CENTER AND CONTAINS CONTAINS CONFEDENTIAL PROPERTY OF LC FUTURE CENTER AND CONTAINS CONTA



https://dr-bios.com







Security Classification LC Future Center Secret Data

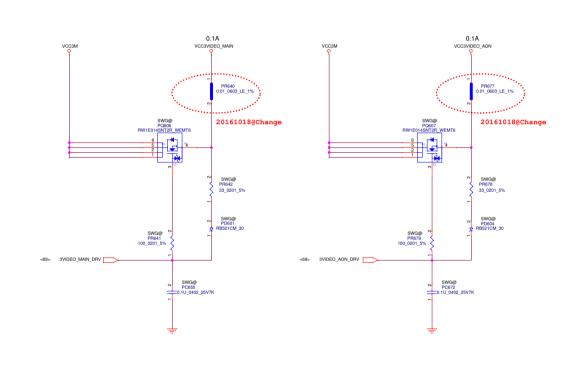
Title

LOAD SW LAN

Title

LOAD SW LAN

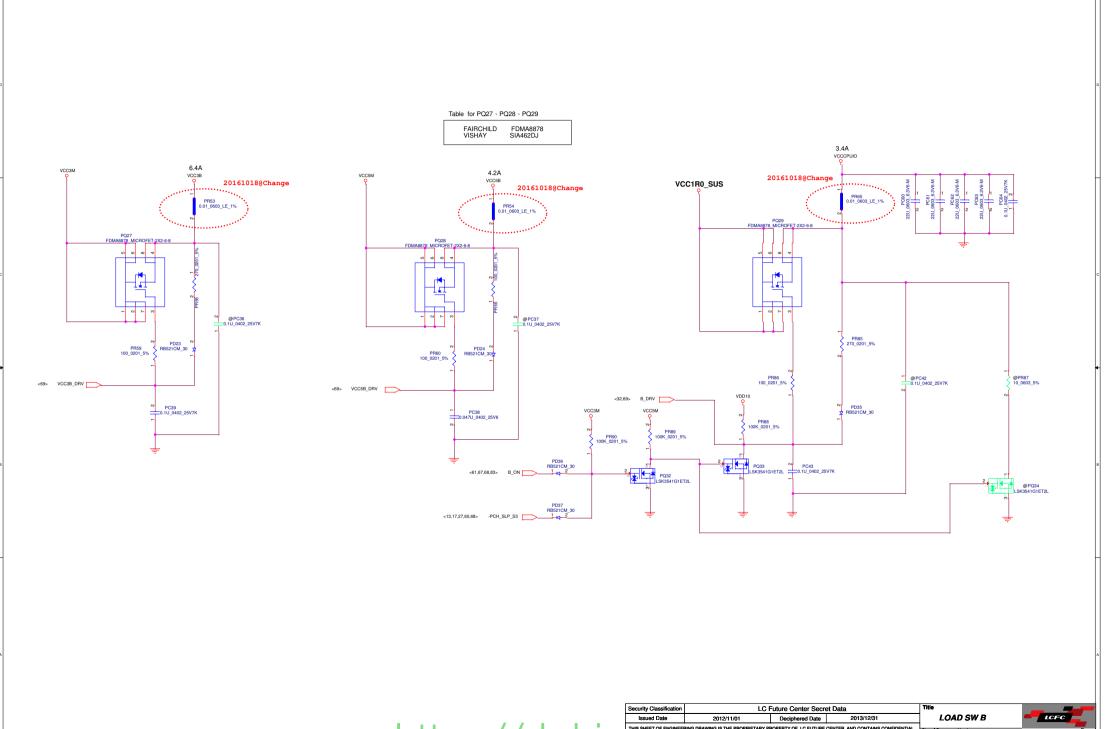
LO



Security Classification L.C. Future Center Secret Data

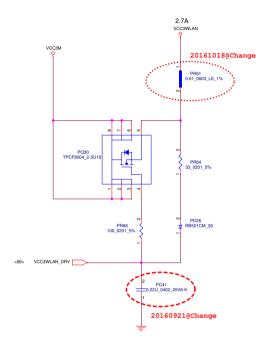
Issued Date 2012/11/01 Deciphered Date 2013/12/31

The secret of the part of the p



THE SHEET OF DIGNESSIND DEWINN IS THE PROPRIETARY PROPERTY OF LIE TUTTURE CURTURE, AND CONTAINS CONTRIBUTION, MICH TRADES STORM FROM MADE THE SHEET THE YOUR THE TRADES FROM THE CURTORY OF THE COMPETENT MADE NO DEPARTMENT EXCEPT AS JUTHORIZED BY LIC PUTURE CENTER HERHER THIS SHEET NOT THE INFORMATION IT CONTAINS WAYE USED BY OOI DISCUSSED TO ANY PHIRD PARTY WINDOUT PRIOR WITTHEN CONSENT OF LE FUTURE CENTER.

Windu Intel
mesday, November 02, 2016 Sheet 96



TABLE

AOAC	YES	NO
PR70	NO-ASM	ASM
PQ35	ASM	NO-ASM
PR72	ASM	NO-ASM
PR74	ASM	NO-ASM
PC40	ASM	NO-ASM
PD23	ASM	NO-ASM



LOGIC

	Security Classification	LCI	Future Center Secre	et Data	Title	
	Issued Date	2012/11/01	Deciphered Date	2013/12/31	LOAD SW WWAN & WLAN	LCFC
ttps://dr-bio	AND TRADE SECRET INFO	RING DRAWING IS THE PROPRIETARY PIRMATION: THIS SHEET MAY NOT BE TRAIN AUTHORIZED BY LC FUTURE CENTER IN LOSED TO ANY THIRD PARTY WITHOUT	ANSFERED FROM THE CU:	STODY OF THE COMPETENT DIV	VISION OF RABIZE DOCUMENT NUMBER	Rev 0.24 97 of 98
			2		1	

