

U10D

VSS5 VSS6

VSS1

VSS1

VSS14 VSS15 VSS16 VSS17

VSS18 VSS18

VSS21 VSS22 AB3 AB5 AB7 AB9 AB11

VSS31 VSS32

VSS33 VSS34

VSS35 VSS36

VSS38 VSS39

VSS40 VSS41

VSS42 VSS43

VSS55 VSS56

VSS57 VSS58 AE18 VSS58 VSS59 VSS60 VSS61

VSS60 VSS61

VSS61

VSS63 VSS64 VSS65

VSS68 VSS69

VSS79 VSS80

VSS87

VSS90 VSS91

VSS94 VSS95

AD1 VSS43 AD4 VSS44 AD7 VSS45 AD9 VSS46 AD11 VSS47 AD15 VSS48 AD15 VSS48 AD15 VSS51 AD25 VSS51 AD25 VSS53 AE3 VSS54

AE6 AE8 AE10 AE12

AE20 AE23 AE26 AF2

AF5 AF9 VSS66 VSS67

AF11 AF13

AF15 AF15 VSS69 VSS70 VSS71 VSS71 VSS72 VSS72

AF19 VSS72
AF21 VSS73
AF24 VSS74
B3 VSS75
B6 VSS76
B9 VSS77
B12 VSS78
B16 VSS78

B19 VSS80 B22 VSS81 B25 VSS82 C1 VSS83 C4 VSS84 C7 VSS85 C10 VSS86 C13 VSS87

C15 VSS88 VSS89 VSS89

D2 VSS92 D5 VSS93

C21 C24

D7

D9 D11 VSS96 Dothan 478F

B16 B19

A2 VSS0

A5 A8 VSS1 VSS2

A11 A11 VSS3 A14 VSS4

A17

A20

A23 A26 AA1 AA4 VSS7 VSS8 VSS9 VSS10

AA4
AA6
AA10
AA12
AA16
AA18
AA20
AA22

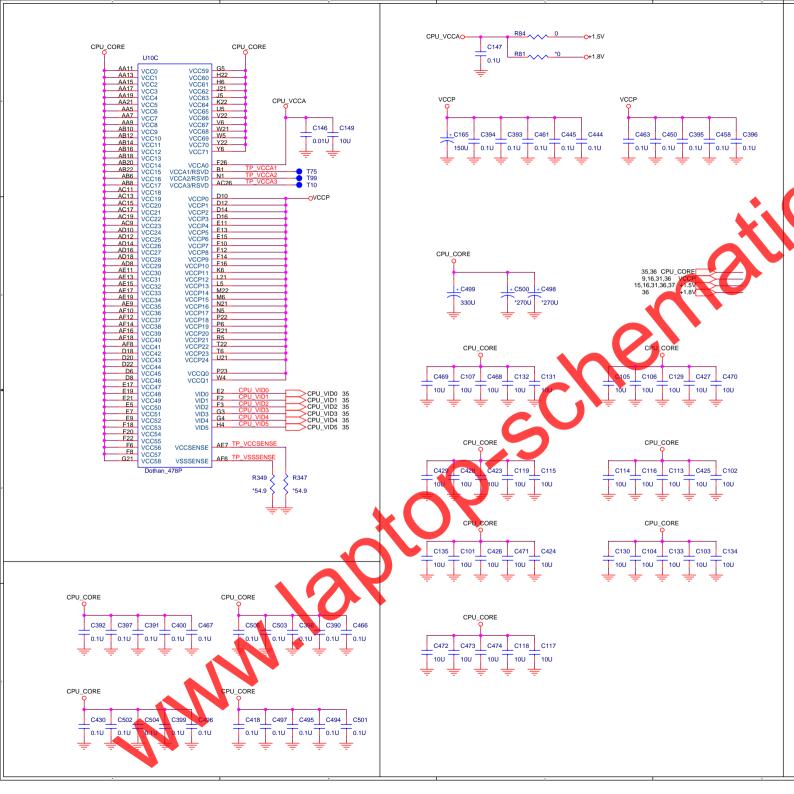
AA25

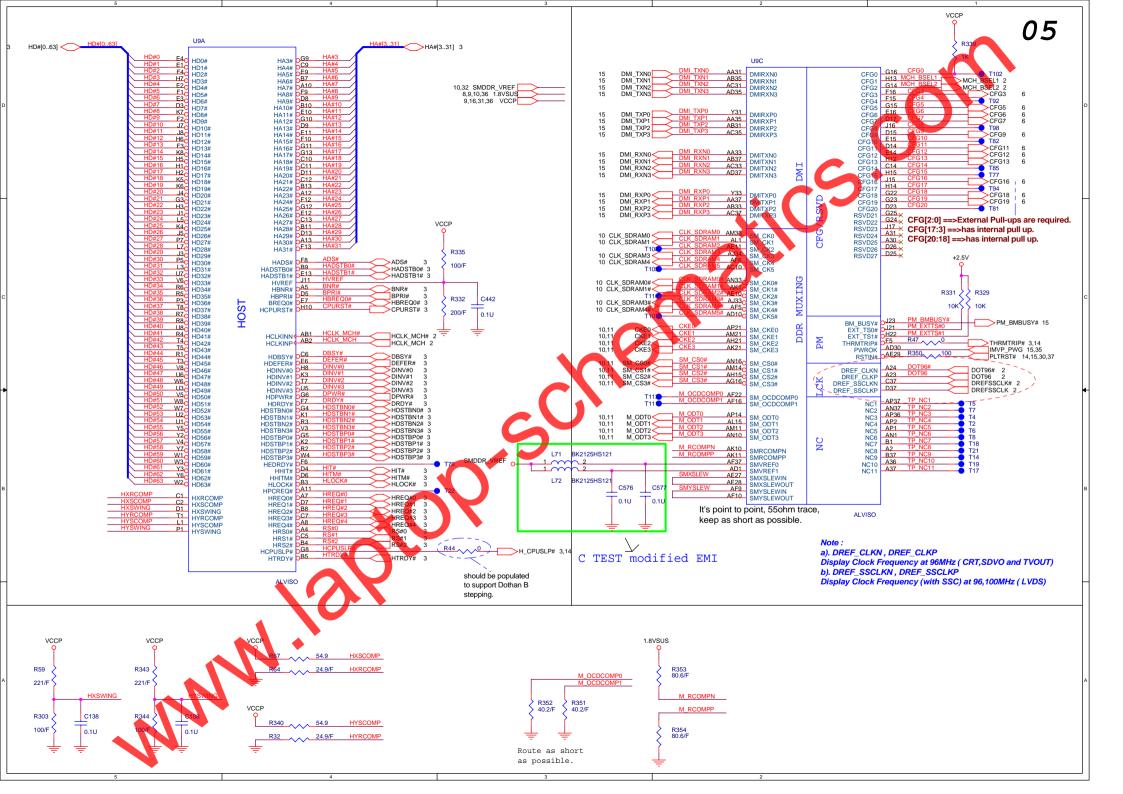
AR3

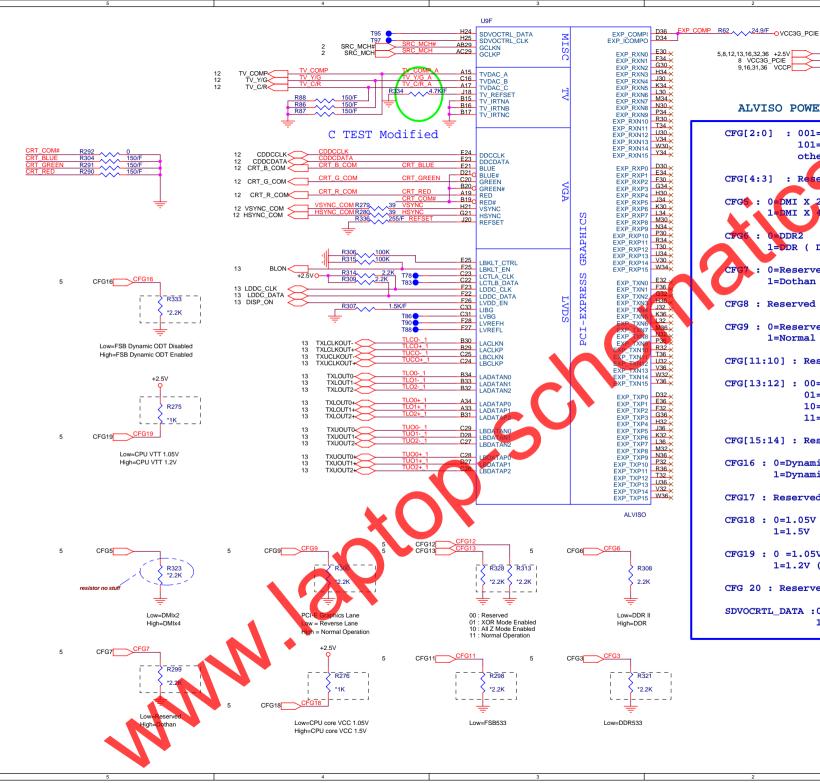
AB19 AB21 AB23 AB26

AB26 AC2 AC5 AC8 AC10 AC12 AC14 AC16 AC18 AC21 AC24 AD1

AB9 VSS22 AB9 VSS23 AB11 VSS25 AB15 VSS26 AB17 VSS27 AB19 VSS29 AB21 VSS29 AB21 VSS29



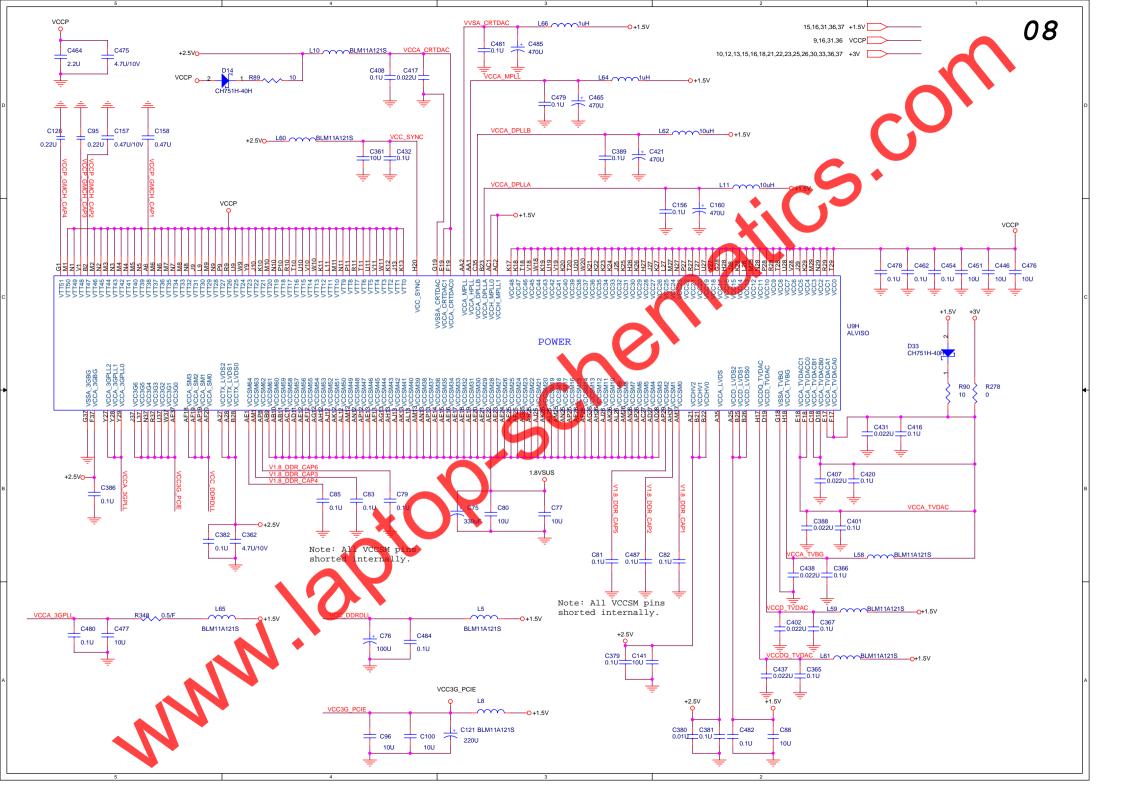


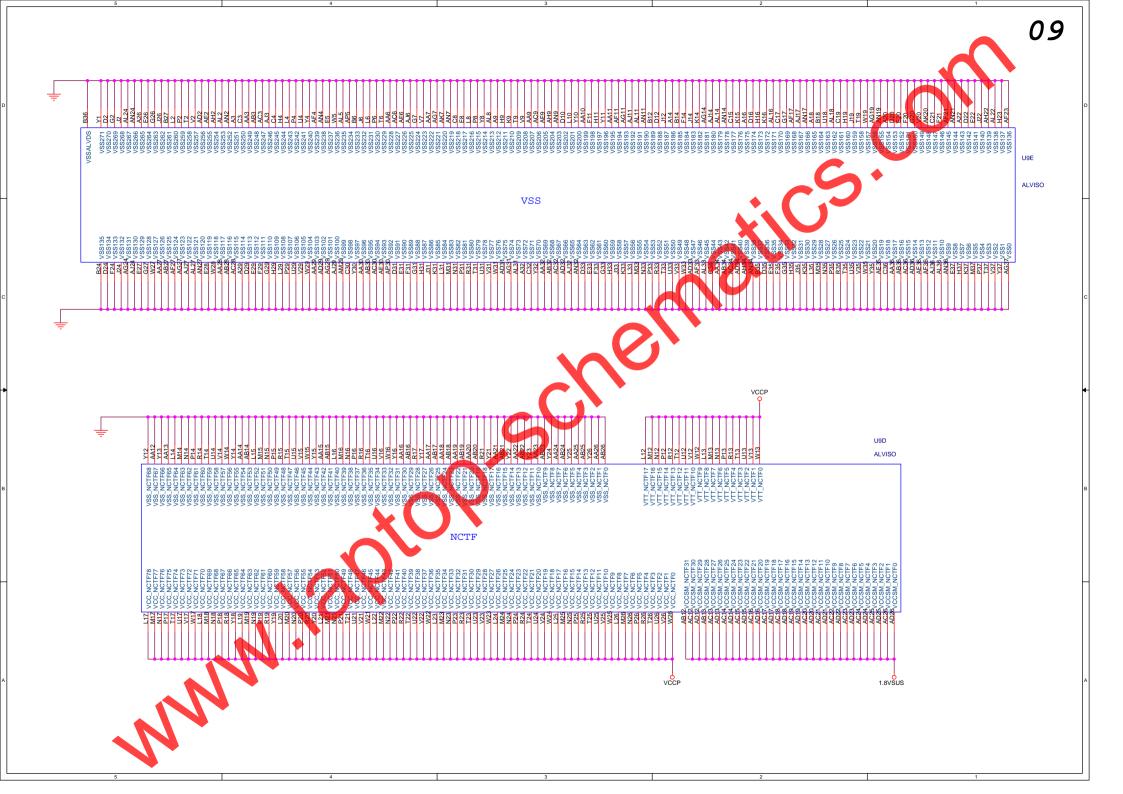


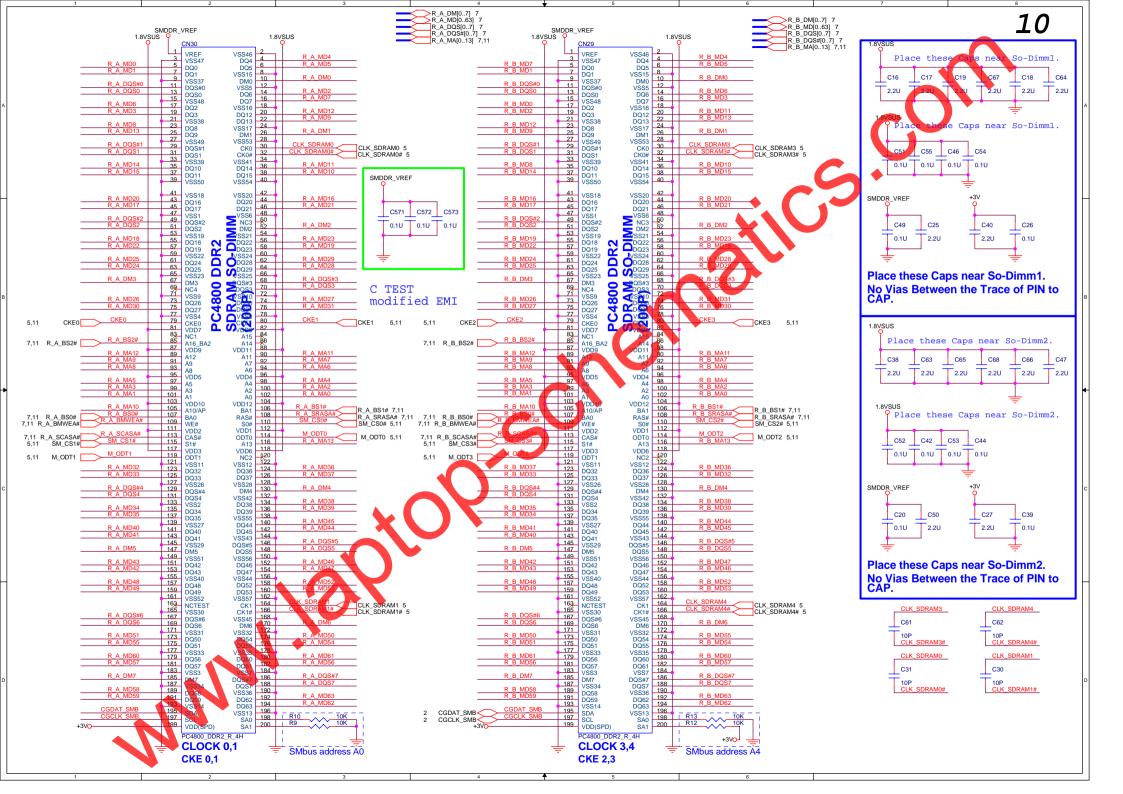
ALVISO POWER STRAP PIN defi CFG[2:0] : 001=FSB533 101=FSB400 other = Rese CFG[4:3] : Reser CFG5 : 0=DMI X 1=DMI X (Default) 1=DDR (Default) 0=Reserved 1=Dothan (Default) CFG8 : Reserved CFG9: 0=Reserve Lanes (15->0, 14->1 etc) 1=Normal Operation (Default) CFG[11:10] : Reserved CFG[13:12] : 00=Reserved 01=XOR Mode Enabled 10=All Z Mode Enabled 11=Normal Operation (Default) CFG[15:14] : Reserved CFG16: 0=Dynamic ODT Disabled 1=Dynamic ODT Enabled (Default) CFG17 : Reserved CFG18 : 0=1.05V (Default) 1=1.5V CFG19 : 0 =1.05V (Default) 1=1.2V (Reserved) CFG 20 : Reserved SDVOCRTL_DATA :0=No SDVO device present (Default) 1=SDVO device present

5.8.12.13.16.32.36 +2.5V

8 VCC3G_PCIE 9 16 31 36 VCCF







DDRII DUAL CHANNEL A,B.

