USB7206

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip USB7206. These checklist items should be followed when utilizing the USB7206 in a new design. A summary of these items is provided in Section 11.0, "Hardware Checklist Summary," on page 25. Detailed information on these subjects can be found in the corresponding section:

- General Considerations on page 1
- Power and Bypass Capacitance on page 2
- Configuration on page 3
- USB Signals on page 4
- USB Connectors on page 9
- Clock Circuit on page 12
- Power and Startup on page 13
- External SPI Memory on page 15
- Miscellaneous on page 18

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The USB7206 implementor should have the following documents on hand:

- *USB7206 6-Port USB 3.1 Gen 2 Controller Hub Data Sheet*
- *USB72x6 Silicon Errata and Data Sheet Clarification*
- *AN26.2 Implementation Guidelines for Microchip USB 2.0 and USB 3.1 Gen 1 Hub Devices Application Note*
- *AN2935 Configuration of USB7202/USB7206/USB725x* Application Note
- *AN3135 USB-to-I^{2}S Bridging with Microchip Hubs*
- *Universal Serial Bus 3.1 Specification*

2.2 Pin Check

Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- The ground flag, **GND**, must be connected to the solid ground plane on the board.
- It is advised that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

2.4 USB-IF Compliant USB Connectors

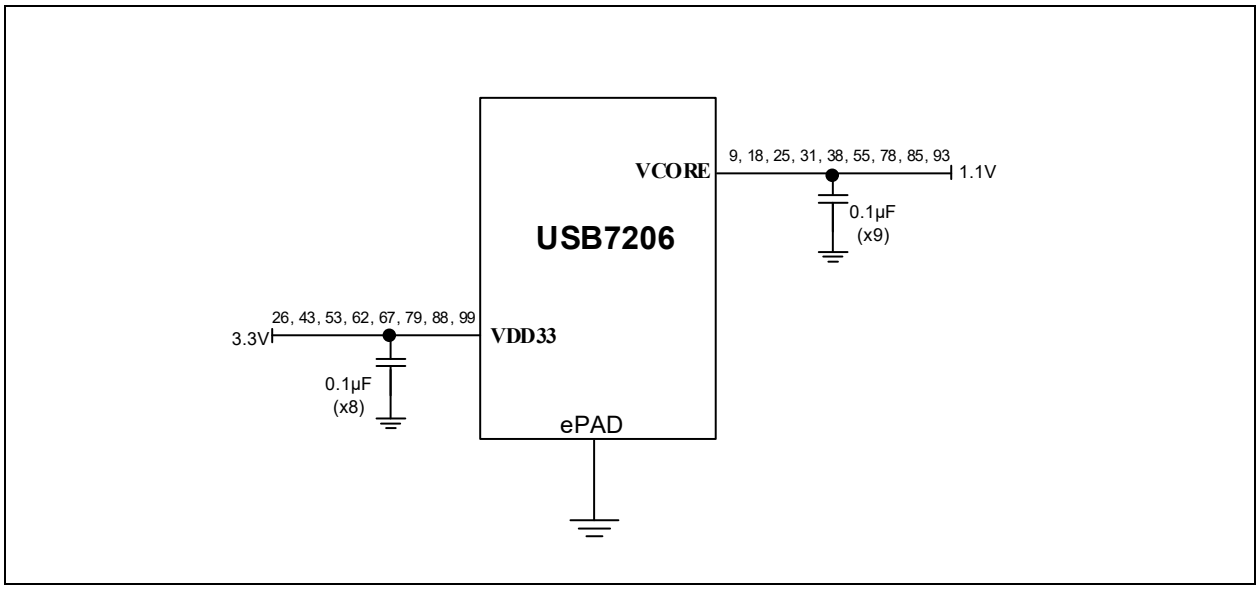
- USB-IF certified USB Connectors with a valid Test ID (TID) are required for all USB products to be compliant and pass USB-IF product certification.

3.0 POWER AND BYPASS CAPACITANCE

- The analog supplies (**VDD33**) require connections to a regulated 3.3V power plane.
  - For USB USB7206, **VDD33** is located on pins 26, 43, 53, 62, 67, 79, 88, and 99.
  - Each **VDD33** pin should include a 0.1 µF capacitor to decouple the device. The capacitor size should be SMD_0603 or smaller.
- The analog supplies (**VCORE**) require connections to a regulated 1.15V power plane.
  - For USB7206, **VCORE** is located on pins 9, 18, 25, 31, 38, 55, 78, 85, and 93.
- Each **VCORE** pin should include a 0.1 µF capacitor to decouple the device. The capacitor size should be SMD_0603 or smaller.

The power and ground connections are shown in Figure 3-1.

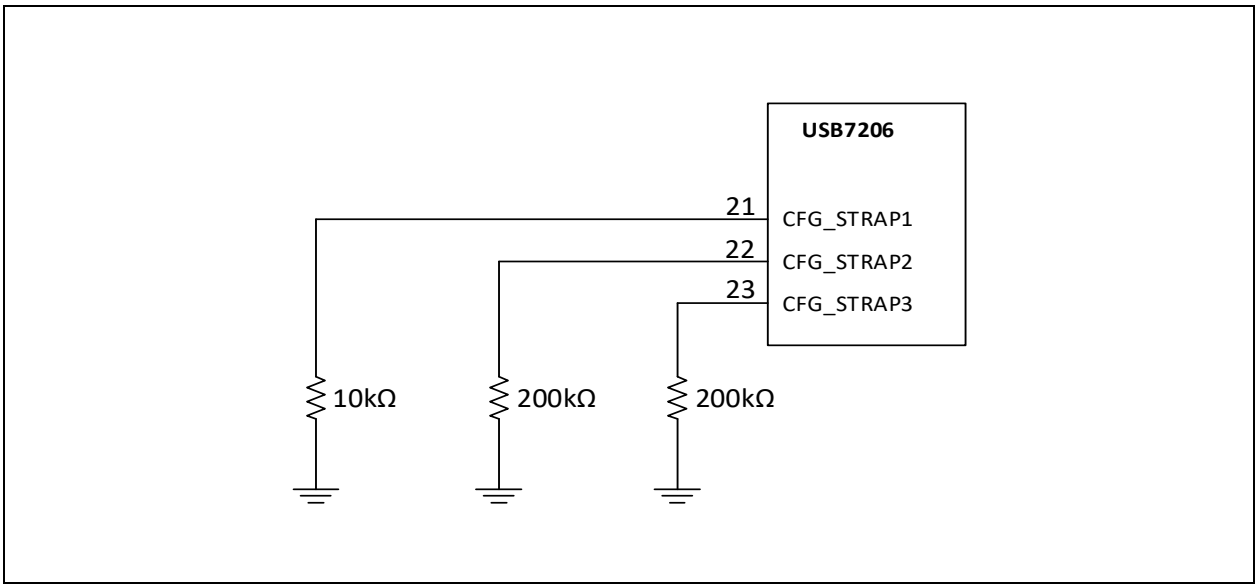
FIGURE 3-1: POWER AND GROUND CONNECTIONS



4.0 CONFIGURATION

Configuration 3 is the only valid configuration for USB7206. Figure 4-1 shows the required Configuration pin connections for USB7206.

FIGURE 4-1: CONFIGURATION STRAP CONNECTION



5.0 USB SIGNALS

5.1 Upstream Port USB Signals

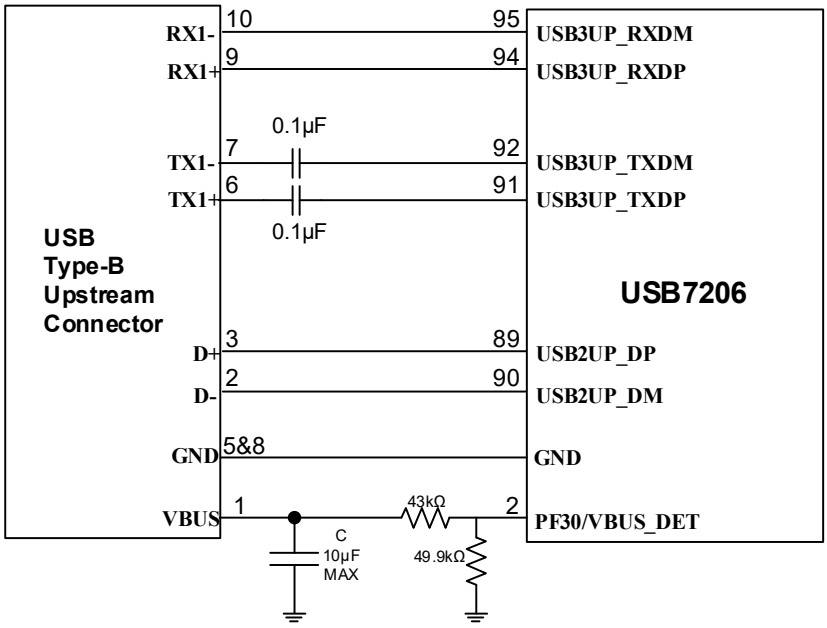
- **USB2UP_DP** (pin 89): This pin is the positive (+) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D+/DP[1] pin of a USB connector.
- **USB2UP_DM** (pin 90): This pin is the negative (–) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D–/DM[1] pin of a USB connector.
- **USB3UP_TXDP** (pin 91): This pin is the positive (+) signal of the upstream USB3.1 'Side A' transmitter (**TX**) differential pair. All necessary USB terminations and resistors are included in the IC. This pin requires a series of 0.1 uF decoupling (DC blocking) capacitor before being connected directly to the **TX+** (or **TX–**)[2] pin of the USB connector.
- **USB3UP_TXDM** (pin 92): This pin is the negative (–) signal of the upstream USB3.1 'Side A' transmitter (**TX**) differential pair. All necessary USB terminations and resistors are included in the IC. This pin requires a series of 0.1 uF decoupling (DC blocking) capacitor before being connected directly to the **TX–** (or **TX+**)[2] pin of the USB connector.
- **USB3UP_RXDP** (pin 94): This pin is the positive (+) signal of the upstream USB3.1 'Side A' receiver (**RX**) differential pair. All necessary USB terminations and resistors are included in the IC. This pin can be connected directly to the **RX+** (or **RX–**)[2] pin of the USB connector.
- **USB3UP_RXDM** (pin 95): This pin is the negative (–) signal of the upstream USB3.1 'Side A' receiver (**TX**) differential pair. All necessary USB terminations and resistors are included in the IC. This pin can be connected directly to the **RX–** (or **RX+**)[2] pin of the USB connector.

Note 1: The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via One-Time Programmable (OTP) or SMBus/I2C configuration registers.

2: A standard feature of USB3.1 is automatic polarity detection and correction. There is no negative impact if the positive and negative pins of the **TX** lines are swapped, or if the positive and negative pins of the **RX** lines are swapped.

For details on standard Type-B port connection, see Figure 5-1.

FIGURE 5-1: UPSTREAM PORT TYPE-B USB CONNECTIONS

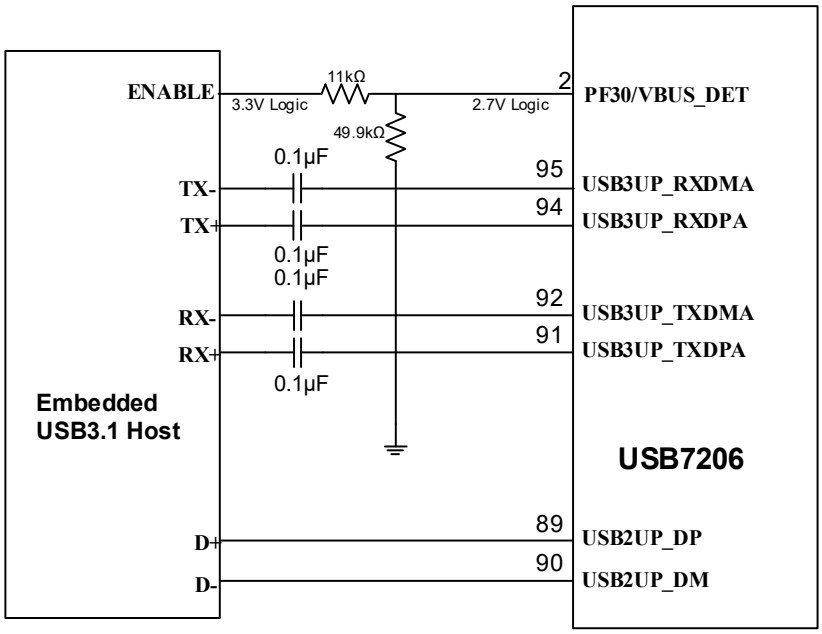


When connecting the upstream port to an embedded USB3.1 host, some pin connections change as indicated below:

- The **VBUS_MON_UP** pin may be connected to an Enable output from the host processor. Alternatively, this can be tied to a 3.3V power rail, but a host control is recommended, whether it be through the **VBUS_MON_UP** pin or the **RESET_N** pin. In any case, the voltage of the signal must be reduced to 2.7V for input to the USB7206.
- Series capacitors are needed in both **TX** and **RX** USB3 signal pairs with an embedded host.

For an example on how to connect the upstream port to an embedded USB3.1 host, refer to Figure 5-3.

FIGURE 5-2: UPSTREAM PORT EMBEDDED HOST USB CONNECTIONS



5.2 Downstream Ports 1, 2, 3, 4, and 5 USB Signals

- **USB2DN_DPx** (pin 5/16/27/34/81): This pin is the positive (+) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D+/DP[1] pin of a USB connector.
- **USB2DN_DMx** (pin 6/17/28/35/82): This pin is the negative (–) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D–/DM[1] pin of a USB connector.
- **USB3DN_TXDPx** (pin 7/19/29/36/83): This pin is the positive (+) signal of the downstream port USB3.1 'Side A' transmitter (**TX**) differential pair. All necessary USB terminations and resistors are included in the IC. This pin requires a series of 0.1 uF decoupling (DC blocking) capacitor before being connected directly to the **TX+** (or **TX–**)[2] pin of the USB connector.
- **USB3DN_TXDMx** (pin 8/20/30/37/84): This pin is the negative (–) signal of the downstream port USB3.1 'Side A' transmitter (**TX**) differential pair. All necessary USB terminations and resistors are included in the IC. This pin requires a series of 0.1 uF decoupling (DC blocking) capacitor before being connected directly to the **TX–** (or **TX+**)[2] pin of the USB connector.
- **USB3DN_RXDPx** (pin 10/14/32/39/86): This pin is the positive (+) signal of the downstream port USB3.1 'Side A' receiver (**RX**) differential pair. All necessary USB terminations and resistors are included in the IC. This pin can be connected directly to the **RX+** (or **RX–**)[2] pin of the USB connector.
- **USB3DN_RXDMx** (pin 11/15/33/40/87): This pin is the negative (–) signal of the downstream port USB3.1 'Side A' receiver (**RX**) differential pair. All necessary USB terminations and resistors are included in the IC. This pin can be connected directly to the **RX–** (or **RX+**)[2] pin of the USB connector.

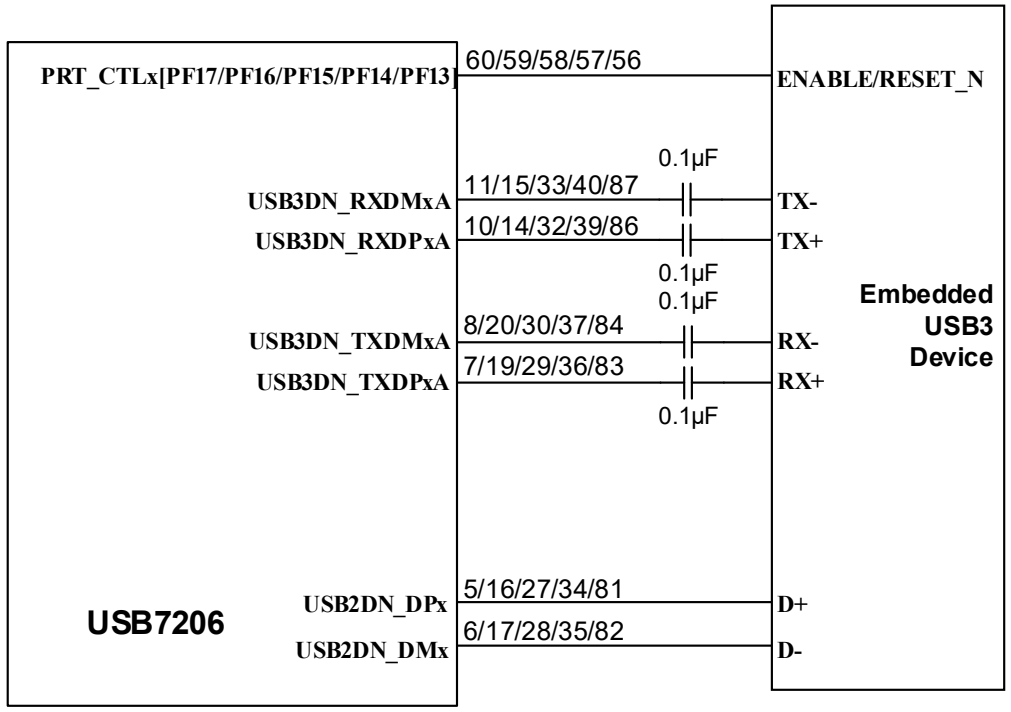
Note 1: The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via OTP or SMBus/I2C configuration registers.

2: A standard feature of USB3.1 is automatic polarity detection and correction. There is no negative impact if the positive and negative pins of the **TX** lines are swapped, or if the positive and negative pins of the **RX** lines are swapped.

- **PRT_CTLx** and **DPx_VBUS_MON** can be shorted together and connected directly to the Enable signal of the USB3.1 device, assuming a 3.3V logic level is required by the device. This gives the USB host the ability to reset the device through standard USB protocol.

For an example on how to connect downstream Port 1, Port 2, or both to an embedded USB3.1 device, refer to Figure 5-3.

FIGURE 5-3: DOWNSTREAM PORTS 1 TO 5 EMBEDDED DEVICE USB CONNECTIONS



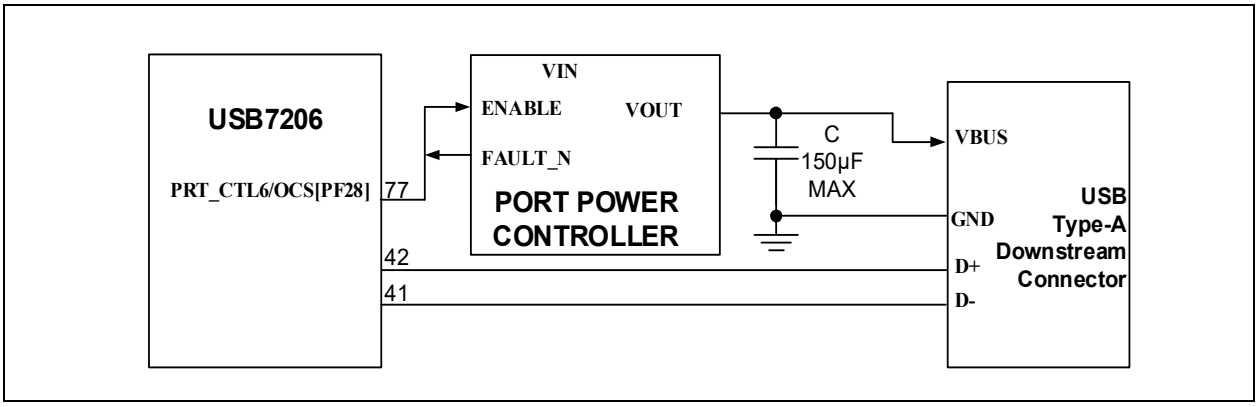
5.3 Downstream Port 6 USB Signals

- **USB2DN_DP3/USB2DN_DP6** (pin 14/37): This pin is the positive (+) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D+/DP1 pin of a USB connector.
- **USB2DN_DM3/USB2DN_DM6** (pin 15/38): This pin is the negative (–) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D–/DM1 pin of a USB connector.
- Downstream Port 6 is a basic USB2.0 (only) port.

Note: The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via OTP or SMBus/I2C configuration registers.

For an example on how to connect downstream Port 6 to USB2.0 connector, refer to Figure 5-4.

FIGURE 5-4: DOWNSTREAM PORT 6 CONNECTIONS



5.4 Disabling Downstream Ports

If a downstream port of the USB7206 is unused, it should be disabled. This can be achieved through hub configuration (I^2C or OTP) or through a port disable strap option.

If using the port disable strap option, the USB_DP2 and USB_DM2 signals should be pulled high to 3.3V. This connection can be made directly to the 3.3V power net or through a pull-up resistor. All other signals related to the associated port may be floated.

5.5 USB Protection

The use of external protection circuitry may be required to provide additional ESD protection beyond what is included in the hub IC. These generally are grouped into three categories:

- TVS protection diodes
  - ESD protection for IEC-61000-4-2 system-level tests
- Application targeted protection ICs or galvanic isolation devices
  - DC overvoltage protection for short to battery protection
- Common-Mode chokes
  - For EMI reduction

The USB7206 can be used in conjunction with these types of devices, but these devices may have a negative effect on USB signal integrity. Thus, it is important to select components accordingly and follow implementation guidelines from the device manufacturer. The following general guidelines for implementing these devices may also be observed:

- Select only devices that are designed specifically for high-speed applications. Per the *USB2.0 Specification*, a total of 5 pF is alloted for connector, PCB traces, and protection circuitry. In a USB3.1 Gen 1 system, ESD protection should add no more than 0.5 pF capacitance to the differential pairs.
- Place these devices as close as possible to the USB connector.
- Never branch the USB signals to reach protection devices. Always place the protection devices directly on top of the USB differential traces.
- Always ensure a very low impedance path to a large ground plane. The effectiveness of TVS devices depends heavily on effective grounding.
- Place TVS diodes on the same layer as the USB signal trace. Avoid vias or place vias behind the TVS device if possible.

5.5.1 ADDITIONAL PROTECTION OPTIONS FOR USB3 PINS

In addition to TVS diodes, some or all of the following may be implemented:

- Use decoupling capacitors on both the **TX** and **RX** differential pairs. Decoupling capacitors on the **RX** pairs are not required for operation but provide some additional ESD immunity at a low cost.
- Use decoupling capacitors with high voltage ratings. The 0.1 µF capacitors at 0402 sizes are widely available.
- A very small resistor of 0.3Ω to 0.5Ω may be placed in series with the decoupling capacitor (placed physically

between the TVS diode and the decoupling capacitor) to help steer more of the ESD energy through the TVS diode. A resistor network (2-resistor/4-contact) in 0402 or 0201 size can be placed with very little impact to the differential routing of the signals.

Note: Microchip PHYBoost, VariSense™, and High-Speed Disconnect Threshold adjustment configuration options are available for compensating the negative effects of these devices. These features can help to overcome marginal failures. It is simplest to determine the appropriate settings using lab experiments, such as USB eye diagram tests, on physical hardware.

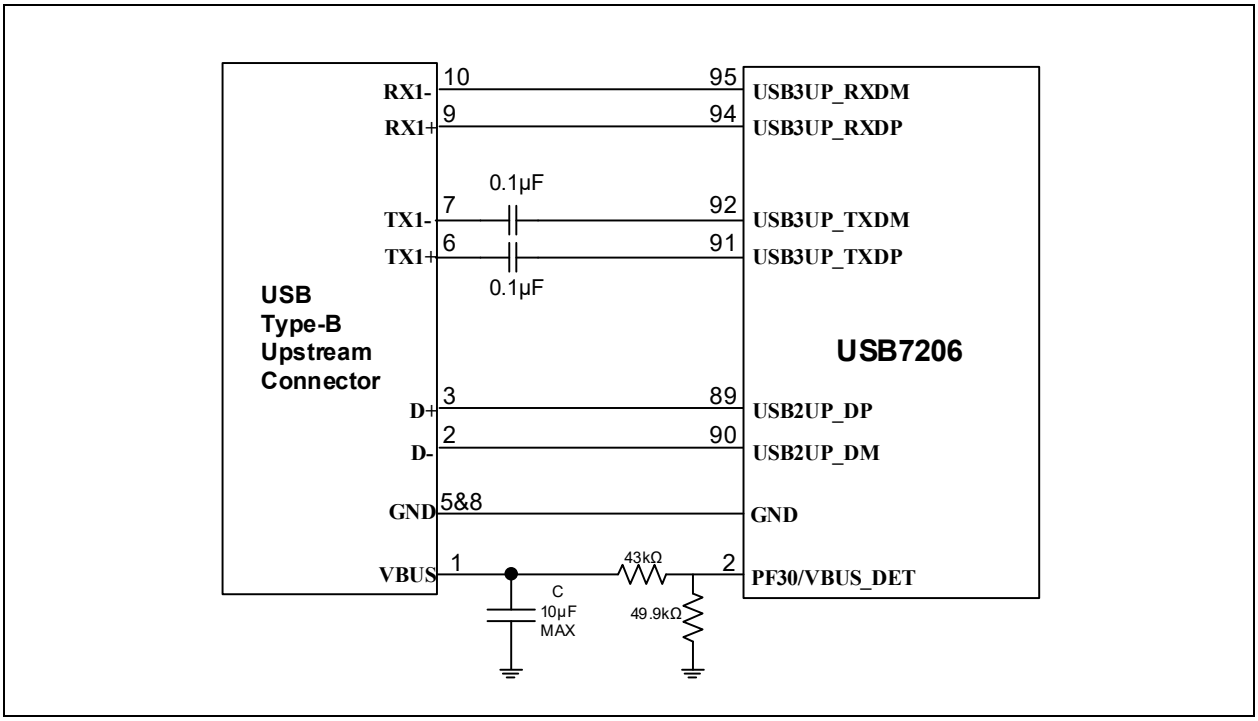
6.0 USB CONNECTORS

6.1 Upstream Port VBUS and VBUS_DET and USB Signals

- The upstream port VBUS line must have no more than 10 µF of total capacitance connected.
- The USB7206 uses the **VBUS_DET** pin to detect the presence of a USB host. The USB host can also toggle the state of VBUS at any time to force a soft reset and reconnection of the USB7206. The **VBUS_DET** may be tied directly to 3.3V. However, this is not recommended as the ability to force a reset of the hub from the USB host VBUS control is lost.

The recommended implementation is shown in Figure 6-1.

FIGURE 6-1: RECOMMENDED UPSTREAM PORT VBUS AND VBUS_DET CONNECTIONS



6.2 Downstream Port VBUS and VBUS_DET and USB Signals

The **PRT_CTLx** pin is a hybrid I/O pin that has the following states:
• PORT OFF: **PRT_CTLx** is an output and drives low. The **PRT_CTLx** pin only transitions to the PORT ON State through a specific command from the USB host.
• PORT ON: **PRT_CTLx** is an input with a weak internal pull-up enabled. The input buffer monitors overcurrent events, which are indicated by the port power controller by pulling the **PRT_CTLx** line low. Once an overcurrent event is detected, the **PRT_CTLx** automatically moves to the PORT OFF State until the USB host can be notified of the overcurrent event.

- When connecting the **PRT_CTLx** pin to a port power controller, the signal should be connected to both the Enable and the fault indicator pins of the port power controller. Do not place an external pull-up resistor on the line.

Note:	The overcurrent detect debounce parameters are configurable and may be adjusted if required to operate properly with the selected port power controller.

An example of a conventional Type-A implementation is shown in Figure 6-2.

FIGURE 6-2: DOWNSTREAM USB SIGNAL AND VBUS CONNECTIONS, PORTS 1 TO 5

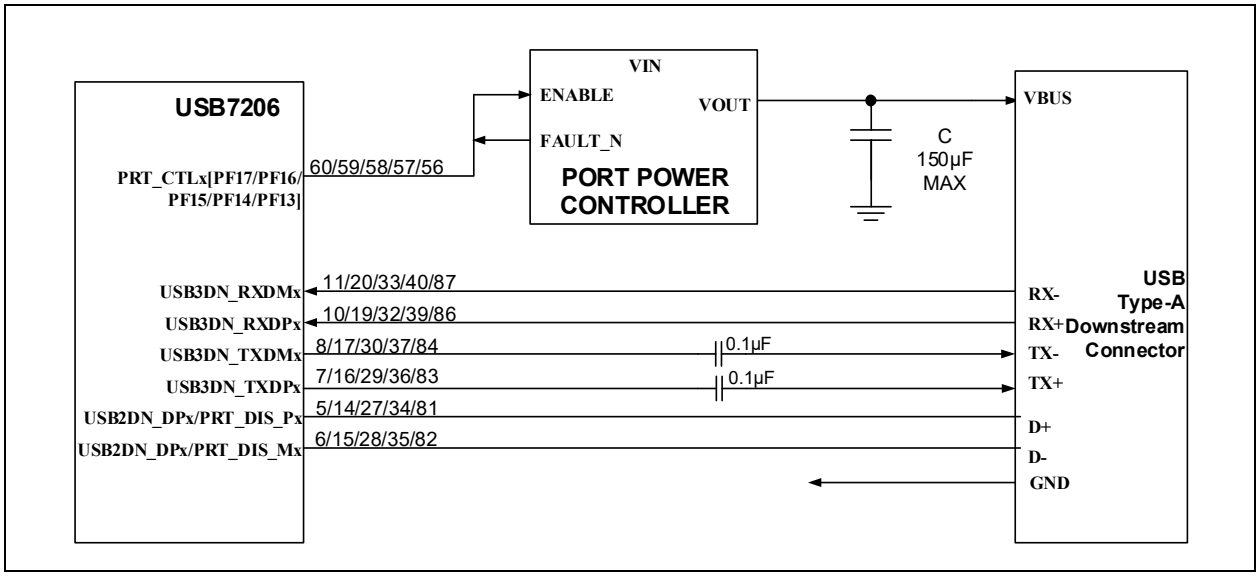
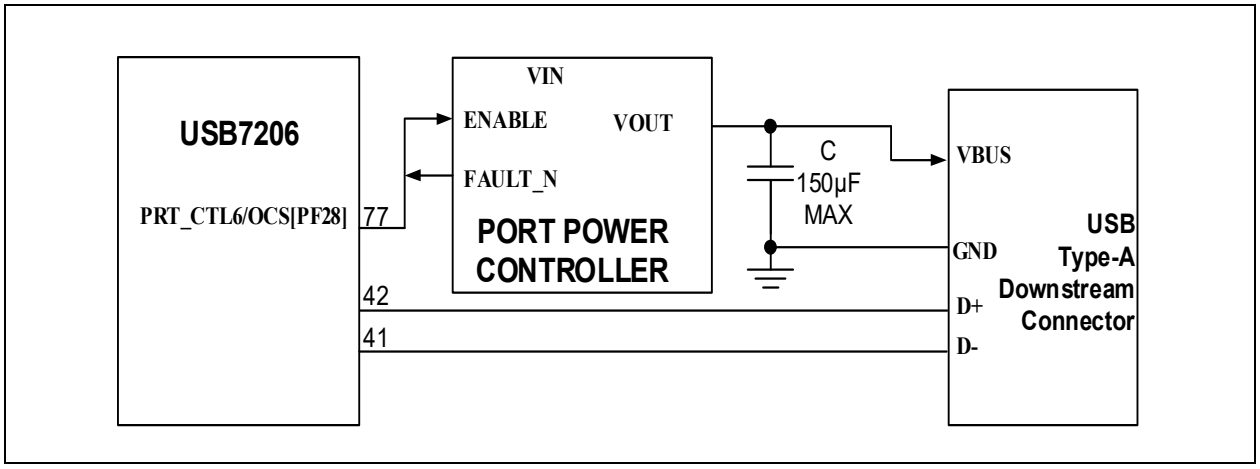


FIGURE 6-3: DOWNSTREAM USB SIGNAL AND VBUS CONNECTIONS, PORT 6



Note: The implementation, as shown in Figure 6-2 and Figure 6-3, assumes that the port power controller has an active-high Enable input, and an active-low, open-drain-style fault indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

6.3 GND and EARTH Recommendations

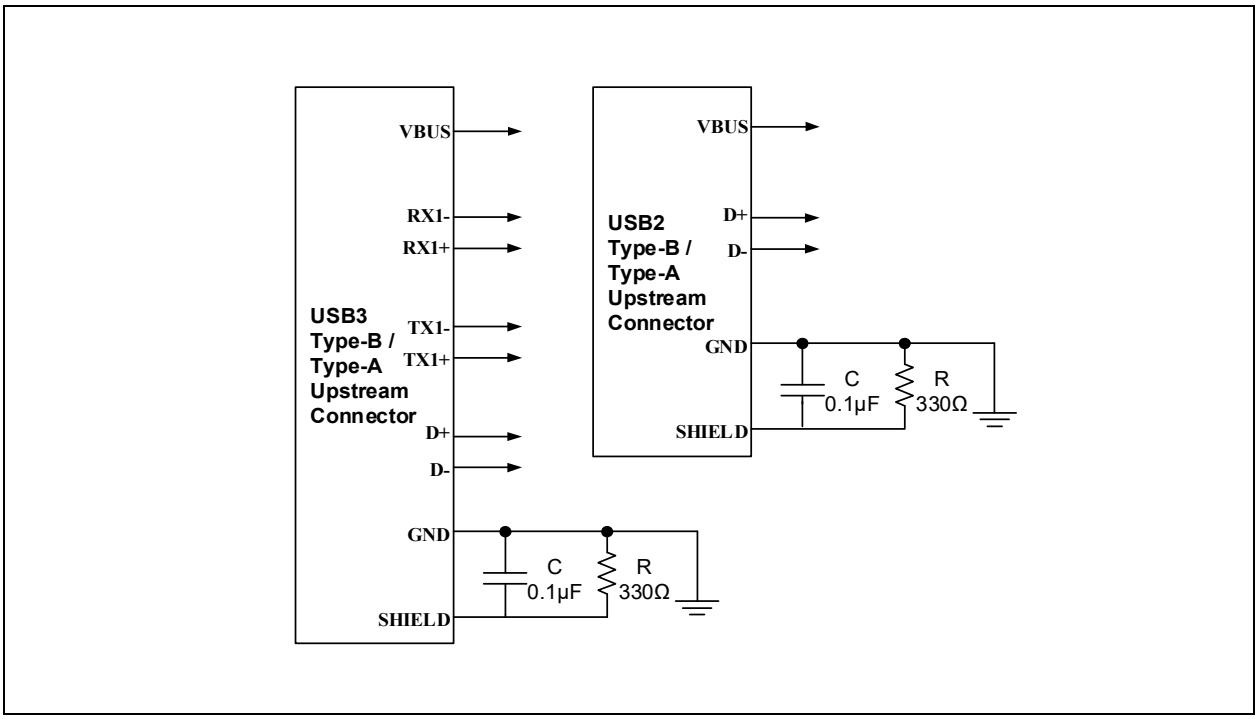
The GND pins of the USB connector must be connected to the PCB with a low impedance path directly to a large GND plane.

The EARTH pins of the USB connector may be connected in one of two ways:

- (Recommended) Connect to GND through a resistor and capacitor in parallel. A resistor-capacitor (RC) filter can help to decouple and minimize EMI between a PCB and a USB cable.
- Connect directly to the GND plane.

The recommended implementation is shown in Figure 6-4.

FIGURE 6-4: RECOMMENDED USB CONNECTOR GND AND EARTH CONNECTIONS



7.0 CLOCK CIRCUIT

7.1 Crystal and External Clock Connection

A 25.000 MHz (±50 ppm) reference clock is the source for the USB interface and for all other functions of the device. For exact specifications and tolerances, refer to the latest version of the *USB7206 Data Sheet*.

- **XTALI** (pin 98) is the clock circuit input for the USB7206. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XTALO** (pin 97) is the clock circuit output for the USB7206. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- The crystal loading capacitor values are system-dependent, which are based on the total CL spec of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit. A commonly used formula for calculating the appropriate physical C1 and C2 capacitor values is shown in Equation 7-1.

EQUATION 7-1:

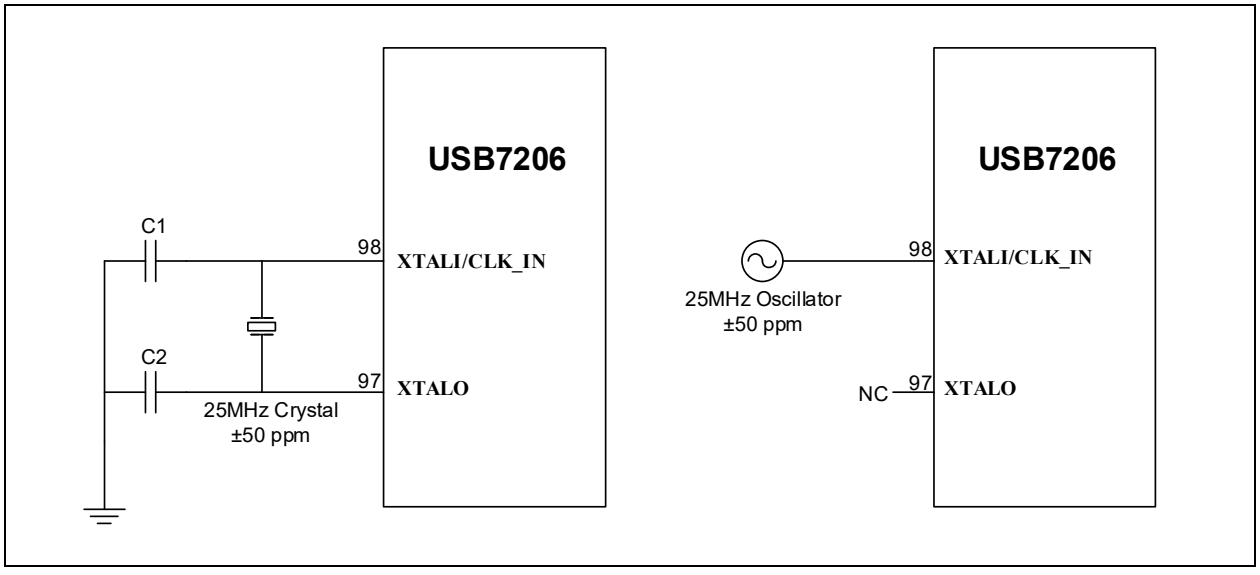
$$C_L = \frac{(C_{X1} \times C_{X2})}{(C_{X1} + C_{X2})}$$

Where CL is the specifications from the crystal data sheet, $C_{X1} = C_{stray} + C_1$, $C_{X2} = C_{stray} + C_2$.

Note: C_{stray} is the stray or parasitic capacitance due to PCB layout. It can be assumed to be very small (between 1 pF to 2 pF range) and verified by physical experiments in the lab if PCB simulation tools are not available.

- Alternatively, a 25.000 MHz, 3.3V clock oscillator may be used to provide the clock source for the USB7206. When using a single-ended clock source, **XTALO** (pin 37) should be left floating as a No Connect (NC).

FIGURE 7-1: CRYSTAL AND OSCILLATOR CONNECTIONS



8.0 POWER AND STARTUP

8.1 RBIAS Resistor

- The **RBIAS** pin on the USB7206 must connect to ground through a 12 kΩ resistor with a tolerance of 1.0%. This is used to set up critical bias currents for the internal circuitry. This should be placed as close as possible to the IC pin, and be given a dedicated, low-impedance path to a ground plane.

8.2 Board Power Supplies

8.2.1 POWER RISE TIME

- The power rail voltage and rise time should adhere to the supply rise time specification as defined in the *USB7206 Data Sheet*.
- If a monotonic or fast power rail rise cannot be assured, then the **RESET_N** signal should be controlled by a reset supervisor and only released when the power rail has reached a stable level.

8.2.2 CURRENT CAPABILITY

- It is important to size the 5V and 3.3V power rails appropriately. The 5V power supply must be capable of supplying 500 mA (if BC1.2 is not enabled), 1.5A (if BC1.2 is enabled), or up to 3.0A (if the maximum Type-C current is enabled) to the USB downstream port VBUS without dropping below the minimum voltage permissible in the USB specification.
- The 3.3V and 1.15V power supply must be able to supply enough power to the USB hub IC. It is recommended that the 3.3V and 1.15V power rails be sized such that they are able to supply maximum power consumption specification as displayed in the applicable *USB7206 Data Sheet*.

8.3 Reset Circuit

- **RESET_N** (pin 28) is an active-low reset input. This signal resets all logic and registers within the USB7206. A hardware reset (**RESET_N** assertion) is not required following power-up. Refer to the latest copy of the *USB7206 Data Sheet* for reset timing requirements. Figure 8-1 shows a recommended reset circuit for powering up the *USB7206* when reset is triggered by the power supply.

FIGURE 8-1: RESET TRIGGERED BY POWER SUPPLY

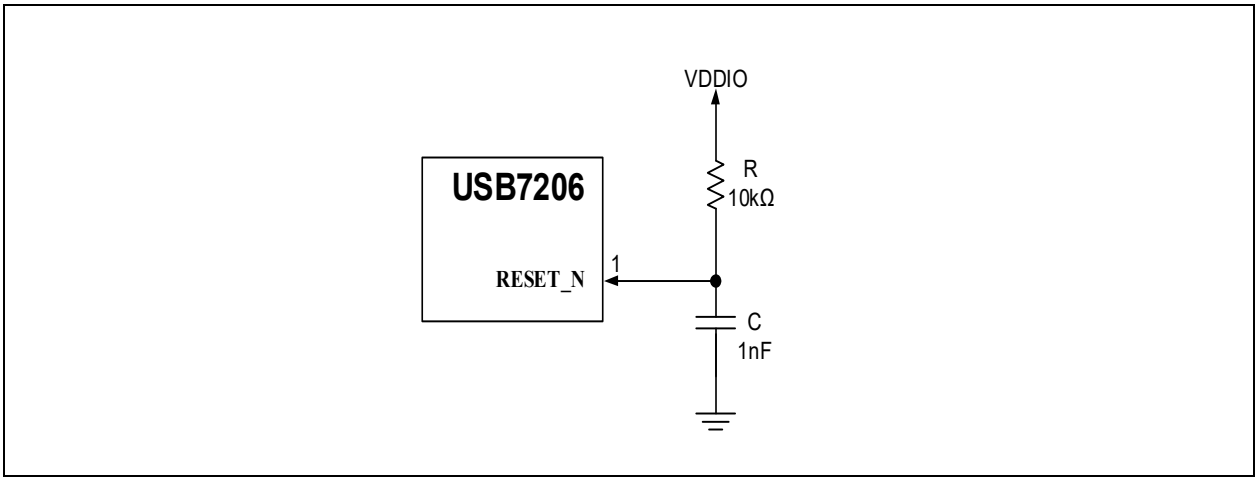
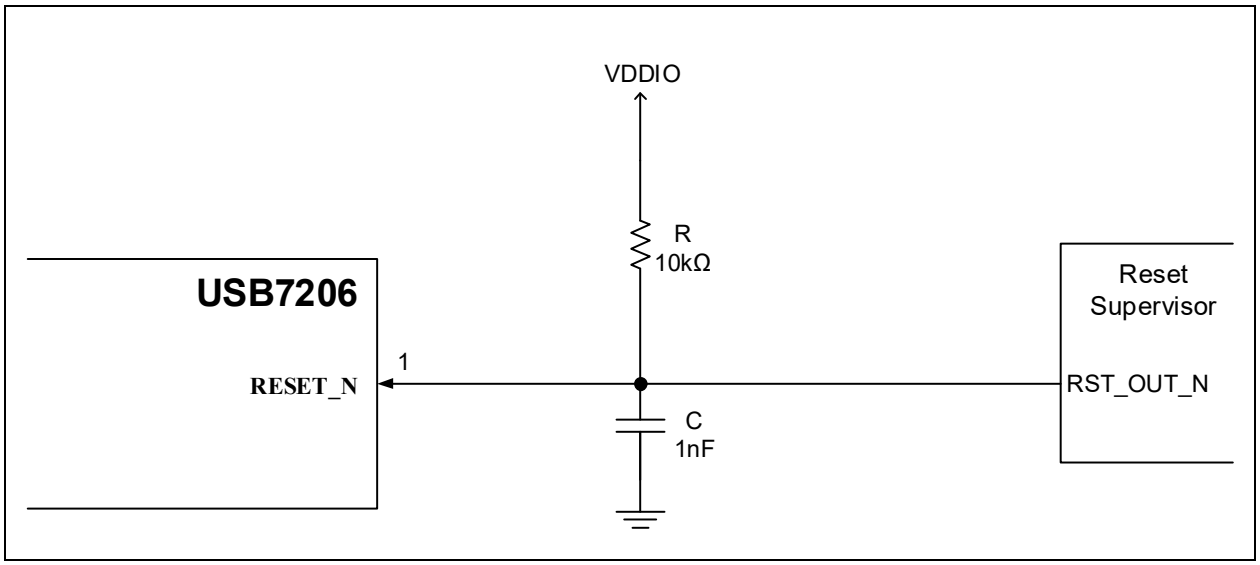


Figure 8-2 details the recommended reset circuit for applications where reset is driven by an external CPU/MCU. The reset out pin (RST_OUT_N) from the CPU/MCU provides the warm reset after power-up.

FIGURE 8-2: RESET CIRCUIT INTERFACE WITH CPU/MCU/SUPERVISOR RESET OUTPUT



9.0 EXTERNAL SPI MEMORY

9.1 SPI Operation Summary

- By default, the USB7206 executes firmware from an internal read only memory (ROM). The USB7206 supports optional firmware execution from an external SPI Flash device. An SPI Flash is only required if a custom firmware is required for the application.
- The SPI interface can operate at 60 MHz or 30 MHz in Dual mode or Quad mode.
- The firmware image can be executed in one of two ways:
  - Execute in place: The firmware is continuously executed directly from the SPI Flash, and the interface is constantly active.
  - Execute in internal SRAM: The firmware is loaded into the hub's internal SRAM and executed internally. This may only be supported if the firmware image is smaller than the hub's SRAM size.

Note:	All firmware images are developed, compiled, tested, and provided by Microchip. The SPI interface speed is an OTP-configurable option and only speeds that were specifically tested with the firmware image should be selected. The execution method is configured with the firmware image itself and cannot be changed via configuration.

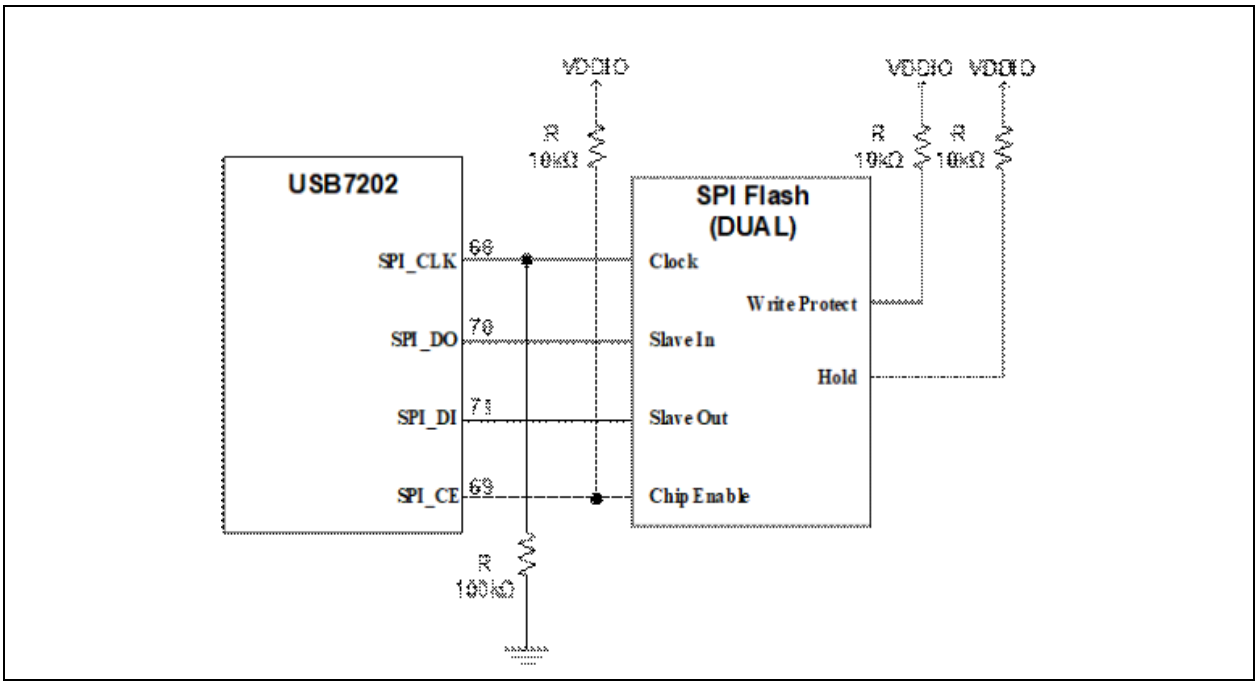
9.2 Compatible SPI Flash Devices

- Microchip recommends SST-brand SPI Flash devices. Microchip has verified compatibility of the following list of SPI Flash devices:
  - SST26VF016B
  - SST26VF032B
  - SST26VF064B
  - SST25VF064C
  - AT25SF041
  - AT26DF081
- Other SPI Flash devices may be used, provided that they meet the following minimum requirements:
  - Operation at 30 MHz or 60 MHz
  - Mode 0 or Mode 3
  - Memory of 256 kB or larger
  - Utilization of the same OpCode commands as with the above list of compatible devices
  - Dual mode or Quad mode operation

9.3 SPI Connection Diagrams

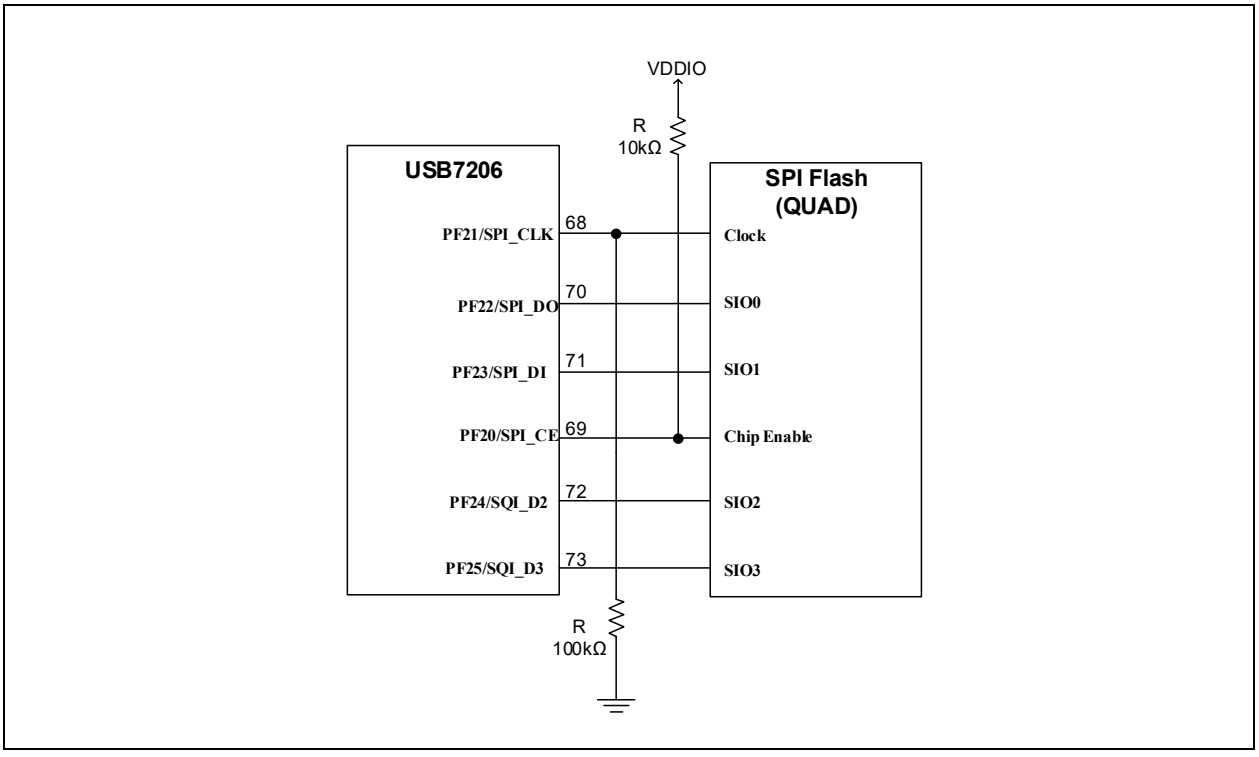
If a Dual SPI Flash device is used, the recommended schematic connections are shown in Figure 9-1.

FIGURE 9-1: DUAL SPI FLASH CONNECTIONS



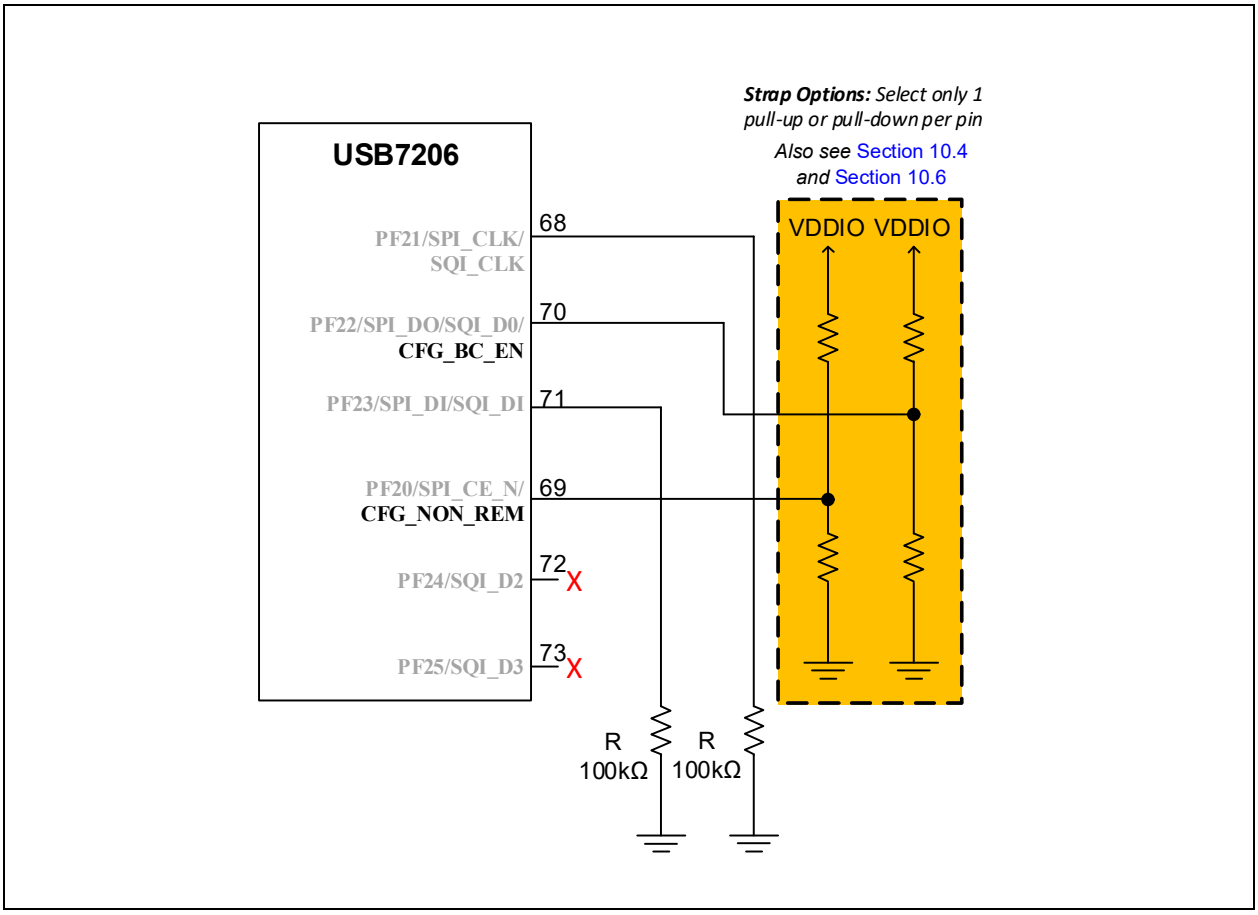
If a Quad SPI Flash device is used, the recommended schematic connections are shown in Figure 9-2.

FIGURE 9-2: QUAD SPI FLASH CONNECTIONS



If an SPI Flash device is not used, the recommended schematic connections are shown in Figure 9-3. Some of the SPI pins become configuration straps when an SPI Flash is not connected. A configuration strap option must be selected, and the pins cannot be floated.

FIGURE 9-3: RECOMMENDED CONNECTIONS IF SPI FLASH IS NOT USED



10.0 MISCELLANEOUS

10.1 GPIOs

- One GPIO pin included on USB7206 may be controlled from the USB host or from an embedded SoC/MCU. This GPIO can be used without any additional configuration. By default, all of the GPIOs are configured as inputs. If a default output Power-On state is required, the default pin output state can be configured in the hub's OTP memory or through the I²C/SMBus slave interface during the configuration stage (SOC_CFG). These pins are described in Table 10-1.

TABLE 10-1: AVAILABLE GPIOS

Pin	PF Pin	Name
74	PF29	GPIO93

- Instructions for operating these pins, including register definitions, are described in full in *AN2932 USB-to-GPIO Bridging with Microchip USB72xx Hubs.*
- Ensure that the voltages applied to these pins are within the electrical specifications for the pins and that any external loading is within the drive strength capabilities as described in the *USB7206 Data Sheet*.

Note: Additional GPIOs may be made available for use under certain conditions or with custom firmware development. Please consult your Microchip support representative or submit a request to the Microchip online support system to discuss options.

10.2 I²C/SMBus Connections

- There are two I²C/SMBus interfaces available on USB7206. These are described in Table 10-2.

TABLE 10-2: I²C/SMBUS PINS

Pin	PF Pin	Name	Role	Configuration Requirements
61	PF18	MSTR_I2C_CLK	USB to I²C master clock	Configuration 3
3	PF31	MSTR_I2C_DATA	USB to I²C master data	Configuration 3
75	PF26	SLV_I2C_CLK	I²C slave data	Configuration 3
76	PF27	SLV_I2C_DATA	I²C slave clock	Configuration 3

10.2.1 SLAVE INTERFACE

- The USB7206 may be configured by an embedded SoC/MCU during both the start-up and runtime stages. Pull-up resistors must be detected by the hub at start-up in order for the I²C/SMBus interface to become active. The interface command specification and configuration register set is described in full in *AN2810 Configuration of USB7002/USB705x*.
- Typically, a pull-up resistor of 1 kΩ to 10 kΩ is sufficient, depending on the interface speed and total capacitance on I²C tree. A pull-up voltage of 1.8V to 3.3V is supported.

Note: If I²C/SMBus pull-up resistors are detected by the USB7206 at start-up, the hub waits indefinitely to be configured by the attached I²C/SMBus master. For early prototyping, it may be necessary to physically remove the pull-up resistors until the I²C/SMBus master is fully operational and can properly configure the hub at start-up.

10.2.2 MASTER INTERFACE

- The USB7206 has an I²C/SMBus master interface that can bridge USB commands to I²C/SMBus. Instructions for operating the I²C/SMBus master interface are contained in *AN2754 USB-to-I²C Bridging with USB7002, USB7050, USB7051, and USB7052 Hubs*.
- Typically, a pull-up resistor of 1 kΩ to 10 kΩ is sufficient, depending on the configured interface speed and total capacitance on I²C tree. A pull-up voltage of 1.8V to 3.3V is supported.
- Ensure that all I²C/SMBus slave devices connected to the bus have unique addresses assigned.
- Ensure that the USB7206 and all I²C/SMBus slave devices connected to the bus can support the target bus speed.

10.3 I²S™ Connections

There is one USB to I²S™ interface available on USB7206. The interface is enabled when Configuration 3 is selected through the **CFG_STRAP** pin. Instructions for configuring the I²S interface, including register definitions, are described in full in *AN3135 USB-to-I²S Bridging with Microchip Hubs.*

A compatible I²S codec is required. By default, the I²S interface is configured to be connected to an ADAU1961. Refer to Table 10-3 to ensure the selected codec is compatible with the options available on USB7206.

TABLE 10-3: I²S™ CODEC COMPATIBILITY GUIDE

Parameter	Supported Values
Sampling Frequency (fs)	8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz
MCLK Frequency	1*fs to 1024*fs Since LRCLK is derived from MCLK source, the MCLK signal should be an even integer multiple of fs.
Audio Sample Size	16-bit, 24-bit, 32-bit
I²S™ Audio Format	I²S™ mode, Left Justified mode, Right Justified mode
I²C Master Control Interface Frequency	100 kHz or 400 kHz
Audio Channels	Mono or Stereo
Interface Enable/Disable Options	Three Options: • Audio OUT and Audio IN mode • Audio OUT Only mode (Speaker Interface) • Audio IN Only mode (Mic Interface)
Audio Jack Insertion Detection	Two Options: • Audio Jack Insertion Detection Enabled (through HID interface) • Audio Jack Insertion Detection Disabled

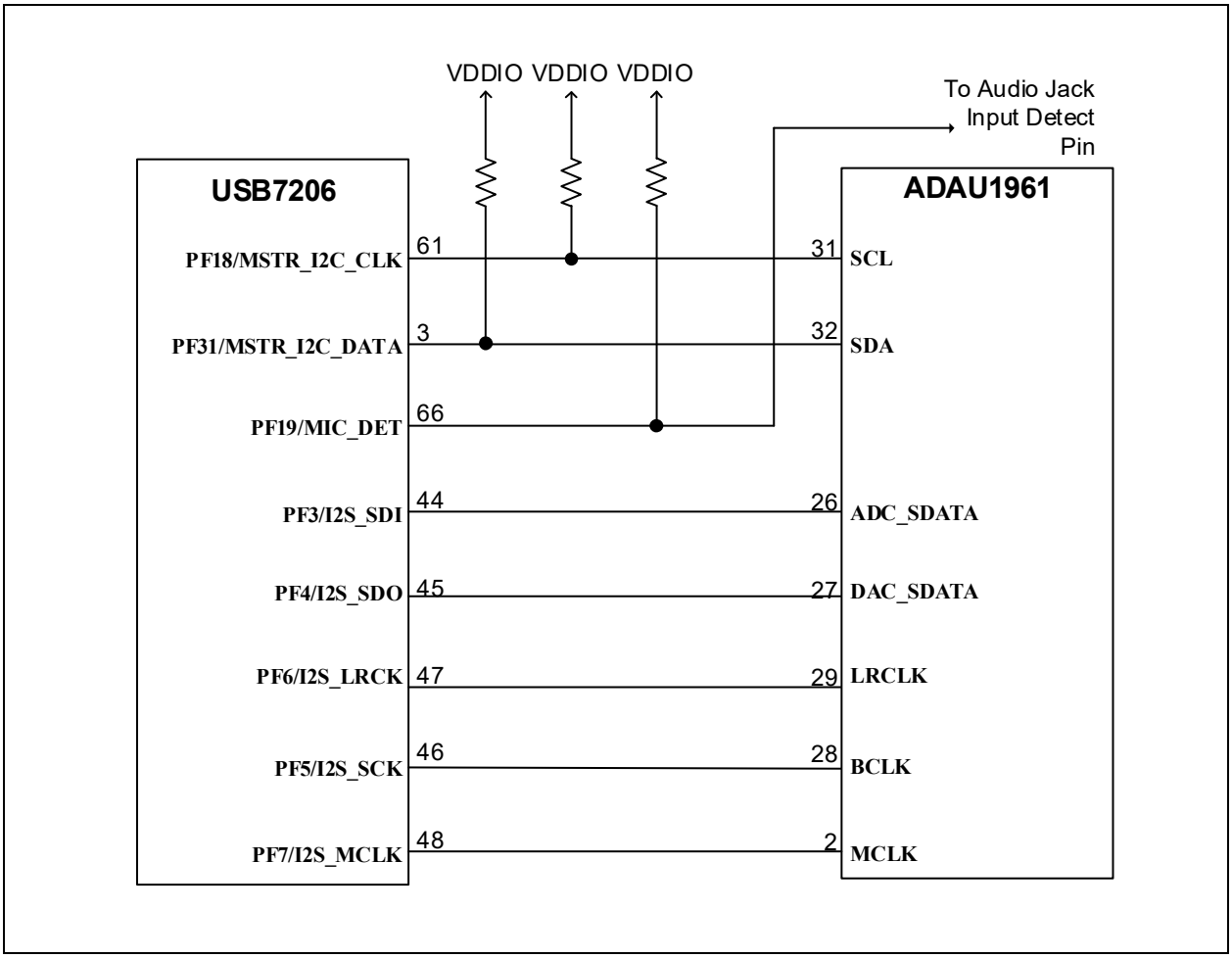
The I²S pins are described in Table 10-4.

TABLE 10-4: I²S™ PINS

Pin	PF Pin	Name	Role	Configuration Requirements
66	PF19	MIC_DET	Optional - Microphone Detection Pin	Configuration 3
44	PF3	I2S_SDI	I²S™ Serial Data In	Configuration 3
47	PF6	I2S_LRCK	I²S Left Right Clock	Configuration 3
45	PF4	I2S_SDO	I²S Serial Data Out	Configuration 3
46	PF5	I2S_SCK	I²S Continuous Serial Clock	Configuration 3
48	PF7	I2S_MCLK	I²S Master Clock	Configuration 3

If connecting to an ADAU1961, the I²S signals should be connected as shown in Figure 10-1. If using a different codec, consult the design guidelines provided by the manufacturer of the selected codec for implementation guidelines.

FIGURE 10-1: ADAU1961 I²S™ CODEC CONNECTIONS



10.4 Non-Removable Port Settings

In a typical USB7206application, downstream Port 1 is routed to a user-accessible USB connector. Thus, the downstream port should be configured as a removable port.

The USB7206 has a configuration strap option, **CFG_NON_REM**, which can be used to set the default configuration for Port 1. This is located on pin 69. The strap setting is sampled one time at start-up. A configuration strap option must be selected unless the hub firmware is being executed from an external SPI Flash device. These are described in Table 10-5.

TABLE 10-5: CFG_NON_REM

Setting	Effect
200 kΩ pull-down to GND	All ports removable (Recommended for most USB7206applications)
200 kΩ pull-up to 3.3V	Port 1 is non-removable. Only a valid selection if Port 1 is connected directly to an embedded USB device.
10 kΩ pull-down to GND	Ports 1 and 2 are non-removable. Only a valid selection if Ports 1 and 2 are connected directly to embedded USB devices.
10 kΩ pull-up to 3.3V	Ports 1, 2, and 3 are non-removable. Only a valid selection if Ports 1, 2, and 3 are connected directly to embedded USB devices.
10 kΩ pull-down to GND	Ports 1, 2, 3, and 4 are non-removable. Only a valid selection if ports 1, 2, 3, and 4 are connected directly to embedded USB devices.

The following guideline can be used to determine which settings to use:

- If the port is routed to a user-accessible USB connector, it is ***removable***.
- If the port is routed to a permanently attached an embedded USB device on the same PCB, or non user-accessible wiring or cable harness, it is ***non-removable***.

Note:	The removable or non-removable device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors, which the USB host may use to understand if a port is a user-accessible port or if the device is a permanently attached device. Under standard operating conditions, the USB host may or may not modify its operation based upon this information. Certain USB compliance tests are impacted by this setting, so designs that must undergo USB compliance testing and certification must have correct configuration settings.

10.5 Self-Powered/Bus-Powered Settings

In a typical USB7206application, the hub should be configured as Self-Powered, which is the default configuration setting.

The following guidelines can be used to determine which setting to use:

- If the entire system (hub included) is powered completely from the upstream USB connector's VBUS pin and the system is designed to operate using standard USB cabling and any standard USB host, the hub system is ***bus-powered***.
- If the entire system (hub included) is always powered by a separate power connector, the hub system is ***self-powered***.
- If the hub included is part of a larger embedded system with fixed cabling and a fixed USB host, the hub system is most likely ***self-powered*** (even if all of the power is derived from the upstream USB connector's VBUS pin).

Note:	The self-powered or bus-powered device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors that the USB host will use to budget power accordingly. Since a standard USB2.0 port is required to supply 500 mA to the downstream port, a self-powered hub and all of its downstream ports must continue to operate within that 500 mA budget. A USB host typically limits the downstream ports of a self-powered hub to 100 mA. Any device that connects to a self-powered hub which declares it needs more than 100 mA is prevented from operating by the USB host.

10.6 Battery Charging Settings

The USB7206 hub includes built-in Dedicated Charging Port (DCP), Charging Downstream Port (CDP), and vendor-specific (SE1) battery charging support.

The USB7206 has a configuration strap option, **CFG_BC_EN**, which can be used to set the default configuration for Port 1. This is located on pin 70. The strap setting is sampled one time at start-up. A configuration strap option must be selected unless the hub firmware is being executed from an external SPI Flash device. The configuration strap options are described in Table 10-6.

TABLE 10-6: CFG_BC_EN

Setting	Effect	Additional Notes
200 kΩ pull-down to GND	Port 1 BC disabled	Battery Charging is not enabled. Select this option if configuration will be done in hub OTP, via I^2C/SMBus or by external firmware in SPI Flash. If SE1 charging is required, this strap option should be selected and SE1 must be enabled in hub OTP, via I^2C/SMBus or by external firmware in SPI Flash.
200 kΩ pull-up to 3.3V	Port 1 BC enabled	Battery Charging is enabled. When no USB host is present (VBUS_DET = 0) downstream Port 1 operates in Dedicated Charging Port mode (DCP mode). When a USB host is present (VBUS_DET = 1), and the USB host has commanded the hub to enable port power, downstream Port 1 operates in Charging Downstream Port mode (CDP mode).
10 kΩ pull-down to GND	Port 1 and 2 BC enabled	Battery Charging is enabled. When no USB host is present (VBUS_DET = 0), downstream Ports 1 and 2 operate in Dedicated Charging Port mode (DCP mode). When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream Ports 1 and 2 operate in Charging Downstream Port mode (CDP mode).
10 kΩ pull-up to 3.3V	Port 1, 2, and 3 BC enabled	Battery Charging is enabled. When no USB host is present (VBUS_DET = 0), downstream Ports 1, 2, and 3 operate in Dedicated Charging Port mode (DCP mode). When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream Ports 1, 2, and 3 operate in Charging Downstream Port mode (CDP mode).
10Ω pull-down to GND	Port 1, 2, 3, and 4 BC enabled	Battery Charging is enabled. When no USB host is present (VBUS_DET = 0), downstream Ports 1, 2, 3, and 4 operate in Dedicated Charging Port mode (DCP mode). When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream Ports 1, 2, 3, and 4 operate in Charging Downstream Port mode (CDP mode).

Note 1: The vendor-specific SE1 charging mode uses the USB data lines to communicate charging capability. Hence, SE1 can only be active when no USB host is present. Additional vendor-specific charging modes exist for charging at elevated current levels when an active data connection is also present. This is handled by a vendor-specific USB protocol between the USB host and the device. The USB7206 supports these vendor-specific protocol exchanges. These vendor-specific command specifications must be obtained from the respective device vendors.

10.7 Test Pins

The USB7206 includes several pins that are in place for manufacturing purposes. These pins are not intended for customer use but must be connected properly for reliable operation of the USB7206.

TABLE 10-7: TEST PIN DETAILS

Pin Name	Required Connection in End Application
TEST1	Pulled up to 3.3V with a 10 kΩ resistor
TEST2	Pulled up to 3.3V with a 10 kΩ resistor
TEST3	Pulled up to 3.3V with a 10 kΩ resistor
TESTEN	Pulled down to ground with a 10 kΩ resistor
TESTA	Not connected

11.0 HARDWARE CHECKLIST SUMMARY

TABLE 11-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	Verify if the ground nets are connected.		
	Section 2.4, "USB-IF Compliant USB Connectors"	Verify if USB-IF-compliant USB connectors with an assigned TID are used in the design (if USB compliance is required for the design).		
Section 3.0, "Power and Bypass Capacitance"	Section 3.0, "Power and Bypass Capacitance"	Ensure that **VDD33** is in the range 3.0V to 3.6V, and a 0.1 µF capacitor is on each pin.		
		Ensure that **VCORE** is in the range 1.09V to 1.21V, and a 0.1 µF capacitor is on each pin.		
Section 4.0, "Configuration"	Section 4.0, "Configuration"	Verify if the CFG_STRAPx pins are set for Configuration 3.		
Section 5.0, "USB Signals"	Section 5.1, "Upstream Port USB Signals" and Section 5.2, "Downstream Ports 1, 2, 3, 4, and 5 USB Signals"	Verify if the USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 D+ and D– data lines, and do not cross the USB3 **TX** and **RX** differential pairs.		
	Section 5.3, "Downstream Port 6 USB Signals"	Verify if the USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 D+ and D– data lines.		
	Section 5.4, "Disabling Downstream Ports"	If any of the USB ports are unused, ensure they are properly disabled via pin strap. If pin strapping is not used, other methods may be used, such as I^2C/SMBus configuration or OTP configuration.		
	Section 5.5, "USB Protection"	Verify if ESD/EMI protection devices are designed specifically for high-speed data applications and that the combined parasitic capacitance of the protection devices, USB traces, and USB connector do not exceed 5 pF on each USB2 trace. Protection devices on USB3 traces should not add more than 0.5 pF to each line.		
Section 6.0, "USB Connectors"	Section 6.1, "Upstream Port VBUS and VBUS_DET and USB Signals"	Verify if the upstream port VBUS has no more than 10 µF capacitance and that the VBUS signal is properly divided down to a 3.3V signal and connected to the **VBUS_DET** pin of the hub.		
	Section 6.2, "Downstream Port VBUS and VBUS_DET and USB Signals"	Verify if **PRT_CTL1** and **PRT_CTL2** are properly connected to both the Enable pin of the downstream port power controller and the fault indicator output of the port power controller. Ensure that the port power controller current capability is sized appropriately (500 mA, 900 mA, 1.5A, or 3A) and that the overcurrent threshold is set appropriately.		
	Section 6.3, "GND and EARTH Recommendations"	Verify if the USB connector is properly connected to PCB ground on both the GND pins and the SHIELD pins. It is recommended that an RC filter be placed between the SHIELD pins and PCB ground.		
Section 7.0, "Clock Circuit"	Section 7.1, "Crystal and External Clock Connection"	Confirm if the crystal or clock is 25.000 MHz (±50 ppm). If a single-ended lock is used, ensure that it is connected to **XTALI** while leaving **XTALO** floating. If a crystal is used, ensure that the loading capacitors are appropriately sized for the crystal loading requirement.		

TABLE 11-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 8.0, "Power and Startup"	Section 8.1, "RBIAS Resistor"	Confirm if a 12.0 kΩ 1% resistor is connected between the **RBIAS** pin and the PCB ground.		
	Section 8.2, "Board Power Supplies"	Verify if the board power supplies deliver 3.0V to 3.6V to VDD33 and 1.09V to 1.21V to VCORE, and that the power-on rise time meets the requirement of the hub as defined in the data sheet. If the rise time requirement cannot be met, ensure that the **RESET_N** line is held low until the power regulators reach a steady state.		
	Section 8.3, "Reset Circuit"	Ensure that the **RESET_N** signal has an external pull-up resistor, or is otherwise properly controlled by an external SoC, MCU, or Reset supervisor device.		
Section 9.0, "External SPI Memory"	Section 9.1, "SPI Operation Summary"	Determine if a custom SPI firmware image is required and which mode of operation the selected SPI Flash device must support.		
	Section 9.2, "Compatible SPI Flash Devices"	Ensure the selected SPI Flash device is compatible with the hub.		
	Section 9.3, "SPI Connection Diagrams"	Verify if the SPI Flash is connected according to the diagrams in Figure 9-1 or Figure 9-2. Follow Figure 9-3 if no SPI Flash is connected in the design.		
Section 10.0, "Miscellaneous"	Section 10.1, "GPIOs"	Verify if the GPIO pins that will be used as GPIOs within the application are connected properly. Never exceed the voltage maximums/minimums or overload the current source/sink maximums as defined in the hub data sheet.		
	Section 10.2, "I2C/SMBus Connections"	If the USB to I^2C/SMBus slave interface is implemented, ensure that appropriate pull-up resistors are connected and that the connections to the I^2C/SMBus master are correct. Note that the pull-up resistors are detected on the I^2C/SMBus slave interface, the USB hub will not enumerate to a USB host until it receives the special “Attach” command from the I^2C/SMBus master.		
	Section 10.3, "I2S™ Connections"	If using the USB-to-I^2C bridging feature, ensure that Configuration 2 is selected via the **CFG_STRAP** pin, and ensure that the pin connections to the I^2S™ codec are correct. If using any codec other that the ADAU1961, ensure that it is compatible by referencing the compatibility guide in Table 10-4.		
	Section 10.4, "Non-Removable Port Settings"	Verify if the CFG_NON_REM configuration strap is set per application requirements. Most USB7206 applications should set this strap to the ‘Port 1 Removable’ setting.		
	Section 10.5, "Self-Powered/Bus-Powered Settings"	Verify the application requirements for Self-Powered or Bus-Powered operation. If Self-Powered operation is required, then no additional configuration or circuitry is required. If Bus-Powered operation is required, then the hub must be configured via OTP or I^2C/SMBus.		
	Section 10.6, "Battery Charging Settings"	Verify that the CFG_BC_EN configuration strap is set per application requirements. Most USB7206 applications should set this strap to the ‘Port 1 BC Enable’ setting.		
	Section 10.7, "Test Pins"	Verify if the test pins are correctly connected.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003336A (12-18-19)	Initial release	

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ISBN:978-1-5224-5425-0

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