3810: Computer Organization
Lecture 10: Memory

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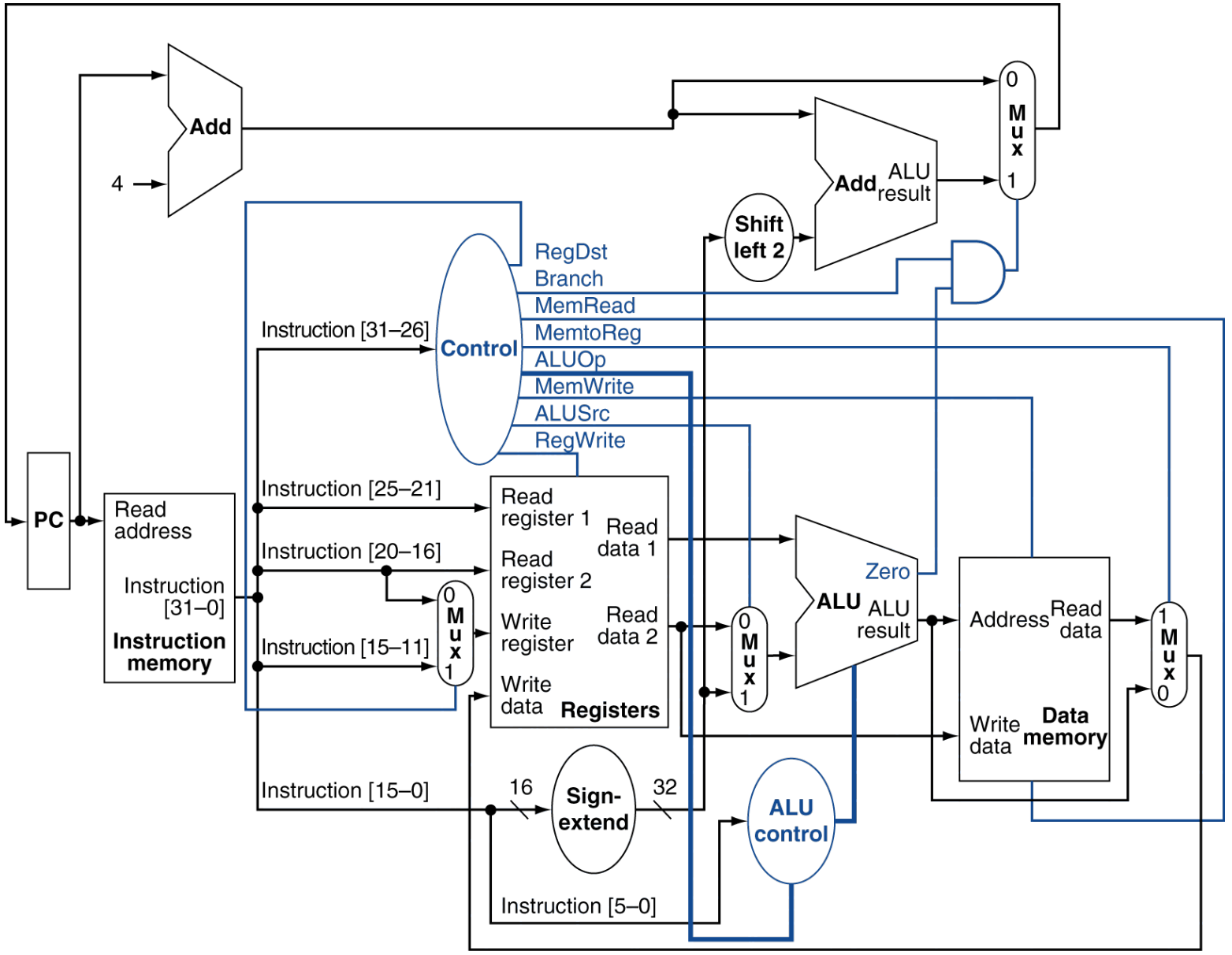
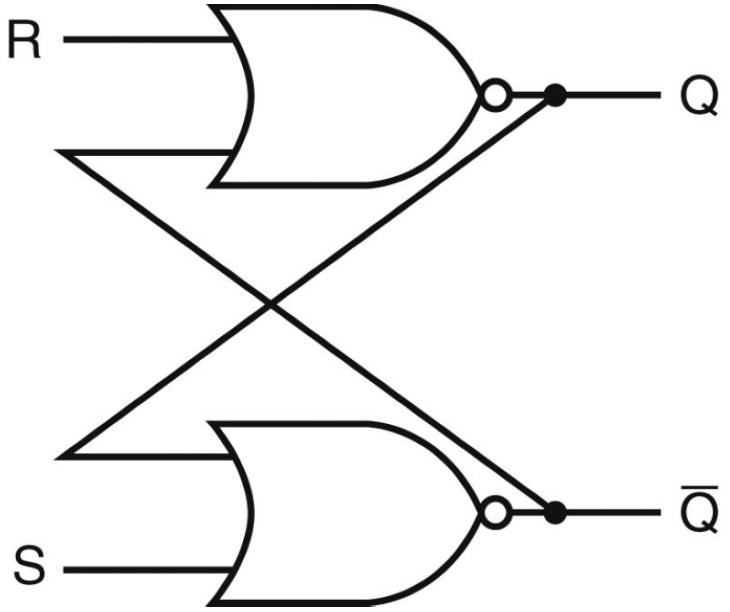
MIPS Datapath



Designing a Latch

- An S-R latch: set-reset latch
  - When Set is high, a 1 is stored
  - When Reset is high, a 0 is stored
  - When both are low, the previous state is preserved (hence, known as a storage or memory element)
  - Both are high – this set of inputs is not allowed

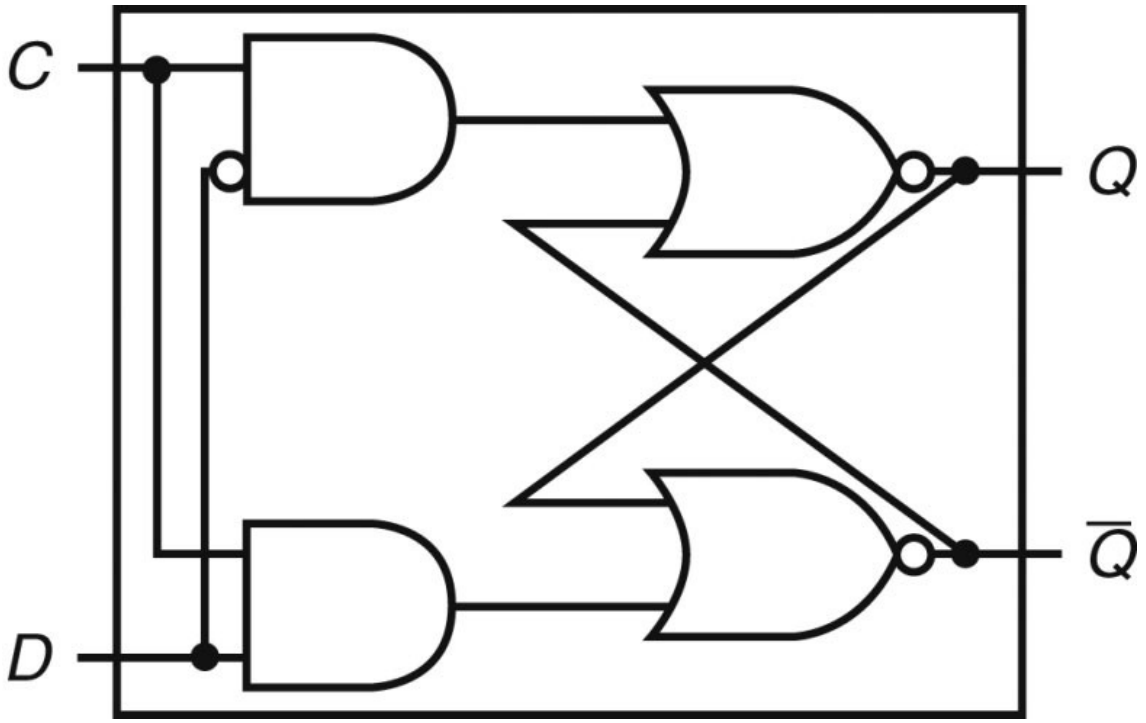
Verify the above behavior!



Source: H&P textbook

D Latch

- Incorporates a clock
- The value of the input D signal (data) is stored only when the clock is high – the previous state is preserved when the clock is low

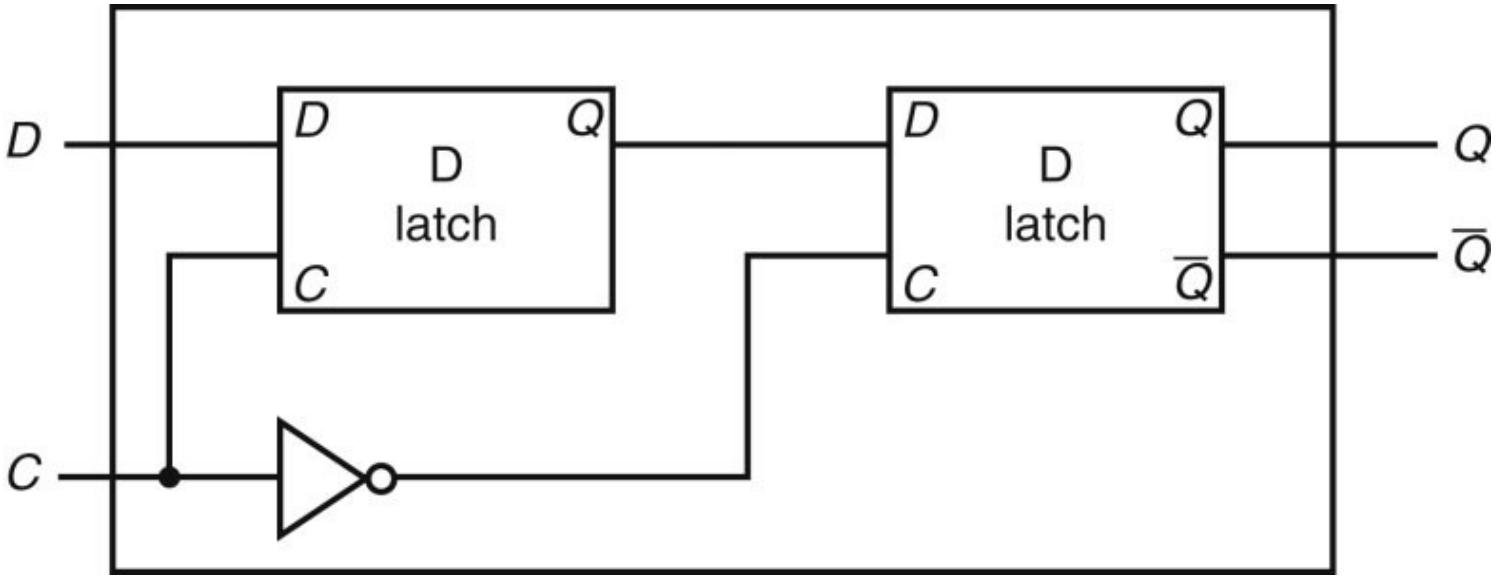


Source: H&P textbook

D Flip Flop

- Terminology:
  Latch: outputs can change any time the clock is high (asserted)
  Flip flop: outputs can change only on a clock edge

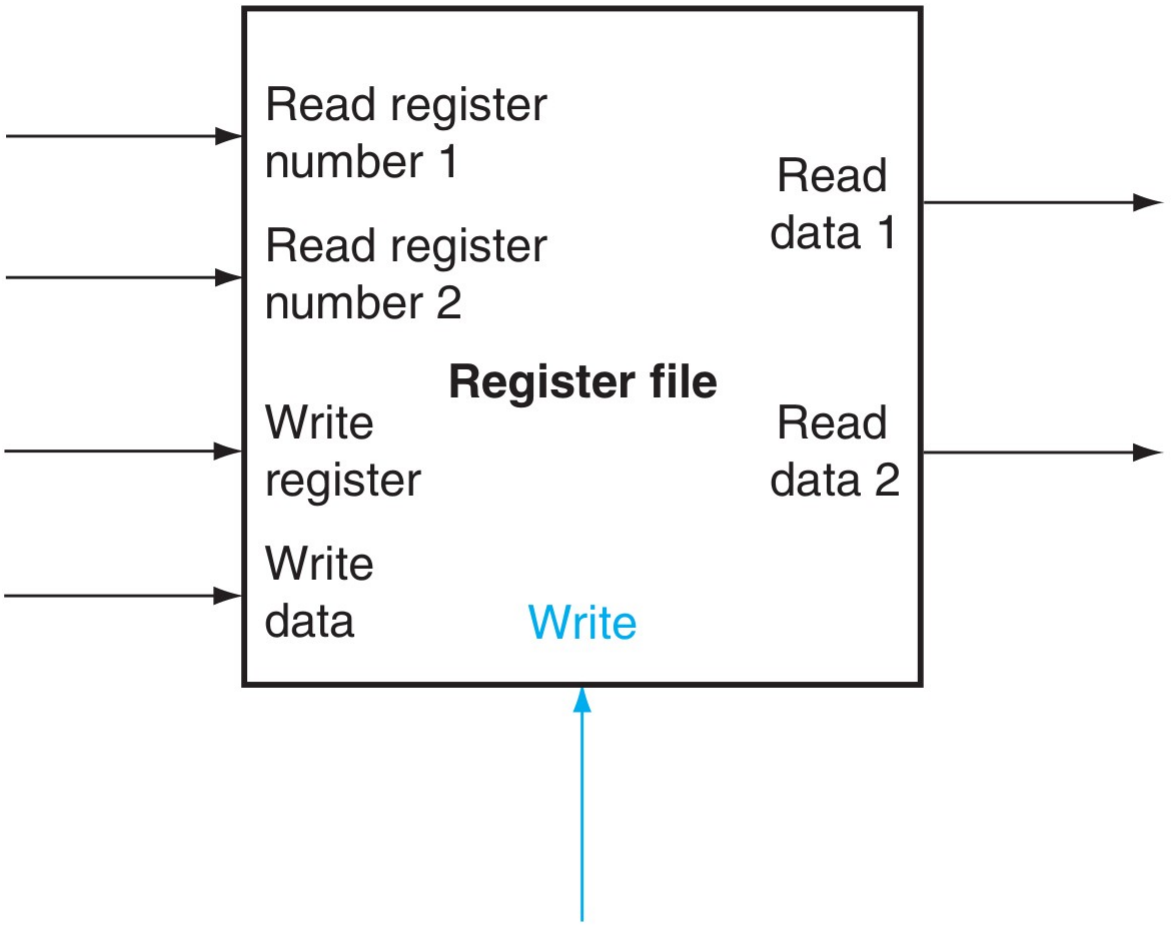
- Two D latches in series – ensures that a value is stored only on the falling edge of the clock



Source: H&P textbook

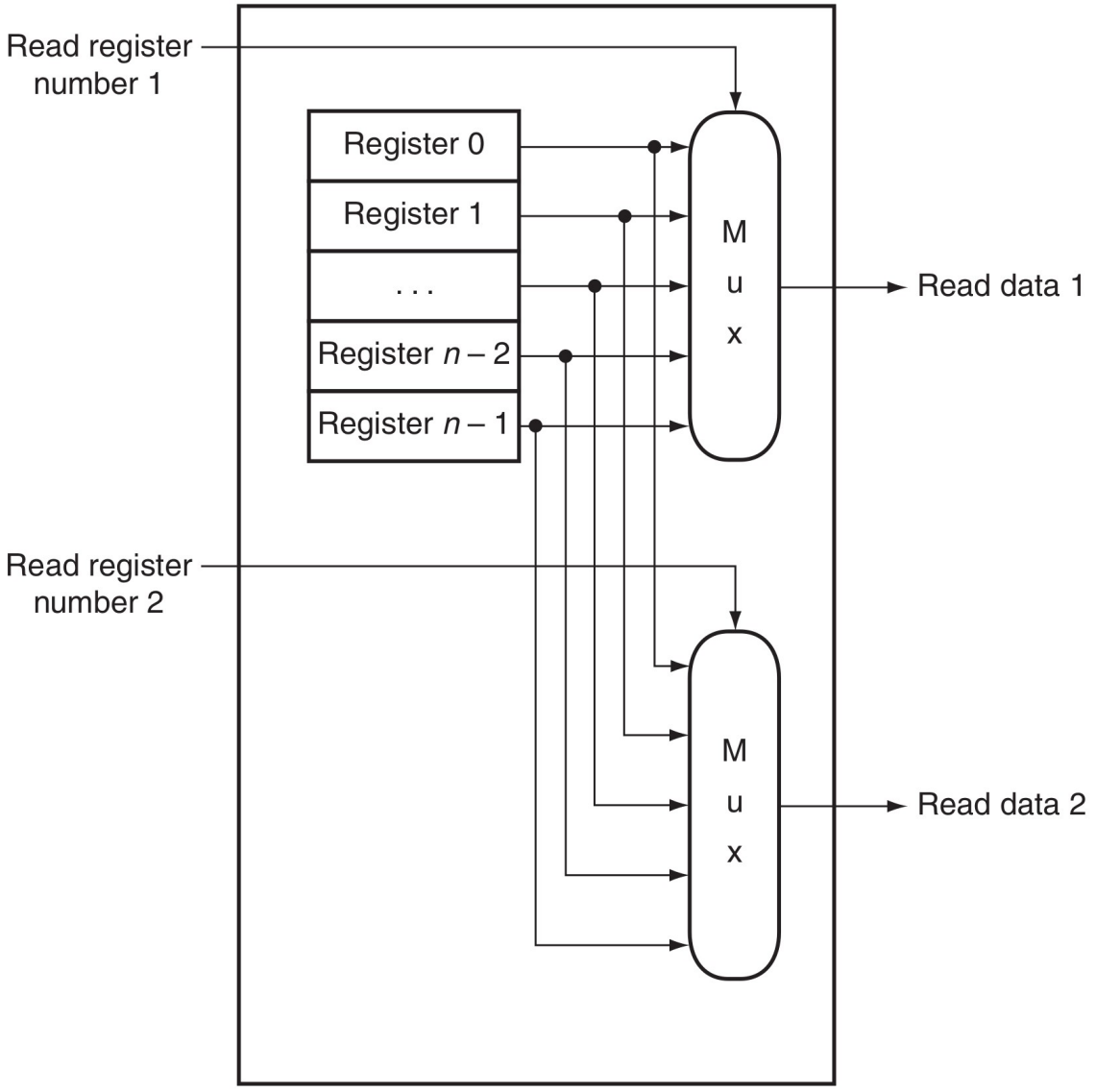
Register file

- Two read ports
- One write port



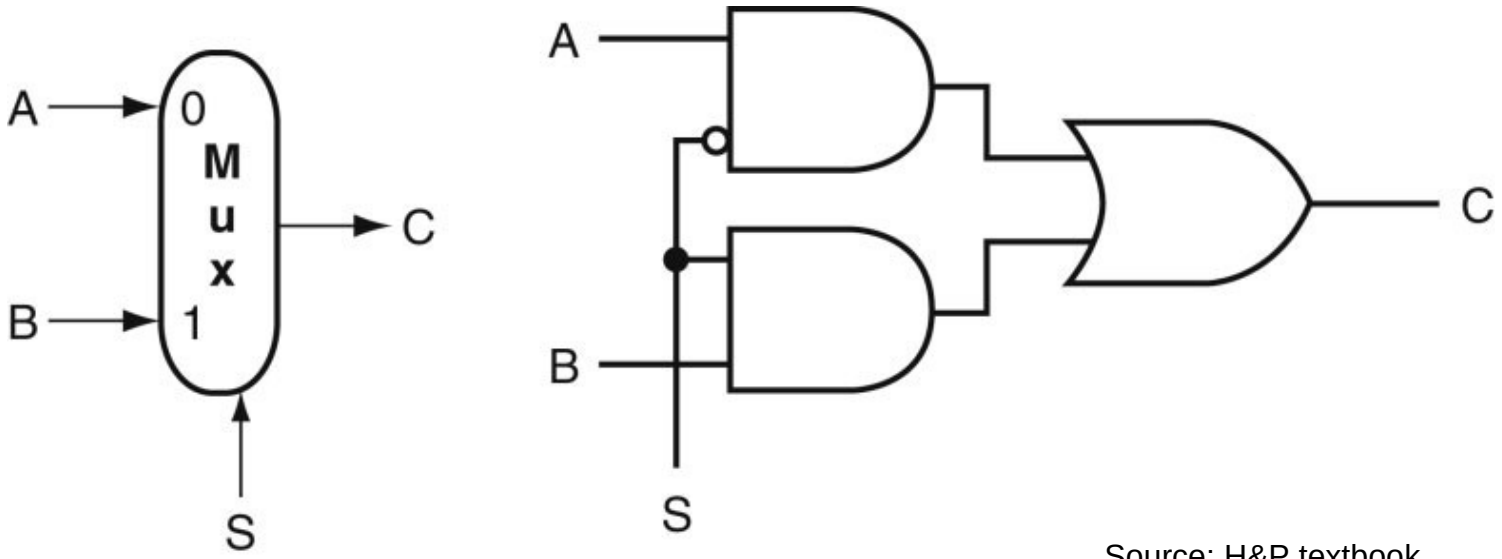
Register file (read ports)

- Build from D-flops
- Read ports
  - Multiplexors
  - N-to-1, 32bit wide



Common Logic Blocks – Multiplexor

- Multiplexor or selector: one of N inputs is reflected on the output depending on the value of the $\log_2 N$ selector bits

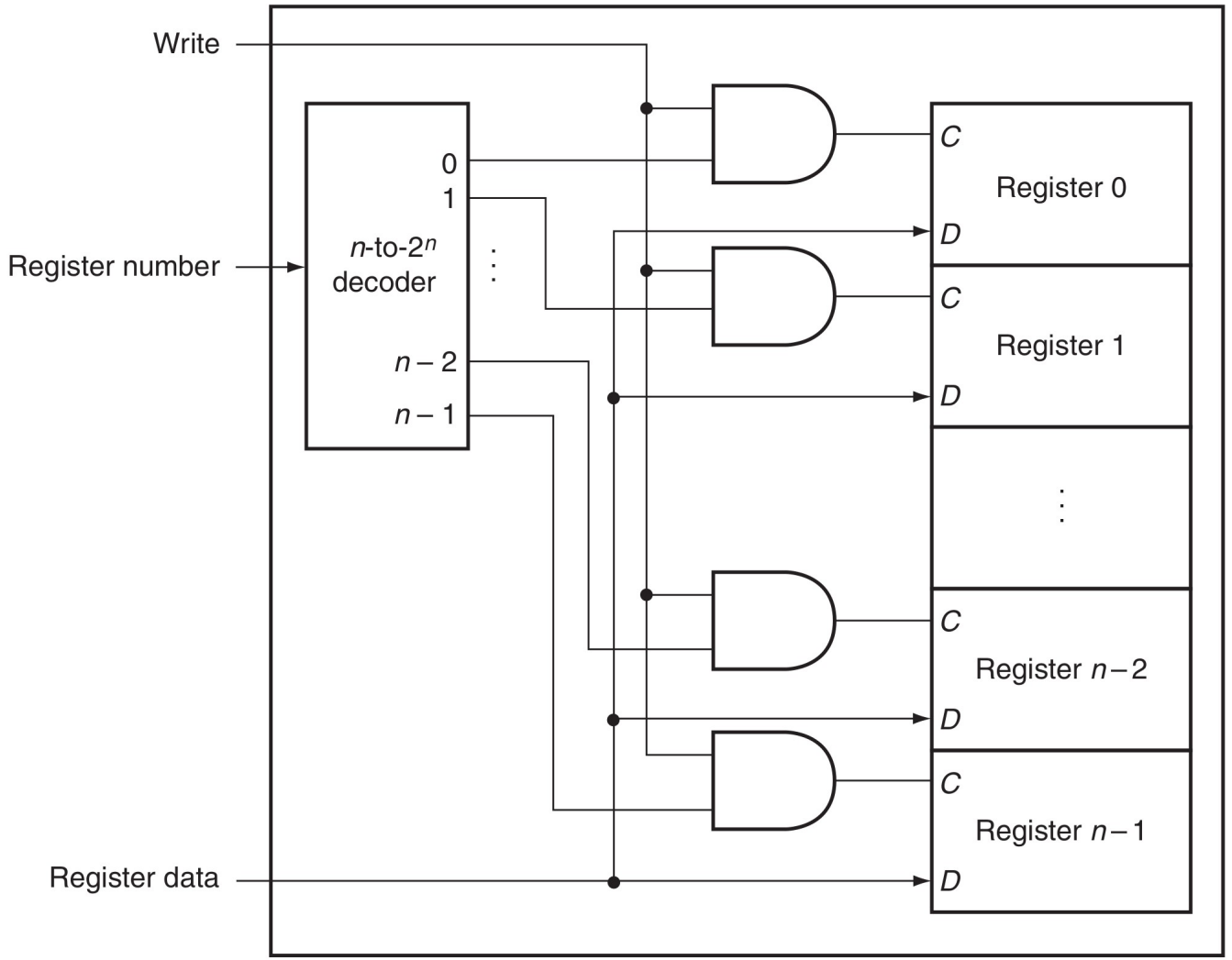


2-input mux

Source: H&P textbook

Register file (write ports)

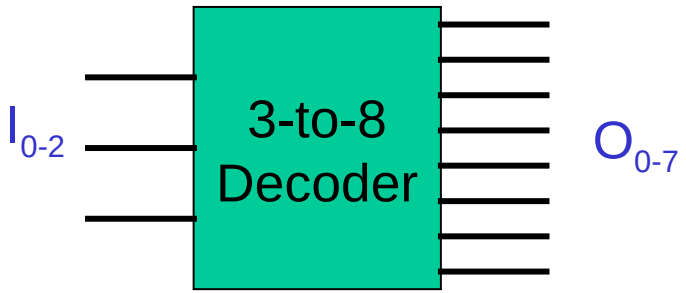
- Decoder



Common Logic Blocks – Decoder

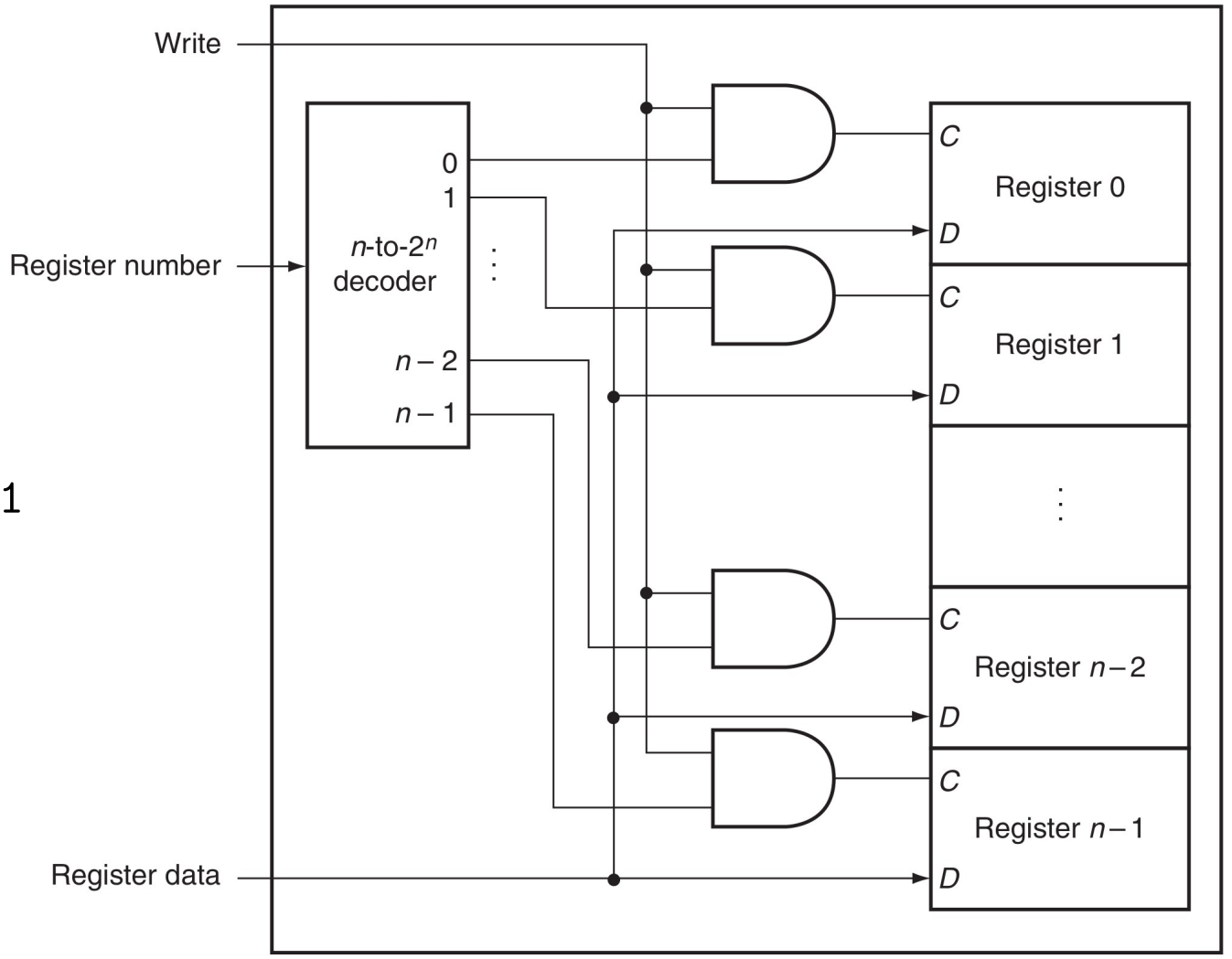
Takes in N inputs and activates one of 2^N outputs

I_0	I_1	I_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

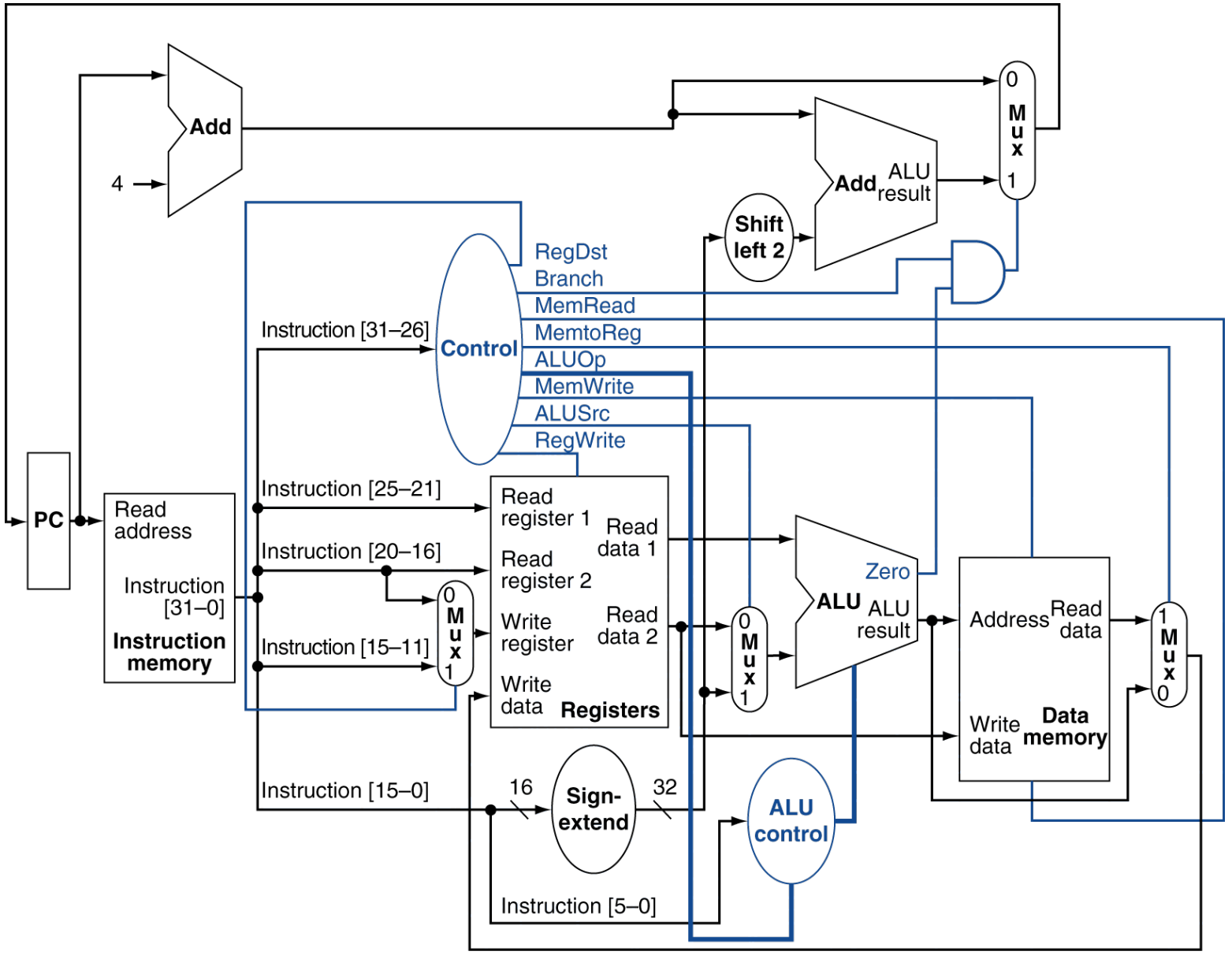


Register file (write ports)

- What if we read and write the register in the same cycle?
  - `add $s0, $s0, $s1`



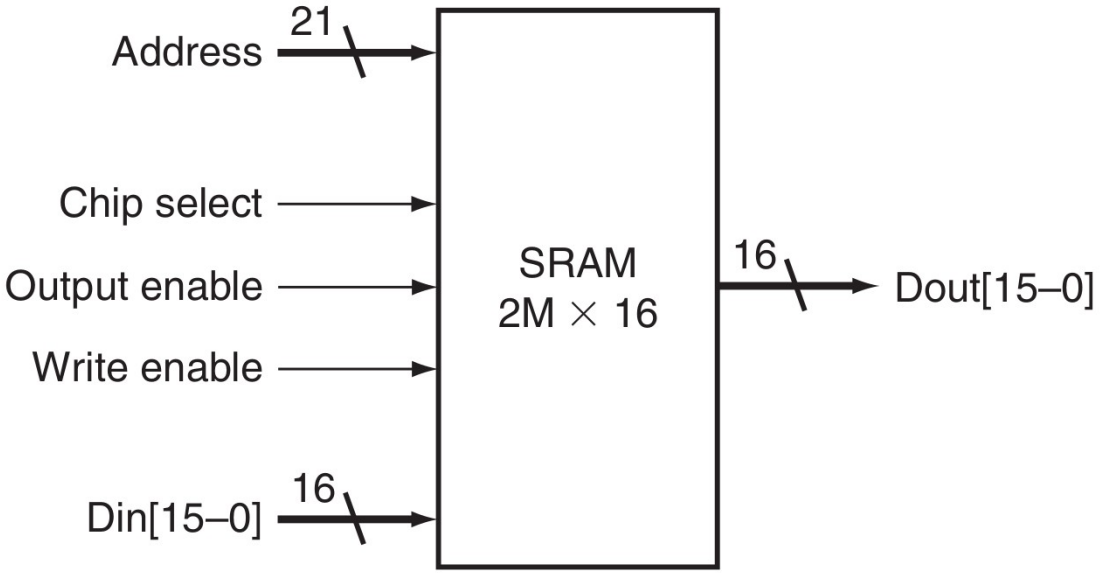
MIPS Datapath



SRAM and DRAM

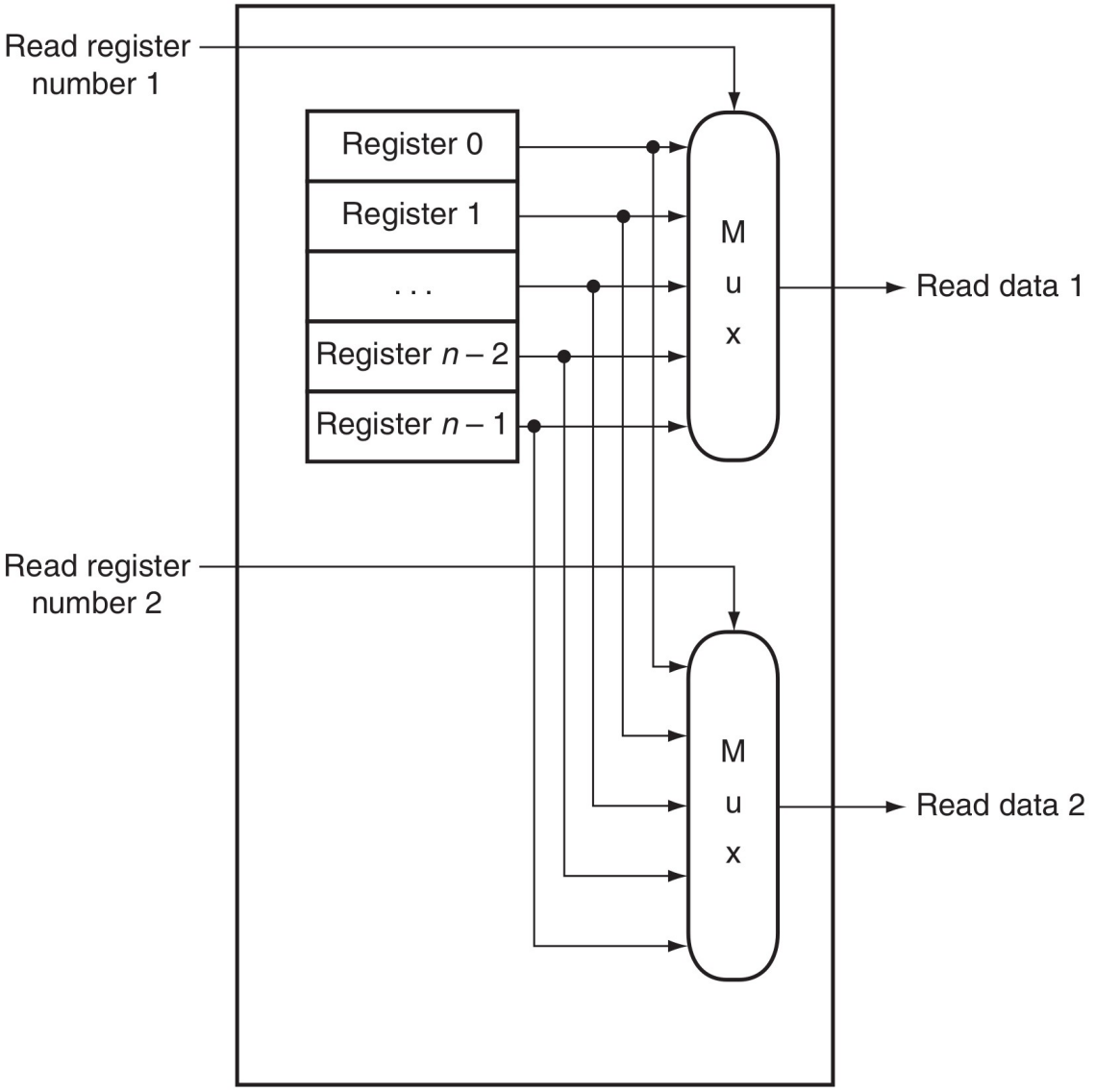
SRAM (Static Random Access Memory)

- Chip select to enable read or write
- Output enable to read



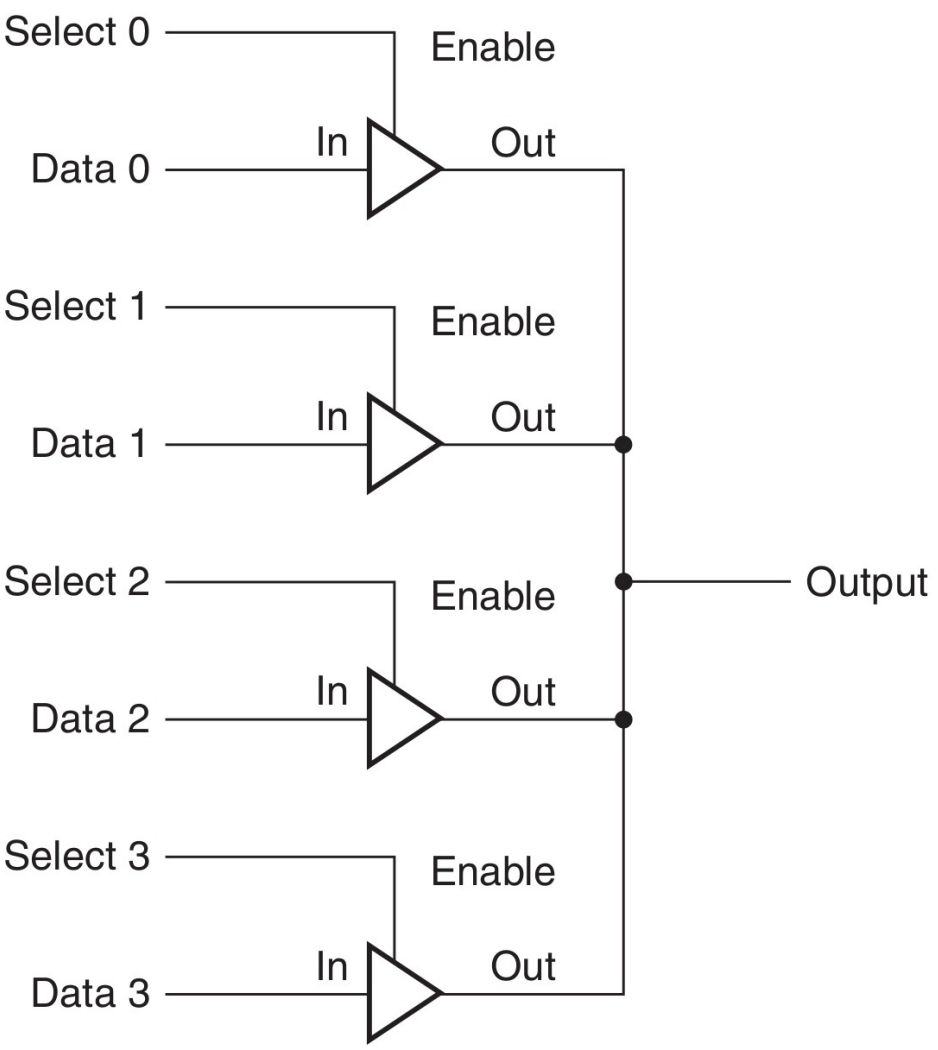
Register file vs memory

- 32-to-1 multiplexor

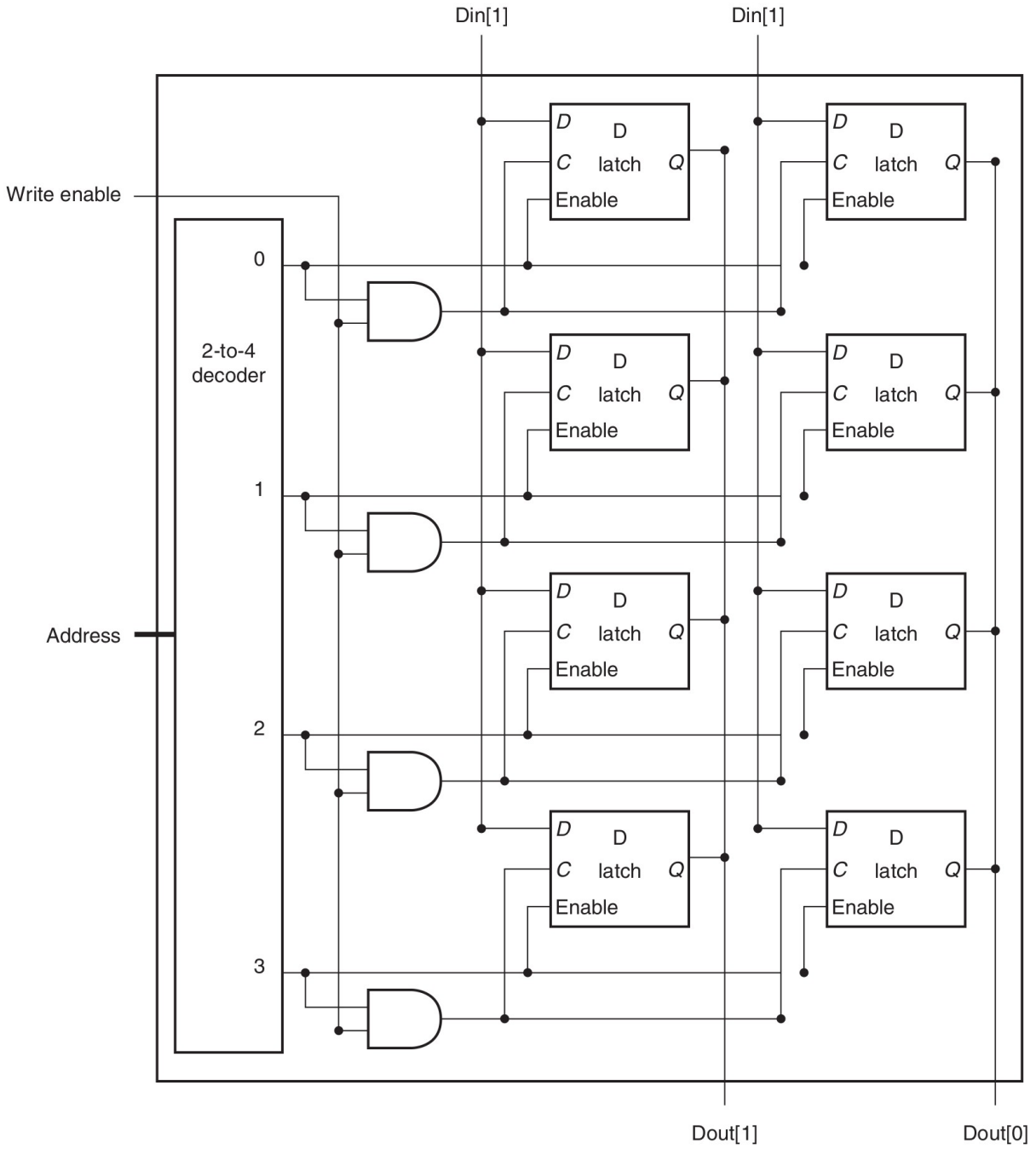


Three-state buffer

- 64K to 1 multiplexors are not practical
- Shared bit line instead
- Output
  - Asserted, deasserted or high-impedance

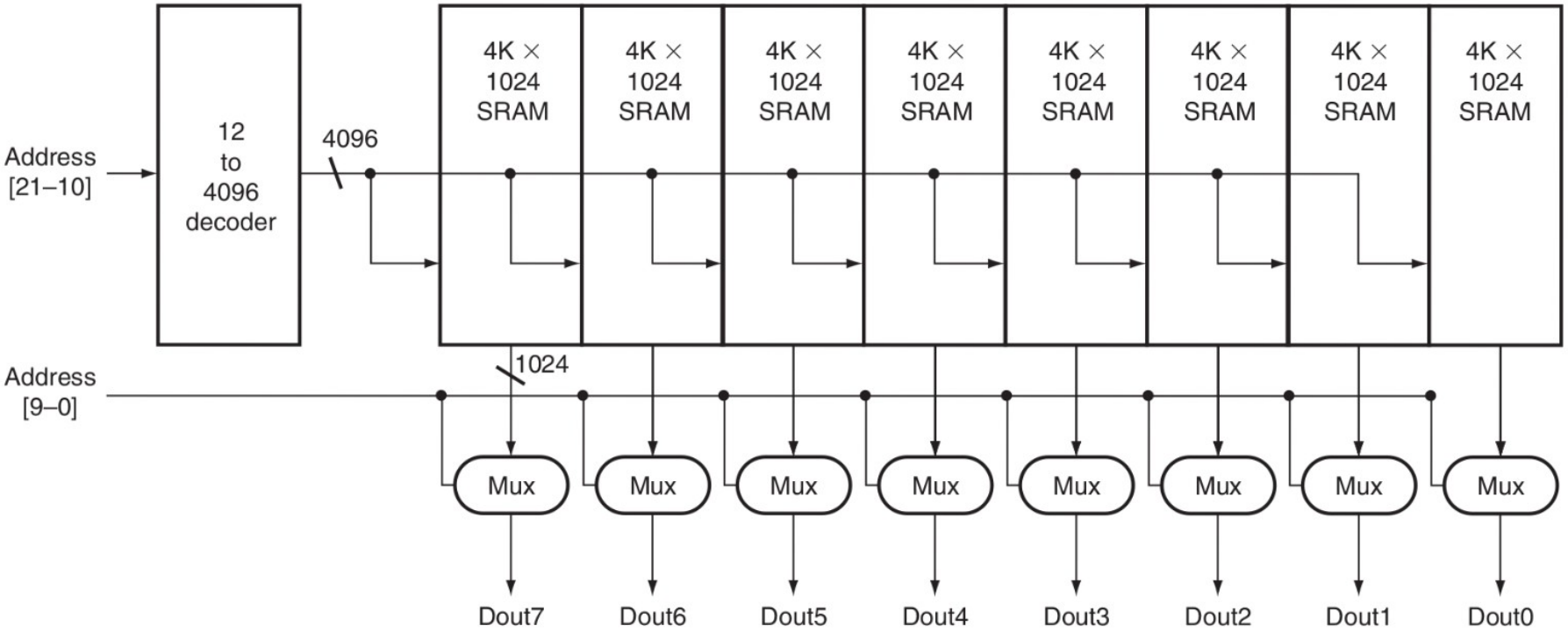


- 4 x 2 SRAM


Din[1]
Din[1]
Write enable
Address
2-to-4
decoder
0
1
2
3
D
C
Enable
D
latch
Q
Dout[1]
Dout[0]

4M x 8 SRAM

- Array of 4K x 1024 arrays



DRAM

- SRAM
  - 4-6 transistors
- DRAM
  - 1 transistor

DRAM cell

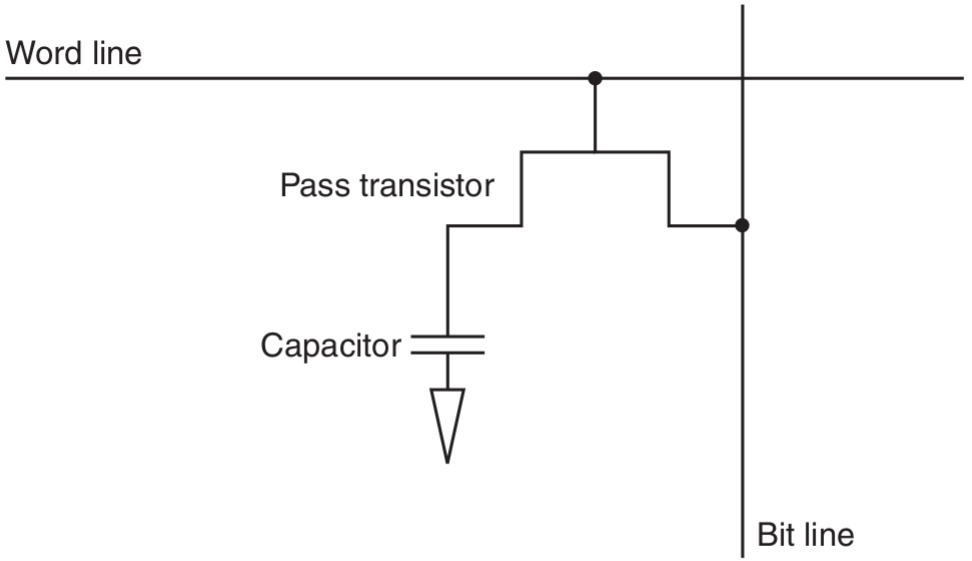


FIGURE B.9.5 A single-transistor DRAM cell contains a capacitor that stores the cell contents and a transistor used to access the cell.

4M x 1 DRAM cell

- 2048 x 2
  array

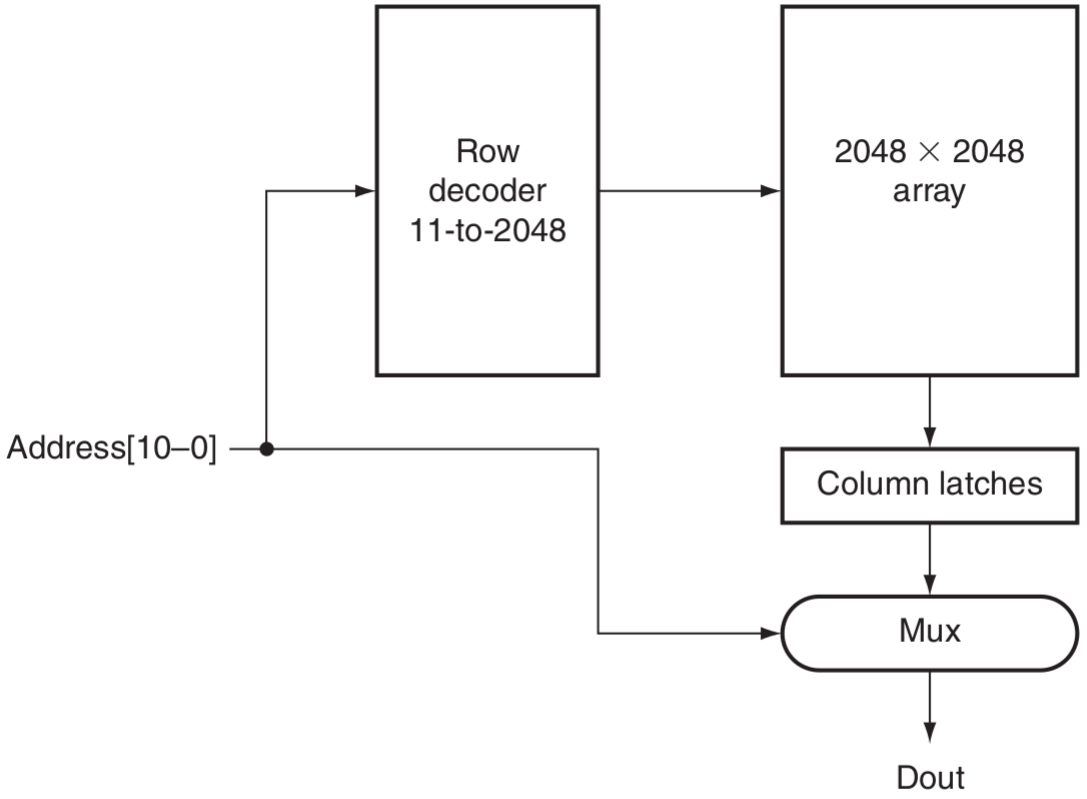


FIGURE B.9.6 A 4M × 1 DRAM is built with a 2048 × 2048 array. The row access uses 11 bits to select a row, which is then latched in 2048 1-bit latches. A multiplexor chooses the output bit from these 2048 latches. The RAS and CAS signals control whether the address lines are sent to the row decoder or column multiplexor.

Error correction

- Parity code
  - Counts number of 1s in a word
  - Parity bit (1 for odd, 0 for even)
  - Detects 1 bit error
  - Hence error detection code (EDC)
- Error correction codes are also used
  - 7-8 bits for every 128 bits of data
  - Correct 2-bit errors