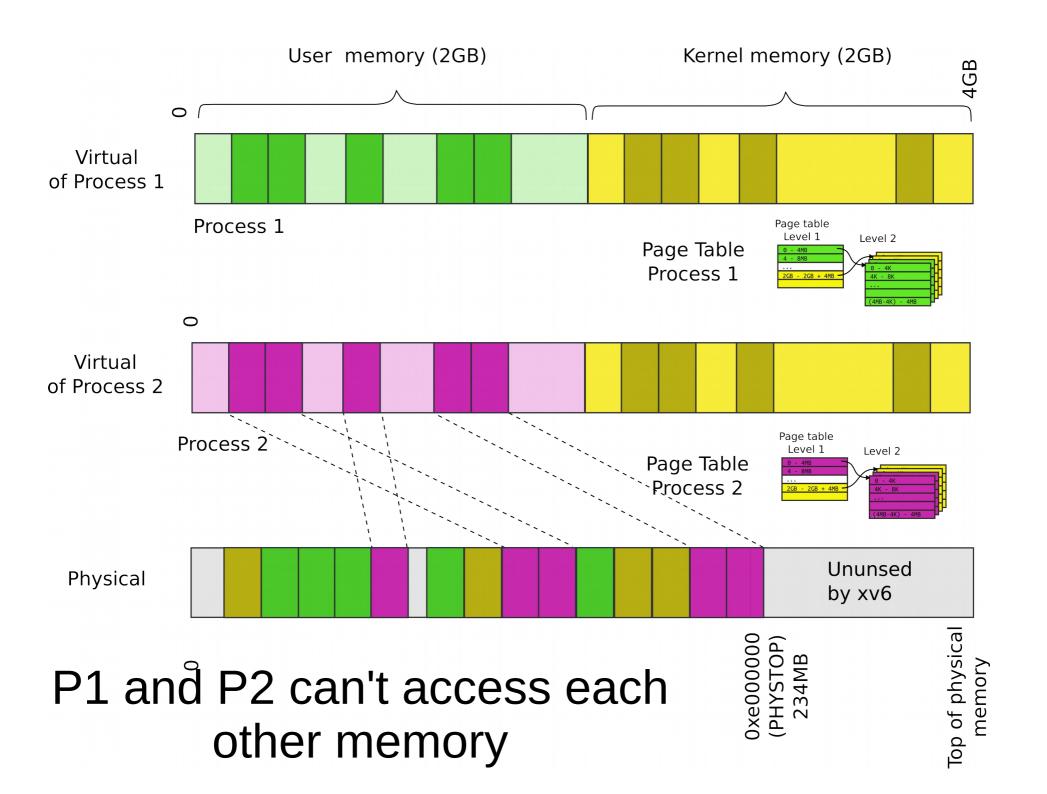
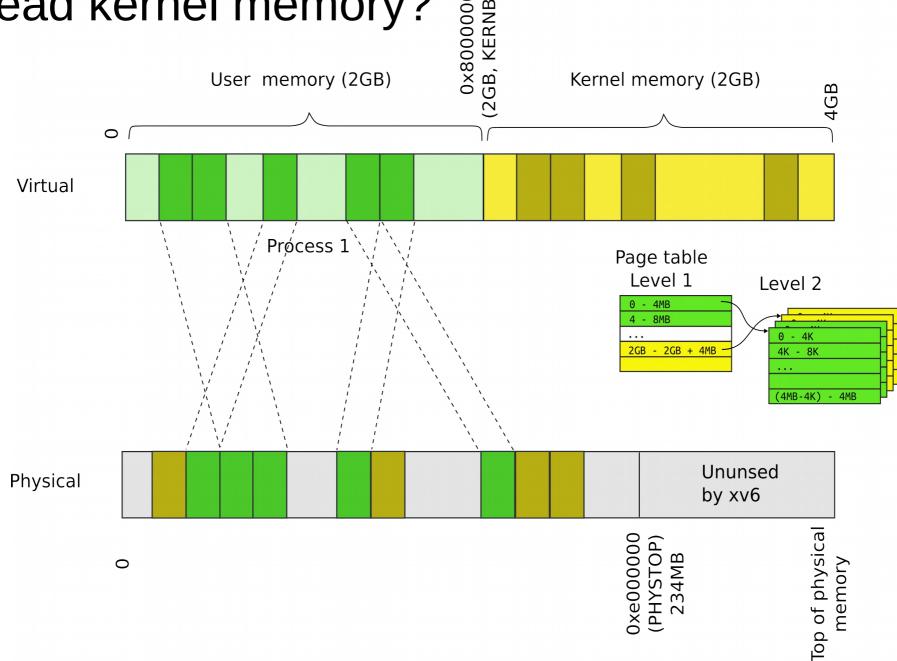
CS/EE3810: Computer Organization

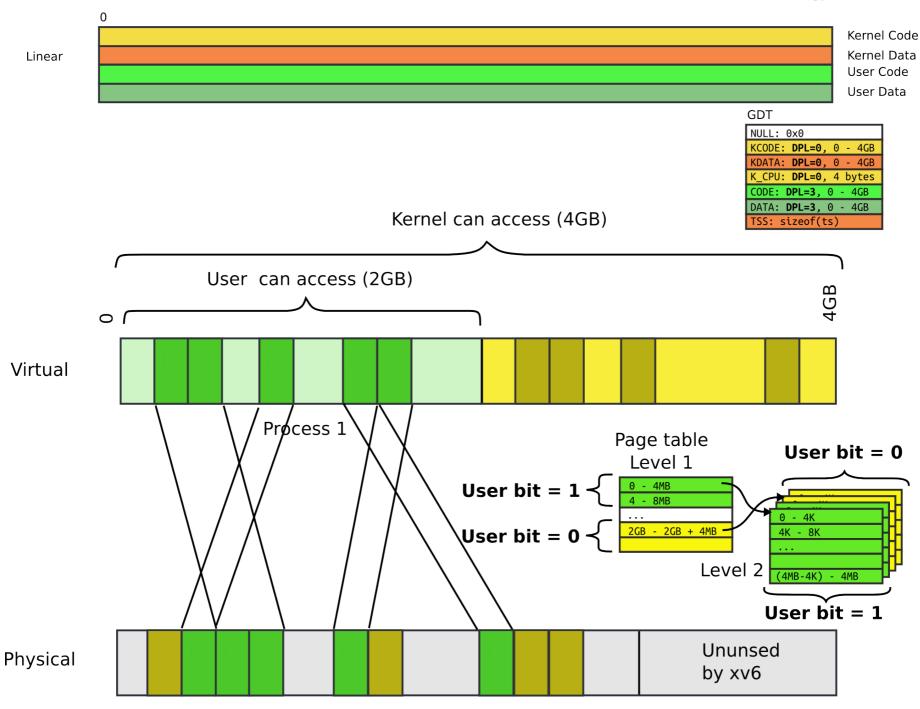
Lecture 18: Side channel attacks (Meltdown)

Anton Burtsev December, 2022



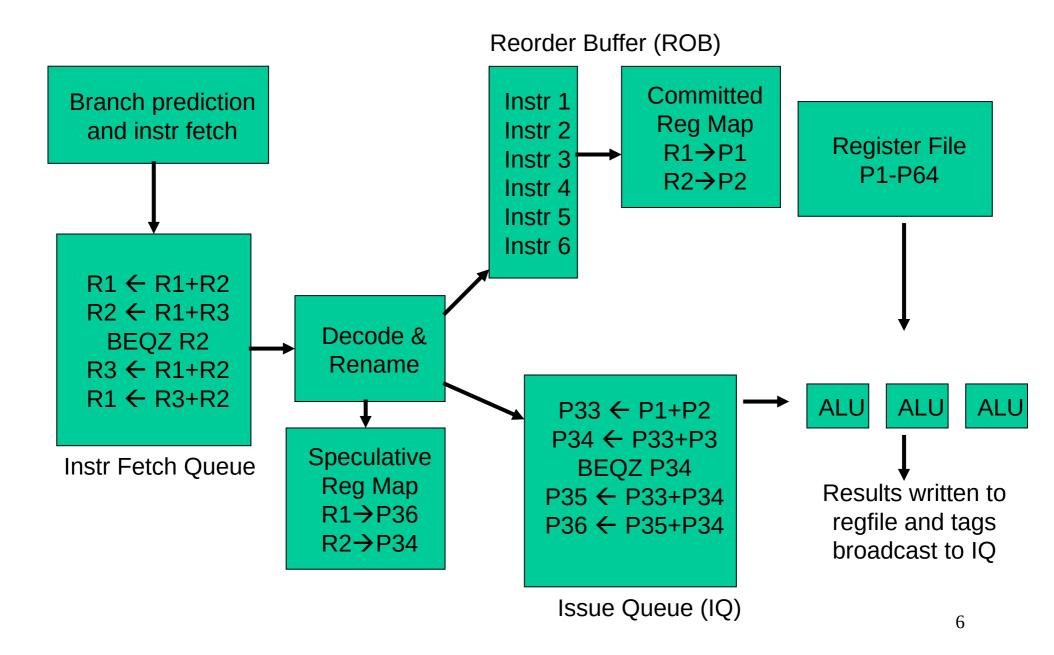
Recap: Can a process 0x80000000 (2GB, KERNBASE) read kernel memory? User memory (2GB)





Page tables and protection

The Alpha 21264 Out-of-Order Implementation

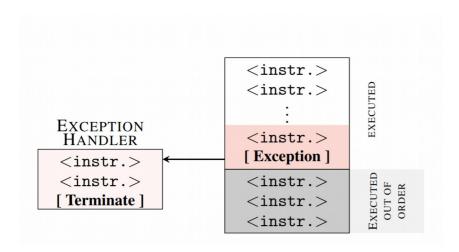


ITLB L1 Instruction Cache Branch Instruction Fetch & PreDecode Frontend Predictor Instruction Queue 4-Way Decode μOP Cache μOPs μ OP μΟΡ MUX Allocation Queue μΟΡ μΟΡ μΟΡ μ OP CDB Reorder buffer μΟΡ μΟΡ μΟΡ μΟΡ μΟΡ μΟΡ **Execution Engine** Scheduler μ OP μΟΡ Store data ALU, Branch Load data Load data ALU, FMA, ... ALU, AES, ... ALU, Vect, ... **Execution Units** Subsystem Load Buffer Store Buffer Memory STLB DTLB← L1 Data Cache L2 Cache

Skylake (simplified)

Exceptions and speculation

```
raise_exception();
// the line below is never reached
conditional access(probe_array[data * 4096]);
```



Core of the attack

```
1 ; rcx = kernel address, rbx = probe array
2 xor rax, rax
3 retry:
4 mov al, byte [rcx]
5 shl rax, 0xc
6 jz retry
7 mov rbx, qword [rbx + rax]
```

Cache access time

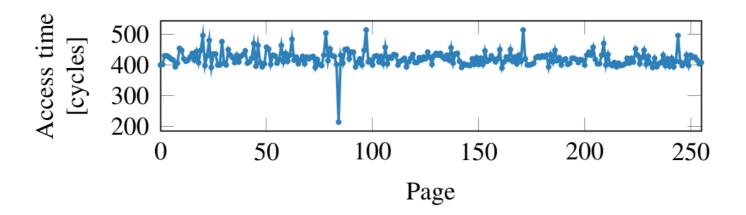


Figure 4: Even if a memory location is only accessed during out-of-order execution, it remains cached. Iterating over the 256 pages of probe_array shows one cache hit, exactly on the page that was accessed during the out-of-order execution.

• data = 84

Core of the attack

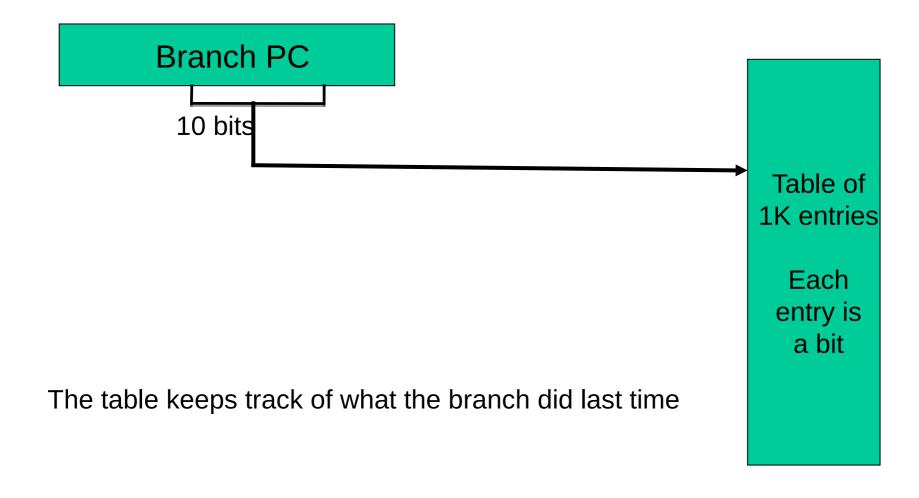
```
1 ; rcx = kernel address, rbx = probe array
2 xor rax, rax
3 retry:
4 mov al, byte [rcx]
5 shl rax, 0xc
6 jz retry
7 mov rbx, qword [rbx + rax]
```

Exception suppression

2-Bit Bimodal Prediction

- For each branch, keep track of what happened last time and use that outcome as the prediction
- What are prediction accuracies for branches 1 and 2 below:

Bimodal 2-Bit Predictor



Thank you!

Gadget

```
if (x < array1_size)
  y = array2[array1[x] * 4096];</pre>
```

Exceptions and speculation