IILM University, Greater Noida
Mid Semester Examination, Odd Semester-2024

Roll No.	

	Name of the School	School of Computer Science & Engineering	**Name of the Department**	Department of Computing and Security/ Department of Machine Learning and Data Science/ Department of Computer Applications
	Name of the Program	Bachelor of Technology	**Course Code-Course Name/ Name of faculty**	Digital Electronics and Computer Organization/ Mr. Awadhesh Kumar Maurya/Ms. Garima Kulshreshtha/Dr. Vanya Arun/Ms. Kshama Pandey/Dr. Akhilesh Mishra/Ms. Priyanka Agrawal/Dr. Damyanti Singh
	Session	2024-25	**Branch, Year & Semester**	CSE, 1st Year, 1st Semester
	Time/Maximum Marks	**90 Minutes/ 50**	**Set**	A
	Note: Attempt all questions.			

Q No.	QUESTIONS	MARKS	CO
	SECTION-A		
1	Explain De-Morgan's law.	2	1
2	Write the truth table of given Boolean expression: $Y = \overline{B}C + AB$	2	1
3	Write the minterms and maxterms of the following binary numbers: (a) 1011 (b) 1001	2	1
4	Write the truth table of 3 input XOR gate.	2	1
5	Draw logical diagram of the given Boolean expression: $Y = A\overline{B} + AB\overline{C}$	2	1
6	Write the output of the given Boolean expressions: (a) $A + A + A =$ (b) $A + \overline{A} =$ (c) $A + AB =$ (d) $A + 1 =$	2	1
7	Write the truth table of full adder.	2	2
8	Differentiate combinational and sequential circuits.	2	2
9	Explain 2:1 MUX.	2	2
10	Explain the design procedure of combinational circuits.	2	2
	SECTION-B		
11	Simplify the given Boolean function using K-map: $f(A, B, C, D) = \sum m(0,1,3,8,11,13,15) + d(2,6,10,14)$	5	1
12	Implement the following Boolean expression using NAND gates only: $Y = AB + \overline{B}C + A\overline{C}$	5	1
13	Simplify the given Boolean function using K-map: $f(A, B, C, D) = \prod M(2,3,7,8,11,12,13)$	5	1
14	Describe NOR gate as a universal gate.	5	1
15	Design and implement full subtractor.	5	2
16	Implement 2:4 decoder using logic gates.	5	2

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	Name of the Program	Bachelor of Technology	**Course Code-Course Name/ Name of faculty**	Digital Electronics and Computer Organization/ Mr. Awadhesh Kumar Maurya/Ms. Garima Kulshreshtha/Dr. Vanya Arun/Ms. Kshama Pandey/Dr. Akhilesh Mishra/Ms. Priyanka Agrawal/Dr. Damyanti Singh
	Session	2024-25	**Branch, Year & Semester**	CSE, 1st Year, 1st Semester
	Time/Maximum Marks	**90 Minutes/ 50**	**Set**	B
	Note: Attempt all questions.			

Q No.	QUESTIONS	MARKS	CO
	SECTION-A		
1	Write the truth table of given Boolean expression: $Y = \bar{A}C + BC$	2	1
2	Write the truth table of 3 input NAND gate.	2	1
3	Draw logical diagram of the given Boolean expression: $Y = \bar{B} + \bar{A}B\bar{C}$	2	1
4	Implement OR gate using NAND gates only.	2	1
5	Explain De-Morgan's law.	2	1
6	Write the output of the given Boolean expressions: (a) $A.A.A =$ (b) $A.\bar{A} =$ (c) $A + \bar{A}B =$ (d) $A.1 =$	2	1
7	Write the truth table of full subtractor.	2	2
8	Explain the design procedure of combinational circuits.	2	2
9	Explain 1:2 decoder.	2	2
10	Differentiate combinational and sequential circuits.	2	2
	SECTION-B		
11	Simplify the given Boolean function using K-map: $f(A, B, C, D) = \prod M(0,2,3,7,11,13,15) + d(1,6,10,14)$	5	1
12	Implement the following Boolean expression using NOR gates only: $Y = AB + \bar{B}C + A\bar{C}$	5	1
13	Simplify the given Boolean function using K-map: $f(A, B, C, D) = \sum m(0,2,3,8,10,11,12.15)$	5	1
14	Describe NAND gate as a universal gate.	5	1
15	Implement 4:1 MUX using logic gates.	5	2
16	Design and implement full adder.	5	2

IILM University, Greater Noida
End Semester Examination

Name: **Enrolment No:**				
	Name of the School	School of Computer Science & Engineering	**Name of the Department**	Department of Computing and Security/ Department of Machine Learning and Data Science/ Department of Computer Applications
	Name of the Program	Bachelor of Technology	**Course Code-Course Name/ Name of faculty**	UCS1001/Digital Electronics and Computer Organization/ Mr. Awadhesh Kumar Maurya/Ms. Garima Kulshreshtha/Dr. Vanya Arun/Ms. Kshama Pandey/Dr. Akhilesh Mishra/Ms. Priyanka Agrawal/Dr. Damyanti Singh/Dr. Sapna Chaudhary
	Session	2024-25	**Branch, Year & Semester**	CSE, 1st Year, 1st Semester
	Time/Max Marks	**3 Hours/100**	**Set**	A
	Note: **1) Attempt all sections (A, B & C).** **2) Attempt all questions in section A & B.** **3) Section C consists of 5 questions. One question from each unit. Questions may have internal choice from the same unit. Attempt all questions.**			

Q No.	QUESTIONS	MARKS	CO
	SECTION-A: Attempt all of the following questions in brief.		**(10x2=20)**
Q1(a)	Draw logical diagram of the given Boolean expression: $Y = A\bar{B}C + AB\bar{C}$.	2	1
(b)	Explain De-Morgan's law.	2	1
(c)	Write the differences between latches and flips flops?	2	2
(d)	Write the truth table of D flip flop.	2	2
(e)	What is the role of the Arithmetic and Logic Unit (ALU) in a computer system?	2	3
(f)	Define the term 'clock rate' in computer system and its significance in determining processor speed.	2	3
(g)	What do you mean by I/O organization?	2	4
(h)	Explain the hardware interrupt in brief.	2	4
(i)	What is a pipeline hazard?	2	5
(j)	Describe different operations of ALU.	2	5
	SECTION-B: Attempt all questions.		**(5x6=30)**
Q2(a)	Simplify the given Boolean function using K-map: $f(A, B, C, D) = \sum m(2,3,5,8,10,13,15) + d(1,6,11,14)$.	6	1
(b)	Explain the Logic diagram and truth table of JK flip-flop?	6	2
(c)	What are memory locations and addresses in computer systems? Describe how they are used in memory operations	6	3

(d)	Explain how I/O devices can be accessed. Also, discuss different I/O techniques.	6	4
(e)	Explain the Design of ALU in detail.	6	5
SECTION-C: Attempt all questions. Attempt any one part of each question.			**(5x10=50)**
Q3(a)	Implement the following Boolean expression using NAND gates only: $Y = AC + A\overline{B} + B\overline{C}$.	10	1
	OR		
Q3(b)	Simplify the given Boolean function using K-map: $f(A, B, C, D) = \prod M\,(0,2,3,7,8,11,13,14,15)$.		
Q4(a)	Draw and explain the operation of SR LATCH using NAND gates?	10	2
	OR		
Q4(b)	Explain a decoder circuit with suitable logic diagram and truth table		
Q5(a)	Describe the basic types of machine instructions in computer systems based on address formats. Provide examples for each type, including zero-address, one-address, two-address, and three-address instructions.	10	3
	OR		
Q5(b)	Discuss the different functional units of a basic computer and explain how these units interact with each other through the bus structure.		
Q6(a)	Draw and explain the block diagram of the DMA Controller.	10	4
	OR		
Q6(b)	What is interrupt? Explain its types in detail. Also, discuss the process of execution of an interrupt.		
Q7(a)	Describe pipeline process in a computer architecture. Define throughput and speedup performance factors**.**	10	5
	OR		
Q7(b)	What is the need of Cache memory? Explain various mapping techniques associated with Cache memory.		

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	Name of the Program	Bachelor of Technology	**Course Code- Course Name/ Name of faculty**	UCS1001/Digital Electronics and Computer Organization/ Mr. Awadhesh Kumar Maurya/Ms. Garima Kulshreshtha/Dr. Vanya Arun/Ms. Kshama Pandey/Dr. Akhilesh Mishra/Ms. Priyanka Agrawal/Dr. Damyanti Singh/Dr. Sapna Chaudhary
	Session	2024-25	**Branch, Year & Semester**	CSE, 1st Year, 1st Semester
	Time/Max Marks	**3 Hours/100**	**Set**	B
	Note: **1) Attempt all sections (A, B & C).** **2) Attempt all questions in section A & B.** **3) Section C consists of 5 questions. One question from each unit. Questions may have internal choice from the same unit. Attempt all questions.**			

Q No.	QUESTIONS	MARKS	CO
	SECTION-A: Attempt all of the following questions in brief.		**(10x2=20)**
Q1(a)	Implement OR gate using NAND gates only.	2	1
(b)	Write the truth table of given Boolean expression: $Y = \overline{A}C + ABC$.	2	1
(c)	Write the difference between combinational and sequential circuit.	2	2
(d)	Write the truth table of clocked T- Flip Flop?	2	2
(e)	What is an instruction in a computer system, and how is it executed?	2	3
(f)	What are addressing modes in computing? Provide two examples.	2	3
(g)	What is an interrupt?	2	4
(h)	Explain the operation of the cache.	2	4
(i)	What is cache memory?	2	5
(j)	Explain process of pipelining.	2	5
	SECTION-B: Attempt all questions.		**(5x6=30)**
Q2(a)	Describe NAND gate as a universal gate.	6	1
(b)	Design a 4:1 multiplexer. How many input line and selection lines are required for 4:1MUX.	6	2
(c)	Explain the concept of bus structure in a computer system. Why is it essential for connecting different functional units?	6	3
(d)	In cycle-stealing data transfer mode (DMA), the device can make one or two transfers; and comment on them with proper justification.	6	4

(e)	Describe pipeline technique and pipeline performance in detail.	6	5
	SECTION-C: Attempt all questions. Attempt any one part of each question.		**(5x10=50)**
Q3(a)	Simplify the given Boolean function using K-map: $f(A, B, C, D) = \prod M\,(1,2,3,7,8,11,13) + d(0,6,10,14,15)$.	10	1
	OR		
Q3(b)	Implement the following Boolean expression using NOR gates only: $Y = AC + \overline{B}C + AB$.		
Q4(a)	Explain the Logic diagram and truth table of Clocked SR flip-flop.	10	2
	OR		
Q4(b)	Explain an Encoder circuit with suitable example.		
Q5(a)	Describe the process of instruction execution and straight-line sequencing. How the concepts of branching impact the program flow?	10	3
	OR		
Q5(b)	Explain the different types of addressing modes used in computer systems. Describe each mode in detail with examples.		
Q6(a)	Discuss the interrupt in the processor's context and explain its classifications. Also discuss, how interrupts can be enabled or disabled?	10	4
	OR		
Q6(b)	What are peripheral devices? Explain it in detail. Also, discuss I/O address lines.		
Q7(a)	Discuss the different mapping techniques used in Cache memory with their merits and demerits.	10	5
	OR		
Q7(b)	Describe different operations of ALU in detail.		