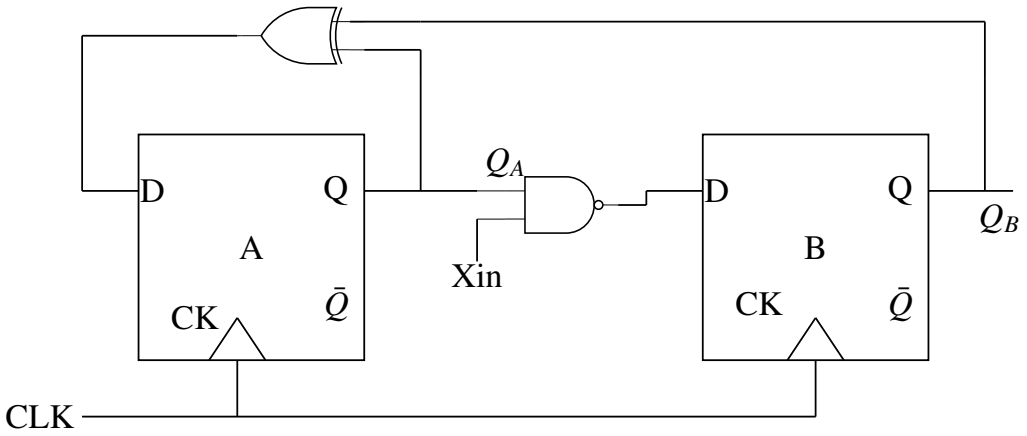
1. A finite state machine (FSM) is implemented using the D flip-flops A and B, and logic gates, as shown in the figure below. The four possible states of the FSM are $Q_A Q_B = 00, 01, 10$ and 11.



Assume that X_{IN} is held at a constant logic level throughout the operation of the FSM. When the FSM is initialized to the state $Q_A Q_B = 00$ and clocked, after a few clock cycles, it starts cycling through

(a) all of the four possible states if $X_{IN} = 1$

(b) three of the four possible states if $X_{IN} = 0$

(c) only two of the four possible states if $X_{IN} = 1$

(d) only two of the four possible states if $X_{IN} = 0$

(GATE EC 2017)